

When and How to Supply an External Bias for Buck Controllers – Part 2



Mathew Jacob

In [part 1](#) of this series, I discussed the need for external bias and under what conditions you need to consider it. In this installment, I will look at whether you can apply external bias to any controller.

As a rule of thumb, you cannot apply external bias to controllers that have a current limit for the control field-effect transistor (FET) (also known as the high-side FET). It boils down to how the current limit is implemented.

Let's look at a couple of examples. The first device is the LM3495, an emulated peak-current-mode buck controller. On first glance, it seems feasible that you can apply external bias on the V_{IN} pin.

Reading through the data sheet, however, there is a section called High-Side Current Limit. A comparator monitors the voltage across the high-side FET when it is on. If the drain-to-source voltage of the high-side FET exceeds 500mV while the FET is on, the LM3495 will immediately enter hiccup mode. A 200ns blanking period after the high-side FET turns on prevents switching transient voltages from tripping the high-side current limit without cause.

Now, how is this voltage across the high-side FET actually monitored? The comparator has two inputs. The first input is the SW pin and the second input is the V_{IN} pin. The assumption is that the drain of the high-side FET and V_{IN} pin are always at one potential.

This configuration saves a pin, but it makes the external bias problematic. Let's say that you apply 5V as the external bias to the V_{IN} pin. The input voltage is 3.3V, applied to the drain of the high-side FET. This causes a 1.7V difference across the comparator looking for 500mV, so the controller enters hiccup mode.

The next device example is the LM27403. Looking through the data sheet, there is no current sensing for the high-side FET. Thus, you can use this device for supplying external bias to the VDD pin in low V_{IN} applications.

How did I know to apply the external bias to the VDD pin? Let's look at the block diagram of the device shown in [Figure 1](#). Take note of the supply voltage shown for the low-side FET drive circuit; in this case, it's VDD. If you look at the application circuit in [Figure 2](#) you'll see where CBOOT is connected through the diode. For the LM27403, it is also VDD. Thus, you can determine that VDD is the right pin with which to apply the external bias.

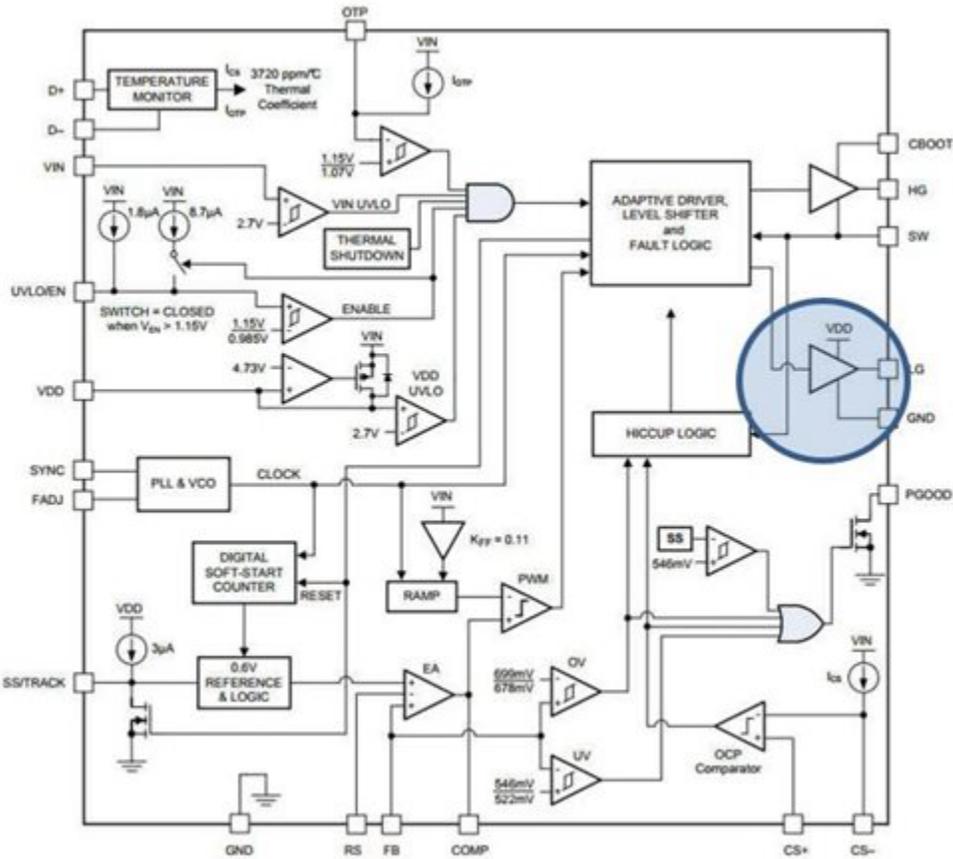


Figure 1. Block Diagram Showing VDD

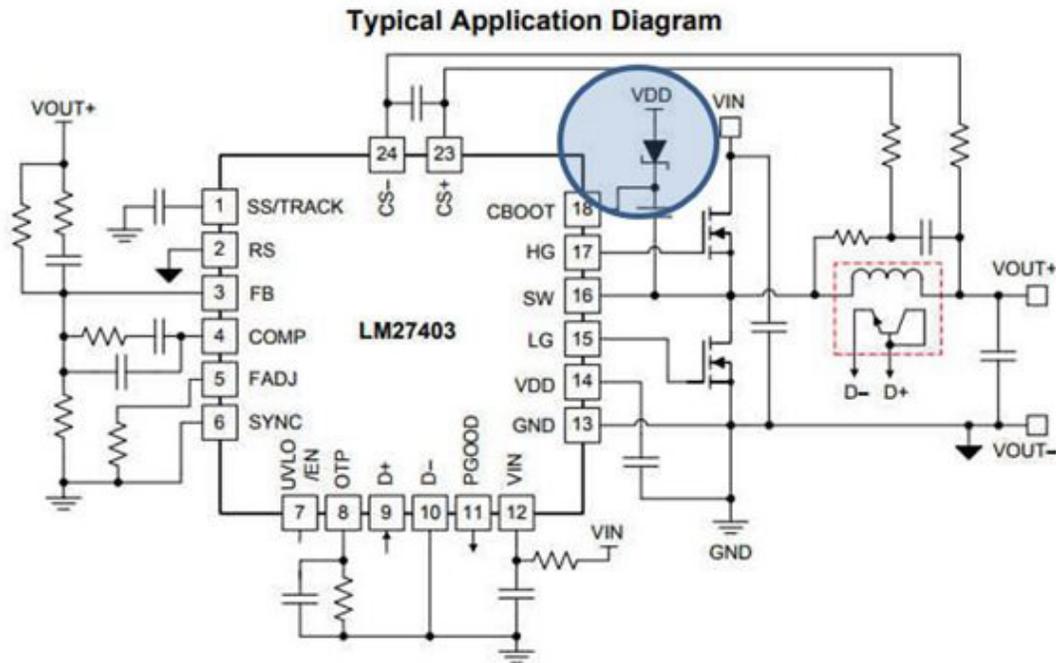


Figure 2. Application Circuit Showing VDD

Now the question is how to determine what value of voltage is OK to apply at the VDD pin. For this, you need to refer to the absolute maximum ratings of the VDD pin and make sure that the external bias applied does not violate this rating. Looking at the LM2403 data sheet, the absolute maximum for VDD is 6V and the recommended operating maximum is 5.5V.

5V is a common rail on boards and would serve as an appropriate bias voltage. The bias voltage needs to be a regulated voltage in order to not violate the absolute maximum ratings of the VDD pin.

In part 3 of this series, I will explore ways to generate your own external bias voltage (in the event that 5V rails are not available) by using charge-pump schemes from the very supply to which you need to supply the external bias.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated