*Technical Article*
# *DC/DC Converter Datasheets – System Efficiency Demystified*

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**TEXAS INSTRUMENTS**

Akshay Mehta

With the variety of regulators on the market, it can be difficult to choose a DC/DC regulator. Most automotive applications require high efficiency over the entire load range since they're running from the battery. But then again, many industrial applications require good efficiency at high loads and efficiency at light loads is not very important. Understanding the losses in a DC/DC regulator is therefore important. Reading the efficiency curves in DC/DC converter data sheets also generates a few questions, such as "Why is the efficiency at light loads low?" and "Why does the efficiency dip at heavy loads?" In this blog series, I will attempt to deconstruct system efficiency into different component losses using the SIMPLE SWITCHER® LM2673 3A step-down voltage regulator as an example.

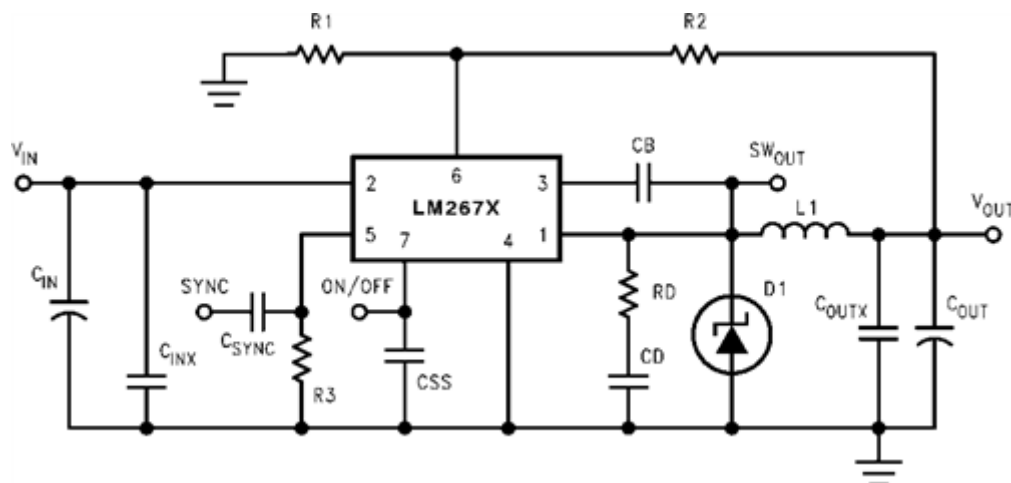Figure 1 shows the evaluation module (EVM) schematic.



**Figure 1. Design Schematic**

**Gate Charge and IC Losses**

In a typical nonsynchronous buck regulator such as the LM2673, the power-dissipating components are the IC itself, the inductor and the catch diode. The root-mean-square (RMS) currents through the input and output capacitors and the parasitic equivalent series resistance (ESR) are very low; thus you can ignore the losses in those components.

Due to their construction, every MOSFET has some parasitic capacitance between its terminals. They are the gate-drain capacitance ($C_{GD}$), gate-to-source capacitance ($C_{GS}$) and drain capacitance ($C_{DS}$), as shown in Figure 1. The capacitance values differ based on MOSFET size, fabrication and other process parameters. Unlike in an ideal MOSFET – where there are zero transition times – the presence of these parasitic capacitances introduces finite switching times, as shown in Figure 2.
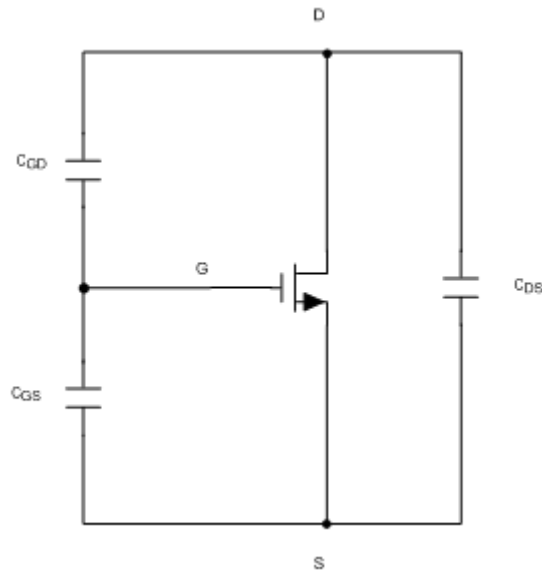
**Figure 2. MOSFET Parasitic Capacitances**

The finite switching times, as shown in Figure 3, are a result of the charging and discharging of the input capacitance ($C_{ISS}$). The input capacitance is basically the addition of $C_{GS}$ and the Miller capacitance ($C_{GD}$). The gate charge ($Q_G$) is the addition of the gate-to-source charge ($Q_{GS}$) and the gate-drain charge ($Q_{GD}$). The gate charge of the MOSFET is the charge needed to completely turn the MOSFET on.
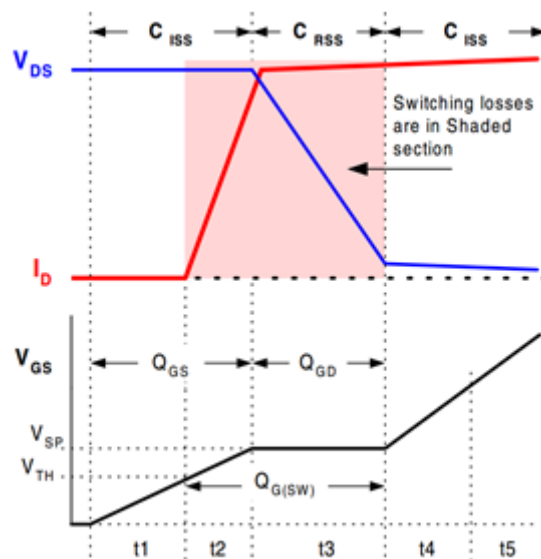


**Figure 3. Gate Charge and Miller Plateau**

The MOSFET drivers provide the current ($I_{CC}$) which you can estimate using Equation 1:

$$I_{CC} = Q_G * F_{SW} \qquad (1)$$

Where, $F_{SW}$ is the switching frequency of the DC/DC regulator.

For a converter like the LM2673, which has an integrated high-side MOSFET, the data sheet doesn't list parameters like $Q_G$. Therefore, you'll need to estimate the $I_{CC}$ in a different way: on the lab bench. With the device enabled and the load disconnected, measure the input current. Without a connected load, this input current measurement is essentially the $I_{CC}$ current measurement. The current $I_{CC}$ is also called the operating quiescent current. Please refer to the link in the 'Additional Resources' section to learn more.

For more accurate calculations, you can use TI's WEBENCH® Power Designer software. WEBENCH Power Designer has information on all internal MOSFET parameters and therefore can take those into consideration while calculating losses.

As you can see from Equation 1, the current is directly proportional to the switching frequency ($F_{SW}$). Since the MOSFET driver is providing this current, there are losses in the driver. The driver voltage ($V_{CC}$) is set by the internal low-dropout regulator (LDO). The losses in the driver are expressed as shown in Equation 2:

$$P_{Driver} = I_{CC} * V_{CC} \qquad (2)$$

Since the LDO internal to the DC/DC regulator provides this current, there will be power dissipation in the LDO as well. This power dissipation is expressed as Equation 3:

$$P_{LDO} = (V_{IN} - V_{CC}) * I_{CC} \qquad (3)$$

If you add up Equations Equation 2 and Equation 3, you'll get the total power dissipation of the LDO and the driver (Equation 4):

$$P_{driver\_LDO} = V_{IN} * I_{CC} \qquad (4)$$

Therefore, with higher input voltages, the loss increases. Also, the gate charge directly affects the switching losses. If the internal MOSFET has larger parasitic capacitances, then the resulting gate charge will be larger; the time spent in the switch transition will also be a bit longer. This will consequently increase the switching losses.

In the next installment of this series, I'll explain how the gate charge is related to the switching losses in the MOSFET, how the light load efficiency is dependent on these losses, and how the total losses affect the conduction losses and overall efficiency of a DC/DC regulator.

### Additional Resources

- The current $I_{CC}$ is also called the operating quiescent current. Read "DC/DC converter datasheets - Quiescent current" to learn more.
- Start a design now with WEBENCH Power Designer.
- Get more information on TI's extensive portfolio of SIMPLE SWITCHER DC/DC regulators.

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