Application Report
SWCA099A–April 2011–Revised July 2011

TWL6030 PCB Guidelines

ABSTRACT

This document describes the constraints and points for special layout considerations when designing with the TWL6030. The TWL6030 is an analog device containing several blocks that have different constraints when designing the board layout. This guide brings a better understanding for some of these constraints and provieds examples to explain of how it can be done.

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1 Introduction

The guide is build-up as a design process and starts with:

- Definition of the PCB
- Division of the signals into groups; requirements and constraints for each group are described.
- Placement of external components
- Use of tunnels for shielding

Design example description:

- PCB build-up

2 Component Description

The TWL6030 is an integrated power-management IC available in an nFBGA package, 7.0 mm x 7.0 mm with a 0.4-mm ball pitch. The device provides seven configurable step-down converters and nine LDO regulators. The device integrates a switched-mode charger.

Figure 1 shows an overview of the TWL6030 features.

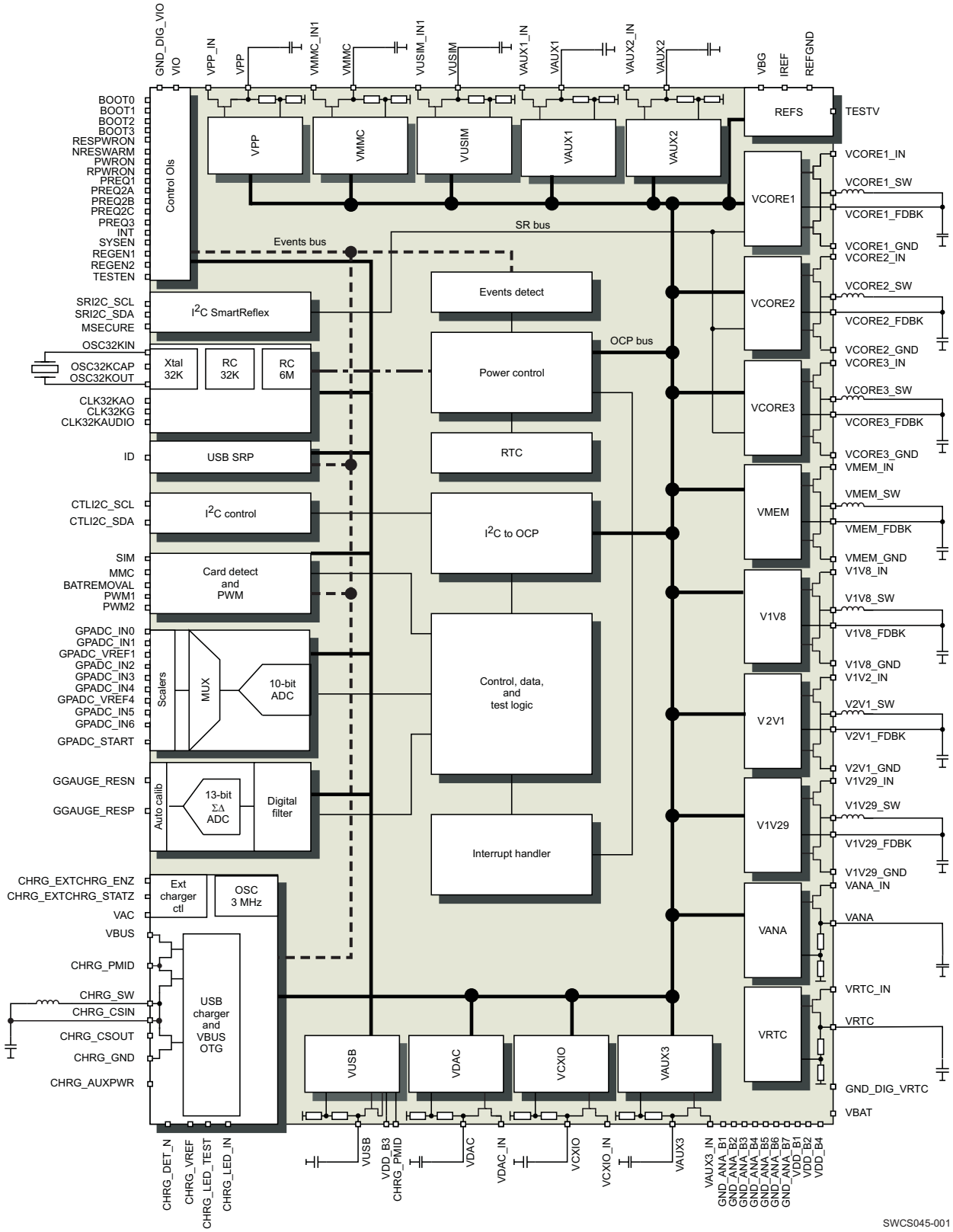

Figure 1. TWL6030 Features Overview

3 PCB Build-Up

Before the layout is started, the PCB build-up is needed to have a good strategy of what to place on what layer. There is a lot of theory to consider if a good and proper design is the goal. Because some of the theories conflict with each other, a complete waterproof strategy is not possible. Hence, the design of the PCB has trade-offs, the strategy is important to get the best possible design even with the compromises.

3.1 Routing Strategy

Routing on different board layers is an advantage for the CAD designer, but some constraints still must be addressed for a good design. Some signals (victims) are sensitive to influence from other signals (aggressors), and these victims must be kept a certain distance from the aggressors even if the signals are on different layers. One of the biggest misconceptions is that different layers for victims with respect to aggressors solves all problems; the PCB does not shield for capacitive or inductive coupling between signals, and here the designer must pay special attention, especially when planning the ground paths from different circuits.

3.1.1 PCB Strategy

When designing the PCB build-up a number of considerations must be taken into account:

- Number of layers
- Number of micro via layers
- Buried vias
- Stacked via layers

All the options are related to cost and hence there will be tradeoffs between the cost and the options chosen.

Figure 2 shows TWL6030 ball placement. This sets the requirement for PCB build-up to have either a number of levels of stackable vias or tracks between the balls (this second solution applies to the TWL6030). The absence of balls in certain places facilitates via placement under the package.

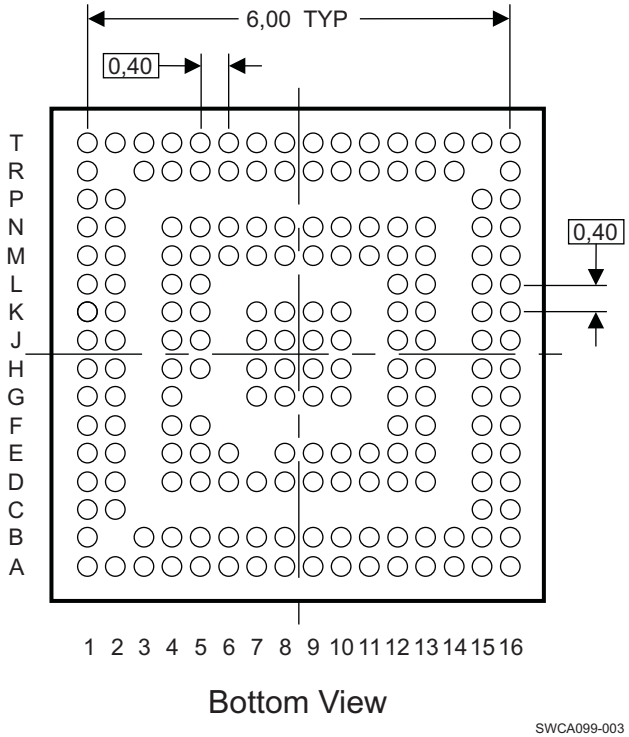

Figure 2. TWL6030 Ballout

The 0.4-mm pitch does not allow routing between balls using standard PCB manufacturing classes.

3.2 Layer Definition

Before the layout is started, the engineer and the PCB designer must consider the locations of the signals. The following can be used to understand the need for a routing strategy.

When sensitive signals and signals that can affect neighboring signals are present, it becomes very practical to have a prestudy of which signals to route where. One of the classic examples is the ground loop for high power consumption devices is surrounding some other signals that cannot withstand the interference from these signals.

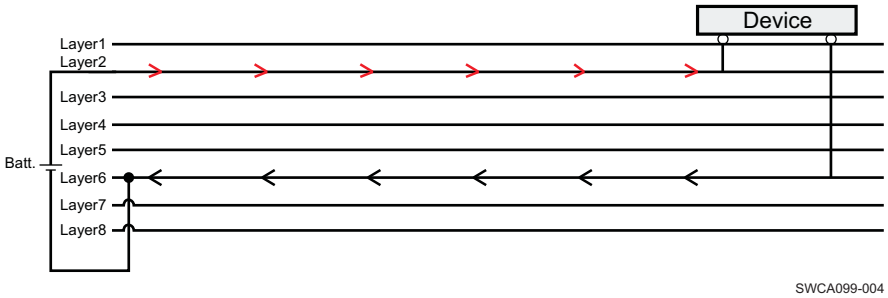

Figure 3. Ground Loop1

In Figure 3, signals are placed in the ground loop; layers 3, 4, and 5. This is not recommended. The signals in the ground loop will be affected by the flux which is generated by the current in the loop. This must be avoided especially with sensitive signals, such as oscillators.

The supply line and the ground path are both very crucial when the layout is made, both have the same importance. Supply has to be placed and calculated so that the flux is not affecting any signals that can not withstand it. The ground plane has to be very solid especially close to the supply trace. If not this is taken into account, then the risk for noise pollution is increased.

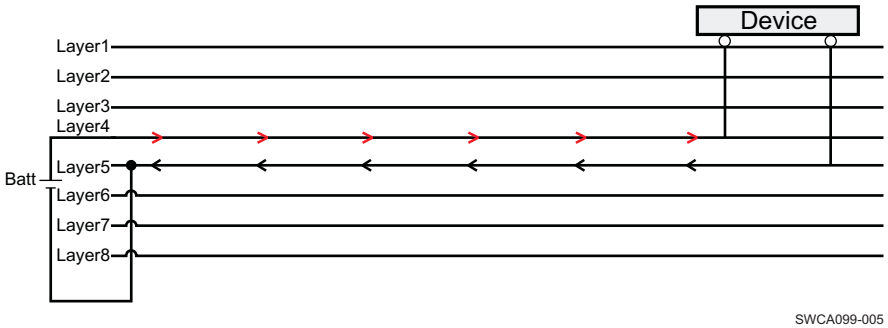

Figure 4. Ground Loop2

In Figure 4, the problem is solved by choosing other layers for supply and ground, no signal layer in between the ground loop. There is still some concern that must be taken into account:

- No sensitive signals in parallel with the supply line and the corresponding ground path

The reason is due to capacitive coupling across layers; the flux generated in either supply path or in ground path will affect the neighboring layers. The current in the ground path, when the frequency is high, will approach that of the supply path. Figure 5 shows the flux in the ground path, this flux cloud is affected by frequency and current level.

The width of the flux is determined by the frequency, low frequency (close to dc), high frequency, and the flux cloud will be very concentrated in parallel with the supply path.

The height is most controlled by the current level. Higher current is equal to higher flux density and therefore can impact other layers.

For both the frequency and the current, it is the transition period which is important. During this phase the current is shifting state and issues can arise due to the current change.

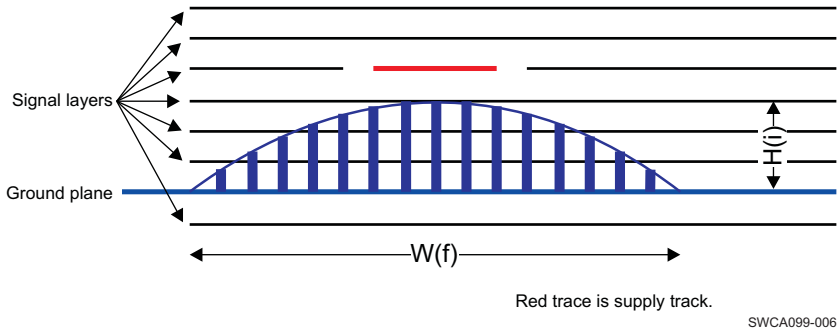

Figure 5. Frequency/Current Impact On Ground Plane

Red trace is the supply track.

3.3 PCB Electrical Characteristics

Table 1 details the maximum affordable RLC parasitics for each signal on the PCB.

Table 1. PCB Electrical Characteristics

Ball	R	L	C	Ball	R	L	C	Ball	R	L	C	Ball	R	L	C
CHRG_ AUXPWR	30	2	2	CLK32KAUDIO	200	15	35	SRI2C_SCL	200	15	35	GPADC_IN3	60	4	4
CHRG_ BOOT	100	10	4	CLK32KG	200	15	35	SRI2C_SDA	200	15	35	GPADC_IN4	60	4	4
CHRG_CSIN	100	10	4	OSC32KCAP	60	4	4	ID	60	4	4	GPADC_ VREF4	60	4	4
CHRG_ CSOUT	100	10	4	OSC32KIN	60	4	4	MMC	200	15	35	GPADC_IN5	60	4	4
CHRG_ DET_N	100	10	4	OSC32KOUT	60	4	4	SIM	200	15	35	GPADC_IN6	60	4	4
CHRG_ EXTCHRG_ ENZ	200	15	35	IREF	60	4	4	VANA	60	4	4	GPADC_ START	200	15	35
CHRG_ EXTCHRG_ STATZ	200	15	35	REFGND	10	1	4	VANA_IN	45	3	3	V1V29_ FDBK	60	4	4
CHRG_ LED_IN	100	10	4	VBG	60	4	4	VAUX1	15	1	1	V1V29_GND	10	10	1
CHRG_ LED_TEST	100	10	4	TESTEN	200	15	35	VAUX1_IN	30	2	2	V1V29_IN	10	1	4
CHRG_ PGND	10	10	1	TESTV	60	4	4	VAUX2	15	1	1	V1V29_SW	10	1	4
CHRG_ PMID	10	1	4	CTLI2C_ SCL	200	15	35	VAUX2_IN	30	2	2	V1V8_FDBK	60	4	4
CHRG_SW	10	1	4	CTLI2C_ SDA	200	15	35	VAUX3	15	1	1	V1V8_GND	10	10	1
CHRG_ VREF	60	4	4	INT	200	15	35	VAUX3_IN	30	2	2	V1V8_IN	10	1	4
VAC	60	4	4	BATREMOVAL	200	15	35	VCXIO	15	1	1	V1V8_SW	10	1	4
VBUS	10	1	4	BOOT0	200	15	35	VCXIO_IN	30	2	2	V2V1_FDBK	60	4	4
GND_ANA_B1	10	1	4	BOOT1	200	15	35	VDAC	60	4	4	V2V1_GND	10	10	1
GND_ANA_B2	10	1	4	BOOT2	200	15	35	VDAC_IN	45	3	3	V2V1_IN	10	1	4
GND_ANA_B3	10	1	4	BOOT3	200	15	35	VMMC	15	1	1	V2V1_SW	10	1	4
GND_ANA_B4	10	1	4	NRESPWRON	200	15	35	VMMC_IN1	30	2	2	VMEM_ FDBK	60	4	4
GND_ANA_B5	10	1	4	NRESWARM	200	15	35	VMMC_IN2	30	2	2	VMEM_GND	10	10	1
GND_ANA_B6	10	1	4	PREQ1	200	15	35	VPP	60	4	4	VMEM_IN	10	1	4
GND_ANA_B7	10	1	4	PREQ2A	200	15	35	VPP_IN	45	3	3	VMEM_SW	10	1	4
GND_DIG_ VIO	10	1	4	PREQ2B	200	15	35	VRTC	60	4	4	VCORE1_ FDBK	60	4	4
GND_DIG_ VRTC	10	1	4	PREQ2C	200	15	35	VRTC_IN	30	2	2	VCORE1_ GND	10	10	1
PBKG	10	1	4	PREQ3	200	15	35	VUSB	60	4	4	VCORE1_IN	10	1	4
VDD_B1	30	2	2	PWM1	200	15	35	VUSIM	15	1	1	VCORE1_ SW	10	1	4
VDD_B2	30	2	2	PWM2	200	15	35	VUSIM_IN1	30	2	2	VCORE2_ FDBK	60	4	4
VDD_B3	30	2	2	PWMFORCE	200	15	35	VUSIM_IN2	30	2	2	VCORE2_ GND	10	10	1
VDD_B4	30	2	2	PWRON	200	15	35	GGAUGE_ RESN	100	10	4	VCORE2_IN	10	1	4
VIO	30	2	2	REGEN1	200	15	35	GGAUGE_ RESP	100	10	4	VCORE2_ SW	10	1	4
VPROG	60	4	4	REGEN2	200	15	35	GPADC_IN0	60	4	4	VCORE3_ FDBK	60	4	4
VBACKUP	60	4	4	RPWRON	200	15	35	GPADC_IN1	60	4	4	VCORE3_ GND	10	10	1

Table 1. PCB Electrical Characteristics (continued)

Ball	R	L	C	Ball	R	L	C	Ball	R	L	C	Ball	R	L	C
VBAT	60	4	4	SYSEN	200	15	35	GPADC_ VREF1	60	4	4	VCORE3_IN	10	1	4
CLK32KAO	200	15	35	MSECURE	200	15	35	GPADC_IN2	60	4	4	VCORE3_ SW	10	1	4

Notes:

1. PCB RLC parasitics expressed in mΩ, nH, and pF, respectively.
2. Those parasitic extracted values have been used during TWL6030 IC design and presilicon verification phases.
3. They represent the PCB RLC parasitic, from the TWL6030 device balls up to the external connected components.
4. Those targets must be fulfilled during the PCB layout design phase, in order to meet TWL6030 full performances.
5. VMMC_IN2 and VUSIM_IN2 are spare inputs, not used in the current TWL6030 version.

4 Signal Grouping

4.1 Ground

4.1.1 Ground for Digital

Group	BGA Ball	Ball Name	Type
GND digital	M8	GND_DIG_VIO	Power
	G4	GND_DIG_VRTC	Power

4.1.2 Ground for DC/DC Power (Short, Thick Traces Required)

Group	BGA Ball	Ball Name	Type
GND DCDC	A5	CHRG_PGND_B1	Power
	A6	CHRG_PGND_B2	Power
	B6	CHRG_PGND_B3	Power
	B5	CHRG_PGND_B4	Power
	M16	V1V8_GND_B1	Power
	L16	V1V8_GND_B2	Power
	M15	V1V8_GND_B3	Power
	T12	VMEM_GND_B1	Power
	R12	VMEM _GND_B2	Power
	M1	VCORE1_GND_B1	Power
	L1	VCORE1_GND_B2	Power
	M2	VCORE1_GND_B3	Power
	H1	VCORE3_GND_B4	Power
	H2	VCORE3_GND_B5	Power
	T5	VCORE2_GND_B1	Power
	R5	VCORE2_GND_B2	Power
	H16	V1V29_GND_B1	Power
	H15	V1V29_GND_B2	Power
	E16	V2V1_GND_B1	Power
	E15	V2V1_GND_B2	Power

4.1.3 Main Analog Ground Plane

Group	BGA Ball	Ball Name	Type
GND power	N8	GND_ANA_B1	Power
	M10	GND_ANA_B2	Power
	E11	GND_ANA_B3	Power
	L13	GND_ANA_B4	Power
	D9	GND_ANA_B5	Power
	H4	GND_ANA_B6	Power
	G7	GND_ANA_B7	Power

4.1.4 Sensitive Ground (Isolate from Noisy Signals)

Group	BGA Ball	Ball Name	Type
GND signal	A9	REFGND_B1	Power
	F12	REFGND_B2	Power

4.1.5 Package Ground (Connect to Main Ground)

Group	BGA Ball	Ball Name	Type
GND	T1	PBKG_B11	Power
	T2	PBKG_B12	Power
	R1	PBKG_B13	Power
	H5	PBKG_B2	Power
	T16	PBKG_B31	Power
	T15	PBKG_B32	Power
	R16	PBKG_B33	Power
	A1	PBKG_B41	Power
	A2	PBKG_B42	Power
	B1	PBKG_B43	Power
	A16	PBKG_B51	Power
	B16	PBKG_B53	Power

4.2 Power

4.2.1 Power Input Lines

Group	BGA Ball	Ball Name	Type
Power input	J4	VPP_IN	Power
	N7	VAUX1_IN	Power
	R8	VAUX3_IN	Power
	N10	VAUX2_IN	Power
	J12	VMMC_IN1	Power
	K13	VMMC_IN2	Power
	F13	VCXIO_IN	Power
	D8	VUSIM_IN1	Power
	B7	VUSIM_IN2	Power
	H13	VDAC_IN	Power
	D10	VANA_IN	Power
	D11	VRTC_IN	Power
	K16	V1V29_IN_B1	Power
	K15	V1V29_IN_B2	Power
	T13	V1V8_IN_B1	Power
	T14	V1V8_IN_B2	Power
	R14	V1V8_IN_B3	Power
	T10	VMEM_IN_B1	Power
	R10	VMEM_IN_B2	Power
	T4	VCORE1_IN_B1	Power
	T3	VCORE 1_IN_B2	Power
	R3	VCORE 1_IN_B3	Power
	K1	VCORE 3_IN_B1	Power
	K2	VCORE 3_IN_B2	Power
	T7	VCORE 2_IN_B1	Power
	R7	VCORE 2_IN_B2	Power
	C15	V2V1_IN_B1	Power
	C16	V2V1_IN_B2	Power
	N9	VDD_B1	Power
	G13	VDD_B2	Power
	B9	VDD_B3	Power
	L4	VDD_B4	Power
	M9	VIO	Power
	E10	VBACKUP	Power
	C1	VBUS_B1	Power
	D1	VBUS_B2	Power
	C2	VBUS_B3	Power
	D2	VBUS_B4	Power
	E1	CHRG_PMID_B1	Power
	F1	CHRG_PMID_B2	Power
	E2	CHRG_PMID_B3	Power
	F2	CHRG_PMID_B4	Power
	E6	CHRG_AUXPWR	Power
	G2	CHRG_BOOT	Power

4.2.2 Power Switching Output Lines (Aggressors – Careful Routing Required)

Group	BGA Ball	Ball Name	Type
Power output	A3	CHRG_SW_B1	Power
	A4	CHRG_SW_B2	Power
	B4	CHRG_SW_B3	Power
	B3	CHRG_SW_B4	Power
	J16	V1V29_SW_B1	Power
	J15	V1V29_SW_B2	Power
	N16	V1V8_SW_B1	Power
	P16	V1V8_SW_B2	Power
	P15	V1V8_SW_B3	Power
	T11	VMEM_SW_B1	Power
	R11	VMEM_SW_B2	Power
	N1	VCORE1_SW_B1	Power
	P1	VCORE 1_SW_B2	Power
	P2	VCORE 1_SW_B3	Power
	T6	VCORE 2_SW_B1	Power
	R6	VCORE 2_SW_B2	Power
	J1	VCORE 3_SW_B1	Power
	J2	VCORE 3_SW_B2	Power
	D16	V2V1_SW_B1	Power
	D15	V2V1_SW_B2	Power

4.2.3 Power Passive Output Lines (IR Drops to be Considered)

Group	BGA Ball	Ball Name	Type
Power output	K4	VPP	Power
	T8	VAUX1	Power
	R9	VAUX3	Power
	T9	VAUX2	Power
	J13	VMMC	Power
	F15	VCXIO	Power
	B8	VUSIM	Power
	A7	VUSB	Power
	G15	VDAC	Power

4.2.4 Decoupling for Internal Functions

Group	BGA Ball	Ball Name	Type
	D7	VRTC	Power
	B10	VANA	Power

4.3 Sensitive Signals

4.3.1 Clock Signals

Group	BGA Ball	Ball Name	Type
Slow clock	E8	OSC32KCAP	Output
	A10	OSC32KIN	Input
	A8	OSC32KOUT	Output

4.3.2 Reference

Group	BGA Ball	Ball Name	Type
Reference	G12	VBG	Output
	H12	IREF	Output
	F5	CHRG_VERF	Input

4.3.3 Voltage Sense

Group	BGA Ball	Ball Name	Type
Voltage sense	E4	CHRG_CSIN	Input
	D4	CHRG_CSOUT	Input
	F16	V2V1_FDBK	Input
	G16	V1V29_FDBK	Input
	L15	V1V8_FDBK	Input
	R13	VMEM_FDBK	Input
	L2	VCORE 1_FDBK	Input
	R4	VCORE 2_FDBK	Input
	G1	VCORE 3_FDBK	Input
	D13	GGAUGE_RESN	Input
	E13	GGAUGE_RESP	Input
	B13	VBAT	Input
	F4	VAC	Input

4.3.4 GPADC Line

Group	BGA Ball	Ball Name	Type
GPADC	D12	GPADC_IN0	Input
	B11	GPADC_IN1	Input
	A11	GPADC_VREF1	Input
	B14	GPADC_IN2	Input
	A13	GPADC_IN3	Input
	B12	GPADC_IN4	Input
	A12	GPADC_VREF4	Input
	A14	GPADC_IN5	Input
	B15	GPADC_IN6	Input

4.4 Digital Signals

4.4.1 Dedicated Dynamic I/Os

Group	BGA Ball	Ball Name	Type
I/Os	H10	CLK32KAO	Output
	E9	CLK32KAUDIO	Output
	J10	CLK32KG	Output
	M4	CTLI2C_SCL	Input/Output
	N4	CTLI2C_SDA	Input/Output
	M13	SRI2C_SCL	Input/Output
	N13	SRSI2C_SDA	Input/Output
	K10	INT	Output

5 External Components Placement

Placement of external components must be done with engineering skills. The placement is expected to be affected by the mechanical dimension, and also the placement of the TWL6030. Placement of the TWL6030 must consider the distance to supplied devices (for example, the processor). The placement has requirements to placement of external components and also to the possibility to route power lines from the integrated PMU to power consumption devices, processors, etc.

When doing the calculation, consider that the tolerance on the DC/DC converter outputs is ±4%.

5.1 Recommended Manufacturer's Components List

Table 2 lists the recommended components.

Table 2. Recommended Components List

Module	Component	#	Manufacturer	Part Number	Value	Pack	Size (mm)
Input Power Supplies External Components							
PM / VBAT	V_{DD} tank capacitor	1	Murata	GRM188R60J106ME84L	10 µF	0603	1.6 x 0.8 x 0.8
PM / VBAT	V_{DD} tank capacitor	2	Taiyoyuden	JMK107BJ106	10 µF	0603	1.6 x 0.8 x 0.8
Backup	Condensator	1	Seiko Instruments	XH414H-IV01E	0.08 F		ø4.8, 1.4
Backup	Condensator	2	Matsushita (MEC)	EECEP0E223AN	0.022 F		
Crystal Oscillator External Components							
32 kHz	Crystal	1	Citizen	CM519	32.768 kHz		3.2 x 1.5 x 0.9
32 kHz	Crystal	2	Microcrystal	CC7V-T1A	32.768 kHz		
32 kHz	Crystal	3	Epson	FC135	32.768 kHz		
32 kHz	Crystal	4	NDK	NX3215SA	32.768 kHz		3.2 x 1.5 x 0.8
32 kHz	Supply decoupling	1	Murata	GRM155R61A105KE15D	1 µF	0402	1 x 0.5 x 0.5
32 kHz	Supply decoupling	2	Taiyoyuden	JMK105BJ105MV-F	1 µF	0402	1 x 0.5 x 0.5
32 kHz	Crystal decoupling	1	Murata	GRM1555C1H220JZ01	22 pF	0402	1 x 0.5 x 0.5
32 kHz	Crystal decoupling	2	AVX	04025A120JAT2A	12 pF	0402	1 x 0.5 x 0.5
Bandgap External Components							
Bandgap	Bias resistor	1	Rohm	0W06 1M 50ppm	1 MΩ	0402	1 x 0.5 x 0.5
Bandgap	Bias resistor	2	Vishay		1 MΩ	0603	1.6 x 0.8 x 0.8
Bandgap	Capacitor	1	Murata	GRM155R61C104K	100 nF	0402	1 x 0.5 x 0.5
Bandgap	Capacitor	2	KEMET	C0402C104K8PAC	100 nF	0402	1 x 0.5 x 0.5

Table 2. Recommended Components List (continued)

Module	Component	#	Manufacturer	Part Number	Value	Pack	Size (mm)
Gas Gauge External Components							
Gas gauge	Resistor	1	Cyntec	RL3720T-R010-FN	10 mΩ	0815	
GPADC External Components							
GPADC	NTC resistor	1	Murata	NCL15WB473F03RC	47 kΩ	0402	1 x 0.5 x 0.5
I²C External Components							
I²C I/F	Pullup resistor	1					
SMPS External Components							
SMPS	Input capacitor	1	Murata	GRM155R60J225ME15D	2.2 µF	0402	1 x 0.5 x 0.5
SMPS	Input capacitor	2	Taiyoyuden	JMK105BJ225MV-F	2.2 µF	0402	1 x 0.5 x 0.5
SMPS	Input capacitor	3	Murata	GRM155R60J475M	4.7 µF	0402	1 x 0.5 x 0.5
SMPS	Input capacitor	4	Taiyoyuden	JMK107BJ475KA-T	4.7 µF	0603	1.6 x 0.8 x 0.8
SMPS	Input capacitor	5	Murata	GRM155R60J335UE97	4.7 µF	0402	1 x 0.5 x 0.5
SMPS	Output capacitor	1	Murata	GRM188R60J106ME84L	10 µF	0603	1.6 x 0.8 x 0.8
SMPS	Output capacitor	2	Murata	GRM188R60J106UE82J	10 µF	0603	1.6 x 0.8 x 0.8
SMPS	Ferrite bead	1	Murata	BLM18SG700TN1D	–	0603	1.6 x 0.8 x 0.8
SMPS	Ferrite bead	2	Murata	BLM15PD121SN1	1300 mA	0402	1 x 0.5 x 0.5
SMPS	Ferrite bead	3	Murata	BLM18KG221SN1	2200 mA	0603	1.6 x 0.8 x 0.8
SMPS 0.6 A	Filter inductor	1	Murata	LQM2MPNR47NG0	0.47 µH	0806	2 x 1.6 x 0.9
SMPS 0.6 A	Filter inductor	2	Taiyoyuden	BR C1608T R45M	0.45 µH	0603	1.6 x 0.8 x 0.8
SMPS 0.6 A	Filter inductor (volume minimization)	3	Murata	LPQM21PN1R0MC0	1 µH	0805	2 x 1.25 x 0.55
SMPS 0.6 A	Filter inductor (performance maximization)	4	TDK	MLP2520S1R0M	1 µH	1008	2.5 x 2 x 1
SMPS 1.2 A	Filter inductor	1	Murata	LQM2HPNR56ME0	0.56 µH	2520	2.5 x 2 x 0.7
SMPS 1.2 A	Filter inductor (volume minimization)	2	Murata	LQM2MPN1R0NG0	1 µH	0806	2 x 1.6 x 1
SMPS 1.2 A	Filter inductor (performance maximization)	3	Murata	LQM32PN1R0MG0 (under development)	1 µH	1210	3.2 x 2.5 x 1
SMPS 1.5 A	Filter inductor (volume minimization)	1	Coilcraft	EPL2010-681ML	0.68 µH		2 x 2 x 1
SMPS 1.5 A	Filter inductor (performance maximization)	2	Murata	LQM32PN1R0MG0 (under development)	1 µH	1210	3.2 x 2.5 x 1
SMPS 2.0 A	Filter inductor (volume minimization)	1	Coilcraft	EPL2010-681ML	0.68 µH		2 x 2 x 1
SMPS 2.0 A	Filter inductor (performance maximization)	2	Murata	LQM32PN1R0MG0 (under development)	1 µH	1210	3.2 x 2.5 x 1

5.2 Placement Overview

Figure 6 shows an example of component placement on the SELAB daughterboard.

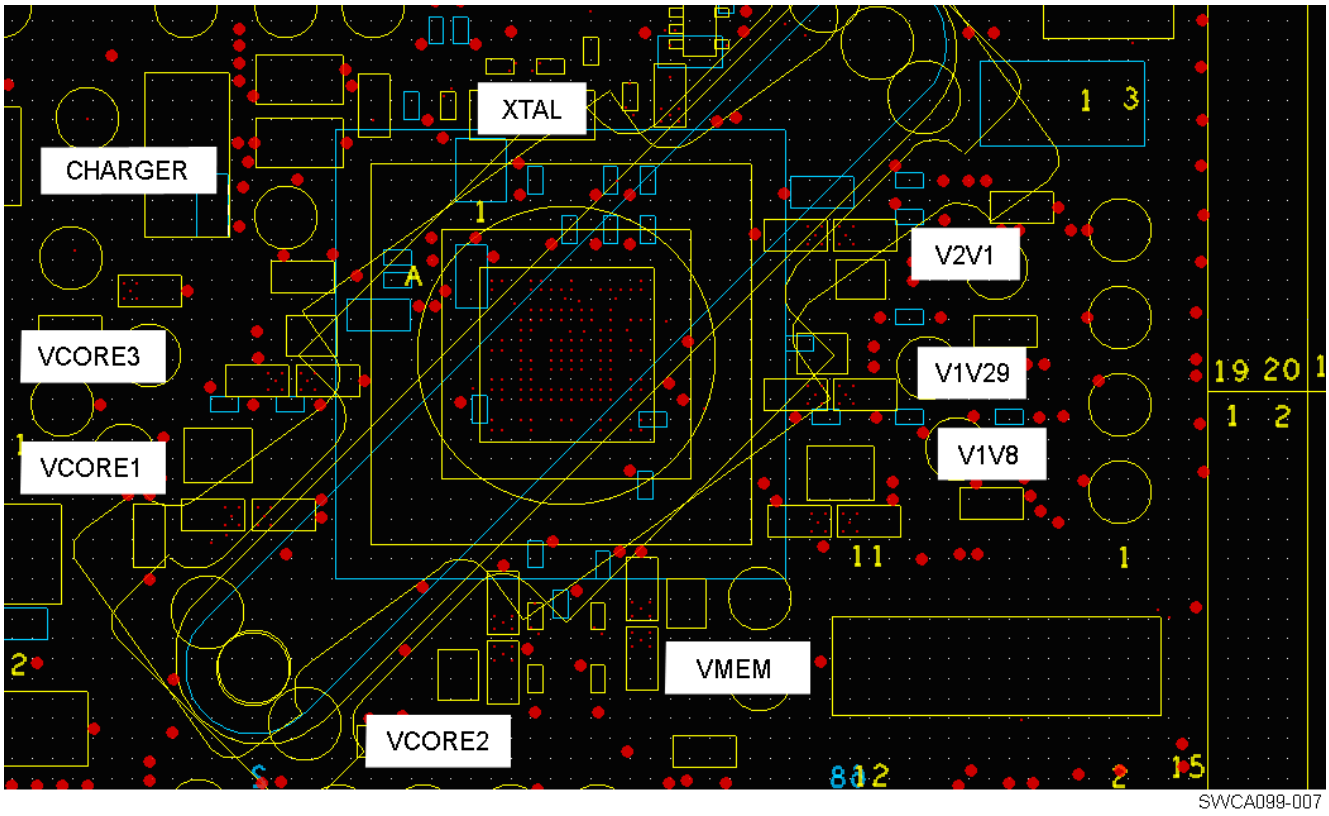

Figure 6. Example of Component Placement on SELAB Daughterboard

Figure 7 shows the SMPS VCORE1 ground plane.

The island for the GND of VIO is broken but not cut from the ground plane. This biases the current flow through the section that is connected to the ground plane and away from circuits that are side by side.

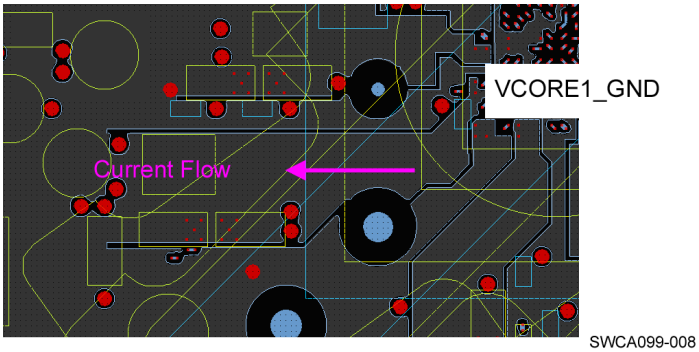

Figure 7. Zoom on SMPS VCORE1 Ground Plane

5.3 DC/DC Converter Outputs

As for all switching power supplies, the board layout is an important step in the design. High-speed operation of the TWL6030 device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold red lines on Figure 8.

The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor.All copnonents(IC, inductor, input and output capacitors) must be placed on the same PCB side. With effort, grounds can be separated between the control and the power devices to minimize the effects of ground noise. Connect these ground nodes together (star point) underneath the IC and ensure that small signal components returning to the AGND pin do not share the high current path of C1 and C2.

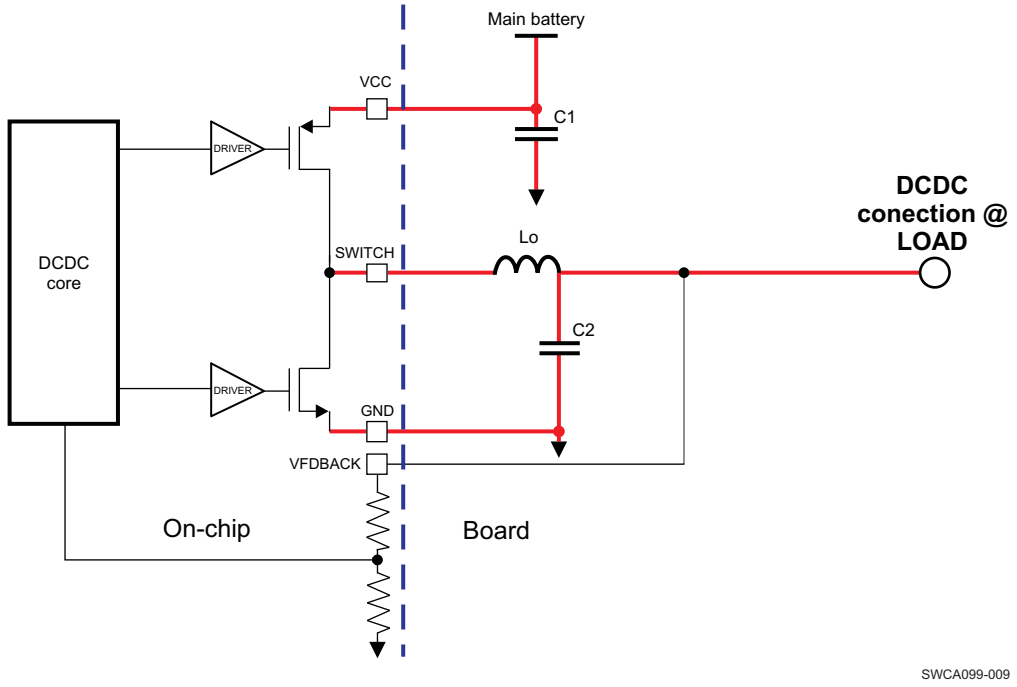

Figure 8. DC/DC Converter

A solution is to isolate the ground plane for the DC/DC converter on the first ground plane (GND layer 1) and then connect multiple vias to the main ground plane (GND layer 2), as shown in Figure 9.

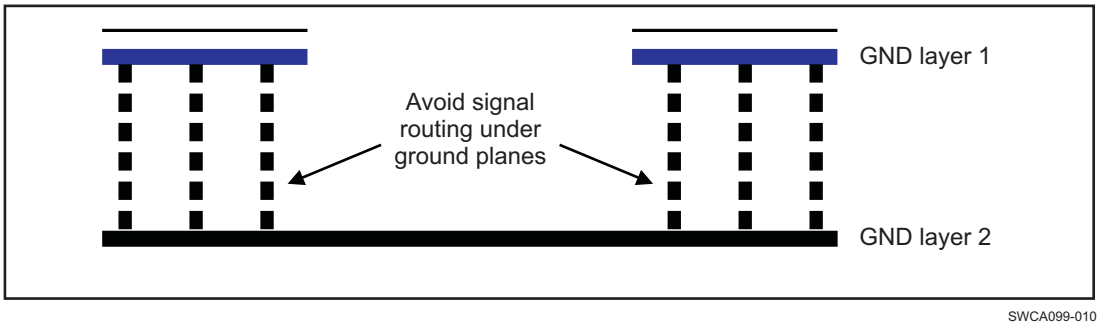

Figure 9. DC/DC Ground Routing

Figure 10 show the DC/DC GND layer 1 on the validation board.

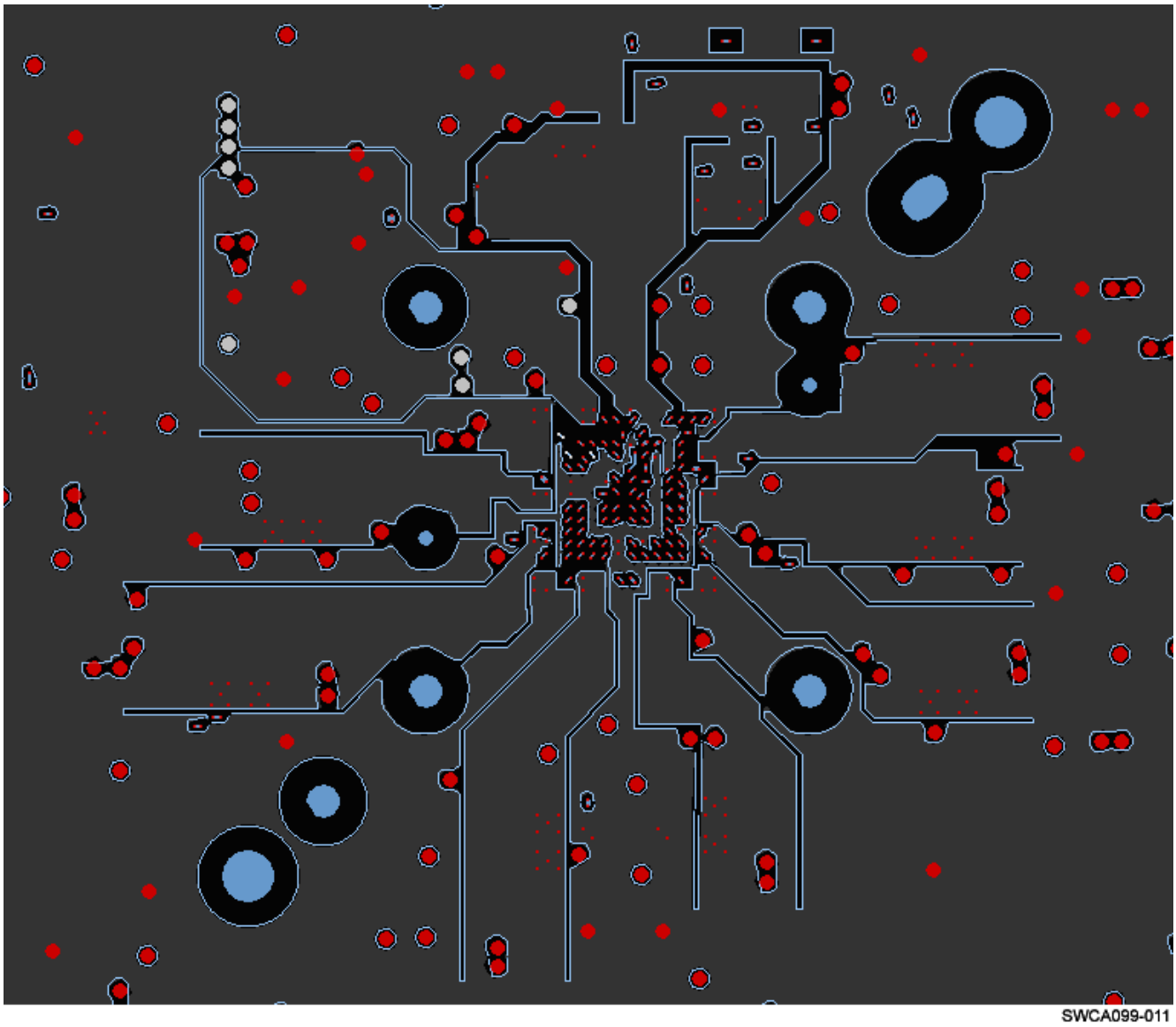

Figure 10. DC/DC GND Layer 1 on Validation Board

5.3.1 DC/DC Routing Example

Figure 11 and Figure 12 show the DC/DC routing on the top layer and GND layer 1, respectively.

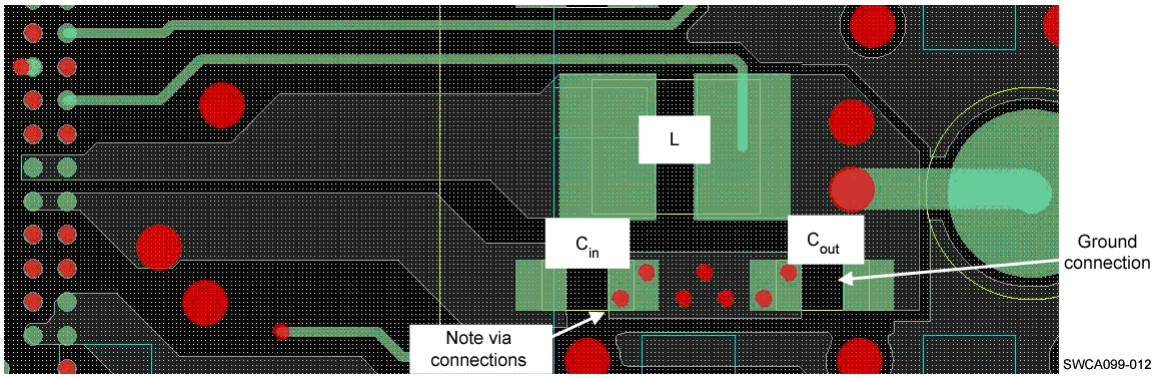

Figure 11. DC/DC Routing on Top Layer

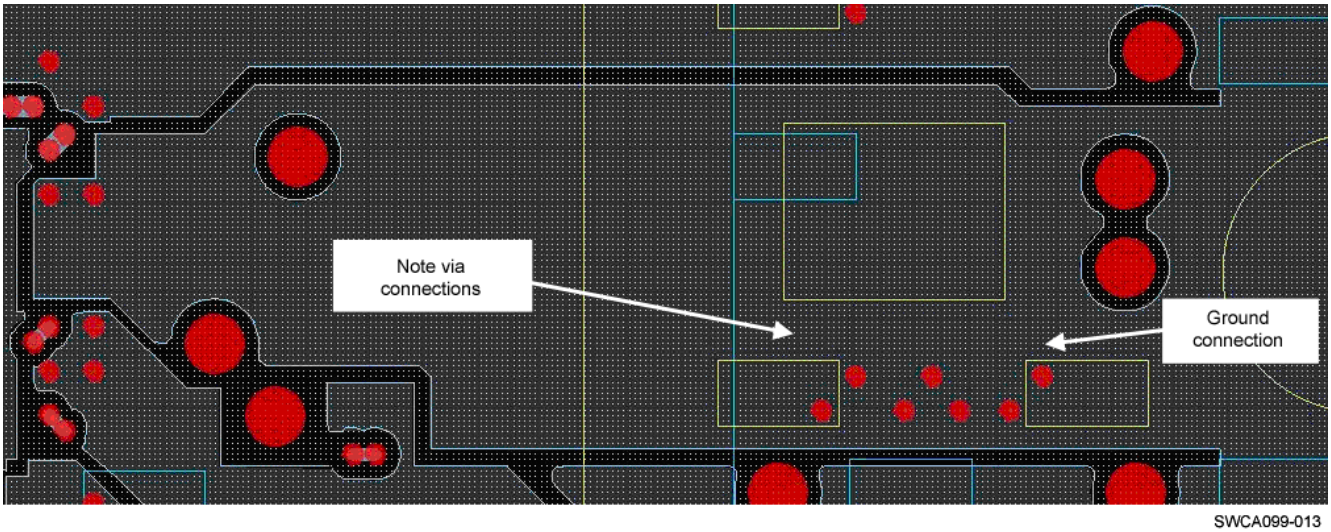

Figure 12. DC/DC Routing on GND1 Layer

Here the DC/DC ground is isolated on top layer and then connects multiple vias to the main ground plane (GND Layer 1).

5.3.2 Sense Signal for DC/DC Converter

The output voltage sense line (FDBK) must be connected to the output capacitor and routed away from noisy components and traces (for example, SWITCH line). Its trace must be minimized and placed in a way such that no signals can affect the voltage level, as that is used to adjust the output voltage from the DC/DC converter.

Ideally, the sense line must not be routed on the same layer as the switched line, but on a lower layer isolated from the switched line by a ground plane.

Figure 13 shows the DC/DC components placement and sense routing.

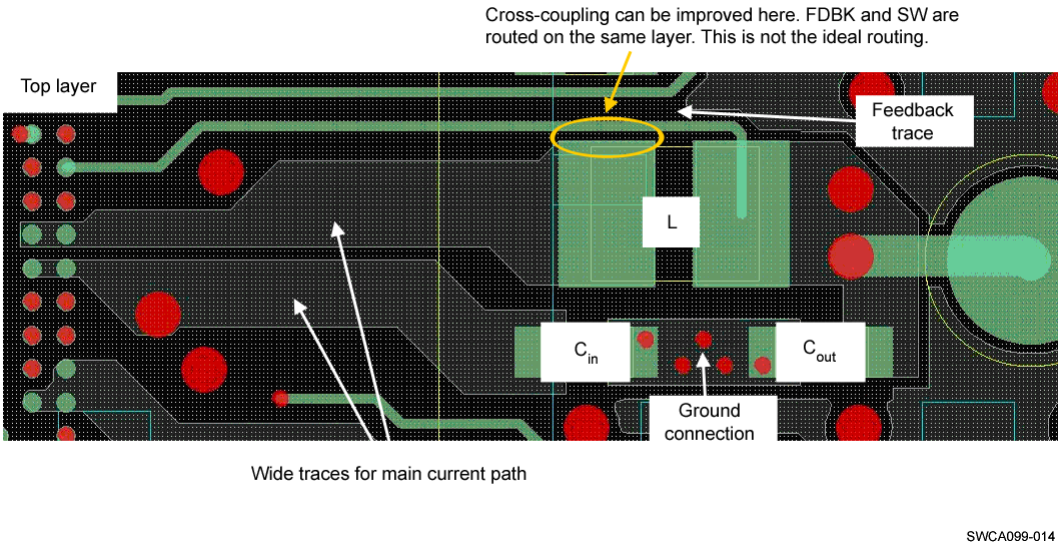

Figure 13. DC/DC Components Placement and Sense Routing

5.3.3 DC/DC High Current Path

High current path must be routed with a trace as wide as possible (see Figure 13).

5.4 Reference Voltage Routing

The reference voltage requires a clean ground. Hence the REFGND ground is used as the ground connection for its filter capacitor. REFGND balls must be connected to a dedicated ground island.

Dedicated ground island is connected to main ground at one point (with via, shrunken ground plane, or shunt resistor).

Dedicated ground island is on the layer under REF components (XTAL, XTAL foot capacitors, OSC32K capactior, IREF resistor, BG_REF capacitor) and follows differential nets from the crystal (see Figure 14).

5.5 32-kHz Oscillator Circuit

The 32-kHz clock circuit is sensitive and certain considerations must be taken into account to prevent impact on the circuit performance.

The buffered 32-kHz output signal CLK32KOUT must also be considered for tunneling because even though it is buffered, it is the core to slow-clocking for the system when used. If noise impacts this signal, then the system may not be able to calibrate the clock signal, and therefore the system will not enter deep sleep if the clock integrity is gating for this purpose.

To prevent disturbance in the ground plane a special restricted area must be defined. We suggest that a plane is placed in the layer directly under the components; this plane may refer only to the REFGND and be connected to the main ground plane with via connections, shrunken ground plane, or shunt resistor.

Ground island width can be reduced between REF components and crystal components to isolate REF components.

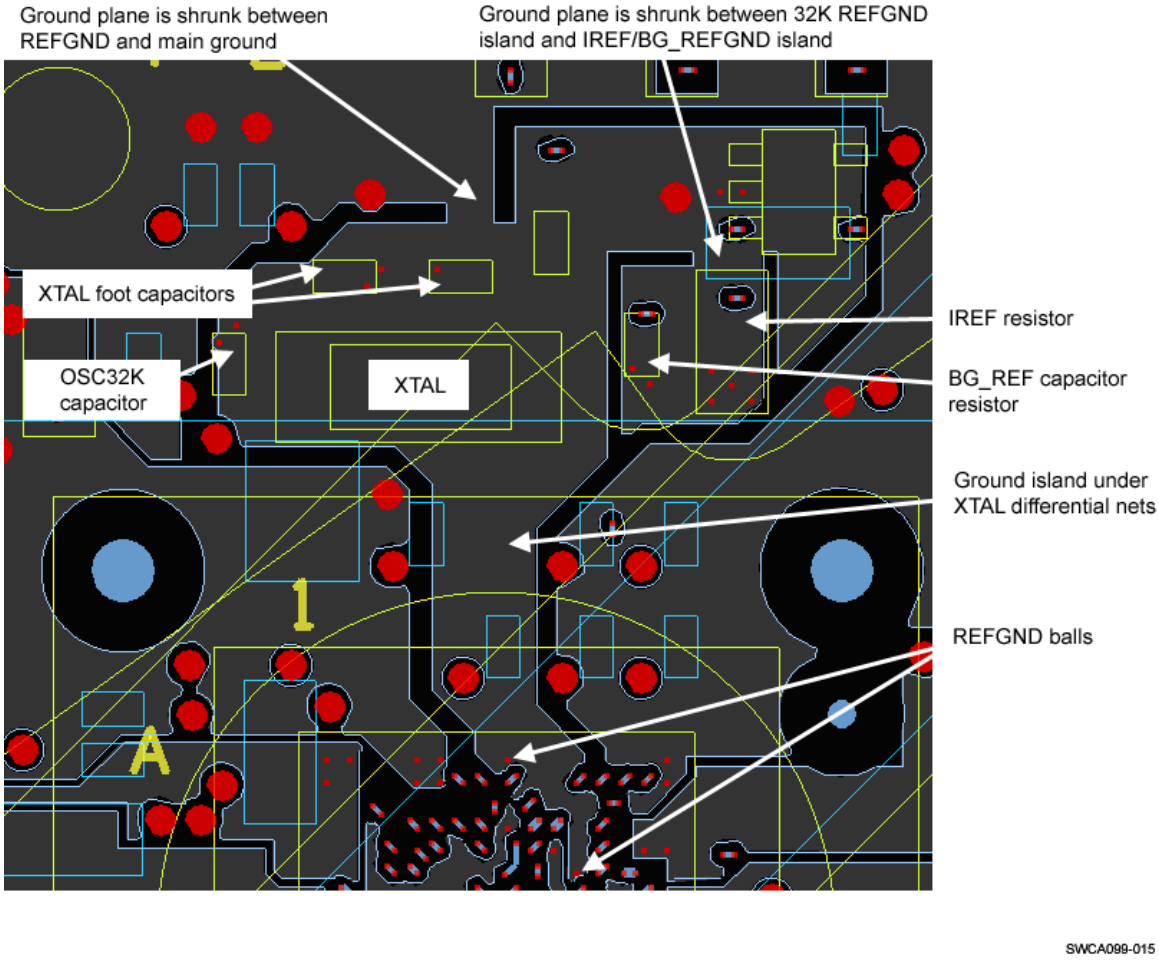

Figure 14. REFGND Ground Plane for REF and Crystal Components

Ideally, a dedicated ground island follows differential nets from the crystal (see Figure 14 and Figure 15). The crystal capacitor must be close to the crystal to reference the capacitor to REFGND (see Figure 15).

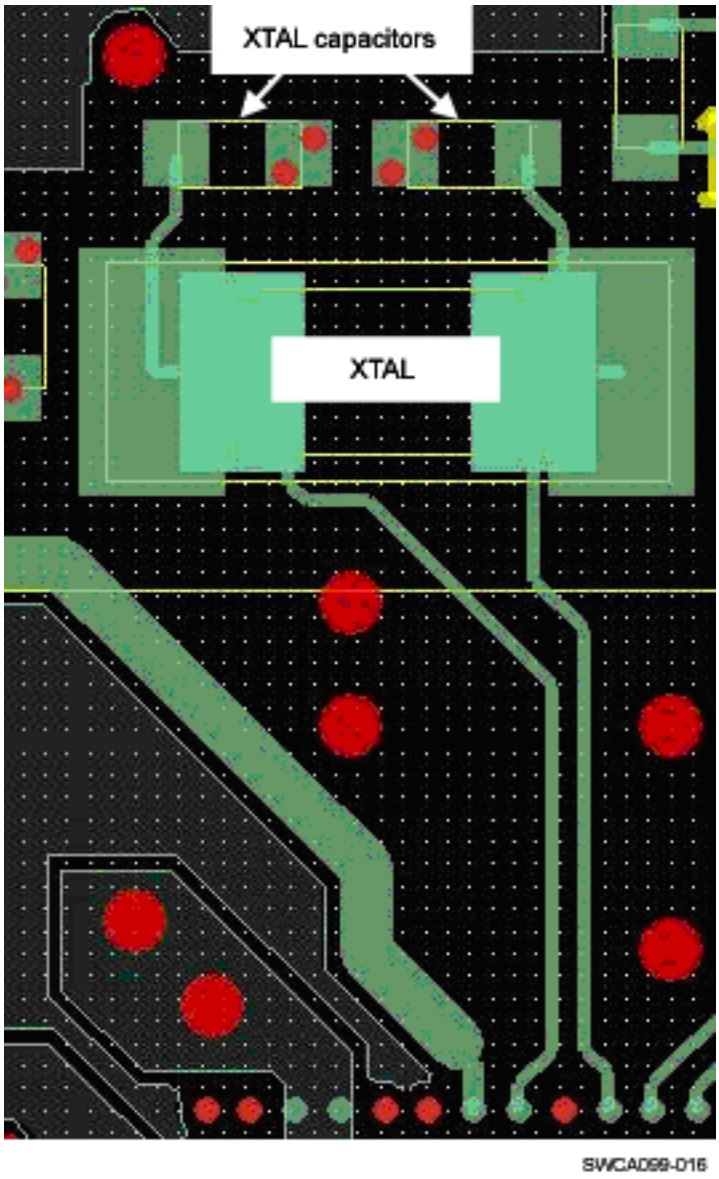

Figure 15. Crystal Components Placement

5.5.1 Use of 32 kHz

The buffered 32-kHz signal CLK32KOUT must also be considered for tunneling because even though it is buffered, it is the core to slow-clocking and hence power saving for the entire system. If this signal is impacted with noise, then the jitter on the clock may be increased.

If the 32-kHz signal must be distributed to more than one device, then it is recommended to use star topology to avoid timing differences. The output is on ball F4.

Keep isolation distance between 32-kHz clock signals (CLK32KAO, CLK32KG, CLK32KAUDIO) and the surrounding signals. Special care must be taken on IREF, VBG, and REFGND where capacitive coupling must be minimized.

Figure 16 shows crosstalk CLK32KOUT versus IREF/VBG.

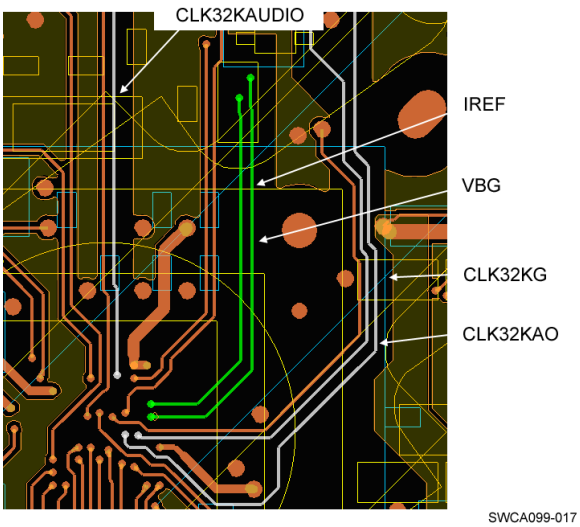

Figure 16. Crosstalk CLK32KOUT Versus IREF/VBG

5.6 Sense Resistor for the Fuel Gauge

The sense resistor must be located close to the battery.

From the sense resistor to balls (GGAUGE_RESP/GGAUGE_RESN), sensing nets must be routed in a differential pair.

Trace is as large as possible for connection between Rsense and the battery pack (also Rsense to GND).

Check that nets connecting PMIC balls to Rsense 20-mΩ resistor are tied at the middle of Rsense pads.

Figure 17 shows the fuel gauge sense resistor routing.

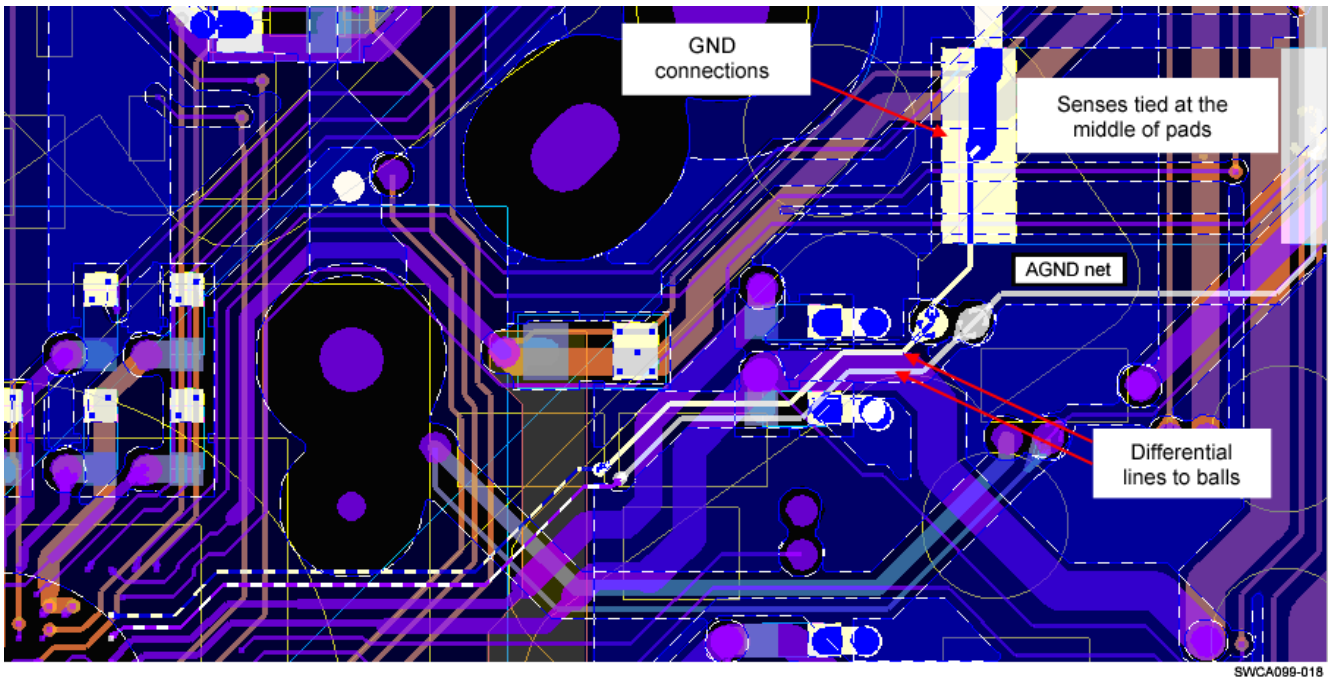

Figure 17. Fuel Gauge Sense Resistor Routing

5.7 Charger

The following traces must be less resistive as possible (area is highlighted in red in Figure 18):

- Rsense must be placed close to the battery pack.
- CHRG_PMID decoupling capacitor must be close to the pin.
- BOOT capacitor must be close as possible to the TWL6030 to reduce noisy loop on PCB.
- CSIN/CSOUT must be route as differential line.
- A large trace is specifically required for the 1.5-A charger path. CHRG_SW_BX must have an impedance of 68 mΩ of resistance and 1 µH of inductance to the battery pack connector.

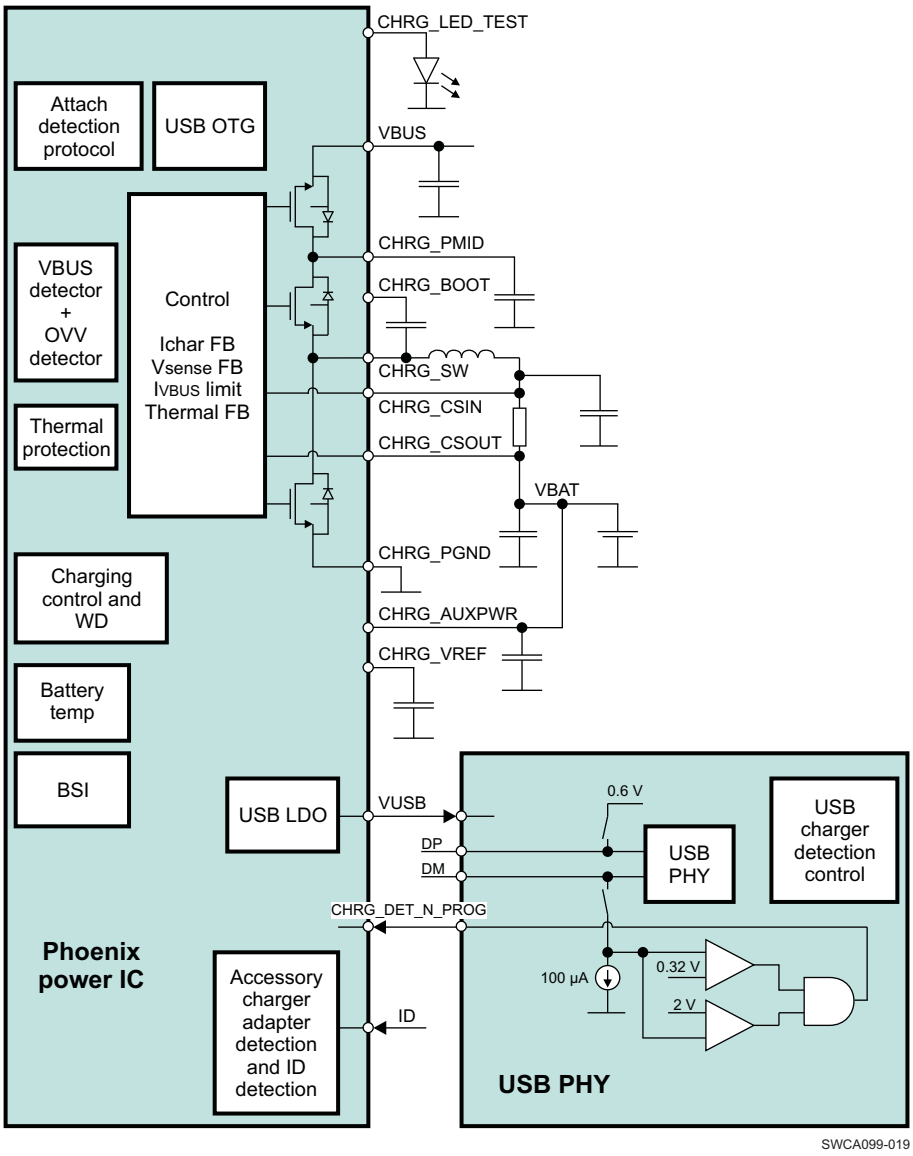

Figure 18. Charger External Components

Figure 19 shows the placement of Rsense.

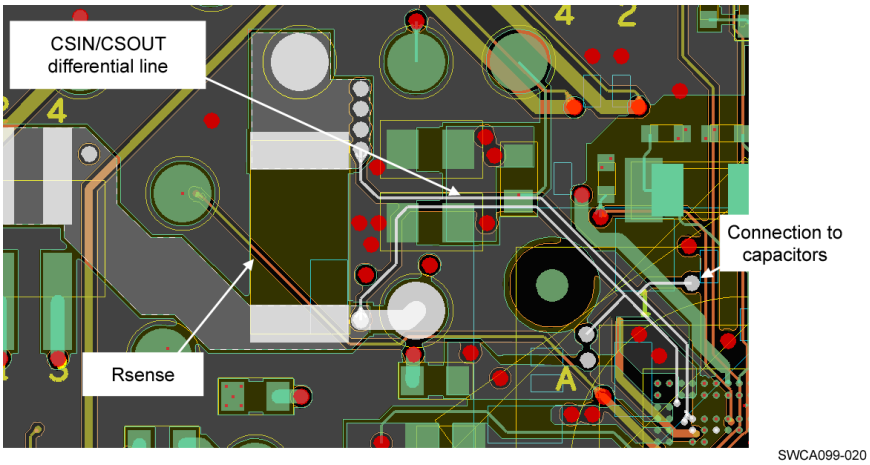

Figure 19. Rsense Placement

5.8 BOOT0, 1, 2, 3 Routing

BOOT0, 1, 2, 3 can be connected to VRTC or to the main ground plane depending on the boot mode required. It must not be left floating; doing so can risk noise coupling on the node and boot mode configuration changes.

6 Routing of Parallel Balls

Routing of parallel balls can be divided into three scenarios. Scenarios are high-power outputs, high-power inputs, and multiple power inputs.

6.1 High-Power Outputs

When routing high-power outputs you must ensure low impedance in the tracks for low IR drop. Furthermore, it is crucial that the routing of the parallel balls ensures that power is distributed evenly between the balls. This can be done by connecting the parallel balls to a power plane. A way to control the current distribution, and hence power distribution, is by consciously connecting to the plane with a well-planned distribution of via connections.

6.2 High-Power Inputs

High-power inputs must be routed with low-impedance tracks to be able to meet requirements for IR drop. If decoupling capacitors are connected, these must be placed as close as possible to the inputs. To ensure good decoupling, the power must first pass the footprint of the decoupling capacitor and then go to the power input. Even the smallest stub from the power track to the capacitor degrades the effect of the capacitor significantly. Grounding the capacitor with a solid connection to the exact same ground to which the high-power device refers is evenly as significant to ensure the best possible performance from the capacitor.

6.3 Multiple Power Inputs

Multiple power inputs are defined as the same power source being distributed to a number of devices or a number of connections on a single device. In this case, a point of distribution must be selected from which to branch out the power supply to the various devices or to the various locations on the same device.

6.3.1 Point of Distribution

A point of distribution is preferably the decoupling capacitor of the device, which generates the power or a similar point in the PCB where there is good decoupling of the power and low-impedance tracks from the power supply. From this point, power is distributed to the various locations where it is needed. When distributing the power, this must be done using the point of distribution as a star point.

CAUTION

Do not distribute power in a daisy-chain manner; doing so causes the quality of the power to deteriorate as the chain moves from power consumer to power consumer.

6.3.2 Connecting Multiple Devices

Use a star point approach when distributing power to multiple devices for the above-mentioned reasons. Consider how much decoupling is necessary. To ensure good decoupling, the power must first pass the footprint of the decoupling capacitor and then go to the power input. Even the smallest stub from the power track to the capacitor degrades the effect of the capacitor. Grounding the capacitor with a solid connection to the exact same ground to which the high-power device refers is evenly as significant to ensure the best possible performance from the capacitor.

6.3.3 Connecting Multiple Pins on a Single Device

When connecting multiple pins on a device, an assessment of the number of decoupling must be made. If in doubt, provide one capacitor pin; however, this is not possible in many cases. Make groups of pins which can share a decoupling, route the power from the point of distribution to the decoupling capacitor, and route from the pins to the decoupling capacitor thus creating a common star connection at the decoupling capacitor. This injects ripple/noise, thus preventing the different balls from affecting each.Make interconnections between parallel balls only at the decoupling capacitor.

6.3.4 Routing of Balanced Signals

Balanced signals must be routed in parallel; same distance from start to end, same impedance for both signals.

Examples of balanced signals are OSC32KIN and OSC32KOUT.

7 Use of Tunnels for Signal Isolation

The tunnelling or shielding in the PCB ensures signal integrity on sensitive signals. Tunnelling is very space consuming in a PCB and must only be used on signals for which this is required.

The tunnelling of signals must be made preferably on a dedicated layer in the PCB on which the signals are routed. The signals are routed with unbroken ground on both sides, and the shield can is formed by having ground on the PCB layers above and below the signals. It is important that the ground planes surrounding are firmly connected with vias ensuring connection between the ground layers as well as to the main ground in the PCB. When implying tunnelling on signals make sure that the signals do not accidentally get exposed to other signals, especially high-speed digital signals with frequent activity.

7.1 Signals Requiring Tunnelling Where Available

32K Crystal: The connections to the 32-kHz crystal must be tunnelled. The 32-kHz oscillator is a very low-power circuit, hence the connections to the crystal must be protected against aggressors.

8 Revision History

The following table summarizes the TWL6030 PCB Guidelines Application Report versions.

Note: Numbering may vary from previous verisons.

Version	Literature Number	Date	Notes
*	SWCA099	April 2011	See (1)
A	SWCA099A	July 2011	See (2)

(1) TWL6030 PCB Guidelines Application Report, (SWCA099) - initial release.

(2) TWL6030 PCB Guidelines Application Report, (SWCA099A):
- Remove NDA statement

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