Application Note Addendum to TIDA-01513 For Two-point Insulation Resistance Measurements

TEXAS INSTRUMENTS

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ABSTRACT

The existing reference design TIDA-01513 is based on single-point isolation leakage error measurement. However, more and more customers require two-point isolation leakage error detection. Two-point isolation leakage error means leakage errors from both positive terminal and negative terminal of high-voltage battery to chassis ground happen at the same time. It is more common to express the required insulation resistance rather than the leakage current, according to International Standards such as ISO6469-1. The insulation resistance provides the information of the possible amount of leakage current. This document explains how to implement two-point insulation resistance measurements based on the existing TIDA-01513 circuit, and discusses the impact of non-ideal characteristics on measurement accuracy.

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1 Introduction

Galvanic isolation is a necessary approach to prevent equipment breakdown and passenger electric shock when there are two distinct grounds of different electrical potentials in EV/ HEVs. Accordingly, isolation leakage measurement is a mandatory means to alert danger and to protect circuits and passengers. Leakage current is the sum of all AC currents from the traction battery to chassis ground through these resistances and impedances. In this way, insulation resistance represents the magnitude of the leakage current as traction battery is regarded as high voltage DC source. Meanwhile, some safety standards require a measurement of insulation resistance instead of leakage current.

TIDA-01513 presents an elaborate concept to realize single-point isolation leakage error measurement. It makes sense to extend TIDA-01513 to two-point insulation resistance measurements with the same hardware circuit topology. In addition, it can also be applied to higher voltage system such as 800 V by replacing appropriate switches and resistors.

2 Two-point Insulation Resistance Measurements

If the isolation leakage errors happen at both positive terminal and negative terminal of a high-voltage battery, the circuit diagram is as shown in Figure 2-1. Here, R_{ISOP} represents the parasitic insulation resistance between high-voltage battery positive terminal and chassis ground, while R_{ISON} represents the parasitic insulation resistance between high-voltage battery negative terminal and chassis ground. In accordance with TIDA-01513 specification, S_1 and S_2 are control switches for positive terminal and negative terminal respectively. Rps (Replace $R_{ps1}+R_{ps2}$ for simplicity) and R_{ns} (Replace $R_{ns1}+R_{ns2}$ for simplicity) are series resistors in positive terminal and negative terminal respectively. Rps (Replace $R_{ps1}+R_{ps2}$ for simplicity) and R_{ns} (Replace $R_{ns1}+R_{ns2}$ for simplicity) are series resistors in positive terminal and negative terminal respectively. R_{s1} and R_{s2} are sampling resistors across op-amp. ISO_POS and ISO_NEG are measured by analog-digital converter for signal processing. Additionally, the battery voltage needs to be measured in order to accomplish the entire insulation resistance measurement. In TIDA-01513, AMC1301-Q1 device is used to perform this measurement and provide an isolated signal for analog-digital converter.

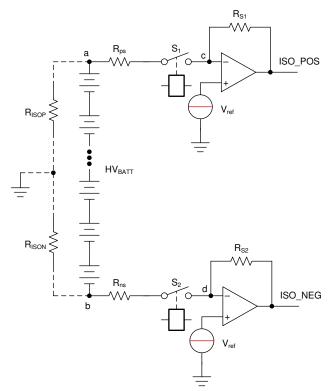


Figure 2-1. Isolation Errors at Both Positive and Negative Terminals

When only S_1 is closed, there are two leakage current paths for the high-voltage battery. One leakage current flows from the positive terminal of high-voltage battery (junction a) to chassis ground, and depends on the positive terminal voltage (referred to chassis ground) and R_{ISOP} . The other leakage current, which goes through

high-voltage battery, flows from the negative terminal of high-voltage battery (junction b) to chassis ground, and depends on the negative terminal voltage (referred to chassis ground) and R_{ISON}.

According to Kirchhoff's Current Law, the sum of currents entering and leaving the same junction is always zero. Equations are found at junction a and junction c respectively.

$$\frac{V_{a} - HV_{BATT1}}{R_{ISON}} + \frac{V_{a}}{R_{ISOP}} + \frac{V_{a} - V_{ref}}{R_{ps}} = 0$$

$$\frac{V_{a} - V_{ref}}{R_{ps}} + \frac{ISO_POS - V_{ref}}{R_{S1}} = 0$$
(1)
(2)

Here V_a is the voltage at junction a, which is the high-battery positive terminal voltage referred to chassis ground. V_{ref} is the reference voltage applied to op-amp non-inverting input (+). R_{ps} is the sum of R_{ps1} and R_{ps2} , that is $R_{ps} = R_{ps1} + R_{ps2}$. HV_{BATT1} is the battery voltage measured by ADC when only S₁ is closed. ISO_POS is the top op-amp output voltage during the same scenario. HV_{BATT1} and ISO_POS should be sampled by ADC synchronously for calculation accuracy.

Let $\alpha = V_a$ for simplicity, and α can be obtained from Equation 2. The voltage at junction a, which is α , is determined by ISO_POS which is measured by ADC.

$$\alpha = V_{ref} \times \left(1 + \frac{R_{ps}}{R_{s1}}\right) - \frac{R_{ps}}{R_{s1}} \times ISO_POS$$
(3)

When only S₂ is closed, there are also two leakage current paths for the high-voltage battery. One leakage current, which goes through high-voltage battery, flows from the positive terminal of high-voltage battery (junction a) to chassis ground, and depends on the positive terminal voltage (referred to chassis ground) and R_{ISOP}. The other leakage current flows from the negative terminal of high-voltage battery (junction b) to chassis ground, and depends on the negative terminal of high-voltage battery (junction b) to chassis ground, and depends on the negative terminal voltage (referred to chassis ground) and R_{ISOP}.

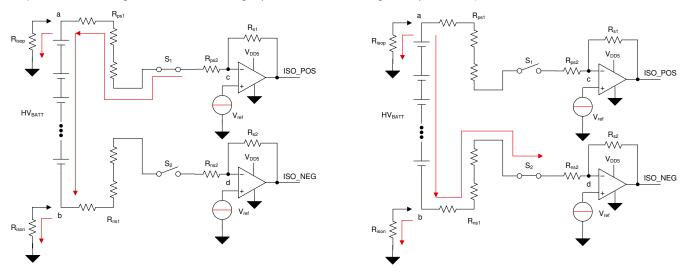


Figure 2-2. Measurement Prodedure: Only One Switch is Closed Periodically

Similarly, the equations of junction b and junction d can be obtained according to Kirchhoff's Current Law respectively.

$$\frac{V_{b} + HV_{BATT2}}{R_{ISOP}} + \frac{V_{b}}{R_{ISON}} + \frac{V_{b} - V_{ref}}{R_{ns}} = 0$$

(4)

$$\frac{V_{b} - V_{ref}}{R_{ns}} + \frac{ISO_NEG - V_{ref}}{R_{S2}} = 0$$

synchronously for calculation accuracy.

Here V_b is the voltage at junction b, which is the high-battery negative terminal voltage referred to chassis ground. V_{ref} is the reference voltage applied to op-amp non-inverting input (+). R_{ns} is the sum of R_{ns1} and R_{ns2}, that is, R_{ns}=R_{ns1}+R_{ns2}. HV_{BATT2} is the battery voltage measured by ADC when only S₂ is closed. ISO_NEG is the bottom op-amp output voltage during the same scenario. HV_{BATT2} and ISO_NEG should be sampled by ADC

Similarly, let $\beta = V_b$ for simplicity, then β can be derived from Equation 5. The voltage at junction b, which is β , can be determined by ISO_NEG which is also measured by ADC.

$$\beta = V_{ref} \times \left(1 + \frac{R_{ns}}{R_{s2}}\right) - \frac{R_{ns}}{R_{s2}} \times ISO_NEG$$
(6)

Different equations are seen during these two switching scenarios, which can be combined to calculate desired R_{ISOP} and R_{ISON} . Equation 1 and Equation 4 are combined to form an equation group while replacing V_a and V_b α with and β respectively.

$$\begin{cases} \frac{\alpha - HV_{BATT1}}{R_{ISON}} + \frac{\alpha}{R_{ISOP}} + \frac{\alpha - V_{ref}}{R_{ps}} = 0\\ \frac{\beta + HV_{BATT2}}{R_{ISOP}} + \frac{\beta}{R_{ISON}} + \frac{\beta - V_{ref}}{R_{ns}} = 0 \end{cases}$$
(7)

Let R_{ps} equals to R_{ns} in the design, that is, $R_{ps} = R_{ns}$, then R_{ISOP} and R_{ISON} are found from above equation group.

$$\begin{cases} \mathsf{R}_{\mathsf{ISOP}} = \frac{\mathsf{HV}_{\mathsf{BATT1}} \times \mathsf{HV}_{\mathsf{BATT2}} \times \mathsf{R}_{\mathsf{ps}} + \mathsf{HV}_{\mathsf{BATT1}} \times \mathsf{R}_{\mathsf{ps}} \times \beta - \mathsf{HV}_{\mathsf{BATT2}} \times \mathsf{R}_{\mathsf{ps}} \times \alpha}{\mathsf{H}_{\mathsf{VBATT1}} \times \mathsf{V}_{\mathsf{ref}} - \mathsf{HV}_{\mathsf{BATT1}} \times \beta + \mathsf{V}_{\mathsf{ref}} \times \beta - \mathsf{V}_{\mathsf{ref}} \times \alpha} \\ \mathsf{R}_{\mathsf{ISON}} = -\frac{\mathsf{HV}_{\mathsf{BATT1}} \times \mathsf{HV}_{\mathsf{BATT2}} \times \mathsf{R}_{\mathsf{ps}} + \mathsf{HV}_{\mathsf{BATT1}} \times \mathsf{R}_{\mathsf{ps}} \times \beta - \mathsf{HV}_{\mathsf{BATT2}} \times \mathsf{R}_{\mathsf{ps}} \times \alpha}{\mathsf{H}_{\mathsf{VBATT2}} \times \mathsf{V}_{\mathsf{ref}} - \mathsf{HV}_{\mathsf{BATT2}} \times \alpha + \mathsf{V}_{\mathsf{ref}} \times \beta - \mathsf{V}_{\mathsf{ref}} \times \alpha} \end{cases}$$
(8)

Generally, the value of α is positive and the value of β is negative as they are referred to chassis ground. In consequence, the ADC measured ISO_POS is smaller than V_{ref} and ISO_NEG is larger than V_{ref}. The absolute values of both α and β are much larger than zero under typical conditions as long as no terminal is shorted to chassis ground.

Equation 8 is the explicit formula, that can be integrated in the software to get the desired insulation resistance R_{ISOP} and R_{ISON} .

3 Equation Verification by Simulation

Simulation can be used to verify that the analysis and the final equations are correct to get the right R_{ISOP} and R_{ISON} . The circuit itself is very simple and TINA simulation is a good choice here.

In this simulation, $R_{ps} = R_{ns} = 1.18 \text{ M}\Omega$, $R_{s1} = R_{s2} = 5 \text{ k}\Omega$. Assume the insulation resistances $R_{ISOP} = 800 \text{ k}\Omega$ and $R_{ISON} = 200 \text{ k}\Omega$. When only S_1 is closed, the battery voltage is 400 V and output ISO_POS is 1.32 V. When only S_2 is closed, the battery voltage fluctuates up to 415 V and the corresponding output ISO_NEG is 2.82 V.

(5)



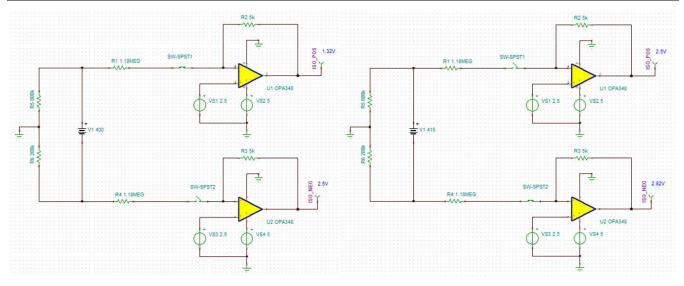


Figure 3-1. TINA Simulation Results of Two Scenarios

 α equals to 280.98 based on Equation 3, and β is equal to -73.02 based on Equation 6. R_{ISOP} and R_{ISON} can be derived to 812 k Ω and 204 k Ω respectively according to Equation 8, which are very close to the simulation values.

4 Op-amp Caused Error Analysis

The operational amplifier is considered to be ideal in the above calculations. That is to say, the op-amp is assumed to be perfect with two main characteristics. The first one is that it has infinite input impedance resulting in 'No current flowing into either of its two inputs'. The other one is that it has infinite open-loop gain resulting in 'Two input voltages are equal without any offset'. However, real op-amps are non-ideal and have finite open-loop gain, finite input impedance, non-zero input voltage offset, etc. These non-ideal characteristics will affect the op-amp output voltage accuracy measured by ADC, as well as the insulation resistance calculation error. The errors of ISO_POS and ISO_NEG sampled by ADC determine the ultimate calculated insulation resistance error.

4.1 Input offset voltage

The output of an ideal op-amp should be zero if the input voltage difference is zero. But the mismatch of differential input transistors of real op-amps causes the output to be zero at a non-zero value of differential input, which is known as input offset voltage.

It is assumed that the inverting input (–) voltage of the op-amp is equal to non-inverting input (+) in the above calculation. And the non-inverting input (+) is connected to the voltage reference V_{ref} .

Once the input offset voltage is considered between the non-inverting input (+) and the inverting input (-), ISO_POS and ISO_NEG can take into account the input offset voltage from Equation 2 and Equation 5 respectively.

$$ISO_POS = \left[\left(V_{ref} \pm V_{offset} \right) \times \left(1 + \frac{R_{ps}}{R_{S1}} \right) - V_{a} \right] \times \frac{R_{S1}}{R_{ps}}$$
(9)
$$ISO_NEG = \left[\left(V_{ref} \pm V_{offset} \right) \times \left(1 + \frac{R_{ns}}{R_{S2}} \right) - V_{b} \right] \times \frac{R_{S2}}{R_{ns}}$$
(10)



4.2 Input bias current

In the above calculations it is assumed that the input impedance is infinite and there is no current flowing into the inverting input (–). But actually a small amount of current must flow into the inputs due to bias requirement or parasitic leakage in real op-amp. The input bias current can either flow into or out of the inputs.

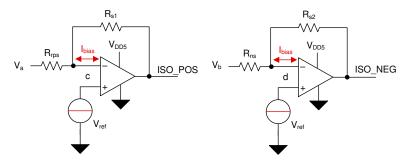


Figure 4-1. Input Bias Current Flows into or out of Inverting Input

If the input bias current is considered in Equation 2 and Equation 5, they can be revised as follows:

$$\frac{V_{a} - V_{ref}}{R_{ps}} = \frac{V_{ref} - ISO_POS}{R_{S1}} \pm I_{bias}$$

$$\frac{V_{b} - V_{ref}}{V_{ref}} = \frac{V_{ref} - ISO_NEG}{V_{ref}} \pm I_{bias}$$
(11)

$$\frac{R_{ns}}{R_{s2}} = \frac{R_{s2}}{R_{s2}} \pm I_{bias}$$
(12)

Then ISO_POS and ISO_NEG can be obtained including input bias current error respectively.

$$ISO_POS = \left[V_{ref} \times \left(1 + \frac{R_{ps}}{R_{s1}} \right) - V_{a} \right] \times \frac{R_{s1}}{R_{ps}} \pm I_{bias} \times R_{s1}$$
(13)

$$ISO_NEG = \left[V_{ref} \times \left(1 + \frac{R_{ns}}{R_{S2}} \right) - V_{b} \right] \times \frac{R_{S2}}{R_{ns}} \pm I_{bias} \times R_{S2}$$
(14)

4.3 Open-loop gain

The initial analysis is based on the assumption that the open-loop gain of operational amplifier approaches infinity. However, if considering the finite open-loop gain of the op-amp, it can be started directly from the definition of open-loop gain.

$$A_{OL} = \frac{ISO_POS}{V_{ref} - V_{c}} = \frac{ISO_POS}{V_{ref} - \left(ISO_POS \times \frac{R_{ps}}{R_{ps} + R_{s1}} + V_{a} \times \frac{R_{s1}}{R_{ps} + R_{s1}}\right)}$$
(15)

$$A_{OL} = \frac{ISO_NEG}{V_{ref} - V_{d}} = \frac{ISO_NEG}{V_{ref} - \left(ISO_NEG \times \frac{R_{ns}}{R_{ns} + R_{s2}} + V_{b} \times \frac{R_{s2}}{R_{ns} + R_{s2}}\right)}$$
(16)

Then ISO_POS and ISO_NEG can be got including open-loop gain error respectively.

$$ISO_POS = \left[V_{ref} \times \left(1 + \frac{R_{ps}}{R_{S1}} \right) - V_{a} \right] \times \frac{R_{S1}}{\left(R_{ps} + \frac{R_{ps} + R_{S1}}{A_{OL}} \right)}$$
(17)

$$ISO_NEG = \left[V_{ref} \times \left(1 + \frac{R_{ns}}{R_{S2}} \right) - V_{b} \right] \times \frac{R_{S2}}{\left(R_{ns} + \frac{R_{ns} + R_{S2}}{A_{OL}} \right)}$$
(18)

If A_{OL} in Equation 17 and Equation 18 is infinite, Equation 17 is equivalent to Equation 2, as well as Equation 18 is equivalent to Equation 5.

5 Summary

This addendum presents an approach to adapt the existing reference design TIDA-01513 to calculate the exact insulation resistances for two-point leakage errors. It is a necessary feature as dictated in many International Standards. This is applicable in HEVs and EVs as battery management systems, traction inverters, DC/DC converters, onboard chargers, and other subsystems operate at high voltage (higher than 60 V). The insulation resistance measurement error is caused by many factors such as resistance tolerance, op-amp non-ideal performance error, and ADC tolerance. The complete error analysis is beyond the scope of this document. However, the effect of the op-amp non-idealities on the measured insulation resistance is presented, and can serve as a starting point for further analysis.

6 References

- TIDA-01513 Automotive High-Voltage and Isolation Leakage Measurements Reference Design
- HANDBOOK OF OPERATIONAL AMPLIFIER APPLICATIONS

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