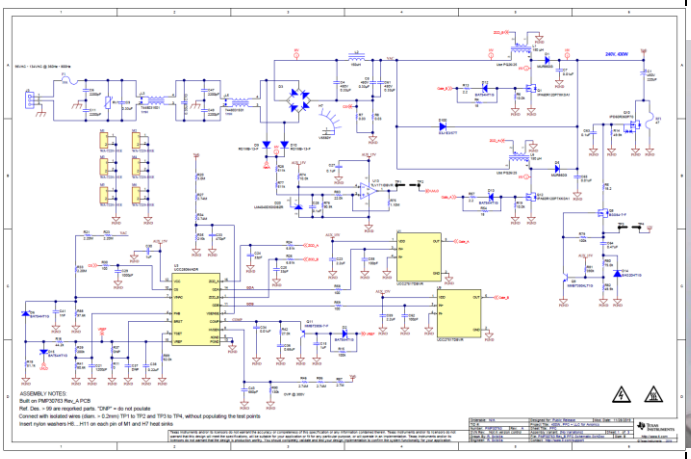
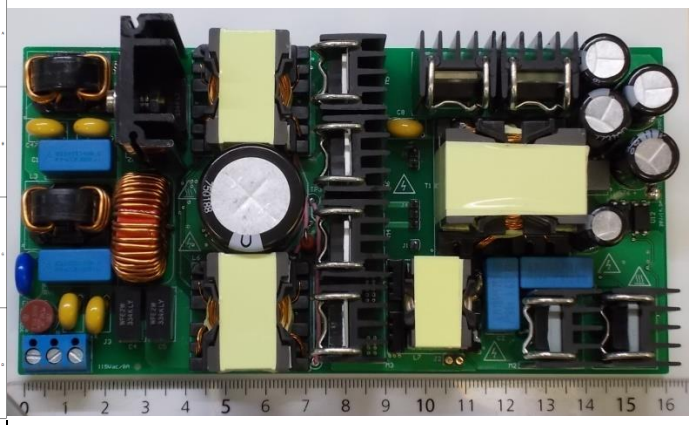
Test Report: PMP30763
93% Efficiency, 400-W AC/DC Reference Design for Avionics

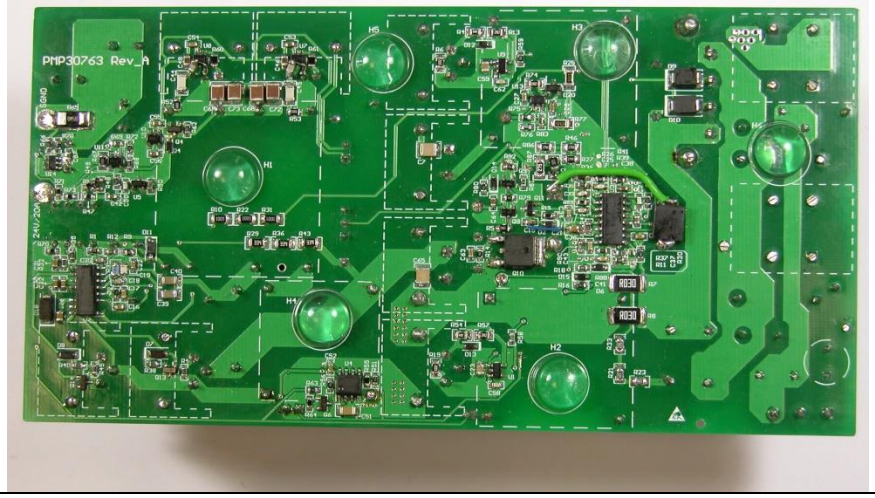
Description

This is a compact, 30-V DC, 400-W reference design for avionics applications, accepting main frequencies between 400 Hz and 800 Hz. This design consists of a front-end, two-phase interleaved transition mode (TM) power factor correction (PFC) based on UCC28064A. This minimizes the PFC inductor size and reduces EMI filter requirements. The DC/DC is implemented by employing the HB-LLC stage, using UCC256404. For efficiency improvement, synchronous rectification is used at secondary side with FETs driven by UCC24612.

The reference design PMP30763 Rev_B has been built on PMP30763 Rev_A PCB.







1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage	96 VAC – 134 VAC
Frequency:	400 Hz – 800 Hz
Output, Voltage:	30 VDC
Output, Current:	13.3 A

1.2 Required Equipment

- 0…150 VAC, 400 Hz…800 Hz (minimum current limit 7 Arms), AC constant voltage source (VS1)
- Electronic load, (constant current range 0…15 A)
- Oscilloscope (min. 100 MHz bandwidth)
- Current probe (min. 100 KHz bandwidth)
- Optional: infrared camera

1.3 Testing Conditions

a) Connect the source VS1 to J3-1 and J3-2; earth connection to J3-3.
b) Connect the load to terminals “30V” (plus) and “R_SENSE” (minus)
c) Attach a current probe in series to VS1 to measure the input current
d) Attach a current probe in series to L7 (by disconnecting one pin) to measure the resonant current
e) Turn on Vs1 (accepted range: 96 VAC…134 VAC).
f) Increase the load on the output
g) After turn off, wait ~ 5 minutes until C1 (PFC capacitor) is completely discharged (warning: HIGH VOLTAGE)

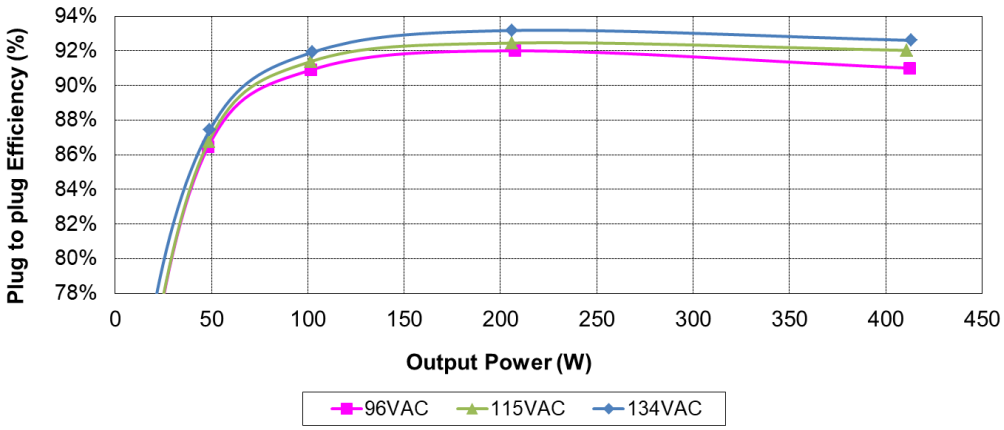
2 Testing and Results

2.1 Efficiency Graph and Data

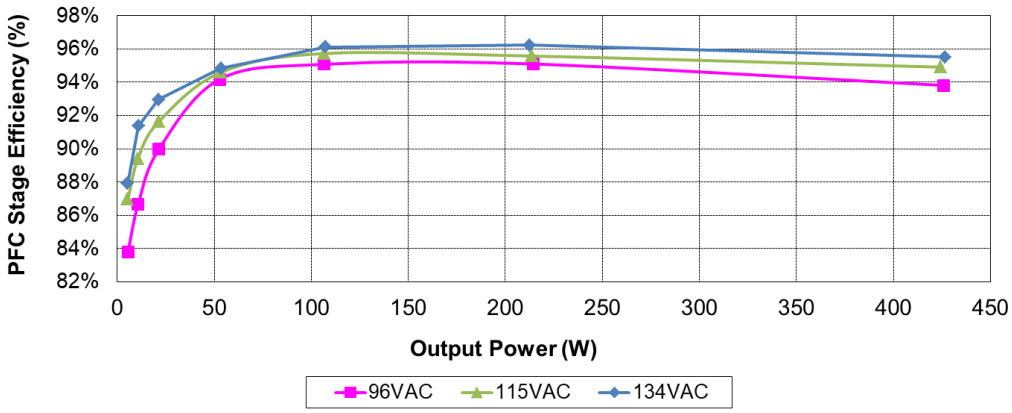
2.1.1 Efficiency Graphs:

The efficiency graphs, regarding respectively plug-to-plug, PFC and LLC stage, versus output power, are shown below. The input voltage has been set to 96 VAC, 115 VAC and 134 VAC, 400, 600 and 800 Hz.

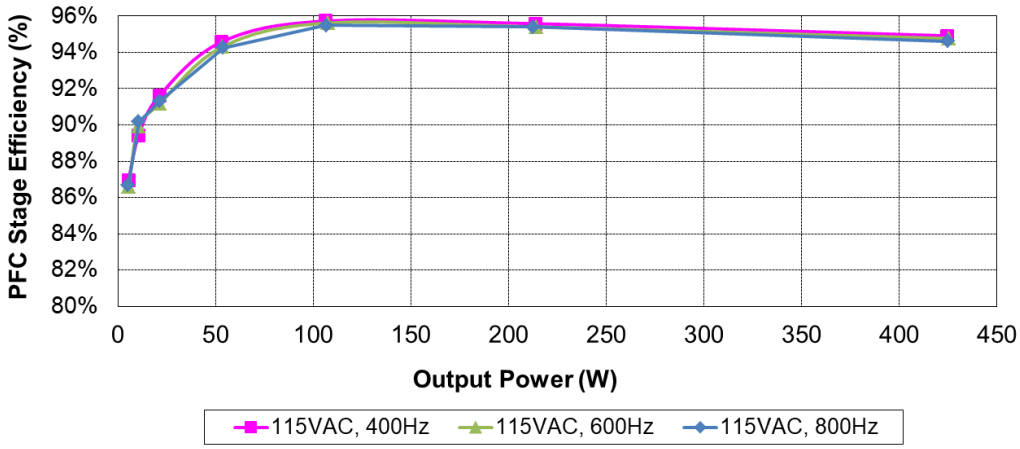
Plug-to-plug:



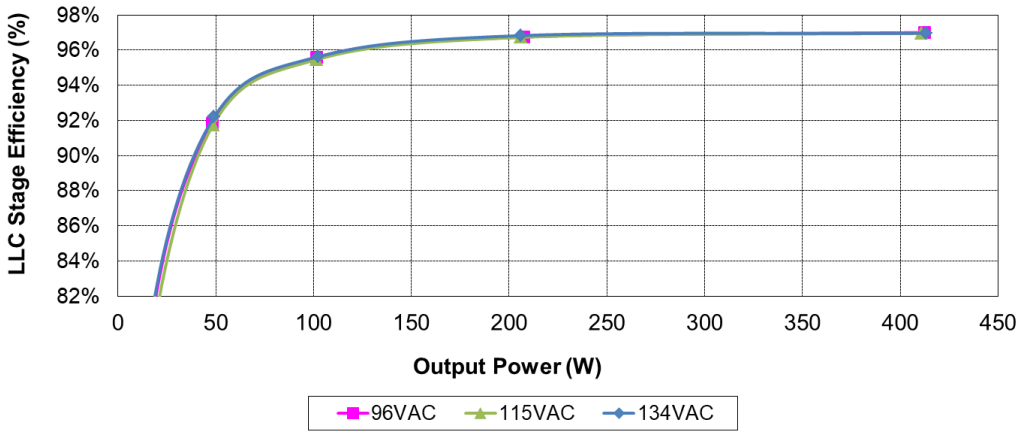
PFC stage versus load and VAC (at 400 Hz):



PFC stage versus load and mains frequency (at 115 VAC):



LLC stage (not dependent on VAC because V_{PFC} is constant):



2.1.2 Efficiency Data:

The efficiency graph reports the data from the table shown below, in output power range 0…400 W (425W for PFC stage):

Vin = 96 VAC, f = 400 Hz, efficiency of PFC stage only							
Pin (W)	V_pfc (V)	I_pfc (mA)	V_aux (V)	I_aux (mA)	Power Factor (%)	Pout (W)	Efficiency (%)
0.328	241.6	0.0	15.0	7.5	0.00	0.00	0.00%
6.398	241.6	22.8	15.0	11.7	29.40	5.51	83.80%
12.216	241.6	44.7	15.0	16.4	45.07	10.80	86.66%
23.540	241.4	88.8	15.0	19.2	64.47	21.44	89.96%
55.721	241.4	218.5	15.0	19.1	86.80	52.75	94.18%
111.92	241.3	442.0	15.0	16.9	95.81	106.65	95.08%
225.11	241.3	888.7	15.0	25.6	98.98	214.44	95.10%
453.77	241.2	1766	15.0	18.7	99.83	425.96	93.81%

Vin = 115 VAC, f = 400 Hz, efficiency of PFC stage only							
Pin (W)	V_pfc (V)	I_pfc (mA)	V_aux (V)	I_aux (mA)	Power Factor (%)	Pout (W)	Efficiency (%)
0.332	241.6	0.0	15.0	7.2	0.00	0.00	0.00%
6.127	241.5	22.6	15.0	10.0	22.16	5.46	86.95%
11.690	241.5	44.0	15.0	13.1	35.08	10.63	89.40%
23.008	241.5	88.4	15.0	19.6	53.81	21.35	91.62%
55.994	241.4	220.5	15.0	18.8	79.03	53.23	94.59%
111.03	241.3	441.5	15.0	17.3	92.13	106.53	95.73%
223.31	241.3	885.4	15.0	14.5	97.77	213.65	95.58%
446.96	241.2	1760	15.0	20.8	99.55	424.51	94.91%

Vin = 134 VAC, f = 400 Hz, efficiency of PFC stage only							
Pin (W)	V_pfc (V)	I_pfc (mA)	V_aux (V)	I_aux (mA)	Power Factor (%)	Pout (W)	Efficiency (%)
0.343	241.6	0.0	15.0	7.4	0.00	0.00	0.00%
5.983	241.5	22.3	15.0	9.5	16.70	5.39	87.92%
11.725	241.5	45.0	15.0	11.3	28.15	10.87	91.37%
22.718	241.5	88.3	15.0	14.8	44.17	21.32	92.96%
56.208	241.4	222.0	15.0	19.5	71.14	53.59	94.85%
111.30	241.3	444.4	15.0	17.7	87.15	107.23	96.12%
220.64	241.3	880.8	15.0	15.3	95.78	212.54	96.23%
446.41	241.2	1769	15.0	22.3	99.01	426.68	95.51%

Vin = 115 VAC, f = 600 Hz, efficiency of PFC stage only							
Pin (W)	V_pfc (V)	I_pfc (mA)	V_aux (V)	I_aux (mA)	Power Factor (%)	Pout (W)	Efficiency (%)
0.074	241.6	0.0	15.0	7.5	0.00	0.00	0.00%
6.235	241.5	22.9	15.0	10.1	16.40	5.53	86.59%
11.604	241.5	43.9	15.0	12.5	26.88	10.60	89.91%
23.120	241.5	88.3	15.0	18.1	43.03	21.32	91.16%
56.602	241.3	222.4	15.0	19.8	68.59	53.67	94.32%
112.14	241.3	445.4	15.0	17.3	85.72	107.48	95.62%
224.26	241.2	887.9	15.0	14.5	95.70	214.16	95.40%
448.42	241.2	1763	15.0	20.8	99.20	425.24	94.76%

Vin = 115 VAC, f = 800 Hz, efficiency of PFC stage only							
Pin (W)	V_pfc (V)	I_pfc (mA)	V_aux (V)	I_aux (mA)	Power Factor (%)	Pout (W)	Efficiency (%)
0.111	241.6	0.0	15.0	7.5	0.00	0.00	0.00%
5.952	241.5	21.9	15.0	9.9	12.40	5.29	86.70%
11.760	241.5	44.6	15.0	12.4	21.87	10.77	90.16%
23.248	241.5	88.9	15.0	17.7	36.04	21.47	91.31%
56.974	241.3	223.7	15.0	19.6	60.97	53.98	94.26%
111.37	241.3	441.8	15.0	17.5	78.89	106.61	95.50%
222.77	241.3	881.6	15.0	14.5	93.00	212.73	95.40%
448.61	241.2	1761	15.0	20.8	98.72	424.75	94.62%

Vin = 96 VAC, f = 400 Hz, plug to plug and LLC efficiency					
Pin (W)	Vout (V)	Iout (A)	Pout (W)	Efficiency plug-to-plug (%)	Efficiency LLC (%)
0.655	29.97	0.0000	0.00	0.00%	0.00%
6.426	29.98	0.0844	2.53	39.34%	46.95%
12.250	29.98	0.2149	6.44	52.58%	60.67%
23.562	29.98	0.5688	17.05	72.32%	80.39%
55.790	29.98	1.6104	48.28	86.46%	91.81%
111.69	29.98	3.3894	101.61	90.90%	95.60%
225.35	29.97	6.9244	207.52	92.01%	96.75%
452.99	29.96	13.772	412.62	91.00%	97.01%

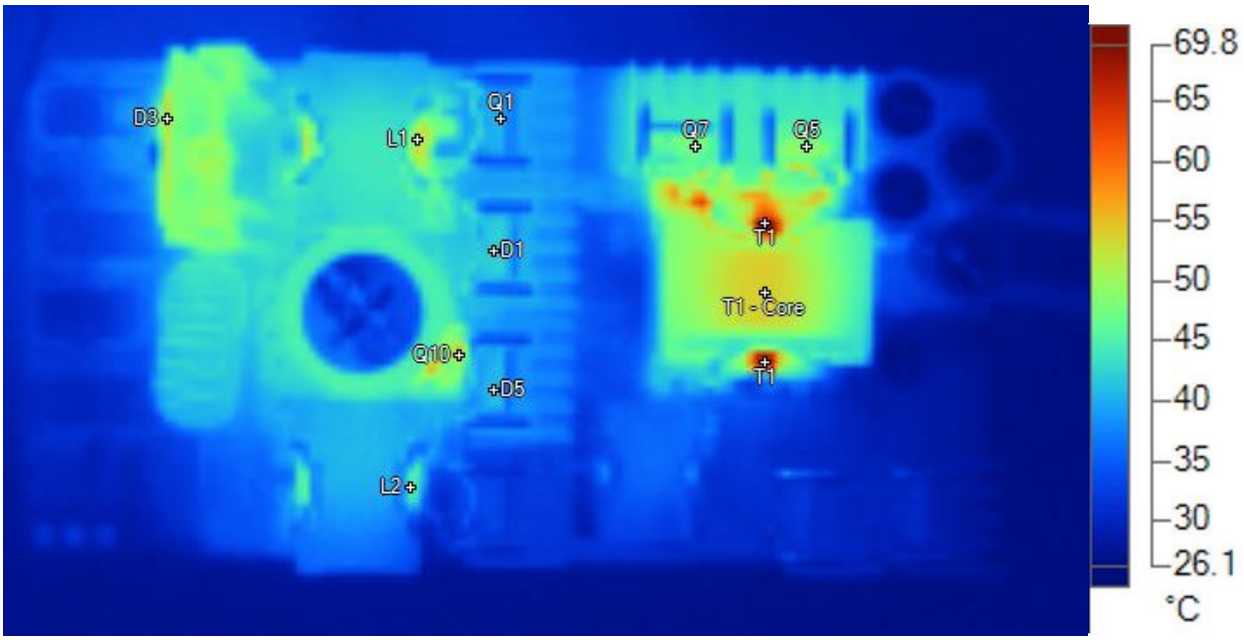
Vin = 115 VAC, f = 400 Hz, plug to plug and LLC efficiency					
Pin (W)	Vout (V)	Iout (A)	Pout (W)	Efficiency plug-to plug (%)	Efficiency LLC (%)
0.682	29.98	0.0000	0.00	0.00%	0.00%
6.165	29.98	0.0847	2.54	41.16%	47.34%
11.630	29.98	0.2104	6.31	54.21%	60.64%
23.131	29.98	0.5591	16.76	72.41%	79.04%
55.931	29.98	1.6202	48.57	86.77%	91.74%
111.03	29.98	3.3876	101.56	91.39%	95.47%
222.51	29.97	6.8704	205.91	92.45%	96.73%
446.17	29.97	13.713	410.99	92.03%	96.96%

Vin = 134 VAC, f = 400 Hz, plug to plug and LLC efficiency					
Pin (W)	Vout (V)	Iout (A)	Pout (W)	Efficiency plug-to plug (%)	Efficiency LLC (%)
0.688	29.98	0.0000	0.00	0.00%	0.00%
5.940	29.98	0.0853	2.56	43.05%	48.97%
11.810	29.98	0.2260	6.78	57.34%	62.76%
22.710	29.98	0.5696	17.08	75.14%	80.83%
56.218	29.98	1.6414	49.21	87.45%	92.20%
111.40	29.98	3.4188	102.50	91.92%	95.64%
220.81	29.97	6.8714	205.94	93.18%	96.83%
445.70	29.97	13.785	413.14	92.61%	96.96%

2.2 *Thermal Image*

The graphs and tables below show the thermal pictures of the converter supplied at 115 VAC and 400 Hz. Thermal shots have been taken after the board was running for 1 hour at ambient temperature of 25°C. The board runs at full load with a fan, blowing on the side (DC/DC output); the fan can be removed if the load is reduced to 300W (see second thermal shot and table).

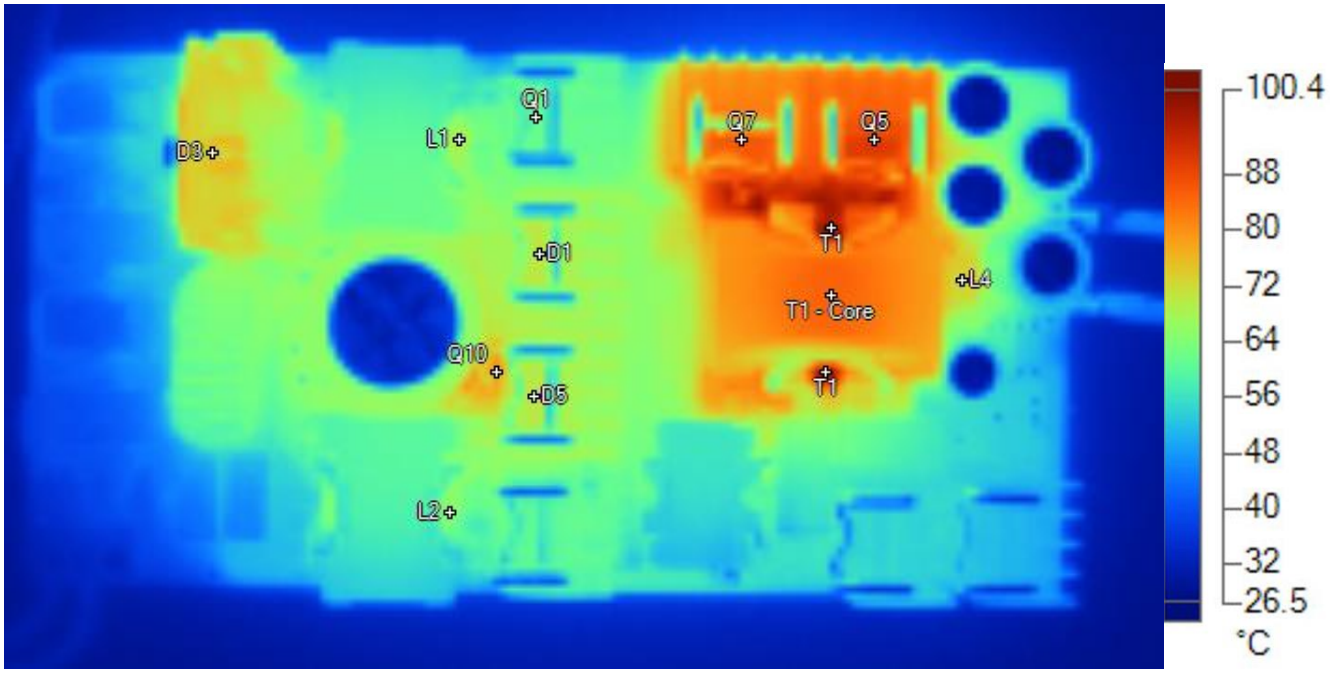
Conditions: mains voltage = 115 VAC, 400 Hz, full load, fan on right side.



Main Image Markers

Name	Temperature	Emissivity	Background
D3	53.4°C	0.96	25°C
L1	51.8°C	0.96	25°C
L2	45.2°C	0.96	25°C
Q10	55.4°C	0.96	25°C
T1	69.8°C	0.96	25°C
T1	67.3°C	0.96	25°C
T1 - Core	54.1°C	0.96	25°C
Q5	49.5°C	0.96	25°C
Q7	47.9°C	0.96	25°C
D1	42.2°C	0.96	25°C
D5	41.3°C	0.96	25°C
Q1	40.4°C	0.96	25°C

Conditions: mains voltage = 115 VAC, 400 Hz, 300 W load, natural convection



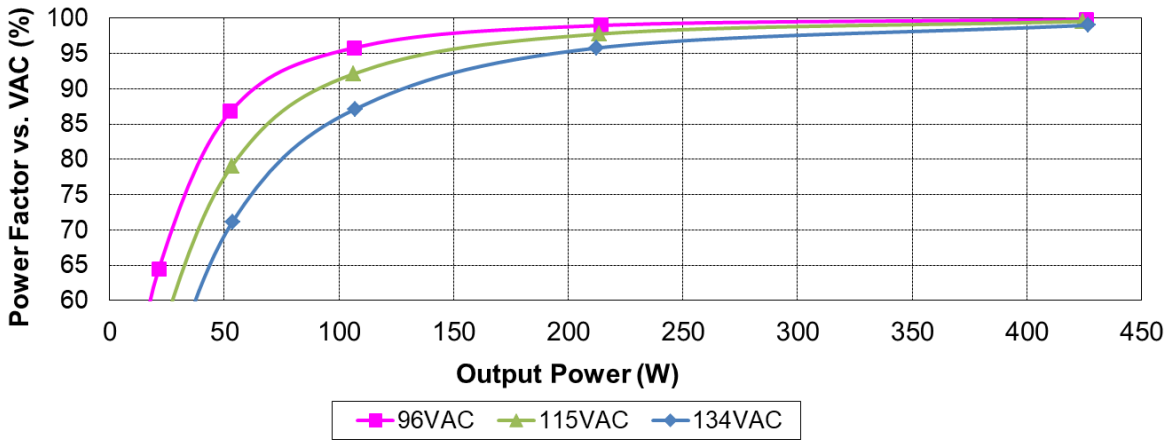
Main Image Markers

Name	Temperature	Emissivity	Background
T1	100.3°C	0.96	25°C
T1	97.7°C	0.96	25°C
T1 - Core	85.0°C	0.96	25°C
Q5	89.6°C	0.96	25°C
Q7	86.5°C	0.96	25°C
Q10	80.7°C	0.96	25°C
D5	70.0°C	0.96	25°C
L2	64.7°C	0.96	25°C
D1	70.5°C	0.96	25°C
Q1	61.3°C	0.96	25°C
L1	67.8°C	0.96	25°C
D3	75.0°C	0.96	25°C
L4	72.8°C	0.96	25°C

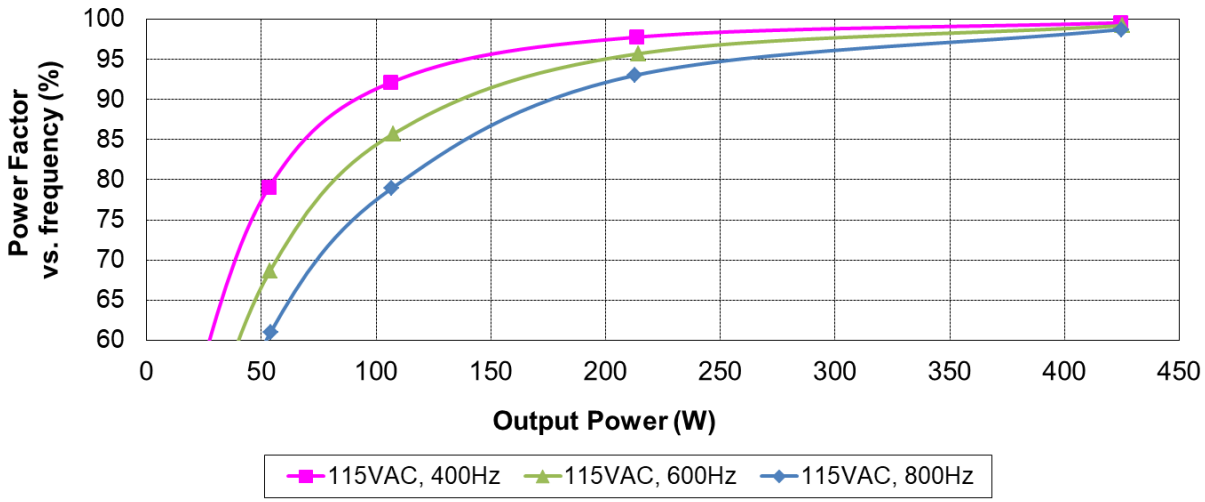
2.3 Power Factor versus Load, VAC and Frequency

The power factor value has been measured by varying the output power of the PFC stage (resistive) in the whole range, for different VAC and frequency range.

Conditions: mains voltage = 96 VAC, 115 VAC and 134 VAC, 400 Hz, 0 to 425 W load

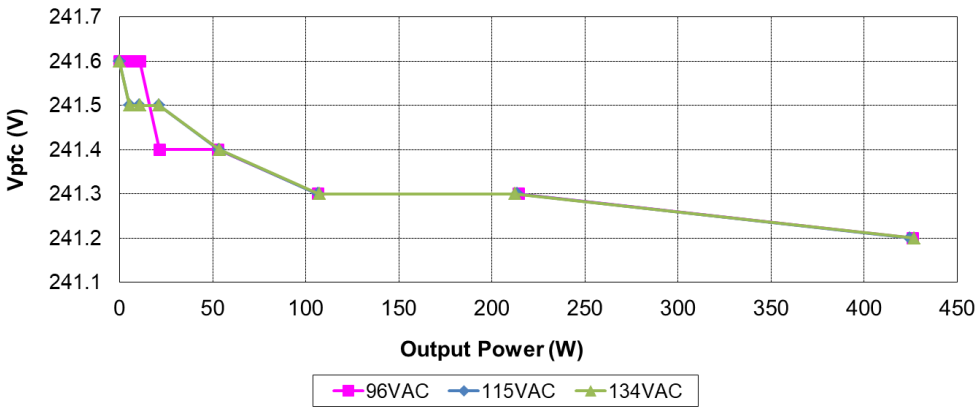


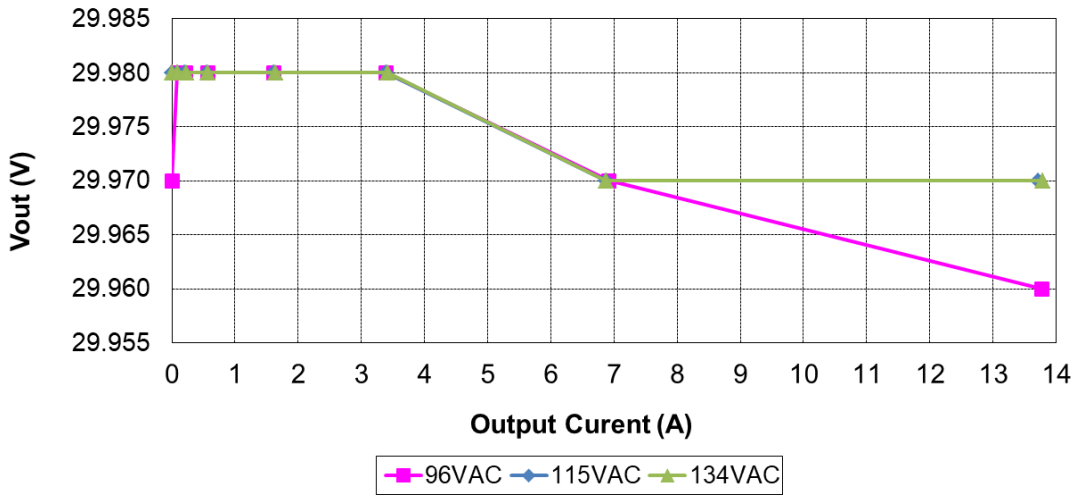
Conditions: mains voltage = 115 VAC, 400 Hz, 600 Hz and 800 Hz, 0 to 425 W load



2.4 Static Output Voltage Variation versus Load

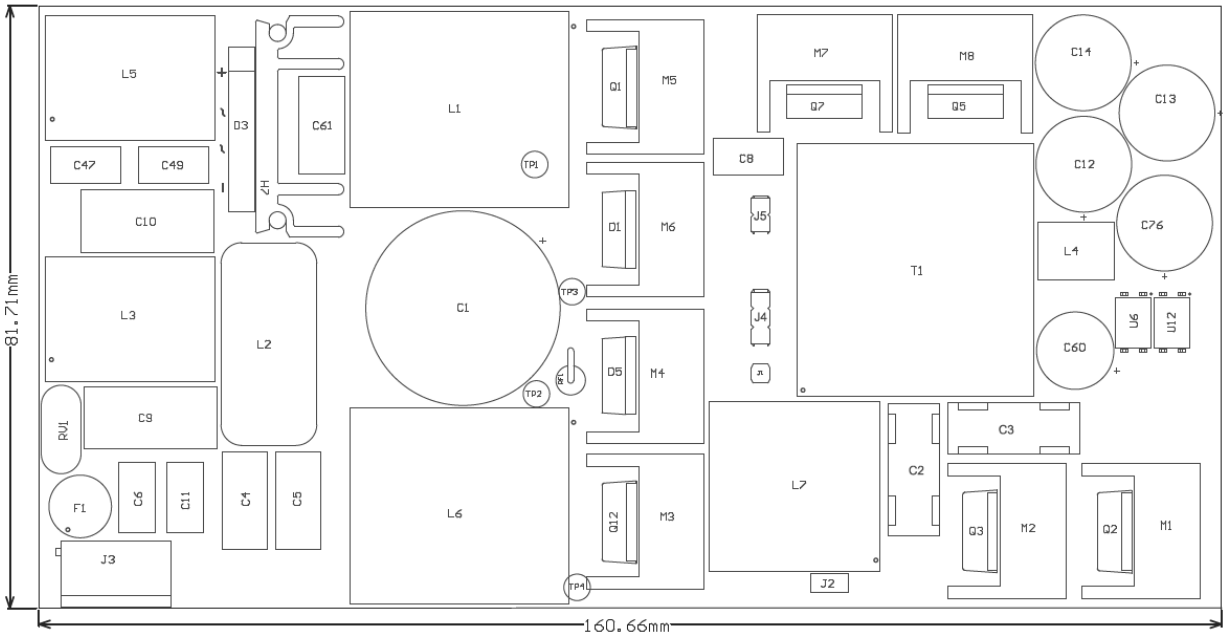
The output voltage regulation of both stages versus load current is shown in the graphs below.





2.5 Dimensions

The board dimensions are 160.66 mm x 81.71 mm, height 30 mm (with exception of H7, which is 50 mm)

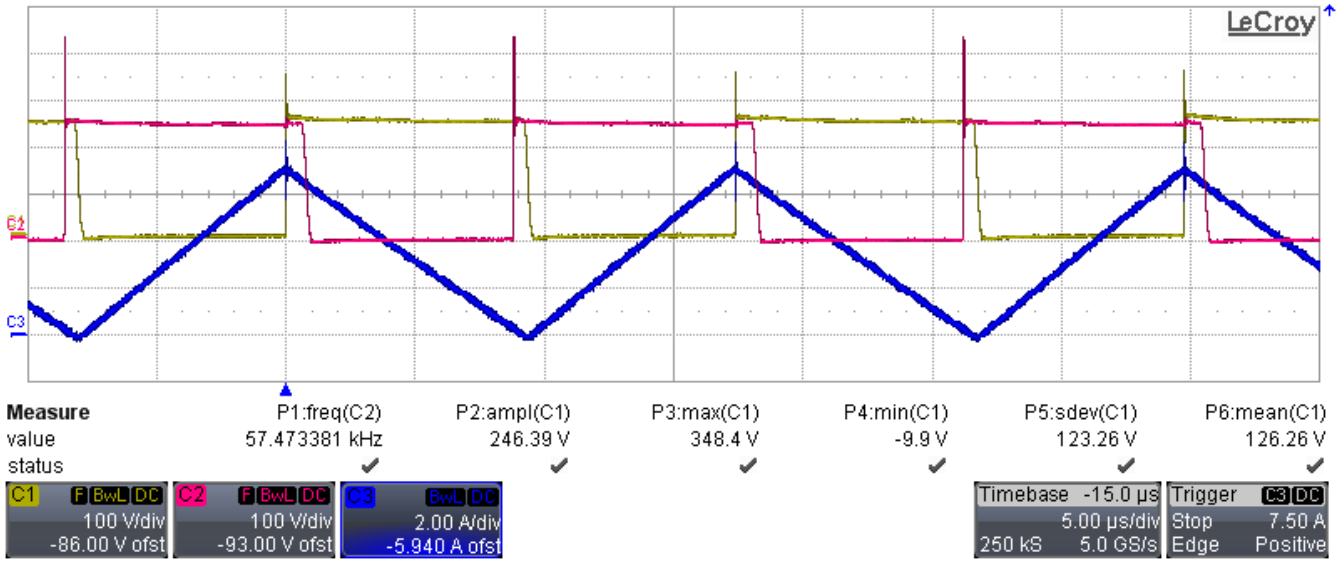


3 Waveforms

3.1.1 Switching Waveforms on FETs of PFC stage, at Full Load

The switching waveforms have been measured by supplying the converter at 96 VAC, 400 Hz at full load.

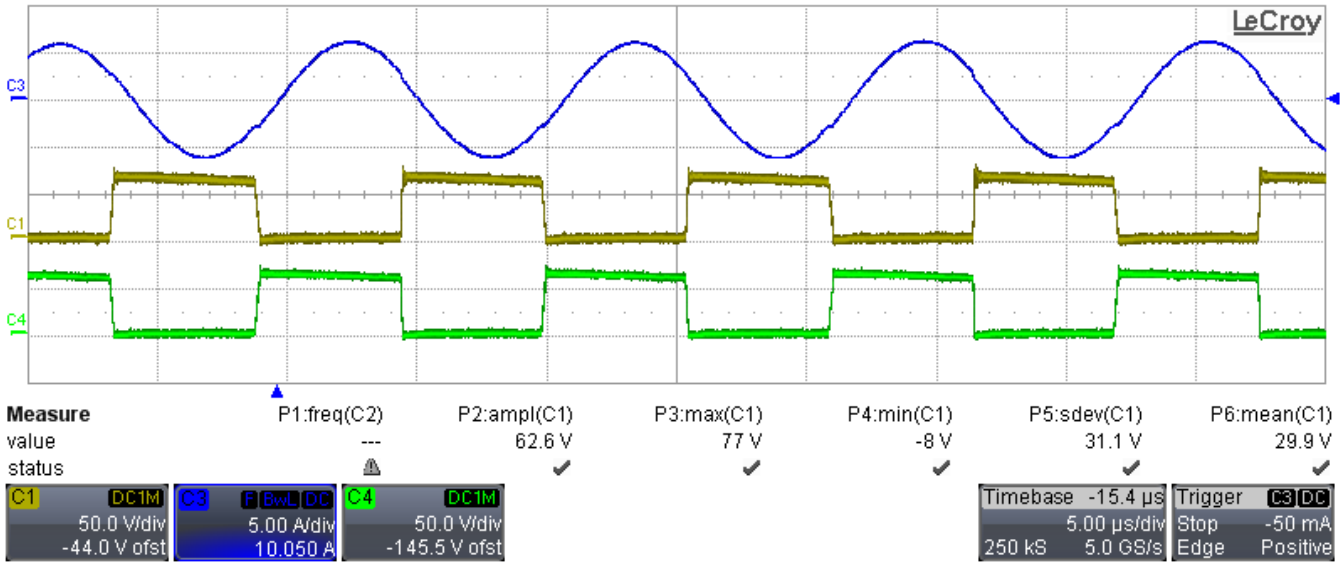
C1: Q12-Vds (100 V/div, 5 usec/div, 200 MHz BWL),
C2: Q1-Vds (100 V/div, 200 MHz BWL)
C3: I(L6) (2 A/div, 20 MHz BWL)



3.1.2 Switching Waveforms on Primary Side FETs and Sync FETs of LLC stage, at Full Load

The switching waveforms have been measured by supplying the converter at 115 VAC, 400 Hz & full load.

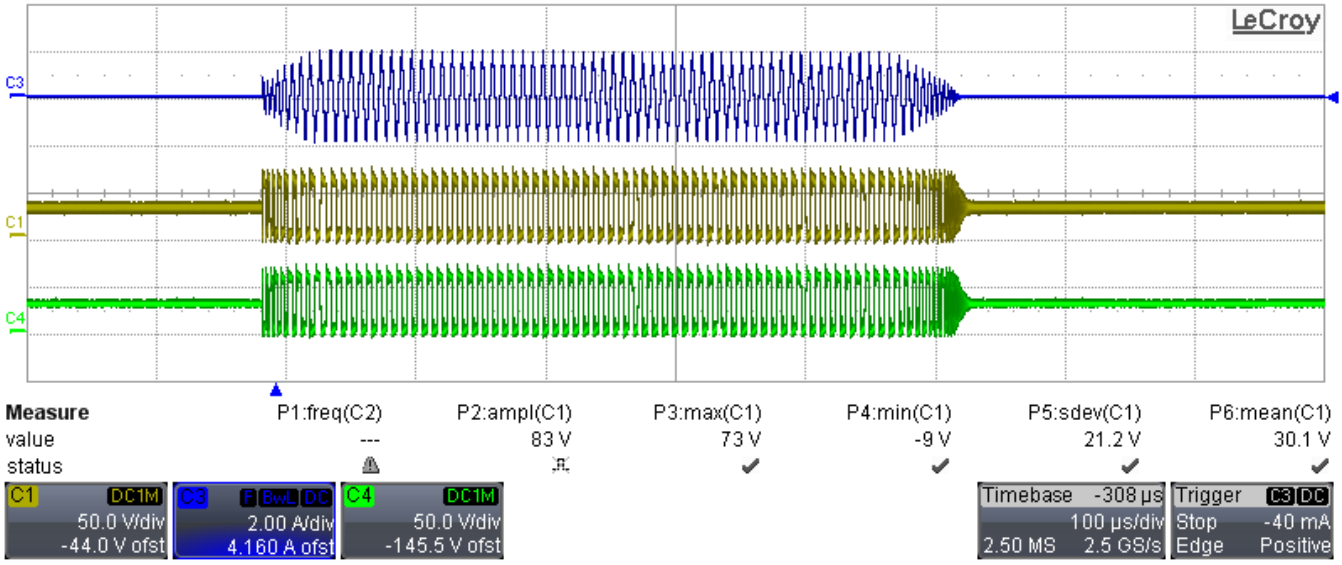
C1: Q7-Vds (50 V/div, 5 usec/div, no BWL),
C3: Resonant current, I(L7) (5 A/div, 200 MHz BWL)
C4: Q5-Vds (50 V/div, no BWL)



3.1.3 Switching Waveforms on Primary Side FETs and Sync FETs of LLC stage, in Burst Mode

Working conditions: 115 VAC, 400 Hz and 50mA load.

C1: Q7-Vds (50 V/div, 100 usec/div, no BWL),
C3: Resonant current, I(L7) (2 A/div, 200 MHz BWL)
C4: Q5-Vds (50 V/div, no BWL)

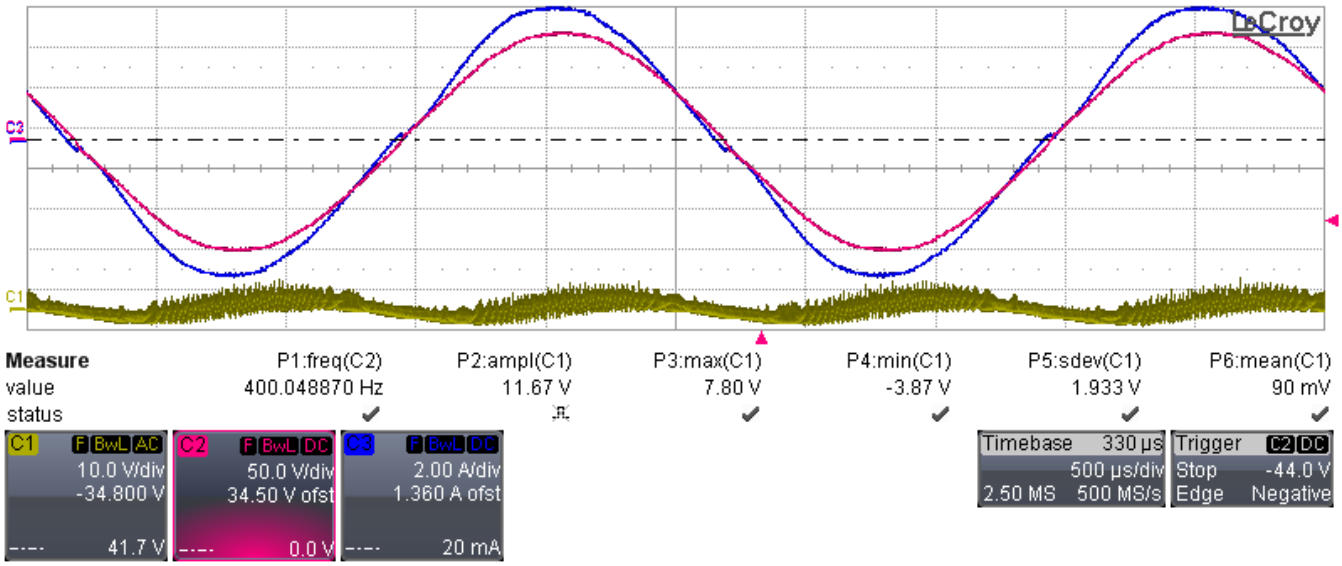


3.1.4 AC waveforms (Input Voltage, Input PFC Current and PFC Output Voltage)

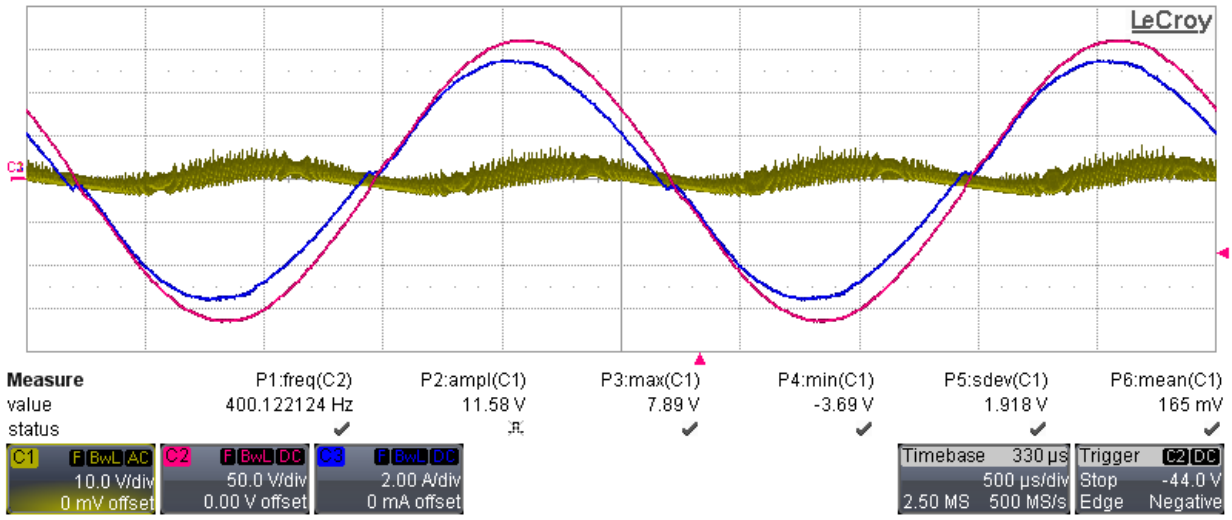
The screenshots shown below show the input voltage and current of the PFC stage, at 96 VAC, 115 VAC and 134 VAC, with mains frequency = 400 Hz, 600 Hz and 800 Hz in full load condition (all waveforms with 20 MHz BWL).

The following setup of the scope has been used for all waveforms of this section 3.1.4, which are:
C1: PFC output voltage (10 V/div, 500 usec/div, AC coupling), C2: AC input voltage (50 V/div (or 100 V/div), DC coupling), C3: AC input current (2 A/div, DC coupling).

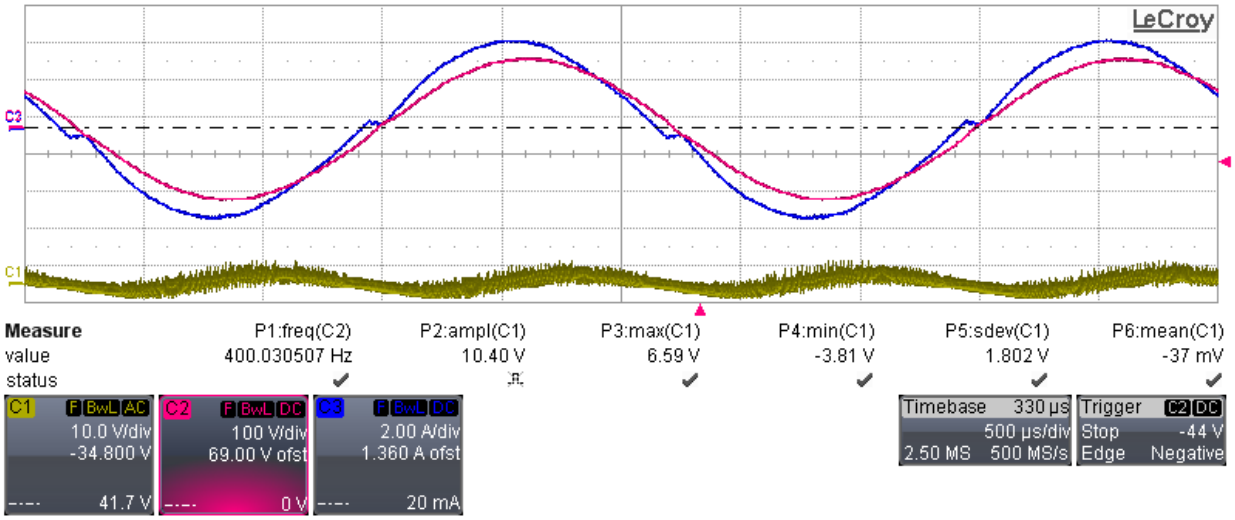
Vin = 96 VAC, 400 Hz



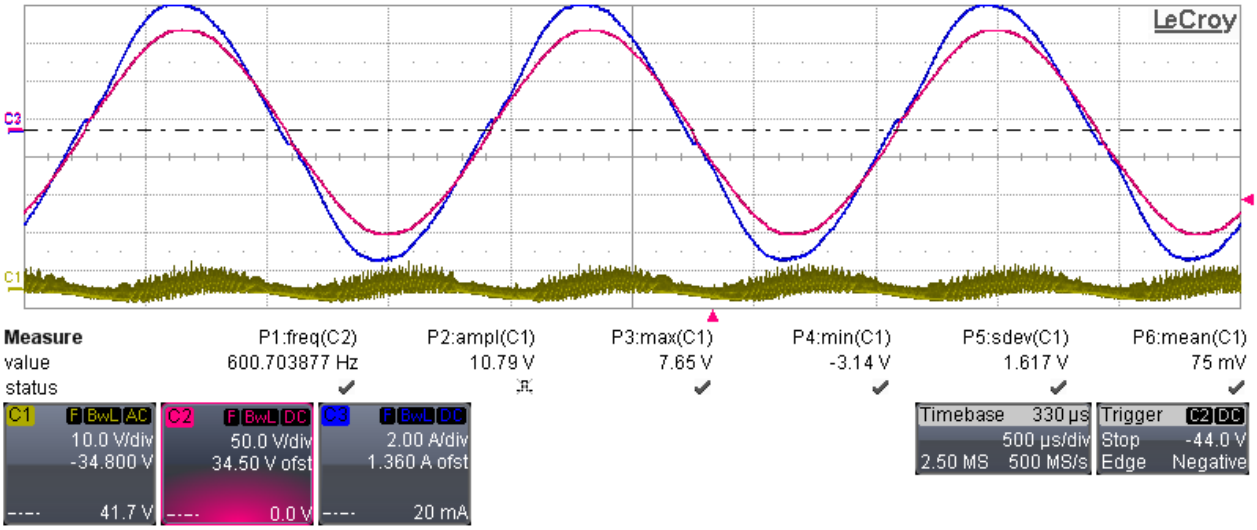
Vin = 115 VAC, 400 Hz



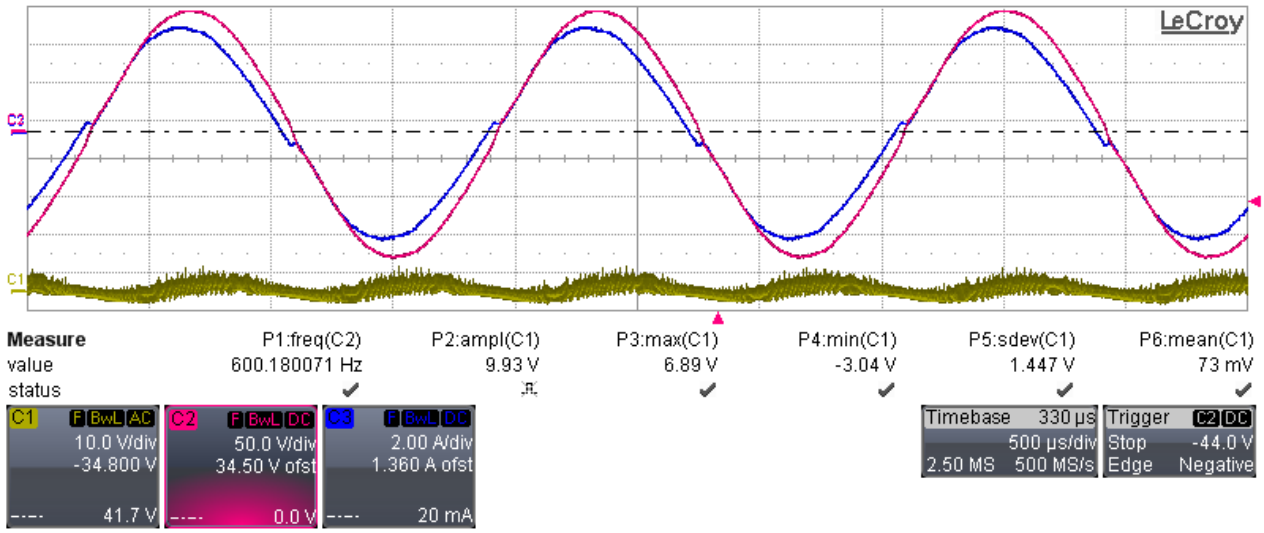
Vin = 134 VAC, 400 Hz



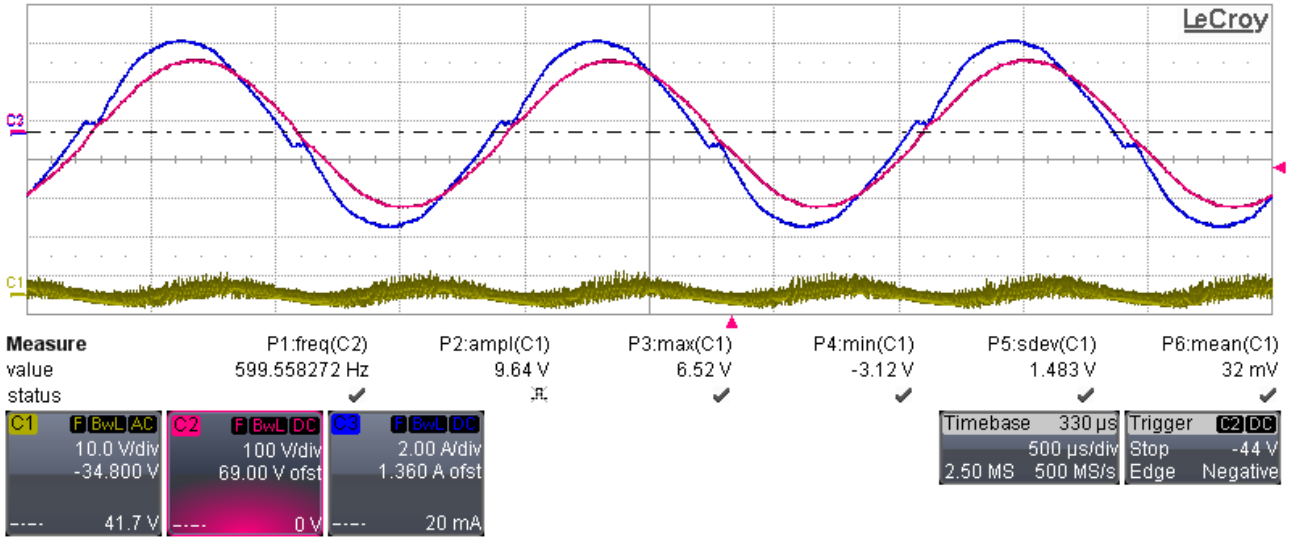
Vin = 96 VAC, 600 Hz



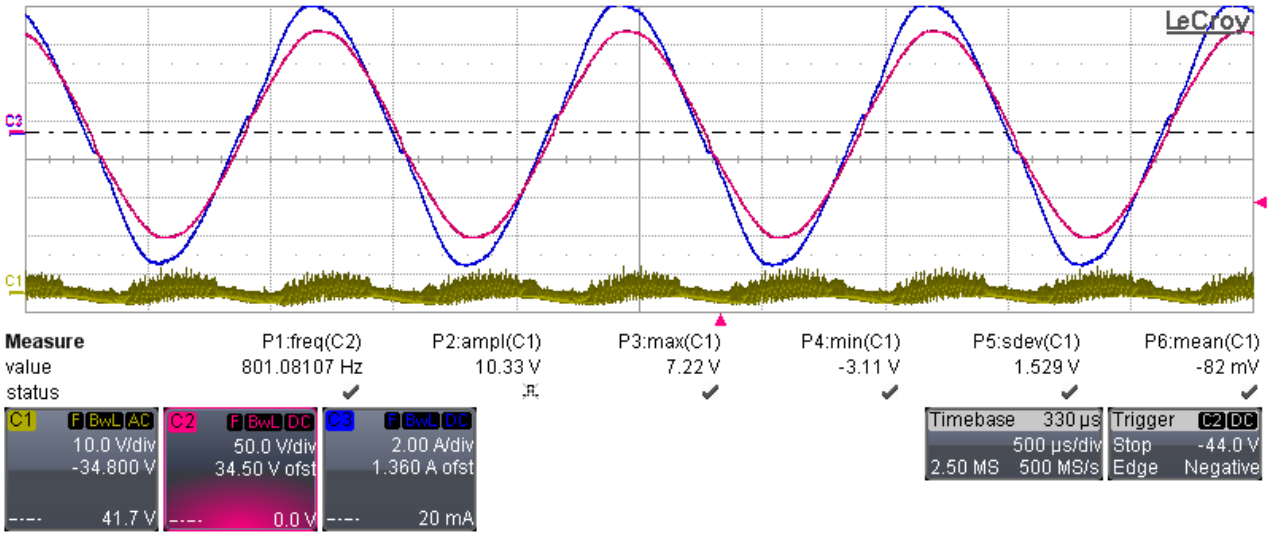
Vin = 115 VAC, 600 Hz



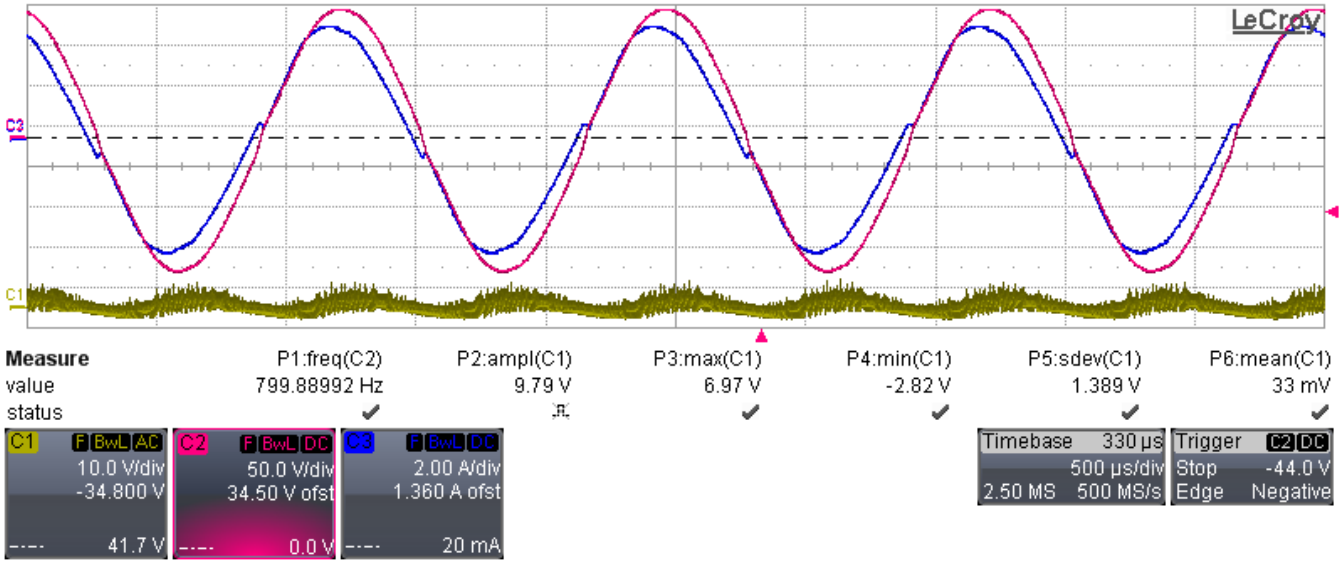
Vin = 134 VAC, 600 Hz



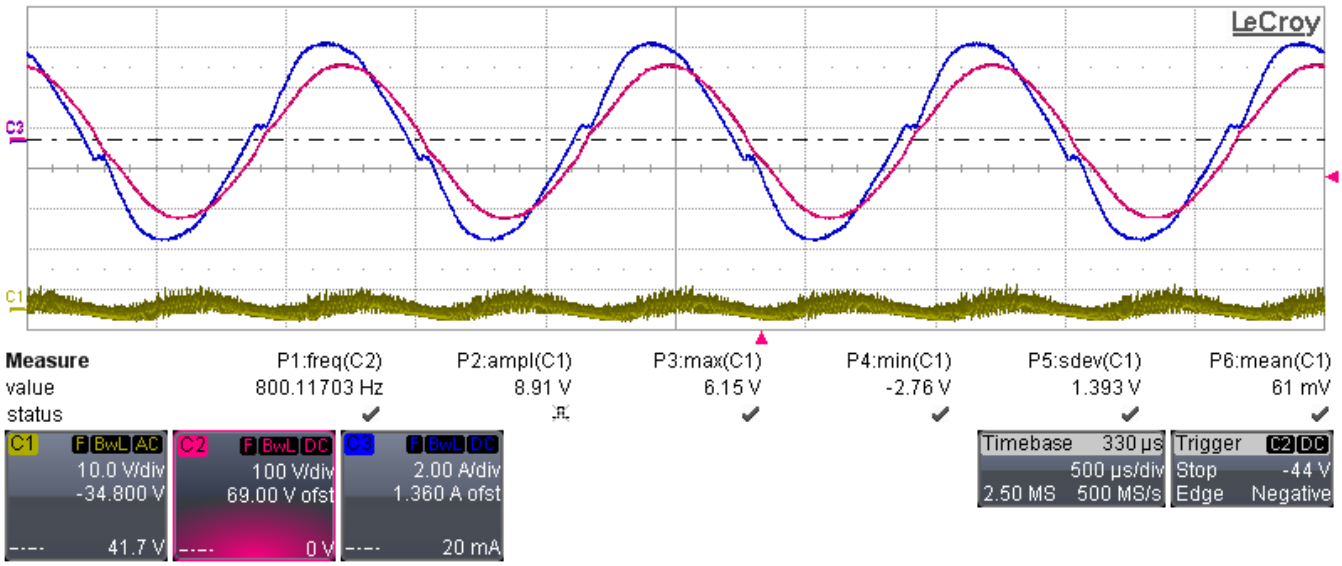
Vin = 96 VAC, 800 Hz



Vin = 115 VAC, 800 Hz



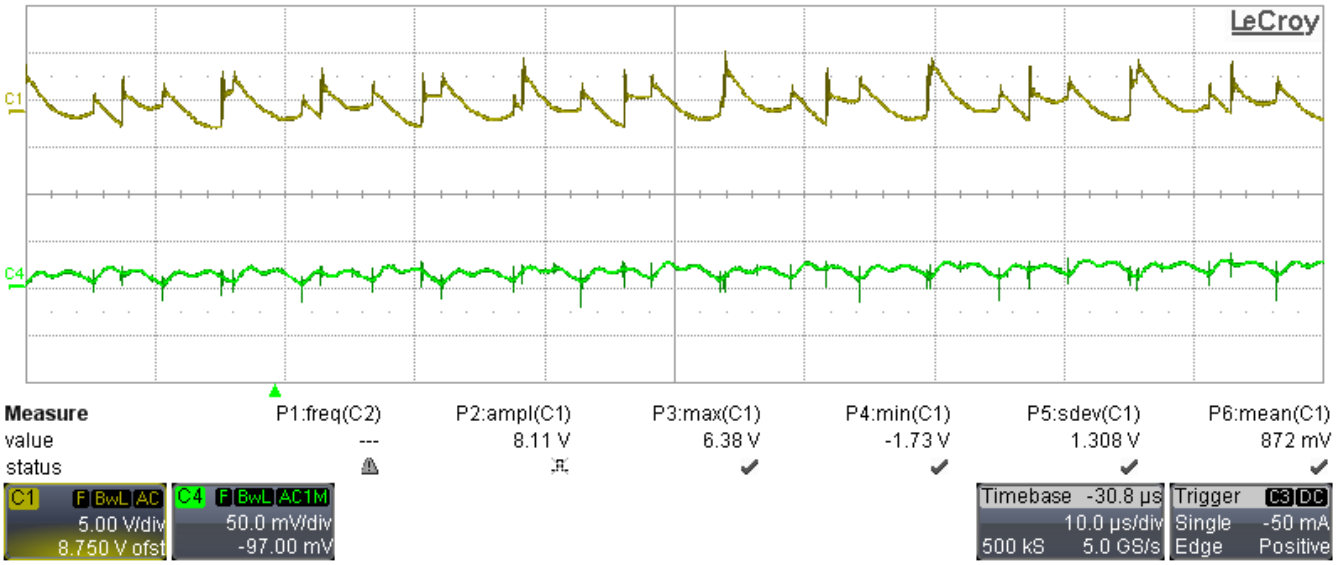
Vin = 134 VAC, 800 Hz



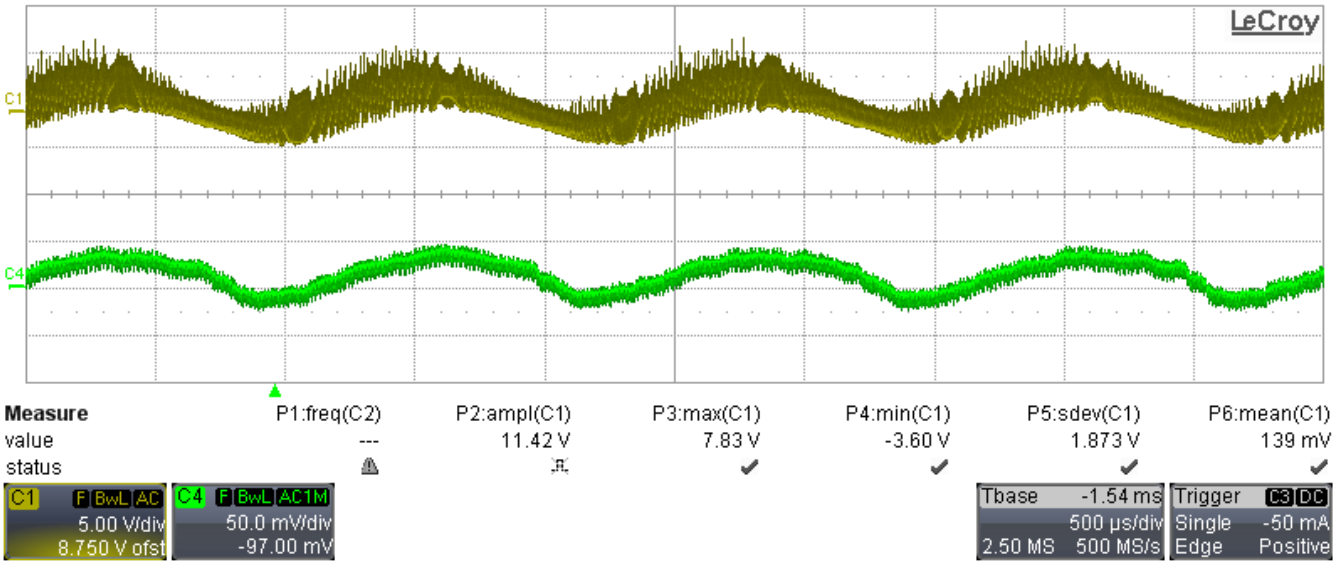
3.2 Output Voltage Ripple

The 30V and PFC output voltage ripple has been measured by supplying the converter at 115 VAC, 400 Hz at full load; the bandwidth limit of the scope (BWL) has been set to 20 MHz.

C1: PFC voltage (5 V/div, 10 usec/div, AC coupling)
C4: 30Vout (50 mV/div, AC coupling)



Same waveform but with longer time division, showing details about low frequency ripple.
C1: PFC voltage (5 V/div, 500 usec/div, AC coupling)
C4: 30Vout (50 mV/div, AC coupling)

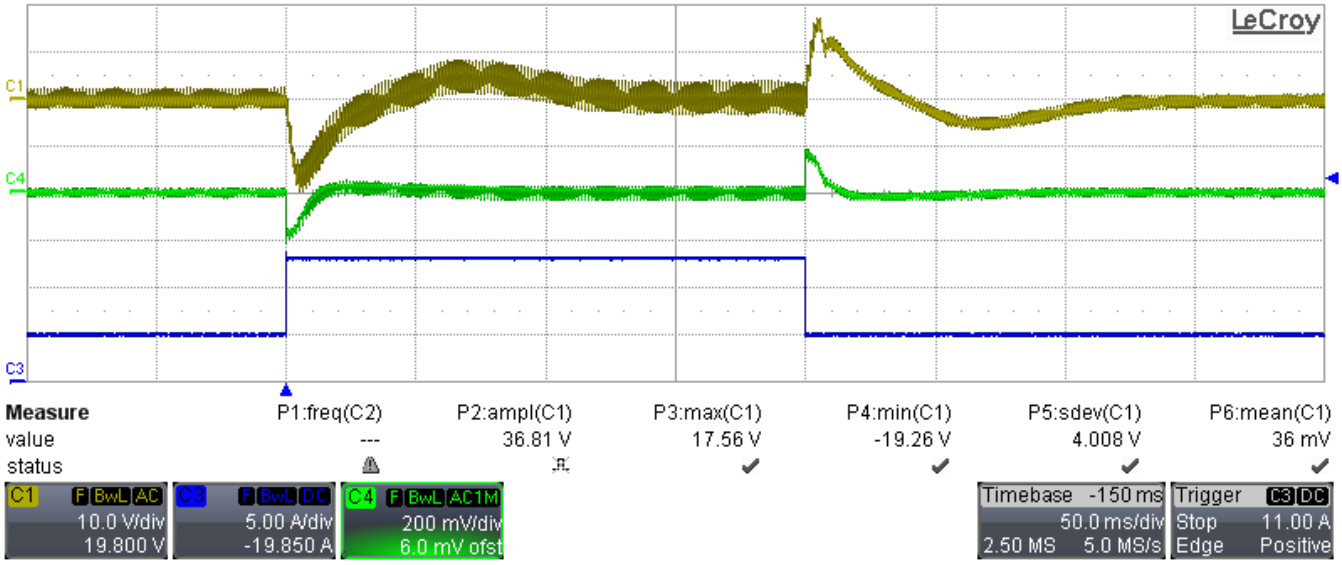


3.3 Load Transients

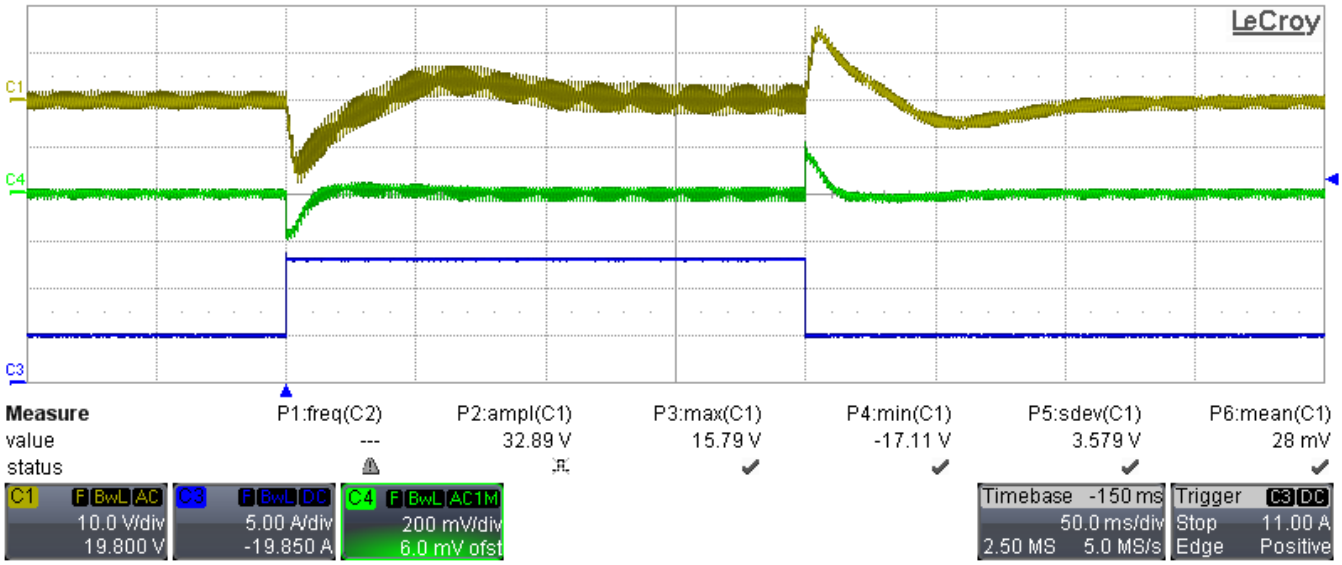
The output and PFC voltage variation, during load transients, has been measured by supplying the converter at 96 VAC, 115 VAC and 134 VAC, 400 Hz and 800 Hz. The load has been switched between 5 A and 13 A. For all waveforms the bandwidth limit of the oscilloscope has been set to 20 MHz.

The following setup of the scope has been used for all waveforms of this section 3.3, which are:
C1: PFC Voltage (10 V/div, 50 msec/div, AC coupling)
C3: Output current (5 A/div, DC coupling)
C4: 30Vout (200 mV/div, AC coupling)

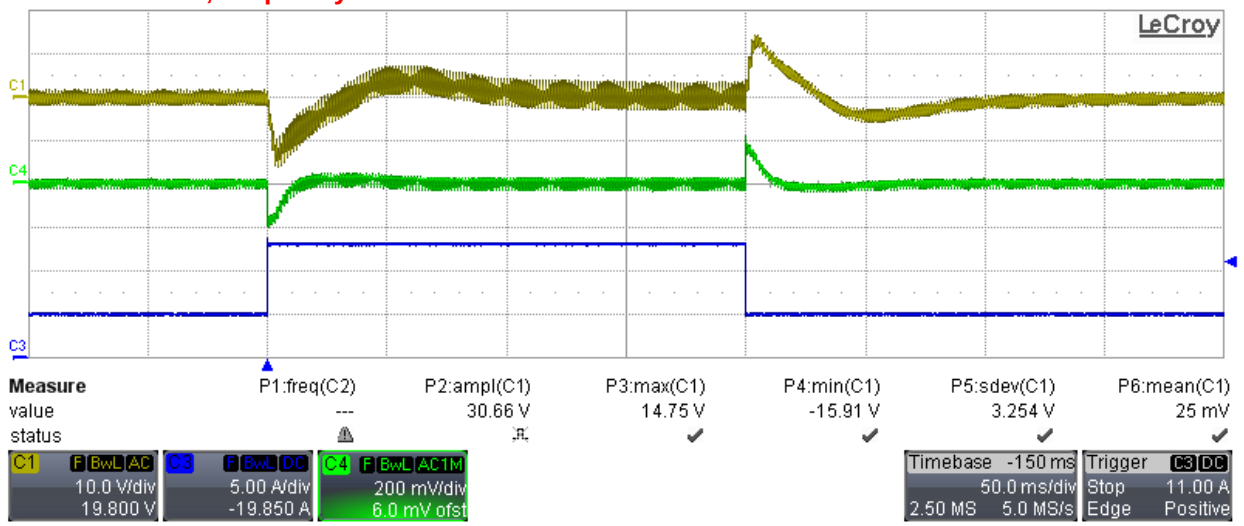
Vin = 96 VAC, frequency = 400 Hz



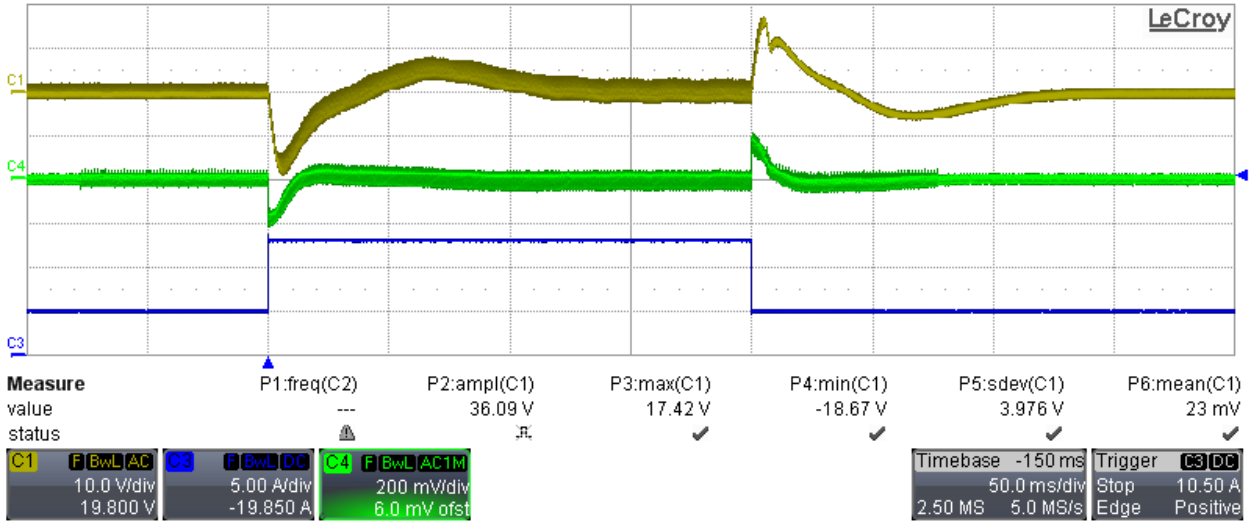
Vin = 115 VAC, frequency = 400 Hz



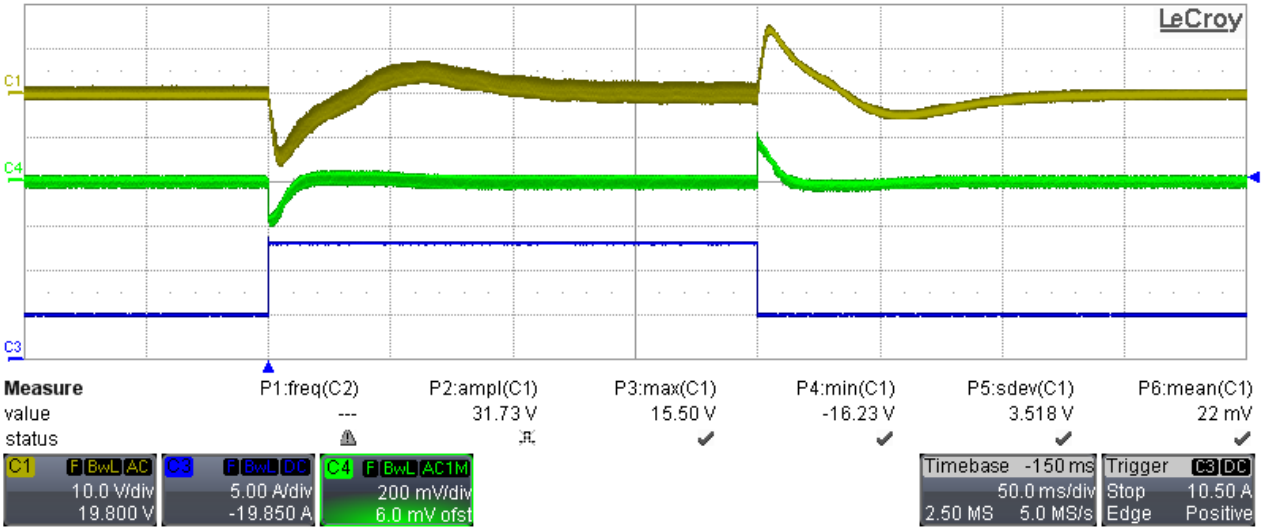
Vin = 134 VAC, frequency = 400 Hz



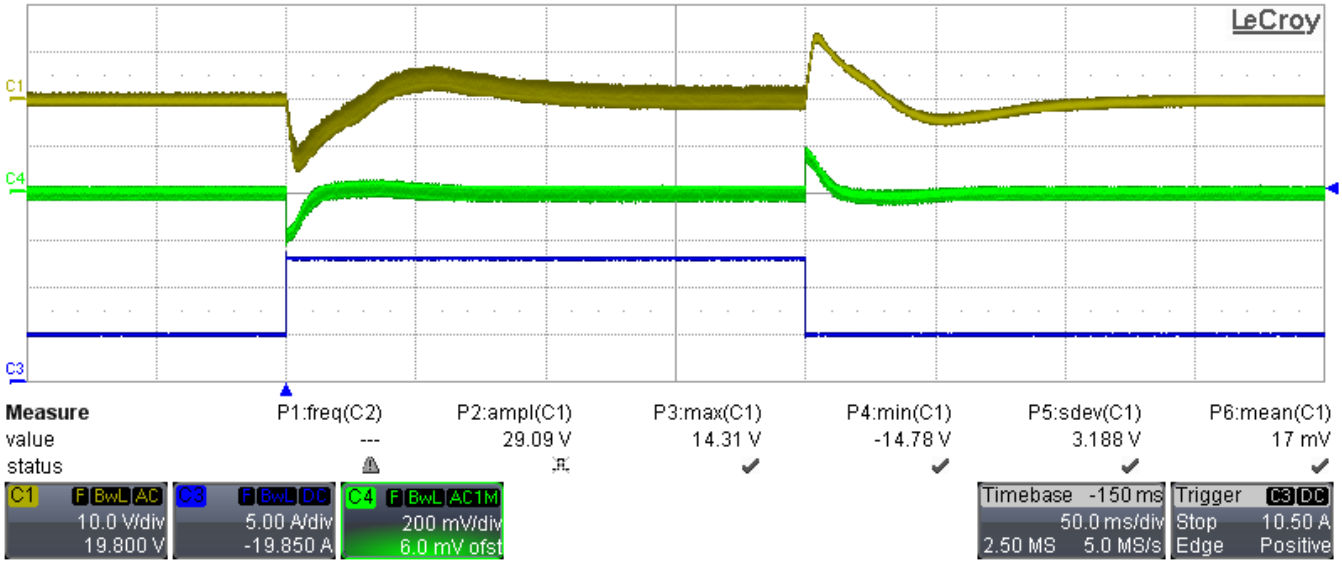
Vin = 96 VAC, frequency = 800 Hz



Vin = 115 VAC, frequency = 800 Hz



Vin = 134 VAC, frequency = 800 Hz

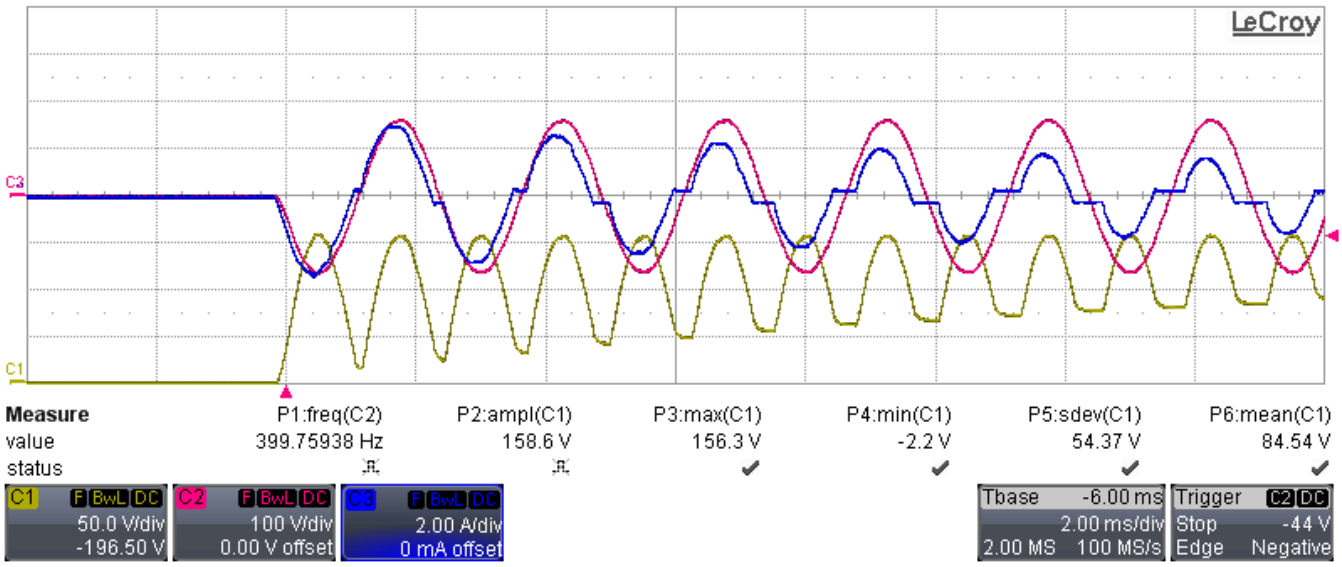


3.4 Inrush Current, Startup and Shutdown

3.4.1 Inrush Current

During this test, the AC source has been turned on and input current and voltage, as well as the PFC voltage, have been measured (with 20 MHz BWL).

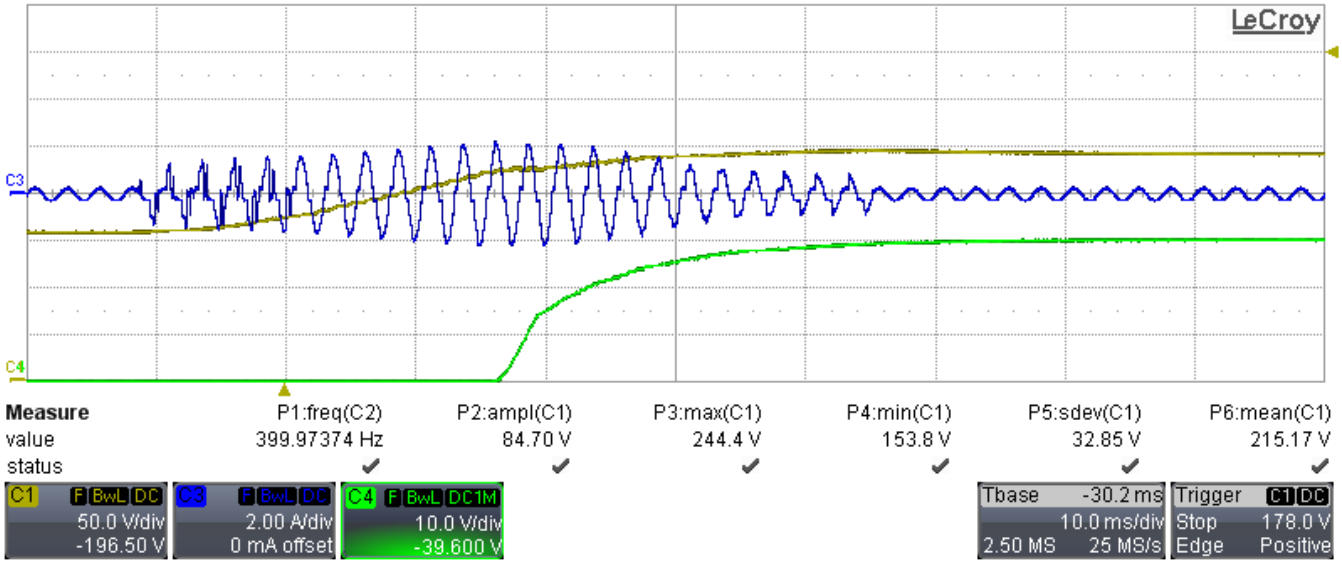
C1: PFC Voltage (50 V/div, 2 msec/div, DC coupling)
C2: Input AC voltage (100 V/div, DC coupling)
C3: Input AC current (2 A/div, DC coupling)
Vin = 115VAC, 400 Hz, no load



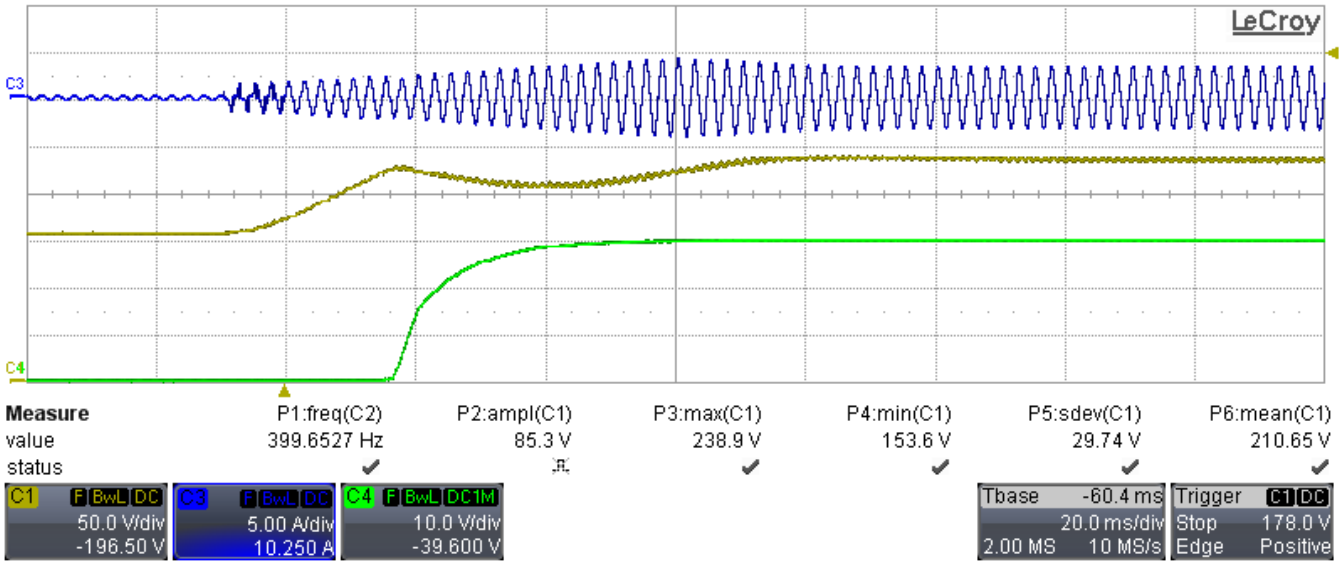
3.4.2 Startup

After the Vcc capacitor C60 is charged, the converter starts up, supplying the LLC and PFC stage. Here Vin was 115 VAC and the frequency = 400 Hz. Two screenshots have been taken, in no-load condition and 8 A load.

C1: PFC Voltage (50 V/div, 10 msec/div, DC coupling)
C3: Input AC current (2 A/div, DC coupling)
C4: 30Vout (10 V/div, DC coupling)
Vin = 115VAC, 400 Hz, no load



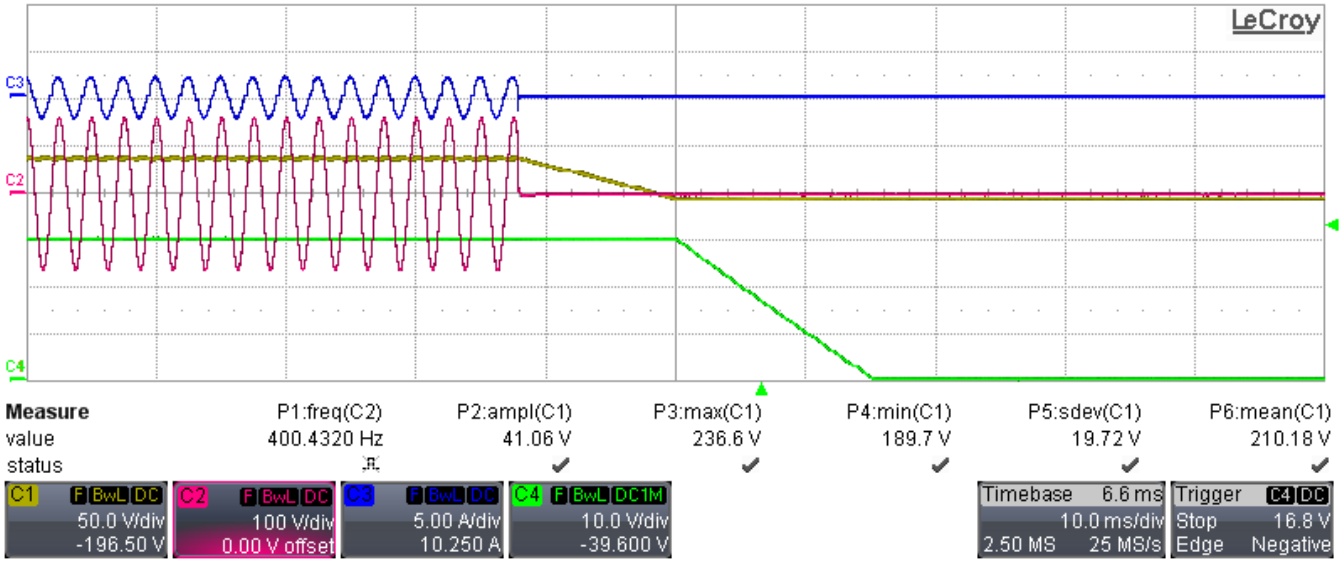
C1: PFC Voltage (50 V/div, 10 msec/div, DC coupling)
C3: Input AC current (2 A/div, DC coupling)
C4: 30Vout (10 V/div, DC coupling)
Vin = 115VAC, 400 Hz, 8 A load



3.4.3 Shutdown

The output voltage of 30Vout and PFC stage have been measured by switching off the AC voltage source while the load was set to 5A, Vin to 115 VAC and the frequency to 400 Hz.

C1: PFC Voltage (50 V/div, 10 msec/div, DC coupling), C2: Input AC voltage (100 V/div, DC coupling)
C3: Input AC current (5 A/div, DC coupling), C4: 30Vout (10 V/div, DC coupling)



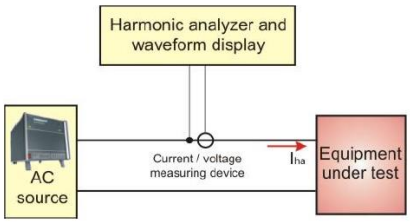
3.5 Input AC Current Measurements: compliance to DO160 Harmonic Limits

All harmonics have been tested according to the extract from DO-160 limits shown below.
In details, the first harmonic (fundamental) of the current should be measured at full load and minimum VAC (in this case 96VAC).
All measurements have been performed at full load and 115VAC (normal steady state condition), by considering the fundamental current previously measured.
The mains frequency has been varied in the range 360Hz….800Hz in 40Hz steps.
A difference from the following limits, for this case, is that for all even harmonics with order > 4 it should be considered an absolute limit of 5mA, regardless on the order number.

Extract from norm DO-160:

16.7.1.2 Current Harmonics limits for Single – Phase Equipment

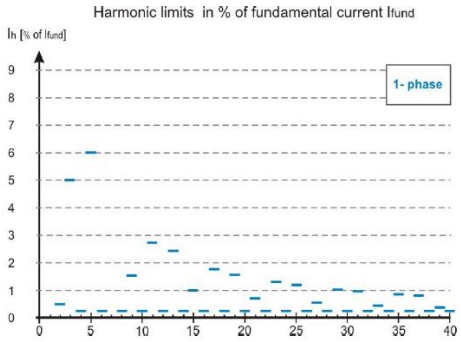
Harmonic Order	Limits
Odd Non Tripplen Harmonics (h= 5, 7, 11, 13,...,37)	$I_h = 0.3 \cdot I_1 / h$
Odd Tripplen Harmonics (h= 3, 9, 15, 21,...,39)	$I_h = 0.15 \cdot I_1 / h$
Even Harmonics 2 and 4	$I_h = 0.01 \cdot I_1 / h$
Even Harmonics > 4 (h= 6, 8, 10,...,40)	$I_h = 0.0025 \cdot I_1 / h$



I_1 = **Maximum fundamental equipment current** during max. steady state power demand at a single test frequency (360Hz, 400Hz, 650Hz, 800Hz) . This maximum shall be used for calculate the harmonic limits.

h = order of harmonic

I_h = Maximum harmonic current of order h obtained for all normal steady states modes of operation.



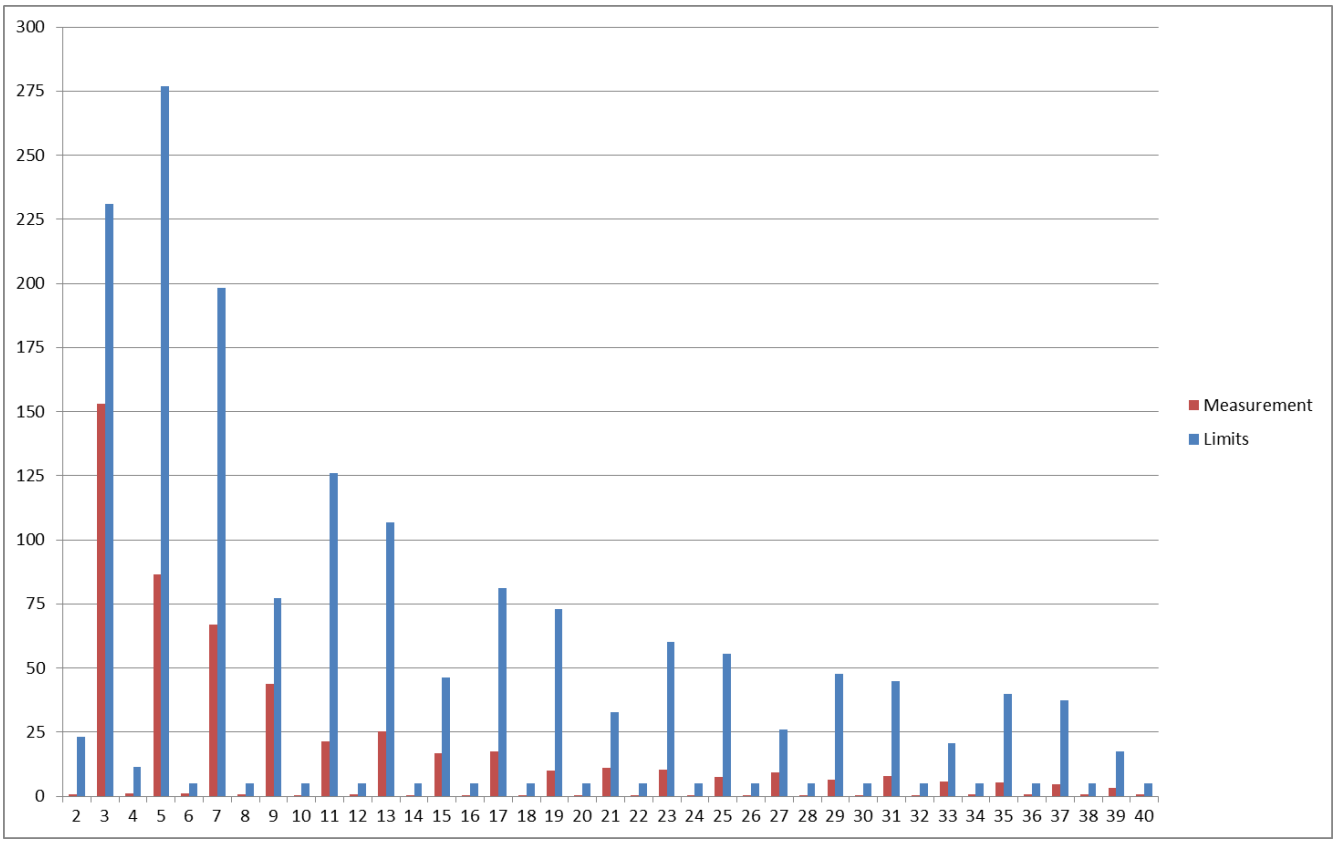
Details:

	Limit %					
Frequencies for test:	Harmonic order		Odd non-Triplen	Odd Triplen	Even 2 and 4	Even > 4
360Hz, 400 Hz, 650 Hz, 800 Hz	1					
	2				0.50	
	3			5.00		
	4				0.25	
	5		6.00			
	6					0.0417
	7		4.29			
	8					0.0313
	9			1.67		
	10					0.0250

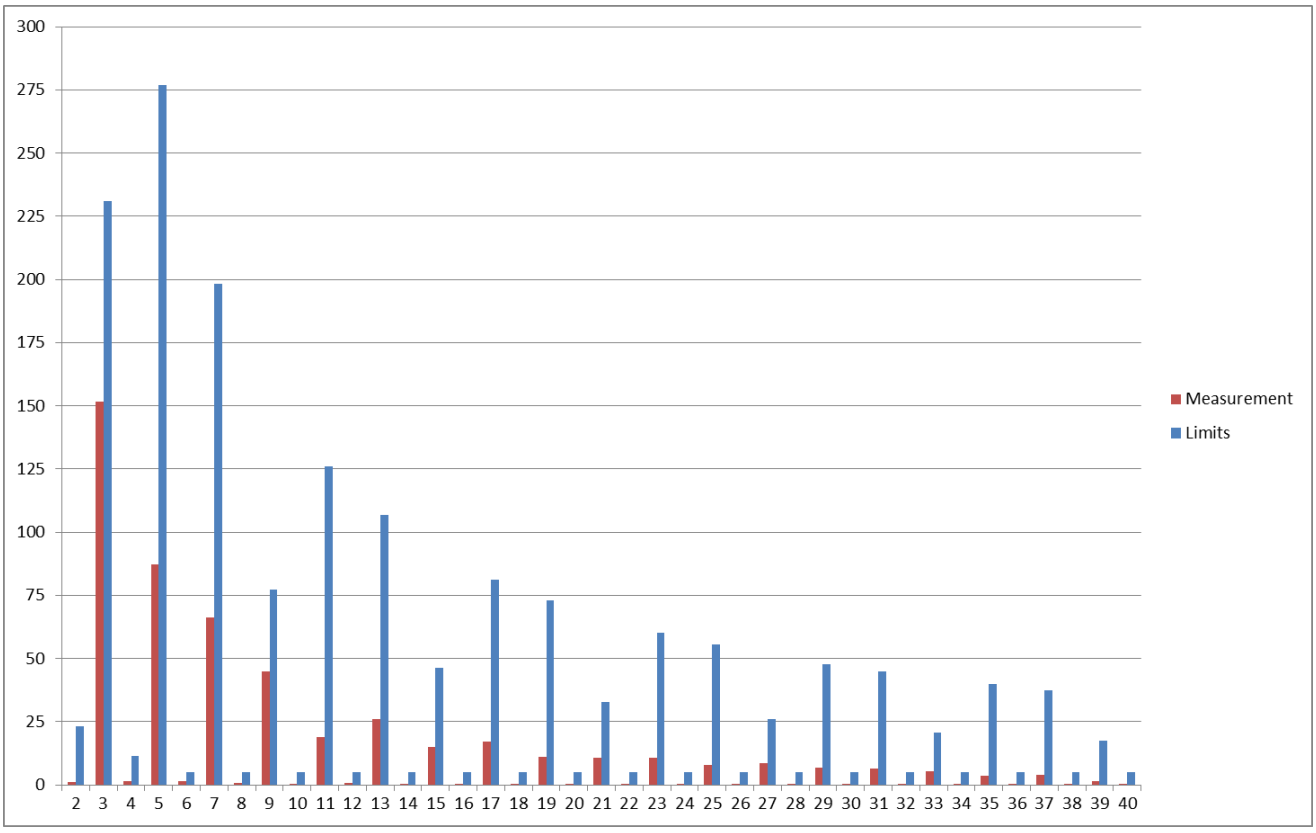
11		2.73			
12					0.0208
13		2.31			
14					0.0179
15			1.00		
16					0.0156
17		1.76			
18					0.0139
19		1.58			
20					0.0125
21			0.71		
22					0.0114
23		1.30			
24					0.0104
25		1.20			
26					0.0096
27			0.56		
28					0.0089
29		1.03			
30					0.0083
31		0.97			
32					0.0078
33			0.45		
34					0.0074
35		0.86			
36					0.0069
37		0.81			
38					0.0066
39			0.38		
40					0.0063

Below are shown all measurements (for details, please refer to the excel sheets) for each mains frequency, showing the absolute value of the current, express in mA_{RMS}, versus harmonic order.

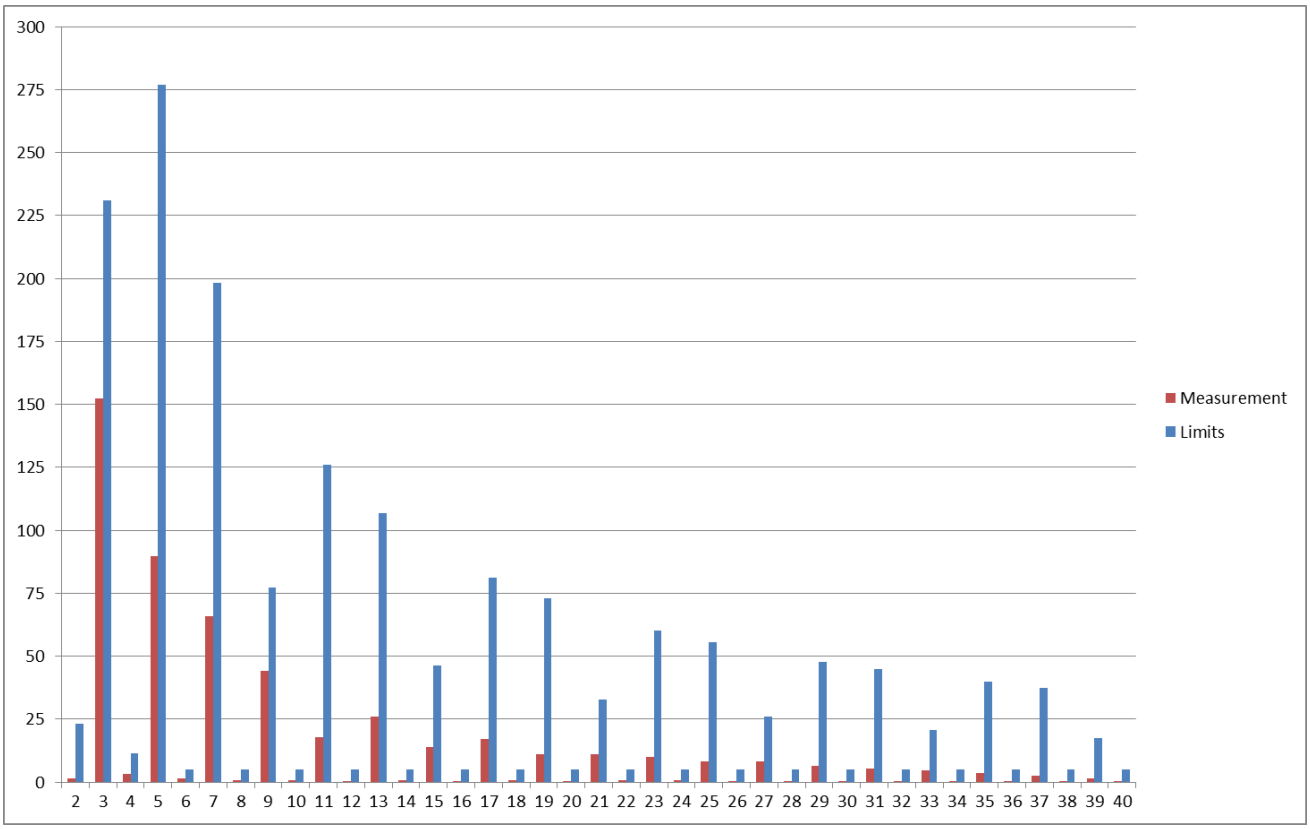
F = 360 Hz



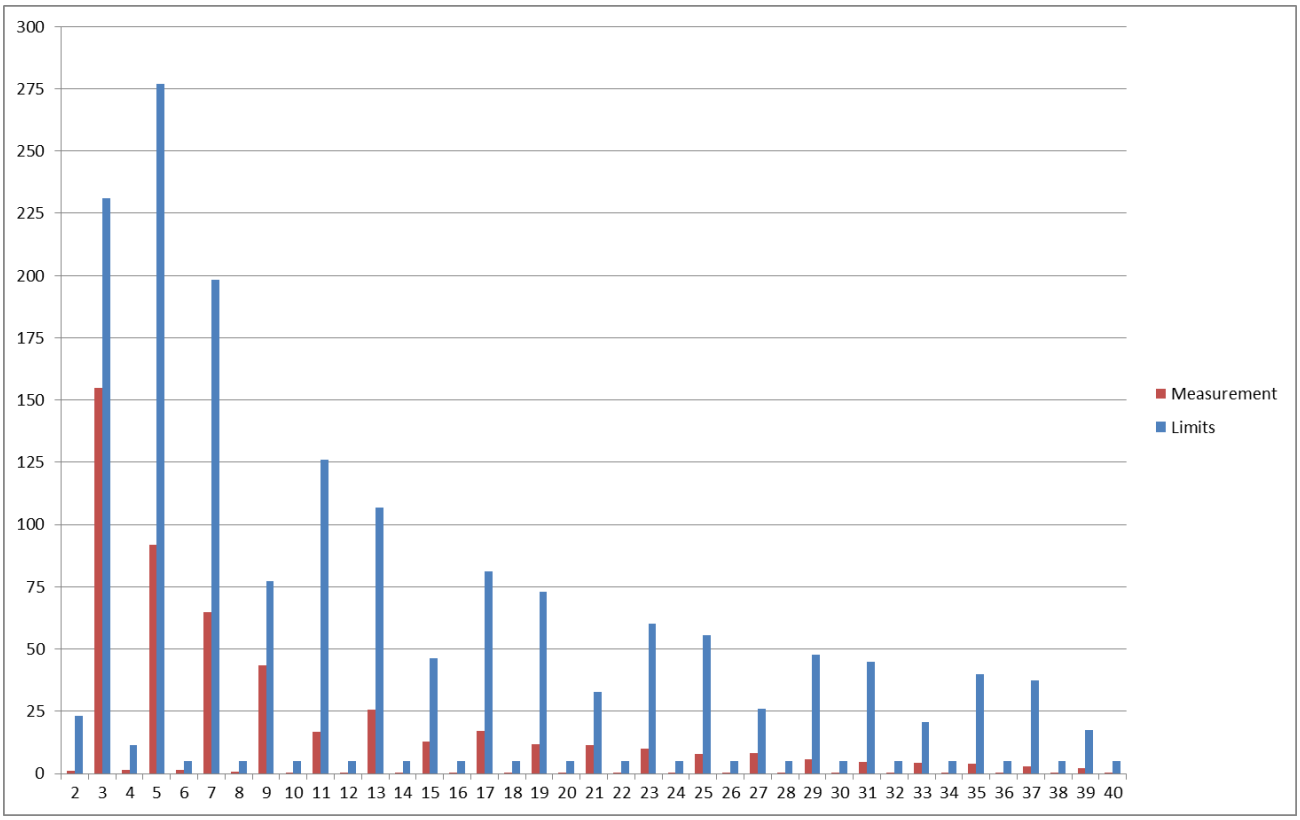
F = 400 Hz



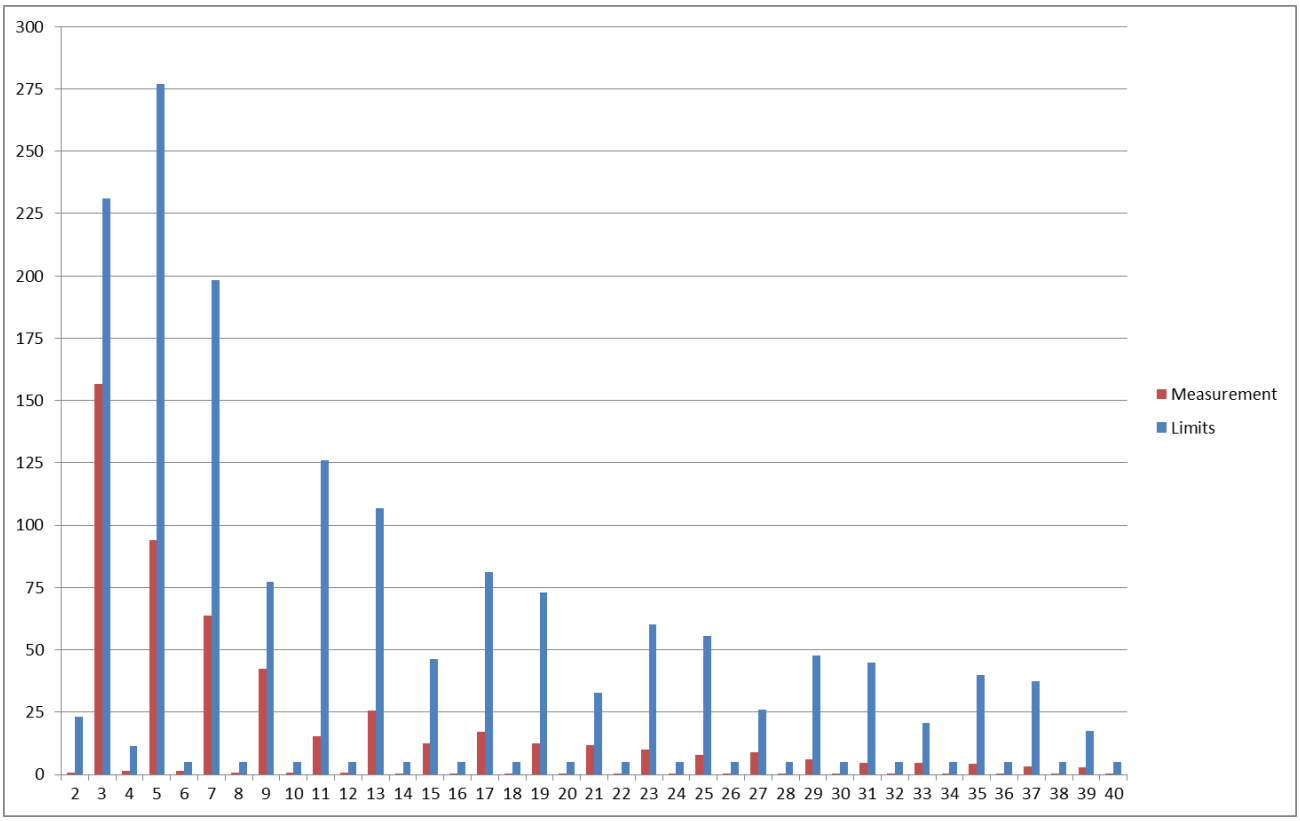
F = 440 Hz



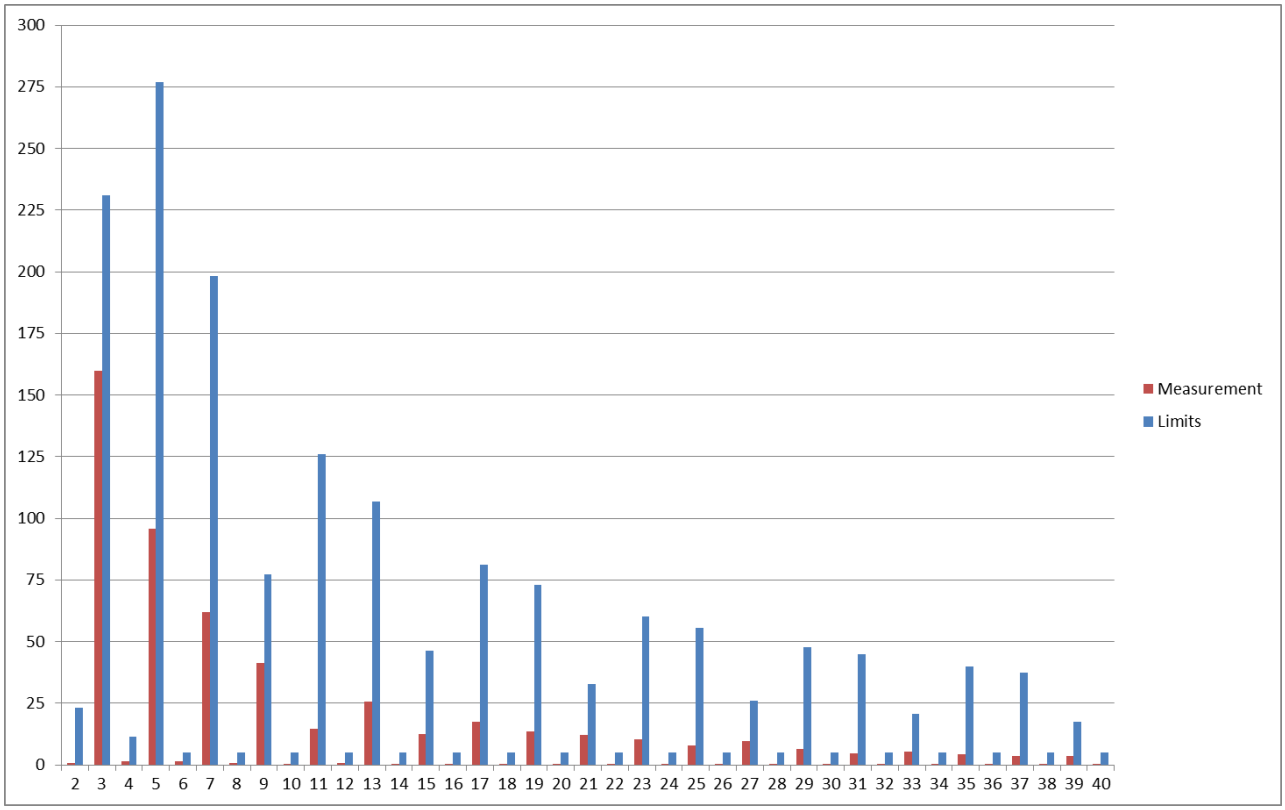
F = 480 Hz



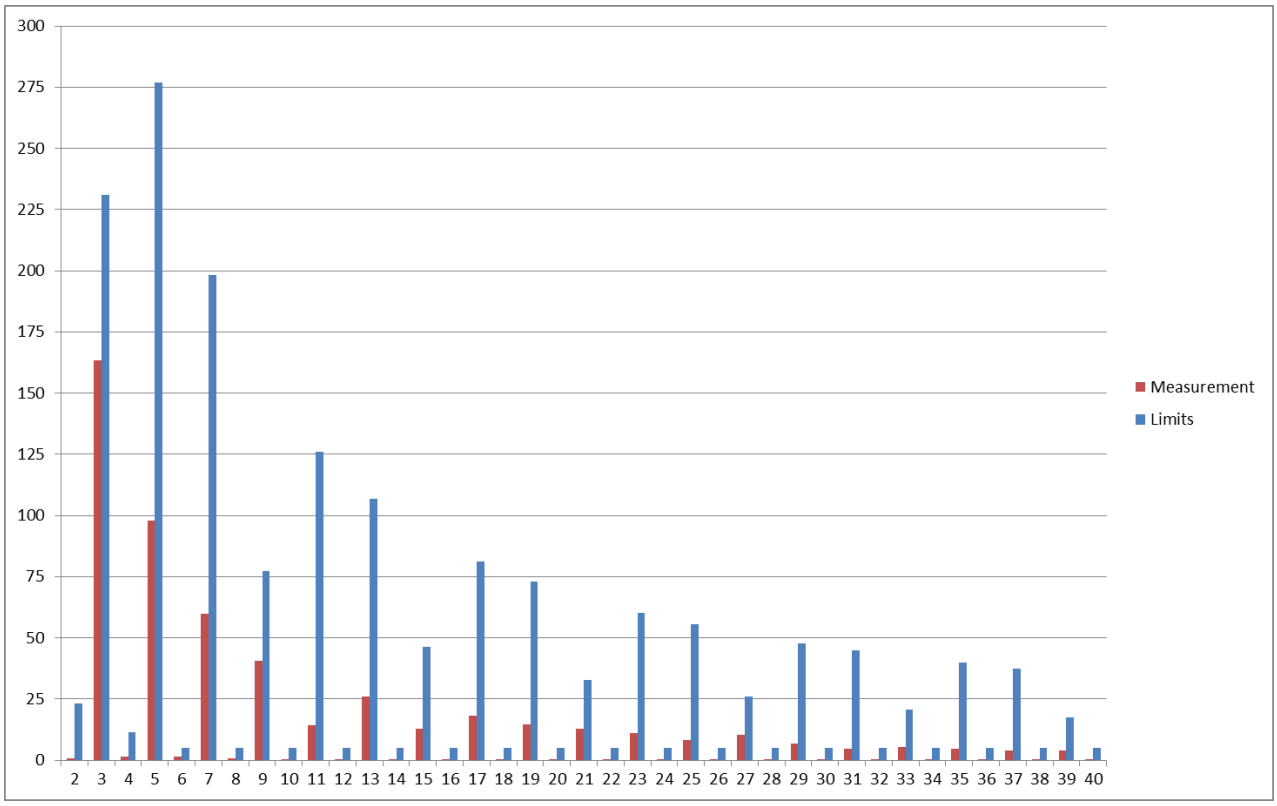
F = 520 Hz



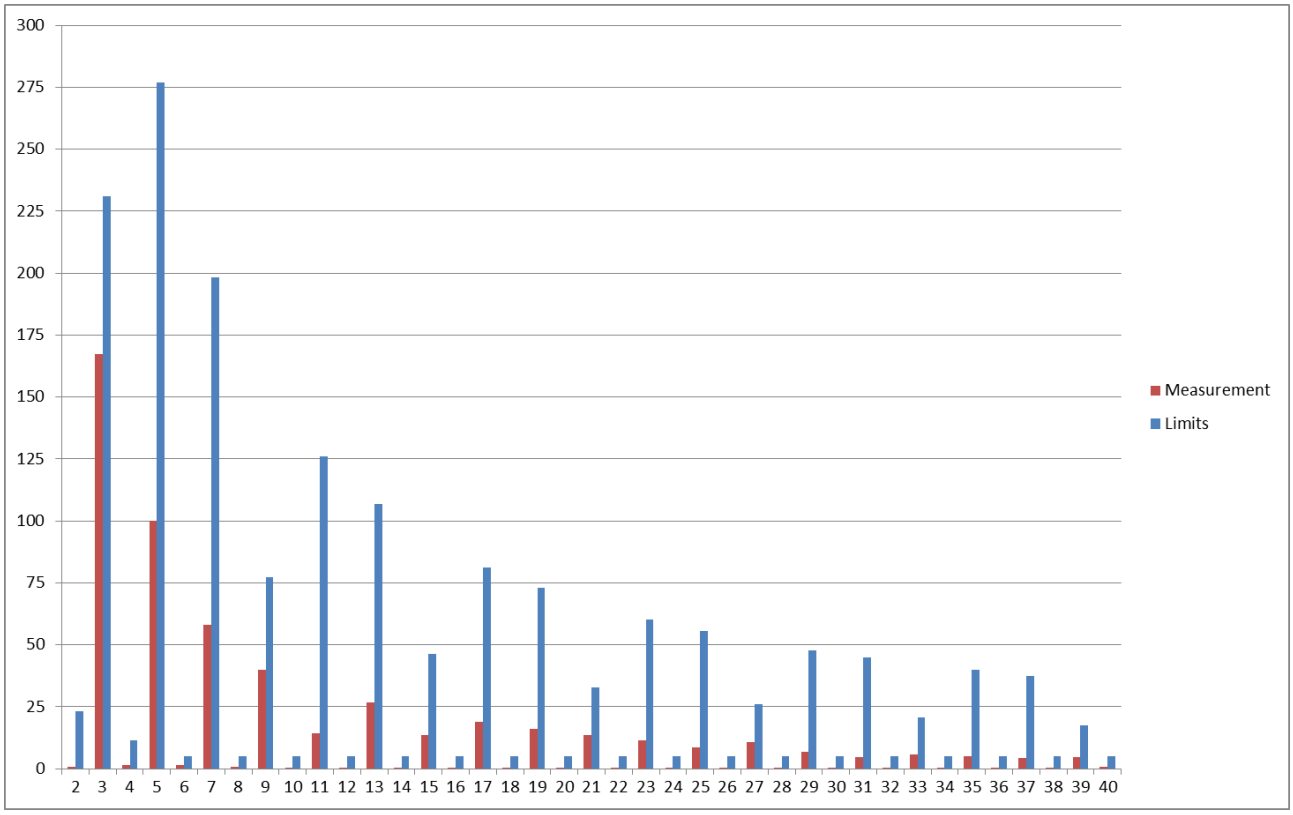
F = 560 Hz



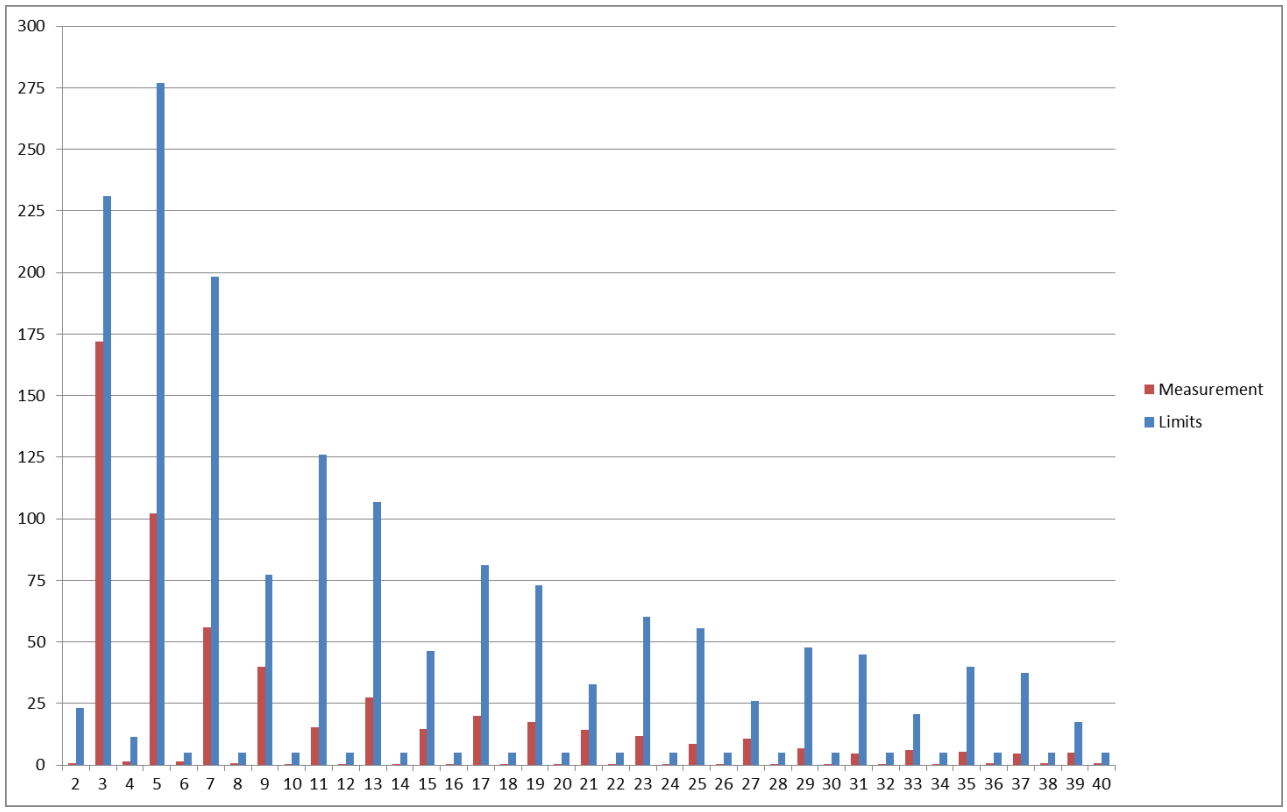
F = 600 Hz



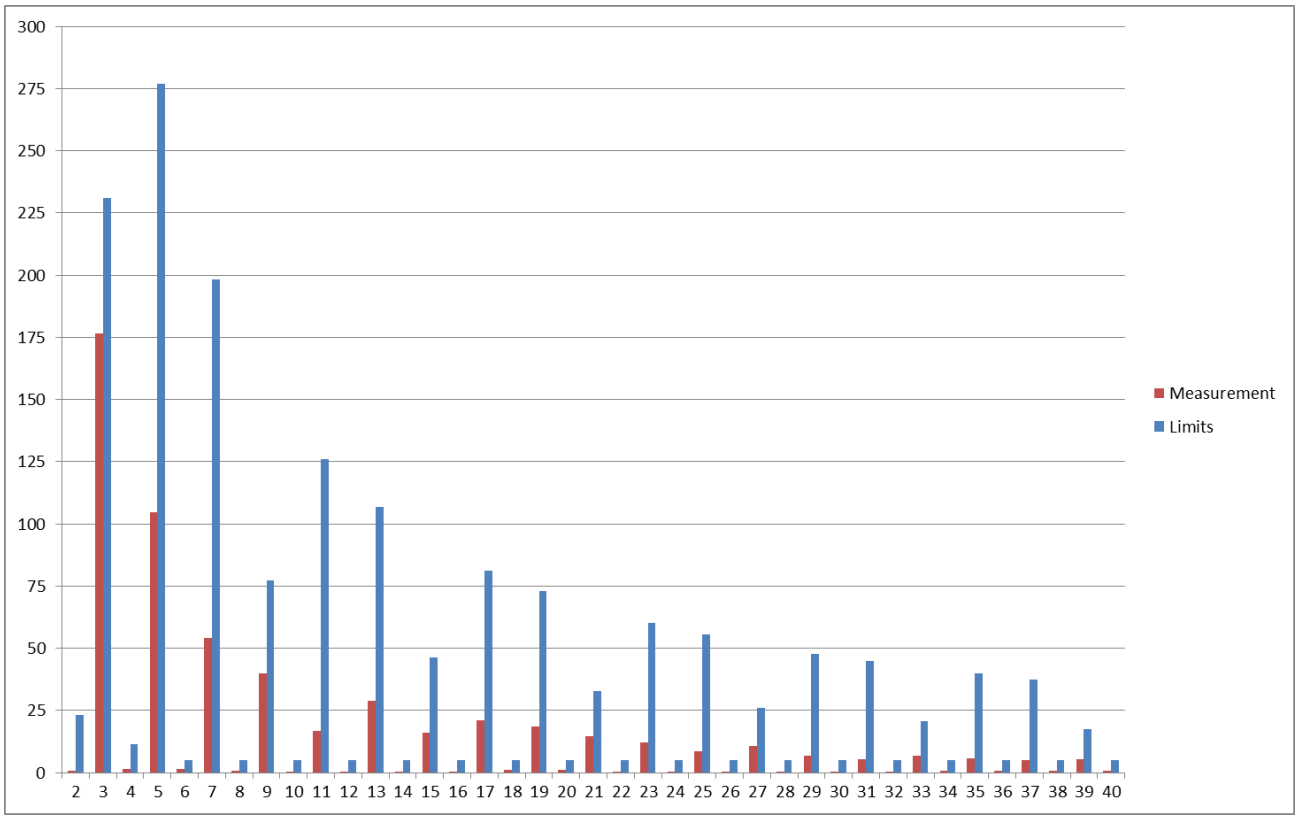
F = 640 Hz



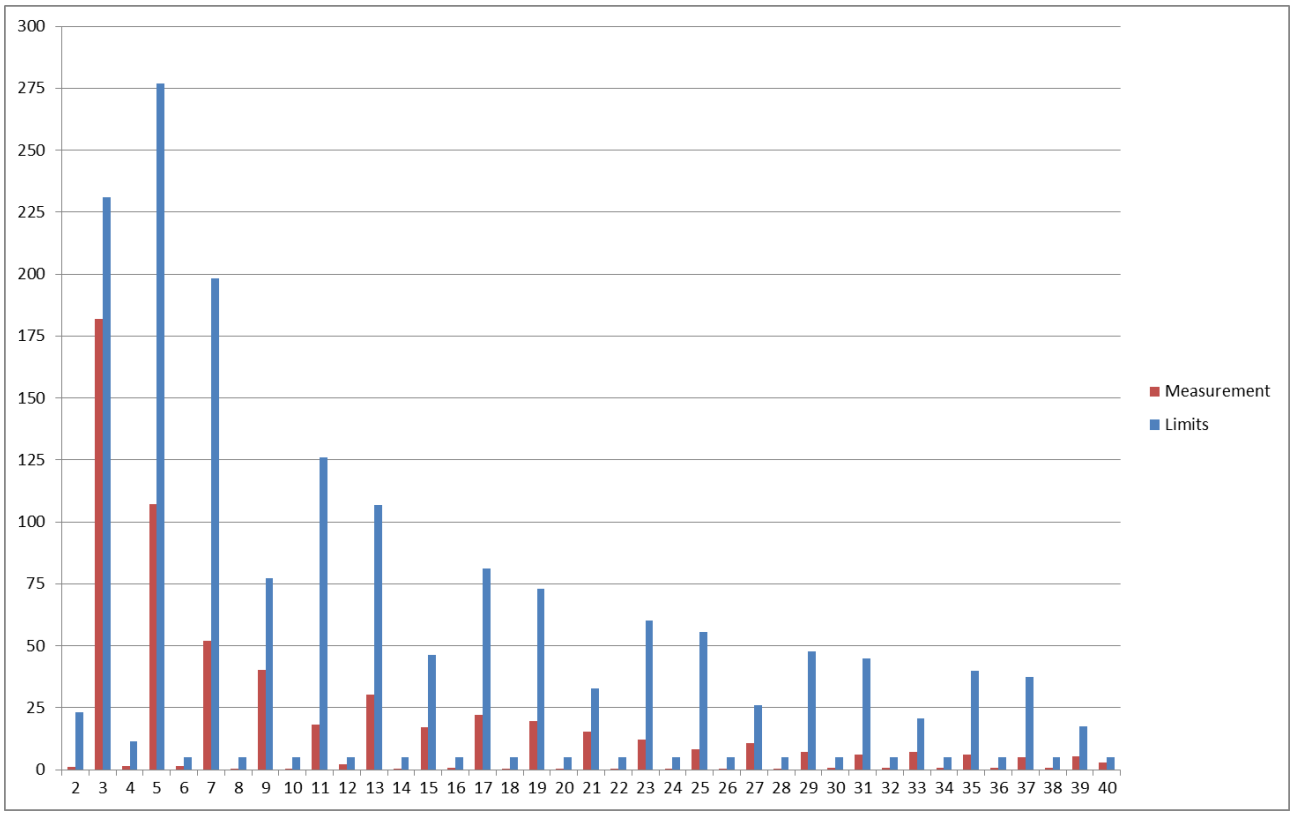
F = 680 Hz



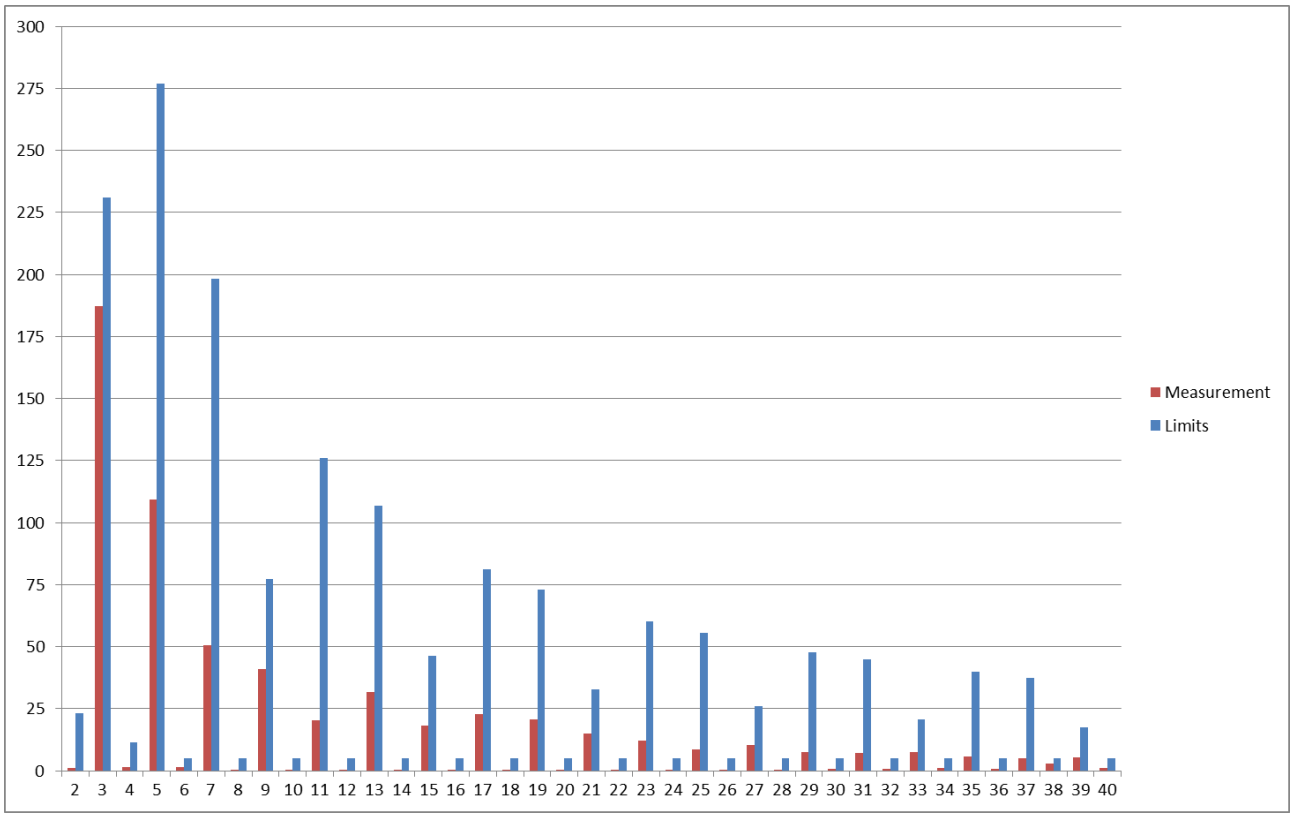
F = 720 Hz



F = 760 Hz

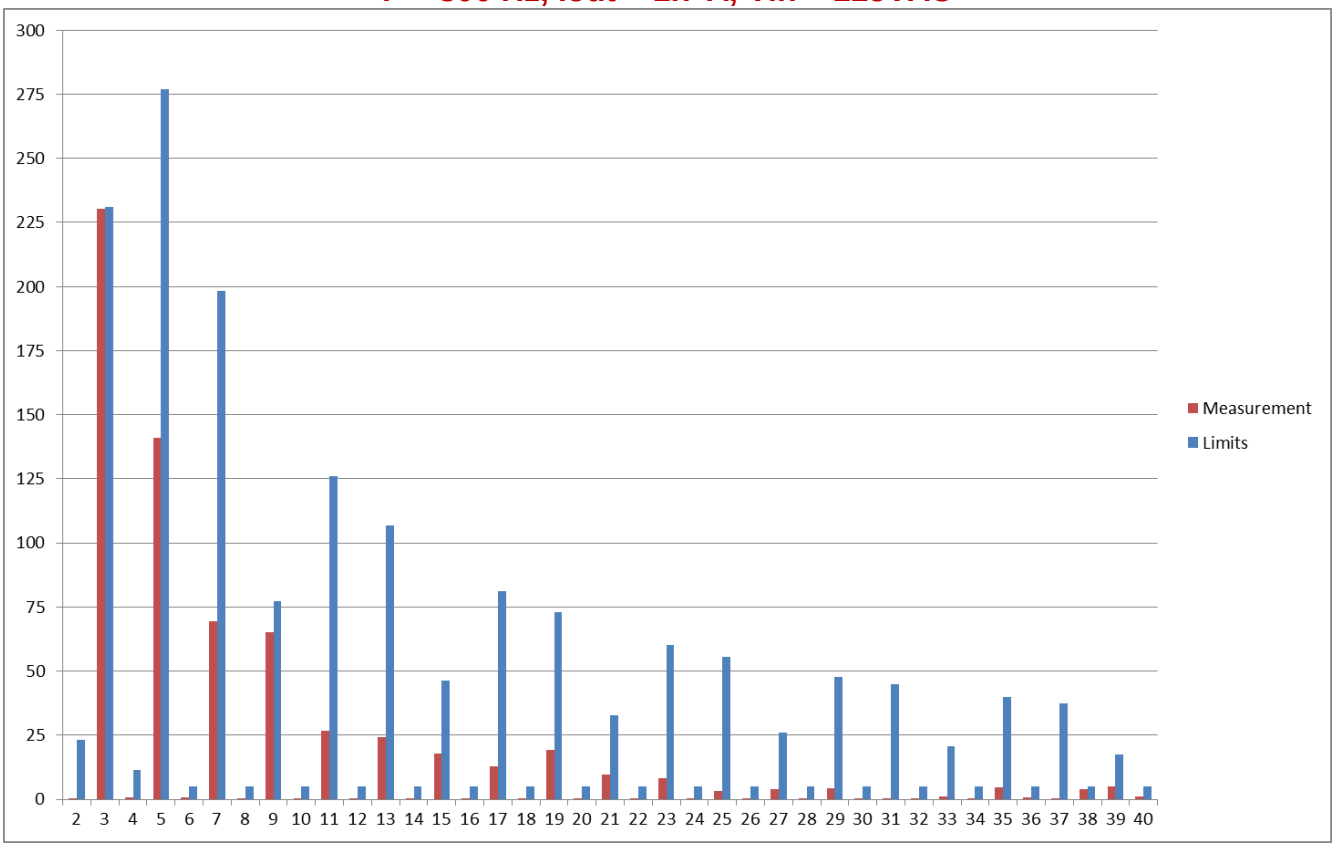


F = 800 Hz



It has been measured at what load level the converter reaches the limits of harmonic currents (which here is the third harmonic and in this case 230.9 mA). The output load was measured = 1.7A and below is shown the last measurement.

F = 800 Hz, Iout = 1.7 A, Vin = 115VAC



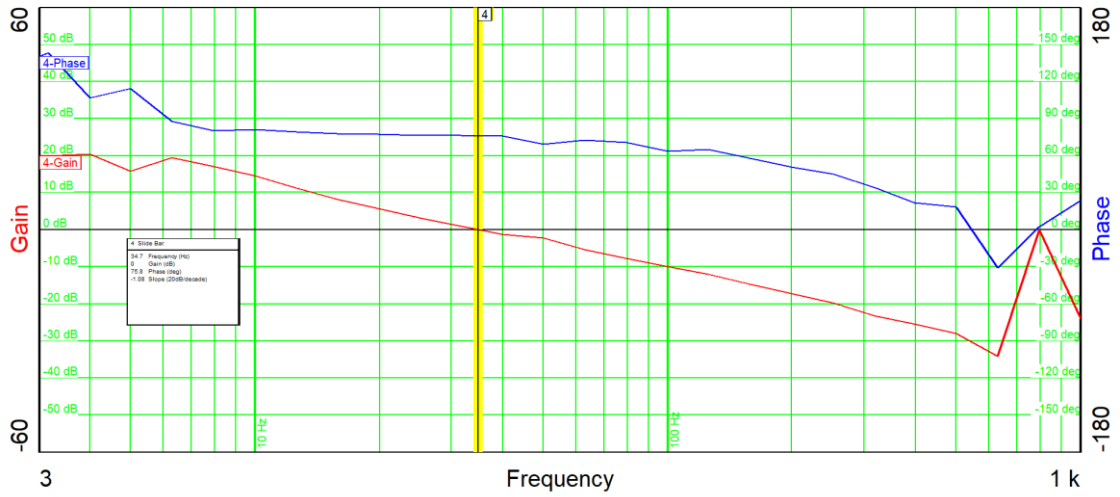
3.6 Feedback Loop for PFC and DC/DC Stages

The following graphs show the bode plots of the converter, when supplied at 115 VAC, 400 Hz and fully loaded (as well as 5 A load).
Here are the results, in terms of crossover frequency, phase margin and gain margin:

3.6.1 PFC Stage

In order to measure the stability of this stage, a 50 Ohm resistor has been inserted in series to R20.

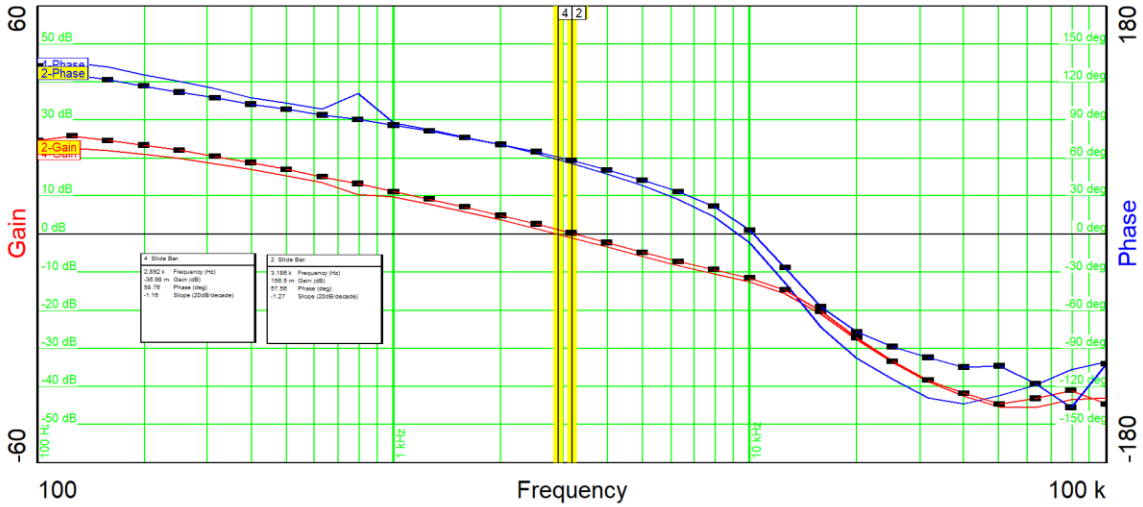
Parameter	Full load
Crossover frequency:	34.7Hz
Phase margin:	75.8 deg.
Gain margin:	30.27 dB



3.6.2 LLC Stage

In order to measure the stability of this stage, a 50 Ohm resistor has been inserted in series to the common connection of R17 & R48 to the net “30V”.

Parameter	Iout = 5A	Iout = 13 A
Crossover frequency:	3.186 KHz	2.892 KHz
Phase margin:	57.56 deg.	58.76 deg.
Gain margin:	11.67 dB	11.99 dB



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