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TI Designs: Verified Design

Reference Clock Generation for the 66AK2E0x & AM5K2E0x Design Guide

TEXAS INSTRUMENTS

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Design Resources

K2EVM	K2 EVM Information
66ak2e05	Product Folder
66ak2e02	Product Folder
am5k2e04	Product Folder
am5k2e02	Product Folder
CDCM6208	Product Folder

Circuit Description

Two CDCM6208 Ultra Low Power, Low Jitter Clock Generators can be used to create all the reference clocks needed for a full implementation of the 66AK2Ex and AM5K2E0x SOCs. The circuit can be easily modified to generate only the reference clocks needed in a customer design.

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1 Design Summary

The 66AK2E0x SOCs include inputs for three system reference clocks, six SerDes reference clocks and the TSREFCLK for the synchronous Ethernet subsystem. A full implementation, similar to the XEVMK2EX, would need a clock driver for each of these with multiple frequencies. Many of these clocks need to have phase noise characteristics that meet or exceed the jitter requirements for the SerDes reference clocks. This can be achieved using two Texas Instruments CDCM6208 low jitter clock generators.

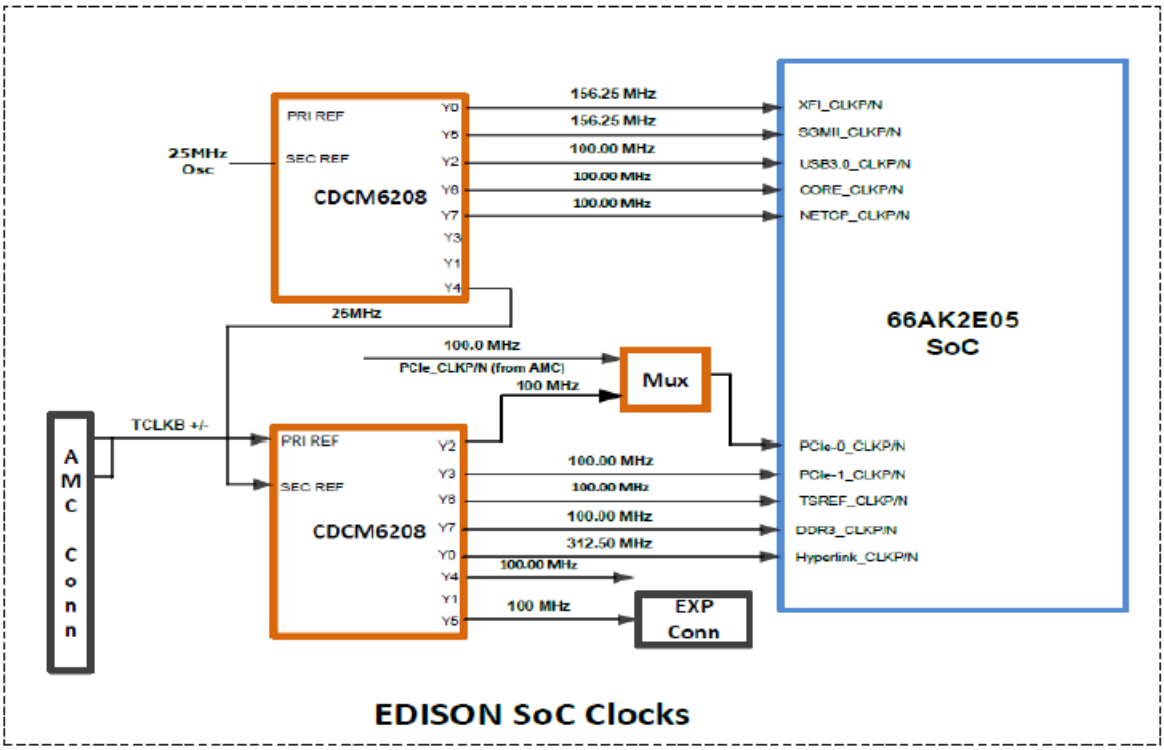

Figure 1: Full Clock Implementation for the XEVMK2EX

1.1 Introduction to the CDCM8208

The CDCM6208 has eight clock drivers that can be configured as LVDS, HCSL or LVCMOS. Four of the outputs are connected to a fractional divider allowing for a wide range of frequency possibilities. The remaining four outputs are connected to two integer dividers with each integer divider driving two clock drivers' outputs. These two drivers must be operated at the same frequency. One integer divider and two fractional dividers are grouped and clocked by one of two predividers. The predividers are directly clocked by the VCO. The CDCM6208 is available in two versions marked as V1 or V2. The V1 component has a VCO centered on 2.5GHz and the V2 version has a VCO centered on 3.0GHz. The best jitter performance is achieved when using an integer divider or a fractional divider in an integer mode.

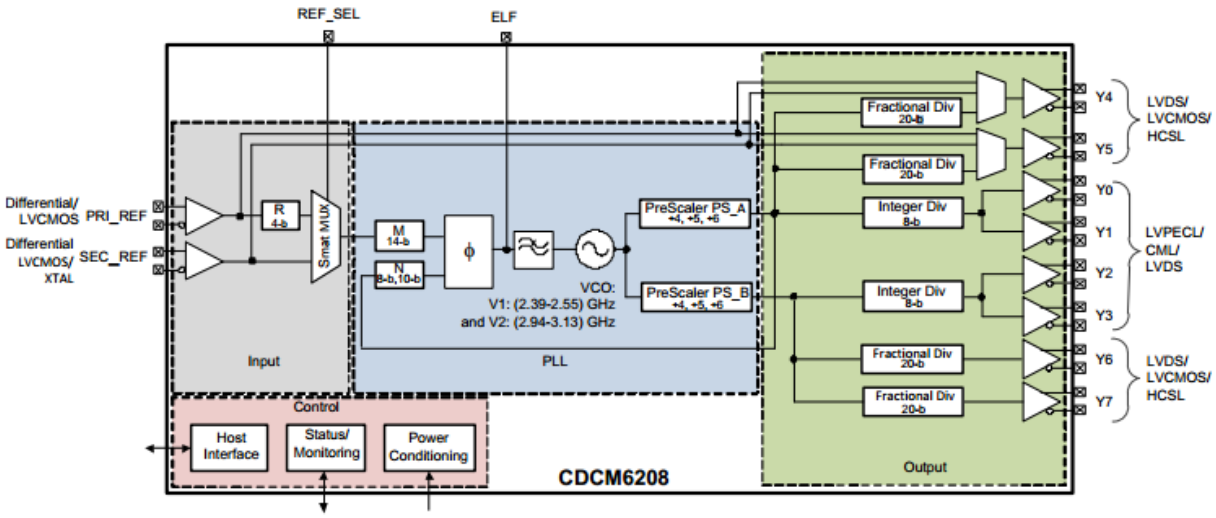

Figure 2: CDCM6208 Functional Block Diagram

1.2 Implementation

The XEVMK2EX was designed to as a flexible software development platform and all the clocks needed by the part are provided. The CDCM6208 uses a 25MHz oscillator as an input source for clock generator 1. Output 4 from clock generator provides the source clock for the second generator. All the clocks used by the 66AK2E0x SOC are generated with either integer dividers or with the integer portion of the fractional divider to decrease the jitter on the output clocks. The clocks generated are shown below.

Table 1. Full Clock Implementation for the XEVMK2EX

Clock	Name	Output Buffer	Frequency	Clock Generator
	System Clocks			
CORECLK	Core PLL	LVDS	100MHz	CDCM6208 #1
DDRCLK	DDR PLL	LVDS	100MHz	CDCM6208 #2
NETCPCLK	NETCP PLL	LVDS	100MHz	CDCM6208 #1
	Serdes Clocks			
SGMIICLK	SGMII Serdes PLL	LVDS	156.25MHz	CDCM6208 #1
XFICLK	XFI Serdes PLL	LVDS	156.25MHz	CDCM6208 #1
PCIE0CLK	PCIE0 Serdes PLL	LVDS	100MHz	CDCM6208 #2
PCIE1CLK	PCIE1 Serdes PLL	LVDS	100MHz	CDCM6208 #2
HYPLNK0CLK	HyperLink Serdes PLL	LVDS	312.5MHz	CDCM6208 #2
USBCLK	USB0 and USB1 Serdes PLL	LVDS	100MHz	CDCM6208 #1
	Other Clocks			
TSREFECLK	Synchronous Ethernet	LVDS	100MHz	CDCM6208 #2

2 Configuration of the CDCM6208

The register values needed to program the CDCM6208 are generated using the CDCM6208 EVM Control GUI. The GUI provides the ability to make changes to the clock frequencies generated and to program the control register values. The XEVMK2EX uses the BMC microcontroller to program the register values into the CDCM6208 after power is applied to the board. The CDCM6208 does not contain non-volatile registers and must be programmed whenever power is applied or when a reset is received.

2.1 Configuration files

The config (.INI) files are provided for both clock generators as an example. These files may be opened in the CDCM6208 EVM Control GUI found on TI.com. A link to that software is show below.

http://www.ti.com/lit/zip/scac134

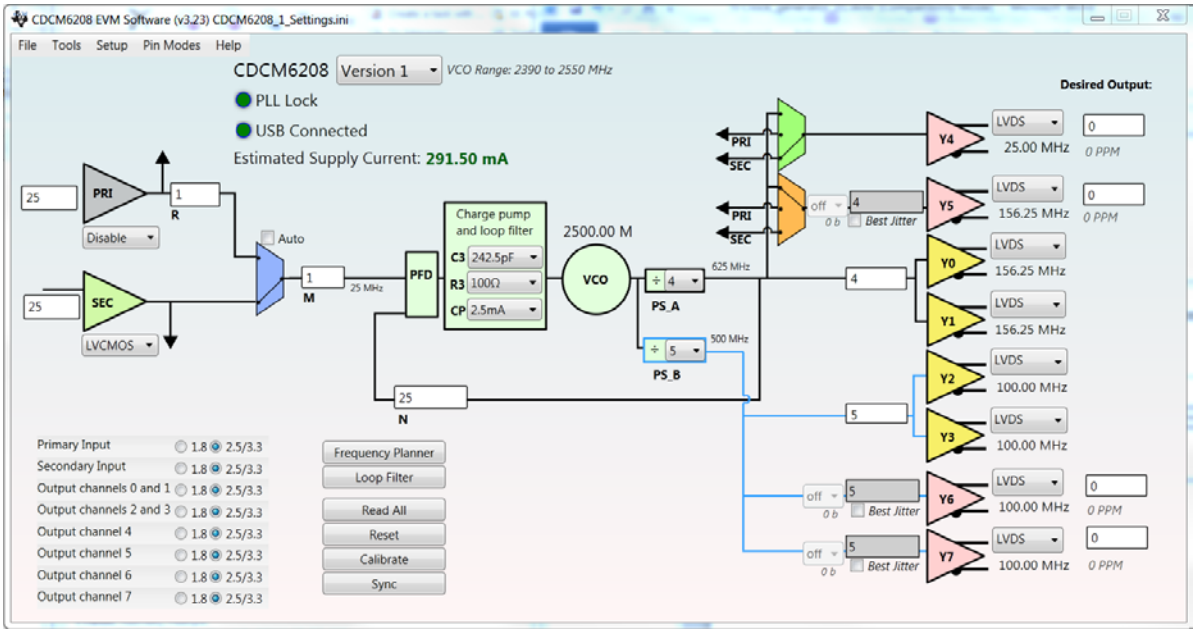

Figure 3: CDCM6208 #1 Configuration GUI

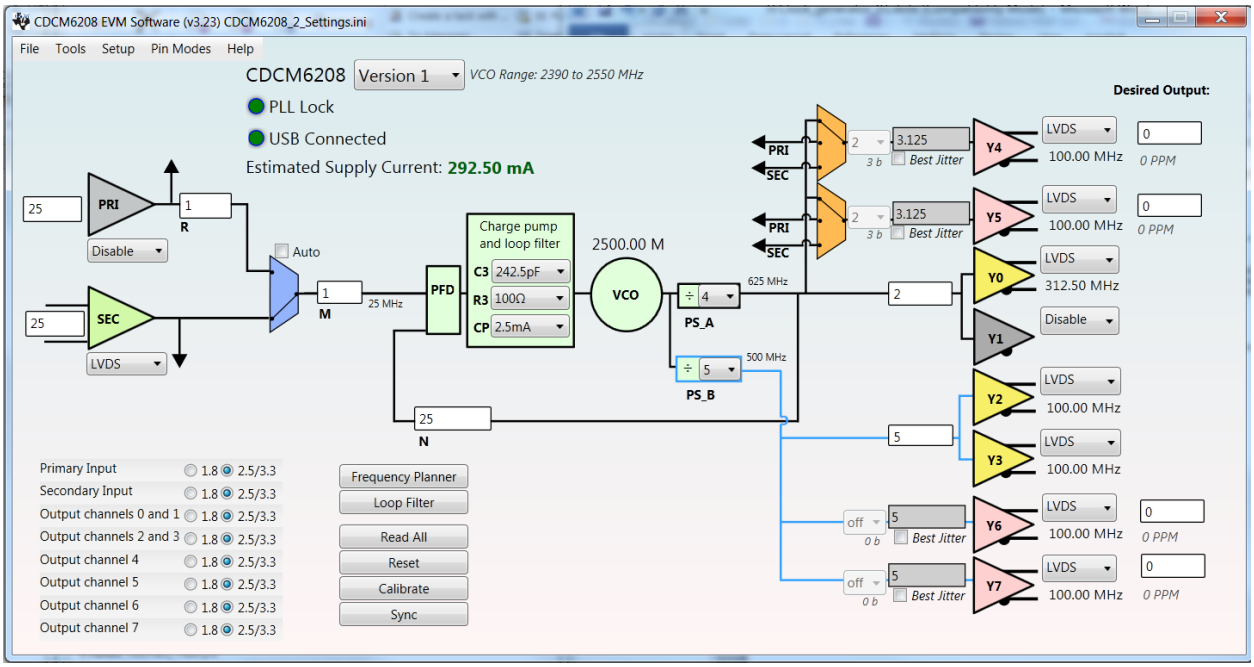

Figure 4: CDCM6208 #2 Configuration GUI

3 PCB Design

The PCB, schematic and bill of materials can be found at the TI Designs link for this design. Refer to the documentation for the CDCM6208 for details on the placement and layout of the PCB for this part. This design was implemented as part of the XEVMK2EX. The PCB file provided includes all the part associated with the 66AK2E0x EVM and not just the components shown in the schematic for this design.

4 Modifications

Most customers will not need to provide all the clocks used on the XEVMK2EX. There are a number of options that will allow the number of necessary clocks to be reduced. This section will highlight some of the design considerations when using the CDCM6208.

4.1 Clock Reduction

There are a number of design decisions that may simplify the clock generation for a customer design. Here are a few items to consider.

4.1.1 CORECLK and DDRCLK

CORECLK and DDRCLK will need separate output drivers connected to the SOC but often these two clocks can used the same frequency. In this example both are configured as 100MHz. The CDCM6208 has two pairs of outputs that are driven by the same divider. If CORECLK and DDRCLK are using the same frequency, consider using outputs Y0 & Y1 or Y2 & Y3.

4.1.2 NETCPCLK

The NETCP PLL can use either the NETCPCLK input or the CORECLK input as a reference based on the NETCPCLKSEL configuration input. If the NETCP PLL can use the same frequency present on CORECLK than the NETCPCLK pins can be tied to an unused state. This will reduce the number of system reference clocks needed.

4.1.3 Unused Serdes

The SOC has six different serdes reference clocks. These clocks must be provided if the serdes is used in your design but are not needed if the serdes interface is not connected. For example, if the customer design uses only the SGMII, PCIE0 and USB0 then only SGMIICLK, PCIE0CLK and USBCLK are needed. Remember that it's best to generate serdes reference clock using an integer divide. Using the integer portion of the fractional divider will also provide a more stable clock.

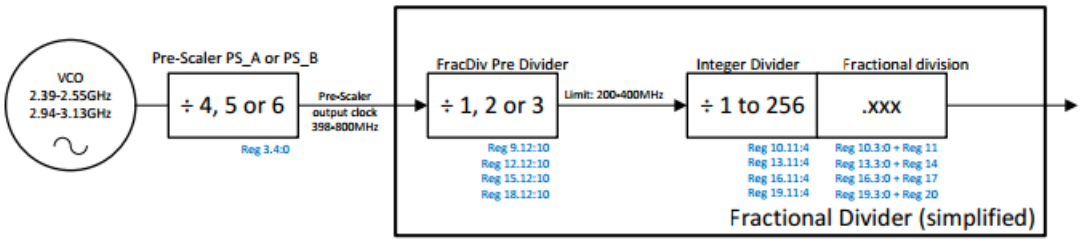

Figure 5: CDCM6208 Fractional Divider

4.1.4 PCIExCLK

If the PCIE interface is acting as an endpoint and is connected to a PCIE bus, a 100MHz reference clock should be present on the bus connector. You can use that PCIE reference clock in place of an output from the CDCM6208. The PCIE Electromechanical Specification requires that a PCIE root complex provide a 100MHz reference clock on the backplane. Often this clock is a spread-spectrum type to reduce EMI. If spread-spectrum is present, it is required that the backplane clock be used for the PCIExCLK input to the SOC.

4.2 Configuration

The CDCM6208 must be configured to provide the required frequencies. This example design uses a microcontroller to program the configuration registers using the SPI interface. When the power is cycled or a reset is applied to the device, the microcontroller must reprogram the control registers for proper operation. The CDCM6208 also supports a pin mode. In this mode the values of the configuration registers are determined based on the value of five configuration pins. This value will determine the configuration of the device based on a lookup table within the CDCM6208. If your clock configuration matches one of the preset look-up values, the need for the microcontroller can be eliminated.

5 Acknowledgements & References (if applicable)

TI Documents Examples:

1. *T CDCM6208 2:8 Ultra Low Power, Low Jitter Clock Generator (SCAS931F)*
2. *66AK2E05, 66AK2E02 Multicore DSP+ARM KeyStone II System-on-Chip (SoC) (SPRS865C)*
3. *AM5K2E04, AM5K2E02 Multicore ARM KeyStone II System-on-Chip (SoC) (SPRS864C)*

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