TI Designs

4-mA to 20-mA Loop Energy Harvester Reference Design

Description

This reference design demonstrates energy harvesting from 4-mA to 20-mA loop-powered systems. The design is simple to insert into existing installations where it scavenges energy from the loop and generates a regulated output voltage. Furthermore, the circuit provides an analog output representing the actual loop current value. The insertion loss can be as low as 400 mV and can also be increased up to 2.85 V to address higher output power levels. All these features provide an easy way to power wireless adapters (WirelessHART® , *Bluetooth*® low energy (BLE), and so forth), indicators, displays, human machine interfaces (HMIs), and others for a seamless upgrade of existing 4-mA to 20-mA loop-powered systems.

Resources

TIDA-00649	Design Folder
BQ25570	Product Folder
TS5A3160	Product Folder
TLV341	Product Folder
CSD17313Q2	Product Folder

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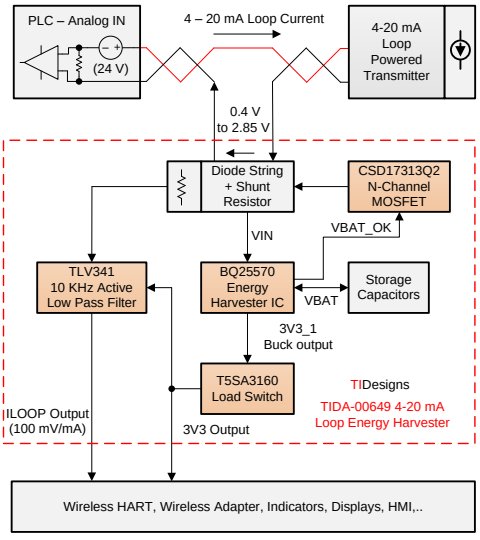
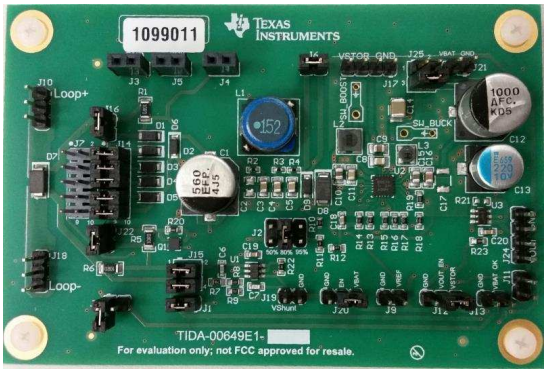
Features

- Minimal Insertion Loss
  - 0.4 V to 2.85 V, Selectable
  - Adaptable to Voltage Margin in Loop and Required Output Power
- Adjustable Output Voltage Between 1.8 V to 3.8 V
- 15-mA Peak-Pulsed Output Current
- Loop Current Sensing
  - Analog Output 100 mV/mA
  - Active 10-kHz Low-Pass Filter
- Reverse Polarity Protection
- Designed to Withstand Surges According to IEC 61000-4-5; ±1 kV; 40 Ω
- Flexible Configurations for Test and Evaluation

Applications

- Loop-Powered Adapters (WirelessHART® , BLE, and So Forth)
- Loop-Powered Indicators, Displays, and HMIs





1 System Overview

1.1 System Description

The intended use of this design is to harvest power from the 4-mA to 20-mA loop current for the purpose of powering additional add-on functions and applications from the scavenged power. Such add-on applications include (but are not limited to) loop-powered WirelessHART adapters or other low-power wireless transceivers, indicators, displays, and HMIs. With such applications, additional functions like wireless communication or displaying the values sensed by a 4-mA to 20-mA transmitter can be added to existing loop-powered systems.

The current flowing in the loop of such a system is controlled by the 4-mA to 20-mA transmitter, which typically ranges from 4 mA to 20 mA. The lowest possible value of the transmitter measurement range is represented by a loop current of 4 mA, whereas 100% of the full-scale value is represented by 20 mA. Therefore, the previously mentioned add-on functions and applications should continue to operate, even when powered by this low 4-mA to 20-mA current. The energy which can be harvested depends strongly on the loop current and on the value of the physical size sensed by the transmitter.

The minimum loop current case can be considered as the worst case condition, which can be even smaller than the 4 mA. Loop-powered transmitters often have an ERROR_LOW current level specified (usually in the range of 3.3 mA to 3.5 mA), which represents the worst-case condition for an energy harvester. Transmitters with HART can drive the minimum loop current value further down based on the fact that they modulate the loop current at a 1-mA_{P-P} sine wave signal for the purpose of digital communication over the loop.

The design of an energy harvester for such systems poses an additional challenge: The available input voltage for such a harvester is limited, as well. The reason for the limited input voltage budget is based on the fact that most loop-powered transmitters require at least 8 V to 10 V as a minimum supply voltage (often specified as compliance voltage). Voltage drops across the system current sense resistors and across the 100s of meters-long connection cable reduce the available voltage at the transmitters loop terminals significantly. Voltage losses caused by the subsequent insertion of an energy harvester into existing loop-powered installations must therefore be minimized to some 100s of mV up to a value in the lower, single-digit volt range.

To ensure proper operation of an energy harvester for such systems, special care is required when defining the principle of its operation, its features, and specifications as well the process of selecting the proper components for the circuit design. The power consumption of the devices used in the design is one of the primary concerns for the selection process.

The design offers features such as ease of connection to a two-wire loop system, selectable insertion loss (input voltage of the harvesters boost converter), selectable storage capacitance, and adjustable output voltage. The design has two terminals to be used for insertion into an existing loop: a loop positive terminal (LOOP+) and a loop negative terminal (LOOP–). A string of diodes (D1 to D5) is placed in between the two input terminals. The loop current flows through the diodes, biases them in a forward direction, and generates a voltage which passes through a pi filter to provide power for the the boost charger of the energy harvester U2. The insertion loss is selectable by shorting one to four diodes of the five diodes (D1 to D5) by means of jumpers used together with the onboard headers J7 and J14. The additional MOSFET Q1 can change this insertion loss selection depending on the VBAT_OK signal, which especially supports the start of the design when configured to operate with the lowest possible insertion loss (with Schottky diode D1).

This reference design showcases the BQ25570 as a nano power boost charger and buck converter. The BQ25570 is the best in its class of energy harvesters, featuring ultra-low quiescent current and the ability to start up (cold start) from an input voltage as low as 330 mV. As soon as a cold start has been initiated and the set threshold voltage has been reached, the converter switches to a high-efficiency mode and is able to perform energy harvesting from ultra-low input voltages down to 100 mV. Therefore, the main advantage of this reference design over existing solutions is its ability to operate with an ultra-low insertion loss, even at the typical ERROR-LOW loop current level. This quality enables the reference design to operate with an insertion loss down to the voltage drop of one Schottky diode.

The boosted voltage charges storage capacitors (C12, C13, and C14) up to a value of 4.2 V. The voltage of the storage capacitors is then stepped down by the harvesters (U2) integrated buck converter to a regulated output voltage of 3.3 V. The value of this output voltage, labeled as 3V3_1 , can be adjusted by the VOUT_SET resistors R18 and R19. An additional low resistance load switch (U3) is used to ensure that the buck converter is not loaded before the storage capacitors have reached the set VBAT_OK threshold level. The implementation of this switch helps the harvesters boost charger to successfully switch from cold start mode to high-efficiency boost mode without oscillating or collapsing. This output voltage of the load switch U3 can be used to power the add-on functions and applications as previously explained in this subsection.

The targeted applications of this reference design are add-on functions and applications. All those applications and functions have something in common—that they somehow must process the value of the current flowing in the 4-mA to 20-mA current loop. Therefore, the reference design contains additional circuitry for measuring the loop current (along with the HART communication signals) and filtering it by means of an active 10-kHz low-pass filter. The design showcases an ultra-low quiescent-current operational amplifier (op amp) for this purpose.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS AND FEATURES
Influence on loop voltage	
Minimum insertion loss at 3.3 mA; 20ºC	≈400 mV
Maximum insertion loss at 3.3 mA; 20ºC	≈2850 mV
DC-DC converter	
Device type	Boost converter with integrated buck
Minimum input voltage (typical for operation)	330 mV (cold start); 100 mV (during normal operation)
Maximum input voltage (typical for operation)	5100 mV
Output voltage (BOOST = VSTOR)	4200 mV (typ)
Output voltage (BUCK = VOUT)	1800 mV – 3800 mV (adjustable)
Efficiency (VIN = 500 mV; T = 20°C; VOUT = 3.3 V)	≈78%
Storage capacitance	100 µF (fixed), 1000 µF, or 220 µF (selectable)
VBAT_OK	3300 mV (typ)
VBAT_OK_HYST	3100 mV
MPPT (maximum power point tracking) percentage	50%, 80%, or 95% (selectable)
Quiescent current	488 nA (typ)
Protection	
Reverse input protection at 21 mA; 20°C	–220 mV (typ)
Surge protection (IEC 61000-4-5; ±1 kV; 42 Ω)	Unidirectional TVS diode in loop
Operating temperature	
Temperature range	–40°C to 125°C

1.3 Block Diagram

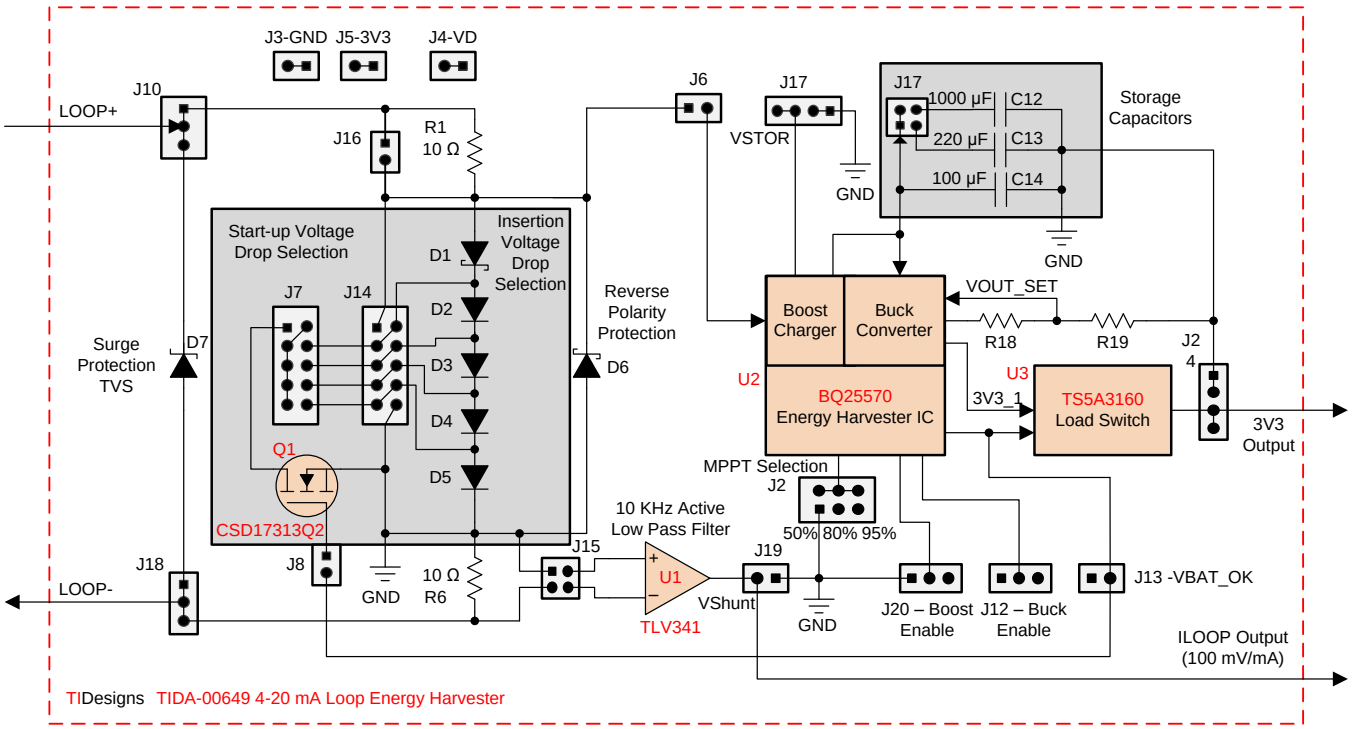


Figure 1. Functional Block Diagram

1.4 Highlighted Products

1.4.1 BQ25570 – Nano Power Boost Charger and Buck Converter

The BQ25570 device is an efficient energy-harvesting solution for meeting the special requirements of ultra-low power applications (see Figure 2). The device has been specially designed to efficiently acquire and manage the microwatt-to-milliwatt range of power from a variety of DC energy-harvesting sources. One of the main assets of the device is the programmable maximum-power-point-tracking (MPPT) sampling network to optimize the transfer of power into the input of the device.

The MPPT sampling network can regulate the input voltage to maximize the efficiency of the DC-DC convertor in a system where the availability of power is often time varying. The MPPT checks the input power every 16 seconds for a period of 256 ms and obtains a new reference voltage every cycle. A fraction of the open circuit voltage is sampled and held in the low leakage capacitance connected to the VOC_SAMP pin. Pulling the VOC_SAMP pin to HIGH by connecting it to VSTOR regulates the input voltage to 80%. This prevents the source from collapsing as a result of loading to its maximum. Solar panels (diodes) have a maximum efficiency when operated at 80% of its open circuit voltage. Pulling the VOC_SAMP to LOW by connecting the pin to ground regulates the input voltage to 50% of the open-circuit voltage. Achieving other MPPT values is possible by using external resistors. Achieving a total resistance of 20 MΩ to minimize the losses is mandatory.

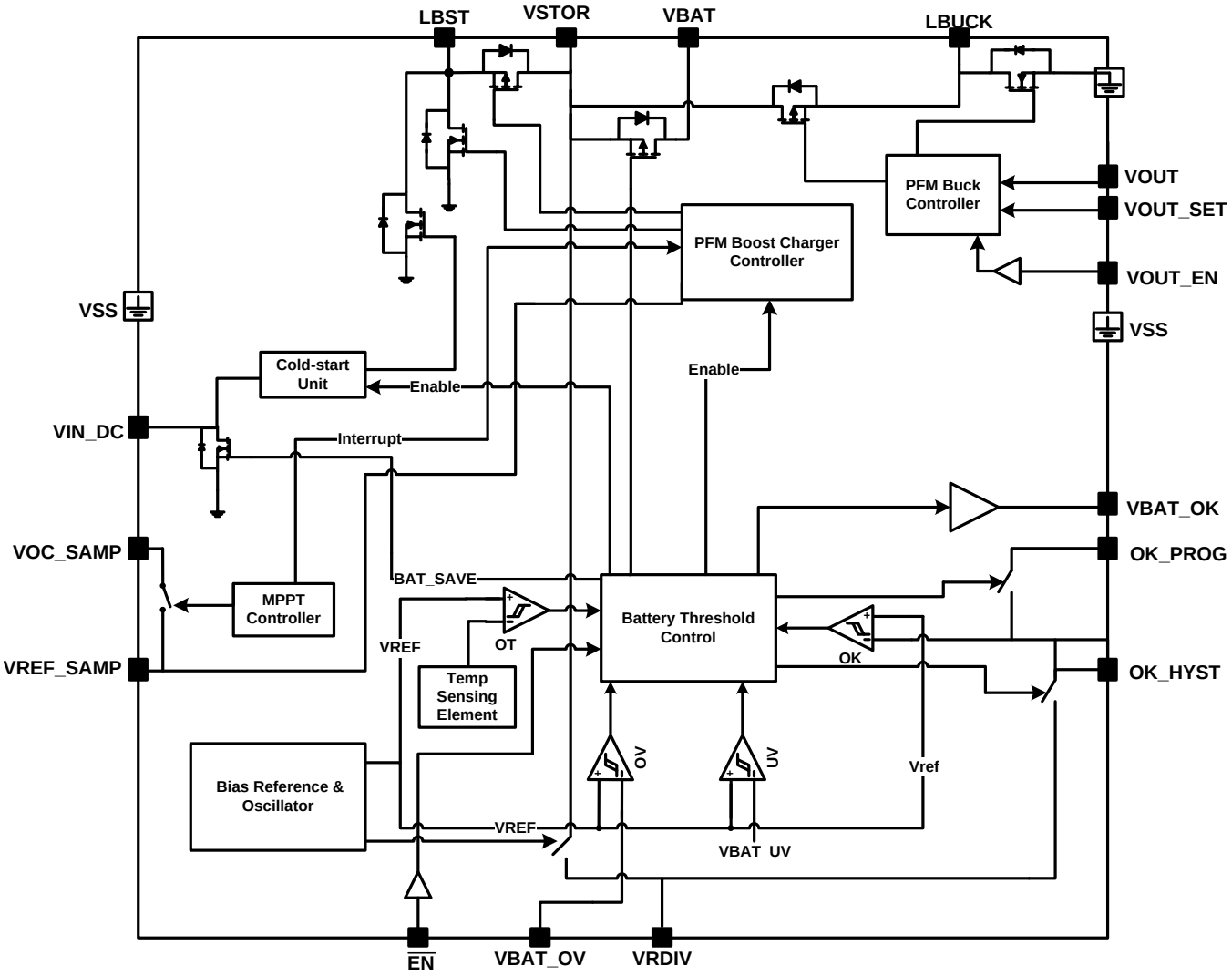


Figure 2. BQ25570 Functional Block Diagram

Another major asset of the BQ25570 is its integrated high-efficiency buck converter. The BQ25570 provides an externally programmable regulated supply through the buck converter. The regulated output has been optimized to provide high efficiency output across low current levels of less than 10 µA up to high current levels of 110 mA. The buck converter is internally connected to the VSTOR pin and steps down the voltage. The buck converter also employs pulse frequency modulation (PFM) control to regulate the voltage close to the desired reference voltage.

1.4.2 TS5A3160 – 1-Ω Single-Pole Double-Throw (SPDT) Analog Switch

The TS5A3160 device is a single-pole double-throw (SPDT) analog switch (see Figure 3). The device offers very low ON state resistance and an excellent channel-to-channel ON state resistance matching. The device consumes very low power to operate (≈500 nA max).

DBV or DCK Packages
6-Pin SOT-23 or SC-70
Top View

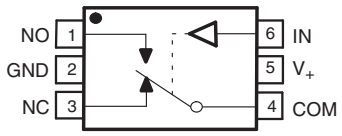


Figure 3. TS5A3160 – Pin Configuration

The COM pin is connected to the NC pin as a default condition. When the IN pin is HIGH, the COM pin is connected to the NO pin. The standard ON time is approximately 4 ns and the OFF time is 9 ns. The device has to be supplied with a voltage of 1.65 V to 5.5 V.

1.4.3 TLV341 – Low Voltage Rail-to-Rail Output CMOS Op Amp

The TLV314 device is a low-power, general purpose op amp (see Figure 4). It is a rail-to-rail output swing device with low quiescent currents (150 µA typ) and a wide bandwidth of 3 MHz. These features make the device suitable for low power applications. These single-supply amplifiers have been designed specifically for ultra-low-voltage (1.5 V to 5 V) operation, with a common-mode input voltage range that typically extends from –0.2 V to 0.5 V from the positive supply rail.

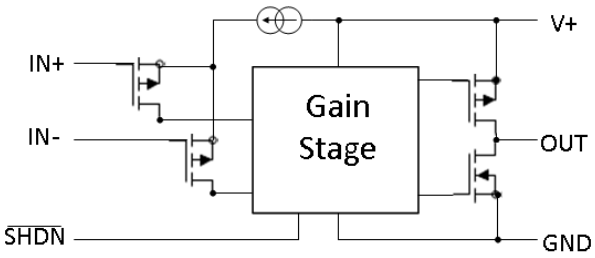


Figure 4. TLV341 – Functional Block Diagram

The TLV341 also offers a shutdown (SHDN) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 45 pA (typical). Offered in both the SOT-23 and smaller SC70 packages, the TLV341 is suitable for the most space-constrained applications.

1.4.4 CSD17313Q2 30-V N-Channel NexFET™ Power MOSFET

The CSD17313Q2 N-channel 30-V NexFET power MOSFET has been designed to minimize losses in power conversion applications (see Figure 5). The 2-mm × 2-mm SON is suitable for space-constrained applications and offers excellent thermal performance for the size of the package. The drain-to-source ON resistance is typically 31 mΩ at a V_{GS} = 3 V and the gate-to-source threshold voltage is 1.3 V at V_{DS} = V_{GS}, I_D = 250 µA.

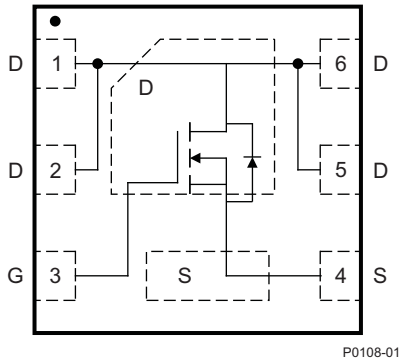


Figure 5. CSD17313Q2 – Top View

2 Getting Started Hardware

The TIDA-00649 reference design provides various test features and enables the user to figure out the circuit performances, such as the required input voltage for seamless operation in maximum, continuous, output-current mode as well as in pulsed-output current mode. To enable the measurements of these parameters and to provide an ease of access to activate or deactivate the measurement sections, multiple headers are placed (see Figure 6). The intended use of the design is for evaluation purposes only and the final size of the board depends on the end user application. This user's guide focuses on all the header settings for measurements. In low-power designs, the user must be certain of various parameters to use the device to its maximum performance.

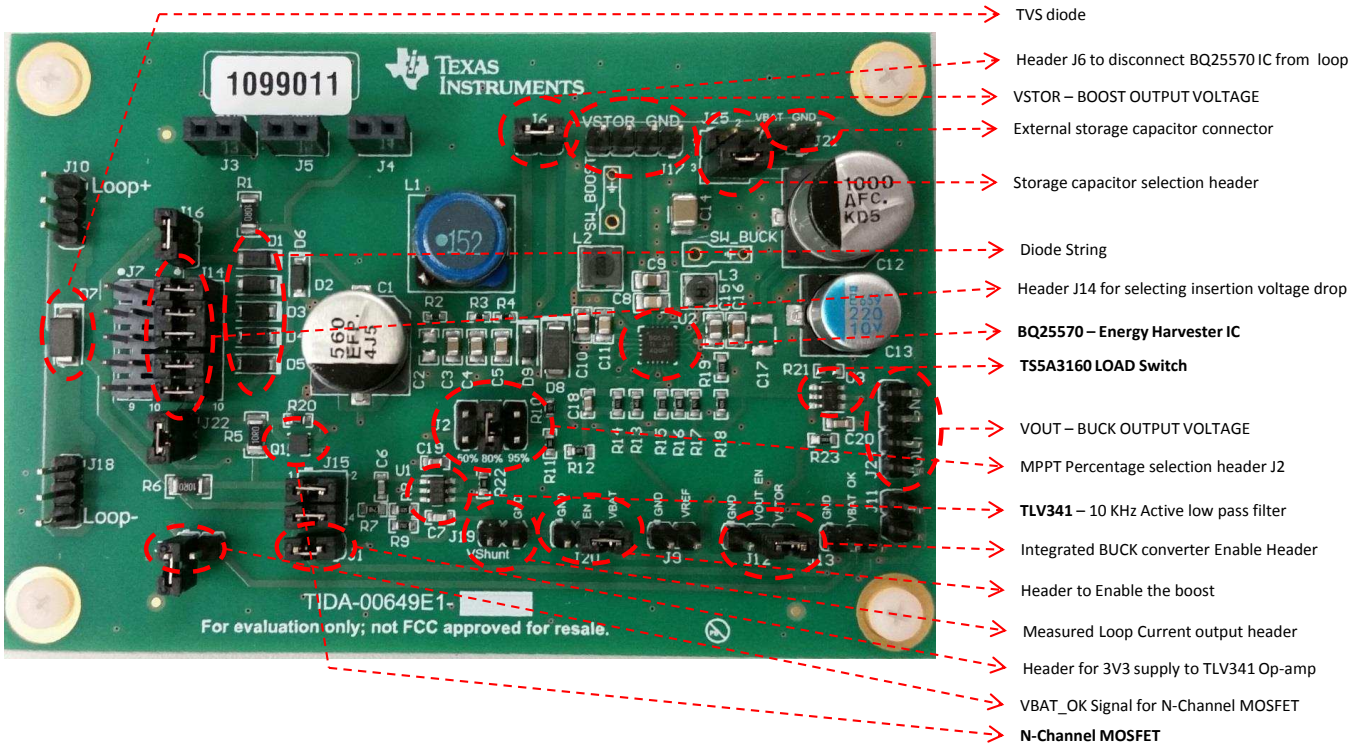


Figure 6. Board Description

2.1 Loop Insertion and Surge Protection

The primary goal of the design is to enable a user to simply insert the board into an existing 4-mA to 20-mA loop-powered system, which consists of two terminals LOOP+ and LOOP–. Figure 7 shows an example of connecting the TIDA-00649 to an existing system by inserting it into the existing negative loop wire. The LOOP+ (J10) of the reference design is connected to the ground of the sensor transmitter and the LOOP– (J18) is connected to the negative terminal of the power supply.

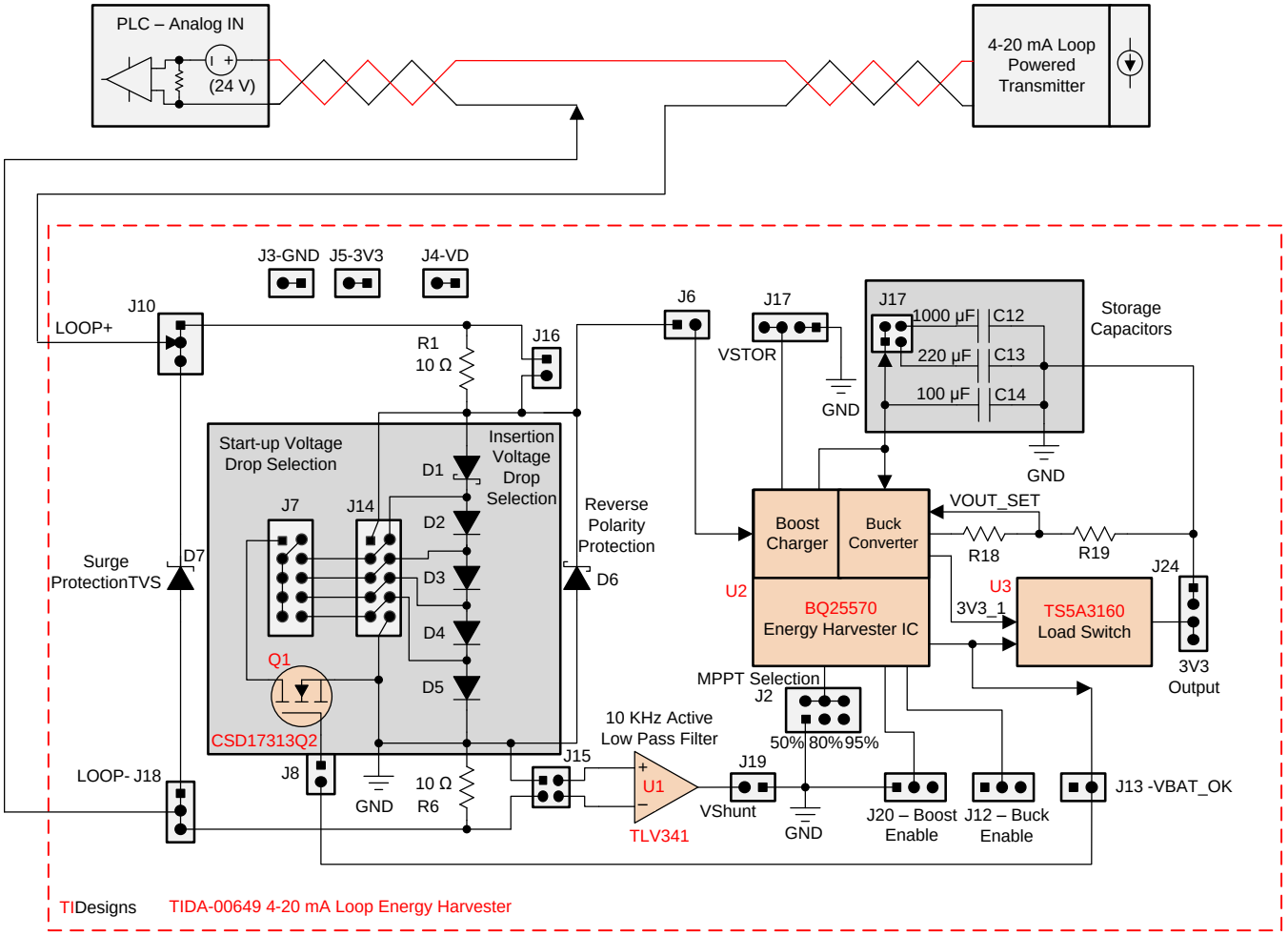


Figure 7. Example Connection Block Diagram

The loop input has been designed to withstand 8/20-µs surges according to IEC 61000-4-5. A transient-voltage-suppression (TVS) diode is added in parallel to the string of diodes for this enduring purpose. During peak surge, the TVS diode breaks down and the majority of the current peak flows through the TVS diode. Equation 1 calculates the clamping voltage of the TVS diode:

$$V_{CLMAX} = V_{CL} - R_D \left(I_{PP} - I_{EXPT}\right) \quad (1)$$

where,

- V_{CLMAX} is the maximum clamping voltage for expected current
- V_{CL} is the clamping voltage rated as per data sheet specification
- R_D is the dynamic resistance
- I_{P-P} is the peak-pulse current as per data sheet specification
- I_{EXPT} is the expected current to flow through the TVS diode.

Sample calculation:

$$V_{CLMAX} = 13.4\ V - 0.036\ \Omega\ (176\ A - 25\ A)$$
$$V_{CLMAX} = 13.4\ V - 5.436\ V$$
$$V_{CLMAX} = 7.964\ V \quad (2)$$

From calculations, it is clear that when 25 A of current flow through the TVS diode, the clamped voltage is approximately 8 V. The design has three sense resistors: a high side shunt resistor, a low side shunt resistor, and a resistor to measure the current through the string of diodes. The total resistance offered by the measuring resistance influences the current flowing through the diode string. The number of diodes in the loop creates a voltage drop in the clamping voltage. To find the current through the diodes or toward the DC-DC converter, divide the remaining clamped voltage by the total shunt resistance. The calculations for Equation 3 are as follows:

$$I_{SD} = \left(\frac{V_{CLMAX} - V_{DIODE}}{R_{SHUNT}} \right) \quad (3)$$

where,

- I_{SD} is the current through the diode string
- V_{DIODE} is the voltage drop across the diode
- R_{SHUNT} is the total shunt resistance.

Sample calculation:

$$I_{SD} = \left(\frac{7.964\ V - 2.5\ V}{30\ \Omega} \right)$$
$$I_{SD} = \left(\frac{6.464}{30\ \Omega} \right)$$
$$I_{SD} = 0.1821\ A \quad (4)$$

Two assumptions exist for the preceding calculations: Five diodes are used with a voltage drop of 500 mV each and three shunt resistors, each with 10-Ω resistance, are connected to the loop.

The TVS diode is the front line of protection for the circuit from surges. After the TVS diode, a string of diodes is connected to the loop. The current through the loop flows through the diodes and creates a voltage drop. This voltage drop is to be used by the DC-DC converter.

In 4-mA to 20-mA loop systems, the sensor transmitter is sometimes placed far away from the controller and the power supply. Thus the voltage available in the loop can be limited. To enable the user to decide the insertion loss, the device has been designed to select the number of diodes in the loop. Headers (J14) with shunts are provided to simply short the diodes. This feature enables the user to decide the least voltage drop possible for the application. The following Table 2 explains the configuration of the headers.

Table 2. Pin Configuration of Header J14

HEADER J14 PIN NUMBERS	DIODES CONNECTED	VOLTAGE DROP AT 3.37 mA; 20°C
1 to 2	D1 – Schottky diode	≈380 mV
3 to 4	D2 – silicon diode	≈550 mV
5 to 6	D3 – silicon diode	≈550 mV
7 to 8	D4 – silicon diode	≈550 mV
9 to 10	D5 – silicon diode	≈550 mV

Connecting the shunts across the header pins shorts the diodes. Placing headers across every pair from pin 3 to pin 10 shorts all the silicon diodes. *Please note that not all the diodes are shorted*. The design includes a Schottky diode to provide an opportunity to test the design at low insertion losses (see Figure 8).

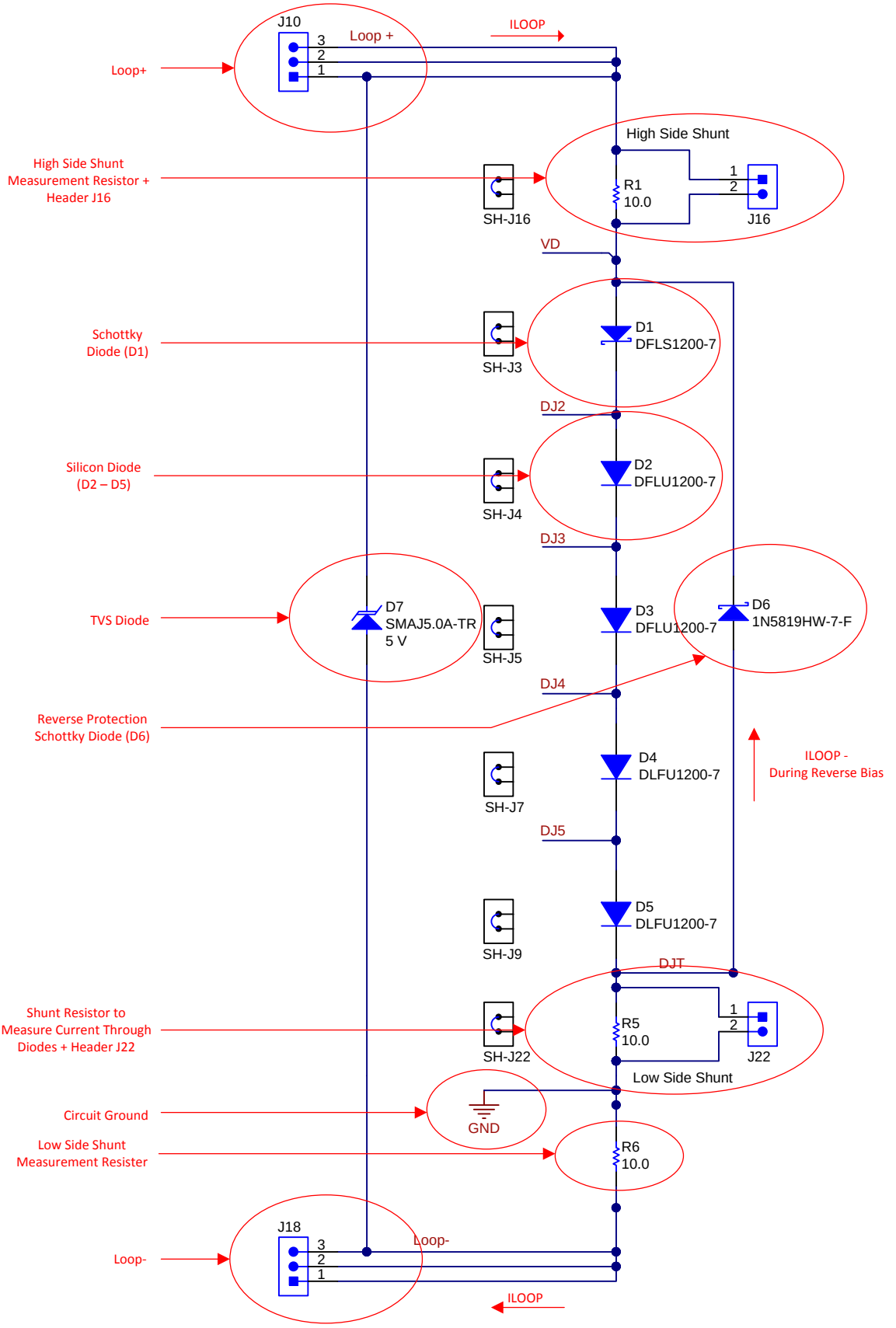


Figure 8. Loop Insertion Section With Surge Protection and Reverse Polarity Protection

The designer must note a special situation when considering the Schottky diode (D1). If an application requires the harvester device to start at high operating temperatures (125 °C for example) at the default current (3.37 mA) flowing through the loop, then the voltage drop across the Schottky diode D1 would be approximately 220 mV. This voltage would not be sufficient for the boost charger (BQ25570) during a cold start. Thus, the BQ25570 would not start as expected. To overcome this situation, all the diodes can be introduced to the loop. The voltage drop across all diodes is sufficient for the boost charger to switch from cold start to high-efficiency boost mode. When the BQ25570 device switches from cold start to the high-efficiency boost mode, diodes D2 to D5 can be short.

To achieve this switch, an N-channel MOSFET is used. The gate of the MOSFET is connected to the V_{BAT_OK} pin. The source is connected to the common ground of the circuit. The drain of the MOSFET is connected to the header J7. Table 3 details the pin configuration of the header J7.

Table 3. Pin Configuration of Header J7

HEADER J7 PIN NUMBERS	CONNECTION DETAILS
1 to 2	Place shunt to connect drain of MOSFET to pins 3, 5, 7, and 9 on header J7
3 to 4	Placing a shunt on this pin shorts all silicon diodes D2 to D5
5 to 6	Placing a shunt on this pin shorts all silicon diodes D3 to D5
7 to 8	Placing a shunt on this pin shorts silicon diodes D4 and D5
9 to 10	Placing a shunt on this pin shorts silicon diode D5

Please note to place a shunt on pins 1 and 2 to connect the drain to the other pins. Also note that placing a shunt on pins 3 and 4 shorts all the silicon diodes (D2 through D5). To introduce all the diodes in the loop during start-up, it is mandatory to remove all other shunts from header J14.

When the N-channel MOSFET is not required for the intended application, remove the shunt from header J8. This removal disconnects the MOSFET from the VBAT_OK pin of the BQ25570 device.

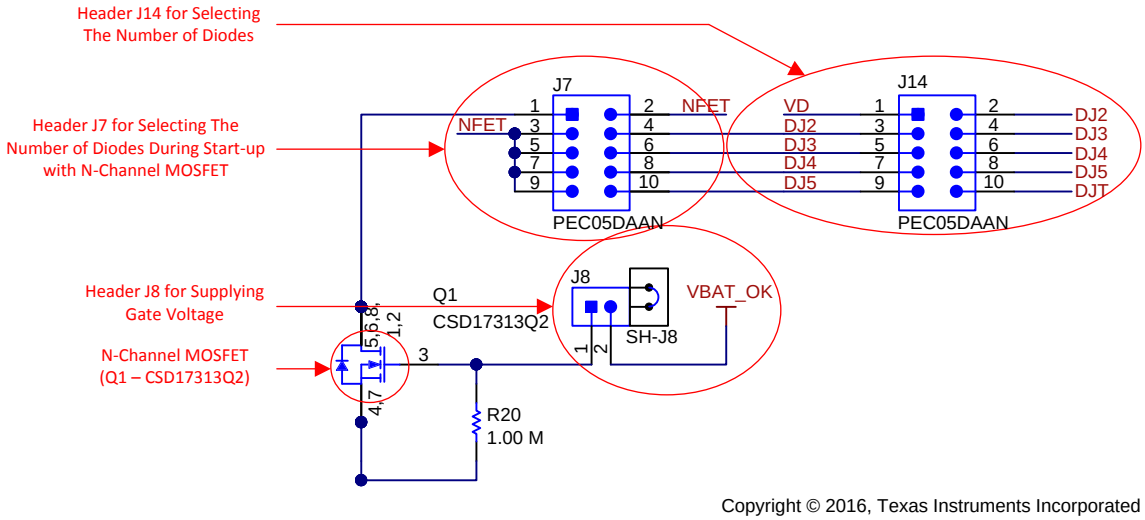


Figure 9. Insertion Voltage Drop Selection Header Configuration

2.2 Reverse Polarity Protection

In two-wire systems, it is necessary to take utmost care to connect the device in the correct polarity; if not, expensive connectors must be installed to ensure that the device is not connected in reverse polarity. To avoid destroying the BQ25570 device if it has been connected in reverse polarity, connect a low forward-bias-voltage Schottky diode (D6) in reverse bias. If the device has been connected in reverse bias, the diode string is also in reverse bias and the single Schottky diode will be connected in forward bias.

The BQ25570 device can withstand a maximum negative voltage of up to 300 mV. Selecting a Schottky diode with a very-low forward-voltage drop is necessary. Considering the worst-case scenario, which is to have the lowest operating temperature and highest current flowing through the loop, the forward voltage drop of the Schottky diode should not exceed the 300-mV limit. The Schottky should also be able to withstand surge currents. After considering these parameters, a 1N5819HW-7-F Schottky diode was selected. The forward voltage drop of the diode is less than 300 mV.

Another Schottky diode (D9) is placed in reverse bias before the input pin of the BQ25570 device. This diode is placed in reverse bias which provides an alternative path for the forward voltage of the reverse protection diode. The preceding Figure 8 shows the reverse protection circuit.

2.3 Loop Current Measurement

The main purpose of loop power harvesting is to power an external communication device or to power an indicator. Measuring the current in the loop is a prerequisite to display the measured current in an indicator or to send the data over a wireless communication device. To enable this, a high-side (R1) and low-side (R6) measurement shunt resistor is added to the design. The user can decide to use the low-side or high-side shunt as per the requirements of the application. To enable measurement of the HART modulation with a low influence of noise, an active 10-kHz active low-pass filter has been designed in the low-side shunt (see Figure 10). An additional shunt resistor is provided to measure the current through the diode string.

The main design challenge for the active filter is to terminate the ground of the circuit to a common ground point. By terminating the ground before the low-side shunt resistor, the voltage measured across this resistor will have a negative potential. Hence, an inverting low-pass filter has been designed to provide a positive voltage output. Multiple-feedback architecture was also used to achieve this effect.

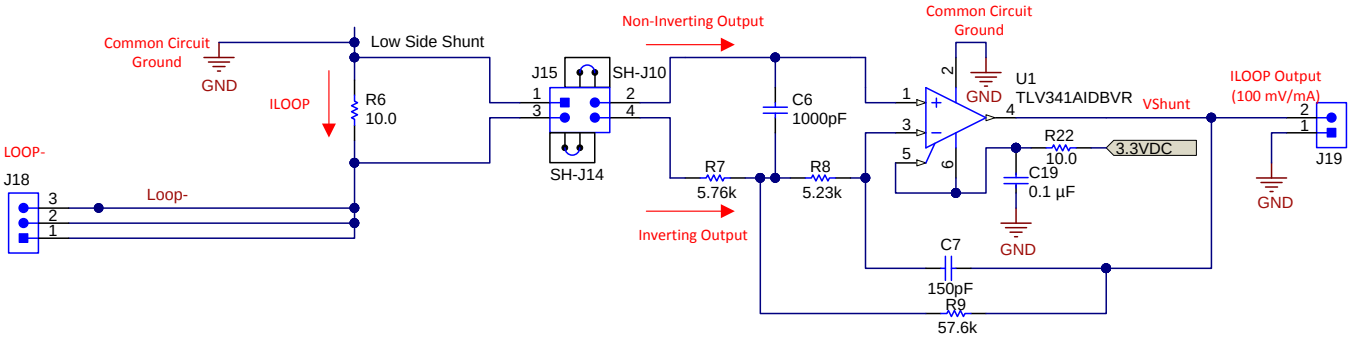


Figure 10. Active Low-Pass Filter Circuit

A 100–Ω resistor can be used to increase the sensitivity of the device; however, when 20 mA of current flows through the loop, an additional 2-V drop is introduced in the loop. To avoid this additional drop, a 10-Ω resistor is used and a gain of 10 is set in the active low-pass filter. resistors R7 and R9 are used for setting the gain. To enable the user to measure the current through the diode string a resistor (R5) has been provided below the string of diode. Table 4 details the header configuration for the high-side and low-side shunt.

Table 4. Header Configuration on Shunt Resistors

HEADER DETAILS	PIN NUMBER	COMMENTS
J16	1	During measurement, connect to positive terminal of measurement device
	2	During measurement, connect to ground terminal of measurement device
	1 to 2	Place shunt to short the shunt resistor R1
J22	1	During measurement, connect to positive terminal of measurement device
	2	During measurement, connect to ground terminal of measurement device
	1 to 2	Place shunt to short the shunt resistor R1
J15	1	During measurement, connect to positive terminal of measurement device
	2	Connected to non-inverting terminal of op amp
	3	During measurement, connect to ground terminal of measurement device
	4	Connected to inverting terminal of op amp
	1 to 2	Place shunt to connect the resistor to non-inverting terminal of op amp
	3 to 4	Place shunt to connect the resistor to inverting terminal of op amp
	1 to 3	Place shunt to short the shunt resistor R6
	2 to 4	Place shunt to connect the inverting and non-inverting terminals to avoid floating terminals
J19	1	Output of op amp, provides positive voltage
	2	Connected to common circuit ground
J1	1 to 2	Place shunt to connect the op amp to the buck output

The headers provide the flexibility to measure the current through the loop or to simply short the shunt resistor to avoid the additional voltage drop introduced in the loop. Note to remove the shunt across the header J1, when the current in the loop is not measured with the low-side shunt, as doing so disconnects the power supply to the op amp. The op amp is powered from the harvested energy from the loop.

2.4 BQ25570 Parameters

The main focus of the design was to provide flexibility for testing the functionality of the BQ25570. Table 5 shows the various header settings.

Table 5. Header Configurations of BQ25570 IC

HEADER DETAILS	HEADER DESCRIPTION	COMMENTS
J2	MPPT percentage	Place shunt across 1 through 2 for 50% MPPT
		Place shunt across 3 through 4 for 80% MPPT
		Place shunt across 5 through 6 for 95% MPPT (external resistor configuration)
J6	V_{IN} connection	Place shunt across pins 1 through 2 to connect the BQ25570 device to the loop
J9	External V_{REF_SAMP}	Shunt uninstalled
J11	Buck enable when V_{BAT_OK} is high	Place shunt across pins to configure the buck to be enabled only when VSTOR is higher than VBAT_OK
J12	Buck enable	Place shunt across pins 1 through 2 to disable the buck converter
		Place shunt across pins 2 – 3 to enable the buck converter
J13	V_{BAT_OK} pinout	External flag interrupt for microcontrollers or for measurement
J17	VSTOR – boost output	Pins 1, 2; ground
		Pins 3, 4; 4.2-V output
J20	Device enable	Place shunt across pins 1 through 2 to enable the IC
		Place shunt across pins 2 through 3 to disable the IC
J21	V_{BAT}	Connect external capacitor of required capacitance
J24	V_{OUT} – buck output	Pins 1, 2; ground
		Pins 3, 4; 3.3-V output

Table 5. Header Configurations of BQ25570 IC (continued)

HEADER DETAILS	HEADER DESCRIPTION	COMMENTS
J25	Storage capacitance	Place shunt across pins 1 through 2 to connect 1000 µF
		Place shunt across pins 3 through 4 to connect 220 µF

MPPT is implemented to maximize the power extracted from the energy harvester source. The boost charger indirectly modulates the input impedance of the main boost charger by regulating the input voltage of the charger, as sensed by the VIN_DC pin, to the sampled reference voltage, as stored on the VREF_SAMP pin (see Equation 5). The MPPT circuit obtains a new reference voltage every 16 s (typically) by periodically disabling the charger for 256 ms (typically) and sampling a fraction of the open-circuit voltage (V_{OC}). Connecting the V_{OC_SAMP} to VSTOR internally sets the MPPT regulation point to 80% of V_{OC}. Connecting the V_{OC_SAMP} to GND internally sets the MPPT regulation point to 50% of V_{OC}. The exact ratio for MPPT can be optimized to meet the requirements of the input source being used by connecting external resistors R_{OC1} and R_{OC2} between V_{IN_DC} and GND with the midpoint at V_{OC_SAMP}.

$$V_{REF\_SAMP} = V_{IN\_DC}\ (\text{Open Circuit}) \left(\frac{R11 + R12}{R11 + R12 + R10} \right) \tag{5}$$

To prevent the storage capacitor from completely depleting, the boost charger has an internally-set undervoltage threshold (VBAT_UV) plus an internal hysteresis voltage ($V_{BAT\_UV\_HYST}$). The undervoltage threshold when battery voltage is increasing is given by V_{BAT_UV} plus BAT_UV_HYST. For the V_{BAT_UV} feature to function properly, the system load should be connected to the VSTOR pin and the storage element should be connected to the VBAT pin. When the VSTOR pin voltage goes above the V_{BAT_UV} plus $V_{BAT\_UV\_HYST}$ threshold, the VSTOR pin and the VBAT pins are effectively shorted through an internal PMOS FET. The switch remains closed until the VSTOR pin voltage falls below the V_{BAT_UV} threshold. The V_{BAT_UV} threshold should be considered for a fail-safe to the system and the system load should be removed or reduced based on the V_{BAT_OK} threshold, which is ideal to set above the V_{BAT_UV} threshold.

To prevent overcharging a capacitive storage element, the overvoltage threshold level (V_{BAT_OV}) must be set using external resistors. This threshold level is also the voltage value at which the charger regulates the VSTOR/VBAT pin when the input has sufficient power. Equation 6 calculates the V_{BAT_OV} threshold when the battery voltage is rising:

$$V_{BAT\_OV} = \frac{3}{2} V_{BIAS} \left(\frac{R14 + R13}{R14} \right) \tag{6}$$

The sum of the resistors is recommended to be no higher than 13 MΩ, that is, $R_{OV1} + R_{OV2}$ = 13 MΩ. When the battery voltage is decreasing, the overvoltage threshold is calculated by V_{BAT_OV} minus $V_{BAT\_OV\_HYST}$. When the voltage at the battery exceeds the V_{BAT_OV} threshold, the boost charger is disabled. The charger starts again when the battery voltage drops by $V_{BAT\_OV\_HYST}$. When there is excessive input energy, the VBAT pin voltage ripples between the V_{BAT_OV} and $V_{BAT\_OV\_HYST}$ levels.

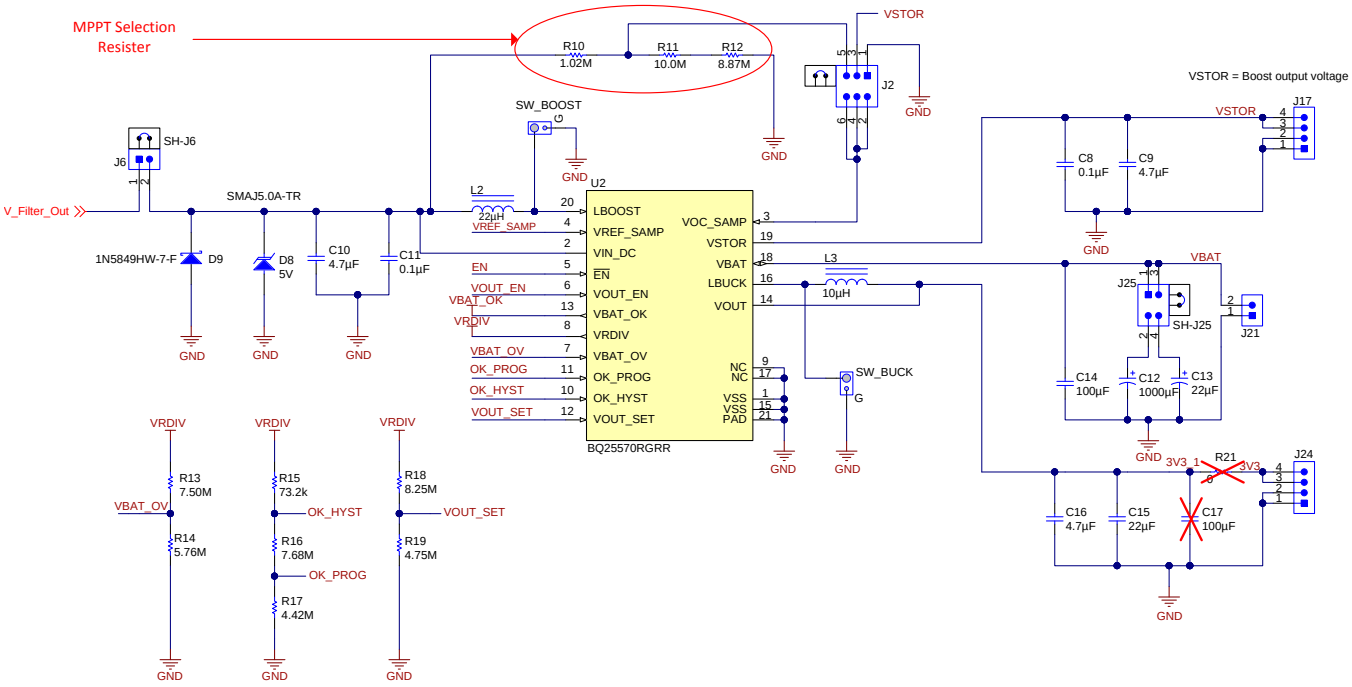


Figure 11. Energy Harvester Circuit Using BQ25570 IC

The buck regulator input power is internally connected to VSTOR and steps the VSTOR down to a lower regulated voltage at the OUT pin. The buck regulator also employs pulse frequency modulation (PFM) control to regulate the voltage close to the desired reference voltage. The voltage regulated at the OUT pin is set by the user-programmed resistor divider. To set the proper output regulation voltage and input-voltage power-good comparator, the external resistors must be carefully selected. Equation 7 shows the formulae for selecting the output voltage:

$$V_{BAT\_OK\_PROG} = V_{BIAS}\left(\frac{R17 + R16}{R17}\right)$$

$$V_{BAT\_OK\_HYST} = V_{BIAS}\left(\frac{R17 + R16 + R15}{R17}\right) \quad (7)$$

Refer to SLUC484 for all the calculations.

$$V_{OUT} = V_{BIAS}\left(\frac{R18 + R19}{R19}\right) \quad (8)$$

2.5 Load Switch

The switch-select input pin (IN) of the load switch is connected to the VBAT_OK signal (see Figure 12). Controlling the load switch by the VBAT_OK signal avoids loading the buck before the boost charger has completely charged. The load switch is powered from the boost output (VSTOR). The NO (normally open) pin is connected to the 3V3 output pin of the header J24 (pins 3 and 4). All add-on functions and applications to be powered by this reference design must be connected to this 3V3 output.

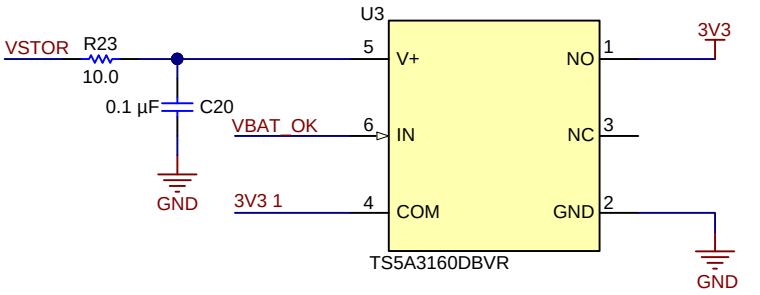


Figure 12. Load Switch

3 Testing and Results

This section addresses all the test results of all the sub parts from Section 2. This section also addresses the required header settings to ease the header connections. Figure 7 shows the important sections of the circuit to consider for the test, which this guide details further in the following subsections.

3.1 Test 1: Insertion Voltage Drop + Reverse Polarity Protection

The goal of the test is to measure the forward voltage drop across the diodes D1 through D5 at different loop currents and to measure the forward voltage drop of the reverse protection diode D6. The forward voltage across individual diodes or as a combination can be measured by placing or removing shunts on pins 1 through 10 on header J14.

The current through the diode introduces a voltage drop in the loop. This voltage drop can be measured on the anode of the diode. With an increase in loop current, the voltage drop also increases respectively. *Note to short the shunt resistors for this test*. The shunt resistors introduce additional voltage drop in the loop.

Requirements:

- Source measurement unit
- Keysight B2900A Quick measurement software (used during test)

The test is performed with a source measurement unit, as Figure 13 shows. Remove the shunt from header J6 to disconnect the DC-DC converter from the circuit. Connect the positive of the *FORCE* and *SENSE* of channel 1 to the *LOOP+* and the ground to *LOOP–*, as Figure 13 shows. Set channel 1 as the current source. Set channel 1 as a four-wire system and set the termination as floating. Apply a compliance voltage of 5 V because the overall voltage drop across all diodes and shunt resistors does not increase more than 5 V.

Channel 1:

- Source: current source
- Compliance voltage: 5 V
- Four-wire system
- Termination: floating

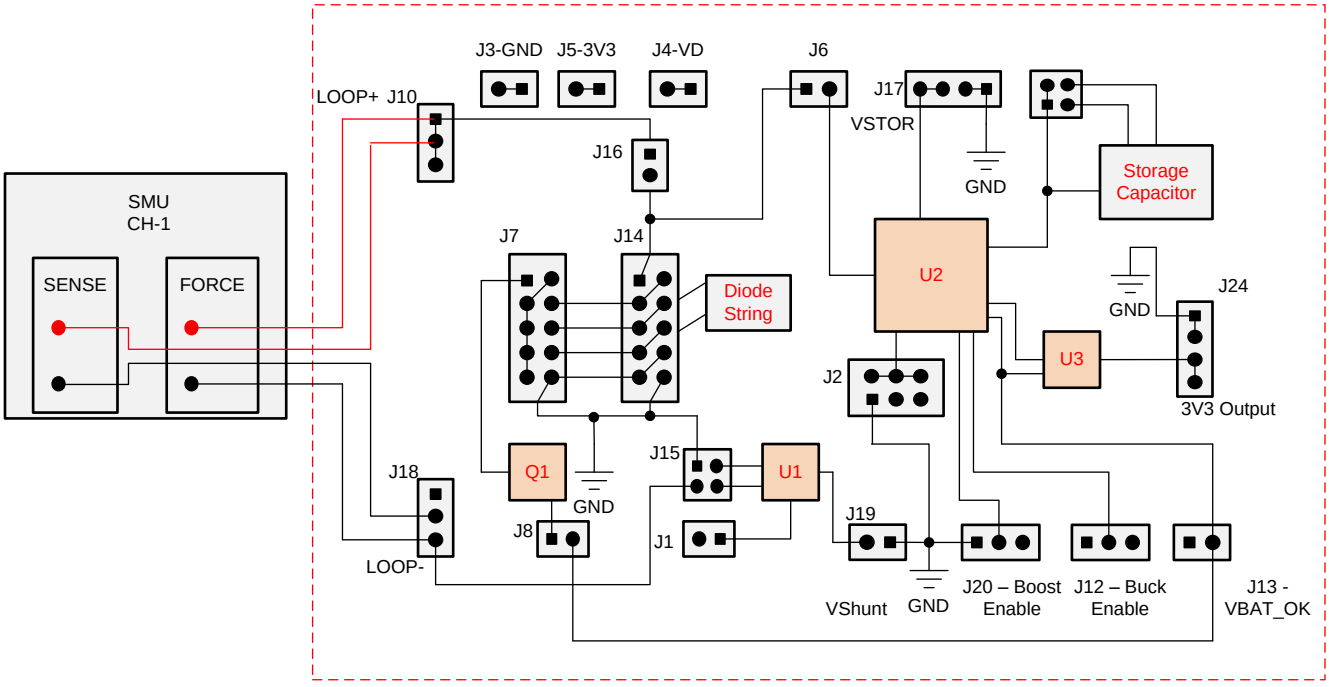


Figure 13. Insertion Voltage Drop Test Configuration

Apply current values as variable and set a start value of 4 mA and an end value of 20 mA. Make sure the sweep count is 17 and the step increase is 1 mA per count. Remove the shunt from header J14 between pins 1 through 2, which introduces D1 (Schottky diode) to the loop. Note to short all measurement shunt resistors to determine the forward voltage drop of diodes. To measure the forward voltage drop, connect the positive terminal of the measurement probe (oscilloscope or multimeter) to a pin of header J4 and connect the ground of the probe to the ground port J3 on the board.

Run the measurement to find out the forward voltage drop of the diode. When the quick measurement software is used, the measurement table displays the measured voltage and current. The input voltage can be obtained from this table and this is the forward voltage of the single Schottky diode.

Place the shunt across pins 1 through 2 in header J14 and remove header from pins 3 through 4 to introduce D2 (silicon diode) to the loop. Run the measurement to obtain the forward voltage drop of a single silicon diode. Remove or add shunts on header J14 across pins 1 through 10 to further introduce the silicon diodes and Schottky diode to the loop as per the required combination. The possible combinations have been tested and summarized in the following Table 6.

Table 6. Insertion Voltage Drop on Diodes

SL-NO.	LOOP CURRENT	SCHOTTKY DIODE (D1)	SILICON DIODE (D2)	D1 + D2	D1 + D2 + D3	D1 + D2 + D3 + D4	D1 + D2 + D3 + D4 + D5
1	4	0.391	0.532	0.922	1.453	1.983	2.515
2	5	0.399	0.540	0.938	1.477	2.016	2.556
3	6	0.405	0.547	0.952	1.498	2.044	2.591
4	7	0.411	0.553	0.964	1.515	2.067	2.621
5	8	0.416	0.559	0.974	1.531	2.088	2.647
6	9	0.420	0.563	0.984	1.545	2.108	2.671
7	10	0.425	0.568	0.992	1.559	2.125	2.692
8	11	0.430	0.572	1.000	1.571	2.141	2.712
9	12	0.434	0.576	1.008	1.582	2.156	2.731
10	13	0.437	0.579	1.015	1.593	2.170	2.748
11	14	0.441	0.582	1.022	1.603	2.183	2.765
12	15	0.444	0.585	1.028	1.612	2.195	2.780
13	16	0.448	0.588	1.034	1.621	2.207	2.794
14	17	0.451	0.591	1.040	1.629	2.218	2.808
15	18	0.454	0.593	1.046	1.637	2.228	2.821
16	19	0.457	0.596	1.051	1.645	2.238	2.833
17	20	0.460	0.598	1.056	1.653	2.248	2.845

The preceding Table 6 shows the voltages across the diodes at different loop current. Figure 14 shows the increase in voltage drop as current increases. From the table and the graph, it is evident that the voltage drop of the various combinations not discussed here can be calculated. For example, the combination of two silicon diodes (D2 + D3) is 1064 mV at 4 mA.

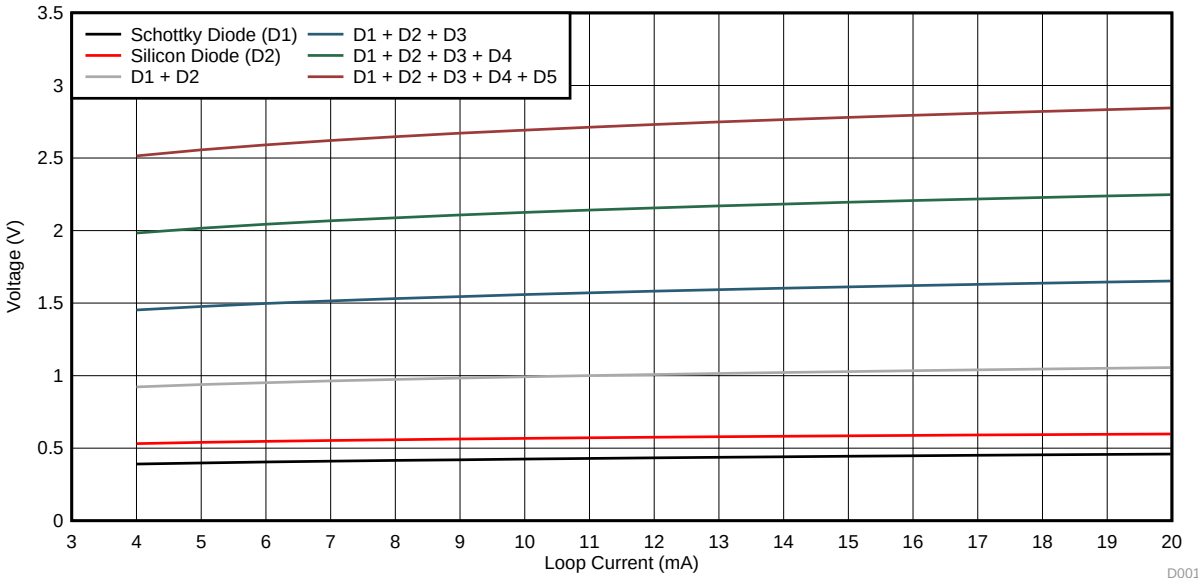


Figure 14. Graph of Insertion Voltage Drop

Reverse polarity protection:

For reverse polarity protection measurement, connect the ground of the sensor transmitter to the LOOP– (J18) and the ground of the power supply to the LOOP+ (J10). Figure 15 shows the connection for reverse polarity protection. Run the measurement to measure the forward voltage of the reverse protection diode. The measured positive forward voltage across the protection diode is the voltage that flows toward the input of the BQ25570 device with a negative potential.

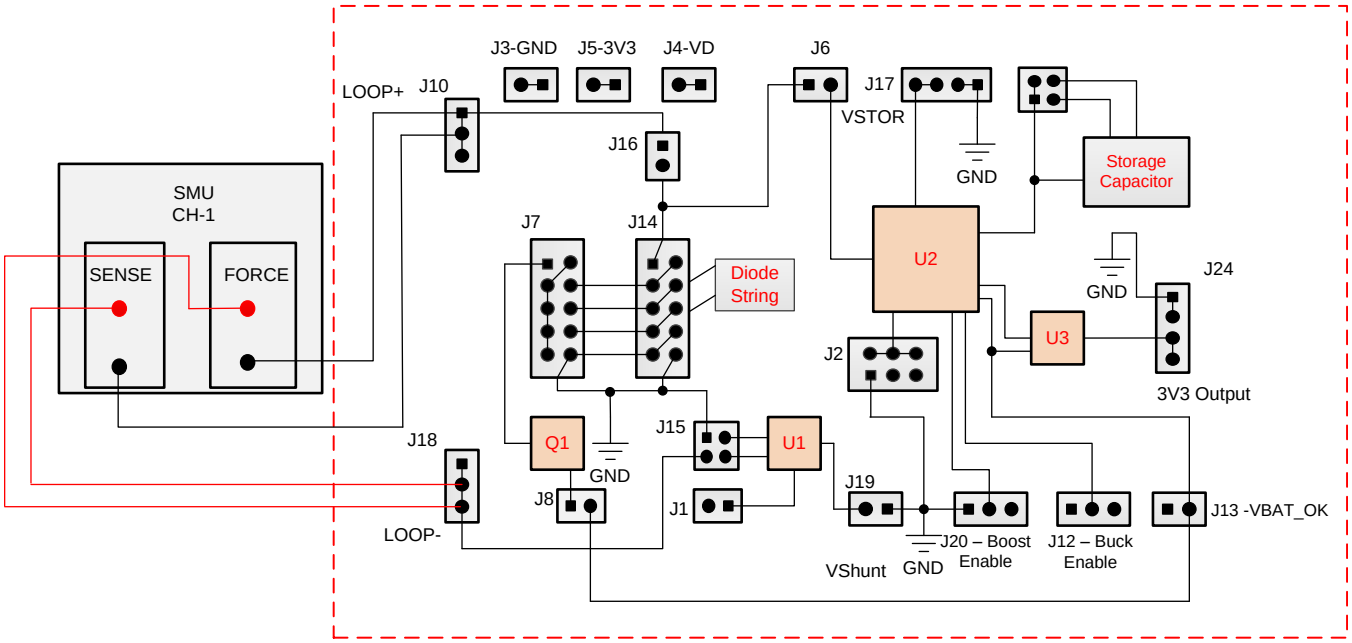


Figure 15. Reverse Polarity Protection Test Configuration

Figure 16 shows the forward voltage drop of the reverse polarity protection Schottky diode. The BQ25570 device can withstand up to –300 mV as an absolute maximum rating. The reverse polarity protection of the circuit is provided by D6, D9, C10, C11, and the filter circuit between D6 and D8. This design ensures protection only during transient reverse polarity condition. It also provides protection against continuous, reverse-polarity conditions in the case of a current-limited source (20 mA). For all other conditions, the protection circuit must be verified so that neither the power dissipation rating of D6 and D9 nor the input voltage rating of U2 is violated.

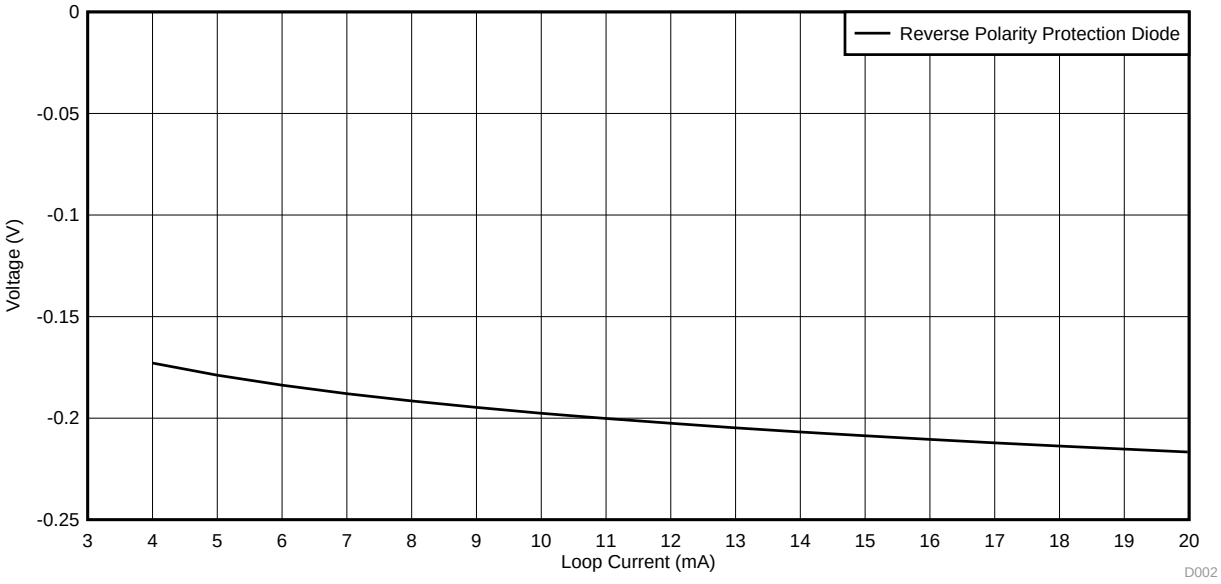


Figure 16. Graph of Reverse Protection Diodes Forward Voltage Drop

Voltage drop on shunt resistors:

The introduction of shunt resistors introduces additional voltage drop on the loop. Three shunt resistors are available in the design: high-side shunt, low-side shunt, and a shunt to measure current through the diode string. Each resistor can introduce a voltage drop of 200 mV when 20 mA flows through the resistor. To measure the voltage of each resistor, remove the shunt from header J16 and J22. For the low-side shunt (J15), place shunts on pins 1 through 2 and 3 through 4. To short the low-side shunt resistor, place a shunt on pins 1 through 3 on header J15. The voltage drop across resistors can be calculated by using Ohms law.

3.2 Test 2: Performance Analysis of BQ25570

The performance of the boost charger is a most interesting parameter to consider. Figure 17 shows the setup required to perform the performance evaluation. To perform the performance analysis of the boost charger, remove the shunt from J6 to disconnect the boost from the loop insertion circuit. Ensure that the shunt is placed between pins 1 through 2 in header J12. This placement is to connect the VOUT_EN to GND to turn on the boost charger. The buck converter must be disconnected for this test. To disconnect it, place a shunt between pins 1 through 2 in header J20.

The BQ25570 regulates the input voltage to set the MPPT percentage. When 80% is set, the device regulates the input to 80% of the open-circuit voltage. That is, when the forward voltage drop of a single silicon diode is 500 mV, the input is regulated to 400 mV, and thus a portion of the loop current flows through the diode to avoid the input voltage from collapsing and the remaining is used by the DC-DC converter. The BQ25570 regulates the input only when it boosts the voltage, which is apparent in the test as detailed further in this subsection.

Boost efficiency:

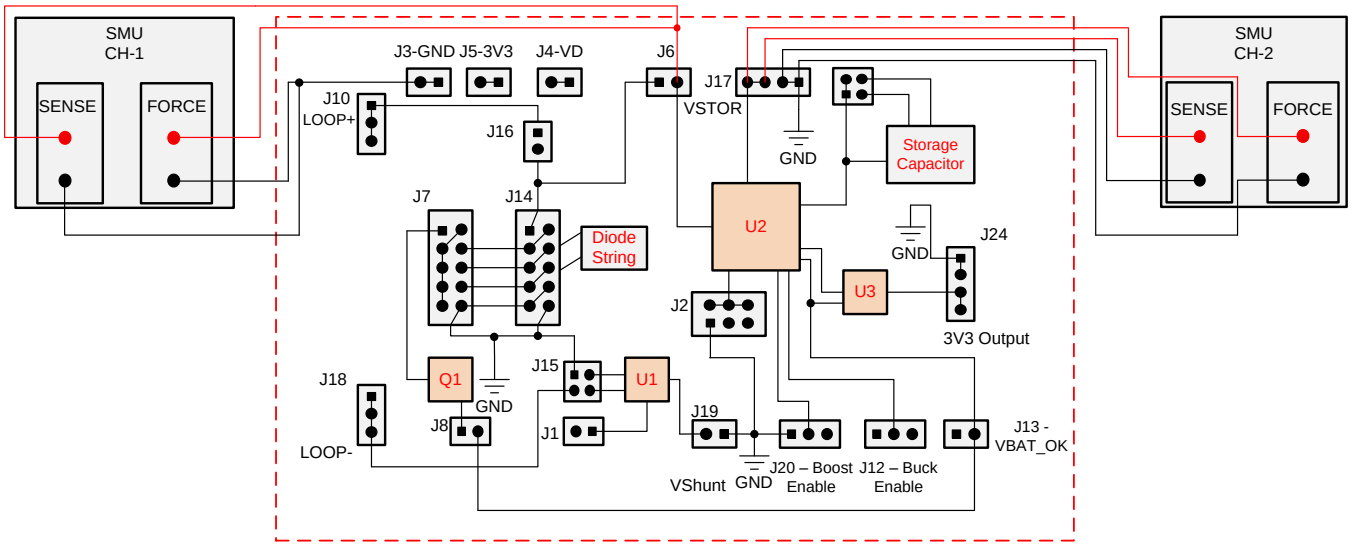


Figure 17. Boost Efficiency Test Configuration

Requirements:

- Source measurement unit
- Keysight B2900A Quick measurement software (used during test)

Connect the *SENSE* and *FORCE* from channel 1 of the SMU to pin 2 of header J6 and the ground to the GND header J3. Set channel 1 as a voltage source. Set the start voltage as 500 mV and stop voltage as 3 V. Set the step increment to 100 mV. Each measurement must be set for a 30-s measurement delay to ensure that a new sample of the set voltage is taken. Set the compliance current to 1 mA.

Connect the *SENSE* and *FORCE* from channel 2 of the SMU to pins 3 and 4 in header J17 and the ground to pins 1 and 2. Set channel 2 as a voltage source and the voltage as 3 V for a measurement and 4 V for the next measurement. Set the compliance current to 1 mA.

Channel 1:

- Source: voltage source
- Voltage output: 500 mV to 3000 mV in increments of 100 mV per step
- Compliance current: 1 mA
- Four-wire system
- Termination: floating

Channel 2:

- Source: voltage source
- Voltage output: 3 V and 4 V
- Compliance current: –1 mA(sinking)
- Four-wire system
- Termination: floating

The plot in Figure 18 shows the efficiency of the boost charger. The efficiency increases when the input increases. The minimum input voltage is set to 500 mV, but during the working of the boost charger, the DC-DC converter regulates the voltage to the set MPPT percentage (80%). The input is regulated to 400 mV. The capacitors used are totally discharged, so the device goes into cold start mode. The minimum required voltage during cold start is 330 mV (typical).

The performance is calculated by measuring the output current. The input voltage, input current, and output voltage is set. The varying factor is the output current. The device has a performance of up to 90% at a 3-V input.

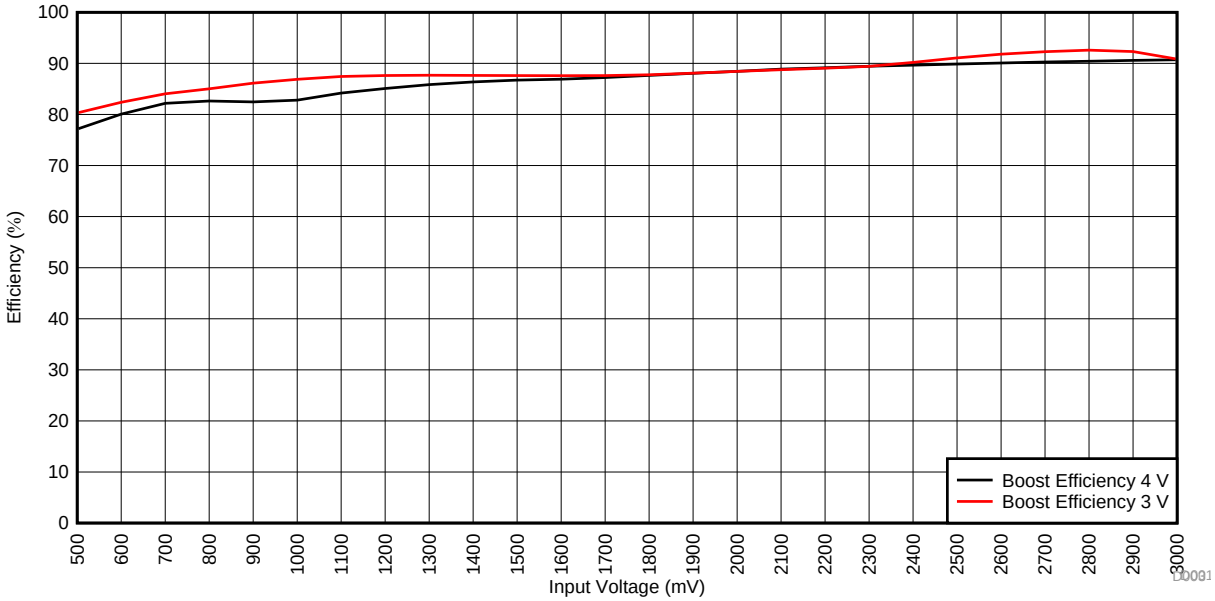


Figure 18. Graph of Boost Efficiency

Buck efficiency:

Measuring the efficiency of the buck requires to make the connections as Figure 19 shows. Channel 1 of the oscilloscope is connected to the boost and channel 2 is connected to the buck converter. The shunt from J6 is removed for this measurement. Connect a shunt across pins 2 and 3 in header J12. Leave header J20 at the default setting to measure boost performance.

Channel 1:

- Source: voltage source
- Voltage output: 3.4 V, 3.8 V, and 4.2 V per measurement
- Compliance current: 100 mA
- Four-wire system
- Termination: floating

Channel 2:

- Source: current source
- Current output: variable from –1 µA to –100 mA (sinking)
- Compliance voltage: 3.4 V
- Four-wire system
- Termination: floating

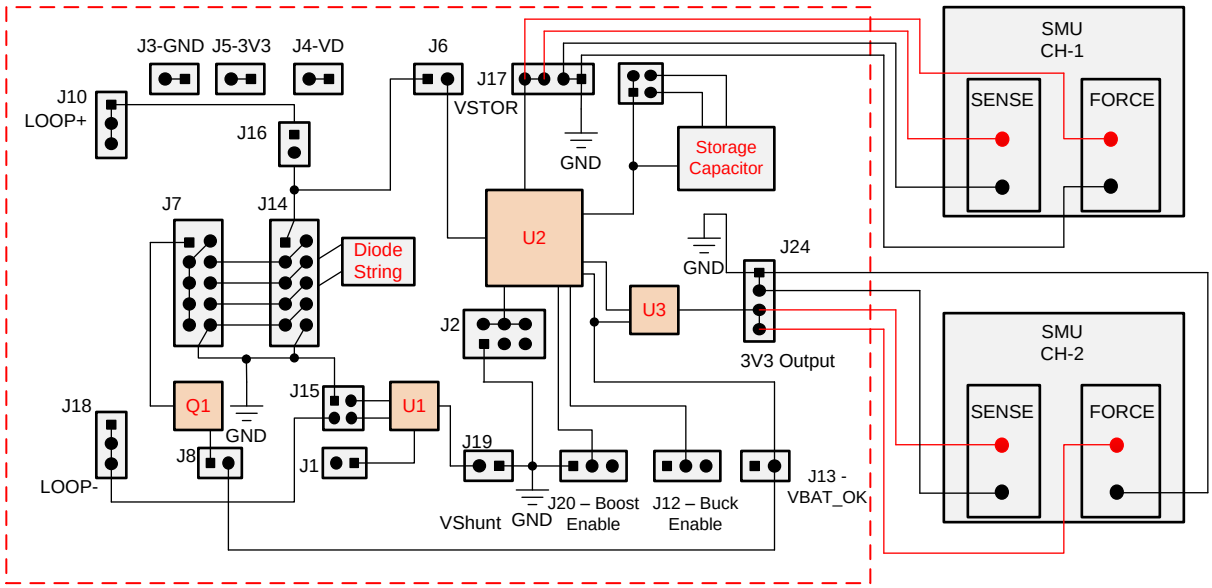


Figure 19. Buck Efficiency Test Configuration

The output of the buck is set to provide an output of 3.3 V. The buck circuit uses some current to operate, hence the low efficiency at low output currents; when the output currents are higher, the losses are higher, which is evident in the following Figure 20. The efficiency peaks between 1 mA to 30 mA and the efficiency slowly reduces. At a 3.4-V input, the current limit is set to 100 mA. This setting collapses the voltage because of the output loading. The set compliance current will be reached and the voltage source collapses. By loading the buck to an optimum level, the best performance can be achieved from the BQ25570.

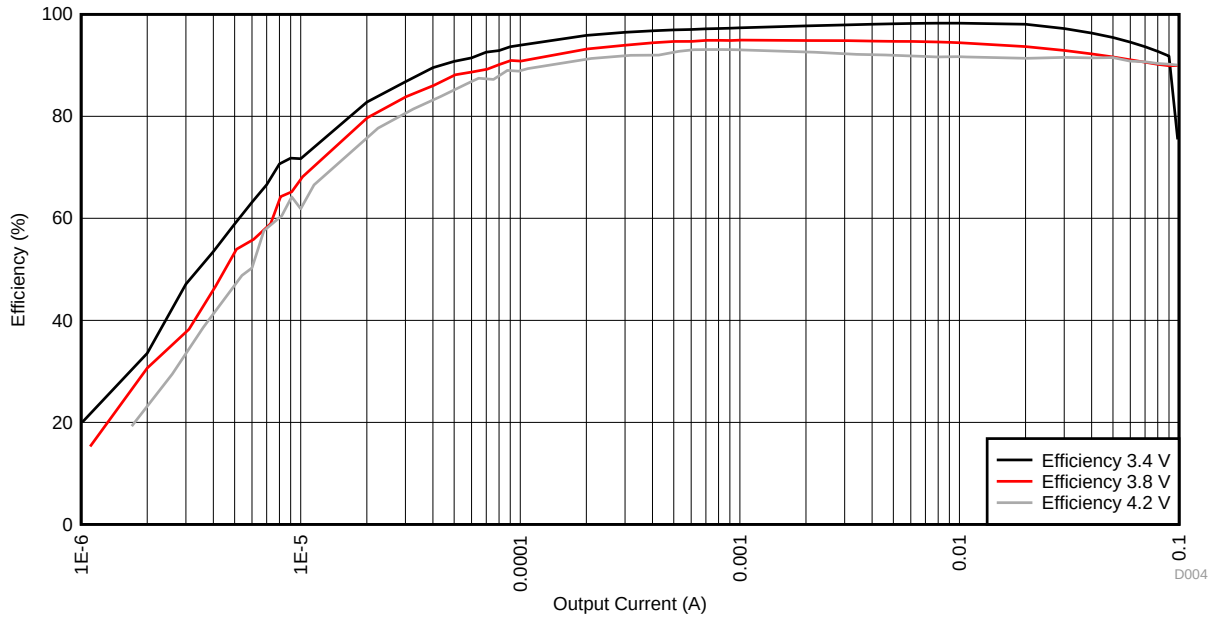


Figure 20. Graph of Buck Efficiency

3.3 Test 3: Capacitance Charging Time and Load Switch Operation

The charging time of capacitors must be measured to find out the minimum time required to start the circuit during installation. Different output capacitance is possible with the design. The minimum required capacitance is 100 µF. The capacitance can be selected with the following header configuration as Table 7 shows.

Table 7. Pin Configuration of Header J25

J25 SHUNT SETTINGS	CAPACITANCE VALUE
No shunts placed on header	100 µF
Shunt placed across pins 3 through 4	320 µF
Shunt placed across pins 1 through 2	1100 µF
Shunt placed across pins 1 through 2 and 3 through 4	1320 µF

Depending on the maximum peak-pulse output, the capacitor value must be selected. Header J21 is provided to connect to an external storage capacitance. The capacitance charging time is directly influenced by the input voltage. The charging time of the capacitors is performed for different capacitor settings for a different input voltage. The input voltage is varied by changing the number of shorted diodes in the string of diodes (D1 through D5). The diodes can be shorted or inserted in the loop by placing or removing shunts across the pins in header J7 and J14, as the preceding Section 3.1 explains.

NOTE: Do not place a shunt on header 21 to avoid shorting all the capacitors.

Requirements:

- Source measurement unit
- Keysight B2900A Quick measurement software (used during test)
- Oscilloscope with four channels

Channel 1:

- Source: current source
- Voltage output: 3.37 mA
- Compliance voltage: 5 V
- Four-wire system
- Termination: floating

Channel 1 of the SMU is connected as Figure 21 shows. The insertion voltage drop, boost output, and buck output are visible on the scope. The charging time of the capacitors can be calculated by measuring the time required for the BQ25570 device to boost the voltage on J17 to the level as given by Equation 6.

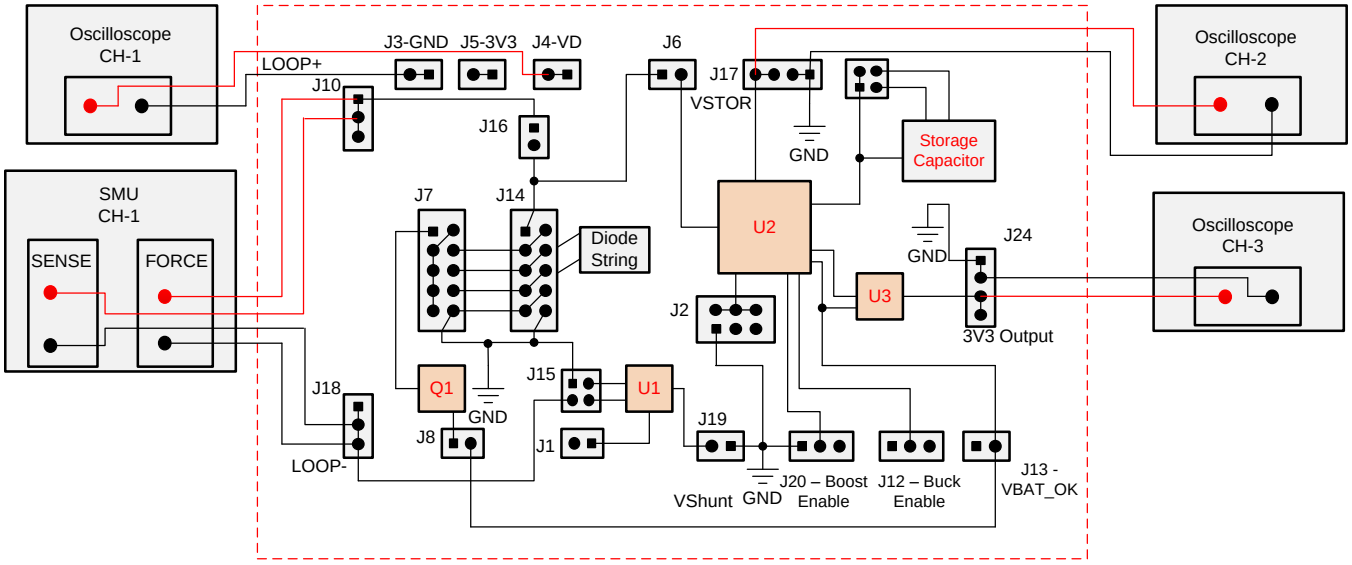


Figure 21. Capacitance Charging Time Test Configuration

The measurements are performed with the lowest current in the loop, which is done to summarize the charging time at the lowest input current. Table 8 summarizes the test results.

Table 8. Capacitance Charging Time for Different Diode Configuration

DIODE CONFIGURATION	INPUT CURRENT (mA)	CAPACITANCE	CAPACITANCE CHARGING TIME (NO LOAD)
D1 (Schottky diode)	3.37	100 µF	3 s
	3.37	320 µF	11 s
	3.37	1100 µF	37 s
	3.37	1320 µF	56 s
D2 (Silicon diode)	3.37	100 µF	1.2 s
	3.37	320 µF	6 s
	3.37	1100 µF	18 s
	3.37	1320 µF	19 s
D1 + D2	3.37	100 µF	1 s
	3.37	320 µF	3.5 s
	3.37	1100 µF	14 s
	3.37	1320 µF	18 s
D2 + D3	3.37	100 µF	1 s
	3.37	320 µF	1 s
	3.37	1100 µF	14 s
	3.37	1320 µF	18 s
D1 + D2 + D3	3.37	100 µF	1 s
	3.37	320 µF	3.5 s
	3.37	1100 µF	14 s
	3.37	1320 µF	18 s
D1 + D2 + D3 + D4	3.37	100 µF	1 s
	3.37	320 µF	3.5 s
	3.37	1100 µF	14 s
	3.37	1320 µF	18 s

Table 8. Capacitance Charging Time for Different Diode Configuration (continued)

DIODE CONFIGURATION	INPUT CURRENT (mA)	CAPACITANCE	CAPACITANCE CHARGING TIME (NO LOAD)
D1 + D2 + D3 + D4 + D5	3.37	100 µF	1 s
	3.37	320 µF	3.5 s
	3.37	1100 µF	14 s
	3.37	1320 µF	18 s

The data is collected from running tests and measuring the values from the results with an oscilloscope. The following Figure 22 shows an oscilloscope graph. The charging time is calculated by measuring the time required for the boost output to reach from start-up to 4.2 V. The input voltage sampling is visible in the graph. During start-up, a lower voltage is sampled and when the boost stops working, the BQ25570 device stops the voltage regulation. Thus the complete forward voltage drop of diodes is visible.

In the oscilloscope image of Figure 22, the working of the load switch can be realized. When the boost output reaches 3.3 V, the buck output is turned ON. This action prevents loading on the boost converter. When the voltage on the boost reduces less than 3.3 V, the buck output is turned OFF.

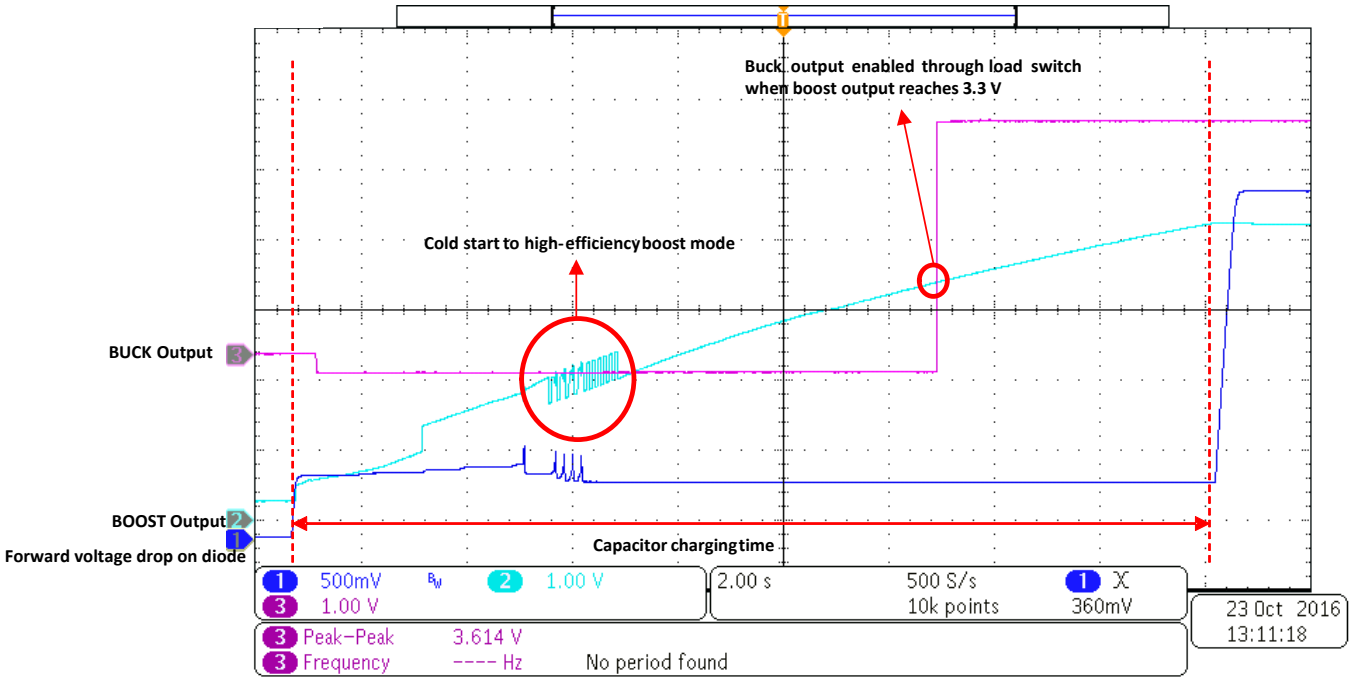


Figure 22. Screenshot on Oscilloscope Showing Image

3.4 Test 4: Continuous Current Output

Figure 23 shows the measurement setup for measuring the maximum current at the buck output of the DC-DC converters. Measuring the maximum output capable for various diode configurations is mandatory. Considering the maximum output current at the low error threshold current is also necessary.

Requirements:

- Source measurement unit
- Keysight B2900A Quick measurement software (used during test)
- Oscilloscope with four channels

Channel 1:

- Source: voltage source
- Voltage output: 3.4 V, 3.8 V, and 4.2 V per measurement
- Compliance current: 100 mA
- Four-wire system
- Termination: floating

Channel 2:

- Source: current source
- Current output: variable from –1 µA to –100 mA (sinking)
- Compliance voltage: 3.4 V
- Four-wire system
- Termination: floating

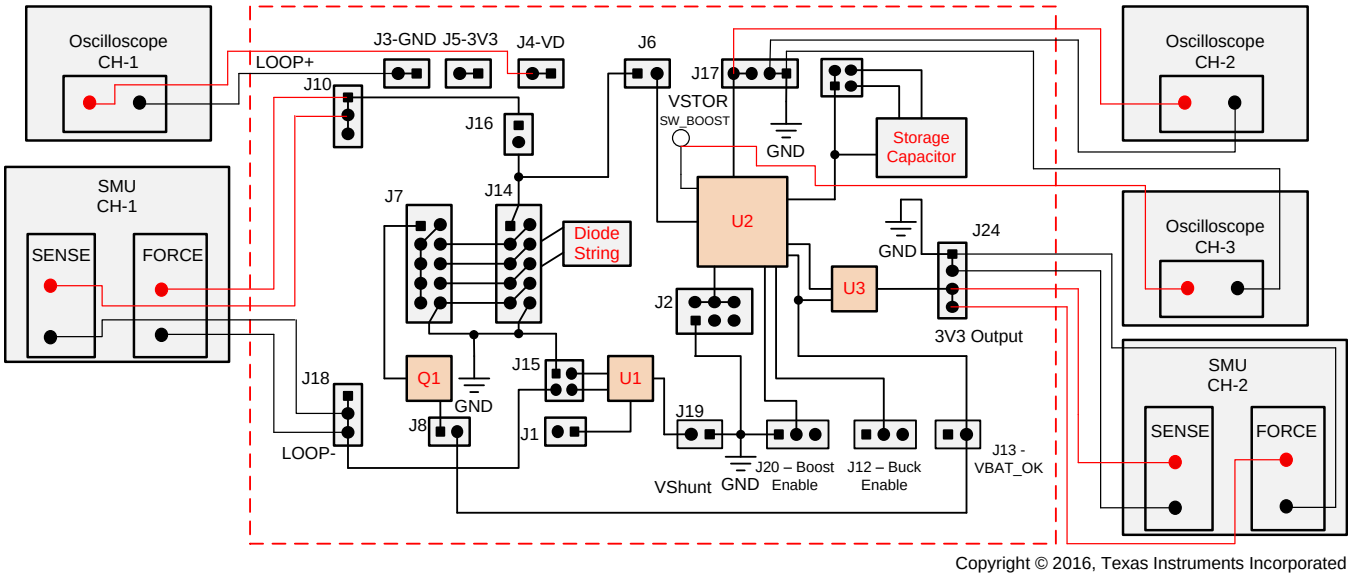


Figure 23. Continues Output Current Test Configuration

The boost charger turns off the output for MPPT sampling for a period of 256 ms. During this period, the output loading should not be higher than the threshold, after which the voltage would collapse. Table 9 shows the maximum output current for each diode configuration.

Table 9. Table of Maximum Output Current for Different Diode Configuration

DIODE CONFIGURATION	INPUT CURRENT (mA)	ICONT_OUT (mA)
D1 (Schottky diode)	3.37	0.164
D2 (Silicon diode)	3.37	0.3
D1 + D2	3.37	0.51
D2 + D3	3.37	0.61
D1 + D2 + D3	3.37	0.86
D1 + D2 + D3 + D4	3.37	1.21
D1 + D2 + D3 + D4 + D5	3.37	1.57

To calculate the maximum output current, the main criteria is that the boost output does not decrease less than 3.3 V and when the 256 ms is complete, the boost output must charge back to 4.2 V before the next cycle. If the boost output does not charge back to 4.2 V within the 16-s period, the output collapses after a certain interval. Figure 24 shows a screen shot when the boost charger is charged immediately after 256 sampling cycle.

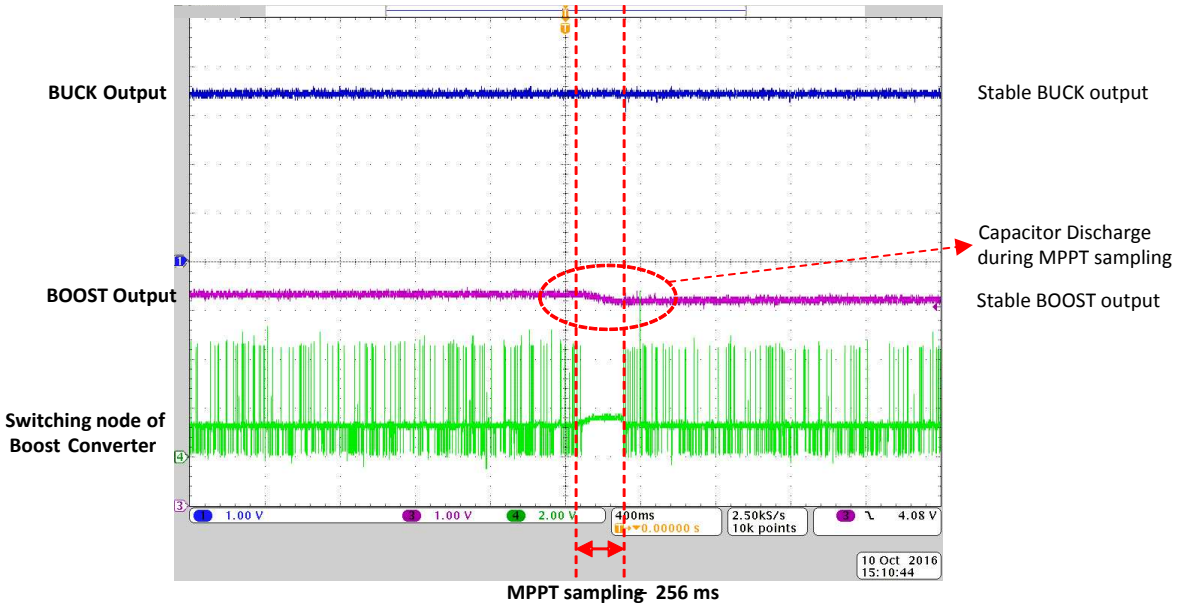


Figure 24. Stable Boost Output

Figure 25 shows that the output loading on the buck causes the boost output to reduce close to 3.3 V. Further loading causes the boost output to collapse the buck output, which Figure 26 shows.

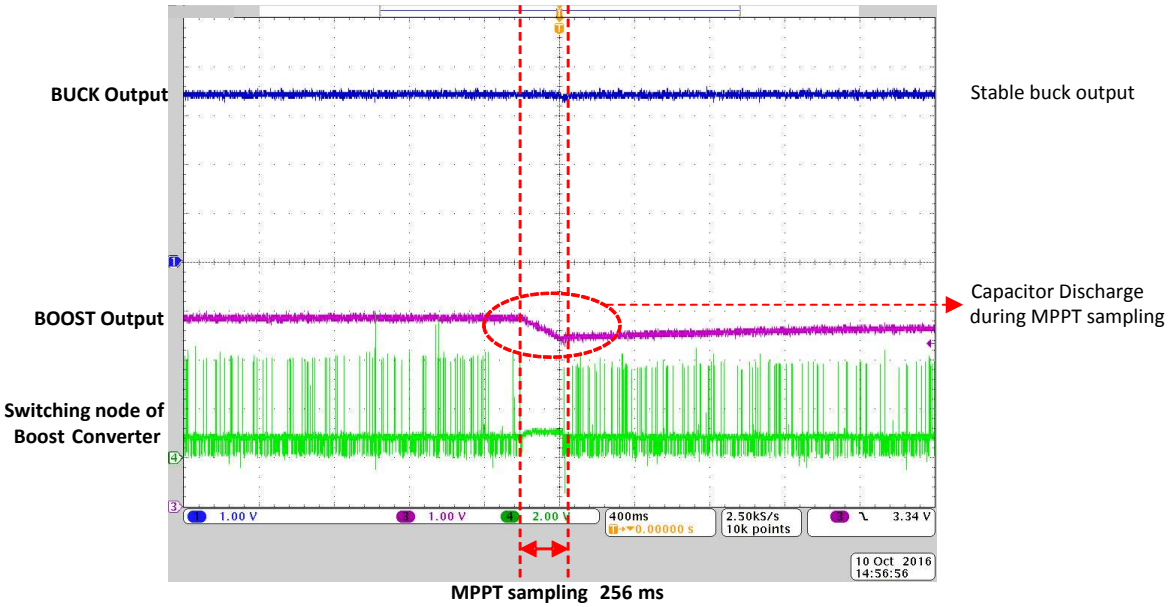


Figure 25. Maximum Loading on Buck

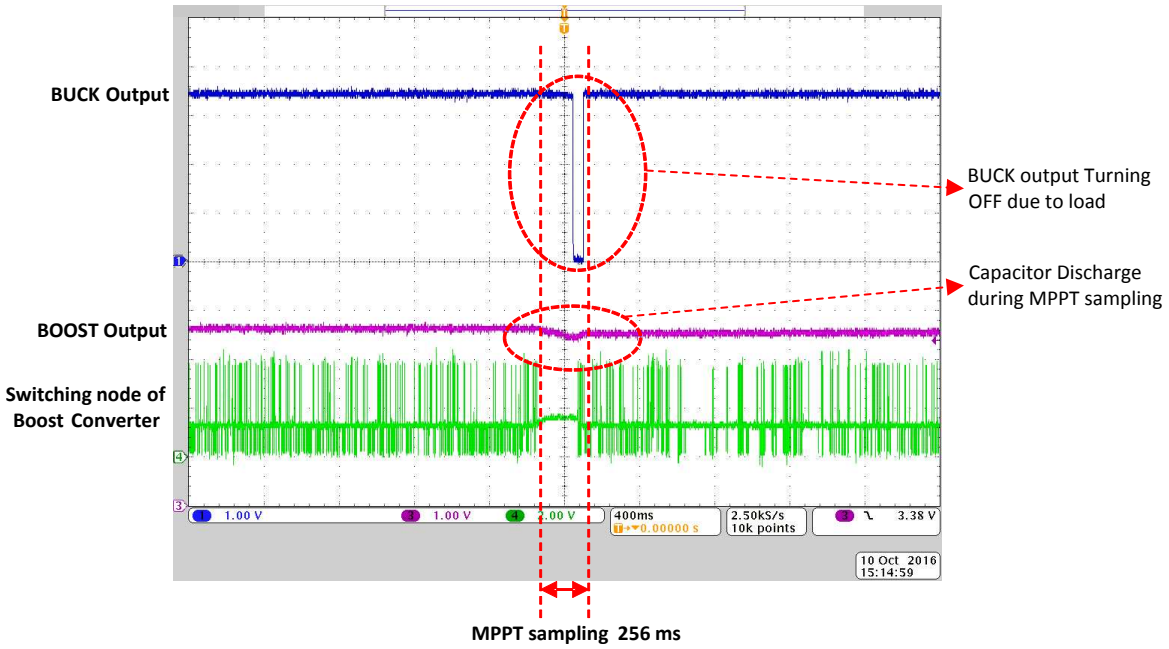


Figure 26. Overloading on Buck

3.5 Test 5: Peak-Pulse Output Current

For high-output current applications such as powering a BLE device, powering the external communication device continuously is not possible, especially when low current is flowing in through the loop. Calculating the maximum peak current and measuring the time interval at which the peak can be obtained is explained further in the section. The test is performed with an 8-mA peak and 15-mA peak pulse output. The BLE device CC2650 from Texas instruments requires about 5 mA for 5 ms per broadcast.

The connections for maximum peak pulse are similar to the maximum continuous-output current output. Figure 27 shows the connections for the test. In channel 2, the sinking current output list is 8 mA. The time interval between every pulse is varied. The BQ25570 must not be loaded until after the first 16 s of starting. This delay is to ensure that the BQ25570 device has sampled the correct input voltage to get an accurate time interval. To measure the best time interval between every peak pulse, provide a 2-s delay between the first and second pulse. Gradually reduce the pulse interval between the subsequent pulses. The optimum pulse interval is when the boost output reaches 4.2 V before the next peak pulse. Table 10 provides the output peak pulse for different diode configurations.

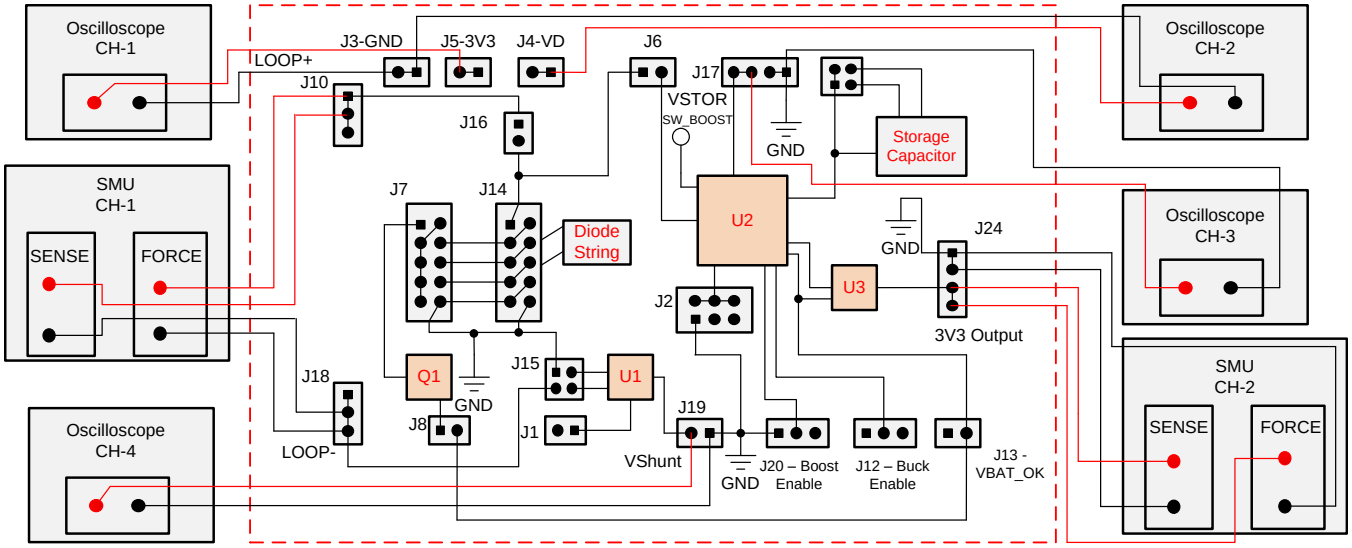


Figure 27. Peak-Pulse Output Test Configuration

Table 10. Peak-Pulse Output Interval at 8-mA Peak Output

DIODE CONFIGURATION	INPUT CURRENT (mA)	IPeak (mA)	Peak_Period (ms)	Peak_Interval (ms)
D1 (Schottky diode)	3.37	8	10	1500
D2 (Silicon diode)	3.37	8	10	600
D1 + D2	3.37	8	10	250
D2 + D3	3.37	8	10	200
D1 + D2 + D3	3.37	8	10	100
D1 + D2 + D3 + D4	3.37	8	10	90
D1 + D2 + D3 + D4 + D5	3.37	8	10	70

Table 11. Peak-Pulse Output Interval at 15-mA Peak Output

DIODE CONFIGURATION	INPUT CURRENT (mA)	IPeak (mA)	Peak_Period (ms)	Peak_Interval (ms)
D1 (Schottky diode)	3.37	15	10	2100
D2 (Silicon diode)	3.37	15	10	900
D1 + D2	3.37	15	10	400
D2 + D3	3.37	15	10	300
D1 + D2 + D3	3.37	15	10	160
D1 + D2 + D3 + D4	3.37	15	10	120
D1 + D2 + D3 + D4 + D5	3.37	15	10	100

Use the low-side shunt to measure the current through the loop. Channel 4 is directly connected to the shunt resistor. The ground of the probe is connected to the circuit ground and the positive of the probe is connected to the resistor. The output has a negative potential when referenced to the circuit ground. The output has been inverted in the oscilloscope for convenience when reading the data.

The oscilloscope image in Figure 28 shows the test results of the peak pulse output.

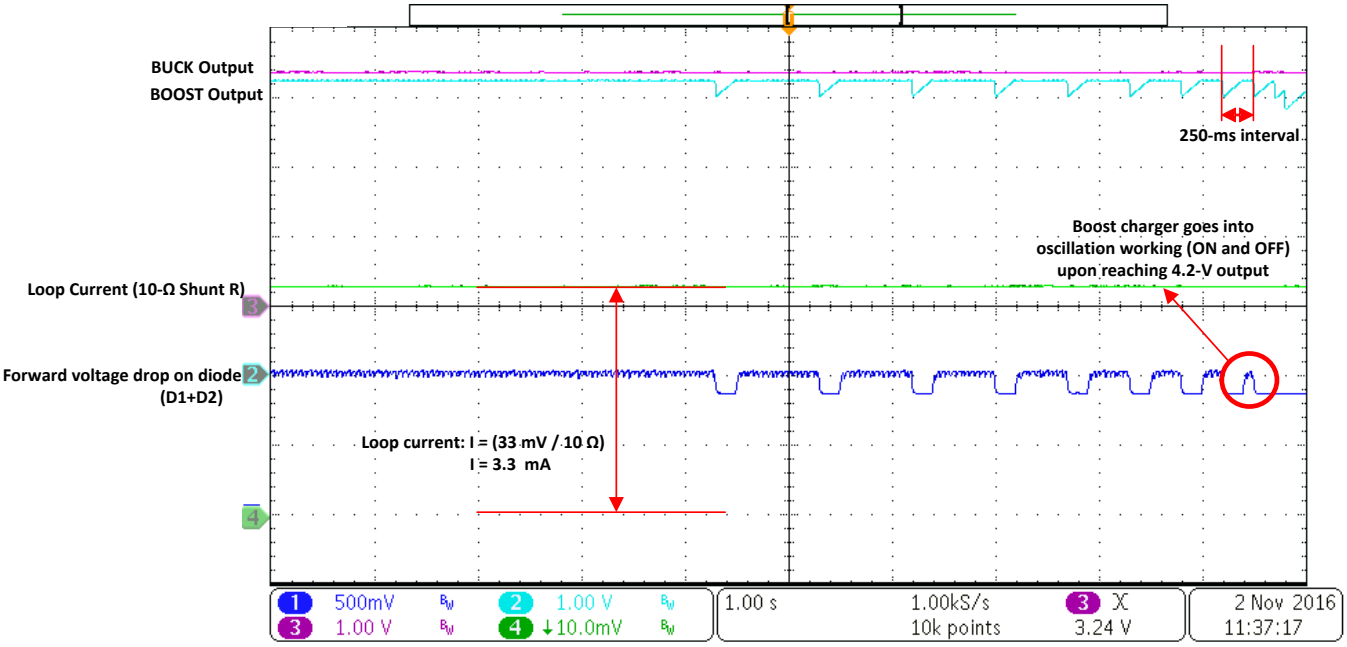


Figure 28. Test Results of Peak Pulse Output

3.6 Test 6: N-Channel MOSFET

In the design, D1 is a Schottky diode. The forward voltage drop is lower than the required input voltage during cold start. Even though the forward voltage drop is low, this diode is provided in the design to allow the user to test the performance and application possibilities. When the device is operated with an exhausted capacitor or at high temperatures, the forward voltage drop is not enough to drive the cold-start circuit. A MOSFET has been provided to avoid this issue, which is driven by the VBAT_OK signal.

Connect a shunt across pins 1 through 2 on header J8 to connect the VBAT_OK signal to the gate of the MOSFET. The number of diodes to be shorted after start-up can be selected with header J7. While performing tests with the Schottky diode (D1), all the shunts from J14 must be removed. Connect shunts across pins 1 through 2 on header J7 to connect the MOSFET to the diode string. Decide the number of diodes required after start-up. When a shunt has been placed across pins 3 through 4 on header J7, all the diodes are used during start-up and diodes D2 through D5 are shorted when the circuit starts up. If the application only requires D1 and D2 to be used during start up, place shunts across pins 5 through 10 on header J14 to short D3, D4, and D5. The oscilloscope output in Figure 29 shows how the MOSFET works.

The buck output turns OFF during the first 16-ms interval because the BQ25570 device has sampled a higher voltage than what is available upon reaching the set 3.3-V VBAT_OK threshold. This issue is automatically rectified during the second MPPT cycle.

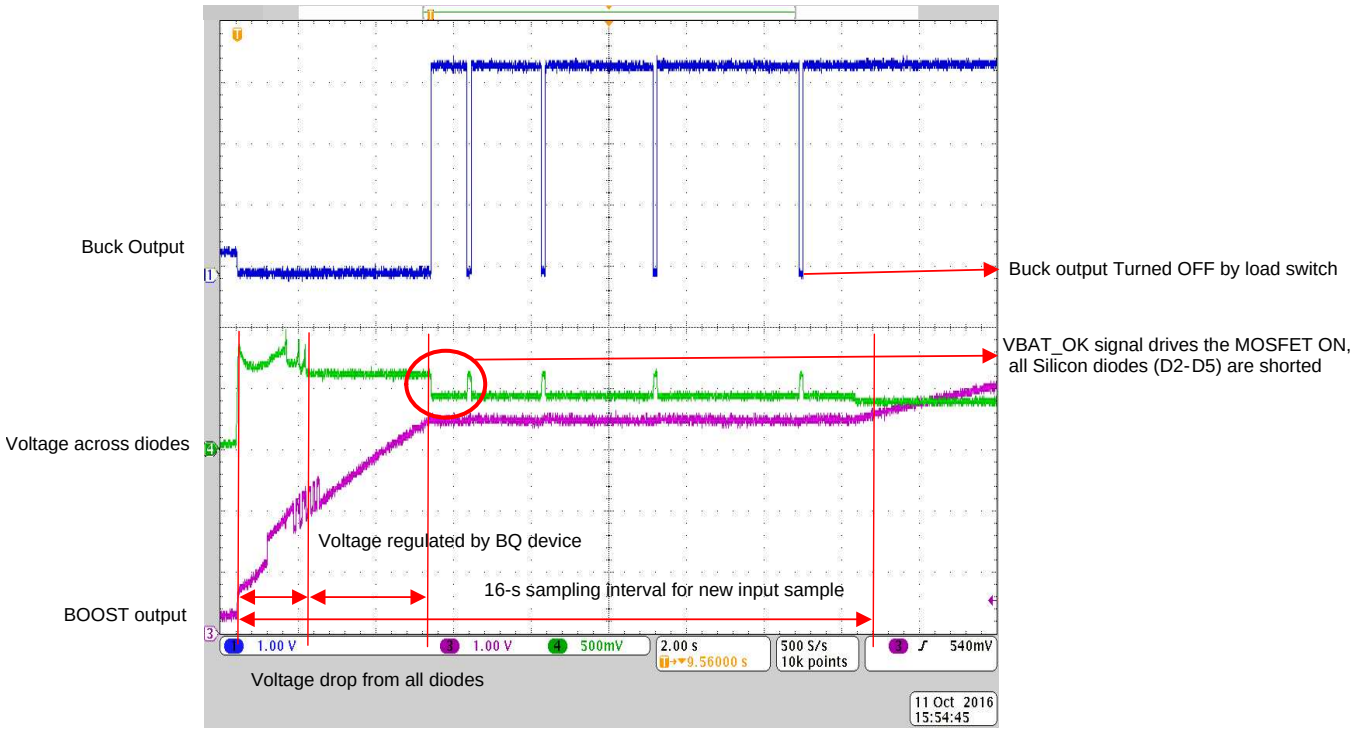


Figure 29. Working of N-Channel MOSFET

3.7 Test 7: 10-kHz Active Low-Pass Filter

The 10-kHz active low-pass filter is designed to provide an inverted output. The first test is to perform the AC analysis to confirm the cutoff frequency and the phase difference. The customer has to perform the offset error analysis to calibrate the system. Figure 30 shows the connections for the test.

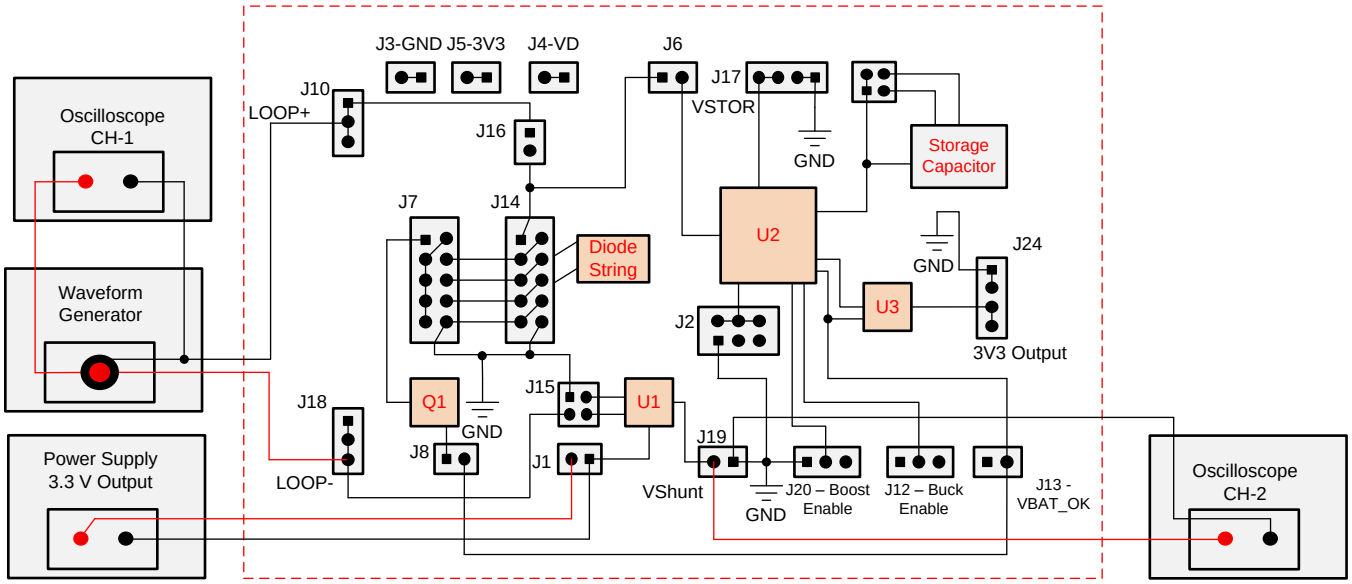


Figure 30. Frequency Analysis Test Configuration for Active Low-Pass Filter

Requirements:

- Source measurement unit
- Keysight B2900A Quick measurement software (used during test)
- Oscilloscope with four channels

For the particular test, remove the shunt from header J6 to disconnect the BQ25570 device from the loop. Short all the diodes by placing shunts in header J14. Connect the oscilloscope channel 1 to the waveform output for reference. Connect the output of the op amp on pin 2 of header J19 to the oscilloscope. Connect the ground to pin 1 of the header. Because the BQ25570 is disconnected from the loop, the op amp must be powered from an external source. Connect the positive terminal to J1 (pin 1) and the ground to J19 (pin 1) . Set the output of the power supply to 3.3 V.

On the waveform generator, set the amplitude as 10.00 mV_{P-P}. Set the offset as –400 µV because the positive of the waveform generator is to be connected to the LOOP–. On the oscilloscope, compare the output on the two connected channels. Set the formulae to compare the phase between the output and input waveform. Measure the peak-to-peak amplitude of the waveforms. The output should have a gain of 10. Increment the input frequency and make a note of the change in phase and amplitude. The graphs in Figure 31 and Figure 32 show the results.

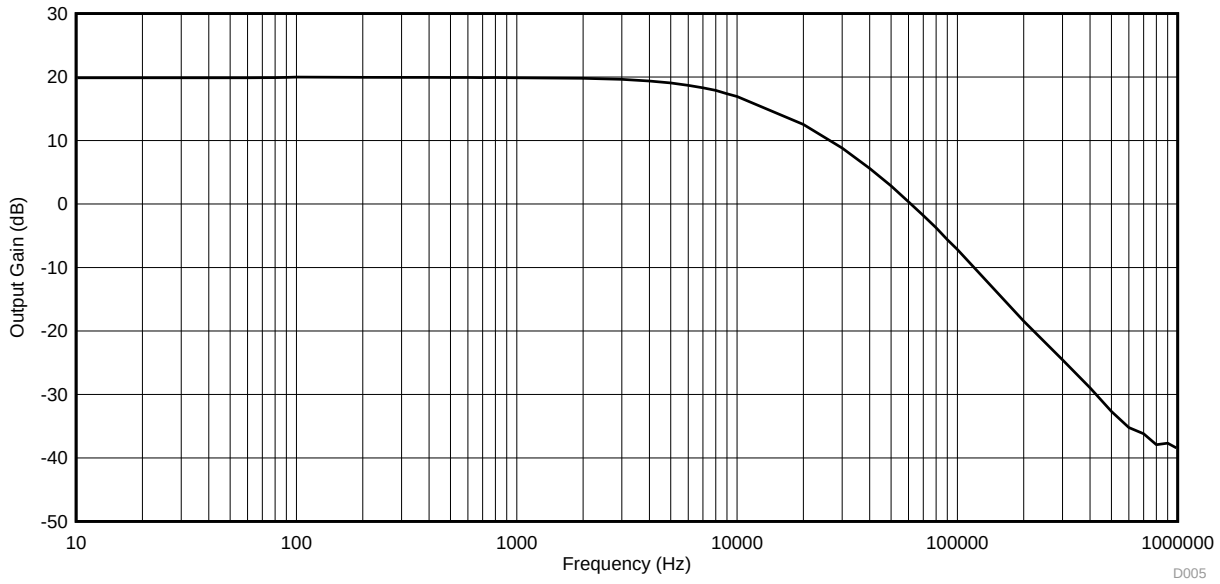


Figure 31. AC Transfer Characteristics of 10-kHz Filter

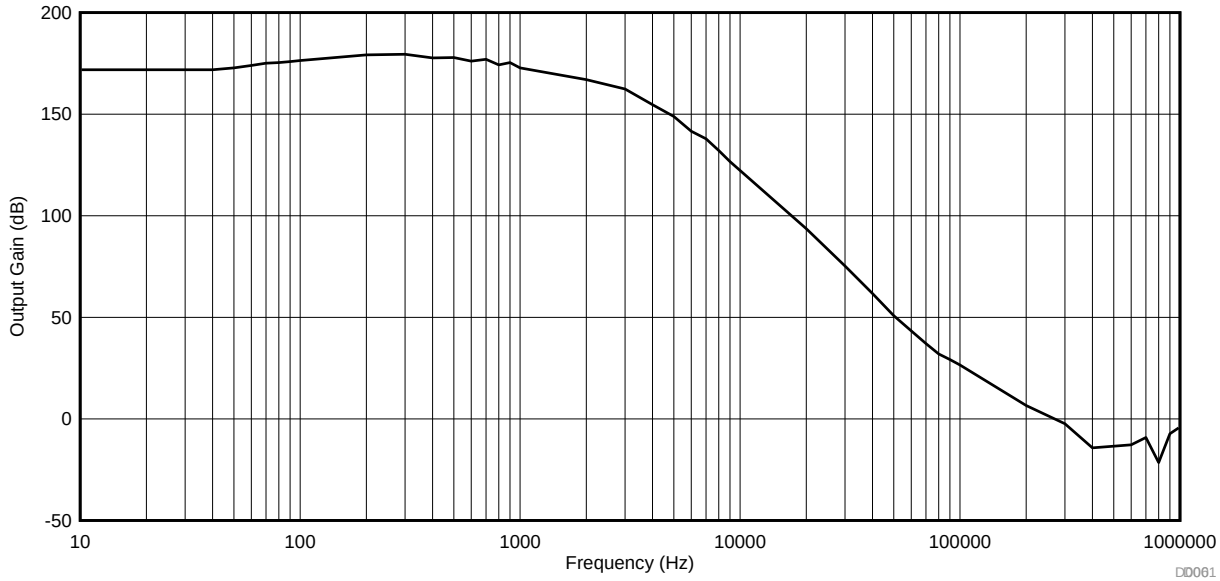


Figure 32. Phase Analysis of 10-kHz Active Filter

The next test regarding the active filter is the output gain at different input currents. The SMU is used as a source to provide input current. The input current is varied from 4 mA to 20 mA and the output is measured. The op amp is powered from the output of the buck converter. Place a shunt on header J1 to power the op amp. Place shunts across pins 1 through 2 and 3 through 4 on header J15 to connect the active filter to the low-side shunt resistor.

Requirements:

- Source measurement unit
- Keysight B2900A Quick measurement software (used during test)
- Oscilloscope with four channels

Channel 1:

- Source: current source
- Current output: 4-mA to 20-mA step increment
- Compliance voltage: 5 V
- Four-wire system
- Termination: floating

A HART communication system is commonly used in 4-mA to 20-mA loop systems. Measuring the HART signals is mandatory. For this test, a HART-enabled sensor transmitter and a HART modulator is used. The oscilloscope image on Figure 33 shows the output of the 10-kHz low-pass filter.

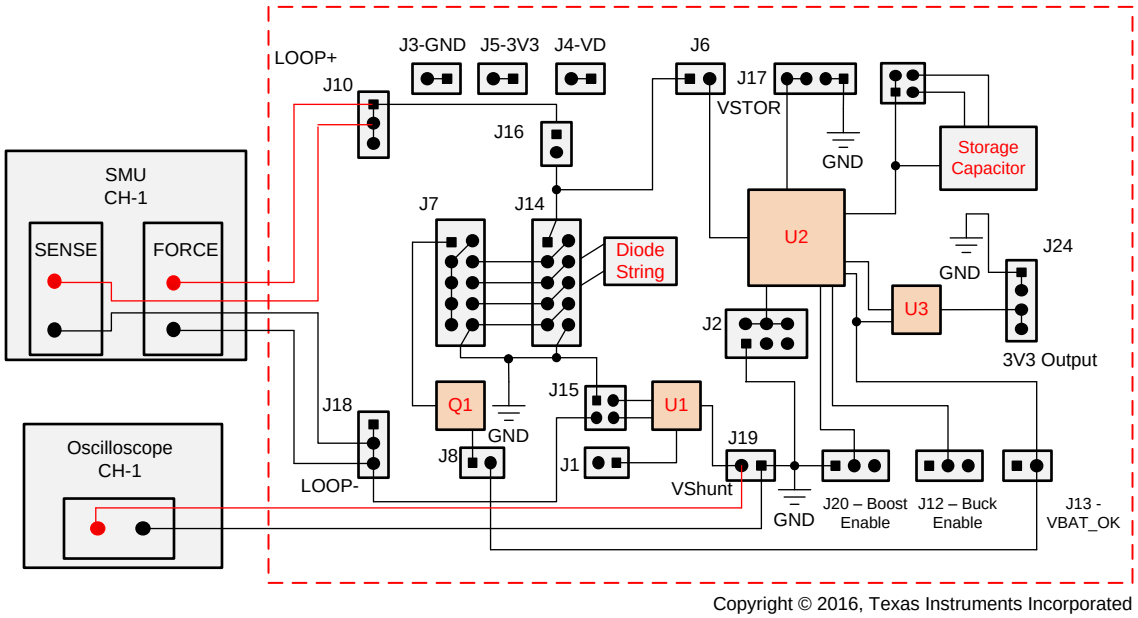
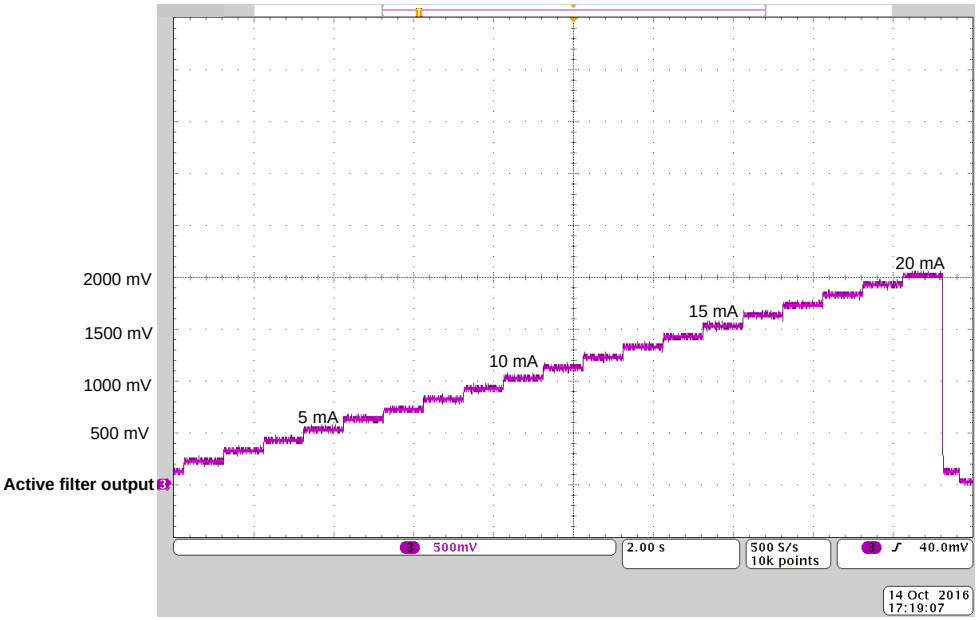


Figure 33. Loop Current Measurement Test Configuration



Parameters:

Shunt resister = 10 Ω
Gain = 10

Calculation: (Expected output at 5 mA)

V_{OUT} = 10 Ω x 0.005 A
= **0.05 V**
(at gain of 10)
V_{OUT} = **500 mV**

Figure 34. Loop Current Measurement Output

Requirements:

- HART modulator
- HART-enabled sensor transmitter
- Oscilloscope with four channels
- 24-V power supply

Figure 35shows an example connection. The HART modulator is used for digital communication over the loop current.

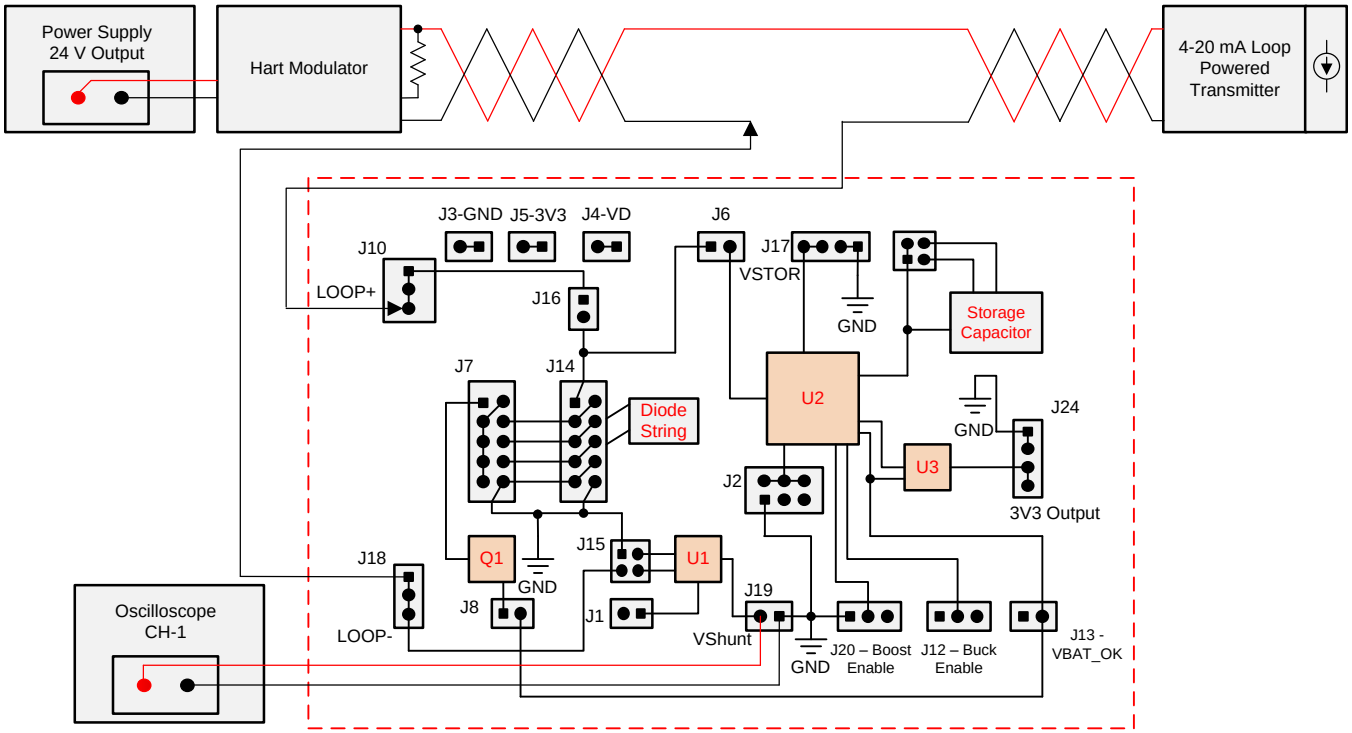


Figure 35. HART Signal Measurement Test Configuration

The 24-V power supply should be connected to the HART modulator. The 250-Ω termination resistor should be connected if it is not already connected internally. Connect the output of the HART modulator to the sensor transmitter loop terminals. Connect the energy harvester board LOOP+ to the ground of the sensor transmitter and the LOOP– to the HART modulator ground terminal.

The current through the loop with the HART modulation can be measured through the active low-pass filter. To view the HART modulation, connect the probes of the oscilloscope to the output of the active low-pass filter. Set an offset on the channel measured to see the 1-mA peak-to-peak signal in detail. The current through the loop should be set as the offset.

For this particular test, a temperature sensor transmitter was used. A resistor was connected to the sense pins to replicate a resistance-temperature detector (RTD). The value of the resistors for current outputs can be downloaded from the Internet. The HART modulates at two frequencies: 1200 kHz (ones) and 2200 kHz (zeros), which is visible in the oscilloscope output in Figure 36.

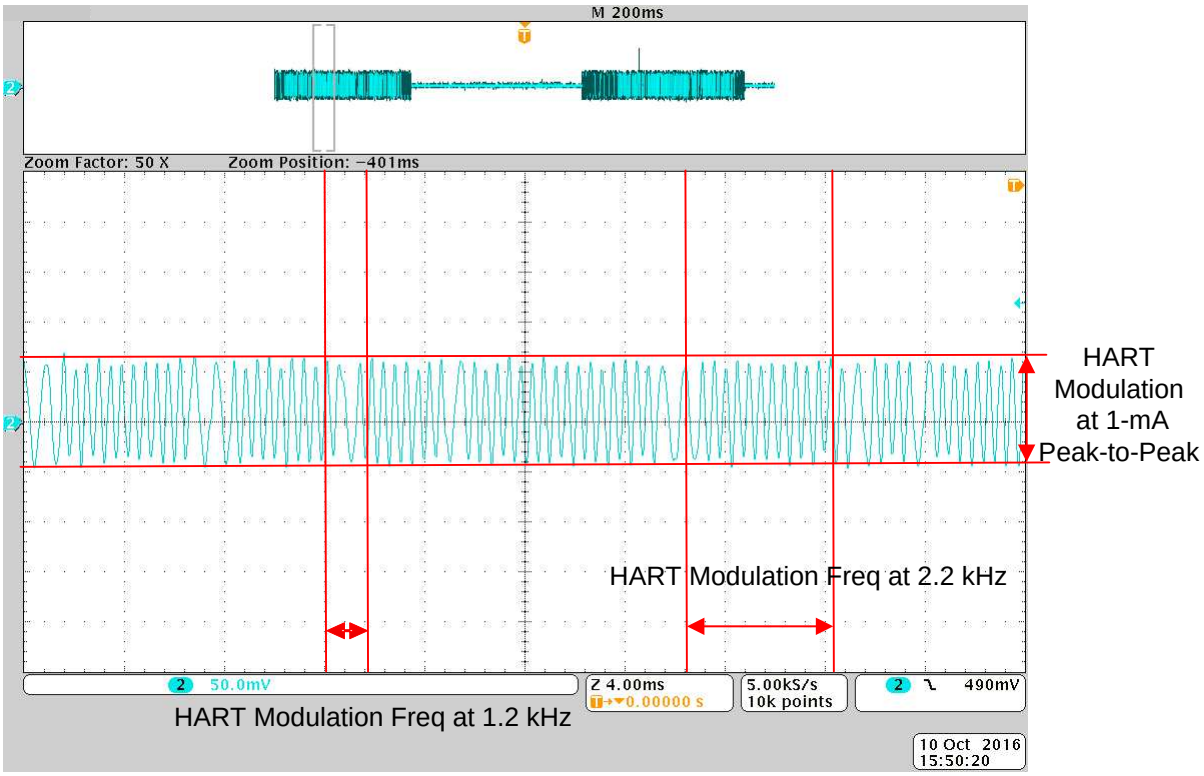


Figure 36. HART Signal Measurement Output

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00649.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00649.

4.3 PCB Layout Recommendations

As with all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger and buck converter can show stability problems as well as electromagnetic interference (EMI) problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors must be placed as close as possible to the integrated circuit (IC).

For the boost charger, the first priority is the output capacitors, including the 0.1-uF bypass capacitor (CBYP), followed by CSTOR, which is to be placed as close as possible between VSTOR, pin 19, and VSS (pin 1). Next, the input capacitor, C_{IN}, must be placed as close as possible between V_{IN_DC} (pin 2) and V_{SS} (pin 1). The last priority is the boost charger inductor, L1, which must be placed close to LBOOST (pin 20) and V_{IN_DC} (pin 2). For the buck converter, the output capacitor C_{OUT} must be placed as close as possible between V_{OUT} (pin 14) and V_{SS} (pin 15). The buck converter inductor (L2) must be placed as close as possible between the switching node L_{BUCK} (pin 16) and V_{OUT} (pin 14). Using vias and bottom traces is best practice for connecting the inductors to their respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, OK_HYST, VOUT_SET), the external resistors must be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (for example, from resistors and C_{REF}), TI recommends to use short traces as well, separated from the power ground traces and connected to V_{SS} pin 15. This action avoids ground shift problems, which can occur as a result of superimposition of power ground current and control ground current. The TI PowerPAD® integrated circuit package must not be used as a power ground return path. The remaining pins are either NC pins, that should be connected to the PowerPAD as Figure 37 shows, or digital signals with minimal layout restrictions.

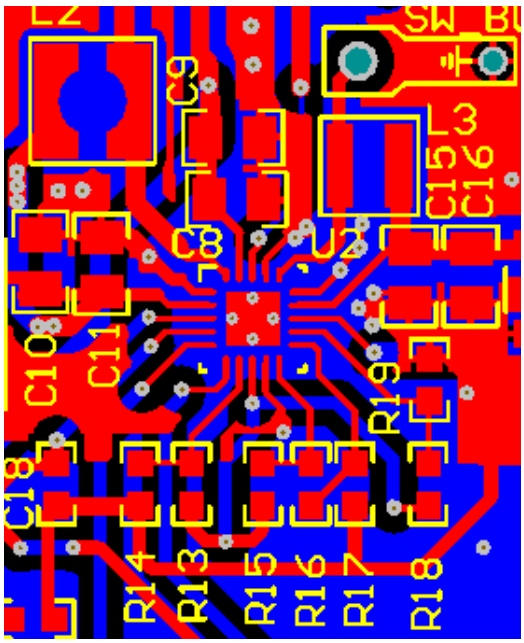


Figure 37. Layout Recommendation of bq25570 IC

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00649.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00649.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00649.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00649.

5 Related Documentation

1. Texas Instruments, *Harnessing wasted energy in 4- to 20-mA current-loop systems*, Application Note (SLYT488)
2. Texas Instruments, *User's Guide for BQ25570 Battery Charger Evaluation Module for Energy Harvesting*, User's Guide (SLUUAA7)

5.1 Trademarks

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6 About the Author

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• Changed Figure 37 caption to highlight bq25570 instead of bq27750	38

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