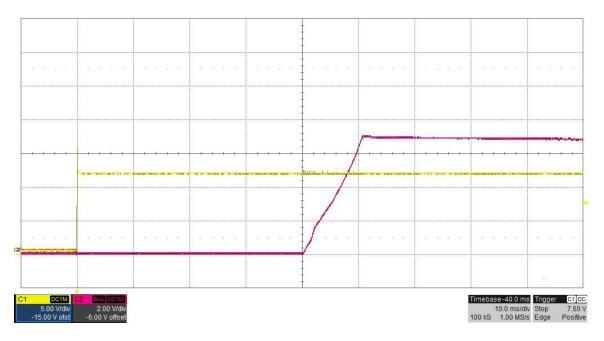
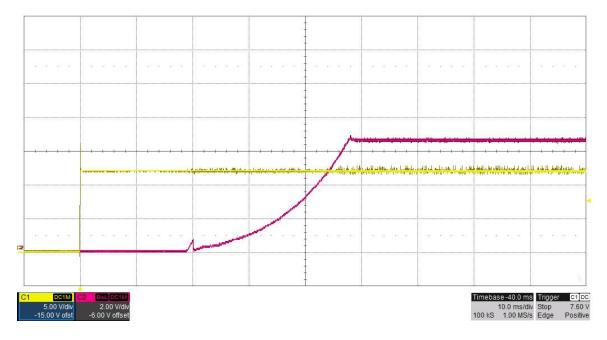


1 Startup

The photo below shows the 6.5V output voltage startup waveform (RED) after the application of 12V in (Yellow) with the output loaded to 0A. (Vin is 5V/DIV, Vout is 2V/DIV, 10mS/DIV)



The photo below shows the 6.5V output voltage startup waveform (RED) after the application of 12V in (Yellow) with the output loaded to 2.5A. (Vin is 5V/DIV, Vout is 2V/DIV, 10mS/DIV)

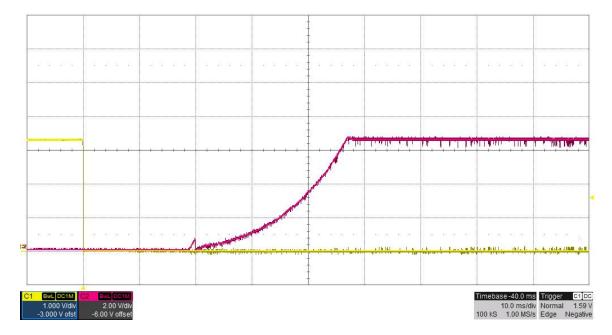




The photo below shows the 6.5V output voltage startup waveform (RED) after the /ENABLE signal (Yellow) is pulled low. Vin is 12V and the output is loaded to 0A. (/ENABLE is 1V/DIV, Vout is 2V/DIV, 10mS/DIV)



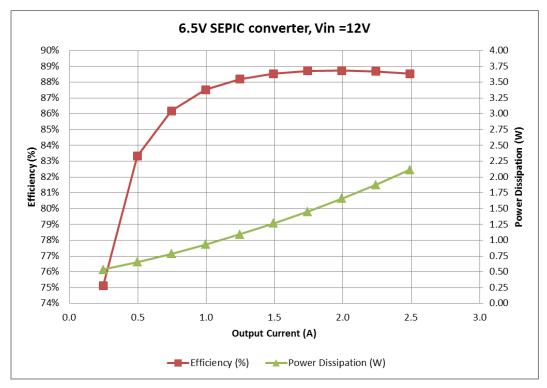
The photo below shows the 6.5V output voltage startup waveform (RED) after the /ENABLE signal (Yellow) is pulled low. Vin is 12V and the output is loaded to 2.5A. (/ENABLE is 1V/DIV, Vout is 2V/DIV, 10mS/DIV)

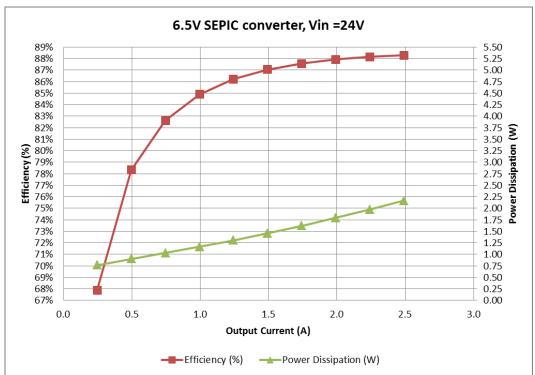




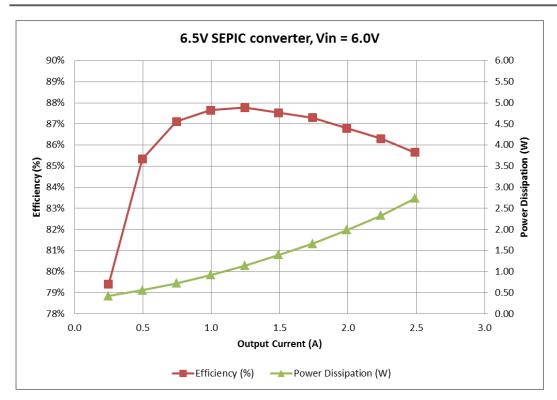
2 Efficiency

The converter efficiency is shown in the figure below.





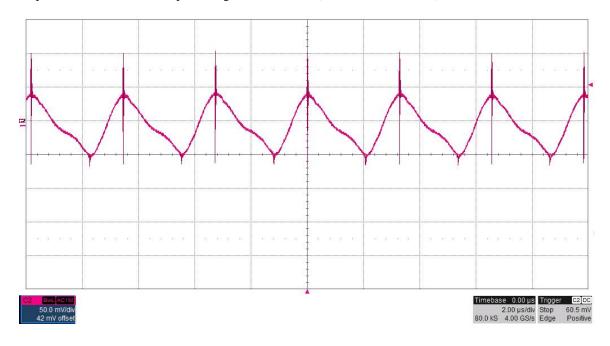




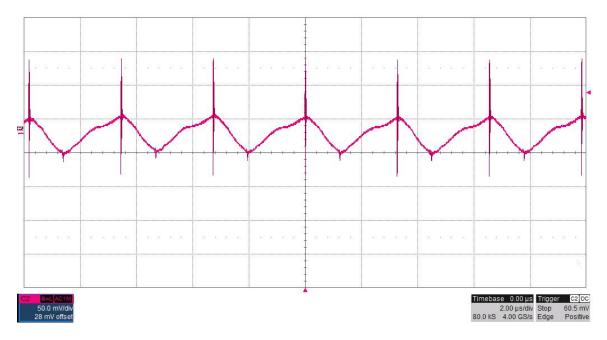


3 Output Ripple Voltage

The 6.5V output ripple voltage (ac coupled) is shown in the figure below. The image was taken with the output loaded to 2.5A. The input voltage is set to 4.5V. (50mV/DIV, 2uS/DIV)

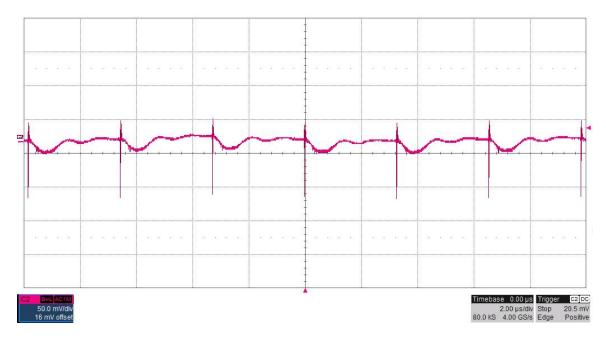


The 6.5V output ripple voltage (ac coupled) is shown in the figure below. The image was taken with the output loaded to 2.5A. The input voltage is set to 12V. (50mV/DIV, 2uS/DIV)





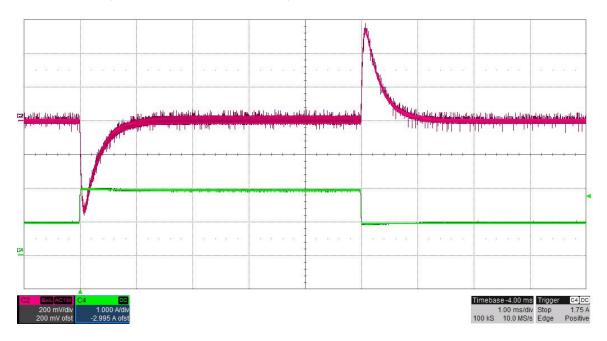
The 6.5V output ripple voltage (ac coupled) is shown in the figure below. The image was taken with the output loaded to 2.5A. The input voltage is set to 60V. (50mV/DIV, 2uS/DIV)



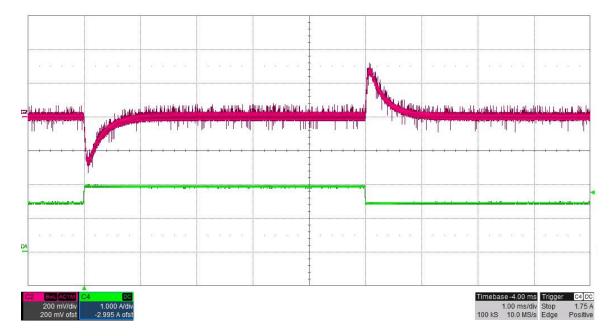


4 Load Transients

The photo below shows the output voltage (ac coupled) when the load current is stepped between 1A and 2A. Vin = 12V. (200mV/DIV, 1A/DIV, 1mS/DIV)



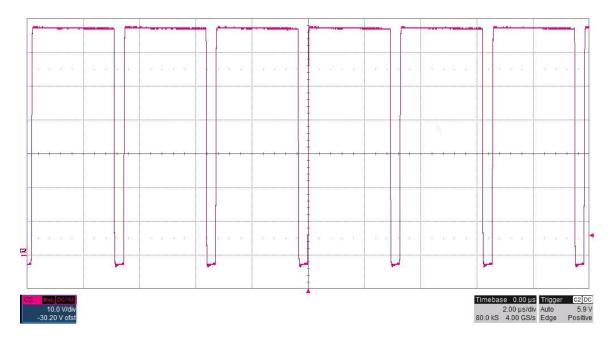
The photo below shows the output voltage (ac coupled) when the load current is stepped between 1.5A and 2A. Vin = 12V. (200mV/DIV, 1A/DIV, 1mS/DIV)



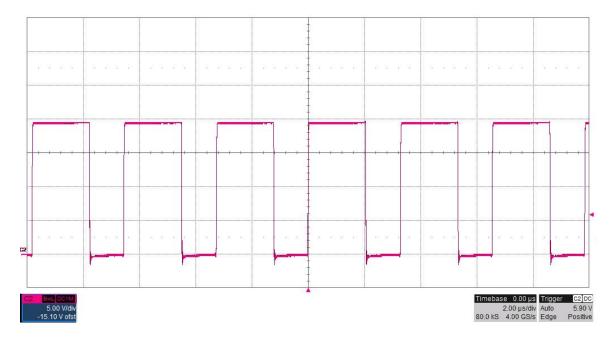


5 Switch Node Waveforms

The photo below shows the SEPIC switch node voltage at TP4. The input voltage is 60V and the output is $6.5V \otimes 2.5A$. (10V/DIV, 2uS/DIV)

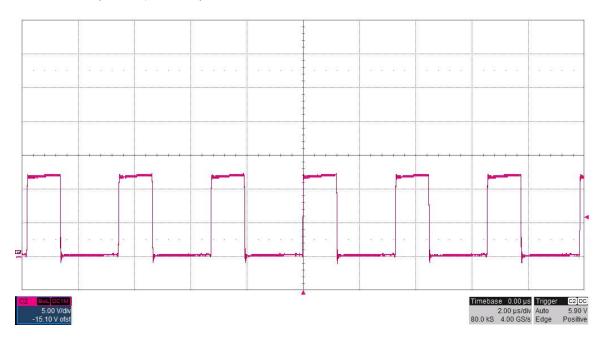


The photo below shows the SEPIC switch node voltage at TP4. The input voltage is 12V and the output is 6.5V @ 2.5A. (5V/DIV, 2uS/DIV)

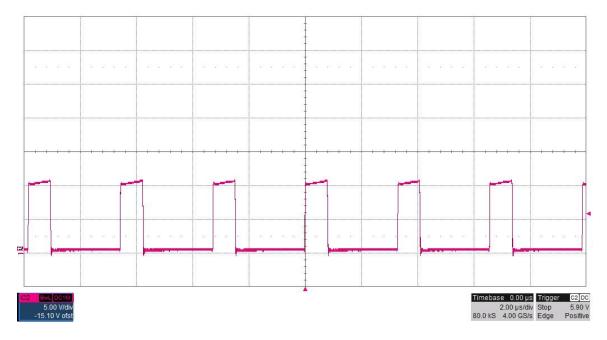




The photo below shows the SEPIC switch node voltage at TP4. The input voltage is 4.5V and the output is 6.5V @ 2.5A. (5V/DIV, 2uS/DIV)



The photo below shows the SEPIC switch node voltage at TP4. The input voltage is 3.0V and the output is 6.5V @ 2.5A. (5V/DIV, 2uS/DIV)

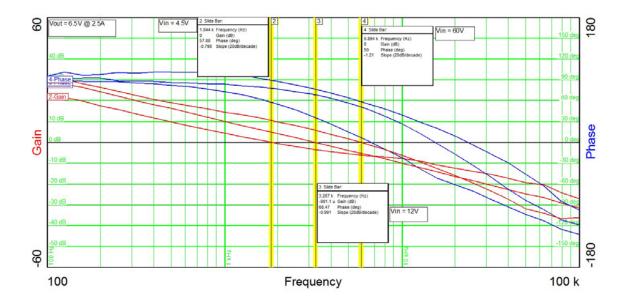




6 Control Loop Gain / Stability

The plot below shows the 6.5V loop gain and phase margin with the output loaded to 2.5A. The input voltage was set to 60V, 12V and 4.5V.

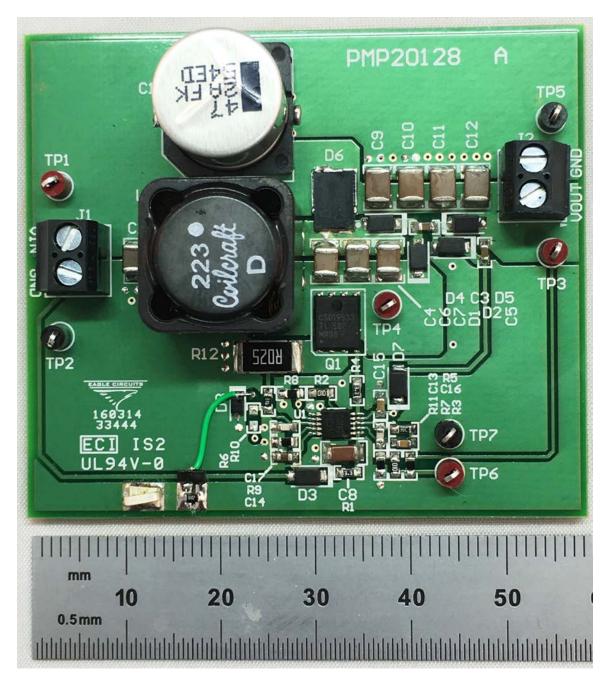
Band Width = 5.89 KHz, Phase Margin = 59 degrees (Vin = 60V) Band Width = 3.27 KHz, Phase Margin = 68 degrees (Vin = 12V) Band Width = 1.84 KHz, Phase Margin = 58 degrees (Vin = 4.5V)





7 Photo

The photo below shows the PMP20128 REVB assembly. The /ENABLE circuit modification is in the lower left.





8 Thermal Image

A thermal image is shown below with the SEPIC converter operating at 12V input and a $6.5V \otimes 2.5A$ output, with no airflow.



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