CMOS Power Consumption and C_{pd} Calculation

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Introduction

Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS devices are best known for low power consumption. However, for minimizing the power requirements of a board or a system, simply knowing that CMOS devices may use less power than equivalent devices from other technologies does not help much. It is important to know not only how to calculate power consumption, but also to understand how factors such as input voltage level, input rise time, power-dissipation capacitance, and output loading affect the power consumption of a device. This application report addresses the different types of power consumption in a CMOS logic circuit, focusing on calculation of power-dissipation capacitance (C_{pd}), and, finally, the determination of total power consumption in a CMOS device.

The main topics discussed are:
- Power-consumption components
- Static power consumption
- Dynamic power consumption
- Power-dissipation capacitance (C_{pd}) in CMOS circuits
- C_{pd} comparison among different families
- Power economy
- Conclusion

Power-Consumption Components

High frequencies impose a strict limit on power consumption in computer systems as a whole. Therefore, power consumption of each device on the board should be minimized. Power calculations determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculations also can determine the maximum reliable operating frequency.

Two components determine the power consumption in a CMOS circuit:
- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

This application report addresses power consumption in CMOS logic families (5 V and 3.3 V) and describes the methods for evaluating both static and dynamic power consumption. Additional information is also presented to help explain the causes of power consumption, and present possible solutions to minimize power consumption in a CMOS system.

Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1.
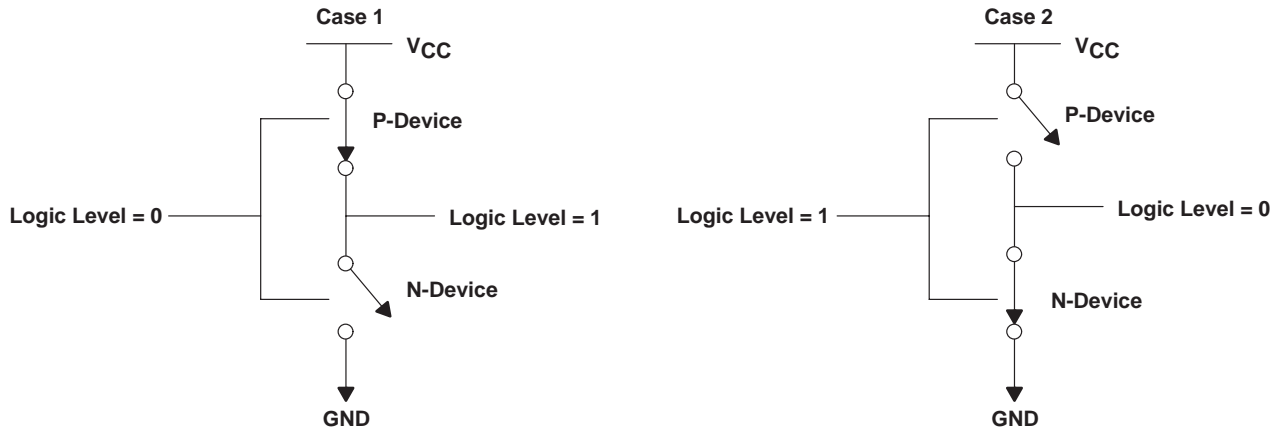
Figure 1. CMOS Inverter Mode for Static Power Consumption

As shown in Figure 1, if the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is V_{CC}, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from V_{CC} to GND, the resultant quiescent (steady-state) current is zero, hence, static power consumption (P_q) is zero.

However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Figure 2.
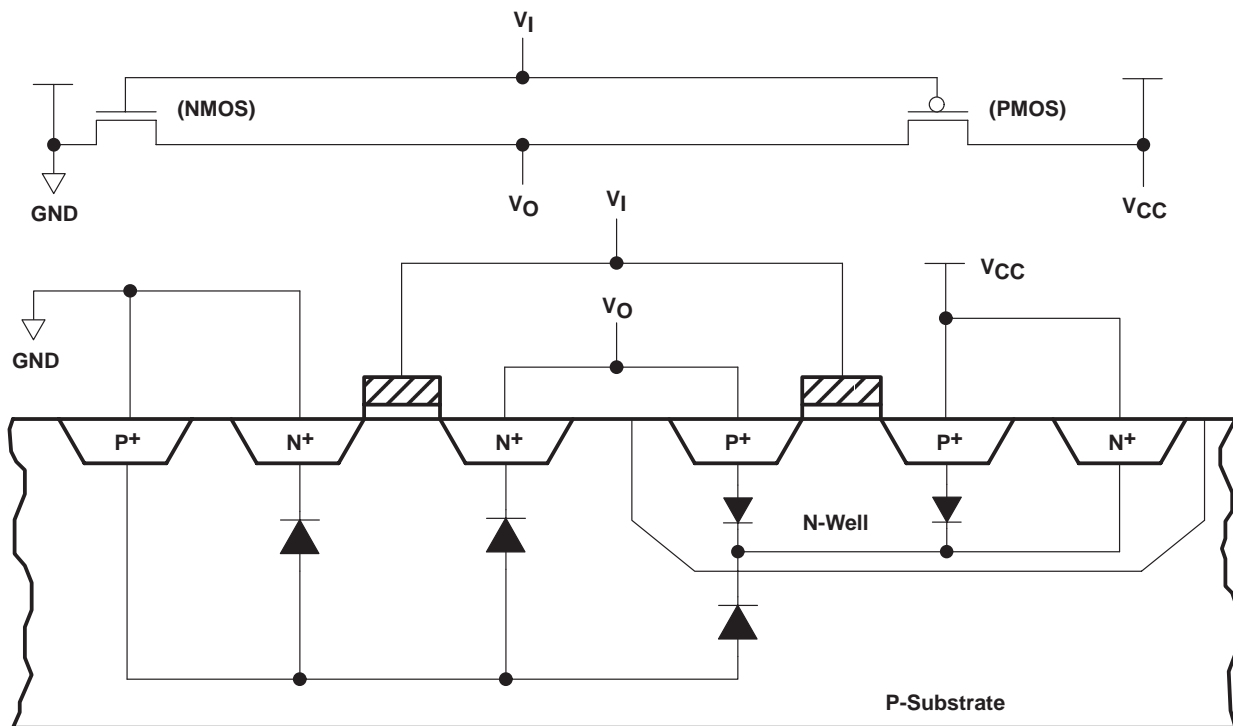

Figure 2. Model Describing Parasitic Diodes Present in CMOS Inverter

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The source drain diffusion and N-well diffusion form parasitic diodes. In Figure 2, the parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption. The leakage current (I_{lkg})of the diode is described by the following equation:

$$I_{lkg} = i_s(e^{qV/kT} - 1) \tag{1}$$

Where:

i_s = reverse saturation current
V = diode voltage
k = Boltzmann's constant (1.38×10^{-23} J/K)
q = electronic charge (1.602×10^{-19} C)
T = temperature

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation 2.

$$P_S = \Sigma \text{ (leakage current)} \times \text{(supply voltage)} \tag{2}$$

Most CMOS data sheets specify an I_{CC} maximum in the 10-μA to 40-μA range, encompassing total leakage current and other circuit features that may require some static current not considered in the simple inverter model.

The leakage current I_{CC} (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or P_S, and can be calculated by equation 3.

$$P_S = V_{CC} \times I_{CC} \tag{3}$$

Where:

V_{CC} = supply voltage
I_{CC} = current into a device (sum of leakage currents as in equation 2)

Another source of static current is ΔI_{CC}. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

Dynamic Power Consumption

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (P_T), and capacitive-load power consumption (P_L).

Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (*switching current*) plus the *through current* (current that flows from V_{CC} to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.

Transient power consumption can be calculated using equation 4.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{SW}$$

(4)

Where:

P_T = transient power consumption
V_{CC} = supply voltage
f_I = input signal frequency
N_{SW} = number of bits switching
C_{pd} = dynamic power-dissipation capacitance

In the case of single-bit switching, N_{SW} in equation 4 is 1.

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance (C_{pd}) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. C_{pd} is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, C_{pd} can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). C_{pd} is discussed in greater detail in the next section.

Capacitive-Load Power Consumption

Additional power is consumed in charging external load capacitance and is dependent on switching frequency. The following equation can be used to calculate this power if all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{SW} \quad (C_L \text{ is the load per output})$$

(5)

Where:

P_L = capacitive-load power consumption
V_{CC} = supply voltage
f_O = output signal frequency
C_L = external (load) capacitance
N_{SW} = total number of outputs switching

In the case of different loads and different output frequencies at all outputs, equation 6 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2$$

(6)

Where:

Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output, numbered 1 through n (Hz)
V_{CC} = supply voltage (V)
C_{Ln} = all different load capacitances at each output, numbered 1 through n.

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions and can be expressed as shown in equation 7, equation 8 (single-bit switching), and equation 9 (multiple-bit switching with variable load and variable output frequencies).

$$P_D = P_T + P_L \tag{7}$$

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2 \right) + \left(C_L \times f_O \times V_{CC}^2 \right) \tag{8}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW} \right) + \Sigma(C_{Ln} \times f_{On}) \right] \times V_{CC}^2 \tag{9}$$

Where:

C_{pd} = power-consumption capacitance (F)
f_I = input frequency (Hz)
f_{On} = all different output frequencies at each output, numbered 1 through n (Hz)
N_{SW} = total number of outputs switching
V_{CC} = supply voltage (V)
C_{Ln} = all different load capacitances at each output, numbered 1 through n.

Total power consumption is the sum of static and dynamic power consumption.

$$P_{tot} = P_{(static)} + P_{(dynamic)} \tag{10}$$

Power-Dissipation Capacitance (C_{pd}) in CMOS Circuits

C_{pd} is an important parameter in determining dynamic power consumption in CMOS circuits. It includes both internal parasitic capacitance (e.g., gate-to-source and gate-to-drain capacitance) and *through currents* present while a device is switching and both n-channel and p-channel transistors are momentarily conducting.

Testing Considerations

Proper setup is vital to achieving proper correlation. Some of the more important issues in performing the measurement are discussed in this section.

Input Edge Rates

When measuring C_{pd}, the input edge rate should be $t_r = t_f = 1$ ns from 10% to 90% of the input signal. Power-dissipation capacitance is heavily dependent on the dynamic supply current, which, in turn, is sensitive to input edge rates. As previously noted, while an input is switching, there is a brief period when both p-channel and n-channel transistors are conducting, which allows *through current* to flow from V_{CC} to GND through the input stage. The amount of dynamic *through current* measured is directly proportional to the amount of time the input signal is at some level other than V_{CC} or GND.

Bypassing

Any circuit must be properly bypassed to function correctly at high frequencies. The bypass capacitor between V_{CC} and GND serves to reduce power-supply ripple and provides a more accurate measure of the current being drawn by the device under test. Improper bypassing can result in erratic voltage at the V_{CC} pin and can disrupt the test. Texas Instruments (TI) uses a 0.1-µF bypass capacitor (from V_{CC} to GND) on the test board.

Pin Combination

Different pin combinations are valid and may be chosen to best suit the application at hand. For example, it is valid to test a device with the outputs either enabled or disabled. For multisection devices, set the device so that the minimum number of sections is active. Virtually any pin combination that causes at least one output to switch at a known frequency is acceptable.

Test Conditions

The test conditions for C_{pd} calculation for any device requires the following information (an LVC device is used as an example):

V_{CC}	5 V
Ambient temperature, T_A	25°C
AC bias levels	0 V, 3.3 V
DC bias level	0 V, 3.3 V
Input edge rates	$t_r = t_f = 1$ ns (smallest possible)
Input frequencies	0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz
C_{pd} frequency	10 MHz
Duty cycle	50%

Similarly, the test conditions for I_{CC} versus frequency are also applicable to determine the C_{pd} for CMOS devices. An AHC00 device is considered as an example for test conditions to calculate C_{pd} through I_{CC} versus frequency data and using the C_{pd} equation described in the next section (*Calculating C_{pd}*).

V_{CC}	5 V
Ambient temperature, T_A	25°C
AC bias levels	0 V, 5V
DC bias level	5 V
Input edge rates	$t_r = t_f = 2$ ns (smallest possible)
Input frequencies	0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz
Duty cycle	50%

For nontransceiver devices with 3-state outputs, testing is performed with the outputs enabled and disabled. When disabled, pullup resistors are not required. For a transceiver with 3-state outputs, testing also is performed with outputs enabled and disabled. However, in the disabled mode, 10-kΩ pullup resistors to the V_{CC} power supply or to GND must be added to all inputs and outputs.

Calculating C_{pd}

C_{pd} is calculated by putting the device in the proper state of operation and measuring the dynamic I_{CC} using a true RMS multimeter. Testing is done at an input frequency of 1 MHz to reduce the contribution of the dc supply current to the point that it can be ignored. Measurements for all devices are made at $V_{CC} = 5$ V or 3.3 V, $T_A = 25$°C. The test frequency must be low enough to allow the outputs to switch from rail to rail. For this reason, devices with 3-state outputs are measured at 10 MHz.

C_{pd} Measurement Procedures

For devices that have several gates in the same package (for example, AHC04 has six individual inverter circuits as shown in Figure 3), the average C_{pd} per output is specified in the data sheet as a typical (TYP) value.
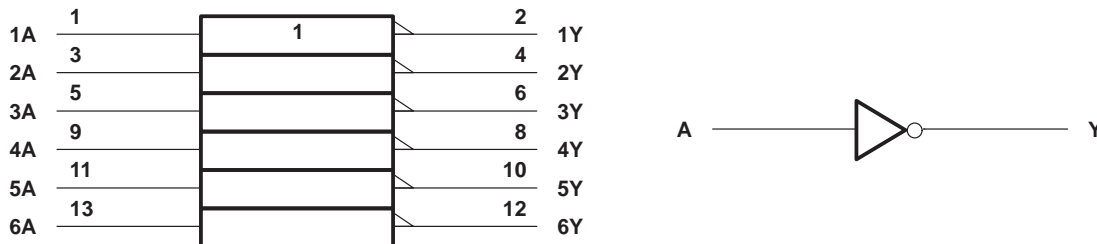

Figure 3. Hex Inverter AHC04

For devices that have several circuits switching simultaneously from a single clock or input (such as the AHC374 in Figure 4), switch all outputs and deduct P_L for each output. In the case of multiple-output switching at different frequencies (i.e., divide counters with parallel outputs) each P_L will have a different frequency factor.
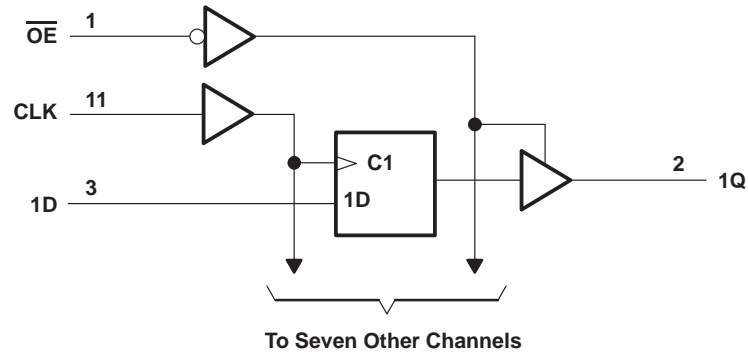
Figure 4. Several Circuits Switching, AHC374

In the case of devices such as ALVC, LVC, and LV, test and calculate C_{pd} for both the enable and disable mode. Typically, C_{pd} in the enable mode is greater than C_{pd} in the disable mode ($C_{pd\_EN} > C_{pd\_DIS}$).

Determination of C_{pd} (Laboratory Testing)

In the laboratory, determine C_{pd} for any device, such as AHC00, by measuring the I_{CC} being supplied to the device under the conditions in the *Test Conditions* section. Figure 5 provides the I_{CC} and frequency data for the AHC00 that can be used to calculate C_{pd} for the device, using equation 6 with a no-load condition.
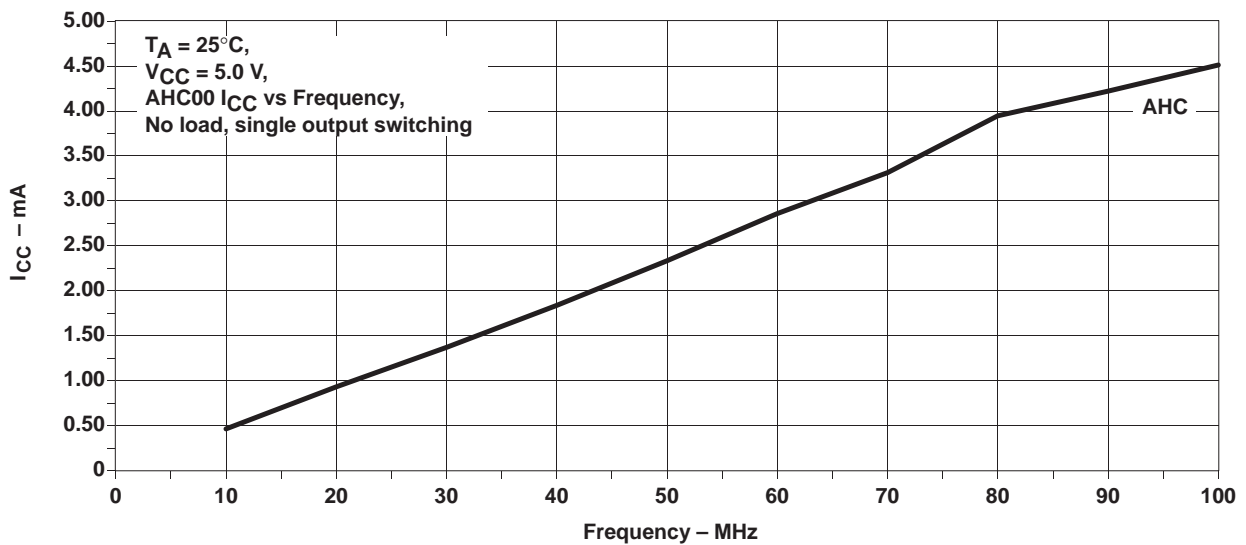

Figure 5. I_{CC} vs Frequency for AHC00

Note that the total capacitance for the switching output must be measured under open-socket conditions for accurate calculations. Considering these conditions, the data sheet C_{pd} is calculated using equation 11. Due to the automatic test-equipment constraints, C_{pd} is not assigned a maximum value in the data sheet.

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \tag{11}$$

Where:

f_I = input frequency (Hz)
V_{CC} = supply voltage (V)
$C_{L(eff)}$ = effective load capacitance on the board (F)
I_{CC} = measured value of current into the device (A)

The effective load capacitance is calculated according to equation 12 (assuming C_L is equal in all outputs).

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I}$$

(12)

Where:

f_O/f_I = ratio of output and input frequency (Hz)
N_{SW} = number of bits switching
C_L = load capacitance (F)

To explain the C_{pd} and the method of calculating dynamic power, see Table 1, which gives the C_{pd} test conditions for AHC devices. The symbols used in Table 1 for C_{pd} of AHC devices are:

V = V_{CC} (5 V)
G = ground (GND) (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = irrelevant: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz), (see Figure 6)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 6)
S = standard ac output load (50 pF to GND)

The table shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations 8 and 9.
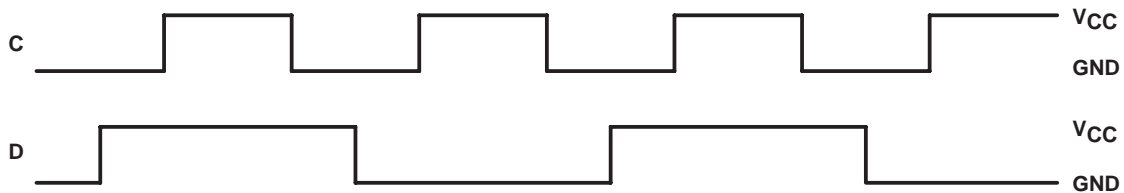

Figure 6. Input Waveform

Table 1. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switchings, but with no active clock signal
‡ All bits switching

Comparison of Supply Current Versus Frequency

C_{pd} and dynamic power consumption can be measured through supply-current-versus-frequency plots. Supply current is critical because it indicates the amount of power consumed by the device. A small value for I_{CC} is desirable because reducing the amount of power consumed yields many benefits. Less power consumed means less heat is generated and the problems of dissipating the heat are reduced. The reliability of a system is also improved, because lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. Figures 7 and 8 illustrate I_{CC} versus frequency data for TI's '245 device in different families for both 5 V and 3.3 V.
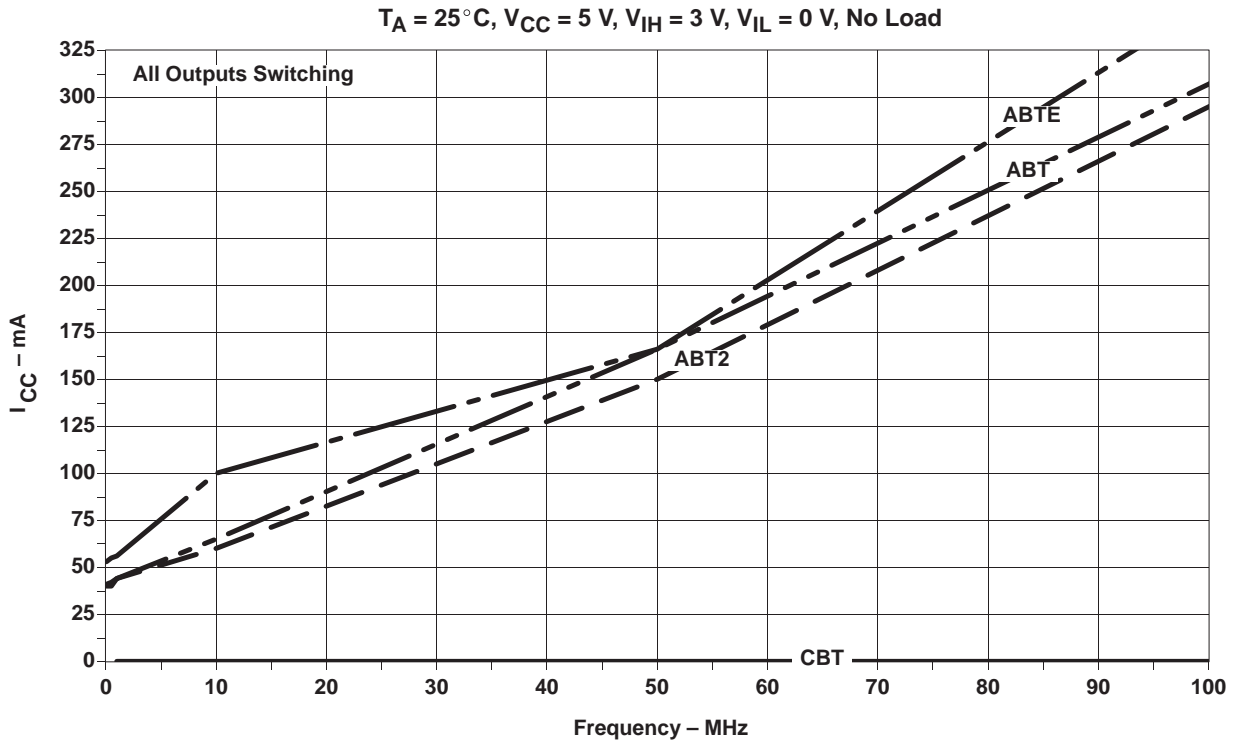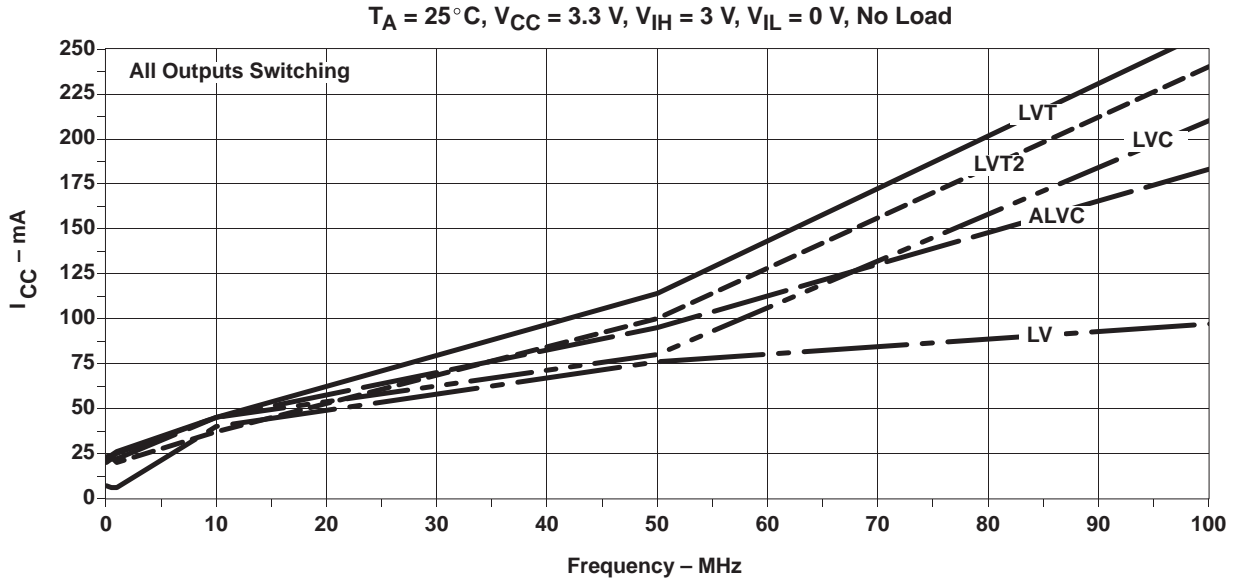
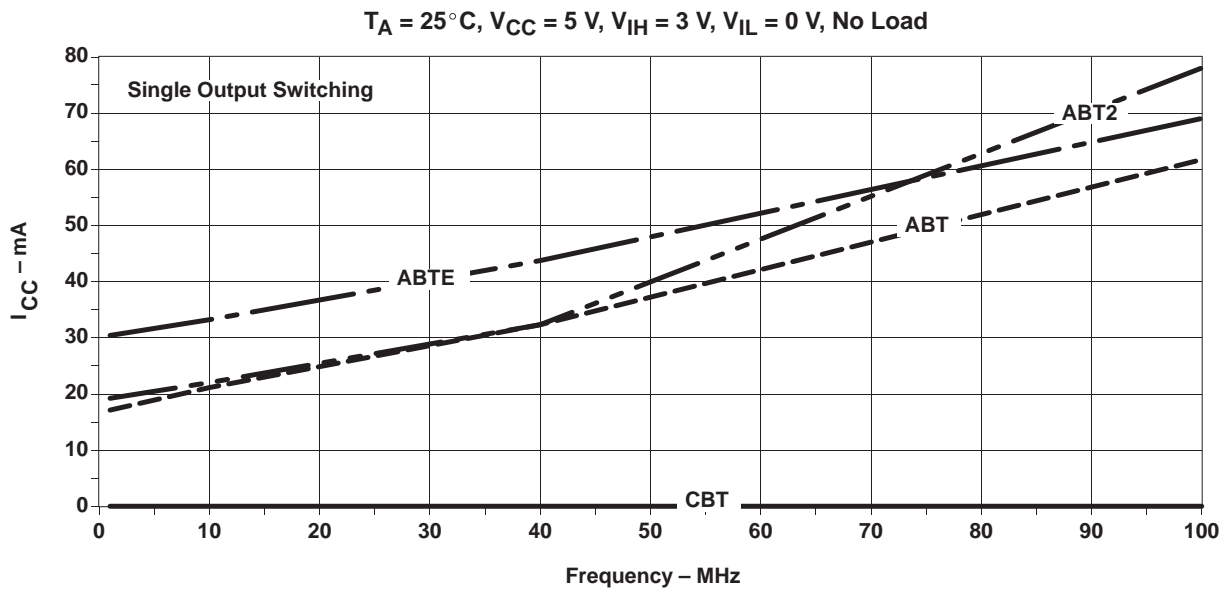**Figure 7. Power Consumption With All Outputs Switching**

$T_A = 25°C$, $V_{CC} = 3.3$ V, $V_{IH} = 3$ V, $V_{IL} = 0$ V, No Load

Single Output Switching

$I_{CC} - mA$

Frequency – MHz

ALVC
LV
LVC
LVT
LVT2

$T_A = 25°C$, $V_{CC} = 5$ V, $V_{IH} = 3$ V, $V_{IL} = 0$ V, No Load

Single Output Switching

$I_{CC} - mA$
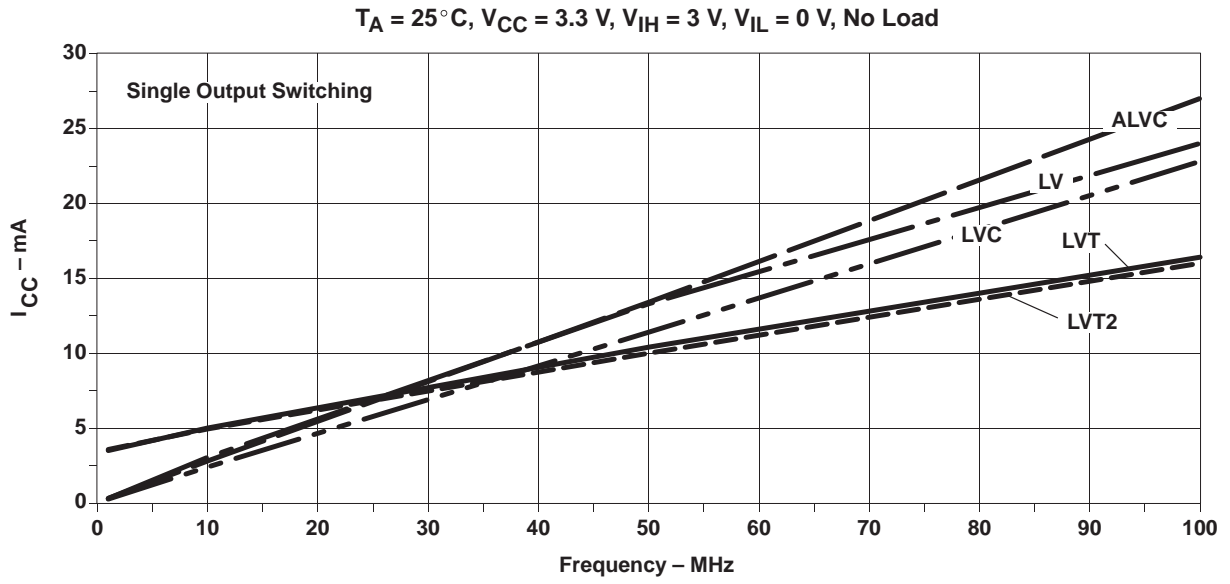
Frequency – MHz

ABT2
ABT
ABTE
CBT

Figure 8. Power Consumption With a Single Output Switching

Power Economy

As noted previously, the industry trend has been to make devices more robust and faster while reducing their size and power consumption. This section describes the rationale and methods used to minimize power consumption in a CMOS circuit. For a CMOS system design, each module is allocated a fixed power budget. This is a power consumption that the module must not exceed. It is important to meet this power consumption allocation constraint, along with other constraints, to achieve a balanced design.

Power consumption minimization can be achieved in a number of ways. The dc power consumption can be reduced to leakage by using only CMOS logic gates, as opposed to bipolar and BiCMOS. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. One of the system design considerations is the choice of low-power devices, with systems today using devices in the 1.5-V to 3.3-V V_{CC} range. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and frequency at which the logic is clocked.

Consider TI's low-power CMOS devices, such as advanced low-voltage CMOS (ALVC) technology as an example. ALVC is the highest-performance 3.3-V bus-interface family. These specially designed 3-V products are processed in 0.6-µm CMOS technology, giving typical propagation delays of less than 3 ns, along with a current drive of 24 mA. This low supply voltage reduces both static and dynamic power consumption for the ALVC family. ALVC also has ultra-low standby power.

Conclusion

Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Acknowledgment