Application Report
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High Speed, Digital to Analog Converters Basics

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ABSTRACT

The goal of this document is to introduce a wide range of theories and topics that are relevant to high-speed, digital-to-analog converters (DAC). This document provides details on sampling theory, data-sheet specifications, common system-level concerns, and the common functions of interpolation DACs such as FIR filters, Digital Mixing and Quadrature Modulator Correction.

Contents

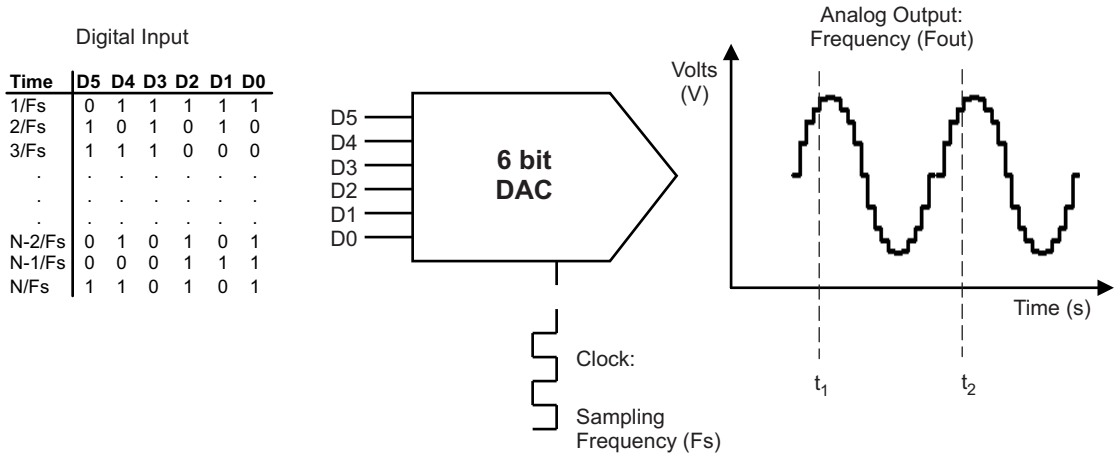
List of Figures

List of Tables

1 Introduction

A Digital to Analog Converter (DAC or D-to-A) is a device that converts digital codes to an analog signal. There are many categories of DACs. Some of these categories include sigma-delta DACs, pulse width modulators, interpolating and high speed DACs. In this paper the focus will be on the interpolating and high speed DACs.

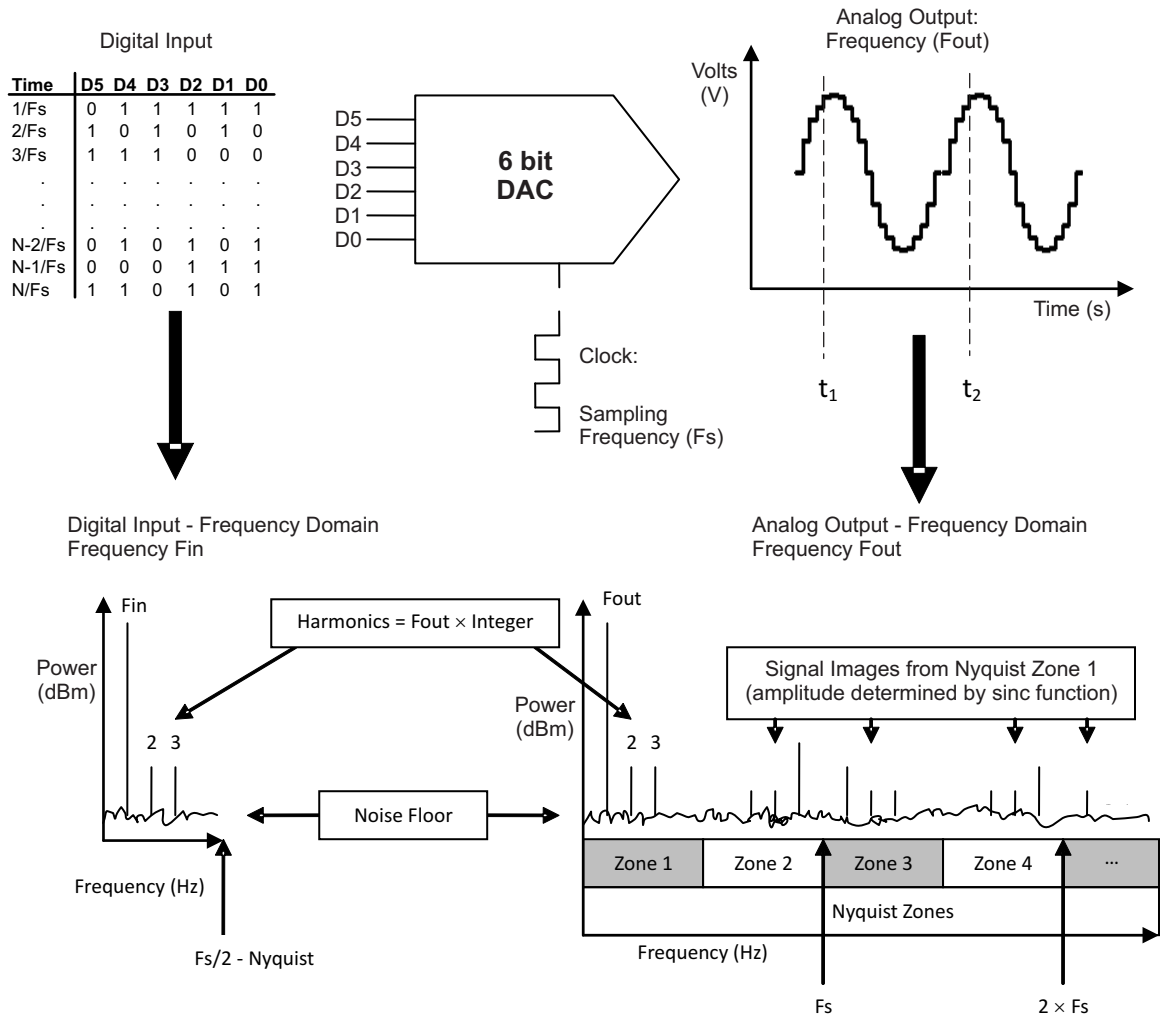
Figure 1 provides the basic block diagram, functionality and common terminology for DACs. This figure shows a digital word applied to the inputs of the DAC, which is then converted to an analog signal at the sampling frequency (Fs) applied to the DAC clock. Figure 1 is a time domain representation of the DACs input and output signals.



Fout: Analog Output Frequency = $1/(t_2 - t_1)$
Fs: Clock Frequency
N: Number of digital samples
n: Number of output bits; in this 6 bit DAC example n = 6

Figure 1. Basic DAC Diagram and Terminology

Time domain representations are often described as real world signals. In Figure 1, notice the analog output's amplitude is shown in volts (linear) and seconds (linear). Also notice the digital input codes are listed with time stamps (1/Fs, 2/Fs, 3/Fs…). Time domain representations are often easy to visualize and help with understanding gross concepts. However the time domain is poor when it comes to measuring performance of DACs and other signal processing devices. Measuring performance is best done in the frequency domain. Therefore, it is important to understand how the time domain and frequency domain relate.



Fout: Analog Output Frequency = $1/(t_2 - t_1)$
Harmonics: Integer Multiples of Fin (2 × Fout, 3 × Fout, …)
Fs: Clock Frequency
Nyquist: Fs/2
Nyquist Zone 1 = 0 to Fs/2; **Zone 2** = Fs/2 to Fs; **Zone 3** = Fs to 3 × Fs/2, ...
Images: Frequencies > Fs/2 (Nyquist) that land in the analog output frequency domain, explained later in more detail
Sinc function: Sinx/x

Figure 2. Frequency Domain vs. Time Domain

Figure 2 demonstrates a high level overview of the differences between the time domain and the frequency domain. Frequency domain plots are measured in Signal Power (log scale) and frequency (linear). Figure 2's frequency domain plots the signal imperfections are labeled as noise and harmonics. Notice the ease with which one can identify and quantify these imperfections. Frequency domain plots are also commonly termed spectrums, spectral plots, or Fast Fourier Transforms (FFT). In Figure 2 the terms Nyquist, harmonics, imaging and the sinc function are introduced. These important signal processing terms will be discussed in more detail later.

2 Spectral Performance Terminology

SNR: Stands for **S**ignal to **N**oise **R**atio. SNR is the ratio of the RMS value of the fundamental (P_S) output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise (P_N), but excluding the first six harmonics and dc. Refer to Figure 3 for the SNR equation and illustration.

SFDR: Stands for **S**purious **F**ree **D**ynamic **R**ange: SFDR is the ratio of the power of the fundamental (P_S) to the next highest spur (P_H). Refer to Figure 3 for the SFDR equation and illustration. Unless noted in the datasheet SFDR includes the harmonics, but excludes dc.

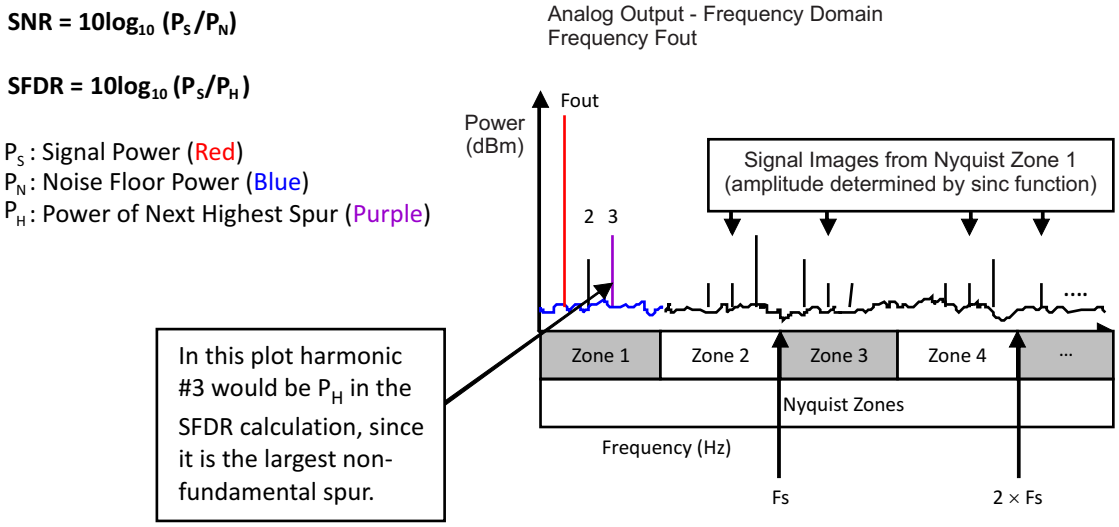


Figure 3. Single tone DAC Performance Terminology

ACLR: Stands for **A**djacent **C**hannel **L**eakage Ratio. ACLR is used to measure a variety of standards with different signal bandwidths and offsets. Figure 4 is provided as an example of the 3.84Mcps 3GPP W-CDMA input signal measured in 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio. Refer to Figure 4 for ACLR equation and illustration.

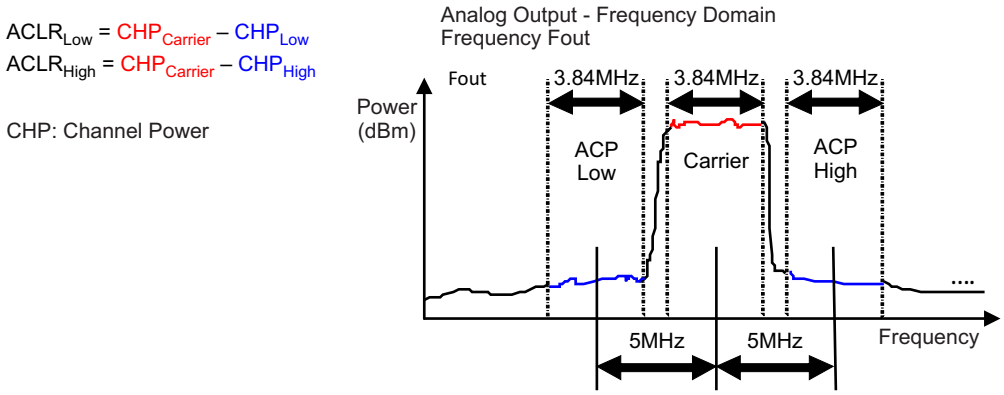


Figure 4. WCDMA ACLR

IMD3: refers to the **I**nter**M**odulation **D**istortion from the 3rd harmonic of a circuit. IMD3 is of particular importance in narrow or wide band signals because its distortion products can land in the signal band or the adjacent channel. This can be seen by looking at a signal that is made up of two sine waves, one at f_1 and one at f_2. The 3rd order products of these sine waves create frequencies at 2 x f_2 – f_1 and 2 x f_1 – f_2, which are very close to the signals f_1 and f_2. Refer to Figure 5 for the IMD3 equation and illustration.

IMD3 = $P_1 - P_3$

P_1: Signal Power (Red)
P_3: IM3 Power (Blue)

Assumes power of $f_1 = f_2$
Assumes power of $IM3_1 = IM3_2$

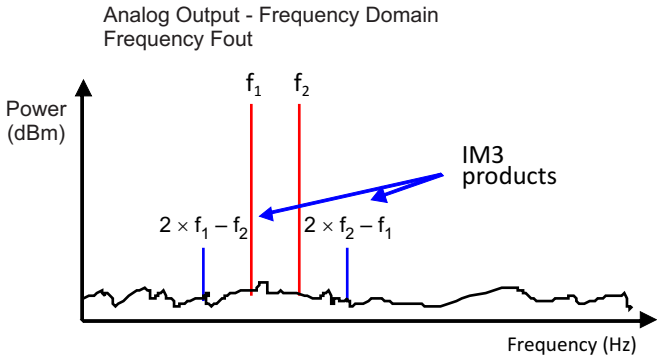


Figure 5. IMD3

3 DAC Nyquist Zones, Zero Order Hold, and Images

The terms Nyquist zones, Zero Order Hold and Images are some basic DAC terms. Once understood, many of the advanced DAC concepts discussed later will follow naturally. The following paragraph asks some questions whose answers will lead to an understanding of these terms.

Why do the frequency domain plots differ in Figure 6 and Figure 7? The answer lies within the red circle in Figure 7's time domain plot. For ease of explanation, there are 2 differences in Figure 7's Frequency domain plot that will be discussed. 1) Why do the F_{out} images exist in every Nyquist zone? (What is a Nyquist Zone?) 2) Why do the F_{out} images decrease in amplitude?

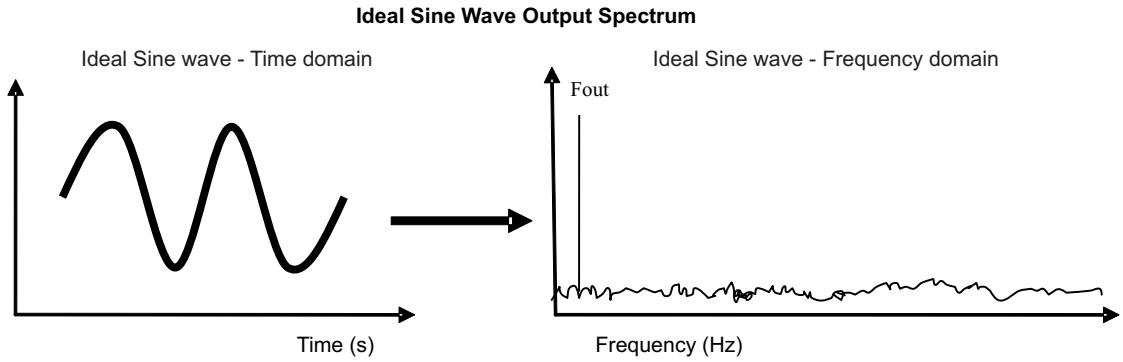


Figure 6. Ideal Sine Wave

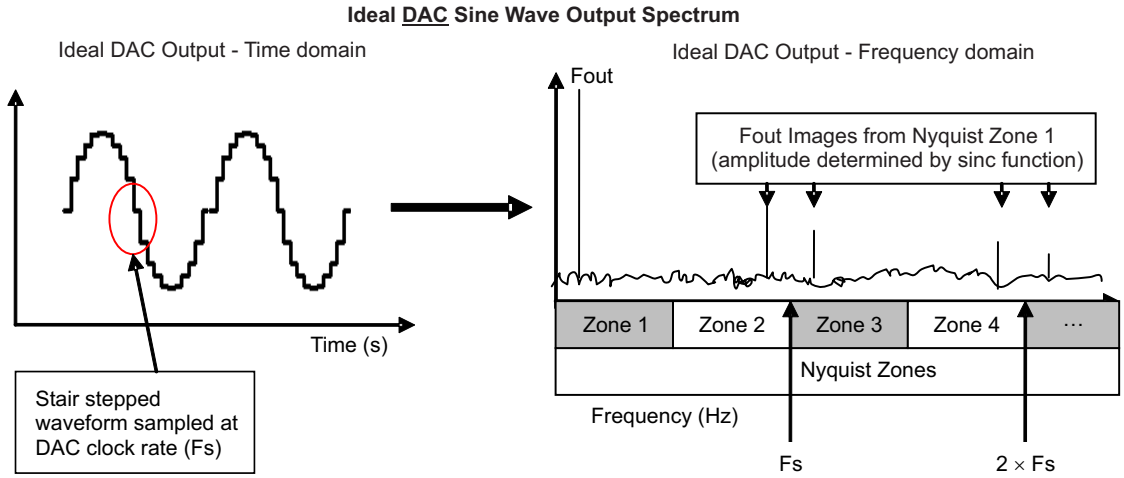


Figure 7. Ideal DAC Sine Wave

1) In Figure 7, why do the F_{out} images exist in every Nyquist zone? What is a Nyquist Zone?

The Poisson summation formula indicates that the samples of function x(t) are sufficient to create a *periodic extension* of function X(f). The result is:

$$X(f) = \sum_{k=-\infty}^{\infty} X(f - kFs) \tag{1}$$

The variable k in Equation 1 causes the Fourier transform output to output a copy of the signal X(f) at every multiple of Fs. Equation 1's output is depicted visually in Figure 8 as copies of X(f) are shifted by multiples of Fs. Figure 8 also provides a visual example of the Nyquist Frequency, Fs/2. Since these signals are repeated at multiples of Fs, then for bandwidths greater than Fs/2 information loss (red area) will occur. As shown in Figure 8 multiples of the Nyquist frequency determines the Nyquist Zones. In most literature, Nyquist Zones are only defined for the positive frequency spectrum.

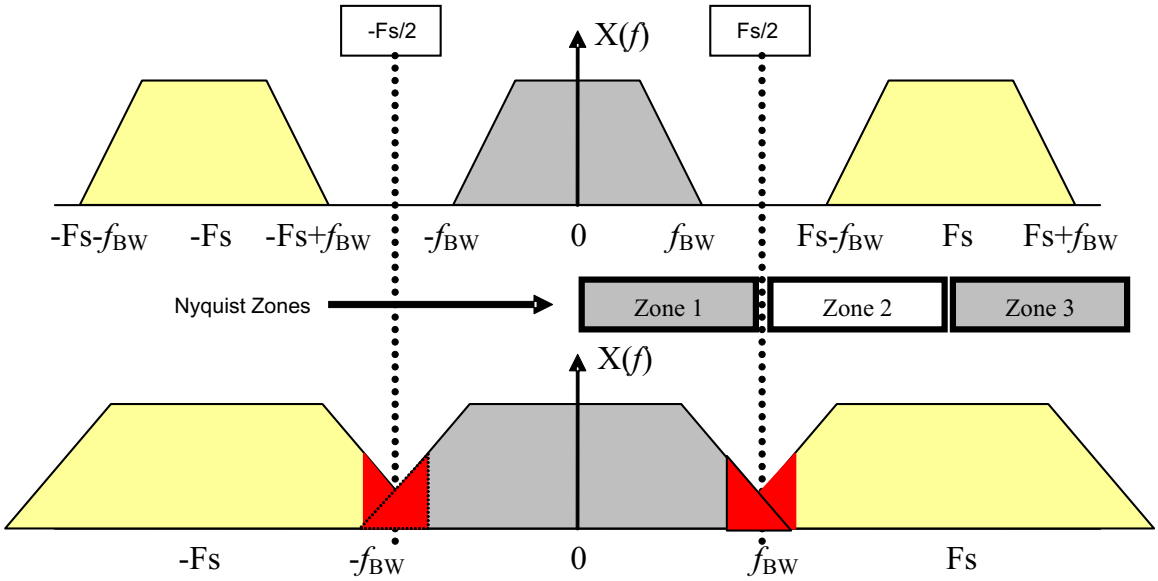


Figure 8. Hypothetical Spectrum (sampled at Fs)

Using Equation 1 in conjunction with Figure 7, X(f) would be sin(f) and the sample rate is F_s. Using Equation 1 this expands to
X(f) = sin(f+∞× F_s)…+ sin(f+2×F_s) + sin(f+F_s) + sin(f) + sin(f-F_s) + sin(f-2×F_s) ...+ sin(f-∞× F_s).

In Figure 7, what is not shown is the –F_{out} plot of the spectrum. Adding F_s to F_{out} and –F_{out} results in the tones shown in Nyquist Zones 2 and 3. Likewise adding 2×F_s to F_{out} and –F_{out} results in the tones shown in Nyquist Zones 4 and 5. This explains why the Fout exist in every Nyquist zone in Figure 7.

2) In Figure 8, why do the F_{out} images decrease in amplitude?

The answer is due to frequency response of the zero-order hold function. In Figure 9, a zero order hold function is shown in the time domain and frequency domain. The frequency domain plot shown in Figure 9 is also the sinc function (sin(x)/x). The sinc function has a decreasing amplitude with frequency due to the denominator x.

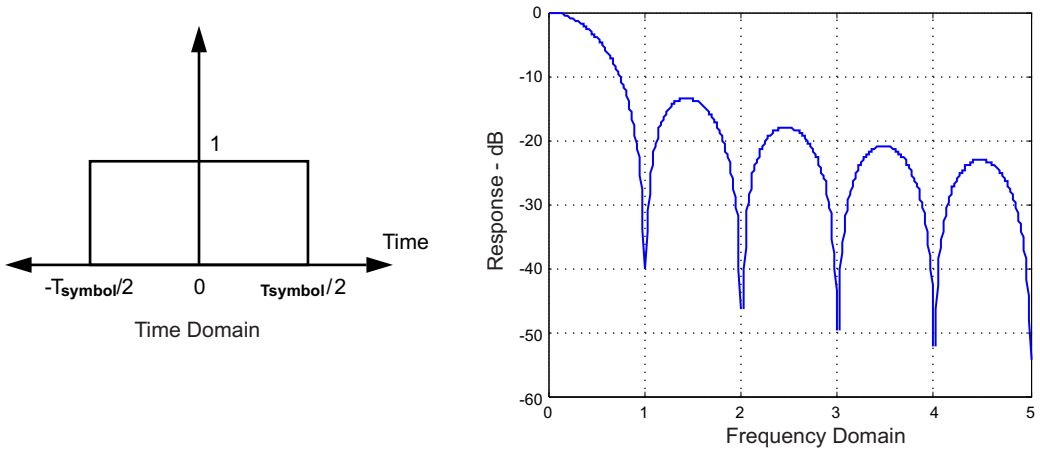


Figure 9. Zero Order Hold Time and Frequency Domain plots

The DACs sampling nature creates the analog output to have a zero order hold function at each sample. This is shown pictorially in Figure 10 and Figure 11. The math behind these concepts is described in many textbooks and is a very lengthy topic. The decreasing amplitude of the F_{out} images in Figure 7, and Figure 11 are determined by the sinc function of the zero order hold as a result.

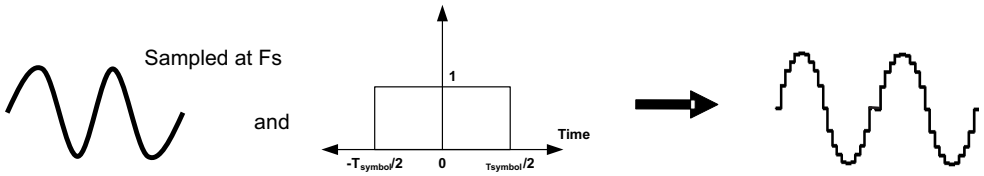


Figure 10. Convolution in the Time Domain

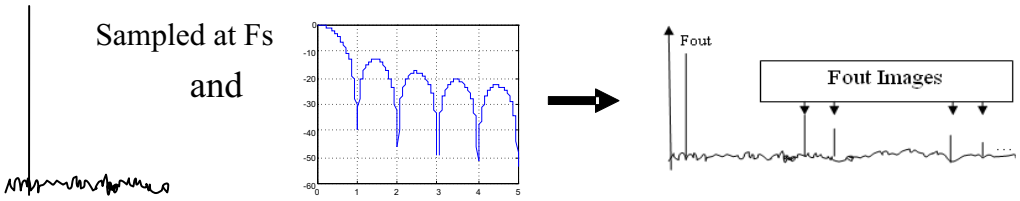
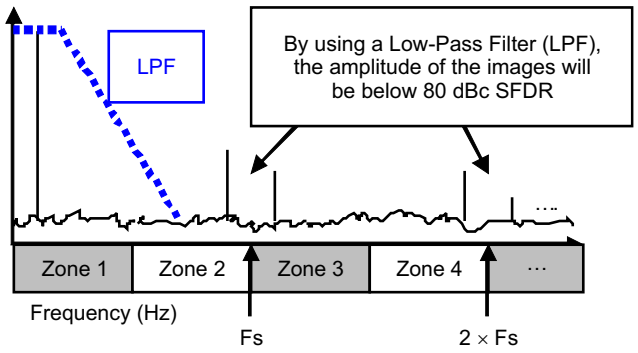
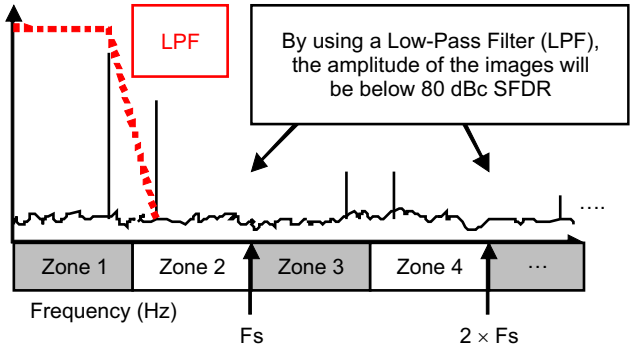
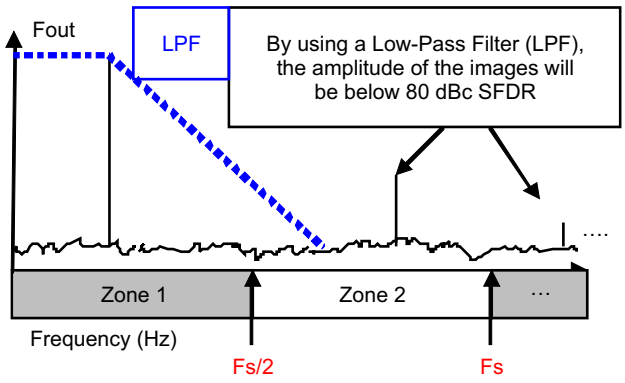


Figure 11. Convolution in the Frequency Domain

4 Interpolating DAC Topic 1: FIR filters

To understand the need for FIR filters in interpolating DACs, the design constraints of high speed DACs should be understood initially. Consider the following three cases in Table 1. Spend some time to understand the concerns and comments in each of the 3 cases.

Table 1. DAC Case Study

Customer Requirements: Fs = 250Msps Fout = 20MHz SFDR = 80dBc **Concerns/Comments:** None	**Case 1:** 
Customer Requirements: Fs = 250Msps Fout = 100MHz ← change from case 1 SFDR = 80 dBc **Concerns/Comments:** Tough LPF requirements due to image amplitude and frequency spacing. Sinc Function: – Amplitude loss in Fout (SNR degraded) – Larger Image at Fs-Fout If this LPF exist it will be more expensive than the one used in Case 1	**Case 2:** 
Customer Requirements: Fs = 500Msps ← change from case 2 Fout = 100MHz SFDR = 80dBc **Concerns/Comments:** A higher sample rate solves LPF and amplitude (SNR) concerns in Case 2. Higher DAC sample rates forces the DAC to have an LVDS interface – complexity, 2× of signals/pins – cost: to achieve higher clock and data rates a higher cost ASIC/FPGA is required	**Case 3:** 

In Table 1, cases 2 and 3 illustrate that as F_{out} frequency increases there are technical trade-offs of SNR, low pass filtering requirements, and data rate requirements. These trade-offs can increase the cost and complexity of the system design.

The FIR filters in interpolating DACs were designed to address the trade-offs shown in Table 1. This basic idea is to provide a slower data rate to the DAC inputs and oversample the data inside the interpolating DAC. Interpolating DACs have the slower data rate benefit of Table 1's case 2 and the LPF and SNR benefits of Table 1's case 3. When compared to a standard DAC the trade-offs are increased cost, a slightly larger package footprint, and possibly a more complicated clock scheme.

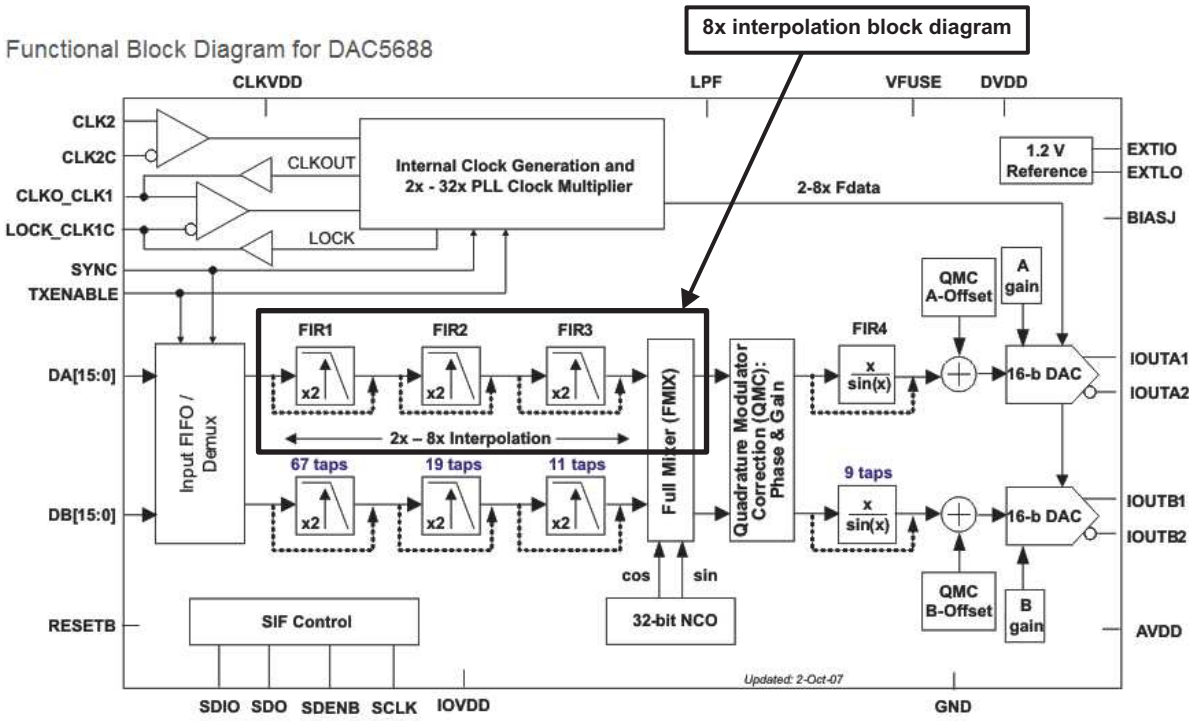
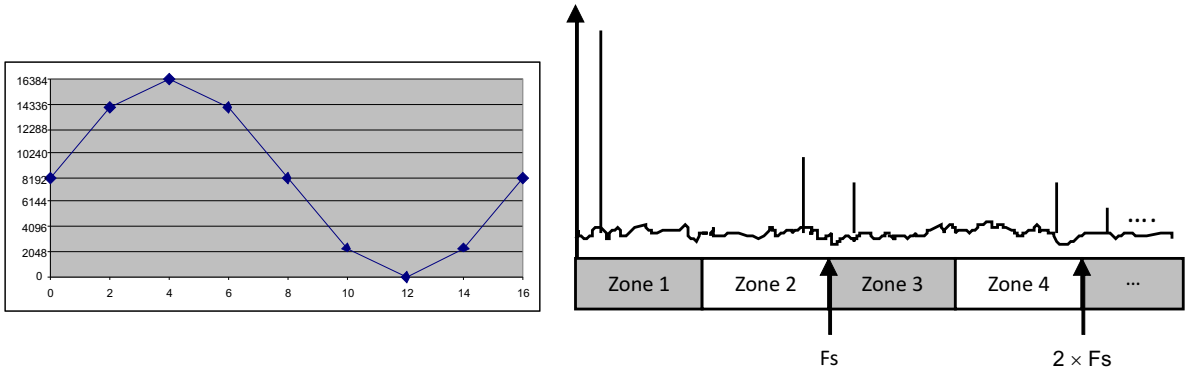


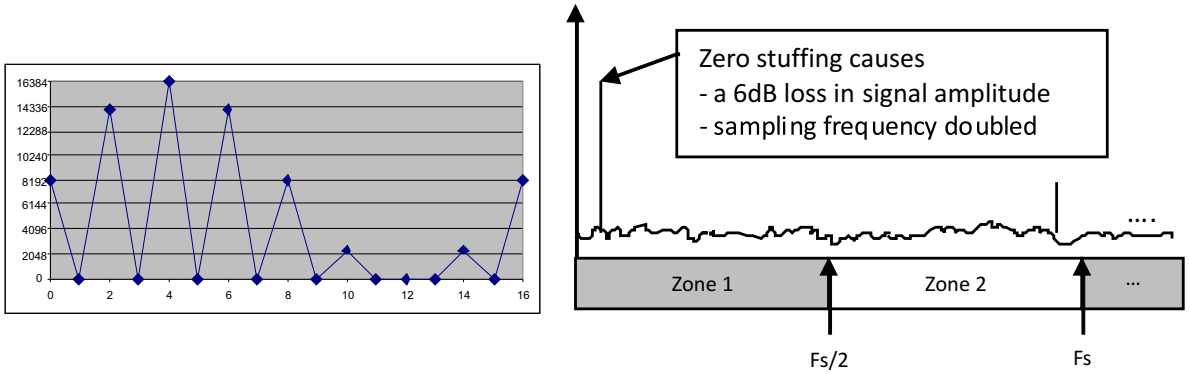
Figure 12. DAC5688 Block Diagram – FIR filters

Interpolating DACs often have capabilities to perform 8x or 16x interpolation by daisy chaining multiple FIR filters as seen in Figure 12. Figure 13 is a pictorial example of how one FIR filter in an interpolating DAC functions. Figure 13 is a simple example of one FIR performing 2x interpolation of the input signal.

Stet 1: Samples sent to DAC inputs
Samples: 8192, 13984, 16383, 13784, 8192, 2399, 8192



Stet 2: Internally the DAC inserts 0's between each sample (2x oversampling - zero stuffing)
Samples: 8192, **0**, 13984, **0**, 16383, **0**, 13784, **0**, 8192, **0**, 2399, **0**, 0, **0**, 2399, **0**, 8192



Stet 3: Using samples from Step 2. The DAC FIR filter creates following samples
Samples: 8192, **11327**, 13984, **15760**, 16383, **15760**, 13784, **11326**,
8192, **1557**, 2399, **623**, 2399, **5057**, 8192

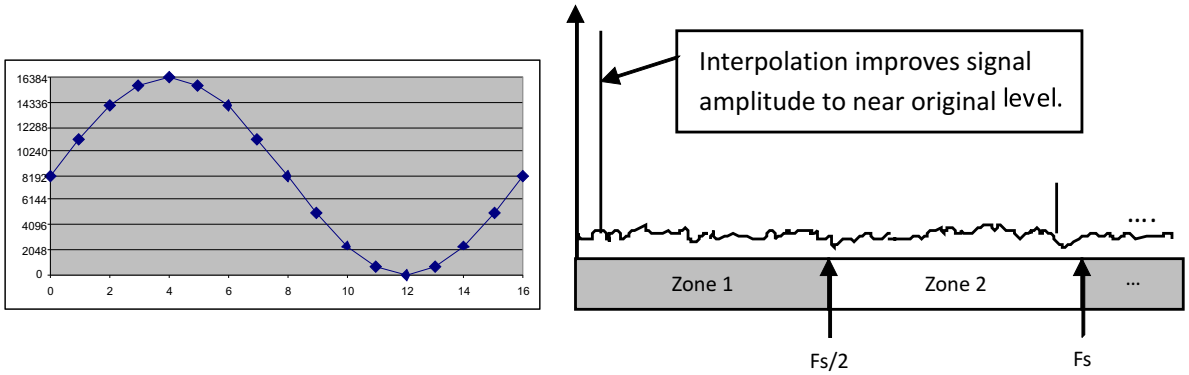


Figure 13. Interpolation Example

A DACs datasheet will provide the FIR (Finite Impulse Response) filter shapes and specifications. Figure 14 provides an example of some plots that can be found in datasheets.

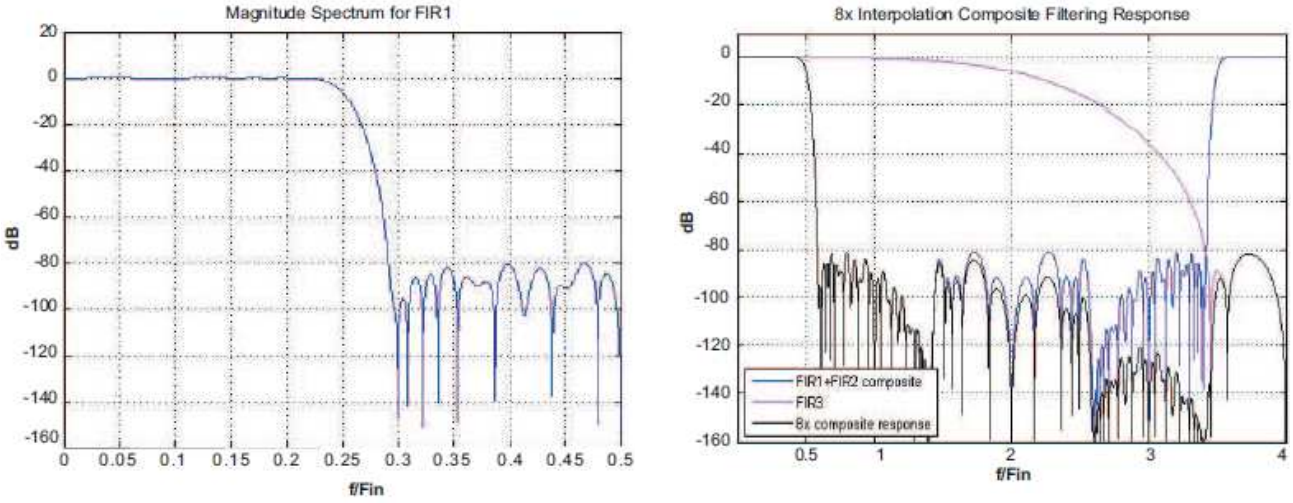


Figure 14. Single FIR Filter and a Composite FIR Filter Spectrum

Interpolation does create a new design consideration. After the FIR filters the DAC will need to be clocked at a multiple of the data rate. This implies there would be two clocks, one for the data and one for the DAC. For instance in a 2x interpolation mode as shown in Figure 13, the DAC will require a clock 2x the speed of the input data rate. Similar statements can be made about 4x, 8x, and 16x interpolation modes.

Most interpolating DACs provide 3 options to solve this clocking concern. Each option has a cost/complexity vs. performance trade-off.

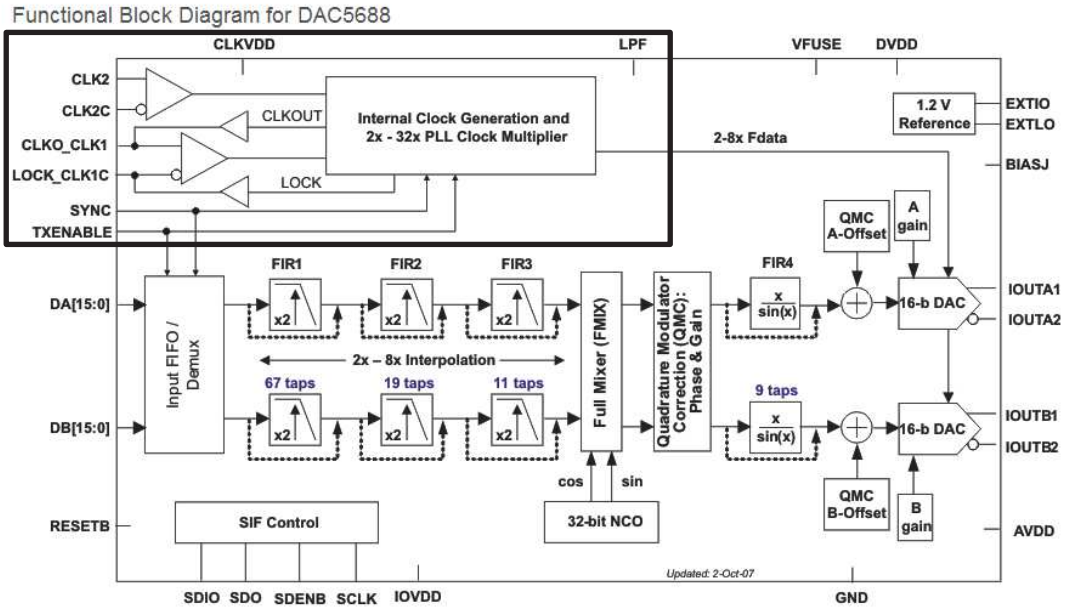


Figure 15. DAC5688 Block Diagram – Clock Section

Option 1: PLL Clock Mode

The PLL clock mode allows for the user to input a reference clock at the data rate. The internal VCO/PLL will than generate the higher frequency DAC clock from the reference clock. This mode reduces system cost and complexity by allowing the designer to use the DAC without the need for a higher speed clock. However, often the PLL/VCO option generates more phase noise than an external clock. This added phase noise will affect the DACs SNR and SFDR performance.

Option 2: External Clock Mode
A high speed clock is applied to the DAC at the DAC sample rate. The data sample rate is divided down from this high speed clock. Compared to option 3 this reduces system cost and complexity as only one clock is needed. This method also has good clock phase noise. If multiple DACs are used in a system, then dividing the high speed DAC clock to the lower speed data clock rate can create some phase uncertainty between multiple DACs, as it is not certain that all the DAC clock dividers are triggering on the same clock edge. This may be a problem in some system designs.

Option 3: Dual Clock Mode
One clock is supplied at the DAC speed and another clock is supplied at the data rate. When used with multiple DACs this method solves the phase uncertainty problem with Option 2. This method has good clock phase noise. The method adds cost to the design when compared with the other methods.

5 Interpolating DAC Topic 2: Digital Mixing

In many system designs the digital mixing function is used to shift a signal to another frequency for channel selection or to improve image filtering requirements. Often this function of digital mixing is performed with an external digital chip, either a DSP or FPGA. Most interpolating DACs include this function in their digital logic section. This helps reduce the complexity of the digital baseband design by moving this functionality inside the DAC.

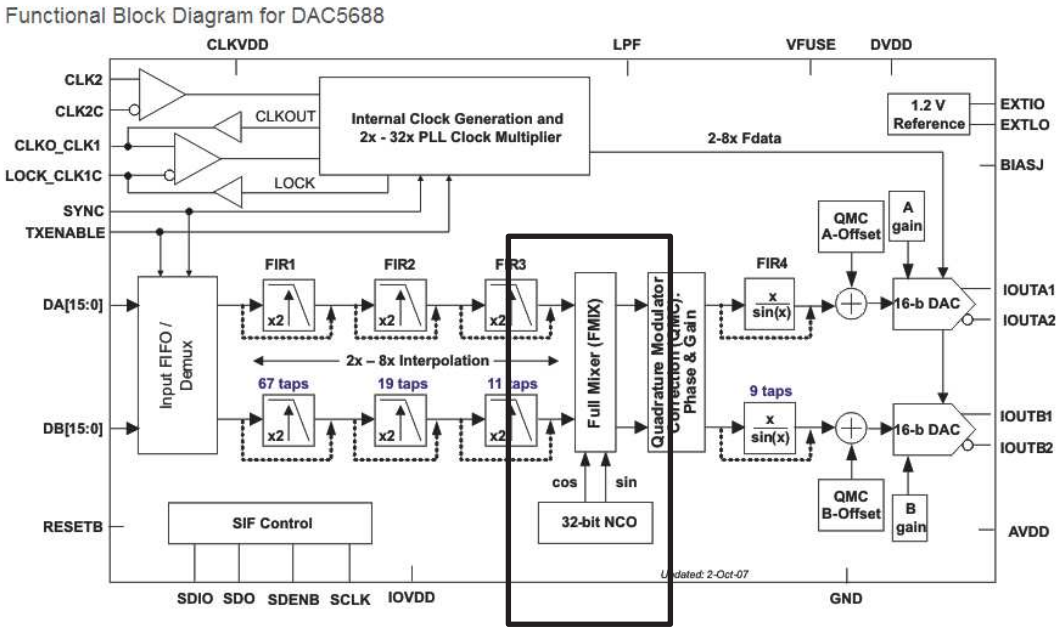


Figure 16. DAC5688 Block Diagram – Digital Mixing Section

Figure 16 provides the block diagram of the digital mixing section. In this digital section signals from the FIR filters are mixed with a digital sine wave from the Numerically Controlled Oscillator (NCO). The output of the mixer will shift the incoming signal to another frequency based on the NCO's frequency.

NCO
The NCO creates a cosine and a sine wave at identical frequencies. The frequency of the NCO is calculated by the DAC clock frequency and the values for the NCO programmed in the serial interface. Equation 2 provides an example of an equation used to set the NCO output frequency. For a given DAC it is best to refer to the datasheet for the exact equation for that DAC. In the Equation 2 example the denominator is 2^{32}. The denominator sets the frequency resolution of the NCO:

$$f_{NCO} = \left(freq \times f_{NCO\_CLK}\right)/2^{32} \quad (2)$$

Where:

f_{NCO}: output frequency of NCO
freq: 32bit frequency word programmed by serial interface

f_{NCO_CLK}: clock frequency supplied to NCO

Digital Mixer (Digital Up Converter – DUC)
The signals from the NCO and FIR filter or Data inputs are then fed into the digital mixer.

The Digital mixer can be used in one of three modes. The three modes are:

1. Complex IQ In and 1 Real Out
2. Complex IQ In and Complex IQ Out
3. 2 Real In and 2 Real Out.

The following will describe how the digital mixer works. Initially mode 1, **Complex IQ In and 1 Real Out** will be analyzed to understand the mixer behavior.

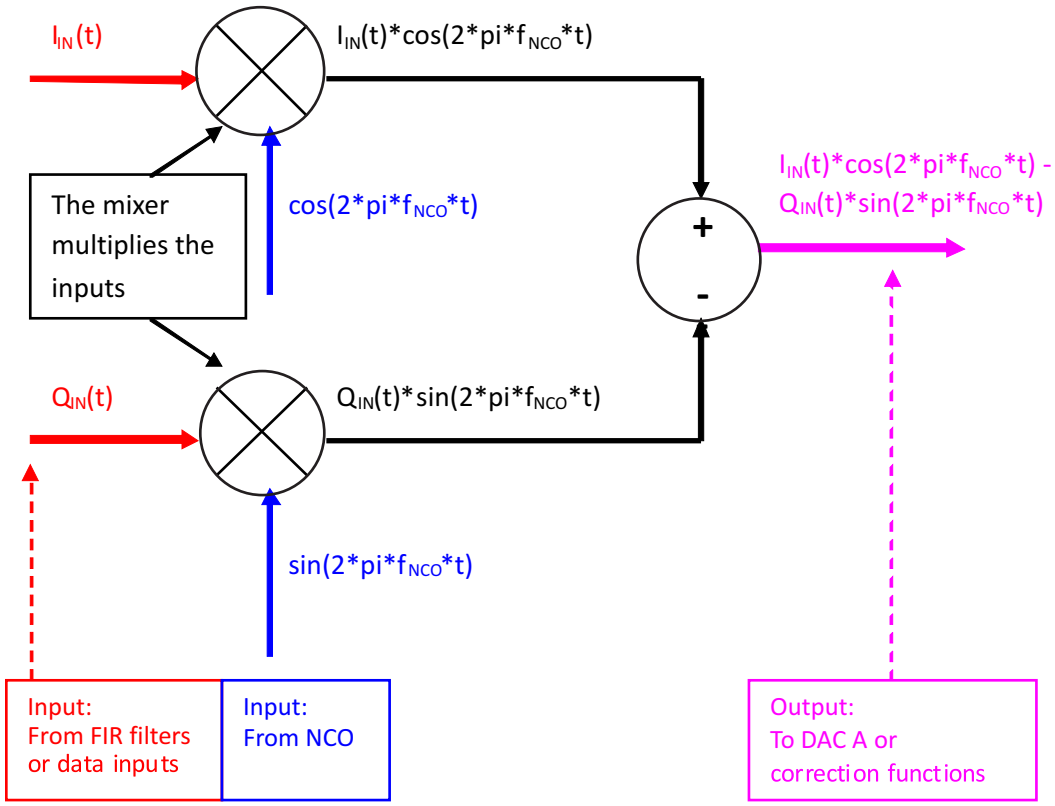


Figure 17. Digital Mixer, Complex IQ In and 1 Real Out

At this point the math is a little cumbersome at the digital mixer output in Figure 17. Using trigonometry identities, and by making an assumption, the output equation can be simplified. The assumption is that input signals I_{IN} and Q_{IN} are the same signal, but are 90 degrees out of phase. The reason this assumption is made is that this is how most customers will use this DAC function in their application. Also, for ease of illustration I_{IN} and Q_{IN} will be single frequency signals (sine wave and cosine waves). The result of this assumption is shown in Figure 18.

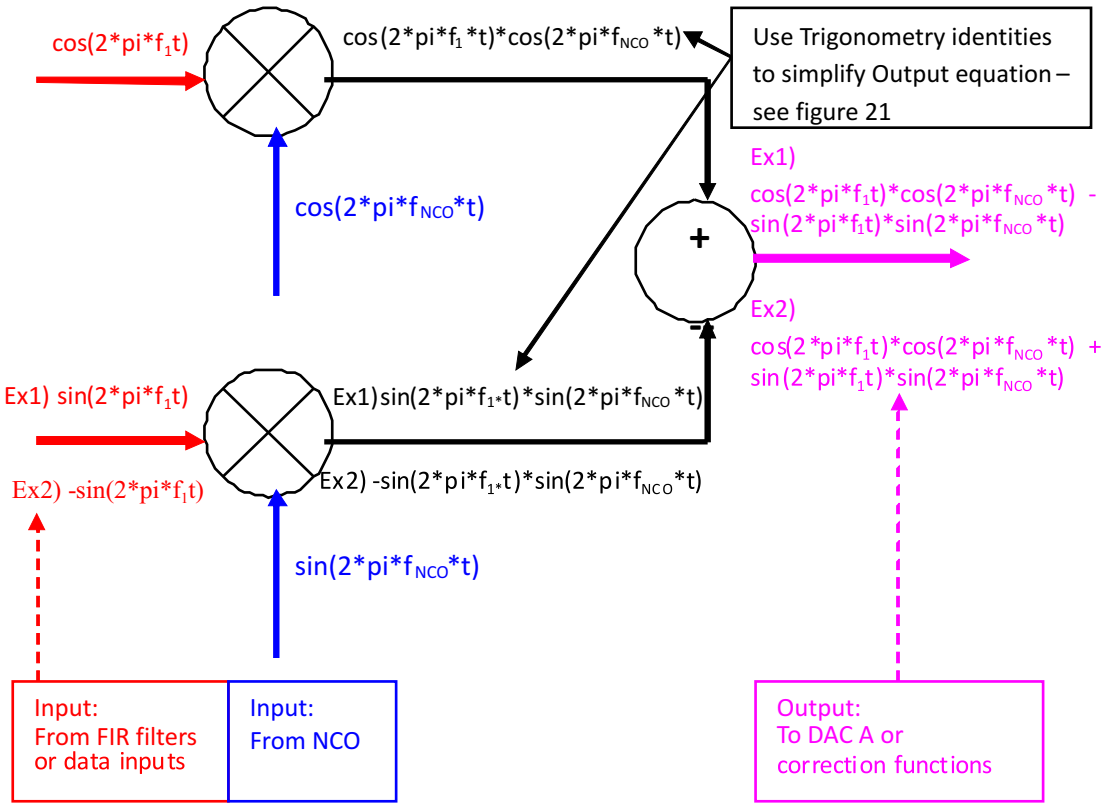


Figure 18. Digital Mixer, Complex IQ In and 1 Real Out (2 examples)

At this point the math is still cumbersome, but it allows for some simplifications using trigonometry identities shown below. Figure 19 shows the result of this simplification.

Product to Sum Identities

$\cos(\Phi) \times \cos(\psi) = 1/2 \times [\cos(\Phi-\psi) + \cos(\Phi+\psi)]$
$\sin(\Phi) \times \sin(\psi) = 1/2 \times [\cos(\Phi-\psi) - \cos(\Phi+\psi)]$
$\sin(\Phi) \times \cos(\psi) = 1/2 \times [\sin(\Phi+\psi) + \sin(\Phi-\psi)]$
$\cos(\Phi) \times \sin(\psi) = 1/2 \times [\sin(\Phi+\psi) - \sin(\Phi-\psi)]$

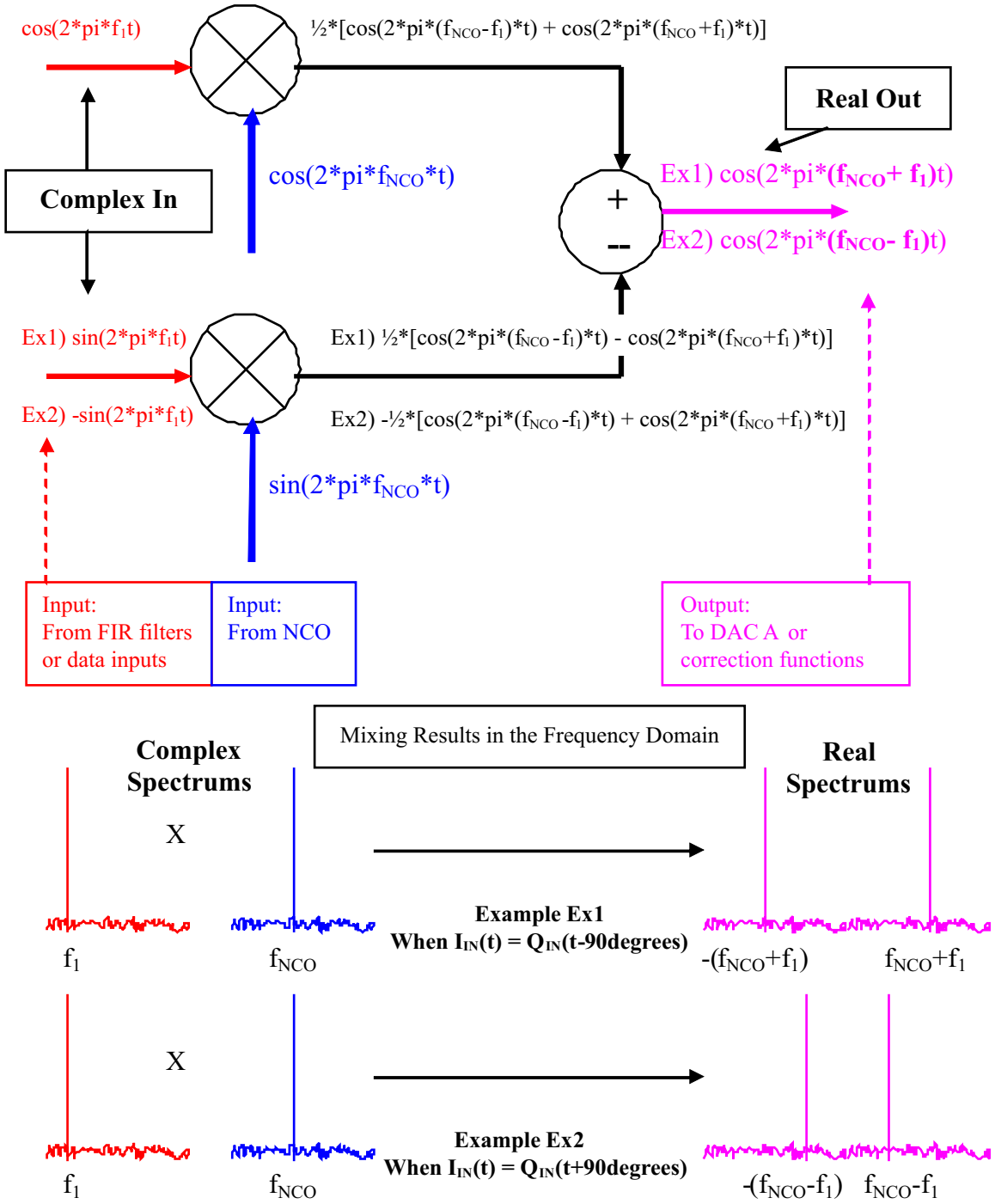


Figure 19. Digital Mixer, Complex IQ In and 1 Real out

The output in Figure 19 produces a very simple formula for this digital mixer operation. Notice the real output is simply a frequency shift of the complex input signal. Whether I_{IN} and Q_{IN} are –90 or +90 degrees out of phase, would determine whether one would add or subtract the NCO and Input frequencies ($f_{NCO} \pm f_1$). This operation is shown in the frequency domain plots in Figure 19.

For wideband signals the same concept of adding or subtracting the wideband signal from the NCO frequency will result in a frequency shift. The wideband signal example is shown in Figure 20.

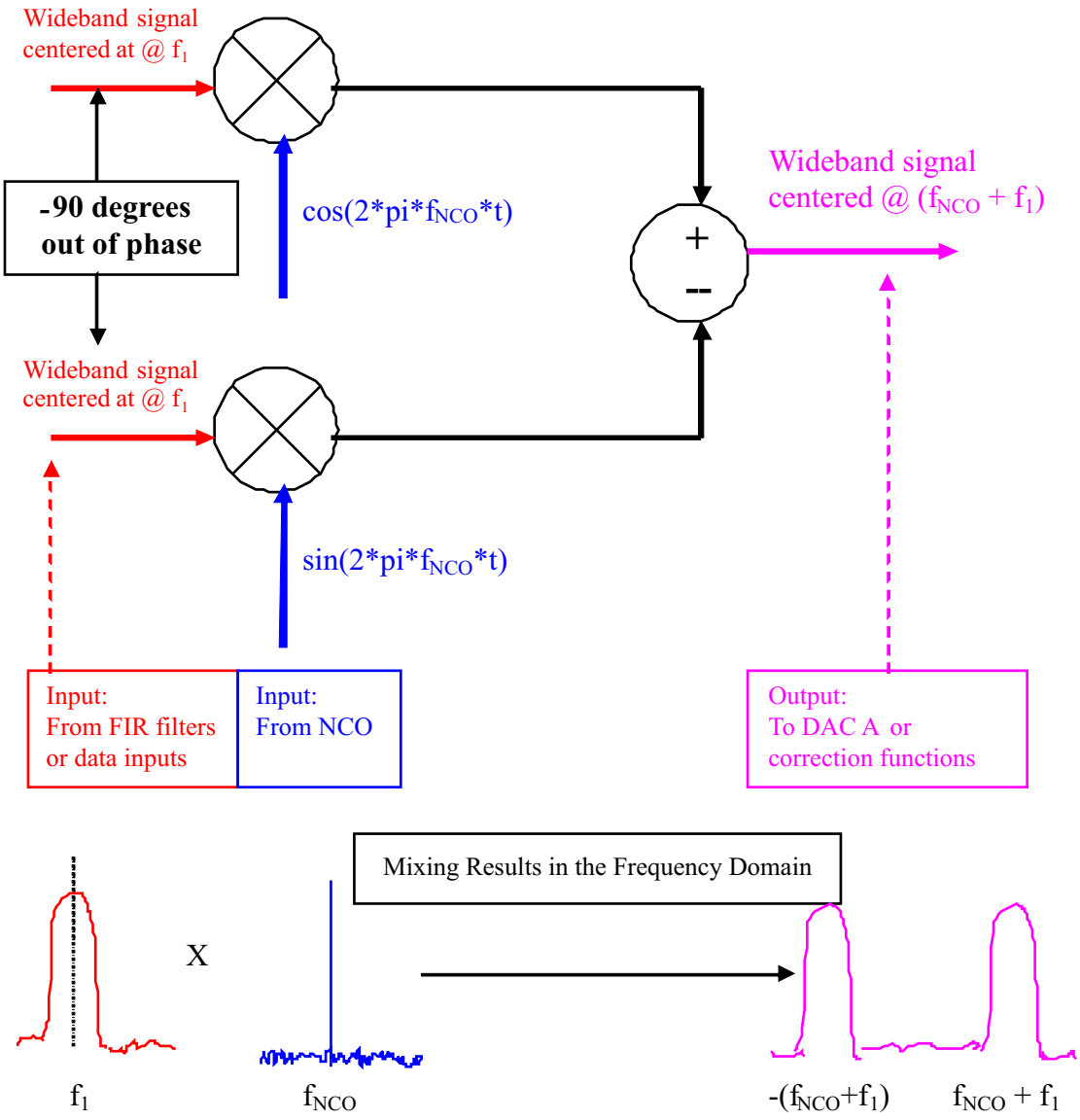


Figure 20. Digital Mixer, Complex IQ In and 1 Real out – Wideband example

Figure 19 and Figure 20 also begin to hint at one of the weaknesses of the complex in to real out architecture. All real signals have a positive and a negative frequency that are equal in amplitude. This weakness is seen in with a radio architecture where the DAC output needs to be up converted to an RF signal by an analog mixer. Notice the analog mixer up converts both the positive and negative IF frequencies. This results in duplicate information since two different RF±IF frequencies (sidebands) are created. Duplicate information has the results of increasing the noise floor by 2x and decreasing the mixer's bandwidth by a half. The end result of this is that BPF #2 is used to remove one of the two signals. In Figure 21, there is a term labeled LO feed through. LO feed through is a common issue with analog mixers. With a real signal a BPF is used to remove the LO feed through. Real signals do not allow for the option of digital correction techniques to remove LO feed through.

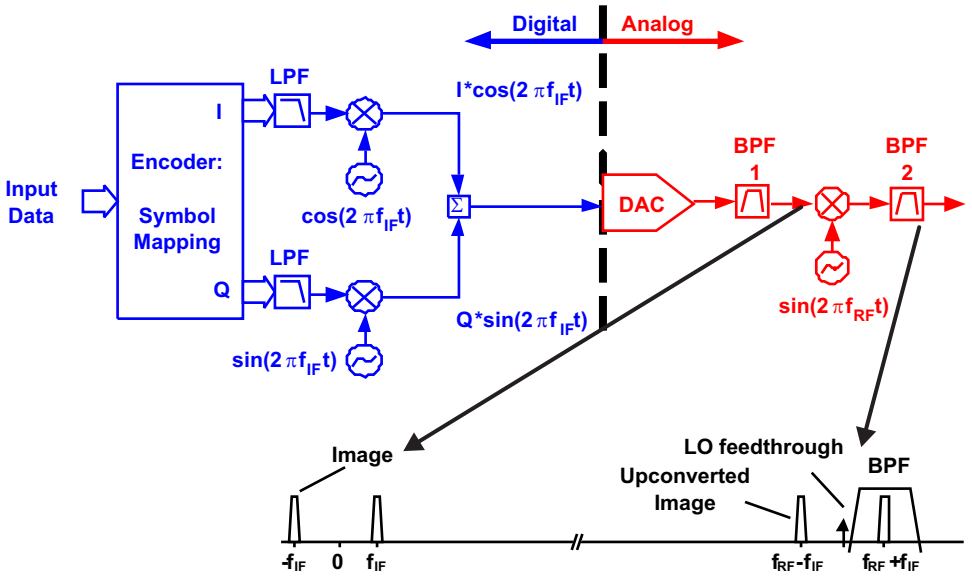


Figure 21. Real Output System Architecture

Mode 2, **Complex IQ In and Complex IQ Out** is a fairly similar concept in the digital section, with the one significant exception being that 2 digital mixers are used. The outputs of the two digital mixers create a complex IQ signal. In theory this complex IQ out signal solves the weakness of the Complex IQ In to Real Out architecture in Figure 21. In practice these theoretical improvements were not possible until recent advances in DSP correction algorithms that are more readily available today. A block diagram of mode 2 is shown in Figure 22.

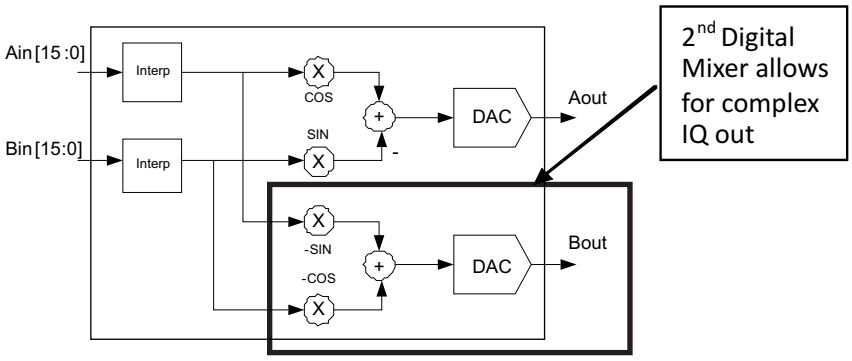
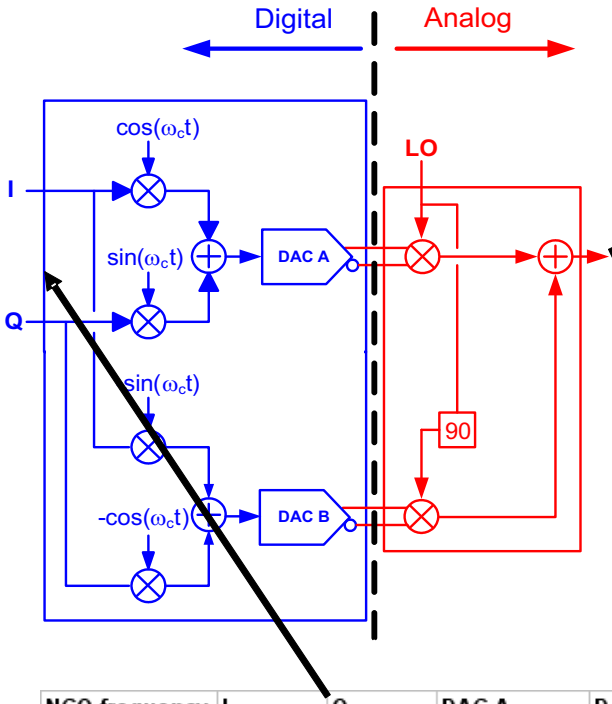


Figure 22. Digital Mixer, Complex IQ In and Complex IQ Out

Figure 22 shows a typical Complex IQ In to Complex IQ Out application schematic. In Figure 23 the Complex IQ Out signal is up converted to a real signal by an analog mixer. Also notice this architecture has the ability to program a –NCO frequency. This is another advantage of this mode over the Complex IQ in to Real Out mode.



This diagram uses the same Trigonometry functions as Figure 18-20. However, for this example only the results are shown in the table below.

NCO frequency	I	Q	DAC A	DAC B	Analog Out
.+ f_{NCO}	cos(f_1)	sin(f_1)	cos(f_{NCO}+f_1)	.-sin(f_{NCO}+f_1)	cos(f_{RF}+f_{NCO}+f_1)
	cos(f_1)	.-sin(f_1)	cos(f_{NCO}-f_1)	.-sin(f_{NCO}-f_1)	cos(f_{RF}+f_{NCO}-f_1)
.-f_{NCO}	cos(f_1)	sin(f_1)	cos(-f_{NCO}+f_1)	.-sin(-f_{NCO}+f_1)	cos(f_{RF}-f_{NCO}+f_1)
	cos(f_1)	.-sin(f_1)	cos(-f_{NCO}-f_1)	.-sin(-f_{NCO}-f_1)	cos(f_{RF}-f_{NCO}-f_1)

Figure 23. Digital Complex IQ In, Digital Complex IQ Out, With an Analog Mixer

Analog mixers inherently have some errors that cause LO feed through or sideband issues. As mentioned previously, in theory the Complex IQ In, Complex IQ Out mode can correct for these issues by adjusting the DACs phase and offset values. This will be discussed in more detail in the Quadrature Modulator Correction (QMC) section.

Mode 3, 2 Real In and 2 Real Out, takes advantage of some unique properties of the mixer and interpolation filters. This mode can only be used when the NCO is set to half of the DAC clock speed. By running the NCO at this rate the cos function of the NCO will output { ..-1,1,-1,1,….}. Likewise the sin function of the NCO will output {…0,0,0,0…}. The result of this the sin function will cancel out the signal and the resulting block diagram is shown in Figure 24.

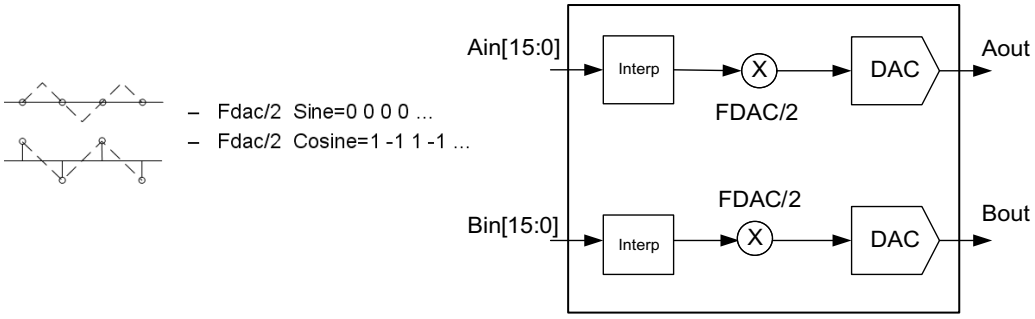


Figure 24. Digital Mixer, 2 Real In and 2 Real Out

6 Interpolating DAC Topic 3: Quadrature Modulator Correction (QMC)

To understand the need for the QMC section of the interpolating DACs it is best to understand that in many applications the DAC outputs are connected to the input of a quadrature modulator. The path between the DAC and the modulator itself have DC, gain and phase errors. As seen in Figure 25 these DC, gain and phase errors create spectral errors. In Figure 25, it can be noticed that 2 unwanted spurs are created in the RF spectrum due to these errors. The unwanted carrier spur (F_{LO}) is a result of the DC error mixing with the LO frequency. The unwanted side band spur (F_{SB}) is a result of the gain and phase errors.

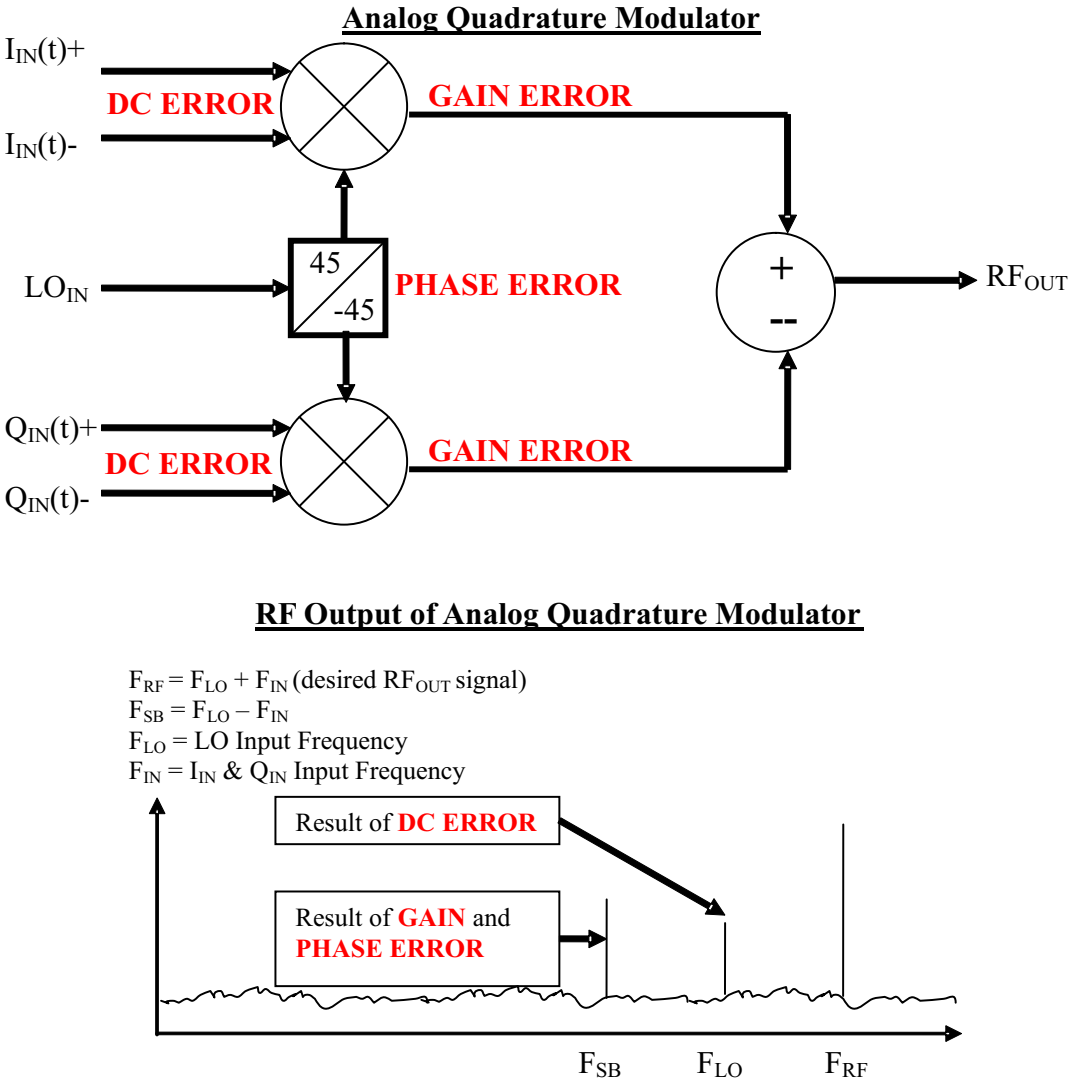
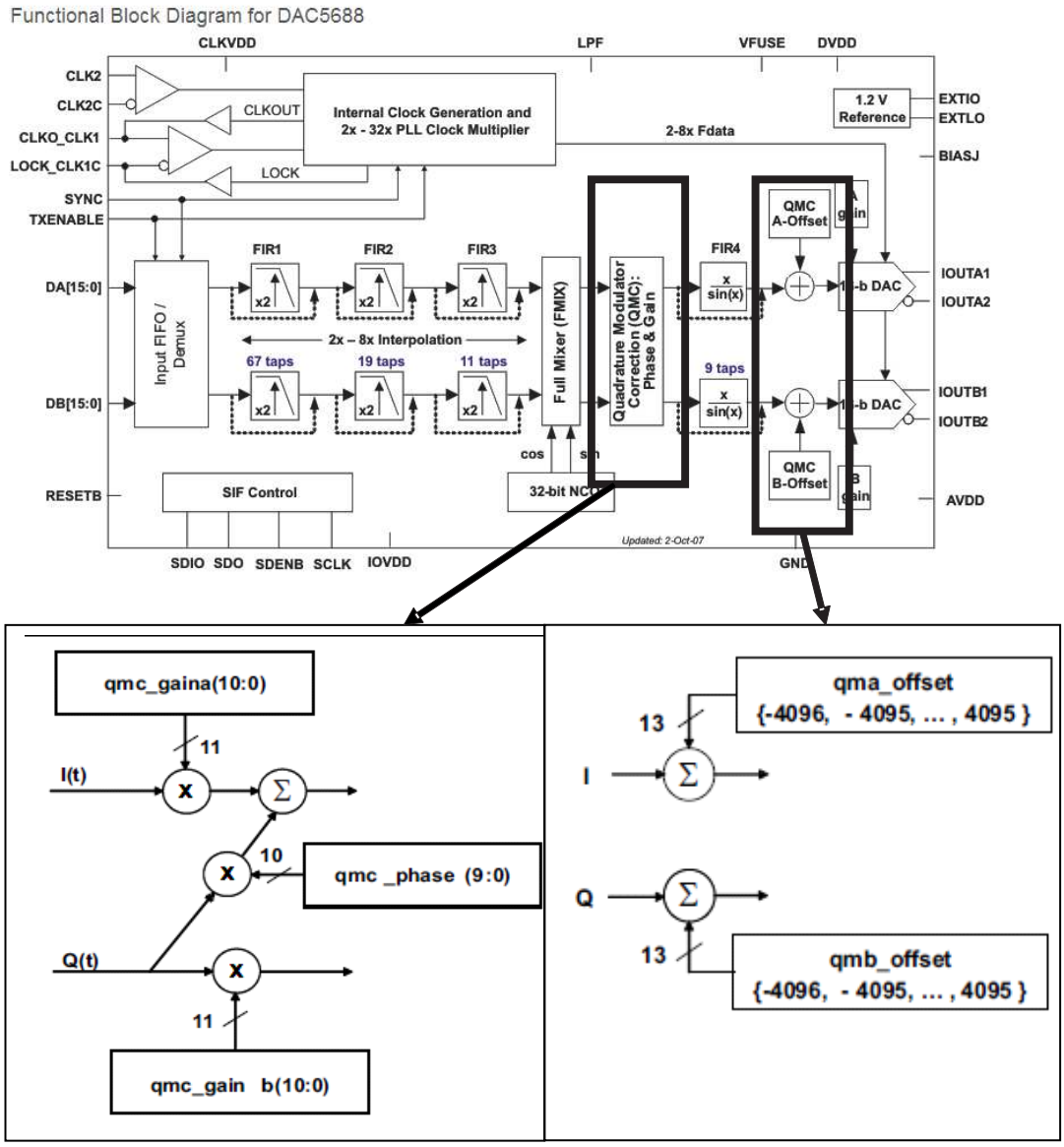


Figure 25. Quadrature Modulator, Common Source of Errors

The goal of the QMC section of a DAC is to manipulate the DC, phase and gain of the DAC signal in such a way that it offsets the errors seen internal to and at the inputs of the quadrature modulator. In an ideal case QMC would remove the spurs at F_{LO} and F_{SB} in Figure 25. In practice, the QMC section has been seen to improve the carrier suppression and sideband suppression to about –70dBc.

Figure 26 shows a typical block diagram of the QMC section of a DAC. As shown in Figure 26, the QMC section provides the DAC an easy way to force offset, gain and phase errors that cancel out the errors at the quadrature modulator. Once the DC, gain and phase errors are known, programming the DAC is straightforward.



QMC Gain and Phase Correction **QMC Offset - DC Correction**

Figure 26. DAC5688 Block Diagram – QMC Functions

These DC, offset and phase errors can drift with phase, temperature and time. In an ideal case the application would have a real time measurement system that could measure these errors and program the DAC to correct these errors. However, a system like this adds complexity and cost to the system design. At the time of this document, most end users manually calibrated their systems QMC values at time zero and 25°C only. A few end users calibrated their systems QMC values at time zero and several temperatures. The values for QMC correction values are then stored in an EEPROM and written to the DAC via DSP or FPGA when the system is in the field.

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