参考資料

TI Designs: TIDA-010036
スタンドアロン ADC を使用する単相シャント電気メーターのリファレンス・デザイン

概要

このリファレンス・デザインは、スタンドアロンのマルチ・チャネル・アナログ/デジタル・コンバータ (ADC) を使用してシャント電流センサをサンプリングする、Class 0.5 単相電力量測定を実装します。シャント・センサと、磁気耐性を持つ小型の電源との組み合わせにより、このデザインは磁気的な改変攻撃からの保護を行います。また、このデザインには中立線切断による改変の可能性を検出する機能もあります。高性能の ARM® Cortex®-M4 MCU による度量衡計算と、8kHz のサンプリング・レートの組み合わせにより、個別の高調波の分析など、電力品質に関する追加機能も実現可能です。

リソース

TIDA-010036	デザイン・フォルダ
ADS131M04	プロダクト・フォルダ
TPS7A78	プロダクト・フォルダ
MSP432P4111	プロダクト・フォルダ
TPS3840	プロダクト・フォルダ
THVD1500	プロダクト・フォルダ
ISO7731B	プロダクト・フォルダ
TRS3232E	プロダクト・フォルダ

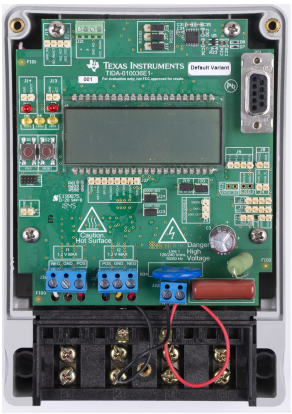
TI E2E™ Community　E2E™エキスパートに質問

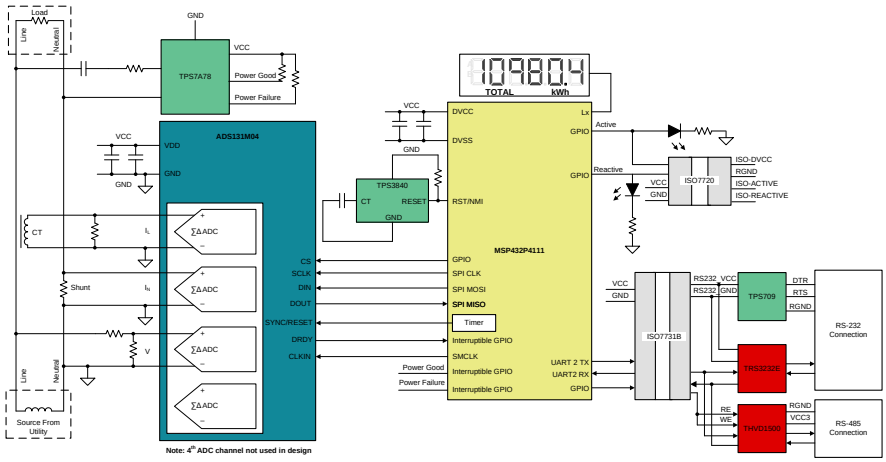
特長

- Class 0.5 の単相計測を 50mA～90A の入力範囲で試験済み
- 有効/無効電力量および電力、RMS ライン電流、RMS 中性電流、RMS 電圧、力率、ライン周波数などのパラメータを計算
- 低消費電力の電流検出モードにより、改変攻撃の可能性を検出
- パワー・グッド表示と電源障害アラートを搭載した小型の非磁性電源
- $5kV_{RMS}$ 絶縁の RS-485 および RS-232 インターフェイス

アプリケーション

- 電気メーター





1 System Description

1.1 End Equipment

1.1.1 Electricity Meter

Each year, billions of dollars are lost by utilities due to nontechnical losses. One form of nontechnical loss for electricity utility providers is electricity meter tampering, where individuals hack meters to slow or stop the accumulation of energy usage statistics, thereby stealing electricity. One of the most common ways someone tries to tamper with an electricity meter is to apply a magnet on it. This magnet paralyzes transformers in power supplies as well as current transformer current sensors, thereby enabling electricity theft. Since magnets can affect current transformers(CT), shunts are often used as a current sensor for one-phase meters. The output voltage produced by shunts at low currents is small, especially when compared to the output voltage produced by current transformers over the same low input current range. As a result, for shunt-based high-accuracy meters, an accurate ADC is needed to sense the low output voltages from shunts to accurately bill utility customers.

In addition to ensuring accurate customer billing, it is the responsibility of the utility company to guarantee good power quality to their customers. However, it is possible for current harmonics from a utility customer's load to induce voltage harmonics, which may effect multiple utility customers. By performing harmonic analysis, utility providers may be able to identify customer loads that negatively impact power quality. Adding harmonic analysis capabilities to an electricity meter may require an increase in the sample rate of the meter to capture the desired frequency range. The increase in sample frequency many times has to be done without compromising on accuracy or even while simultaneously increasing accuracy. The high sample rate, in turn, also requires more processing.

As the accuracy and amount of processing expected from electricity meters increases, it becomes more difficult to find a metrology SoC that fulfills both the processing and accuracy requirements of an electricity meter. To address this limitation, a standalone ADC can be used with a host microcontroller (MCU) to simultaneously overcome the processing and accuracy limitations of electricity meter SoCs. Using an accurate standalone ADC typically has the following advantages:

- It enables meeting the most stringent of accuracy requirements

- It enables meeting minimum sample rate requirements(without compromising on accuracy) that may not be obtainable with applications-specific products or metrology SoCs
- It enables flexibility in selecting the host MCU since you are not limited to selecting host MCUs that have accurate ADCs. The host MCU can be selected solely based on application requirements, such as processing capability, minimum RAM and Flash storage for logging energy usage, and MCU security features for ensuring meter data security.

In this reference design, Class 0.5 one-phase shunt-based energy measurement is implemented by using a standalone ADC device. The standalone ADC senses the Mains voltage and current. For sensing the current, the design measures both the line and neutral current by using a shunt and CT. By measuring both currents, metrology parameters can be properly sensed in case someone tries to tamper with the meter by bypassing the sensed line or neutral current in an attempt to have the meter register a smaller energy consumption than what is actually consumed.

When there are new ADC samples available from the standalone ADC, the host MCU communicates to the standalone ADC using SPI to get the new samples. The host MCU uses the new ADC samples from the standalone ADC to calculate metrology parameters. In addition to calculating the metrology parameters, the host MCU also drives the liquid crystal display (LCD) of the board and communicates to a personal computer (PC) graphical user interface (GUI) through either the isolated RS-232 circuitry or isolated RS-485 circuitry on the board. As an additional safeguard, an external SVS device is added to the design to reset the host MCU when the supplied voltage to power the host MCU is not sufficient. In general, using an external SVS provides more security than the internal SVS on a host MCU.

In this design, the test software specifically supports calculation of various metrology parameters for one-phase energy measurement. These parameters can be viewed either from the calibration GUI or LCD. The key parameters calculated during energy measurements are:

- Active, reactive, apparent power and energy
- RMS line current, RMS neutral current, and RMS voltage
- Power factor
- Line frequency

In addition to affecting current transformer current sensors, magnetic tampering could affect a transformer in the power supply as well. To deal with magnetic tamper attacks affecting the power supply of the meter, one option is to use cap-drop supplies, which do not use a magnetically-susceptible transformer. However, one disadvantage of cap-drop supplies is their small maximum output current. To increase the maximum output current from a cap-drop supply without increasing the capacitor size of the power supply, a buck converter could be used with the cap-drop supply instead of the LDO that is used in traditional cap-drop supplies; however, using a buck converter would require adding an inductor, which may be affected, like a CT, by an external magnet. In this design, an AC voltage regulator is used to create a compact, cap-drop power supply that can provide more output current than conventional cap-drop supplies without having to use magnetic components, thereby making the power supply magnetically immune.

Another technique used to tamper with an electricity meter is to remove the neutral wire from the meter. If the neutral is disconnected, the voltage measured is 0 V, which in turn leads to a 0 W measured value for the active power. With the neutral missing, the main AC/DC is not functional so a backup power supply like a battery or powering CT must be used to power the meter. For this tamper technique, although the active power reading is 0 W because of the 0 V reading, there is still current flowing through the line wire that could be sensed. The standalone ADC used in this design has a current-detection mode that could be used to detect the presence of current for this tamper scenario. In this mode, the ADC runs off an internal

oscillator and provides an interrupt to the MCU if a user-configurable number of samples have surpassed a user-defined ADC threshold value, which may indicate tampering. Since the ADC is doing this current detection, the MCU can enter a sleep mode until it is alerted that current has been detected by the standalone ADC. This current-detection mode is low-power, which allows the mode to be entered periodically without significantly draining the backup power supply that the meter is running on. The AC/DC power supply of the design provides an early alert of AC supply failure, which can be either be from an actual power outage condition or from the removal of the neutral connection, so that the standalone ADC could be triggered to enter this current-detection mode. When the meter sees AC mains again after power has been restored from a power outage, the AC/DC in the design provides an alert that can be used to exit current-detection mode.

1.2 Key System Specifications

表 1. Key System Specifications

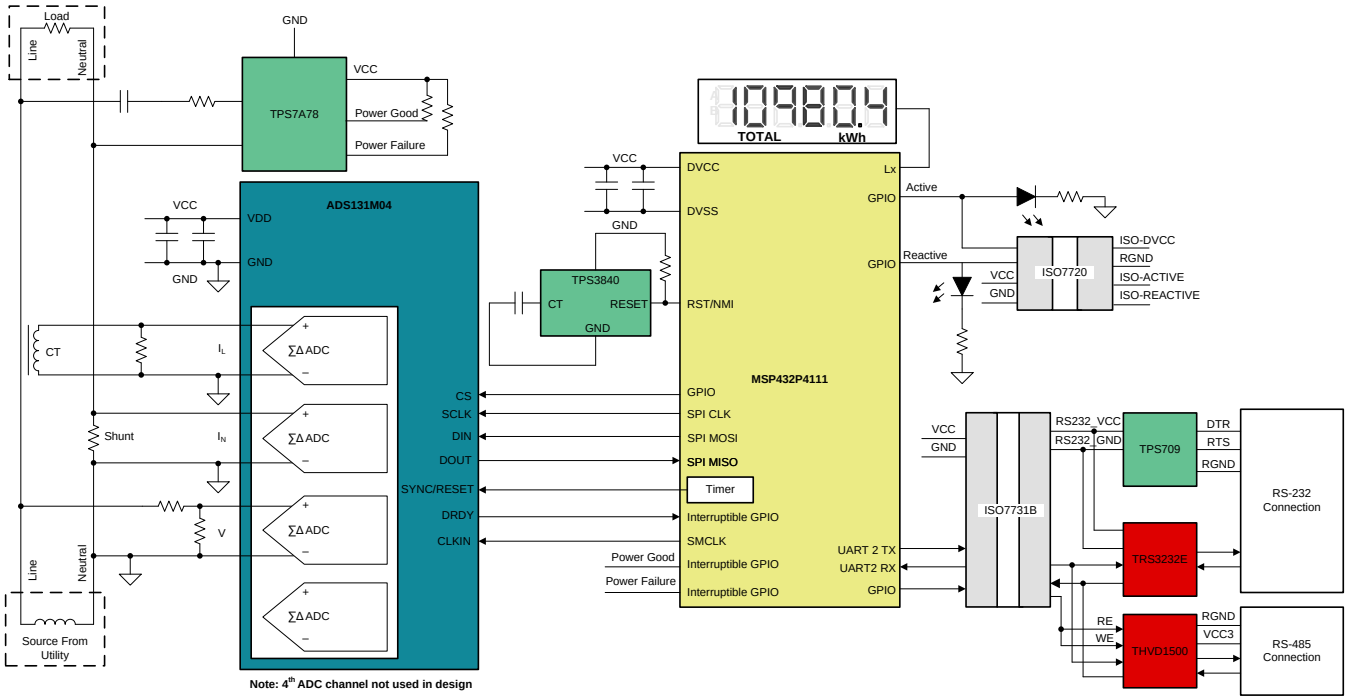
FEATURES	DESCRIPTION
Number of phases	1
Electricity meter accuracy class	Class 0.5
Current sensor	Shunt, current transformer
Tested current range	0.05–90 A
ADS131M04 CLKIN frequency	8,192,000 Hz
ADS131M04 delta-sigma modulation clock frequency	4,096,000 Hz (= CLKIN / 2)
SPI Clock	8,192,000 Hz
Oversampling ratio (OSR)	512
Digital filter output sample rate	8,000 samples per second
Phase compensation implementation	Software
Phase compensation resolution	0.0088° at 50 Hz or 0.0105° at 60 Hz
Selected CPU clock frequency	48 MHz
MCU external SVS voltage	2.0–2.1 V
System nominal frequency	50 or 60 Hz
Measured parameters	• Active, reactive, apparent power and energy • Root mean square (RMS) line current, neutral current, and voltage • Power factor • Line frequency
Update rate for measured parameters	Approximately equal to 1 second
Communication options	• LCD • PC GUI via 5-kV_{RMS} isolated RS-232 or isolated RS-485
Utilized LEDs	Active energy and reactive energy
Board power supply	Option 1: Power derived from AC mains using cap-drop supply Option 2: External power

2 System Overview

2.1 Block Diagram

図 1 depicts a block diagram that shows the high-level interface used for an ADS131M04-based one-phase energy measurement application.

図 1. TIDA-010036 Block Diagram



In 図 1, a simple voltage divider is used for translating the Mains voltage to a voltage that can be sensed by the ADC. For the current, two current sensors are used, where one current sensor is used for sensing the line current and another current sensor is used to sense the neutral current. The design uses a shunt and a current transformer for the current sensors. In 図 1, the system shows that the CT measures the line current, the shunt measures the neutral current, and the system is referenced with respect to the neutral; however, the design also supports a second configuration where the CT measures the neutral current, the shunt measures the line current, and the system is referenced with respect to the line.

For the shunt current sensor, the resistance of the shunt is selected based on the current range required for energy measurements and also the minimization of the maximum power dissipation of the shunt. For the CT current sensor, the CT has an associated burden resistor that must be connected at all times to protect the measuring device. The selection of the CT and the burden resistor is made based on the manufacturer and current range required for energy measurements.

The choice of voltage divider resistors for the voltage channel is selected to ensure the Mains voltage is divided down to adhere to the normal input ranges of the ADS131M04 device. Since the ADS131M04 ADCs have a large dynamic range and a large dynamic range is not needed to measure voltage, the voltage front-end circuitry is purposely selected so that the maximum voltage seen at the inputs of the voltage channel ADCs are only a fraction of the full-scale voltage. By reducing the voltage fed to the ADS131M04 voltage ADC, voltage-to-current crosstalk, which actually affects metrology accuracy more than voltage ADC accuracy, is reduced at the cost of voltage accuracy.

In this design, the ADS131M04 device interacts with the MSP432™ MCU in the following manner:

1. The CLKIN clock used by the ADS131M04 device is provided from the SMCLK clock signal output of the MSP432 MCU.
2. The ADS131M04 device divides the clock provided on its CLKIN pin by two and uses this divided clock as its delta-sigma modulation clock.
3. When new ADC samples are ready, the ADS131M04 device asserts its $\overline{\text{DRDY}}$ pin, which alerts the MSP432 MCU that new samples are available.
4. After being alerted of new samples, the MSP432 MCU uses one of its SPI interfaces and its DMA to get the voltage and current samples from the ADS131M04 device.

In this design, a TPS3840 device is used as an external SVS for the MSP432 MCU. Although the MSP432 MCU has an internal SVS that suffices for this application, the TPS3840 standalone SVS is used because there is additional security in having an SVS that is independent of the MCU.

To power this design, a TPS7A78 device is used to implement a cap-drop supply. This TPS7A78 device allows a higher output current than traditional cap-drop supplies. It also has a power failure pin, which can be used to alert the MCU whenever the system sees an AC supply failure either because of a power outage or if the neutral connection has been removed from the meter. The TPS7A78 has a power good pin, which can be used to alert the MCU that the output voltage of the cap-drop supply has ramped up after power has been restored from a power outage.

Other signals of interest in 図 1 are the active and reactive energy pulses used for accuracy measurement and calibration. The ISO7720 device provides an isolated connection for these pulses for connecting to non-isolated equipment. This is especially needed if the shunt measures the line current since the system is referenced to this high-voltage line connection as well for this configuration.

In addition to isolated pulses, the design supports isolated RS-232 communication through the use of the TPS70933, ISO7731B, and TRS3232E devices. The design can be configured to use RS-485 as well instead of RS-232 through the use of the ISO7731B and THVD1500 devices on the board.

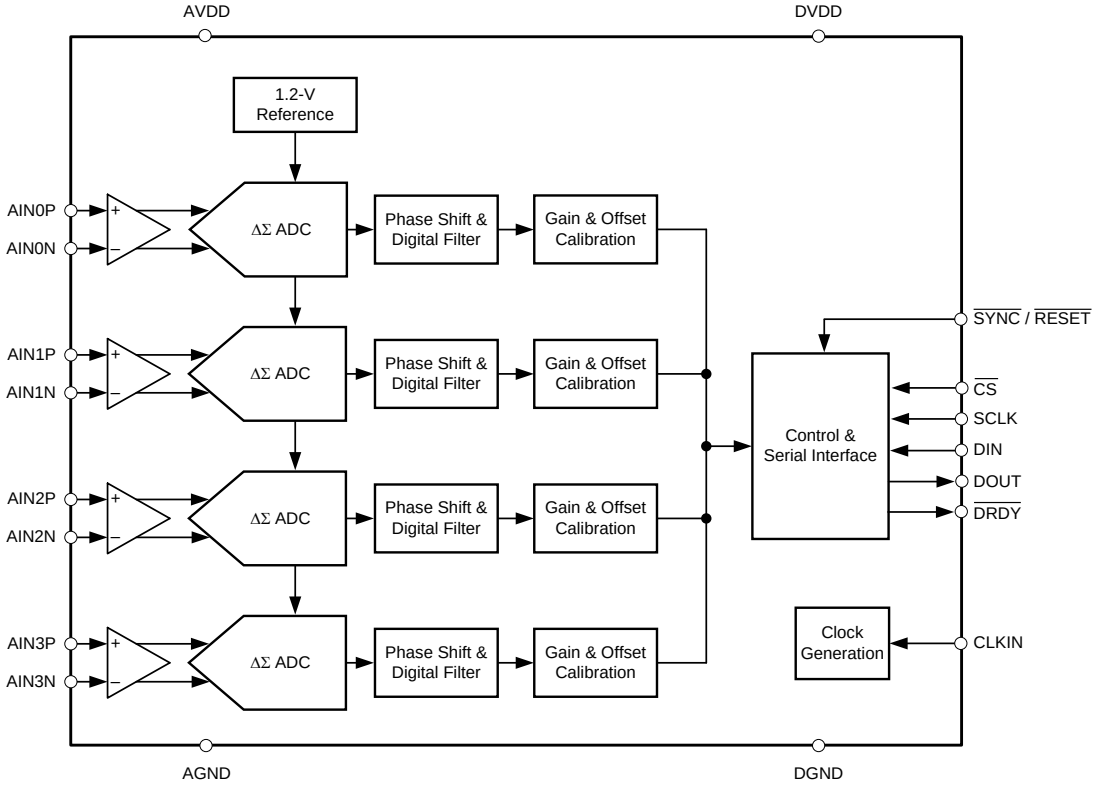
2.2 Highlighted Products

2.2.1 ADS131M04

The ADS131M04 device is a four-channel, simultaneously-sampling, 24-bit, 2nd order delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range, and internal calibration features making it well-suited for energy metering, power quality, and protection applications. The ADC inputs can be directly interfaced to a resistor-divider network, a transformer to measure voltage or current, a shunt to measure current, or a Rogowski coil to measure current.

The individual ADC channels can be independently configured depending on the sensor input. A low noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals. Additionally, these devices integrate channel-to-channel phase alignment and offset and gain calibration registers to help remove signal chain errors. A low-drift, 1.2-V reference is integrated into the device reducing printed circuit board (PCB) area. Cyclic redundancy check (CRC) options can be individually enabled on the data input, data output, and register map to ensure communication integrity. 図 2 shows a block diagram of this device.

図 2. ADS131M04 Functional Block Diagram



In 図 2, 2.7 V–3.6 V must be fed between AVDD and AGND as well as between DVDD and GND. In addition, an external clock must be connected to CLKIN. When the ADS131M04 device is configured for high-resolution mode, this clock must be between 1 MHz and 8.3 MHz for the ADS131M04 to properly work. The CLKIN clock of the ADS131M04 device can be generated from the SMCLK clock output of the MSP432 MCU. The ADS131M04 divides this clock by two and uses this divided clock for its delta-sigma modulator clock. When new ADC samples are ready, the ADS131M04 asserts its $\overline{\text{DRDY}}$ pin to alert the host MCU that there are new ADC samples available. Since the ADS131M04 device can accept a clock with a wide frequency range, the device itself can also be used for applications that require coherent sampling.

2.2.2 TPS7A78

The TPS7A78 device improves the overall efficiency and standby power in power supplies for an easy-to-use non-magnetic approach to AC/DC conversion. The TPS7A78 device uses an external capacitor to create a current source and actively clamps the rectified voltage. The device then regulates the voltage down to the application-specific operating voltage. The unique architecture of the device allows the standby power to be reduced from several 100s of milliwatts to just a few 10s of milliwatts. The TPS7A78 device takes advantage of an innovative switched capacitor stage to reduce the clamped voltage down by approximately 1/4th of the value, which in turn multiplies the current by 4. Thus, the current source capacitor can be much smaller in size, which minimizes standby power, reduces solution size, and can lead to a lower system cost.

The TPS7A78 device is optimized for electricity meters where the power supply must be reliable and magnetic tamper-proof. The TPS7A78 device requires no external magnetics, which makes complying with IEC 61000-4-8 and any magnetic tampering tests easier while minimizing costly magnetic shielding.

Additionally, the TPS7A78 also comes with a user programmable power-fail detection threshold that can provide an early alert to AC supply failures so the system can save data before losing main power and then enter a low-power mode before switching to a backup power supply. A power-good indication on the TPS7A78 can be used to alert the system that power has returned so that the system could exit low power mode and resume normal operation.

2.2.3 MSP432P4111

The SimpleLink™ MSP432P4111 MCUs are optimized MCUs that deliver ultra-low-power performance with FPU and DSP extensions. This device has an ARM® Cortex®-M4F 32-bit CPU with floating-point unit and memory protection unit, a real-time clock, LCD driver, port mappable GPIOs, an AES encryption and decryption accelerator, and multiple serial communication options. The MSP432P4111 microcontroller is part of the SimpleLink MCU platform, which consists of Wi-Fi®, *Bluetooth*® low energy, sub-1 GHz, and host MCUs. All of these devices share a common, easy-to-use development environment with a single-core software development kit (SDK) and rich tool set.

The MSP432 MCU in this design retrieves voltage and current samples from the ADS131M04 device and calculates metrology parameters. In addition, the device also keeps track of time with its RTC module, drives the LCD on the board with its internal LCD driver module, and uses one of its UART interfaces to communicate to a PC GUI using either the isolated RS-232 or isolated RS-485 circuit of the board. The CRC module of the MSP432 MCU is also used to accelerate the CRC calculations that are done to verify the integrity of the ADC packet sent by the ADS131M04 device.

2.2.4 TPS3840

The TPS3840 family of voltage supervisors or reset ICs can operate at high voltage levels while maintaining very low quiescent current across the whole VDD and temperature range. The TPS3840 device offers the best combination of low power consumption, high accuracy, and low propagation delay.

The reset output signal of the device is asserted when the voltage at VDD drops below the negative voltage threshold (V_{IT-}) or when manual reset is pulled to a low logic ($V_{\overline{MR}\_L}$). The reset signal is cleared when VDD rises above V_{IT-} plus hysteresis (V_{IT+}) and manual reset ($\overline{MR}$) is floating or above $V_{\overline{MR}\_H}$ and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor to ground in the CT pin, for a fast reset the CT pin can be left floating. Additional features include low power on reset voltage (V_{POR}), built in glitch immunity protection for $\overline{MR}$ and VDD, build in hysteresis and low open drain output leakage current ($I_{LKG(OD)}$).

For electricity meters, some manufacturers prefer to have external SVS devices to reset any MCUs in the system, even if the MCUs already have an internal SVS. External SVS devices are sometimes preferred over using the SVS within an MCU because the external option can be more secure than the internal option, since the external devices function independently of the MCU. Although the SVS of the MSP432 MCU suffices for this application, the TPS3840 external SVS device is added to this design for an additional level of security. External SVS devices may sometimes also be used for early detection of a Mains blackout condition by monitoring one of the rails of an AC/DC powered from Mains.

In this design, the TPS3840DL20 variant is specifically used, which has a 2-V threshold and an open drain, active low output.

2.2.5 THVD1500

The THVD1500 device is a robust half-duplex RS-485 transceiver for industrial applications. The bus pins are immune to high levels of IEC Contact Discharge ESD events eliminating the need of additional system-level protection components.

The device operates from a single 5-V supply. The wide common-mode voltage range and low input leakage on bus pins make the THVD1500 device suitable for multi-point applications over long cable runs.

The THVD1500 device is available in an industry standard 8-pin SOIC package for drop-in compatibility. The device is characterized from –40°C to 125°C. The device also meets or exceeds the requirements of the TIA/EIA-485A Standard and the State Grid Corporation of China (SGCC) Part 11 Serial Communication Protocol RS-485 Standard.

This device is specifically used in this design to convert from UART to RS-485 signals.

2.2.6 ISO7731B

To add isolation to the RS-232 and RS-485 connection to a PC, the isolated RS-232 and isolated RS-485 portion of this reference design uses capacitive galvanic isolation, which has an inherent life span advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, the maintenance of effective isolation over a period of 15 years or longer is important.

The variant of the ISO7731B device used in the RS-232 and RS-485 circuitry of this reference design provides galvanic isolation up to 5 kV_{RMS} for one minute per UL. This digital isolator has three isolated channels where two channels are forward channels and the other is a reverse channel. In this design, two isolation channels are used for the TX and RX. If RS-485 is selected for communication, the third isolation channel is used for the control signal to enable the receiver or driver. If RS-232 is selected, the third isolation channel is not needed. If RS-232 is desired in a customer's system instead of RS-485, only two isolation channels are needed, so a two-channel ISO7721B device could be used to reduce cost instead of using the three-channel ISO7731B device (keep in mind that these two devices are not pin-to-pin compatible). Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. This chip supports a signaling rate of 100 Mbps. The chips can operate from a 2.5 V, 3.3-V, and 5-V supply and logic levels.

2.2.7 TRS3232E

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232E device. The TRS3232E device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/µs driver output slew rate.

2.2.8 TPS709

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this reference design uses the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 V to 12 V, depending on the driver implementation. The 5 V to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 device is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

The TPS70933 linear regulator is an ultra-low quiescent current device designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy overtemperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA (typical).

2.2.9 ISO7720

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC. The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. The ISO7720 device has both channels in the same direction while the ISO7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x family of devices is available in 16-pin SOIC wide-body (DW) and 8-pin SOIC narrow-body (D) packages.

To test the active energy and reactive energy accuracy of a meter, pulses are output at a rate proportional to the amount of energy consumed. A reference meter can then determine the accuracy of the electricity meter by calculating the error based on these pulses and how much energy is provided to the meter. In this reference design, pulses are output through headers for the cumulative active and reactive energy consumption. Using the ISO7720 device provides an isolated version of these headers for connection to non-isolated equipment, which is especially needed when the design is referenced with respect to line. In this design, the D package of the ISO7720 device is used, which provides an isolation voltage of 3000 V_{RMS} for these signals. These isolated active and reactive signals can be set to have either a 3.3- or 5-V maximum voltage output by applying the selected maximum voltage output between the VCC (ISO_VCC) and GND (ISO_GND) of the isolated side.

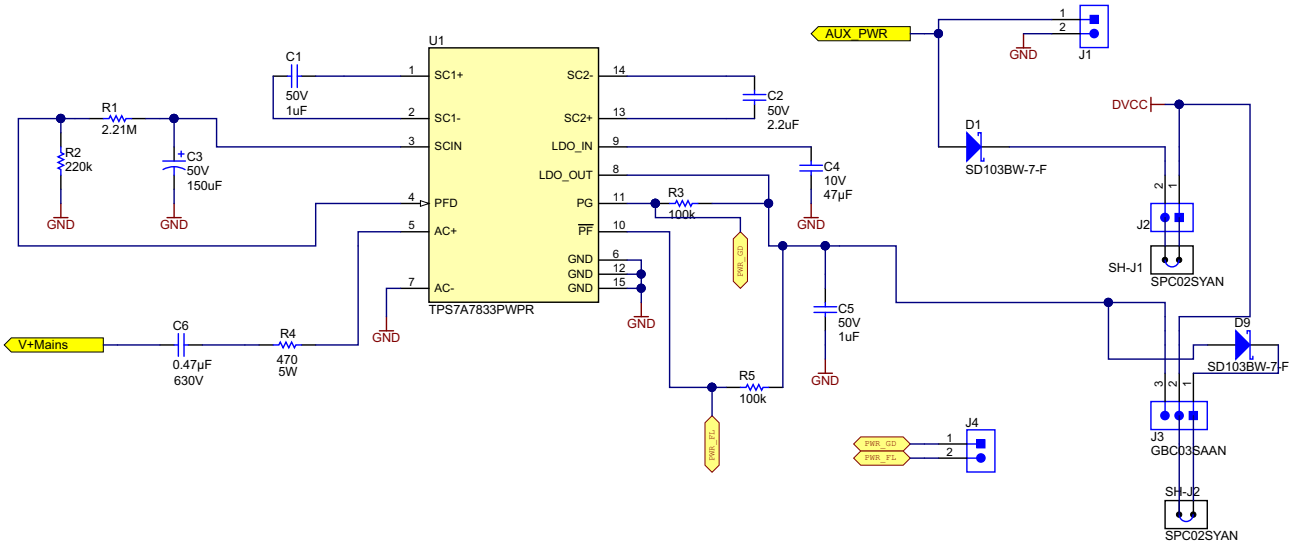
2.3 Design Considerations

2.3.1 Design Hardware Implementation

2.3.1.1 TPS7A78 Cap-Drop Supply

This design uses a TPS7A78 device to create a cap-drop supply with a larger maximum output current than conventional cap-drop LDO-based power supplies without using magnetic components. 図 3 shows the circuit used in this design to implement the cap-drop supply. The *TPS7A78 120-mA, Smart AC/DC Linear Voltage Regulator* data sheet has details on how to select the optimal values of the components shown in 図 3 for various system requirements.

図 3. TPS7A78 Cap-Drop Supply Circuit



In 図 3, capacitor C6 is the high-voltage capacitor that determines the maximum output current possible with this cap-drop supply. Resistor R4 is a resistor that is used to limit the inrush current to the TPS7A78 device. This resistor can be used to protect the device from surge currents in conjunction with transient voltage suppressor (TVS) or a metal-oxide varistors (MOV). If the design is selected to be referenced with respect to neutral, "V+Mains" in 図 3 is connected to the line through resistor R29 (shown in 図 4), and GND is connected to the neutral through resistor R37 (also shown in 図 4). If the design and shunt is selected to be referenced with respect to line instead, GND in 図 3 is connected to the line through resistor R29 (shown in 図 4) and "V+Mains" is connected to the neutral through resistor R37 (also shown in 図 4). In this design, note that R29 and R37 can be replaced with ferrite beads for EMI suppression instead of using the 0-Ω resistors currently populated in the design.

The TPS7A78 device uses an internal active clamp instead of using the external Zener diodes typically used in traditional cap-drop supplies. In addition, the device uses a 4:1 switch-cap stage that divides the clamped voltage by 4, which multiplies the current by 4. As a result, you are able to get a larger output current than conventional cap-drop supplies without having to use magnetic components. The larger output current from the TPS7A78 enables getting more output current from the same capacitor size used in a conventional cap-drop supply, or decreasing the capacitor size to get the same maximum output

current as a conventional cap-drop supply, or both. The increased output current allowed by a TPS7A78-based cap-drop supply enables the maximum output current from the power supply to be designed so that it is sufficiently greater than the maximum current consumption of the system, which ensures that the cap-drop supply can still power the meter, even if the value of the capacitor decreases slightly over time. In this design, a 470-nF capacitor is used, which allows powering loads up to 50 mA.

The TPS7A78 device also has an integrated power-fail indication that can be used for an alert of a potential power outage so that the MCU can take any final actions. The power fail indication is done at the input of the switch-cap stage, which allows an early detection of a power failure. The power failure threshold is set using a resistor divider between the SCIN pin, PFD pin, and ground of the TPS7A78 device. In this design, this power failure indication is used to put the ADS131M04 device in current-detection mode before the system is switched to being powered from the backup supply. This design has support for a backup supply, such as a battery, by connecting the negative terminal of the backup supply to pin 2 of J1 in 図 3 and its positive terminal to pin 1 of J1. If a backup power supply is used in this design, an OR of the TPS7A78 output and the backup battery has to be implemented, which can be done with diodes D1 and D9, as 図 3 shows. Note that using diodes to OR the two power supplies results in a voltage drop; however, to reduce the effect of a reduced output voltage, the 3.3-V TPS7A7833 variant used in this design can be replaced with the higher voltage TPS7A7836 3.6-V variant to offset the drop-in voltage from the diode. In this design, it is assumed that the TPS7A78 output voltage is higher than the voltage of the backup supply so that the design is powered from the TPS7A78 when AC Mains is available. If the voltage of the backup supply was larger than the TPS7A78 device, then the design is powered from the backup supply even if AC Mains is available.

In addition to a power-failure indication, the TPS7A78 device has a power good indication, which is asserted when the voltage at the output of the LDO is greater than 90% of the desired LDO output voltage. This power good indication is used to inform the system when power has returned after an outage, which alerts the MCU to tell the ADS131M04 to exit current-detection mode. The TPS7A78 also integrates an LDO on the output stage of the switched cap to regulate V_{OUT} and attenuate ripple.

The reduced capacitor size allowed by the TPS7A78 and the TPS7A78 integrated active clamp, integrated LDO, integrated power failure indication, and integrated power good indication reduces the PCB size taken by this cap-drop supply compared to conventional cap-drop supplies.

2.3.1.2 TPS3840 SVS

The TPS3840 device is an external supply voltage supervisor (SVS) that is used to externally reset the MSP432 MCU. The TPS3840 maintains very low quiescent current, which enables this device to still be used if there is a power outage and the meter is running from a backup battery. The MSP432 MCU has an internal SVS device that can be used as well, which will suffice for this application; however, using an external SVS instead of the internal SVS of the MCU adds an additional layer of security since it is not independent of the MCU, and therefore, is less affected by any issues that affect the MCU itself.

In this design, the TPS3840DL20 device variant is specifically used, which has a negative-voltage threshold voltage of 2 V. When the voltage rail that powers the MSP432 MCU drops below 2 V, the TPS3840 device resets the MSP432 MCU. When the monitored voltage rises above the undervoltage threshold plus hysteresis voltage value (approximately equal to 2.1 V total) , the RESET pin of the TPS3840 is pulled back high after a user-defined reset delay time, t_D, elapses. t_D is determined based on the value of the capacitor connected to the CT pin of the TPS3840 device. In this design, a 0.33-µF capacitor is connected to the CT pin of the TPS3840 device, which leads to a reset delay time of about 204 ms.

The TPS3840 device is available with both push-pull and open-drain outputs. The open-drain output is specifically selected for this design since a 47-kΩ pullup resistor is recommended in the JTAG circuitry of the MSP432 MCU.

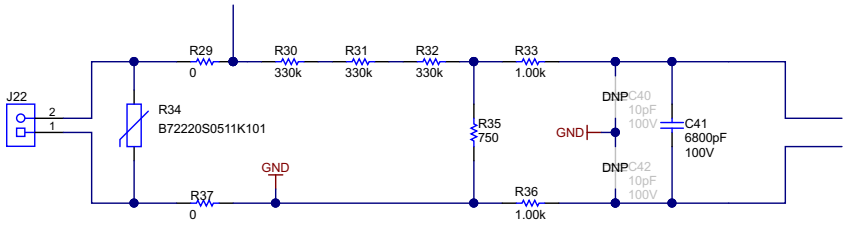
2.3.1.3 Analog Inputs

The analog front end in this design consists of the ADS131M04 delta-sigma standalone ADC. Each of the ADS131M04 converters is differential and requires that the input voltages at the pins does not exceed ±1.2 V (gain = 1). To meet this input voltage specification, the current and voltage inputs must be divided down. In addition, the ADS131M04 device can sense voltages down to −1.2 V; therefore, AC signals from mains can be directly interfaced without the need for level shifters. This subsection describes the analog front end used for voltage and current channels.

2.3.1.3.1 Voltage Measurement Analog Front End

The nominal voltage from the mains is from 100 V–240 V so it needs to be scaled down to be sensed by an ADC. 図 4 shows the analog front end used for this voltage scaling. J22 is where the voltage is applied.

図 4. Analog Front End for Voltage Inputs



In the analog front end for voltage, there consists a spike protection varistor (R34), footprints for electromagnetic interference filter beads (resistor footprints R29 and R37) , a voltage divider network (R30, R31, R32, and R35), and an RC low-pass filter (R33, R36, C40, C41, and C42).

At lower currents, voltage-to-current crosstalk affects active energy accuracy much more than voltage accuracy. To maximize the accuracy at these lower currents, in this design the entire ADC range is not used for voltage channels. Since the ADCs of the ADS131M04 device are high-accuracy ADCs, using the reduced ADC range for the voltage channels in this design still provides more than enough accuracy for measuring voltage. 式 1 shows how to calculate the range of differential voltages fed to the voltage ADC channel for a given Mains voltage and selected voltage divider resistor values.

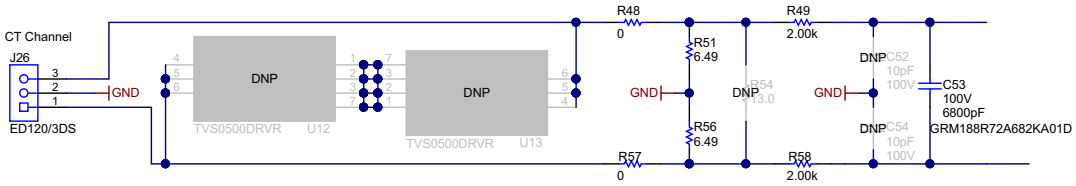
$$V_{ADC\_Swing,Voltage} = \pm V_{RMS} \times \sqrt{2} \left(\frac{R_{35}}{R_{30} + R_{31} + R_{32} + R_{35}} \right) \quad (1)$$

Based on this formula and the selected resistor values in 図 4, for a mains voltage of 230 V, the input signal to the voltage ADC has a voltage swing of ±246 mV (181 mV_{RMS}). The ±246-mV voltage range is well within the ±1.2-V input voltage that can be sensed by the ADS131M04 device for the selected PGA gain value of 1 that is used for the voltage channel.

2.3.1.3.2 Current Measurement Analog Front End

The analog front end for current inputs is different from the analog front end for the voltage inputs. 図 5 shows the analog front end used for the CT current channel, where the positive and negative leads from a CT are connected to pins 3 and 1 of header J26.

図 5. Analog Front End for CT Current Inputs



The analog front end for current consists of footprints for electromagnetic interference filter beads (R48 and R57), burden resistors for current transformers (R51 and R56), and an RC low-pass filter (R49, R58, C52, C53, and C54) that functions as an anti-alias filter. There are also footprints (U12 and U13) that can be replaced with the TVS0500 for supplemental protection from surges, if required.

As 図 5 shows, resistors R51 and R56 are the burden resistors, which are in series with each other. For best THD performance, instead of using one burden resistor, two identical burden resistors in series are used with the common point being connected to GND. This split-burden resistor configuration ensures that the waveforms fed to the positive and negative terminals of the ADC are 180 degrees out of phase with each other, which provides the best THD results with this ADC. The total burden resistance is selected based on the current range used and the turns ratio specification of the CT (this design uses CTs with a turns ratio of 2000). The total value of the burden resistor for this design is 12.98 Ω.

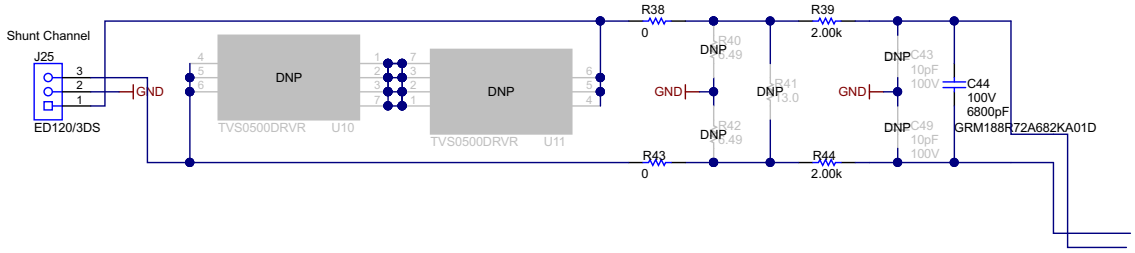
式 2 shows how to calculate the range of differential voltages fed to the current ADC channel for a given maximum current, CT turns ratio, and burden resistor value.

$$V_{ADC_{Swing},Current,CT} = \pm \frac{\sqrt{2}\left(R_{51} + R_{56}\right) I_{RMS,max}}{CT_{TURNS\_RATIO}} \quad (2)$$

Based on the maximum current of 100 A, CT turns ratio of 2000, and burden resistor of 12.98 Ω of this design, the input signal to the current ADC has a voltage swing of ±918 mV maximum (649 mV_{RMS}) when the maximum current rating of the meter (100 A) is applied. This ±918-mV maximum input voltage is well within the ±1.2-V input range of the device for the selected PGA gain of 1 that is used for the current channels.

図 6 shows the analog front end used for the shunt current channel, where the positive and negative leads from the shunt are connected to pins 1 and 3 of header J25. The ground connection for the shunt is connected to pin 2 of this J25 header.

図 6. Analog Front End for Shunt Current Inputs



The circuitry in 図 6 is similar to the circuit shown for the CT channel, except the R51 and R56 burden resistors are now removed since a shunt is used instead of a CT. **Since the burden resistors have been removed, do not connect a CT to this channel because it may cause a large output voltage that may damage the meter.** In addition, note that the pin order of the AINxP and AINxN pins on the ADS131M04 device is swapped when going from one converter to another. As an example, AIN1N is pin 5 and AIN1P is pin 6, but AIN2P is pin 7 and AIN2N is pin 8. The swapped order is why the order of the CT positive output terminal and negative output terminal on J26 is swapped when compared to the shunt positive and negative output terminal on J25.

式 2 shows how to calculate the range of differential voltages fed to the current ADC channel for a given maximum current and shunt value.

$$V_{ADC_{Swing},Current,Shunt} = \pm\sqrt{2}\left(R_{shunt}\right)I_{RMS,max} \quad (3)$$

With shunt current sensors, the shunt sensor value is selected based on the tradeoff between accuracy and shunt power dissipation. If the shunt value is decreased, less power is dissipated through the shunt; however, the decreased shunt value means a smaller output voltage from the shunt, which leads to worse accuracies at lower currents, even if a higher PGA gain is used to boost the shunt output. In this design, tests are performed with both 100- and 200-μΩ shunts.

Based on the $V_{ADC,shunt}$ range, select the proper PGA gain by looking at the full-scale range table in 表 2 to find the two gain ranges that $V_{ADC,shunt}$, shunt voltage fits between. From these two gain values, select the lower gain setting as the selected PGA gain value for the shunt channel. This gain value maximizes the ADC range without saturation occurring at higher currents. As an example of this process, suppose a 100-A maximum RMS current and a 200-μΩ shunt is used. Based on these values, $V_{ADC,shunt}$ varies between ±28.3 mV. This voltage range is between the maximum ±37.5 mV voltage at a gain of 32 and ±18.75 mV at a PGA gain of 64 so the PGA gain setting of the shunt channel is set for 32.

表 2. Full-Scale Range

GAIN SETTING	FSR
1	±1.2 V
2	±600 mV
4	±300 mV
8	±150 mV
16	±75 mV
32	±37.5 mV
64	±18.75 mV
128	±9.375 mV

2.3.2 Current-Detection Mode

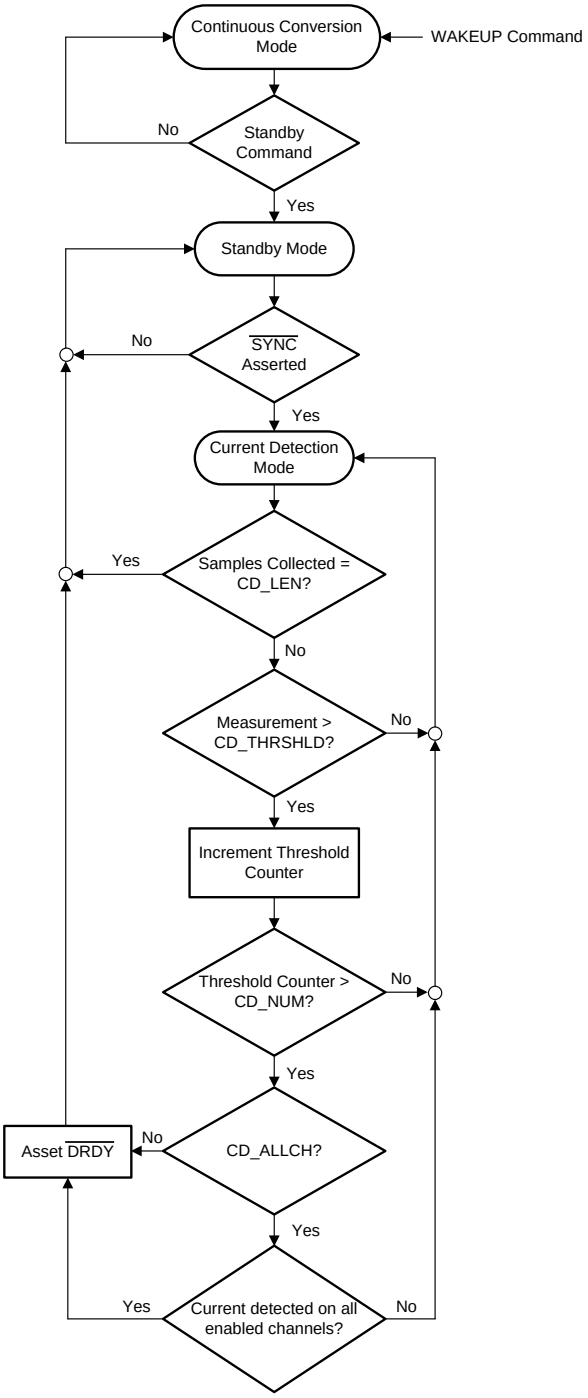
One technique used to tamper with the meter is to remove the neutral connection. If the neutral is disconnected, the RMS voltage and active power cannot be measured. In addition, the main AC/DC power supply is not functional so a backup power supply, such as a battery, must be used to power the meter. For this tamper technique, although the active power reading may be 0 W from not being able to measure voltage, there is still current flowing through the line wire. The presence of this line current can be used to distinguish a power outage event from someone removing the neutral connection of the meter.

The ADS131M04 device has a current-detection mode that can be used to detect the presence of this current for this tamper scenario without drawing too much current so that the lifetime of the backup battery is not significantly affected. In this mode, the ADS131M04 device collects a configurable number of samples at 2.7 kSPS using an internal oscillator and then the absolute value of the results are compared to a programmable threshold. If a configurable number of the samples within a sample window exceed a threshold, the host MCU is notified. If the ADS131M04 device is put in current-detection mode after the system detects an AC supply failure(either due to an outage or removing the neutral connection) and an interrupt is provided from the ADS131M04 device to the MCU by asserting its $\overline{\text{DRDY}}$ pin low, this can indicate that someone has tried to tamper with a meter by removing its neutral connections. Instead of only sensing tamper current on the line from the removal of the neutral, the ADS131M04 device can also be set to simultaneously detect the removal of the line connection by performing current detection on the neutral current channel.

2.3.2.1 ADS131M04 Current-Detection Procedure

図 7 shows the details of the procedure followed by the ADS131M04 device to enter current-detection mode as well as the procedure followed when in this mode.

図 7. ADS131M04 Current-Detection Mode Process

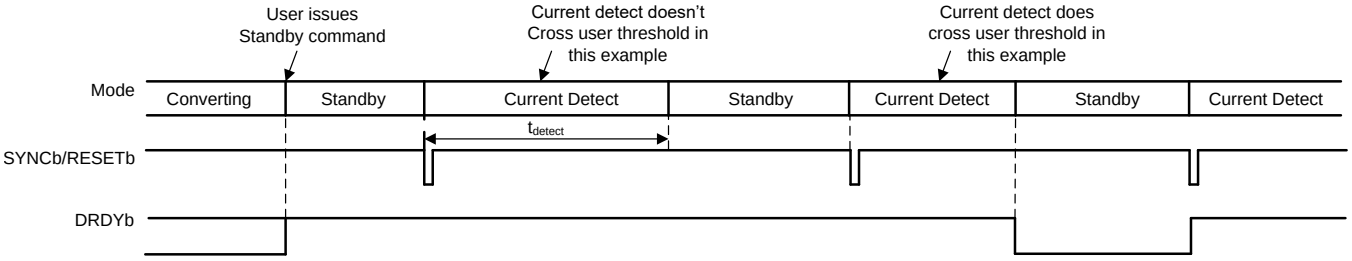


This process begins by the MCU sending a standby command to the ADS131M04 device from its normal continuous conversion mode. By sending this command, the ADS131M04 device is put in standby mode. Note that the $\overline{\text{DRDY}}$ pin should not be asserted every time a new sample is available, like it was when the device was in normal conversion mode. The $\overline{\text{DRDY}}$ pin is only asserted low when in current-detection mode if tamper current is detected. In addition, the $\overline{\text{DRDY}}$ pin is not asserted low in standby mode since the device is not converting samples.

After the device is in standby mode, provide a pulse on the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin, which enables the device to enter current-detection mode, assuming the CD_EN bit is already enabled in the corresponding ADS131M04 register. When in current-detection mode, the ADS131M04 checks to see if the absolute value of each sample is above the user-defined threshold, which is set by the CD_THRSHLD registers. If a sample is beyond the set threshold, a threshold counter for this current sampling window is incremented. After this threshold is incremented, a check is done to see if the threshold counter is above the value set by the CD_NUM bits in the corresponding ADS131M04 register. The CD_NUM bits configure the number of samples which need to exceed the threshold (CD_THRSHLD) for detection to occur. The purpose of requiring multiple samples for detection is to allow for noisy values that may exceed the threshold, but do not represent a high enough power level to warrant action by the host. If the threshold counter is greater than the value set by the CD_NUM bits, $\overline{\text{DRDY}}$ is asserted if the CD_ALLCH bit in the ADS131M04 register is set to 0 or if the CD_ALLCH bit is set to 1 and current is detected on all enabled channels. After $\overline{\text{DRDY}}$ is asserted, the device goes back to standby mode even if a full sample window has not been checked yet. If the number of samples checked equals the sample window, which is set by the CD_LEN bits in one of the ADS131M04 registers, and the threshold counter is not above CD_NUM, the device goes back to standby mode without $\overline{\text{DRDY}}$ having been asserted.

図 8 shows two example scenarios of running current-detection mode. In 図 8, more than CD_NUM number of samples are not beyond the current-detection threshold for the first time current-detection mode is triggered. As a result, the ADS131M04 device is in current-detection mode for the maximum time period. For the second time current-detection mode is triggered, more than CD_NUM number of samples are beyond the current-detection threshold, which may indicate tampering has occurred. Immediately after more than CD_NUM samples are beyond the current-detection threshold, the ADS131M04 alerts the MCU and then exits current-detection mode instead of continuing in current-detection mode until the CD_LEN number of samples has been obtained. As a result, the time spent in current-detection mode is smaller the second time the current-detection mode is triggered in this example compared to the first time current-detection mode was triggered.

図 8. ADS131M04 Current Detection Example



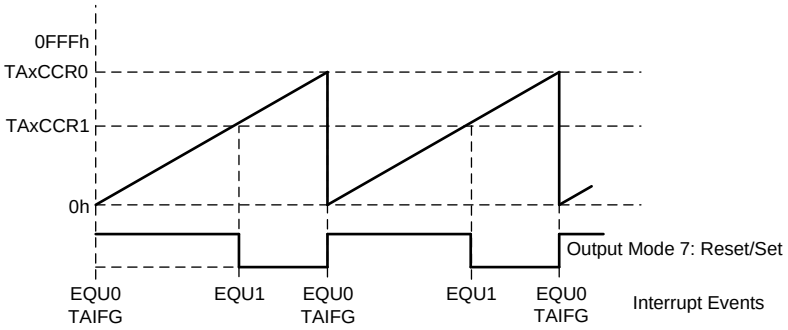
2.3.2.2 Using an MCU to Trigger Current-Detection Mode

2.3.2.2.1 Using a Timer to Trigger Current-Detection Mode Regularly

To have the ADS131M04 device enter current-detection mode regularly without CPU intervention, one option is to connect the timer output of an MCU to the $\overline{\text{SYNC}}/\overline{\text{RST}}$ pin on the ADS131M04 device. The timer can be set to have its output provide the necessary pulse to cause the ADS131M04 device to enter current-detection mode from standby mode at regular intervals. In this design, the pin connected to the ADS131M04 $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin can be port mapped to a timer output from one of the timer A modules of the MSP432 MCU. This timer can be clocked from the low-frequency crystal on the board, which enables the timer to be functional if the MSP432 MCU were to enter a low-power mode where SMCLK and its CPU clock were disabled, thereby enabling the reduction of the system current consumption.

In this design, the timer for driving the $\overline{\text{SYNC}}/\overline{\text{Reset}}$ pin is configured to count in up-mode, where the timer counts to a value set in its TAxCCR0 register. After counting up to TAxCCR0, the timer is reset back to 0 at the next timer clock cycle. 図 9 shows the timer output connected to the $\overline{\text{SYNC}}/\overline{\text{Reset}}$ pin is set for a “reset/set” output mode. In this mode, the $\overline{\text{SYNC}}/\overline{\text{Reset}}$ pin is asserted low when the timer first counts up to the value in the TAxCCR1 register and the pin is asserted high when the timer counts back to 0 again. To enter current-detection mode immediately, the timer count is initialized with a value equal to TAxCCR1 before the timer is first started.

図 9. Timer Output Configuration



The TAxCCR0 register and the frequency of the timer sets the frequency for entering into current-detection mode. The timer A module of the MSP432 MCU has clock dividers, which are used to divide the clock source for a slower frequency timer. 式 4 shows the frequency of the timer based on the selected clock divider.

$$f_{timer} = \frac{f_{timer\_clock\_source}}{\text{total timer clock divider value}} \tag{4}$$

The time between triggers to enter current-detection mode can be calculated with 式 5:

$$t_{CD\_mode\_period} = \frac{TAxCCR0 + 1}{f_{timer}} \tag{5}$$

The duration of the time of when the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin is held low, the negative pulse width time, is also calculated as 式 6 shows:

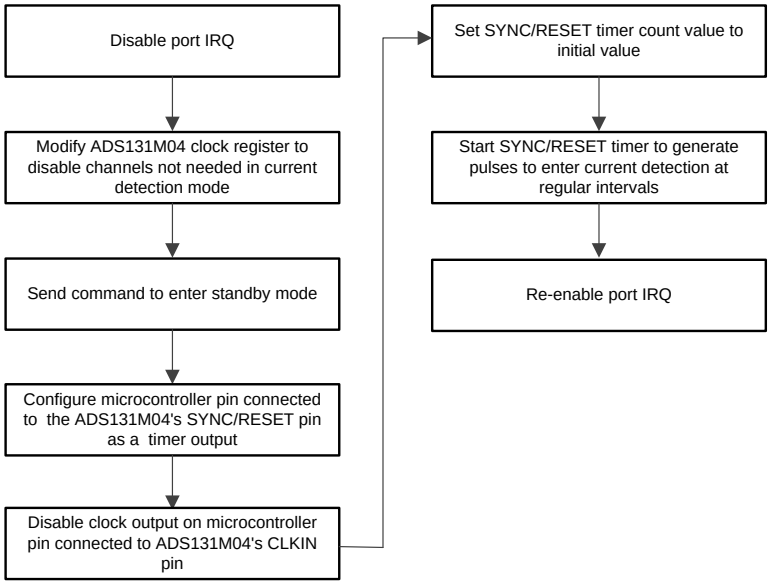
$$t_{negative\_pulse\_width} = \frac{(TAxCCR0 + 1 - TAxCCR1)}{f_{timer}} \tag{6}$$

As an example, suppose that the frequency of the timer clock source is 32,768 Hz and the values of TAxCCR0 and TAXCCR1 registers are 65,535, which is the maximum value that these two 16-bit registers could hold. If current-detection mode is desired to occur once every 10 seconds, then the timer clock divider can be set to a value to 5, which results in a timer frequency of 6553.6 Hz and a negative pulse width time of 153 microseconds. As a different example, if current-detection mode is to occur once very 64 seconds, then the timer clock divider value can be set to 32, which results in a timer frequency of 1024 Hz and a negative pulse width time of 977 microseconds.

2.3.2.2.2 MCU Procedure for Entering and Exiting Current-Detection Mode

図 10 shows an example procedure that can be followed by the host MCU to trigger the ADS131M04 device to enter current-detection mode. An example time the ADS131M04 device can be selected to enter current-detection mode is when there is an early indication that the input voltage to the power supply is dropping, which may indicate either a power outage or the neutral removal from the meter. In this design, this mode triggered using the power fail indication on the TPS7A78 device.

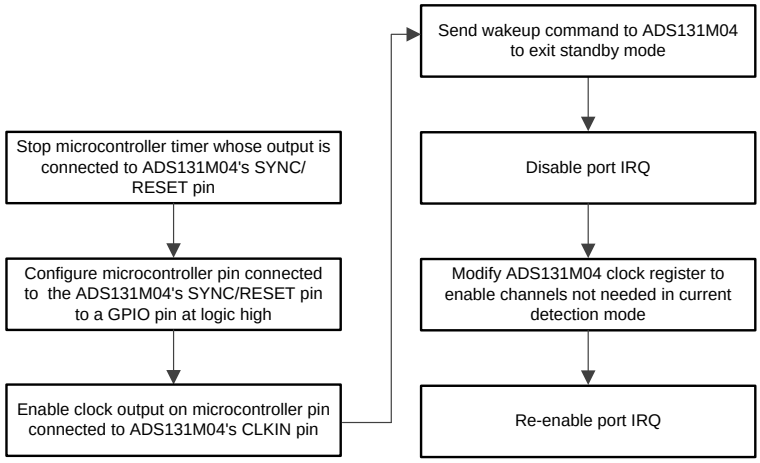
図 10. Example Procedure for Entering Current-Detection Mode



In this example procedure, the port interrupt associated with the ADS131M04 $\overline{\text{DRDY}}$ pin assertion is disabled so that the device can be properly configured without the software being triggered to read ADC samples. After disabling the port interrupt, the host MCU can modify one of the ADS131M04 registers to disable all the channels that a comparison should not be done on for current-detection mode. Namely, disable all of the voltage channels and potentially one of the two current channels. Subsequently, the host MCU should send a command to the ADS131M04 for it to enter standby mode. After sending the command to enter standby mode, the MCU pin connected to the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin of the ADS131M04 device can be configured using the port mapping controller to be a timer output instead of a regular GPIO pin. Disable the clock from the MCU to the CLKIN pin of the ADS131M04 device to reduce current consumption since this external clock is not needed for standby mode or current-detection mode. In addition, initialize the counter on the timer that is used to generate the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pulse so that there will not be a long wait before the MSP432 MCU first provides the pulse to the ADS131M04 to enter current-detection mode. After the timer count is initialized, the timer is then started, which provides the pulses on the ADS131M04 $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin to start current-detection mode at regular intervals, as mentioned in the previous section. At this point, any time $\overline{\text{DRDY}}$ is asserted low indicates that tamper current has been detected so the $\overline{\text{DRDY}}$ port interrupt is re-enabled to capture this. The host MCU can then be put in a low-power mode (note that for this design specifically the MCU was not put in a low power mode). If tamper current has been detected, the $\overline{\text{DRDY}}$ assertion causes an interrupt to the MCU, which wakes the MCU up, if it is in a low-power mode.

図 11 shows an example process for exiting current-detection mode. An example when this can be triggered is when power has been restored to the electricity meter after the end of a power outage. For this design, this event is triggered by the power good signal of the TPS7A78 device being asserted.

図 11. Example Procedure for Exiting Current-Detection Mode



This example process for exiting current-detection mode first begins by the MCU exiting any low power mode that the device may have been put in during the power outage. Next, the timer that was used to provide the pulses on the $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin is disabled. The GPIO pin of the MCU that was connected to the ADS131M04 $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin can be configured back to GPIO operation in case it is desired to reset the ADS131M04 manually later. Next, the clock from the MCU to the CLKIN pin of the ADS131M04 device is enabled again. After enabling the clock, a wake-up command is sent from the host MCU to the ADS131M04 device so that it can exit standby mode and go back to continuous conversion mode. At this point, the device is now converting so the $\overline{\text{DRDY}}$ pin is asserted at a regular rate. Samples are not read at this point because some of the channels may have been disabled from before current-detection mode was entered. The port interrupt associated with $\overline{\text{DRDY}}$ is specifically disabled so that samples are not read yet. Next, one of the ADS131M04 registers is modified so that all of the ADC channels are enabled again. After enabling all the channels, the port interrupt is enabled again so that ADC values can start getting read again. At this point, the normal sampling process from before current-detection mode was entered has been resumed.

2.3.2.3 How to Implement Software for Metrology Testing

The MSP432 software used for evaluating this design is test software. This section discusses the features of the test software, which should provide insights on how to implement custom software for metrology testing. The first subsection discusses the setup of the ADS131M04 device and various peripherals on the MSP432 MCU. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

2.3.2.3.1 Setup

2.3.2.3.1.1 Clock

The MSP432 MCU is configured to have its CPU clock (MCLK) set at 48 MHz and its subsystem master clock (SMCLK) set to 8.192 MHz. The clock source for MCLK is the internal DCO of the MSP432 MCU, which is configured for a frequency of 48 MHz. The clock source for SMCLK is an external 16.384-MHz crystal, which is internally divided by 2 to create the 8.192-MHz SMCLK frequency. An external 32.768-kHz crystal is used as the clock source for the auxiliary clock (ACLK) of the device. This ACLK clock is set to a frequency of 32.768 kHz.

2.3.2.3.1.2 Port Map

The MSP432 MCU has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP432 device in particular, the SPI clock, SOMI, and SIMO functionality of the EUSCIB0 SPI module are all available options to port to ports P2, P3, and P7. In addition, the SMCLK clock output is also available for output to ports P2, P3, and P7. In the test software, this port mapping feature is used for providing flexibility in the PCB layout.

Using the port mapping controller, the following mappings are used:

- PMAP_SMCLK (SMCLK clock output) → Port P2.0 (connected to the CLKIN pin of the ADS131M04 device so that it can be used to generate the modulator clock of the ADS131M04; however, note that this mapping is not enabled initially and is only enabled after the ADS131M04 is initialized.); this is pin 1 of header J27, which is labeled SMCLK on the board
- PMAP_UCB0SIMO (EUSCIB0 SPI SIMO) → Port P2.1 (connected to the DIN pin of the ADS131M04 device); this is pin 2 of header J27, which is labeled SPI DOUT on the board
- PMAP_UCB0SOMI (EUSCIB0 SPI SOMI) → Port P2.2 (connected to the DOUT pin of the ADS131M04 device); this is pin 3 of header J27, which is labeled SPI DIN on the board
- PMAP_UCB0CLK (EUSCIB0 SPI Clock) → Port P2.3 (connected to the SCK pin of the ADS131M04 device); this is pin 4 of header J27, which is labeled SPI CLK on the board
- PMAP_TA0CCR1A→Port 2.6(Timer A0 CCR1 compare output OUT1); this is pin 7 of header J27, which is labeled RST SYNC on the board; note that this mapping only occurs when the ADS131M04 device is in current-detection mode

2.3.2.3.1.3 UART Setup for GUI Communication

The MSP432 MCU is configured to communicate to the PC GUI through either the RS-232 or RS-485 connection on this reference design. The MSP432 MCU communicates to the PC GUI using a UART module configured for 8N1 at 9600 baud.

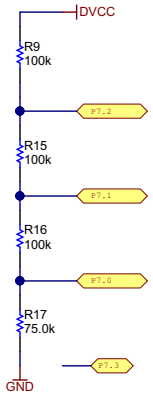
2.3.2.3.1.4 Real-Time Clock (RTC)

The real-time clock module of the MSP432 MCU is configured to give precise one-second interrupts and update the time and date, as necessary.

2.3.2.3.1.5 LCD Controller

The LCD controller on the MSP432P4111 MCU can support up to 8-MUX displays and 320 segments or 4-MUX displays and 176 segments. In the current design, the LCD controller is configured to work in 4-MUX mode using 144 segments. The eight segment lines not used in the 4-MUX mode of this design are used for the port mapping functionality. In this reference design, the LCD is configured for a refresh rate set to ACLK / 64, which is 512 Hz. For contrast control, external resistors are added between the R23, R13, R03 pins and GND, as 図 12 shows.

図 12. LCD External Resistors



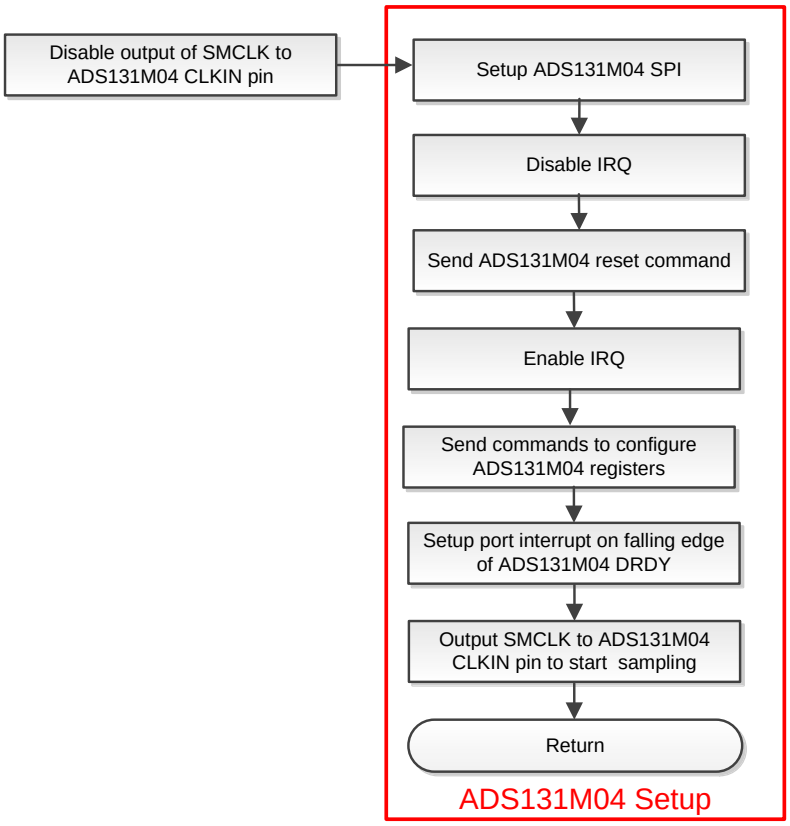
2.3.2.3.1.6 Direct Memory Access (DMA)

The direct memory access (DMA) module transfers packets between the MSP432 MCU and ADS131M04 device with minimal bandwidth requirements from the MSP432 CPU. Two DMA channels are used for communicating to the ADS131M04. One channel (channel 0) is used to send data to the ADS131M04 and the other channel (channel 1) is used to receive data from the ADS131M04. Once a complete packet has been received from the ADS131M04, an interrupt is generated to complete any necessary post-transfer processing, such as CRC verification and packet assembly. 図 17 shows the packets that are sent and received using the DMA of the MSP432 MCU.

2.3.2.3.1.7 ADC Setup

図 13 shows the process used to initialize the ADS131M04. This process is followed when the ADS131M04 device is first setup after the MSP432 MCU resets as well as each time calibration is performed.

図 13. ADC Initialization and Synchronization Process



Before setting up the ADS131M04 device, the test code disables the ADS131M04 modulator clock to prevent the ADS131M04 from generating new samples while trying to set it up. The code disables the modulator clock by disabling the SMCLK output of the MSP432 MCU, which is fed to the CLKIN pin of the ADS131M04 device. Disabling the SMCLK output only needs to be done after calibration and not after an MSP432 MCU reset event since the SMCLK clock output is automatically not output after the MSP432 MCU resets.

After the SMCLK output is disabled, the EUSCIB0 SPI module of the MSP432 MCU is configured for communication to the ADS131M04 device. The EUSCIB0 SPI module is specifically configured as a master device that uses 3-wire mode (the chip select signal is manually asserted high and low in the test software instead of using the chip select feature of the SPI module) and has an 8.192-MHz SPI clock that is derived from the 8.192-MHz SMCLK clock. After the SPI is setup, all interrupts are disabled and a reset command is sent from the MSP432 MCU to the ADS131M04 via SPI. Interrupts are then re-enabled and the MSP432 MCU sends commands to the ADS131M04 to configure its registers.

At this point, note that the modulation clock is not output by the MSP432 MCU, which means that sampling is not started yet. By sending commands to the ADS131M04 to initialize the ADS131M04 registers, the ADS131M04 is configured for the following:

- MODE register settings: 16-bit CCITT CRC used, 24-bit length for each word in the ADS131M04 packet, $\overline{\text{DRDY}}$ signal asserted on most lagging enabled channel, $\overline{\text{DRDY}}$ asserted high when conversion value is not available, $\overline{\text{DRDY}}$ asserted low when conversion values are ready
- GAIN1 register settings: PGA gain of 1 used for voltage channel and CT channel; PGA gain of 32 used for shunt channel (assuming 200-μΩ shunts)

- CFG register settings: CD=1 (current-detection mode enabled), CD_ALLCH=0(MCU triggered based on if any enabled channel detects tamper current), CD_NUM(current-detect number of threshold exceeds to trigger detect)=8, CD_LEN(current-detect measurement length in conversion periods)=256
- CH*n*_CNG register settings (where *n* is the channel number) : Channels 0, 1, and 2 inputs connected to external ADC pins and channel phase delay set to 0 for channels 0, 1, and 2 (note that software phase compensation is used instead of ADS131M04 hardware phase compensation); the channel 3 config register is not modified since channel 3 is not used for this configuration.
- CLOCK register settings: 512 OSR, all channels enabled, and high-resolution modulator power mode
- CD_THRSHLD=80000
- CH*n*_OCAL register settings (where *n* is the channel number) = measured channel DC offset (for only current channels)

Before initializing the registers, an estimate of the ADC offset(in ADC units) for each current channel is determined using the PC GUI. The offset calibration registers for the current channels are then updated with the corresponding offsets to subtract out most of the ADC offset from both current channels. This offset calibration is done to have better matching between the line and neutral ADC channels, which has significantly different ADC offsets due to different gains being used on these channels. Having better matching between the line and neutral ADC channels enables the line and neutral current channels to cause a trigger in current-detection mode when nearly the same neutral and line current is applied to the meter. For even more precise matching between the line and neutral currents needed to trigger current-detection mode, the gain registers on the two current channels can be modified as well; however, for this design, good enough ADC matching was obtained without modifying the gain calibration registers of the ADS131M04 device so these registers were left unmodified.

In this design, CD_LEN=256, which allows current-detection to be performed over more than 4 Mains cycles of ADC samples. The CD_LEN time determines the maximum time spent in current-detection mode before the device returns to standby mode. Decreasing the value of CD_LEN decreases the time in current-detection mode, which reduces the average current consumption drawn from the ADS131M04 device after an AC supply failure.

After the ADS131M04 registers are properly initialized, the MSP432 MCU is configured to generate a port interrupt whenever a falling edge occurs on the $\overline{\text{DRDY}}$ pin, which indicates that the ADS131M04 device has new samples available. Next, the MSP432 MCU outputs the SMCLK clock to the ADS131M04, which starts the voltage and current sampling.

The ADS131M04 modulator clock is derived from the clock fed to its CLKIN pin, which is output from the SMCLK output of the MSP432 MCU. The clock fed to the CLKIN pin of the ADS131M04 device is internally divided by two, to generate the ADS131M04 modulator clock. The sampling frequency of the ADS131M04 is therefore defined as:

$$f_s = f_M / OSR = f_{CLKIN} / (2 \times OSR) \quad (7)$$

where

- f_s is the sampling rate
- f_M is the modulator clock frequency
- f_{CLKIN} is the clock fed to the ADS131M04 CLKIN pin
- OSR is the selected oversampling ratio

In this design, the SMCLK clock of the MSP432 MCU that is fed to the ADS131M04 CLKIN pin has a frequency of 8.192 MHz. The oversampling ratio is selected to be 512. As a result, the ADS131M04 modulator clock is set to 4.096 MHz and the sample rate is set to 8000 samples per second.

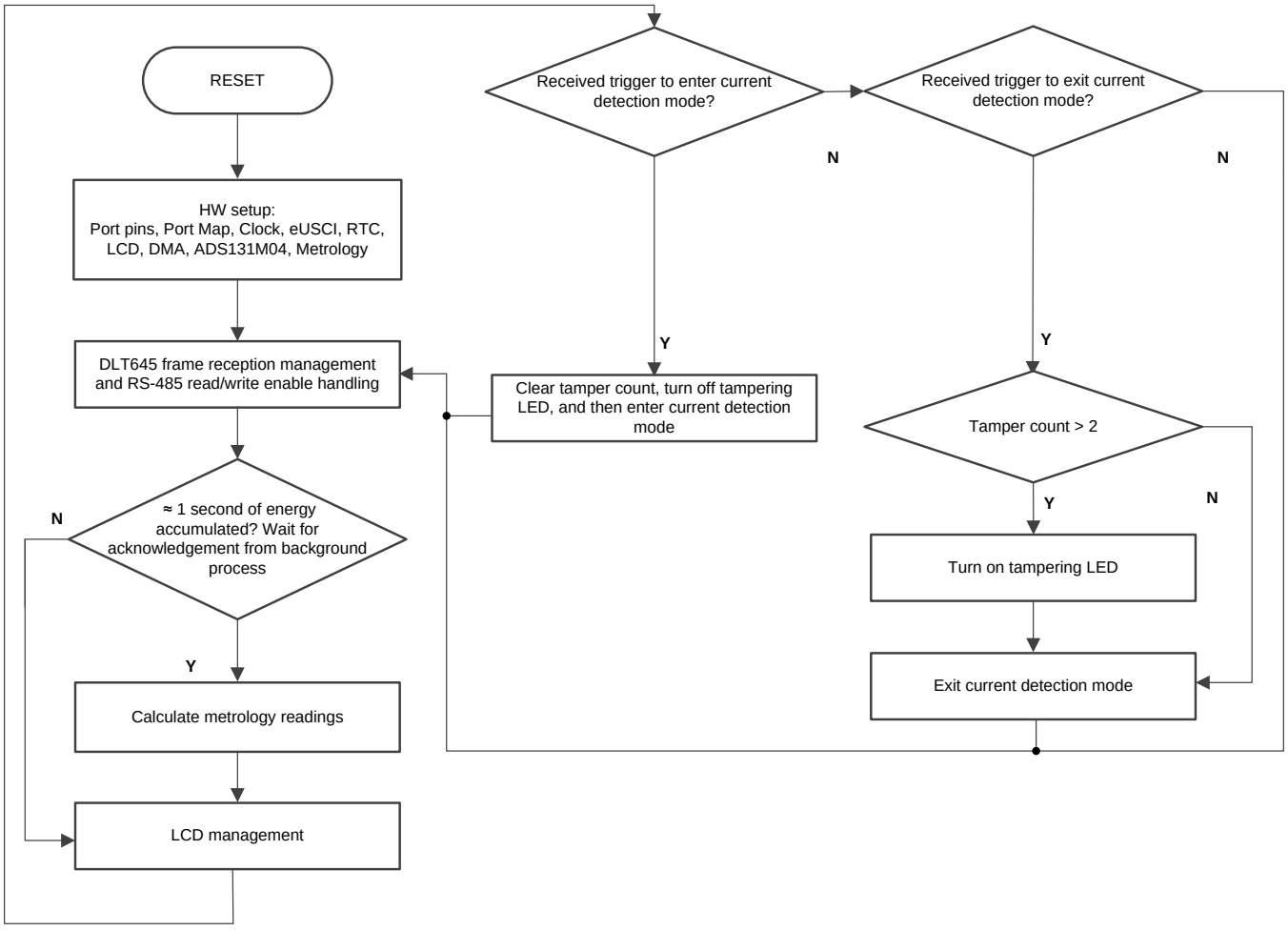
In this design, the following ADS131M04 channel mappings are used:

- AIN0P and AIN0N ADS131M04 ADC channel pins → Voltage
- AIN1N and AIN1P ADS131M04 ADC channel pins →Shunt Current (This is the primary current channel; this can measure either the neutral or line current)
- AIN2P and AIN2N ADS131M04 ADC channel pins →CT Current(This is the secondary current channel; this can measure either the line or neutral current)
- AIN3P and AIN3N ADS131M04 ADC channel pins → Not used in design

2.3.2.3.2 Foreground Process

The foreground process includes the initial setup of the MSP432 hardware and software and the ADS131M04 registers immediately after a device RESET. 図 14 shows the flow chart for this process.

図 14. Foreground Process



The initialization routines involve the setup of the MSP432 general purpose input/output (GPIO) port pins and associated port map controller; MSP432 clock system; MSP432 USCI_A0 for UART functionality; MSP432 RTC module for clock functionality; MSP432 LCD; MSP432 DMA; ADS131M04 registers; and MSP432 metrology variables.

After the hardware is setup, any received frames from the GUI are processed. If RS-485 is selected for communication to the PC GUI, the THVD1500 device must have its RE and DE pins driven to enable the receiver and driver during the proper points in time to receive packets from the PC GUI and send responses back to the GUI. After any packet is sent from the MSP432 MCU to the PC GUI, the foreground process is responsible for asserting the RE and DE pins after the packet has been completely sent out from the MSP432 MCU but before the GUI sends out its next packet.

Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters. This notification is accomplished through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for approximately one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming Mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage dot products, current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power of the foreground process, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in 2.3.2.3.2.1.

The foreground process also updates the LCD. The LCD display item is changed every two seconds. See 2.4.2.1.4.1 for more information about the different items displayed on the LCD.

The foreground process is also where the MSP432 MCU triggers the ADS131M04 device to enter or exit current-detection mode. In this design, the LED labeled LED1 is turned ON to indicate that tampering was previously detected sometime in the interval from when the TPS7A78 device has provided a power failure indication to the time when it has provided a power good indication. In addition, a variable logs how many times the ADS131M04 device has alerted the MSP432 that a tamper event has been detected by the ADS131M04 device during this same time interval.

If the MSP432 has received a trigger to enter current-detection mode based on the power fail indication from the TPS7A78 device, the tamper count variable is cleared so that this variable only counts the number of times tampering has been detected from the last power failure instance instead of it counting the total number of times tampering has been detected from the last time the MSP432 MCU has been reset. After clearing the tamper count variable, the tampering LED is turned off in case it was already on from the previous time. Current-detection mode is then entered.

If the MSP432 has received a trigger to exit current-detection mode based on the power good indication from the TPS7A78 device, the tamper count variable is checked to see if there has been more than two tamper events that were detected by the ADS131M04 device. If more than two tamper events were detected by the ADS131M04, the tampering LED is turned ON to indicate that tampering was detected. The reason why a tamper event is defined based on having more than two tamper events detected by the ADS131M04 is so that the system does not indicate tampering from the following two scenarios: (1) when power is first lost, current-detection mode is triggered when the current has not fallen below the current-detection mode threshold yet, despite already being indicated of a power failure event, and (2)power is being restored to the meter and the sensed current is now above the current-detection mode threshold but the system still did not have enough time to exit current-detection mode so this is seen as a tamper event.

After checking to see if the tamper count variable is greater than 2 and turning on the tampering LED if it is, current-detection mode is exited. The code then returns to the beginning of the foreground loop by checking for any new messages from the PC GUI again.

2.3.2.3.2.1 Formulas

This section briefly describes the formulas used for the voltage, current, power, and energy calculations. As previously described, voltage and current samples are obtained at a sampling rate of 8000 Hz. All of the samples that are taken in approximately one second frames are kept and used to obtain the RMS values for voltage and current. The RMS values are obtained with the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample Count}}} - v_{offset,ph}$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample Count}}} - i_{offset,ph}$$

where

- $V_{ph}(n)$ = Voltage sample at a sample instant n
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $I_{ph}(n)$ = Each current sample at a sample instant n
- $I_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples within the present frame
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for current (8)

Power and energy are calculated for active and reactive energy samples of one frame. These samples are phase-corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample Count}} v_{ph}(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{ACT\_Offset,ph} \quad (9)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample Count}} V_{90,ph}(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{React\_Offset,ph} \quad (10)$$

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample Count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample Count}}} - v_{offset,ph}$$

where

- $V_{90}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power
- $P_{ACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the active power measurements
- $P_{REACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the reactive power measurements (11)

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents
2. This approach conforms to the measurement method specified by IEC and ANSI standards

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, the mains frequency is first measured accurately to phase-shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays.

Using the calculated powers, energies are calculated with the following formulas in 式 12:

$$E_{ACT,ph} = P_{ACT,ph} \times \text{Samplecount}$$
$$E_{REACT,ph} = P_{REACT,ph} \times \text{Samplecount}$$
$$E_{APP,ph} = P_{APP,ph} \times \text{Samplecount} \quad (12)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples-per-mains cycle. The foreground process then converts this samples-per-mains cycle to Hertz with 式 13:

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \quad (13)$$

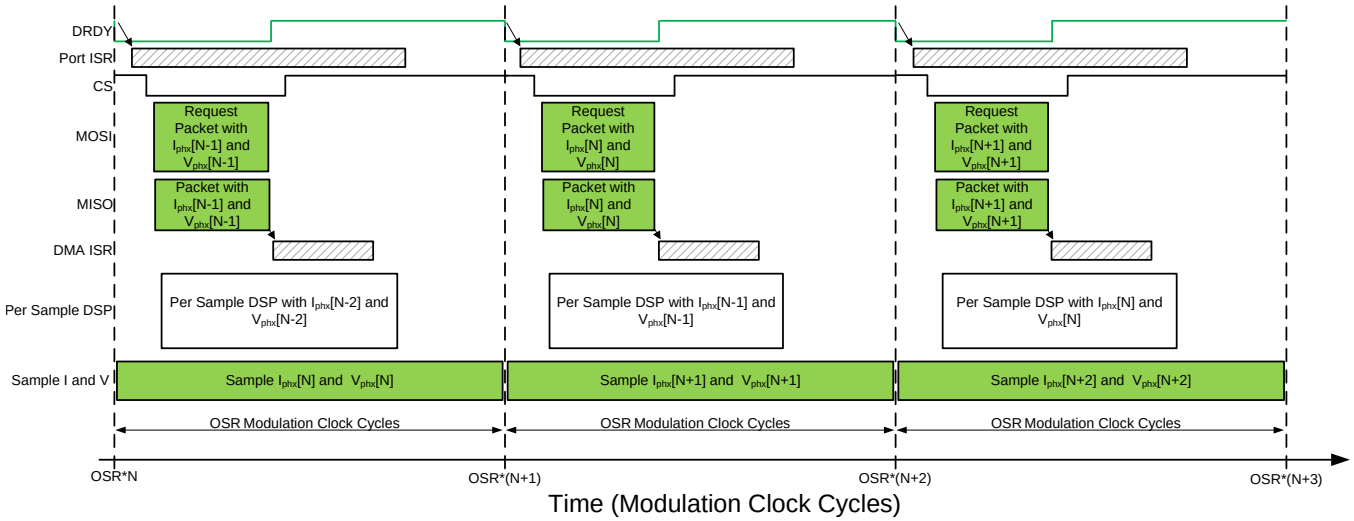
After the active power and apparent power are calculated, the absolute value of the power factor is calculated. In the internal representation of power factor of the system, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated with 式 14:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{ if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{ if inductive load} \end{cases} \quad (14)$$

2.3.2.3.3 Background Process

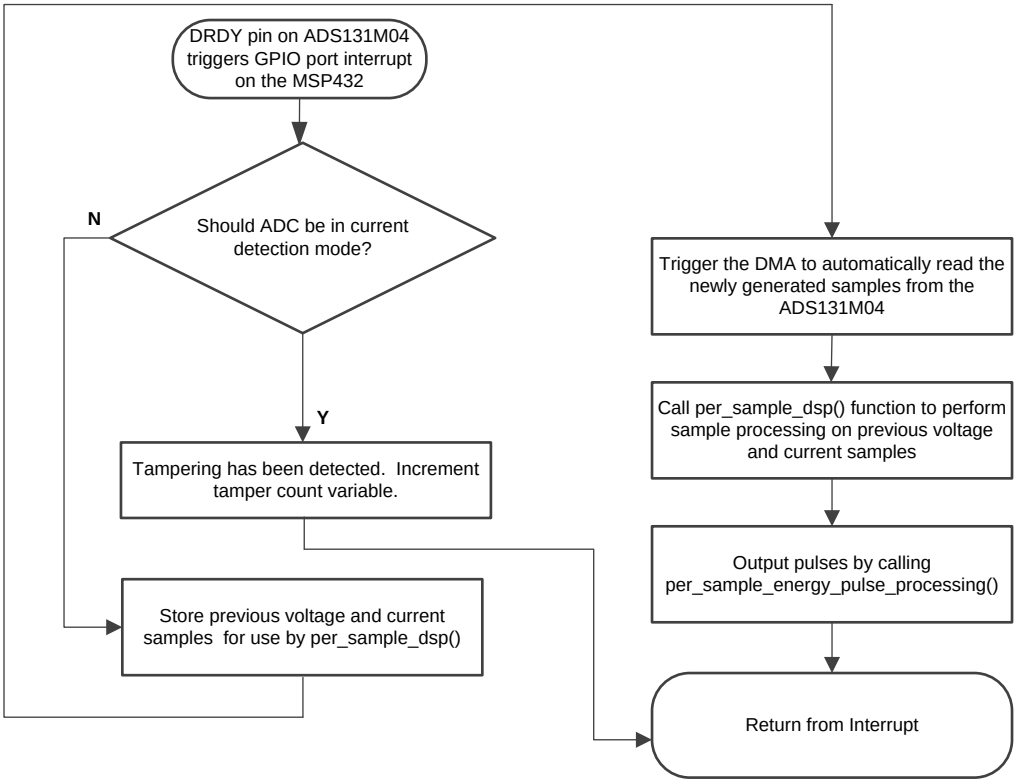
図 15 shows the different events that occur when sampling voltage and current, where the items in olive green are done by the hardware settings and not the test software.

図 15. Voltage and Current Sampling Events



To go over the process mentioned in 図 15, new current samples are ready every OSR, or 512 for this design, modulation clock cycles. Suppose the most recently ready current (both from the shunt and CT channels) and voltage samples from the ADS131M04 device corresponds to the N^{th} – 1 current and voltage samples, or $I_{phx}[N - 1]$ and $V_{phx}[N - 1]$. Once new samples are ready, the $\overline{DRDY}$ pin is asserted low by the ADS131M04. The falling edge on the $\overline{DRDY}$ pin on the ADS131M04 device causes a GPIO port interrupt on the MSP432 MCU, which triggers the Port ISR on the MSP432 MCU. The background process is run within the Port ISR. 図 16 shows the background process, which mainly deals with timing-critical events in the test software.

図 16. Background Process

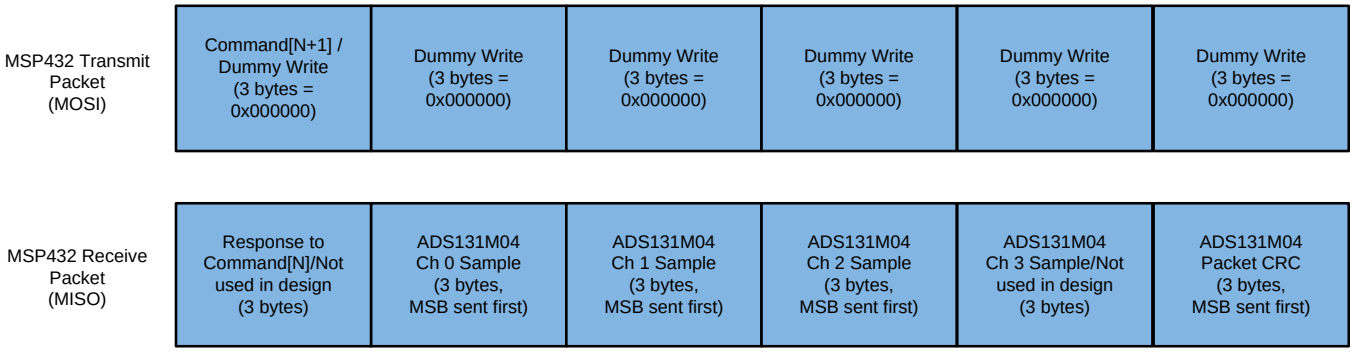


The background process occurs every time there is a port interrupt due to the $\overline{\text{DRDY}}$ pin of the ADS131M04 device being asserted. In the background process, if the device was supposed to be in current-detection mode, the only way for the $\overline{\text{DRDY}}$ pin to have been asserted is if the ADS131M04 device has potentially detected tampering from removing the neutral connection from the meter. If the port ISR has been triggered because of this, this potential tamper event is logged by incrementing the tamper count variable.

If the ADS131M04 device is not supposed to be in current-detection mode, the assertion of the $\overline{\text{DRDY}}$ pin and subsequent triggering of the port ISR is because there are new samples from the ADS131M04. When this occurs, the previously-obtained voltage samples ($V_{phx}[N - 2]$) and previously obtained current samples ($I_{phx}[N - 2]$) are stored in buffers that are later read by the per_sample_dsp function, which is responsible for updating the intermediate dot product quantities used to calculate metrology parameters. After the previously obtained voltage and current samples are stored, communication to the ADS131M04 device is enabled by asserting the chip select signal low. The DMA is then configured to both send a request for the newest current and voltage samples ($I_{phx}[N - 1]$ and $V_{phx}[N - 1]$) of the ADS131M04 device and also to receive the data packet response from the ADS131M04. The request and reception of the current samples is done automatically by the DMA module instead of it being done by the software.

図 17 shows the packet that is transmitted by the DMA of the MSP432 MCU and the response packet from the ADS131M04 device that is received and assembled by the DMA as well. The transmission and reception packets contain six words, where each word is three bytes long.

図 17. ADS131M04 ADC Sample Request Packet



When requesting the ADC data from the ADS131M04 device, the first word that has to be sent to the ADS131M04 is the command word. Since the test software does not need to change the settings of the ADS131M04 or read any registers during typical ADC sample readouts, a NULL command is sent to the ADS131M04, which allows you to get the ADC samples from the ADS131M04 without changing the state of the device. The actual size of the null command is 16-bits; however, since 24-bit words are used, the 16-bit command must be padded with an extra value of 0x00 at the end of the command. The NULL command word sent therefore has a value of 0x000000. While the MSP432 MCU is shifting out the command word, the MSP432 is simultaneously shifting in the response word to the command word of the previous packet. The response word to a NULL command is the contents of the STATUS register. The contents of the STATUS register are not used in this design so the first word received from the ADS131M04 is ignored.

After writing the command word, it is necessary to perform a dummy write for each byte that is read. The dummy byte write is necessary to enable the SPI clock, which is necessary to read a byte from the ADS131M04 device. For each dummy byte write, a value of 0x00 is written to the SPI transmit register for EUSCIB0. Immediately after writing the command byte, writing three dummy bytes allows the MSP432 MCU to receive the 3-byte ADC value from channel 0 of the ADS131M04. Writing the next nine dummy bytes gets the ADC data for channel 1, channel 2, and channel 3, respectively. Since channel 3 is not used for measuring anything, the channel 3 word is ignored. Finally, writing the next three dummy bytes gets the CRC word. The CRC word is 24-bits; however, note that the actual CRC is only 16-bits, which are placed in the most significant bits of the 24-bit word. As a result, when parsing the CRC word, the last byte is not needed (note though that the dummy write for this zero-padded byte must still be sent though for proper ADS131M04 operation).

図 17 shows that whenever the DMA has received the entire $I_{phx}[N - 1]$ packet, the DMA ISR is automatically called. Within the ISR, the CRC is calculated over the five command and ADC words (15 bytes in total). This CRC calculation uses the CRC module of the MSP432 MCU. Since the CRC module works with an even number of bytes but there are a total of 15 bytes available, the CRC module is used for the first 14 bytes. The final CRC is calculated in software from the CRC module result and the 15th byte. Note that the software CRC calculation on the last byte is only necessary because the word size is selected to be three bytes in this design. If the word size is selected to be two bytes or four bytes instead, the software CRC calculation is not needed since there is an even number of bytes. 図 18 shows the code snippet for calculating the CRC over 15 bytes by using the MSP432 CRC module and software.

図 18. Code Snippet for Using the CRC Module of the MSP432 MCU for Calculating CRC Over an Odd Number of Bytes

```
CRC32->INIRES16 = 0xFFFF;                   // Init CRC16 HW module
for(i=0; i<CRC_BYTE_START/2; i++) //This for loop uses the MSP432's CRC module for calculating CRC for first 14 bytes of packet
{

    CRC32->DIRB16 = (((uint16_t )packet[i<<1])<<8) | packet[(i<<1) +1];
    __no_operation();
}
CRC16_Result = (unsigned char) (CRC32->INIRES16 >> 8) | (CRC32->INIRES16 << 8); //Stores CRC result for first 14 bytes from CRC module
CRC16_Result ^= packet[CRC_BYTE_START-1]; //packet[CRC_BYTE_START-1] is the last (15th byte) not used by the CRC module's calculation
CRC16_Result ^= (unsigned char) (CRC16_Result & 0xFF) >> 4;
CRC16_Result ^= (CRC16_Result << 8) << 4;
CRC16_Result ^= ((CRC16_Result & 0xFF) << 4) << 1; //The final CRC result over 15 bytes is now stored in CRC16_Result after this line executes.
```

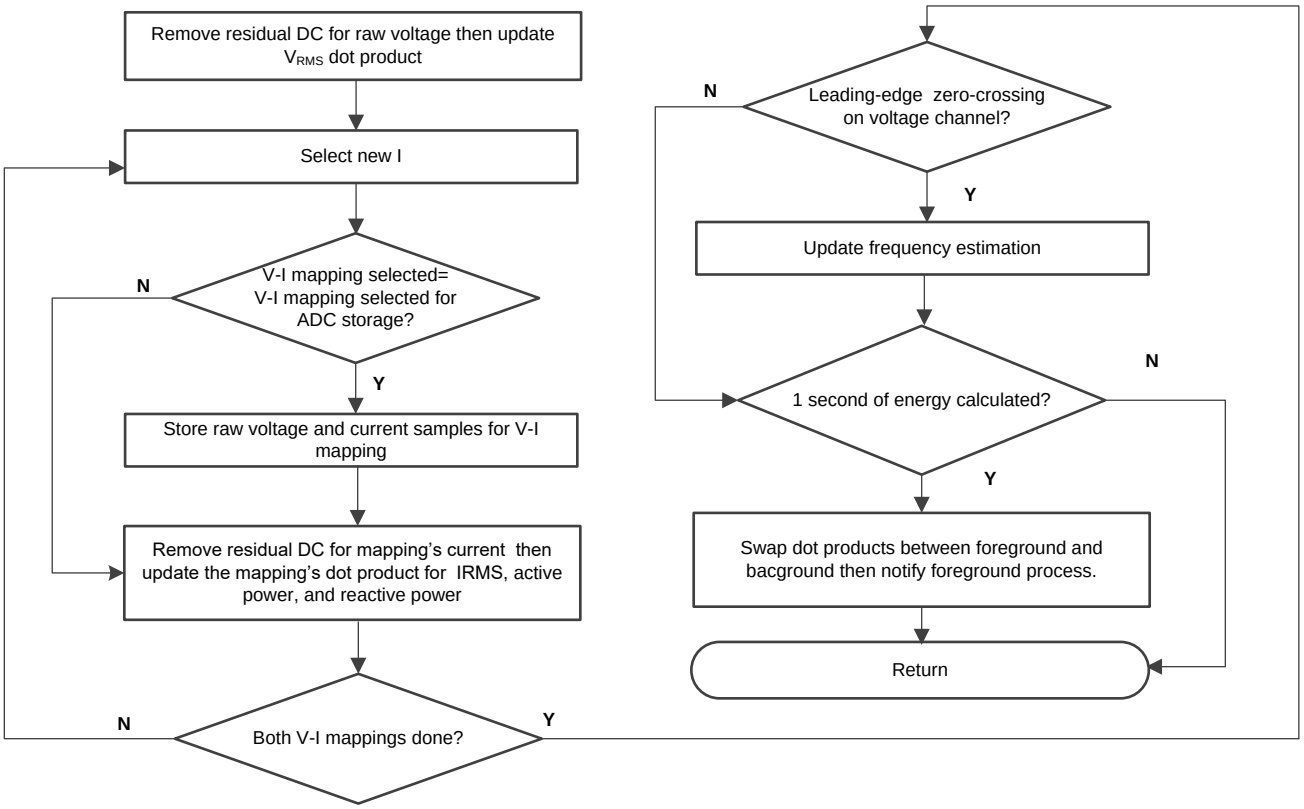
Once the CRC has been calculated over the packet, it is compared to the CRC obtained in the packet sent from the ADS131M04 device. The sent CRC is parsed from bytes 16 and 17 of the ADS131M04 packet (byte 18, which is part of the CRC word, is zero-padded so it is not used in parsing). If the calculated CRC and the parsed CRC are equal, then the CRC check passes and the ADC data is parsed to get the values of the voltage and current samples at time N – 1. The parsed voltage and current samples are put in temporary buffers so that they are used the next time the per_sample_dsp function is called at the next interrupt. Before the DMA interrupt ends, the chip select line is pulled back high again to properly reset the ADS131M04 communication before the next time current samples are ready from the ADS131M04.

In parallel to receiving the newest current samples from the ADS131M04 device using the DMA, the ADS131M04 is currently sampling the next voltage (V_{phx}[N]) and current samples (I_{phx}[N]) and the test software also performs per-sample processing on the last voltage (V_{phx}[N – 2]) and current samples (I_{phx}[N – 2]) obtained from the ADS131M04. This per-sample processing is used to update the intermediate dot product quantities that are used to calculate the metrology parameters. After sample processing, the background process uses the "per_sample_energy_pulse_processing" for the calculation and output of energy-proportional pulses. Once the per_sample_energy_pulse_processing is completed, the test software exits from the port ISR.

2.3.2.3.3.1 per_sample_dsp()

図 19 shows the flow chart for the *per_sample_dsp()* function. The *per_sample_dsp()* function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. Both voltage and current samples are processed and accumulated in dedicated 64-bit registers. Active power and reactive power are also accumulated in 64-bit registers.

図 19. *per_sample_dsp* **Function**



After sufficient samples (of approximately one second) are accumulated, the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; and power factor. In the test software, there are two sets of dot products for a phase: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly-acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products. Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the *per_sample_dsp()* function is also responsible for updating the corresponding frequency (in samples per cycle) of the phase.

The following sections describe the various elements of electricity measurement in the *per_sample_dsp()* function.

2.3.2.3.3.1.1 Voltage and Current Signals

The test software of the design has support for storing the raw voltage and storing either the shunt ADC values or current ADC values.

The raw ADS131M04 samples are signed integers and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current raw ADC sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively (Note that separate dot product variables are used for the CT current and the shunt current since current and power calculations are done for both line and neutral currents.)
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

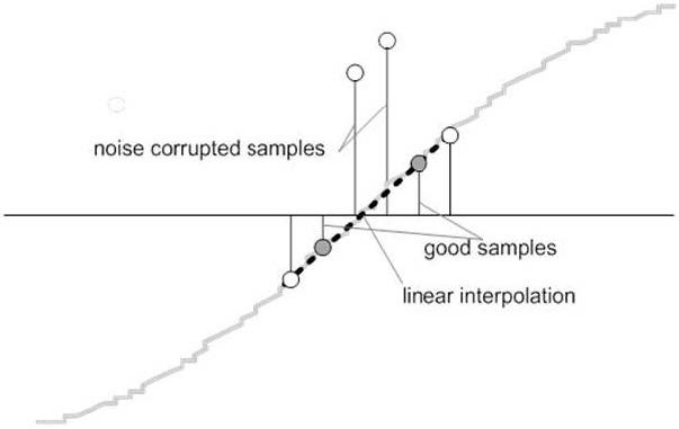
The foreground process processes these accumulated values.

2.3.2.3.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltages, currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When samples of approximately one second have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. 図 20 shows the samples near a zero cross and the process of linear interpolation.

図 20. Frequency Measurement



Because noise spikes can also cause errors, the application uses a rate-of-change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

2.3.2.3.3.2 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSP432 MCU) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

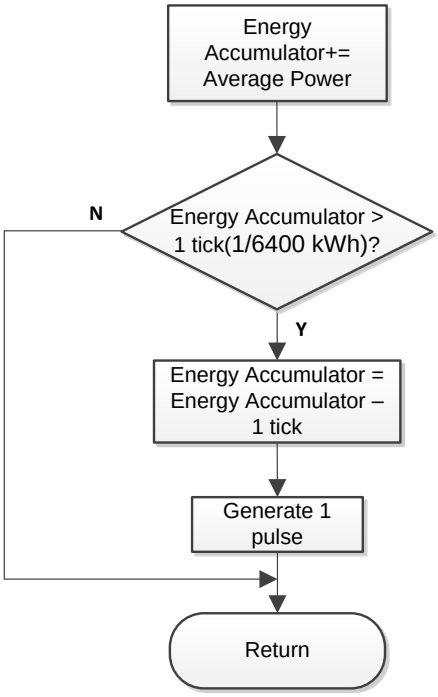
This application uses average power to generate these energy pulses. The average power accumulates at every $\overline{\text{DRDY}}$ port ISR interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The tick is usually defined in pulses-per-kWh or just in kWh. One pulse must be generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh / 6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses.

In the reference design, the LED that is labeled "Act" corresponds to the active energy consumption for the two-phase sum. "React" corresponds to the cumulative two-phase reactive energy sum.

図 21 shows the flow diagram for pulse generation.

図 21. Pulse Generation for Energy Indication



The average power is in units of 0.001 W and a 1-kWh threshold is defined as:

1-kWh threshold = 1 / 0.001 × 1 kW × (Number of interrupts per second) × (Number of seconds in one hour) = 1000000 × 8000 × 3600 = 0x1A3185C50000

2.3.2.3.3.3 Phase Compensation

When a current transformer (CT) is used as a sensor, it introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit may introduce another phase shift. The user must compensate the relative phase shift between voltage and current samples to ensure accurate measurements. The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the test software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 8000-Hz sample rate used in this application corresponds to a 0.0088° degree resolution at 50 Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

An alternative option to the software phase compensation used in this design is to use the phase compensation feature on the ADS131M04 device. If this hardware phase compensation scheme is used, filter coefficients are not necessary so it is not needed to divide by the gain of the filter coefficients.

2.4 Hardware, Software, Testing Requirements, and Test Results

2.4.1 Required Hardware and Software

2.4.1.1 Cautions and Warnings

At high currents, the terminal block can get warm. In addition, note that the line voltage is fed to the board so take the proper precautions, especially if the system is referenced with respect to line.

WARNING

Hot Surface! Contact can cause burns. Do not touch. Take the proper precautions when operating.

CAUTION

High Voltage! Electric shocks are possible when connecting the board to live wires. The board must be handled with care by a professional. For safety, use of isolated test equipment with overvoltage or overcurrent protection is highly recommended.

2.4.1.2 Hardware

The following figures of the reference design best describe the hardware: 図 22 is the top view of the energy measurement system, 図 23 shows the location of various pieces of the reference design on the top layer of the PCB, and 図 24 shows the location of various pieces of the reference design on the bottom layer of the PCB.

図 22. Top View of TIDA-010036 Design

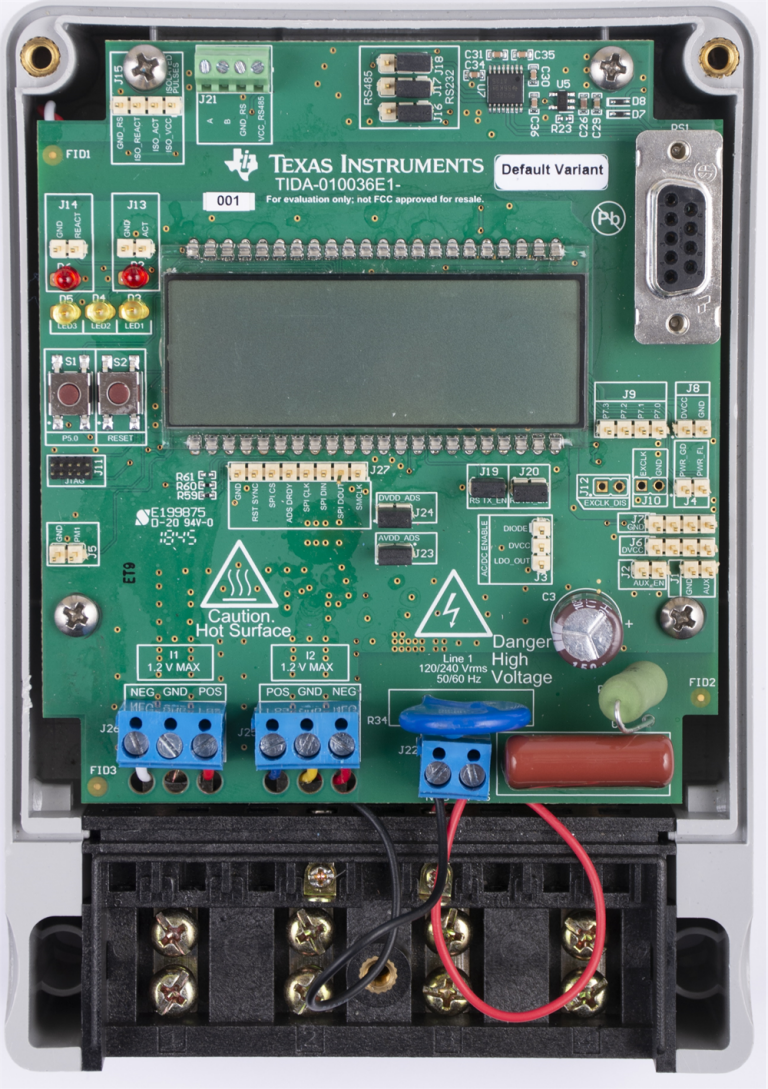


図 23. Top Layer of TIDA-010036 PCB With Components Highlighted

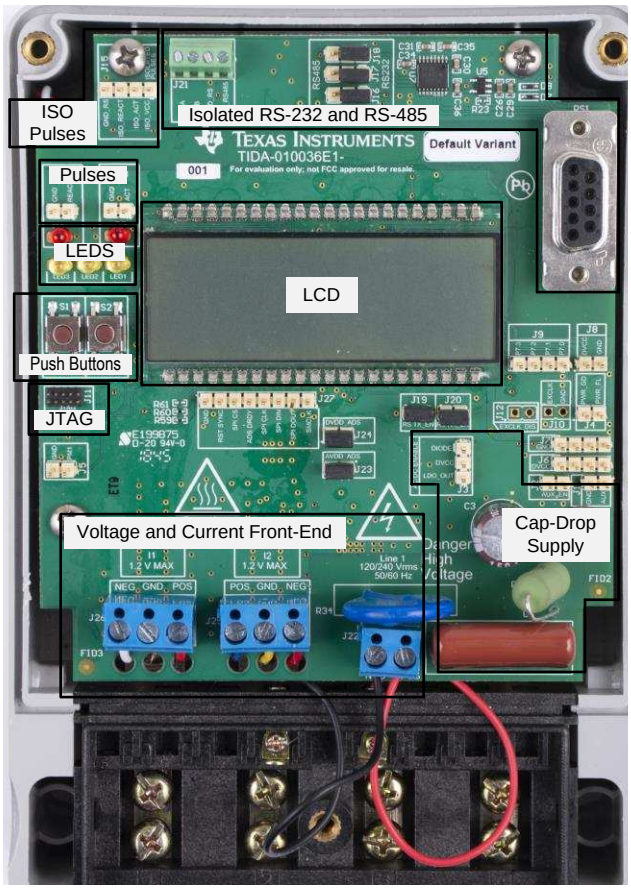
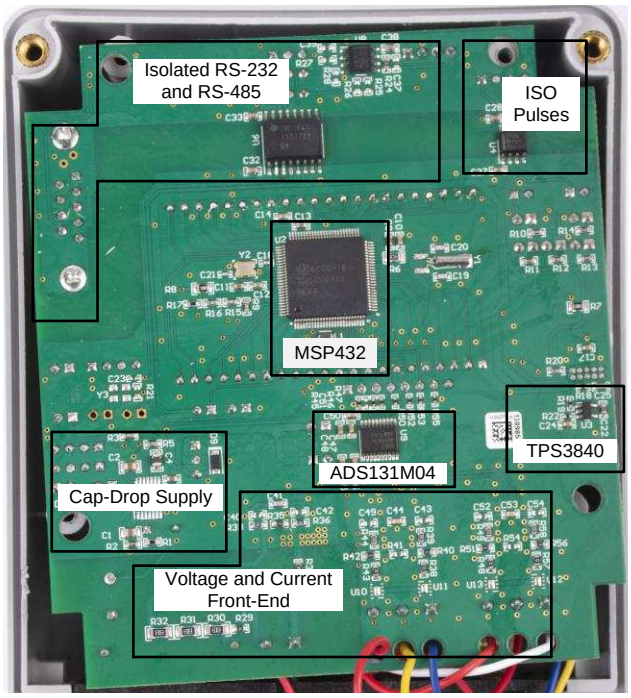


図 24. Bottom Layer of TIDA-010036 PCB With Components Highlighted



2.4.1.2.1 Connections to the Test Setup

AC voltages and currents can be applied to the board for testing purposes at these points:

- Terminal block "J22" is a two-position terminal block that corresponds to the line and neutral voltage connection. If referencing the shunt and system ground with respect to the neutral, connect the terminal block position on the left, which is labeled "NEG", to the neutral and connect the terminal block position on the right, which is labeled "POS", to the line. If referencing the shunt and system ground with respect to the line, connect the terminal block position on the left, which is labeled "NEG", to the line and connect the terminal block position on the right, which is labeled "POS", to the neutral. If the system is referenced with respect to the line, note that all voltage samples obtained from the ADS131M04 should be multiplied by –1 in the software to ensure that the phase shift between voltage and current is properly reflected for the power-related metrology readings.
- Terminal block "J25" is connected to the output terminals of the shunt. This terminal block is a three-position terminal block with positions labeled "POS", "GND", and "NEG". For the gain of 32 used in this design, the differential voltage across the "POS" and "NEG" terminals of this terminal block should be less than ±37.5 mV. **Do not connect a CT here since a burden resistor is not present for the circuitry of this channel like it is present for the J26 current circuitry.** 図 25 shows a mapping between shunt terminals and the positions on J25. The differential voltage output from the shunt, which is fed to the POS and NEG positions of J25, should not exceed ±37.5 mV.
- Terminal block "J26" corresponds to the current inputs after the CT. This terminal block is a three-

position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Connect the positive terminal of the CT to the terminal block position (labeled "POS") on the most right. Connect the negative terminal of the CT to the terminal block position (labeled "NEG") on the most left. Select the applied current to the input of the CT so that it does not exceed 100 A. **In addition, before performing any test, verify that this terminal block is securely connected to both output leads of the CT**.

図 25. Mapping Between Shunt Terminals and J25 Terminal Block Positions

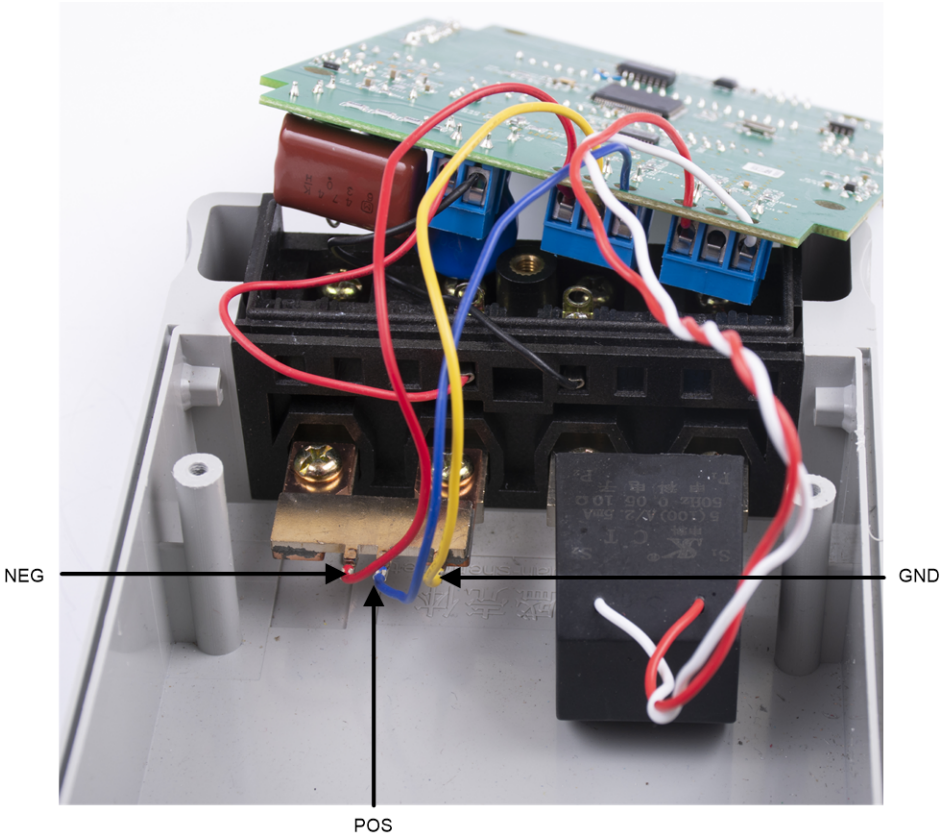
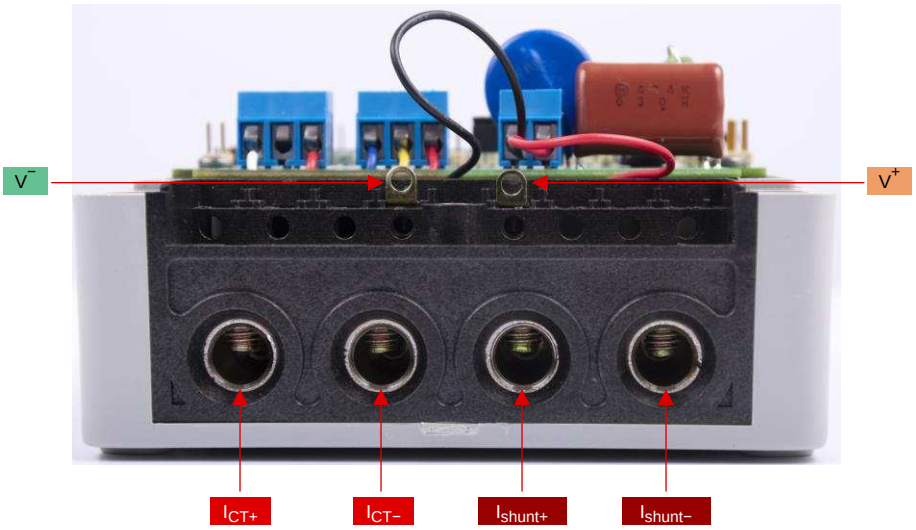


図 26 shows the various test setup connections required for the reference design to function properly. If the shunt and system is referenced with respect to the neutral, V^+ corresponds to the line connection and V^- corresponds to the neutral connection. If the shunt and system is referenced with respect to the line, V^+ corresponds to the neutral connection and V^- corresponds to the line connection.

I_{shunt+} and I_{shunt-} correspond to the current inputs to the shunt of the design while I_{CT+}, and I_{CT-} correspond to the current inputs to the current transformer of the design.

図 26. View of Reference Design With Test Setup Connections



2.4.1.2.2 Power Supply Options and Jumper Settings

The MSP432 MCU and ADS131M04 device portion of this design is powered from a single voltage rail (DVCC), which can be derived from two potential methods. In the first method, DVCC can be powered from AC mains by using the TPS7A78-based cap-drop supply of the design. The output of the TPS7A78 device can be connected directly to DVCC by putting a jumper between the DVCC and LDO_OUT pins of the J3 header. Connect the TPS7A78 device indirectly to DVCC through a diode in case there is an auxiliary power source (such as a battery) connected to header J1 that the system can switch to, in case of an AC supply failure. Make this connection by placing a jumper between the DVCC and DIODE options of the J3 header and placing a jumper at the J2 header.

The diode ORs the TPS7A78 power supply with the auxiliary power supply connected at J1. To ensure that the system is powered from the TPS7A78 power supply when Mains is available, the output voltage from the TPS7A78 (3.3 V for this design) should be greater than the output voltage from the auxiliary power supply connected to J1. If the output voltage from the TPS7A78 is not larger than the auxiliary power source output voltage, the design is powered from the auxiliary power source even when Mains is available. It should also be noted that powering DVCC through the diodes results in a lower output voltage than if the diodes are not used because of the voltage drop across the diode. As a result, if an auxiliary power supply is not needed, it is recommended to connect the TPS7A78 directly to DVCC instead of connecting it to DVCC through a diode.

In the second method for deriving power for DVCC, DVCC can be powered from an external power supply by connecting a 3.3-V external power supply at the DVCC header J6 and GND. To support this direct way of driving DVCC, do not place a jumper on jumper header J3.

Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. 表 3 indicates the functionality of each jumper on the board.

注: The headers with **(WARNING)** text in the *MAIN FUNCTIONALITY* column are not isolated, so do not use measuring equipment there (especially if the system is referenced with respect to the line) when running off the Mains. This applies, unless either isolators external to the board of the design are used to connect at the headers, if the equipment is battery powered and does not connect to Mains, or if AC mains is isolated.

表 3. Header Names and Jumper Settings

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J1	2-pin header	Auxiliary power input **(WARNING)**	Apply 3.2 V between here and GND to create the auxiliary power supply that can be used to power the design when the TPS7A78 is not able to power the design because of an AC supply failure seen at its input.	Place a jumper at J2 and another jumper between the DVCC and DIODE options of the J3 header to support using the voltage applied here as a backup power supply. In addition, the voltage applied at this header should be less than the TPS7A78 output voltage.
J2	2-pin jumper header	Auxiliary power input enable**(WARNING)**	Place a jumper at this header to connect the auxiliary power supply at header J1 to DVCC.	A jumper here connects the auxiliary power supply at header J1 to DVCC through a diode. To support using the voltage applied here as a backup power supply, a jumper must be placed between the DVCC and DIODE options of the J3 header to OR the TPS7A78 and auxiliary power supplied together. Note that the output voltage connected to DVCC is smaller than the voltage applied at this header because of the voltage drop across the diode.

表 3. Header Names and Jumper Settings (continued)

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J3	3-pin jumper header	TPS7A78 DVCC connection**(WARNING)**	The LDO_OUT pin of this header can be probed to view the output voltage produced from the TPS7A78. A jumper can be placed here to connect the TPS7A78 directly through DVCC or indirectly to DVCC through a diode.	Place a jumper between the DVCC and DIODE option of this header if using the auxiliary power supply at header J1 as a backup power supply when the AC mains input to the TPS7A78 fails. Additionally, place a jumper at J2. By placing these two jumpers, the TPS7A78 device and auxiliary power supplies are ORed together. Note that the output voltage connected to DVCC is smaller than the TPS7A78 output voltage because of the voltage drop across the diode. If an external power supply is to be connected to DVCC instead of using the TPS7A78, do not place a jumper here.
J4	2-pin header	Header connected to TPS7A78 PG and $\overline{PF}$ pins **(WARNING)**	Probe at pin 2 of this header to determine if the TPS7A78 device has detected AC supply failure at its input. Probe at pin 1 to determine if the output voltage from the TPS7A78 has ramped up beyond 90% of the set 3.3-V LDO output voltage.	The $\overline{PF}$ pin is used in this design to trigger the ADS131M04 device to enter current-detection mode. The PG pin is used in this design to trigger the ADS131M04 to exit current-detection mode.
J5	2-pin header	PM1 header **(WARNING)**	P2.7 GPIO pin and GND.	This header has two pins: GND and PM1, where PM1 is the P2.7 GPIO pin of the MSP432 MCU. The P2.7 GPIO pin can be port mapped to different functions, which allows this header to potentially be used to debug multiple items.
J6	4-pin header	DVCC voltage header **(WARNING)**	Probe here for DVCC voltage. Connect the positive terminal of the bench or external power supply when powering the board externally directly through DVCC.	Probe between here and J7 to measure the output voltage used to power the board. If DVCC is powered directly (remove the jumper from header J3), 3.3 V must be applied between here and J7.
J7	4-pin header	Ground voltage header **(WARNING)**	Probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally directly through DVCC.	Probe between J6 and here to measure the output voltage used to power the board. If DVCC is powered directly (remove the jumper from header J3), 3.3 V must be applied between J6 and here.
J8	2-pin header	Extra DVCC and GND connections **(WARNING)**	Header containing DVCC and ground.	For more info on the DVCC pin, see the description on J6. For more info on the ground pin, see the description on J7.
J9	4-pin header	Header containing MSP432 P7.0, 7.1, P7.2, and P7.3 pins **(WARNING)**	Probe here for P7.0, P7.1, P7.2, and P7.3 GPIO pins.	The P7.0, P7.1, and P7.2 pins are used for adjusting the contrast of the LCD. P7.3 is not used in this design. These pins are all port mappable. If the LCD is not needed, it can be disabled in software and R9, R15, R16, and R17 can be removed so that P7.0, P7.1, and P7.2 can be port mapped for other purposes.
J11	10-pin 2-row connector	JTAG: MSP432 programming header **(WARNING)**	Connect the MSP-FET- 432ADPTR adapter to this connector to program the MSP432 MCU.	The MSP-FET-432ADPTR is used to allow the MSP-FET tool to program the MSP432 device. One connector of the MSP-FET-432ADPTR adapter connects to the FET tool and the other connector connects to the JTAG connector of the MSP432 MCU. Note that the MSP432 has to be powered externally to program the MSP432 MCU. Since this header and the FET tool is not isolated, do not connect to this header when running off Mains and Mains is not isolated.
J13	2-pin header	Active energy pulses **(WARNING)**	Probe here for active energy pulses based on the shunt active power readings. This header has two pins: GND and ACT, which is where the active energy pulses are actually output.	This header is not isolated from AC mains, so do not connect measuring equipment here (especially when referencing the system from line) If it is desired to test the active power pulses, use the "ISO_ACT" pin of J15 instead since it is isolated.
J14	2-pin header	Reactive energy pulses **(WARNING)**	Probe here for active energy pulses based on the shunt active power reading. This header has two pins: GND and REACT, which is where the reactive energy pulses are actually output.	This header is not isolated from AC mains, so do not connect measuring equipment here (especially when referencing the system from line) If it is desired to test the reactive power pulses, use the "ISO_REACT" pin of J15 instead since it is isolated.
J15	4-pin header	Isolated pulses header	Probe here for the isolated active energy pulses and the isolated reactive energy pulses. Using this header for pulses is recommended, especially when referencing the system with respect to line.	This header has four pins: ISO_GND, ISO_REACT, ISO_ACT, and ISO_VCC. ISO_GND is the isolated ground for the energy pulses. ISO_VCC is the VCC connection for the isolated active and reactive energy pulses. ISO_ACT is where the isolated active energy pulses are output. ISO_REACT is where the isolated active energy pulses are output. This header is isolated from AC mains so it is safe to connect to a scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce the active energy pulses and reactive energy pulses at this header. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
J16	3-pin jumper header	RS-232 or RS-485 selection-power	Place a jumper at either the RS-232 or RS-485 positions depending on which of these two communication options are desired.	Put a jumper in the RS-232 position on this header, J17, and J18 to select RS-232 communication. Put a jumper in the RS-485 position on this header, J17, and J18 to select RS-485 communication.
J17	3-pin jumper header	RS-232 or RS-485 selection-TX	Place a jumper at either the RS-232 or RS-485 positions depending on which of these two communication options are desired.	Put a jumper in the RS-232 position on this header, J16, and J18 to select RS-232 communication. Put a jumper in the RS-485 position on this header, J16, and J18 to select RS-485 communication.
J18	3-pin jumper header	RS-232 or RS-485 selection-RX	Place a jumper at either the RS-232 or RS-485 positions depending on which of these two communication options are desired.	Put a jumper in the RS-232 position on this header, J16, and J17 to select RS-232 communication. Put a jumper in the RS-485 position on this header, J16, and J17 to select RS-485 communication.

表 3. Header Names and Jumper Settings (continued)

HEADER OR HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
J19	2-pin jumper header	TX_EN: RS-232 or RS-485 transmit enable **(WARNING)**	Place a jumper here to enable RS-232 or RS-485 transmissions.	
J20	2-pin jumper header	RX_EN: RS-232 or RS-485 receive enable **(WARNING)**	Place a jumper here to enable receiving characters using RS-232 or RS-485.	
J21	4-pin terminal block	RS-485 connection	Connection point for RS-485	To view the GUI using RS-485, connect the USB to RS-485 adapter here. 5 V must be provided externally on pin 1 of this header. Pin 2 of this header is the RS-485 ground, pin 3 is the B bus I/O line, and pin 4 is the A bus I/O line.
J22	2-pin terminal block	Mains voltage input **(WARNING)**	Line and neutral connection	This terminal block is connected to the line and neutral. Connect the terminal block position on the left (labeled "NEG" on the PCB) to the *neutral*, if referencing the shunt and system ground with respect to the *neutral*. Also, connect the terminal block position on the right (labeled "POS" on the PCB) to the line. Connect the terminal block position on the left (labeled "NEG" on the PCB) to the *line*, if referencing the shunt and system ground with respect to the *line*. Also, connect the terminal block position on the right (labeled "POS" on the PCB) to the *neutral*. If the system is referenced with respect to the *line*, note that all voltage samples obtained from the ADS131M04 device should be multiplied by –1 in the software to ensure that the phase shift between voltage and current is properly reflected for the power-related metrology readings. Also, only probe here if using equipment that can measure the Mains voltage.
J23	2-pin jumper header	ADS131M04 AVDD jumper **(WARNING)**	A short (either through jumper of ammeter) must be present at this jumper header for proper operation of the ADS131M04 device.	This header along with J24 allow measuring the current consumption of the ADS131M04 device.
J24	2-pin jumper header	ADS131M04 DVCC jumper **(WARNING)**	A short (either through jumper of ammeter) must be present at this jumper header for proper operation of the ADS131M04 device.	This header along with J23 allow measuring the current consumption of the ADS131M04 device.
J25	3-pin terminal block	Shunt connection **(WARNING)**	Shunt connections	This terminal block is connected to the output terminals of the shunt. This terminal block is a three-position terminal block with positions labeled "POS", "GND", and "NEG". For the gain of 32 used in this design, the differential voltage across the "POS" and "NEG" terminals of this terminal block should be less than ±37.5 mV. Do not connect a CT here since a burden resistor is not present for the circuitry of this channel like it is present for the J26 current circuitry.
J26	3-pin terminal block	CT connection **(WARNING)**	Current inputs after the CT sensor	This terminal block is a three-position terminal block but only the leftmost and rightmost positions are used. The center position, which is connected to GND, is not connected to the CT. Connect the positive terminal of the CT to the terminal block position on the most right, which is labeled "POS". Connect the negative terminal of the CT to the terminal block position on the most left, which is labeled "NEG". Before performing any test, verify that this terminal block is securely connected to both output leads of the CT.
J27	8-pin header	ADS131M04 MSP432 communication header **(WARNING)**	Probe here for connections to the chip select signal, SPI signals, $\overline{\text{RST}}$ signal, CLKIN signal, and $\overline{\text{DRDY}}$ signal of the ADS131M04 device.	The $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin of the ADS131M04 device is used to reset the ADS131M04 device. When initializing the ADS131M04, the MSP432 MCU drives this pin to reset the ADS131M04. The $\overline{\text{DRDY}}$ pin of the ADS131M04 device is used to alert the MSP432 MCU that new current samples are available. The CLKIN pin is fed from the SMCLK clock output of the MSP432 MCU to the ADS131M04 device, which divides the clock down to produce the used modulator clock. This header is not isolated from AC mains, so do not connect measuring equipment when running from Mains, unless isolators external to the reference design are available. The pin mappings on this header are as follows: ● Pin 1: SMCLK (ADS131M04 CLKIN pin) ● Pin 2: SPI DOUT (ADS131M04 DIN pin/SIMO) ● Pin 3: SPI DIN (ADS131M04 DOUT/ pinSOMI ● Pin 4: SPI CLK (ADS131M04 SCLK pin) ● Pin 5: ADS DRDY (ADS131M04 $\overline{\text{DRDY}}$ pin) ● Pin 6: SPI CS (ADS131M04 $\overline{\text{CS}}$ pin) ● Pin 7: RST SYNC (ADS131M04 $\overline{\text{SYNC}}$/$\overline{\text{RESET}}$ pin) ● GND

2.4.1.3 Software

The MSP432 software used for evaluating this design is test software. 2.3.2.3 discusses the features of the test software, which provides insights on how to implement custom software for metrology testing.

2.4.2 Testing and Results

2.4.2.1 Test Setup

2.4.2.1.1 SVS and Cap-Drop Functionality Testing

In addition to metrology accuracy testing, functionality testing was done on the TPS3840 SVS device. For the TPS3840 testing, the board is powered by connecting an external power supply directly to DVCC (a jumper should not be placed on J2 to properly power DVCC directly) and the output voltage of the power supply is slowly varied from 3.3 V down to 1.9 V. The threshold voltage at which the MSP432 MCU is reset by the TPS3840 device, which is referred to as the negative voltage threshold, is logged. After the negative voltage threshold is reached, the power supply output voltage is slowly increased from 1.9 V back to 3.3 V. The voltage at which the reset is released, which is equal to the negative voltage threshold plus hysteresis voltage, is logged as well.

A few functionality tests were also performed on the TPS7A78-based cap-drop supply of this design. In the first test, the output voltage from the TPS7A78 was measured as the AC mains input varied from 75 V to 270 V. The TPS7A78 was connected directly to DVCC for this test by placing a jumper between the LDO_OUT and DVCC positions on J3.

In addition, the power supply was tested to verify that 50-mA loads could be powered. This test was conducted when DVCC was connected directly to the TPS7A78 output with an AC mains input of 230 V. Under normal operation, the design consumes between 14–18 mA, which is well below the maximum output current for which the cap-drop was designed. To create a current consumption of 50 mA from the design, four of the five LEDs on the board were turned ON, which led to a system current consumption of around 50 mA. With the board set to consume about 50 mA from the cap-drop supply, the output voltage from the TPS7A78 was measured.

The resulting DVCC voltage from doing an OR of the TPS7A78 power supply with the auxiliary power supply at header J1 was also tested. This test was performed by placing a jumper between the DIODE and DVCC positions on J3. The measured voltage is less than the output voltage from the TPS7A78 because of the voltage drop across the diode used to OR the power supplies. For this test, an AC mains input of 230 V was used and the system was operating under normal conditions, which would consume from 14–18 mA.

2.4.2.1.2 Electricity Meter Metrology Accuracy Testing

To test for metrology accuracy, a source generator was used to provide the voltage and current to the system at the proper locations mentioned in 2.4.1.2.1. Additionally, a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz are used. During all of the tests, the board is powered directly using the TPS7A78-based power supply by placing a jumper between the LDO_OUT and DVCC positions on J3. In addition, the system and shunt is referenced with respect to the neutral for most of the tests.

When the voltage and current are applied to the system, the system outputs the active energy pulses and reactive energy pulses at a rate of 6400 pulses/kWh. The pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the active and reactive energy output pulse of the system. In this reference design, active energy error testing, reactive energy error testing, voltage variation testing, and frequency variation testing are performed after performing energy gain calibration, phase calibration, and energy offset calibration as described in 2.4.2.1.4.2.2.

Reactive energy testing is performed using a 200-μΩ shunt for the current readings. Active energy testing is performed using both the shunt and CT channel on the board for the current readings. Since the default channel used for active energy pulses is the shunt channel, the software was modified to use the CT channel as the default channel for pulse outputs to test the active energy error when using the CT channel. For the active energy tests performed using the shunt channel, both a 200-μΩ shunt and a 100-μΩ shunt were tested.

For the active energy error and reactive energy error testing on the shunt channel, current is varied from 50 mA to 90 A when testing using the shunt for measuring current. When performing the CT active energy test, conversely, current is varied from 50 mA to 100 A . For active energy error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current waveforms fed to the reference design. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts. For reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used and reactive energy error is plotted instead of active energy error.

In performing metrology tests, two sets of voltage tests were also performed, both of which were performed with a 200-μΩ shunt. In the first test, the 230-V nominal voltage was varied by ±10% at different currents and power factors. The resulting active energy error at each test point was then logged. For the second test, the active energy error was plotted when voltage was varied over a larger voltage range at unity power factor. Specifically, voltage was varied from 75 to 270 V. Testing beyond 270 V can also be done; however, this requires the 275-V varistors to be removed from the design and replaced with varistors that are rated for a higher voltage.

Another set of tests performed are frequency variation tests, which are performed using a 200-μΩ shunt. For this test, the frequency is varied by ±2 Hz from its 50-Hz nominal frequency. This test is conducted at 0.5 A and 10 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error under these conditions are logged.

2.4.2.1.3 Current-Detection Mode Testing

For testing current-detection mode, the trigger current on the line and neutral channel was tested as well as the average current consumption of the ADS131M04 device. These tests were performed using the register settings mentioned in 2.3.2.3.1.7.

Before performing trigger current testing, the ADS131M04 offset registers are used to subtract the average ADC offset on the shunt and CT current channels. This is necessary because the shunt and CT current channels have different PGA gain settings(PGA gain=1 for CT and PGA gain=32 for shunt). At these different gains, the channels would have a difference in ADC offset so offset calibration was performed to provide better matching between the two current channels, which is necessary to get consistent results between the two channels using only one threshold value. Based on the test settings,

the ADS131M04 is then placed in current detection. After placing the device in current-detection mode, the input current is varied from 50 mA to 10 A on the shunt channel(while no current is on the CT channel) to see at which current would the ADS131M04 start indicating to the MSP432 MCU of tampering. This first current is logged in the test results. A similar test is done on the CT channel as well to determine its triggering current in current-detection mode.

Two sets of current-detection current-consumption tests were performed in this design. For both tests, the ADS131M04 and the rest of the board are powered separately with the two power supplies sharing the same ground connection. The ADS131M04 was powered at 3.3 V by the N6705 power analyzer, which plots the average current consumption of the ADS131M04. The rest of the board was powered at 3.3 V from a regular power supply.

In the first test, the current consumption of the ADS131M04 is measured during current-detection mode for different combinations of enabled channels. The number of channels used in current-detection mode affects the current consumption of the device in this mode. In addition, for the scenario where current-detection mode is enabled for two channels, the pairings of enabled channels can also affect the current consumption. There is shared circuitry between channels 0 and 1 as well as between channels 2 and 3 that are on if one of the two channels in these pairs are enabled. As a result, the lowest current consumption is expected for the two-enabled channel case when channels 0 and 1 are enabled or when channels 2 and 3 are enabled. In this design, channels 1 and 2 are used for the current channel so these two channels are the two channels that are potentially enabled in current-detection mode; however, a lower current consumption is expected if the design was modified to use channels 0 and 1 for the current and channel 2 for voltage since the shared circuitry for channels 3 and 4 could be turned off in current-detection mode.

For the second current consumption test, the average current consumption was measured when current-detection mode is entered once every 10 seconds ($t_{CD\_mode\_period}$ = 10) and once every 64 seconds ($t_{CD\_mode\_period}$ = 64). Current-detection mode is enabled in the shunt (channel 1) and CT (channel 2) channels for this test. In this test, the ADS131M04 alternates between standby mode and current-detection mode. Since the current consumption in standby mode and current-detection mode are significantly different, the standby mode current consumption and current-detection mode current-consumption had to be taken separately using two different current range settings on the N6705 power analyzer. 図 27 shows an example reading for standby mode, where an average current of 1.429 µA is measured. The duration the device is in current-detection mode is estimated by measuring the current consumption positive pulse width. 図 28 shows an example reading for current-detection mode, where an average current of 648.762 µA and a current-detection duration of 95.23 ms are measured. Using this estimated current-detection duration, the average current during the estimated current-detection duration, and the average standby mode current consumption, the total average current consumption value across time is estimated. This average current consumption test was performed on three separate boards and averaged together for the total average current consumption test results shown in this design. The estimated current-detection duration and average standby mode current from this test was also used to estimate the average current consumption for the different combinations of enabled channels used in the first current-detection current-consumption test.

図 27. Example Standby Mode Current Consumption Reading

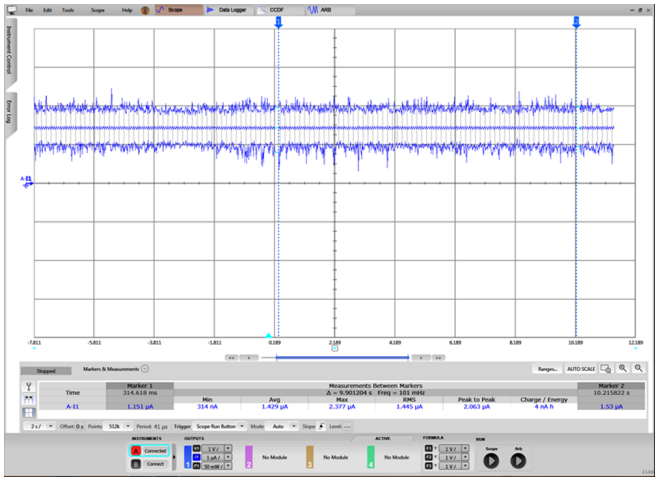
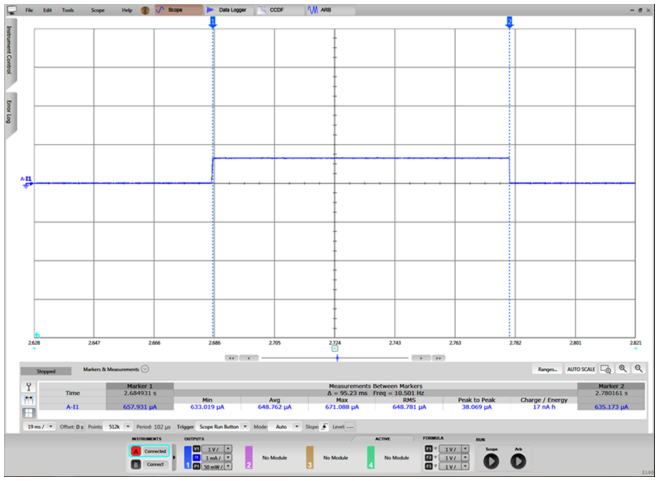


図 28. Example Current-Detection Mode Current Consumption Reading



2.4.2.1.4 Viewing Metrology Readings and Calibration

This section describes the methods used to verify the results of this design with the test software.

2.4.2.1.4.1 Viewing Results From LCD

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. 表 4 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

表 4. Displayed Parameters

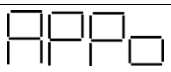
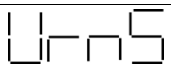
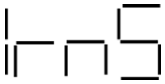
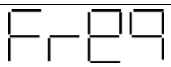
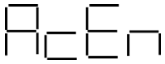
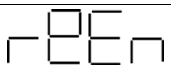
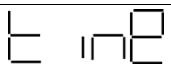
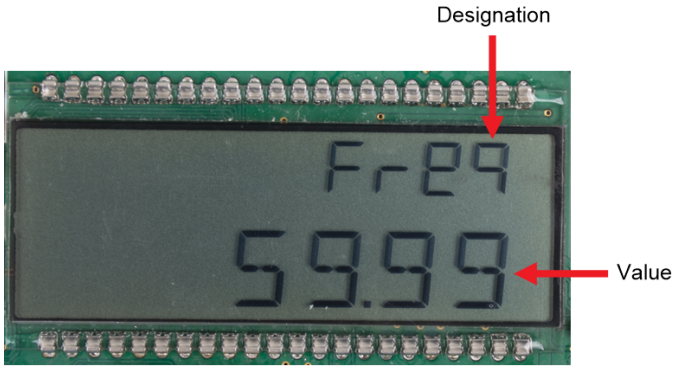
PARAMETER NAME	DESIGNATION	UNITS
Active power		Watt (W)
Reactive power		Volt-Ampere Reactive (var)
Apparent power		Volt-Ampere (VA)
Power factor		Constant between 0 and 1
Voltage		Volts (V)
Current		Amps (A)
Frequency		Hertz (Hz)
Total consumed active energy		kWh
Total consumed reactive energy		kVarh
Time		Hour:minute:second
Date		Year:month:day

図 29 shows an example of the measured frequency of 59.99 Hz displayed on the LCD.

図 29. LCD



2.4.2.1.4.2 Calibrating and Viewing Results From PC

2.4.2.1.4.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

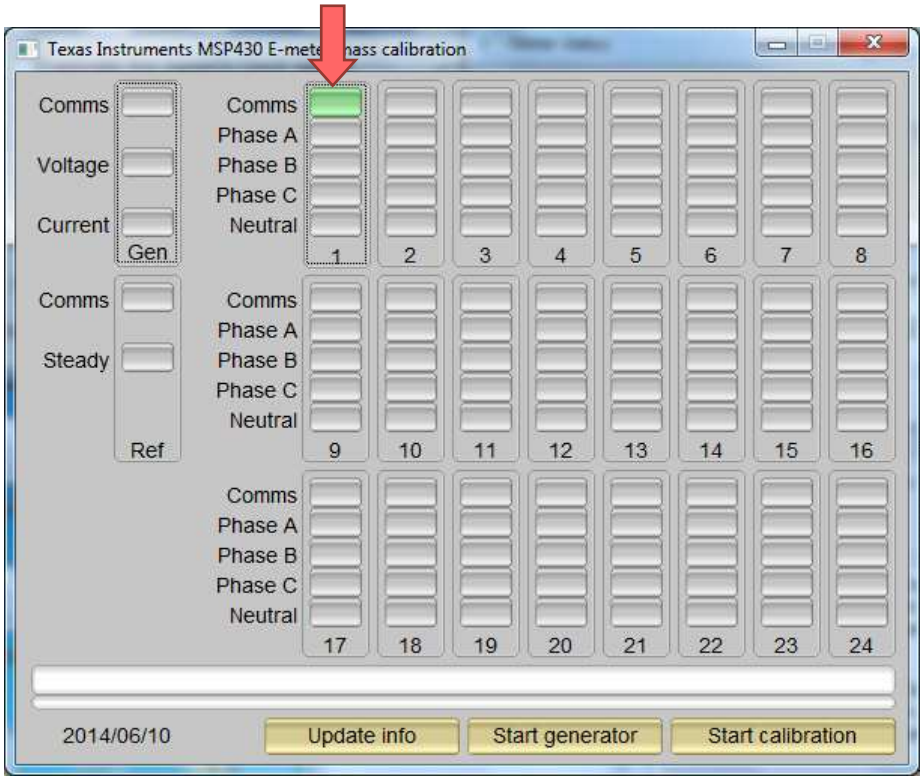
1. Select whether to use the RS-485 or RS-232 connection for communication to the PC GUI. This selection is done by placing 3 jumpers on jumper headers J16, J17, and J18. To select the RS-485 communication option, put the jumpers on the top two leftmost pins (labeled RS-485 on the board) of these three headers. To select the RS-232 communication option, put the jumpers on the two rightmost pins (labeled RS-232 on the board) of the three headers.
2. Connect the reference design to a PC
   - RS-232 option: Connect the reference design to a PC using a RS-232 cable. If the PC does not have a RS-232 adapter, use a serial RS-232 adapter. The RS-232 adapter should create a COM port on the PC when it is plugged in.
   - RS-485 option: Use a USB to RS-485 adapter to communicate between the PC GUI and the RS-485 port on this design. The USB to RS-485 adapter should create a COM port on the PC when it is plugged in. The other end of the adapter should have wires for the RS-485 Data A and Data B connections as well as a GND connection and a 5-V power connection., Connect all these wires to the J21 screw terminal block of the design according to the connection labels next to the terminal block pins. For testing this circuit, the following USB to RS-485 adapter is specifically used: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_USB_RS485_CABLES.pdf. For this specific adapter, the Data A connection is orange, the Data B connection wire is yellow, the GND connection is black, and the 5-V power connection is red.
3. Open the GUI folder and open *calibration-config.xml* in a text editor.
4. Change the *port name* field within the *meter* tag to the COM port connected to the system. As 図 30 shows, this field is changed to *COM7*.

図 30. GUI Configuration File Changed to Communicate With Energy Measurement System

```
260       </correction>
261     </phase>
262     <temperature/>
263     <rtc/>
264   </cal-defaults>
265   <meter position="1">
266     <port name="com7" speed="9600"/>
267   </meter>
268   <reference-meter>
269     <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270     <type id="chroma-66202"/>
271     <log requests="on" responses="on"/>
272     <scaling voltage="1.0" current="1.0"/>
273   </reference-meter>
```

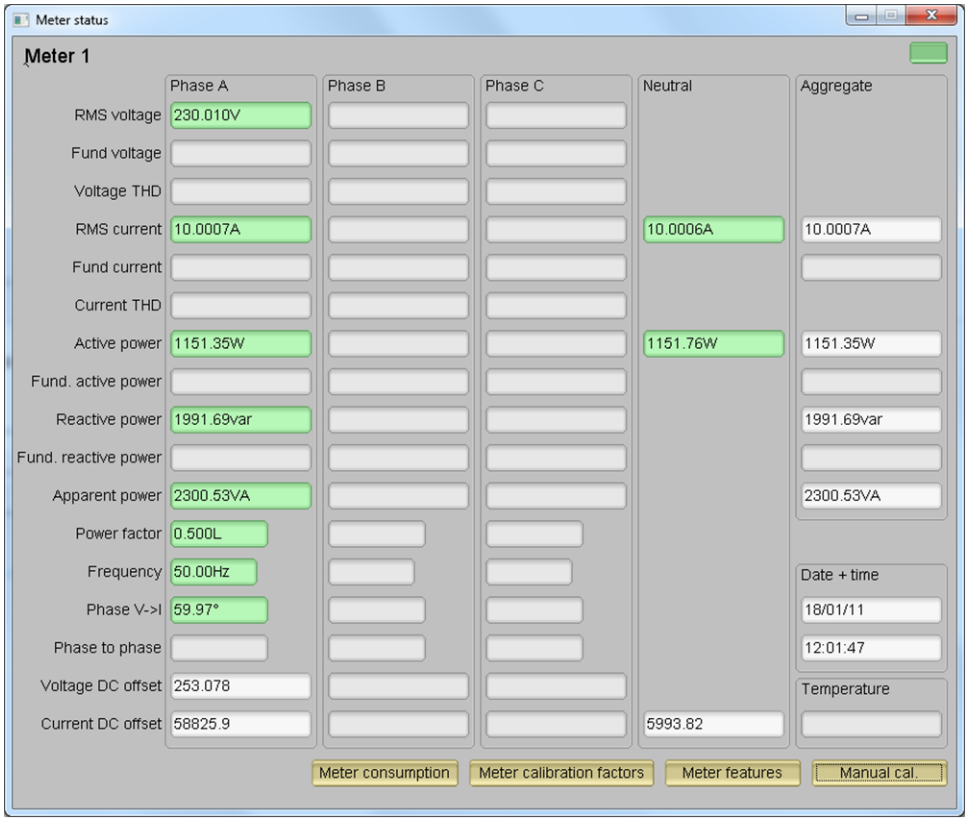
5. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the reference design, the GUI opens (see 図 31). If the GUI connects to the design properly, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

図 31. GUI Startup Window



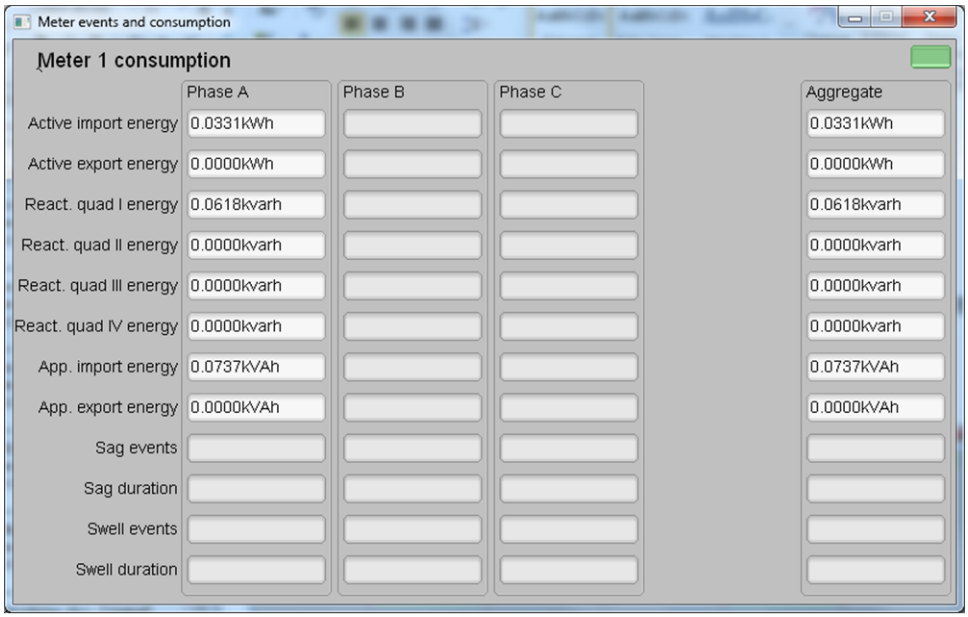
Upon clicking on the green button, the results window opens (see 図 32). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively. Note that by default, the column in the GUI labeled "Phase A" is actually the shunt channel and the column labeled "Neutral" is actually the CT channel. If the system and shunt is referenced with respect to the neutral, the shunt would actually measure the neutral current and the CT would measure the line current, unlike how the GUI is labeled.

図 32. GUI Results Window



From the results window, the total-energy consumption readings can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as 図 33 shows.

図 33. Meter Events and Consumption Window



From the results window, the meter settings can be viewed by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

2.4.2.1.4.2.2 Calibration

Calibration is key to any meter performance, and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase design.

The GUI used for viewing results can easily be used to calibrate the design. During calibration, parameters called calibration factors are modified in the test software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, active power offset (erroneously called voltage AC offset in the GUI), current scaling factor, reactive power offset (erroneously called current AC offset in the GUI), power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The power offset is used to subtract voltage to current crosstalk, which appears as a constant power offset and causes greater

inaccuracies at lower currents. Note that offset calibration was only used for the shunt channel and not the CT channel. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter SW is flashed on the MSP432 devices for the first time, default calibration factors are loaded into these calibration factors. These values are modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted.

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with 2.4.1.2.1, and the energy pulses connected to the reference meter.

2.4.2.1.4.2.3 Gain Calibration

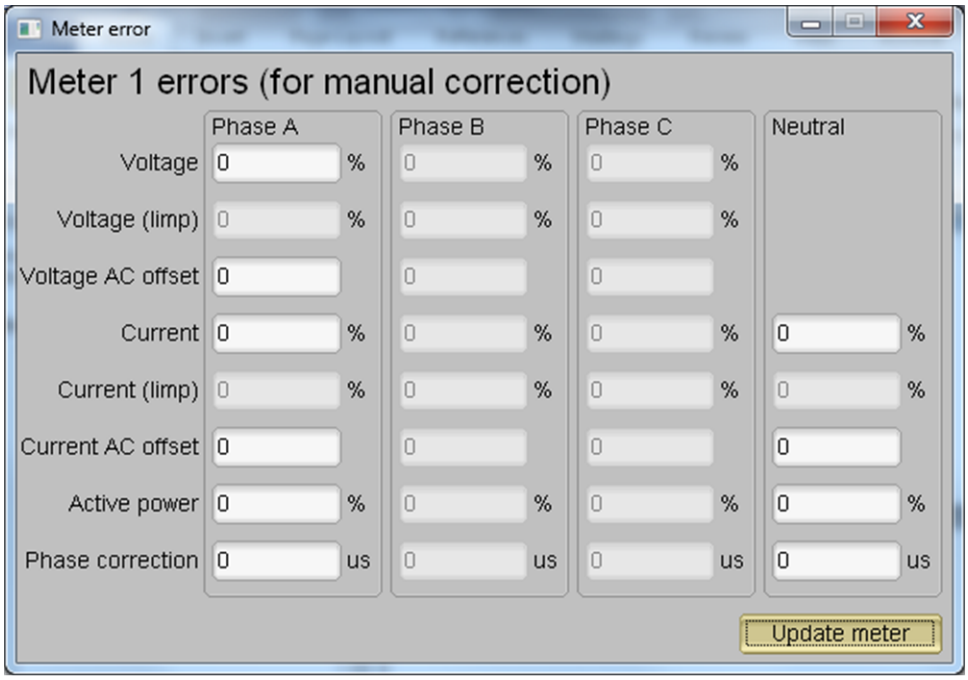
Usually, gain correction for voltage and current can be done simultaneously. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power.

2.4.2.1.4.2.4 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply the desired voltage and current. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between voltage and current. For example, for 230 V, 10 A, 0º (PF = 1).
3. Click on the *Manual cal.* button that 図 32 shows. The screen in 図 34 pops up:

図 34. Manual Calibration Window



4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated using 式 15:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (15)$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltage and currents on the GUI settle immediately to the desired voltages and currents.

2.4.2.1.4.2.5 Active Power Gain Calibration

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating the active energy % error as is done with voltage and power can be done, avoid using this method because it is not the most accurate.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, complete the following steps:

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source.
3. Repeat Step 1 to Step 3 from 2.4.2.1.4.2.4 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
5. Enter the error obtained in Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

2.4.2.1.4.2.6 Offset Calibration

After performing gain calibration, if the accuracy at low currents is not acceptable, offset calibration could be done. Offset calibration removes any crosstalk, such as the crosstalk to the current channels of a phase from the line voltages.

To perform active power offset calibration for a phase, add the offset to be subtracted from the active power reading (in units of mW) to the current value of the active power offset (labeled "voltage AC off" in the meter calibration factors window) and then enter this new value in the *Voltage AC offset* field in the Manual Calibration window. As an example, if the "voltage AC off" has a value of 200 (0.2 W) in the meter calibration window, and it is desired to subtract an additional 0.300 mW, then enter a value of 500 in the *Voltage AC offset* field in the Manual Calibration window. After entering the value in the *Voltage AC offset* field in the Manual Calibration window, press "Update meter".

To perform reactive power offset calibration for a phase, a similar process is followed as the process used to perform active power offset calibration. Add the offset to be subtracted from the reactive power reading (in units of mvar) to the current value of the reactive power offset (labeled "Current AC offset" in the meter calibration factors window) and then enter the value in the *Current AC offset* field in the Manual Calibration window. After entering the value in the *Current AC offset* field in the Manual Calibration window, press "Update meter".

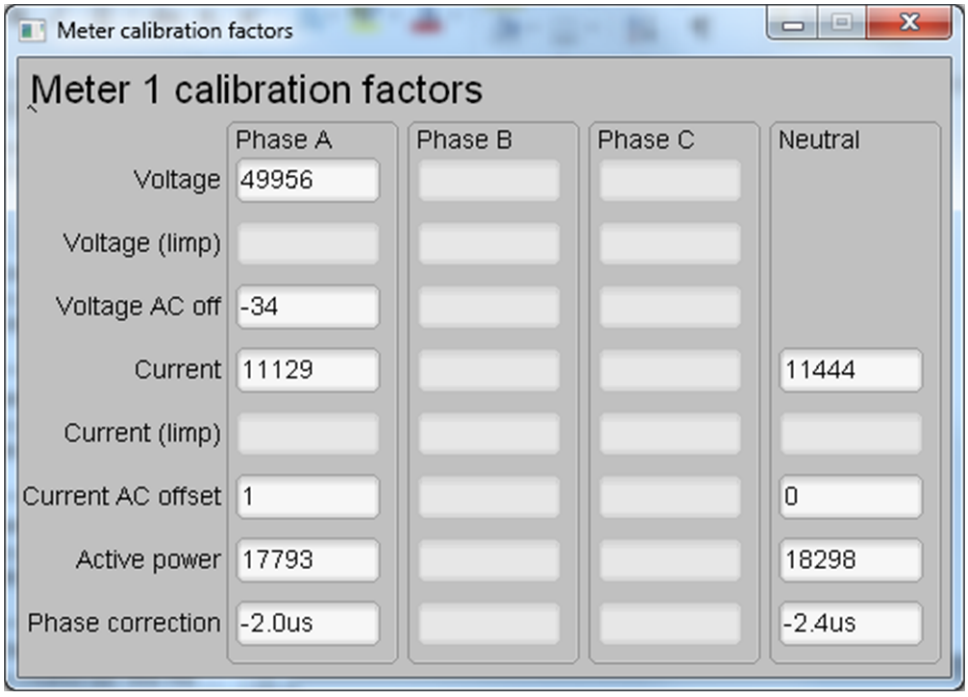
2.4.2.1.4.2.7 Phase Calibration

After performing power gain correction, do the phase calibration. To perform phase correction calibration, complete the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 1 through Step 3 from 2.4.2.1.4.2.4 using the identical voltages and currents used in that section.
2. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
3. If the error from Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   a. Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error requires a positive (negative) number as correction.
   b. Click on the *Update meter* button and monitor the error values on the reference meter.
   c. If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   d. Change the phase now to −60° and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

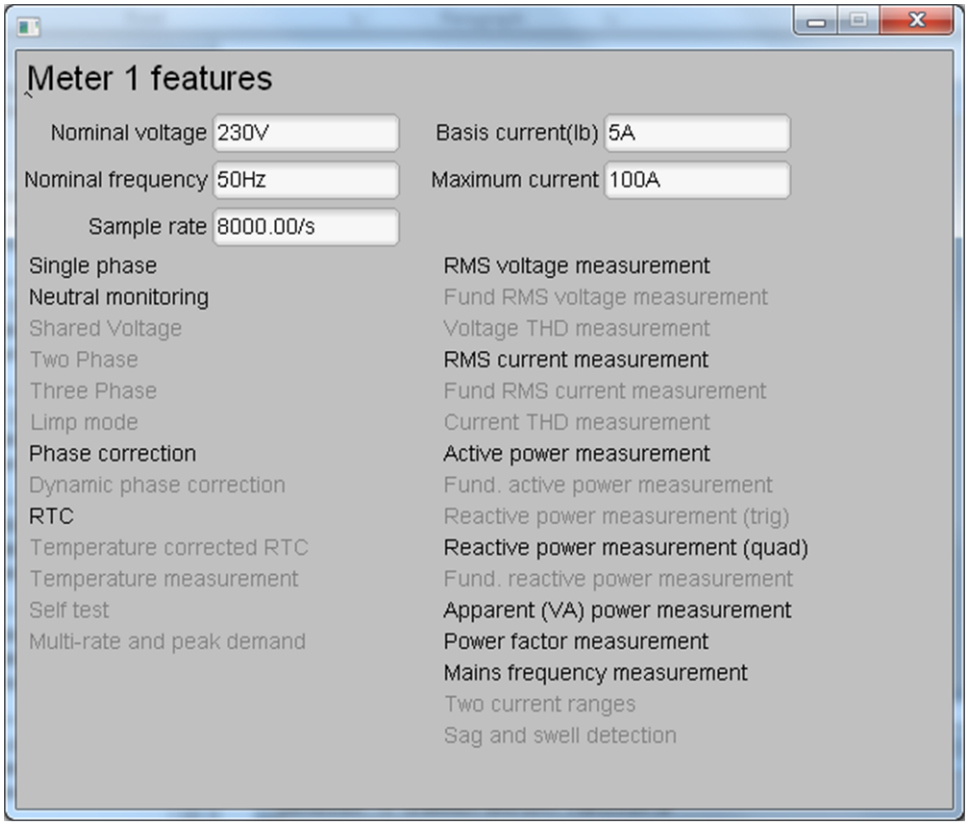
After performing phase calibration, calibration is complete. The new calibration factors (see 図 35) can be viewed if desired by clicking the *Meter calibration factors* button of the GUI metering results window in 図 32. For these displayed calibration factors, note that the "Voltage AC off" parameter actually represents the active power offset (in units of mW) subtracted from each measurement and the "Current AC offset" parameter actually represents the reactive power offset subtracted (in units of mvar) from reactive power readings.

図 35. Calibration Factors Window



View the configuration of the system by clicking on the *Meter features* button in 図 32 to get to the window that 図 36 shows.

図 36. Meter Features Window



2.4.2.2 Test Results

2.4.2.2.1 SVS and TPS7A78 Functionality Testing Results

表 5. SVS Test Results

CONDITION	MEASURED VOLTAGE (V)	DATA SHEET TYPICAL VOLTAGE VALUE (V)
Negative voltage threshold, VIT–	2.00 V	2.00 ±1% V
Positive voltage threshold, VIT+ = VIT– + VHYS	2.11 V	2.10 V
Hysteresis voltage, VHYS = VIT+ – VIT–	2.11 – 2.00 = 0.11 V	2.1 – 2.0 = 0.10 V

The measured values of VIT– and VHYS, match closely with the expected values from the data sheet.

表 6. TPS7A78 Output Voltage vs. Input AC Voltage

INPUT AC VOLTAGE (V_{RMS})	TPS7A78 OUTPUT VOLTAGE
75	3.278 V
100	3.278 V
110	3.278 V
120	3.278 V
150	3.277 V
180	3.277 V
210	3.277 V
220	3.277 V
230	3.277 V
240	3.277 V
250	3.277 V
260	3.277 V
270	3.277 V

表 7. TPS7A78 Output Voltage vs. Load Current

LOAD CURRENT	TPS7A78 OUTPUT VOLTAGE
16 mA (normal operation)	3.277 V
50 mA	3.275 V

The TPS7A78 voltage does not vary that much across AC input voltage and load current.

表 8. Voltage When DVCC is Connected to TPS7A78 Through Diode(Jumper Placed Between "DIODE" and "DVCC" on J3)

CONDITION	VOLTAGE
TPS7A78 output voltage	3.277 V
DVCC voltage	2.948 V
Voltage drop across diode	0.329 V

The voltage drop due to connecting the TPS7A78 to DVCC through a diode is 0.33 V. For a larger DVCC output voltage, the 3.3-V variant of the TPS7A78 used in this design can be replaced with the 3.6-V variant of the TPS7A78.

2.4.2.2.2 Electricity Meter Metrology Accuracy Results

For the following test results, gain, phase, and offset calibration are applied to the meter. At higher currents, the % error shown is dominated by shunt resistance drift caused by the increased heat generated at high currents.

表 9. Active Energy % Error Versus Current, 200-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.05	0.0625	0.137	0.034
0.10	0.036	0.048	0.072
0.25	–0.0027	0.041	0.058
0.50	–0.022	0.004	0.022
1.00	–0.0123	0.004	–0.014
2.00	–0.0293	–0.024	–0.019
5.00	–0.0123	–0.024	0.001
10.00	–0.0127	–0.023	0.0003
20.00	–0.0233	–0.032	–0.032
30.00	–0.019	–0.019	–0.028
40.00	–0.025	–0.026	–0.032
50.00	–0.03	–0.05	–0.03
60.00	–0.058	–0.075	–0.062
70.00	–0.088	–0.117	–0.092
80.00	–0.1243	–0.164	–0.151
90.00	–0.181	–0.224	–0.219

図 37. Active Energy % Error Versus Current, 200-µΩ Shunts

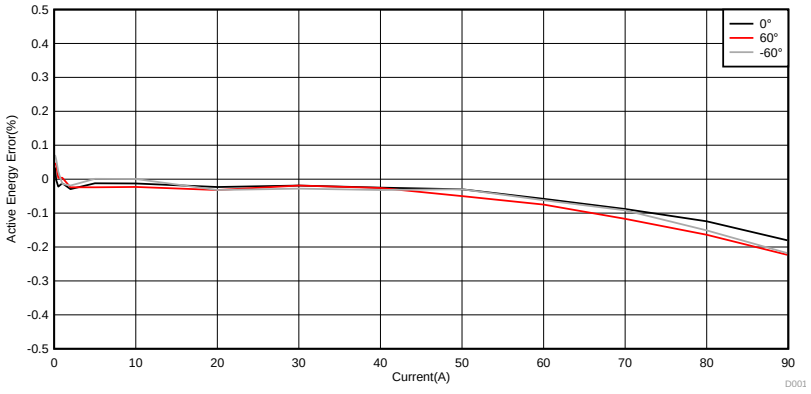


表 10. Active Energy % Error Versus Current, 100-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.05	0.147	0.216	0.209
0.10	–0.042	–0.052	–0.058
0.25	0.035	0.093	0.0175
0.50	0.0453	0.037	–0.009
1.00	0.013	0.0377	–0.017
2.00	–0.0167	0.0303	–0.011
5.00	0.006	0.032	–0.014
10.00	0.009	0.034	–0.014
20.00	–0.007	0.032	–0.045
30.00	–0.002	0.04	–0.036
40.00	–0.007	0.032	–0.007
50.00	–0.004	0.017	–0.035
60.00	–0.019	–0.002	–0.058
70.00	–0.053	–0.032	–0.092
80.00	—0.083	–0.07	–0.143
90.00	–0.122	–0.113	–0.19

図 38. Active Energy % Error Versus Current, 100-µΩ Shunts

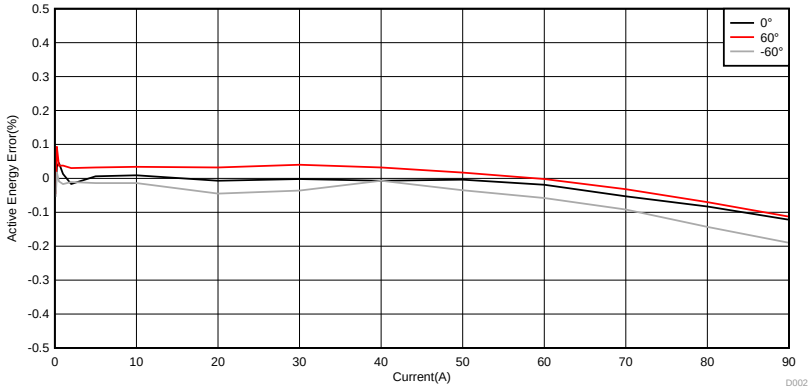


表 11. CT Channel Active Energy % Error Versus Current

CURRENT (A)	0°	60°	–60°
0.05	0.01	–0.004	–0.011
0.10	0.007	0.019	0.005
0.25	–0.004	0.017	–0.021
0.50	0.006	0.024	–0.017
1.00	0.009	0.027	–0.009
2.00	–0.011	0.019	–0.041
5.00	0.006	0.006	0.001
10.00	0.0015	–0.004	0.004
20.00	–0.015	–0.019	0.006
30.00	–0.011	–0.045	0.023
40.00	–0.013	–0.07	0.038
50.00	–0.004	–0.081	0.083
60.00	–0.005	–0.092	0.087
70.00	–0.001	–0.0997	0.109
80.00	0.013	–0.106	0.115
90.00	0	–0.102	0.134
100.00	0.018	–0.111	0.147

図 39. CT Channel Active Energy % Error Versus Current

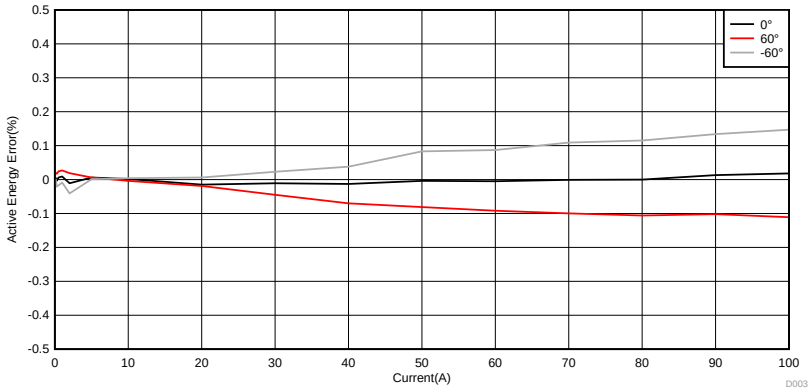


表 12. Reactive Energy % Error Versus Current, 200-µΩ Shunts

CURRENT (A)	30°	60°	–30°	–60°
0.10	–0.035	0.001	0.118	0.056
0.25	0.032	0.008	–0.022	0.008
1.00	0.009	0.014	0.006	–0.0013
5.00	0.017	0.006	0.011	0.006
10.00	0.0195	0.014	0.006	0.006
30.00	0.006	0.0017	0.006	0.006
50.00	0.017	–0.004	–0.009	–0.0115
70.00	–0.019	–0.0415	–0.063	–0.085
90.00	–0.1	–0.133	–0.151	–0.194

図 40. Reactive Energy % Error Versus Current, 200-µΩ Shunts

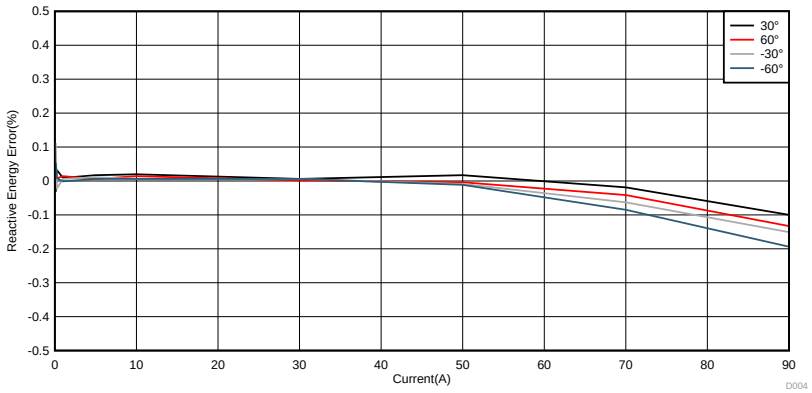


表 13. Active Energy Measurement Error Versus Voltage, 75 to 270 V, 200-µΩ Shunts

VOLTAGE (V)	%ERROR
75	–0.119
100	–0.101
110	–0.093
120	–0.091
150	–0.068
180	–0.0435
210	–0.0233
220	–0.014
230	0.003
240	0.0053
250	0.006
260	0.017
270	0.02

図 41. Active Energy Measurement Error Versus Voltage, 75 to 270 V, 200-µΩ Shunts

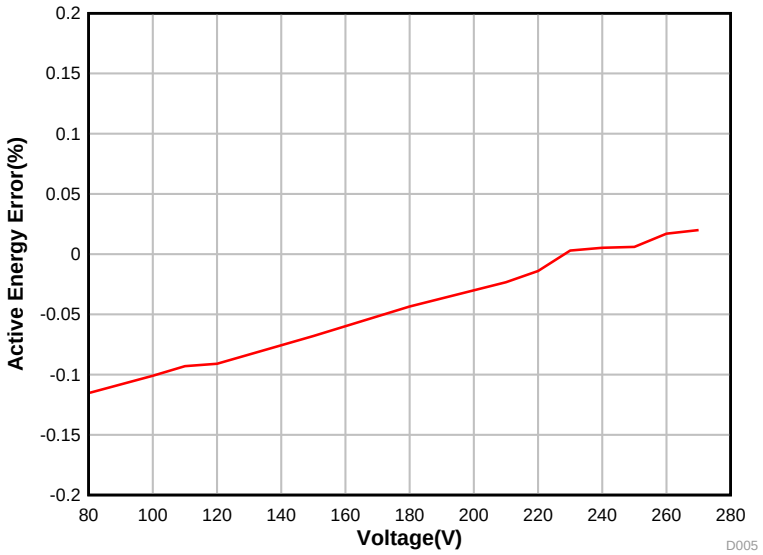


表 14. Cumulative Active Energy Measurement Error Versus Voltage, ±10% Nominal Voltage

VOLTAGE (V)	0°, 10 A	60°, 10 A	300°, 10 A	0°, 0.5 A	60°, 0.5 A	300°, 0.5 A
207	–0.028	–0.045	–0.012	–0.0073	0.017	0.027
230	–0.01	–0.022	0.004	–0.004	–0.007	–0.012
253	0.006	–0.004	0.011	0.011	–0.009	0.011

表 15. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency, 200-µΩ Shunts

CONDITIONS	48 Hz	50 Hz	52 Hz
0.5 A, 0	0.009	0.001	0.006
0.5 A, 60	0.001	–0.012	–0.017
0.5 A, 300	0.034	0.045	0.014
10 A, 0	–0.007	–0.011	–0.009
10 A, 60	–0.022	–0.0245	–0.027
10 A, 300	0.006	0.004	–0.001

2.4.2.2.3 Current-Detection Mode Results

表 16. Current-Detection Current-Consumption vs. Number of Enabled Channels

NUMBER OF ENABLED CHANNELS	CURRENT-DETECTION MODE CURRENT	AVERAGE CURRENT ESTIMATE AT $t_{CD\_mode\_period}$=10	AVERAGE CURRENT ESTIMATE AT $t_{CD\_mode\_period}$=64
2 (ch 1 and 2)	626.822 µA	7.421 µA	2.385 µA
2 (ch 0 and 1)	565.645 µA	6.837 µA	2.293 µA
1 (ch 2)	386.59 µA	5.128 µA	2.026 µA
1 (ch 1)	397.716 µA	5.234 µA	2.043 µA
1 (ch 0)	391.505 µA	5.175 µA	2.034 µA

When Channel 0 and 1 are enabled, the current consumption is smaller than when channel 1 and 2 are enabled because enabling only channel 0 and 1 allows the shared circuitry between channels 2 and 3 to be turned off. In addition, if current detection is only performed on one channel instead of the two channels used in this design, the average current consumption can be reduced.

表 17. Average Current Consumption When Current-Detection Mode is Entered Once Every 10 seconds

STANDBY MODE	CURRENT CONSUMPTION	DURATION ESTIMATE
Average from standby mode trials on 3 boards	1.452 µA	9904.548 ms
Average from current-detection mode trials on 3 boards	636.155 µA	95.453 ms
Total average current consumption	7.510 µA	10000 ms

表 18. Average Current Consumption When Current-Detection Mode is Entered Once Every 64 seconds

STANDBY MODE	CURRENT CONSUMPTION	DURATION ESTIMATE
Average from standby mode trials on 3 boards	1.452 µA	63904.548 ms
Average from current-detection mode trials on 3 boards	636.155 µA	95.453 ms
Total average current consumption	2.399 µA	64000 ms

The minimum triggering current for the shunt and CT channels was found to be 0.6 A and 1.2 A when testing was performed on one of these boards.

3 Design Files

3.1 Schematics

To download the schematics, see the design files at TIDA-010036.

3.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010036.

3.3 PCB Layout Recommendations

For this design, the following general guidelines must be followed:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially near the ADS131M04 device. In this design, there is a ground plane on both the top and bottom layer; for this situation, ensure that there is good stitching between the planes through the liberal use of vias.
- Keep the two traces to the inputs of an ADC channel symmetrical and as close as possible to each other.
- For the ADS131M04 device, place the 0.1-µF capacitor closer to the AVDD pin than the 1-µF capacitor. Do the same thing also for the 0.1-µF and 1-µF capacitors connected to DVDD.
- Note that the order of the AINxP and AINxN pins on the ADS131M04 switches when going from one converter to another. This swapped order is dealt with in this design by swapping the connection order of the wires connected to the voltage and current terminals.
- Minimize the length of the traces used to connect the crystal to the MCU. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and avoid placing any traces underneath the crystal. Also, keep high-frequency signals away from the crystal.
- Use wide traces for power-supply connections.
- Use a different ground plane for the isolated RS-232 and RS-485. This other ground plane is at the potential of the RS-232 and RS-485 ground and not the GND used elsewhere in the board.
- Ensure that the recommended clearance and creepage spacing are met for the ISO7731B and ISO7720 isolation devices in this design.

3.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010036.

3.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010036.

3.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010036.

3.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010036.

4 Related Documentation

1. Texas Instruments, *ADS131M04 4-Channel, Simultaneously-Sampling, 24-Bit, Delta-Sigma ADC Data Sheet*
2. Texas Instruments, *TPS7A78 120-mA, Smart AC/DC Linear Voltage Regulator Data Sheet*
3. Texas Instruments, *MSP432P411x, MSP432P401x SimpleLink™ Mixed-Signal Microcontrollers Data Sheet*
4. Texas Instruments, *TPS3840 Nano Power, High Input Voltage Supervisor With $\overline{MR}$ and Programmable Delay*
5. Texas Instruments, *THVD1500 500 kbps RS-485 Transceivers With ±8-kV IEC ESD Protection*
6. Texas Instruments, *ISO7731B High-Speed, Basic Insulation Triple-Channel Digital Isolator*
7. Texas Instruments, *TRS3232E 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ±15-kV IEC ESD Protection Data Sheet*

4.1 商標

4.2 Third-Party Products Disclaimer

5 About the Author

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