**TI Precision Designs: Verified Design**

5% Error, 0.5-4.5 V Input, +/-2 A Output, Bridge-Tied-Load (BTL) Voltage-to-Current (V-I) Converter

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**Circuit Description**

This bridge-tied load (BTL) voltage-to-current (V-I) converter circuit creates a bidirectional current source used to drive a floating load from a single-ended source. The circuit makes use of an internal output current monitor circuit (IMON) in a specialty power amplifier. The V-I transfer function is accomplished by using the IMON current as the feedback for the first amplifier. The second amplifier inverts the output of the first amp to achieve the BTL operation which doubles the voltage swing and slew rate across the load, and allows for a bidirectional output from a single-ended power supply.

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**Design Resources**

- [Design Archive](#)
- [TINA-TI™ SPICE Simulator](#)
- [OPA569 Product Folder](#)
- [REF5025 Product Folder](#)

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- [TI Precision Designs Library](#)

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**Diagram**

- [Circuit Diagram](#)

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[5% Error, 0.5-4.5 V Input, +/-2 A Output, BTL V-I Converter](#)
1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V dc
- Input: 0.5 - 4.5 V dc, zero-scale output at 2.5 V dc
- Output: +/-2 A dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

<table>
<thead>
<tr>
<th></th>
<th>Goals</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset (%FSR)</td>
<td>1</td>
<td>0.033</td>
<td>0.0125</td>
</tr>
<tr>
<td>Gain Error (%FSR)</td>
<td>5</td>
<td>1.825</td>
<td>4.55</td>
</tr>
<tr>
<td>Load Compliance (V)</td>
<td>4.5</td>
<td>4.698</td>
<td>4.724</td>
</tr>
</tbody>
</table>

Figure 1: Measured Transfer Function
2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The V-I transfer function of the circuit is based on the relationship between the input voltage, \(V_{\text{IN}}\), the reference voltage, \(V_{\text{REF}}\), the current sensing resistor, \(R_{\text{SET}}\), and the properties of the \(I_{\text{MON}}\) current monitor in the op-amp.

The transfer function for this design is defined in Equation 1.

\[
I_{\text{LOAD}} = \frac{(V_{\text{IN}} - V_{\text{REF}})}{R_{\text{SET}}} \times 475
\]  

(1)

2.1 Circuit Design

The first amplifier controls the current flowing through the load by using the \(I_{\text{MON}}\) current as feedback to the inverting terminal as opposed to standard resistive feedback from the output. The transfer function is based on cancelling the input current, \(I_{\text{IN}}\), with the \(I_{\text{MON}}\) current to keep voltage on the inverting terminal equivalent to \(V_{\text{REF}}\). Since the \(I_{\text{MON}}\) current is directly related to the output current of the amplifier, \(I_{\text{LOAD}}\), the output current can be controlled by changing the input current to the circuit.

\(V_{\text{REF}}\) was selected to be +2.5 V to bias the circuit to mid-supply in order to get equal output swings in both the positive and negative directions. By applying \(V_{\text{REF}}\) to the non-inverting terminal of the OPA569, negative feedback will set the voltage at its inverting terminal to be +2.5 V as well. Applying an input voltage to the circuit other than +2.5 V will therefore cause an input current to flow into the summing node at the inverting input based on the value of \(R_{\text{SET}}\).

\[
I_{\text{IN}} = \frac{(V_{\text{IN}} - 2.5 \text{ V})}{R_{\text{SET}}}
\]  

(2)

The \(I_{\text{MON}}\) circuit creates a 1:475 bidirectional copy of the output current delivered to the load. Having this circuit internal to the OPA569 eliminates the need for a series current sensing resistor in the design and increases the overall efficiency of the circuit. The relationship between the \(I_{\text{MON}}\) circuit and load current is shown in the equation below.

\[
I_{\text{MON}} = \frac{I_{\text{LOAD}}}{475}
\]  

(3)

Kirchhoff’s current law states that the sum of currents that flow into a common node must be equivalent to the sum of the currents flowing out of the node. Therefore, \(I_{\text{IN}}\) and \(I_{\text{MON}}\) flow in different directions and must be equal and opposite.
\[ I_{IN} = -I_{MON} \]  

Replacing terms in the equation above yields the equation below.

\[ \frac{(V_{IN} - 2.5 \, V)}{R_{SET}} = \frac{I_{LOAD}}{475} \]  

Solving for \( I_{LOAD} \) yields the transfer function of the design.

\[ I_{LOAD} = \frac{(V_{IN} - V_{REF})}{R_{SET}} \times 475 \]  

\( R_{SET} \) can be solved for using the ideal full-scale current and the full-scale input voltage. Solving for \( I_{LOAD} \) yields the transfer function of the design.

\[ R_{SET} = \frac{(4.5 \, V - 2.5 \, V)}{2 \, A} \times 475 \]

\[ R_{SET} = 475 \, \Omega \]  

The OPA569 device also features a current limit function which limits the max output current, \( I_{LIMIT} \), from exceeding the maximum desired value. The \( I_{LIMIT} \) value for the amplifiers is controlled by appropriately setting the current limit resistors, \( R_{CL1} \) and \( R_{CL2} \). The current limit should not turn on during normal operation and should be set safely outside of the desired output current span. To limit the output current of the amplifiers to 2.1 A, follow the equation provided in the OPA569 datasheet.

\[ I_{LIMIT} = 2.1 \, A = 9800 \times \left( \frac{1.18 \, V}{R_{CL}} \right) \]  

\[ R_{CL1} = R_{CL2} = 5.49 \, k\Omega \]  

3 Component Selection

3.1 Operational Amplifier

To enable the V-I transfer function described in this design, the power amplifier needs to include an internal output current monitor, eliminating most power amplifier options. The OPA569 power amplifier is a high-current device that is capable of driving a wide variety of loads with an output current over 2 A. It is optimized for low-voltage, single or dual-supply operation with rail-to-rail swing on both the input and output. The OPA569 is unity-gain stable, has low dc errors, and does not have any of the phase inversion problems commonly found in other power amplifiers. The OPA569 was chosen for this design because it includes the \( I_{MON} \) circuit with +/-3% accuracy which meets or exceeds the performance requirements for this design.

3.2 Voltage Reference Selection

A +2.5 V reference voltage was applied to this circuit to accommodate for a bi-directional output with a single-supply. Along with the need for reference voltage accuracy, key considerations were made to ensure that the solution would also provide a low level of noise and temperature drift. The REF5025 was chosen for this design to exceed these key specifications.
3.3 Output Protection Diode Selection

Reactive and other electromotive force (EMF) generating loads can cause the output voltage to exceed the supply voltage, VCC, and potentially damage the circuit. This scenario can be avoided by clamping the output terminal voltage to the power supplies through the use of Schottky rectifier diodes. To protect the OPA569 from damage, a 3 A or greater continuous rating is needed. The 30BQ015 Schottky rectifier diode was chosen for this design to meet this specification and protect the circuit from damage.

3.4 Output Snubber Network \((R_{SN}, C_{SN})\)

Designs that directly drive reactive loads will also benefit from an R-C snubber network placed directly on the output of the amplifiers. The values used in the design are standard values and may need to be modified based on the load.

3.5 Loop Compensation Components \((R_C, C_C)\)

Compensation components \(R_C\) and \(C_C\) provide a high frequency path for currents to flow to the reference voltage at the non-inverting input. These components help dampen the response and should be included in the design. The values were obtained experimentally during simulation and then modified based on lab testing.

3.6 Passive Component Selection

The critical passive component for this design is the resistor that is part of the transfer function, \(R_{SET}\). To meet the gain error design goal of 5% FSR, the tolerance of this resistor was chosen to be 1%.

Other passive components in this design may be selected for 1% or greater as they will not directly affect the transfer function of this design.

4 Simulation

The TINA-TI™ schematic shown in Figure 3 includes the circuit values obtained in the design process.

![Figure 3: TINA-TI™ Simulation Schematic](image)
4.1 DC Transfer Function

The dc transfer function simulation results of the circuit in Figure 3 are shown in Table 2 and Figure 4. The results can be used to reference the voltage or current at a given node as a function of the input voltage.

Table 2: Simulated DC Transfer Function Performance

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Simulated Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negative Full-Scale Current (A)</td>
<td>-1.981</td>
</tr>
<tr>
<td>Positive Full-Scale Current (A)</td>
<td>1.949</td>
</tr>
<tr>
<td>Zero-Scale Current mA</td>
<td>-1.333</td>
</tr>
</tbody>
</table>

Figure 4: TINA-TI™ – DC Transfer Characteristic

The simulation results in Figure 4 were obtained using ideal passive components which reduces errors in the circuit to only the performance of the op-amps. More realistic simulation results can be obtained by running a Monte-Carlo simulation which will take into account the tolerance of the passive components.

Figure 5 displays the results of a ten iteration Monte-Carlo dc sweep performed after entering the actual passive component tolerances. The averaged statistical results of the Monte-Carlo simulation are summarized in Table 3.
Figure 5: TINA-TI™ - Monte-Carlo Simulation of I_{LOAD}

Table 3: Average Monte-Carlo DC Transfer Results

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero-Scale Current (mA)</td>
<td>-1.333</td>
</tr>
<tr>
<td>Positive Full-Scale Current (A)</td>
<td>1.948</td>
</tr>
<tr>
<td>Negative Full-Scale Current (A)</td>
<td>-1.979</td>
</tr>
<tr>
<td>Full-Scale Current (A)</td>
<td>3.927</td>
</tr>
<tr>
<td>Full-Scale Current Standard Deviation (σ) (mA)</td>
<td>6.11</td>
</tr>
</tbody>
</table>

The total system gain error from the ideal component sweep was determined using the following equation:

\[
\text{Gain Error(%) = } \left| \frac{I_{\text{LOAD}}(\text{Ideal } \max) - I_{\text{LOAD}}(\text{Ideal } \min) - (I_{\text{LOAD}}(\max) - I_{\text{LOAD}}(\min))}{I_{\text{LOAD}}(\text{Ideal } \max) - I_{\text{LOAD}}(\text{Ideal } \min)} \right| \times 100
\]  

The positive and negative gain errors were calculated using similar equations using the ideal positive and negative spans (2A).

The standard deviation of the Monte Carlo sweep was very low revealing that the tolerance of the R_{SET} resistor was not too critical and most of the final system error will be due to the +/-3% typical accuracy of the I_{MON} circuit.
4.2 Step Response

The step response of the design is shown in Figure 6. The results show that the output settles to the proper value with little overshoot and ringing, indicating a stable design. The stable response was obtained by manipulating the compensation components, $R_C$ and $C_C$.

![Figure 6: TINA-TI™ – Small-Signal Step Response](image)

4.3 Compliance Voltage

To test the maximum compliance voltage and load resistance, the output was set to positive full-scale maximum current, and the load resistor, $R_{LOAD}$, was swept from 0 Ω - 5 Ω. The results are shown in Figure 7. The output compliance voltage was found to be 4.698 V and the maximum output resistance was 2.36 Ω.
Figure 7: TINA-TI™ Maximum Load Resistance and Compliance Voltage

4.4 Simulated Result Summary

The simulation results are compared against the design goals in Table 4.

<table>
<thead>
<tr>
<th></th>
<th>Goals</th>
<th>Simulated</th>
<th>Simulated Monte-Carlo</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset (%FSR)</td>
<td>0.1</td>
<td>0.033</td>
<td>0.033</td>
</tr>
<tr>
<td>Positive Gain Error (%FSR)</td>
<td>N/A</td>
<td>2.55</td>
<td>2.6</td>
</tr>
<tr>
<td>Negative Gain Error (%FSR)</td>
<td>N/A</td>
<td>0.95</td>
<td>1.05</td>
</tr>
<tr>
<td>Total Gain Error (%FSR)</td>
<td>5</td>
<td>1.75</td>
<td>1.825</td>
</tr>
<tr>
<td>Load Compliance (V)</td>
<td>4.5</td>
<td>4.698</td>
<td>4.698</td>
</tr>
</tbody>
</table>
5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1 and A.2.

5.1 PCB Layout

Trace thickness is a primary concern in this design due high current. Any traces in the design that carry a high current should have thickness that ensures a proper degree of current-carrying capacity. In this design, at least 100 mil traces were used for the high current paths.

The PCB layout for this design is shown in Figure 8.

![Altium PCB Layout](image)

Figure 8: Altium PCB Layout

In addition to these rules, please reference and abide by general PCB layout guidelines.
6 Verification and Measured Performance

6.1 Transfer Function

Data was collected by sweeping $V_{\text{IN}}$ from 0.5 V – 4.5 V dc while measuring the voltage across the load, $V_{\text{LOAD}}$, and load current, $I_{\text{LOAD}}$. Figure 9 displays a plot of $I_{\text{LOAD}}$ vs $V_{\text{IN}}$.

![Figure 9: Measured $I_{\text{LOAD}}$ vs. $V_{\text{IN}}$](image)

Table 5: Measured Performance

<table>
<thead>
<tr>
<th></th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negative Full-Scale Current (A)</td>
<td>-2.096</td>
</tr>
<tr>
<td>Positive Full-Scale Current (A)</td>
<td>2.086</td>
</tr>
<tr>
<td>Zero-Scale Current (mA)</td>
<td>-0.5</td>
</tr>
</tbody>
</table>

To observe the errors in the circuit more easily, the error current of the load, $I_{\text{LOAD\_ERROR}}$, was calculated by taking the difference between, $I_{\text{LOAD\_Ideal}}$, and $I_{\text{LOAD}}$. The results are shown in Figure 10.
The positive, negative, and system gain errors were calculated using the equations in Section 0 and are displayed in Table 6.

**Table 6: Measured Performance %FSR**

<table>
<thead>
<tr>
<th></th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Error (%FSR)</td>
<td>0.0125</td>
</tr>
<tr>
<td>Positive Gain Error (%FSR)</td>
<td>4.8</td>
</tr>
<tr>
<td>Negative Gain Error (%FSR)</td>
<td>4.3</td>
</tr>
<tr>
<td>Total Gain Error (%FSR)</td>
<td>4.55</td>
</tr>
</tbody>
</table>

The measured output voltages of each amplifier versus $V_{IN}$ while driving a 1 Ω load are shown in Figure 11.
6.2 Transient Response

A full-scale 4 Vpp, 100 Hz triangle wave centered around 1 V dc is applied to $V_{IN}$ to observe how the design reacts when a full-scale ramp is applied to the input. Figure 12 shows an oscilloscope screen capture of the input voltage, Channel 1, and the output current through the load resistor, Channel 2.
A full-scale 4 Vpp, 100 Hz full-scale step response centered at 1 V dc is applied to VIN to observe the full-scale settling response of the design. Figure 13 shows an oscilloscope screen capture of the input voltage, Channel 1, and the output current through the load resistor, Channel 2.

Figure 13: Full-Scale Settling Response

A 260 mVpp, 1 kHz small-signal input step centered around 1 V dc was applied to VIN to test the small-signal stability of the design. Figure 14, Figure 15, and Figure 16 show the resulting oscilloscope screen captures of the input voltage, Channel 1, the output voltage at the negative terminal of the load, V_{LOAD-}, Channel 2, the output voltage at the positive terminal of the load, V_{LOAD+}, Channel 3, and the output current through the load resistor, Channel 4.

Figure 14 shows the resulting system response while sinking current when VIN is set to 1.5 V. Figure 15 shows the resulting system response at mid-range when VIN is set to 2.5 V. Figure 16 shows the resulting system response while sourcing current when VIN is set to 3.5 V. In all three circumstances, the design quickly settles to the final value with a properly damped response without overshoot or ringing. A slight glitch can be observed as the I_{LOAD} current passes through the transition region between when the I_{MON} circuit is sinking and sourcing current.
Figure 14: Small-Signal Stability as a Current Sink

Figure 15: Small-Signal Stability at Mid-Range
6.3 Compliance Voltage

The compliance voltage of the circuit, $V_{COMP}$, is based on the supply voltage, $V_{CC}$, and the output swing-to-rail characteristics of the amplifier specified in the amplifier product datasheet. Figure 17 displays the output swing to both the positive and negative rails for the OPA569.

As shown in Figure 17, with ±2 A output current, the positive swing is approximately 150 mV from the positive rail and the negative swing is 200 mV from the negative rail. A quick estimate of the load compliance voltage can be made by subtracting the 350 mV of output swing limitation from the 5 V power supply, leaving 4.65 V of output load compliance. The measured value was found to be 4.724 V.
Based on the measured maximum load compliance voltage the maximum load resistance, \( R_{\text{LOAD}}(\text{max}) \), can be calculated as shown in the following equations.

\[
R_{\text{LOAD}}(\text{max}) = \frac{V_{\text{COMP}}}{I_{\text{LOAD}}} \tag{12}
\]

\[
R_{\text{LOAD}}(\text{max}) = 2.362 \Omega \tag{13}
\]

6.4 **Measured Result Summary**

The measured results are compared against the design goals in Table 7.

**Table 7: Comparison of Design Goals and Measured Performance**

<table>
<thead>
<tr>
<th>Goals</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset (%FSR)</td>
<td>0.0125</td>
</tr>
<tr>
<td>Positive Gain Error (+%FSR)</td>
<td>4.8</td>
</tr>
<tr>
<td>Negative Gain Error (-%FSR)</td>
<td>4.3</td>
</tr>
<tr>
<td>Total Gain Error (%FSR)</td>
<td>4.55</td>
</tr>
<tr>
<td>Load Compliance (V)</td>
<td>4.724</td>
</tr>
</tbody>
</table>

7 **Modifications**

The components selected for this design were based on the design goals outlined at the beginning of the design process. The circuit requires a power amplifier that has an internal current-monitoring circuit that can be used as feedback to create the V-I transfer function. The use of alternative amplifiers is not feasible in this exact configuration because of the lack of the I\_MON circuit. However, almost all power amplifiers can be used in a BTL configuration with voltage feedback to the first amplifier. This would produce a standard voltage output system instead of a current output, but would still benefit from all of the performance benefits of a BTL design.

The \( R_{\text{SET}} \) and the \( R_{\text{CL}} \) resistors can be adjusted to lower the output current and output current limits depending on the design requirements. However, increasing the output current swing past the ±2 A shown in this design is not possible without the risk of damage to the circuit.

To reduce cost in the reference circuit at the expense of accuracy, a low-cost shunt regulator can be used in place of the REF5025 to provide the +2.5 V reference.

8 **Potential Application: TEC Driver**

Additional data was collected by using a CP30338 Thermo-Electric Cooler, TEC, as the load of the circuit to observe the operating temperature characteristics of the TEC when used in conjunction with this circuit. A TEC creates a heat differential between its two plates based on the Peltier effect, which occurs when a current flows through the TEC. A stick-on resistive-temperature-detector (RTD) temperature probe was used to measure both sides of the TEC.

Data was collected by sweeping \( V_{\text{IN}} \) from 1.8 V – 2.5 V dc while measuring the temperature of the hot and cold sides of the TEC. Figure 18 displays a plot of the hot-side temperature of the TEC versus \( V_{\text{IN}} \), while Figure 19 displays a plot of cold-side temperature versus \( V_{\text{IN}} \).
Figure 18: Hot-Side Temperature vs. $V_{IN}$

Figure 19: Cold-Side Temperature vs. $V_{IN}$
9 About the Authors

David F. Chan graduated from the Rochester Institute of Technology in May of 2012, where he earned a Bachelor of Science in Electrical Engineering Technology and a minor in both Management and Psychology. He joined Texas Instruments through the Applications Rotation Program in August 2012, where he worked with the Precision Analog - Linear and the Analog Centralized Applications teams.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

10 Acknowledgements & References

A special thanks to Neil Albaugh who originally created the base for this circuit as part of the TINA-TI™ example circuit library.
Appendix A.

A.1 Electrical Schematic

The electrical schematic is shown in Figure 20.

Figure 20: Altium Schematic
### A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 21.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Supplier Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0.1μF</td>
<td>C1, C3, C5, C7, C9</td>
<td>GAP, CERM, 0.1μF, SMD, ±10%, X7R, 1206</td>
<td>AVX</td>
<td>1206CQ101JAT2A</td>
<td>479-3751-ND</td>
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<tr>
<td>4</td>
<td>47μF</td>
<td>C2, C4, C6, C13</td>
<td>GAP, TANT, 47μF, 16V, ±20%, 0.7 ohm, 7418±31 SMD</td>
<td>Vishay-Sprague</td>
<td>293D0470K00502T1E3</td>
<td>719-1096-1-ND</td>
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<td>2</td>
<td>2μF</td>
<td>C9, C10</td>
<td>GAP, CERM, 2μF, 25V, ±10%, X7R, 0503</td>
<td>MURATA</td>
<td>GRM180BB71M051KD</td>
<td>499-5107-1-ND</td>
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<td>1</td>
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<td>Cc</td>
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<td>CR216K7M2A47K</td>
<td>445-2284-1-ND</td>
</tr>
<tr>
<td>2</td>
<td>0.1μF</td>
<td>C1, C2</td>
<td>GAP, CERM, 0.1μF, SMD, ±10%, X7R, 0402</td>
<td>Kemet</td>
<td>C0603X102K6R392</td>
<td>399-1095-1-ND</td>
</tr>
<tr>
<td>1</td>
<td>0.1μF</td>
<td>C3, C4, C5, C7, C9</td>
<td>GAP, CERM, 0.1μF, SMD, ±10%, X7R, 0402</td>
<td>Kemet</td>
<td>C0603X102K6R392</td>
<td>399-1095-1-ND</td>
</tr>
<tr>
<td>1</td>
<td>6.3V</td>
<td>D1, D2, D3, D4</td>
<td>Diode, Schottky, 150V, 5A, SMD</td>
<td>International Rectifier</td>
<td>IRFQ015STRPBF</td>
<td>VS-8280105604CT-ND</td>
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<td>4</td>
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<td>BUMPMON EJ07M0101, 310V, 200μH, 22 V</td>
<td>NEX</td>
<td>NMCY6012</td>
<td>0.0570-5-ND</td>
<td></td>
</tr>
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<td>2</td>
<td>GRND, GND</td>
<td>Standard Banana Jack, Uninsulated, 5.5mm</td>
<td>Keystone</td>
<td>575-4</td>
<td>575-4C-ND</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Load</td>
<td>ConnTerm Block, 2PO, 5.08mm PCB</td>
<td>Phoenix Contact</td>
<td>1713721</td>
<td>277-1265-ND</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>20Ω</td>
<td>R1</td>
<td>RES, 20Ω, ohm, 0.1%, 0.1W, 0402</td>
<td>Susumu Co Ltd</td>
<td>RG1600P-100-8-8.5</td>
<td>RG1600P-100-9-BCT-ND</td>
</tr>
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<td>1</td>
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<td>RES, 249 ohm, 1%, 0.1W, 0603</td>
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<td>RO603F1-0.2490R</td>
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<td>2</td>
<td>5.4kΩ</td>
<td>R01, R02</td>
<td>RES, 5.4k ohm, 1%, 0.1W, 0603</td>
<td>Yageo America</td>
<td>RO603F1-0.2500R</td>
<td>311-5.4KHMCT-ND</td>
</tr>
<tr>
<td>1</td>
<td>1kΩ</td>
<td>R5, R4</td>
<td>RES, 1kΩ, ohm, 1%, 0.1W, 0603</td>
<td>Yageo America</td>
<td>RO603F1-0.1000R</td>
<td>311-1.0KHMCT-ND</td>
</tr>
<tr>
<td>2</td>
<td>475Ω</td>
<td>R3</td>
<td>RES, 475 ohm, 1%, 0.1W, 0603</td>
<td>Yageo America</td>
<td>RO603F1-0.4700R</td>
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<tr>
<td>2</td>
<td>18.2kΩ</td>
<td>R03, R04</td>
<td>RES, 18.2k ohm, 1%, 0.1W, 0603</td>
<td>Yageo America</td>
<td>RO603F1-0.1850R</td>
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<tr>
<td>3</td>
<td>Red</td>
<td>TP1, TP9, TP13</td>
<td>Test Point, TH Miniature, Red</td>
<td>Keystone</td>
<td>5001</td>
<td>S098K-ND</td>
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<tr>
<td>6</td>
<td>Black</td>
<td>TP2, TP4, TP5, TP6, TP7</td>
<td>Test Point, TH Miniature, Black</td>
<td>Keystone</td>
<td>5001</td>
<td>S098K-ND</td>
</tr>
<tr>
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<td>TP10, TP11</td>
<td>Test Point, TH Miniature, White</td>
<td>Keystone</td>
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<td>Texas Instruments</td>
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<td>E Leahwa Network Power</td>
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**Figure 21: Bill of Materials**
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