TLK1xx Software GUI

The purpose of this document is to provide a thorough overview of the TLK1xx software GUI. The document presents the different GUI functionalities that activate the different special features and capabilities of the chip. In this document, illustrations and software executables referring to TLK100 also apply to any TLK1xx device.

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1 General

1.1 Overview

The TLK1xx is an Ethernet Phy chip that consists of one core: Fast Ethernet-phy (FE) core (10/100BT). The chip's main interfaces are:

- One10/100BT port
- Digital test-ports
- MII and RMII
- Clock ports
- Power supply pins

2 Installation Guide

2.1 Operating System

The recommended operating system for the software is Windows® 7 and Windows XP.

2.2 SmartBits 200 and SmartBits 2000

The test partner for the TLK1xx EVM is the SmartBits 200 or SmartBits 2000.

The computer where the GUI software is installed should be connected via Ethernet to the smart bit. The EVM and the TLK1xx is controlled through the smart bit.

Figure 1 illustrates this setup:

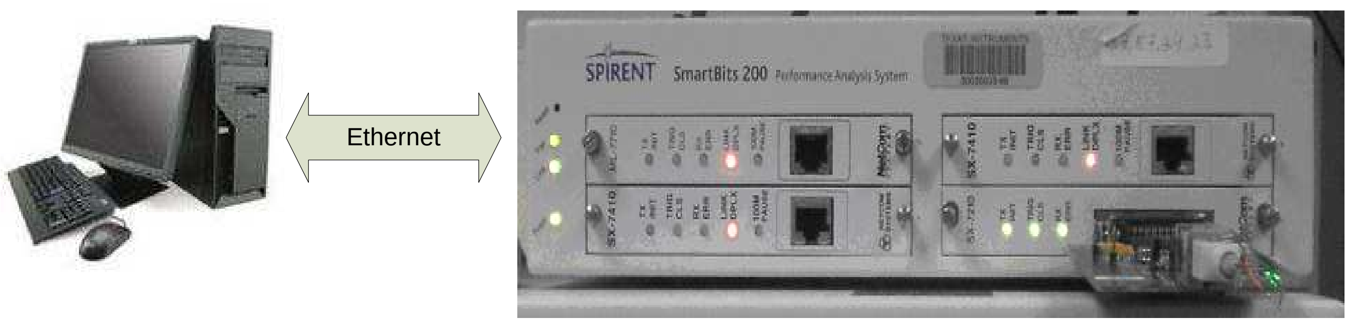

Figure 1. TLK1xx Setup

After it is verified that the Spirent SMB-200/2000 (SmartBits) is connected to the PC, verify that the SX-7210 MII Card is installed in the SMB Chassis.

Figure 2 and Figure 3 show the 2 different SmartBits devices in use:

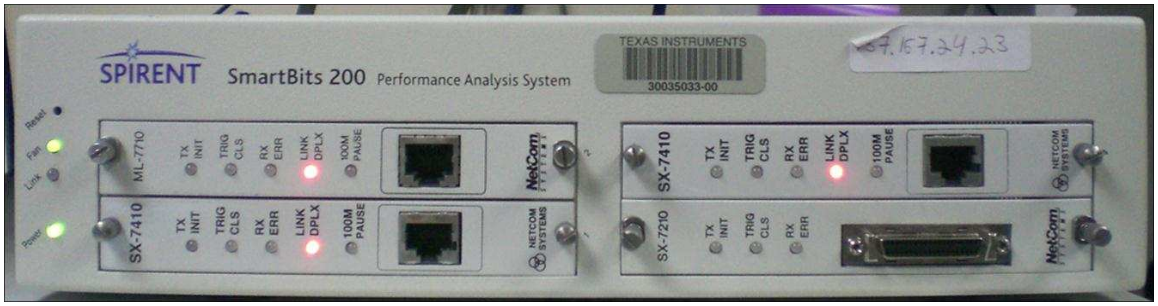

Figure 2. SMB 200

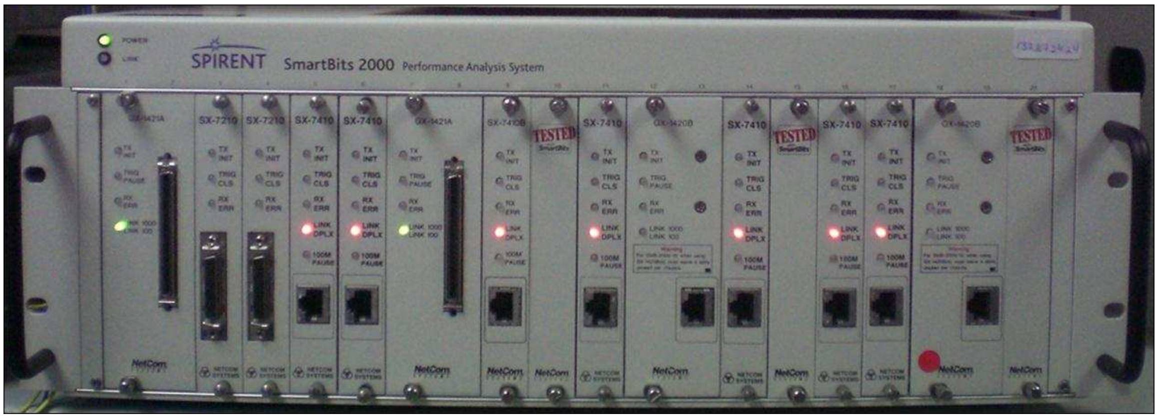

Figure 3. SMB 2000

Figure 4 shows the MII card connected to the SMB 2000:

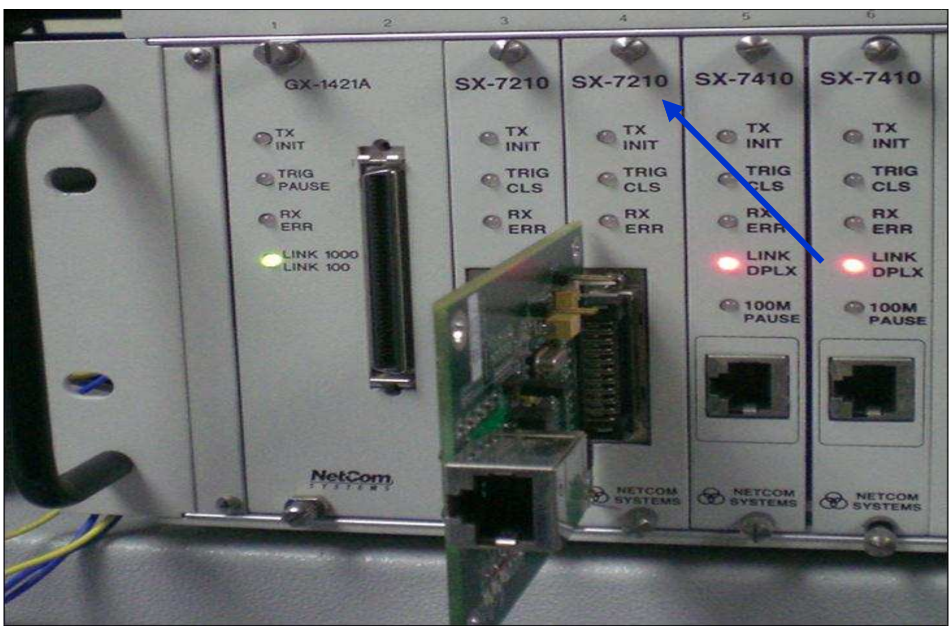

Figure 4. MII Card Connected to the SmartBits 2000

The next step is to verify that the SmartBits application *SmartLibrary* is installed on the computer. The GUI uses the *SmartLibrary* libraries to control the SmartBits.

After installing the *SmartLibrary*, check that no application is currently communicating with SmartBits. This can be seen while verifying that the link indication on the SMB chassis is off, as shown in Figure 5.

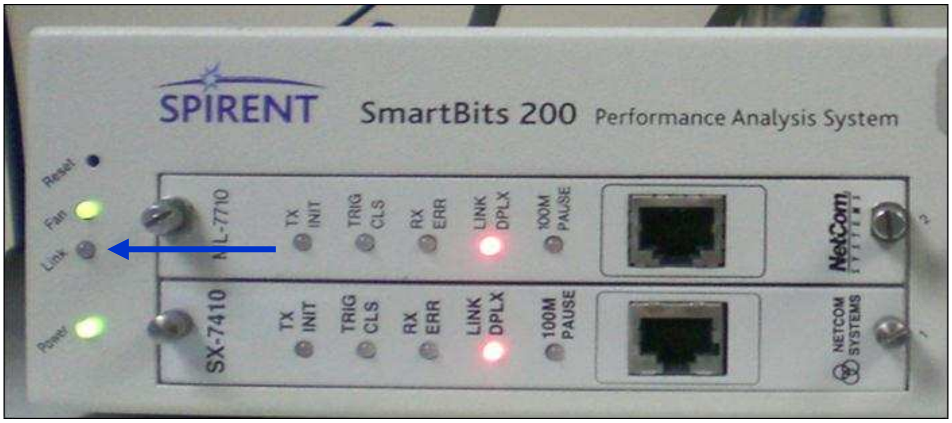

Figure 5. SmartBits Link Indication

2.3 Software Installation

Install the software with the following steps:

1. Unzip the package file.
2. Run the setup program.
3. When the screen shown in Figure 6 appears, choose *TLK110_Customer_SW*.

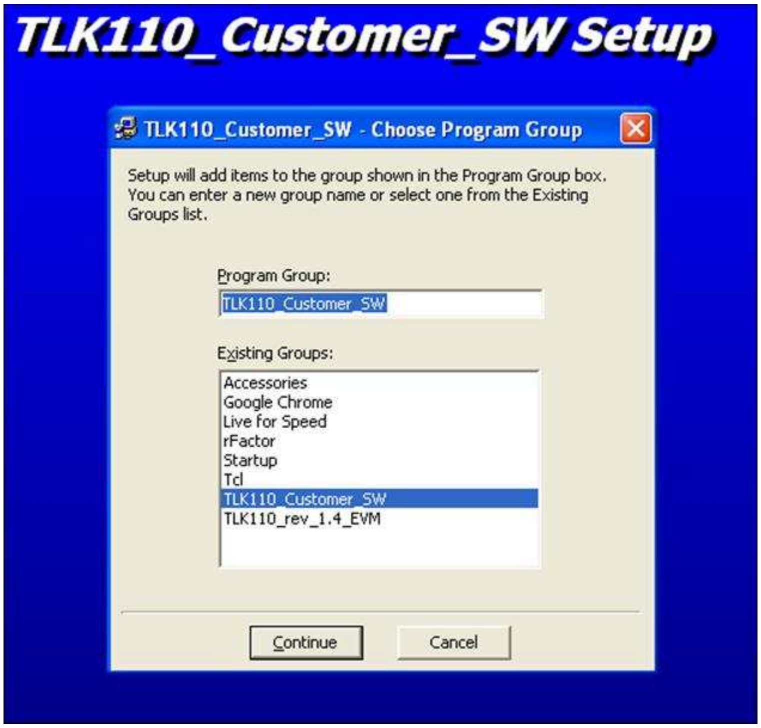

Figure 6. Setup Installation

After the installation is complete, double click the *TLK110_SW.exe* file added to your folder as illustrated in Figure 7.

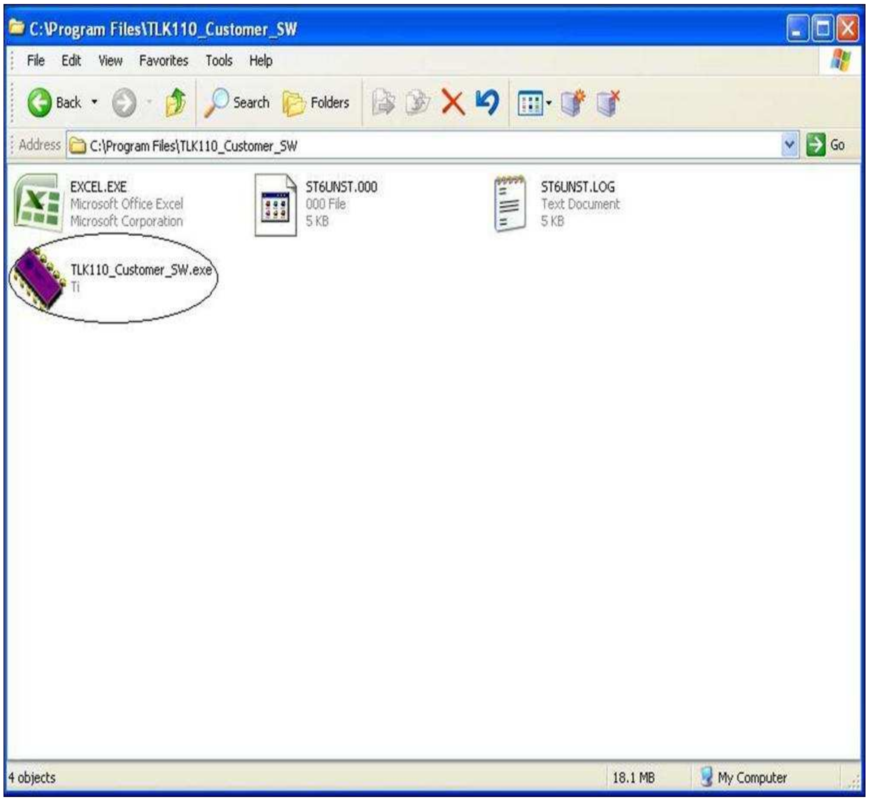

Figure 7. Application Folder

2.4 Initialization Window

The initialization window appears when the program is started. When it appears, enter the IP address and slot as shown in Figure 8.

Figure 8. Initialization

3 Software Functionality and Front Panel

The GUI is based on a row of tabbed windows. Each of the available tabbed windows can be selected (clicked) to display a window associated with each functional aspect of the device.

3.1 PHY Control

The following fields describe the GUI tabs and functionality:

1. **Summary Tab:** Brief operational overview and status of the device.
2. **Settings Tab:** Quick and fast control buttons of the chip different modes of work.
3. **Registers Tab:** Ability to read and write the contents of the registers.
4. **Scripting Tab:** Provides scripting ability via loading a text file.
5. **LPBK/PRBS:** Enables loopback (LPBK) settings, Pseudo-Random Binary Sequence (PRBS) engine, and control of the different power modes.
6. **CD Tab:** Cable diagnostics, ALCD and PRBS (not operational in rev_1.0).
7. **Pinout Tab:** Functional description of each pin of the device.

3.1.1 Summary Tab

Provides a brief operational overview of the selected device's operational status.

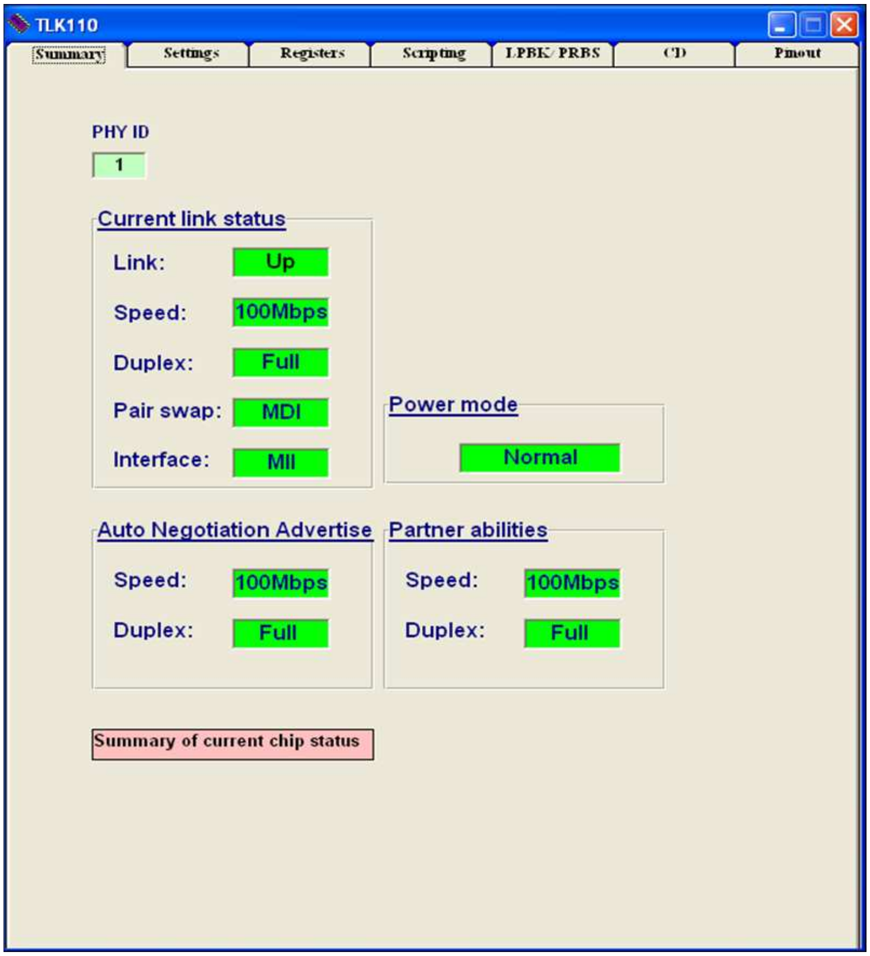

Figure 9. Summary Window

The summary window is refreshed every second keeping the window constantly updated.

The fields in this tab are:

- **PHY ID:**
  Address read from the phy address range 31:0
- **Current link status:**
  Link: Up or Down
  Speed: 100Mbps or 10Mbps
  Duplex: Full or Half
  Pair swap: MDI or MDI-X
  Interface: MII or RMII
- **Auto Negotiation Advertise:**
  Speed: 100Mbps or 10Mbps
  Duplex: Full or Half
- **Power mode:**
  Normal, active, or passive
- **Partner abilities:**
  Speed: 100Mbps or 10Mbps
  Duplex: Full or Half

3.1.2 Settings Tab

The device's main settings and operation modes are modified in the *Settings* tab via the option buttons.

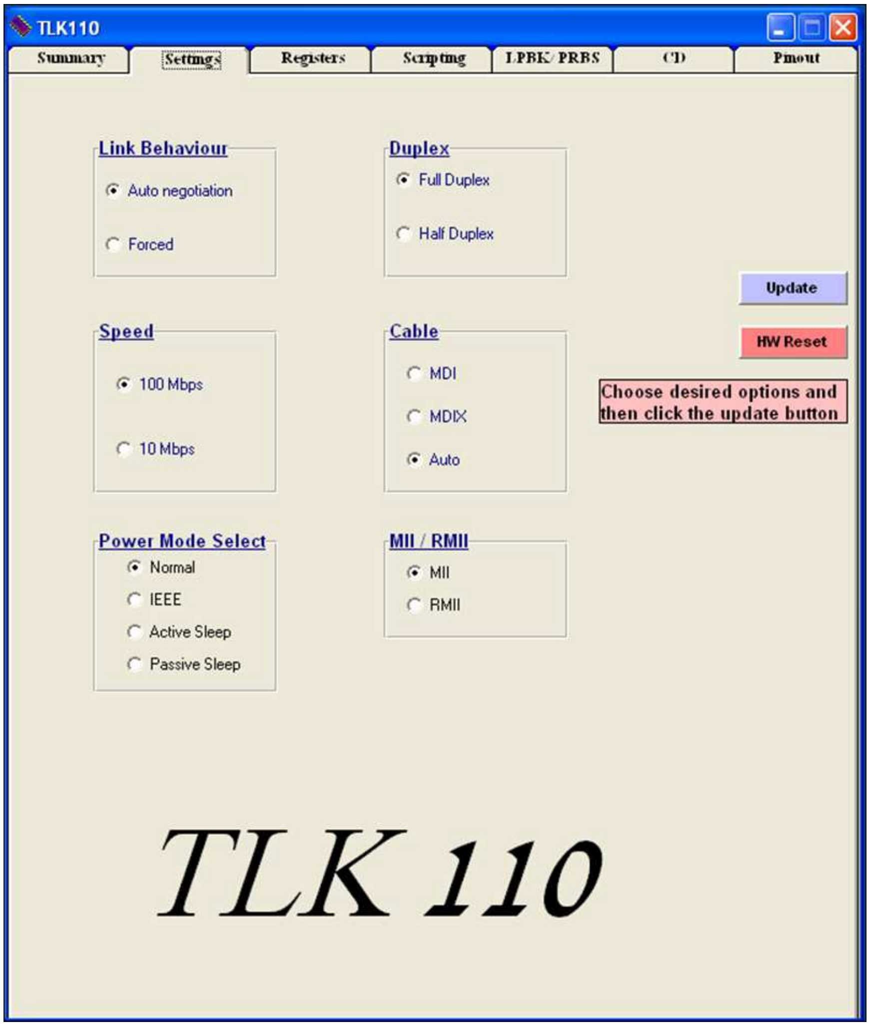

Figure 10. Settings

The settings window is updated every time it is accessed.

The fields in this tab are:

- **Link behavior**
  Auto Negotiation or Forced
- **Speed**
  10 or 100 Mbps
- **Power Mode Select**
  Choose between Normal and Power save modes of operation
- **Duplex**
  Full or Half duplex
- **Cable**
  Force Straight (MDI)
  Force Crossover (MDIX)
  Automatic
- **MII / RMII**
  MII or RMII MAC interface
  (XI clock 50 MHz for RMII)
- **Update button**
  Updates the setting
- **HW Reset**
  Writes to register

Fields Explanation:

- **Link behavior** is set via register 0x0 BMCR bits 12, 9
- **Speed** and **Duplex** selection for Auto Negotiation is set via register 0x4 ANAR, for Forced mode, **Speed** is set via 0x0 BMCR bit 13 and **Duplex** via bit 8.
- **Cable Crossover** is set via register 0x19 PHYCR bits 15, 14.
- **MII / RMII** is set via reg 0x17 RCSR bit 5
- **Power mode select**
  - Normal: normal operation
  - IEEE mode: power down all digital and analog blocks initiates a write to BMCR register address 0x0 bit '11' = '1'
  - Active sleep: same as passive sleep, but also send NLP every ~1.4 s to wake Up link-partner Initiates a write to PHY Control Register address 0x0011 bits '14:12' = '110'
  - Passive sleep: power down all digital and analog blocks, automatic power-up is done when link partner is detected Initiates a write to PHY Control Register Address 0x0011 bits '14:12' = '111'
- **Update** button writes the setting to the registers
- **HW Reset** button writes register 0x0 BMCR bit 15 'reset' and 0x1f PDR bit 15 'Software global reset'

3.1.3 Registers Tab

Datasheet register descriptions paired with the ability to read and write the contents of the registers for evaluation and experimentation.

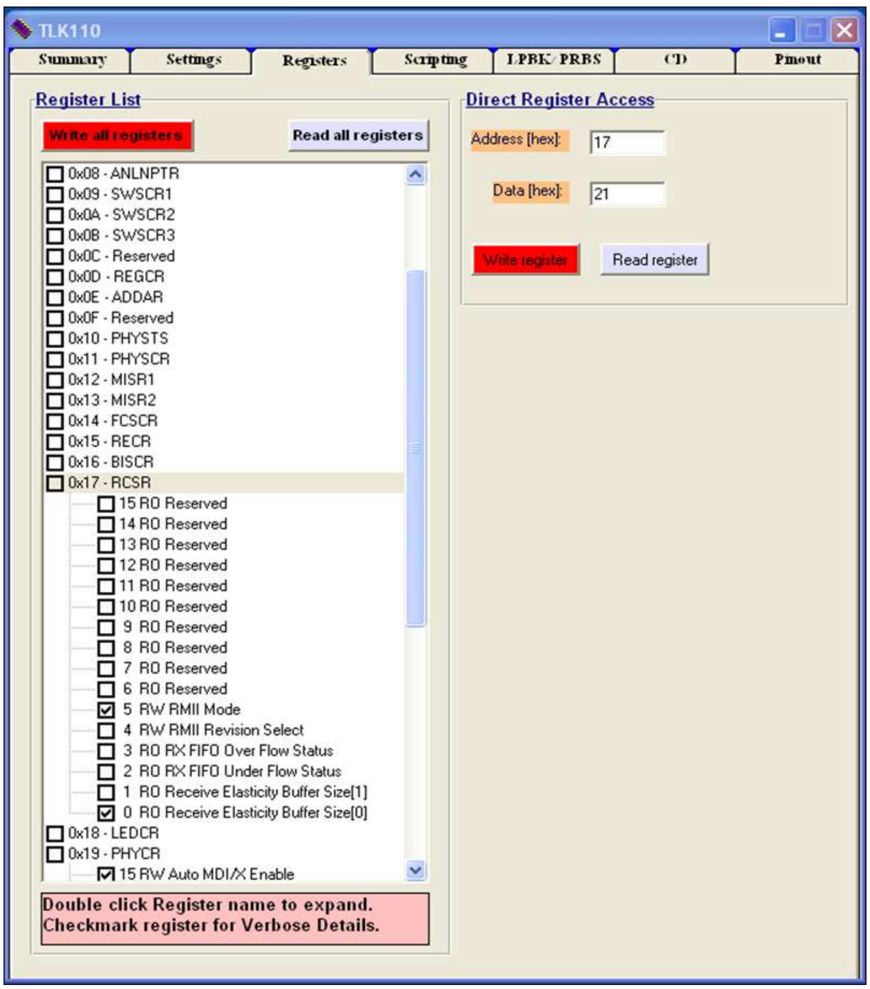

Figure 11. Registers

The registers window is updated every time it is accessed.

The fields in this tab are:

- **Register List**
  Registers address 0x0 up to address 0x0F: IEEE802.3 specific registers
  Registers address 0x10 up to address 0x1F TI's specific registers
- **Direct Register Access**
  Enables read or write to any register.

Fields Explanation:

Register List: Drop-down list of the registers

- Double click register name to expand
- **Write all registers** button: updates all registers with new writings
- **Read all registers** button: reads all registers and updates list

Write all and read all buttons take up to 2 s to complete because they refresh all the registers in the list.

Direct register access:

- Write register: specify register address and data in the appropriate fields.
  After writing the value the software will read the same register And will also update the entire Register list.
- Read register: specify register address.

Figure 12. Direct Registers Access

3.1.4 Scripting Tab

Provides the user with a scripting ability via a text file.

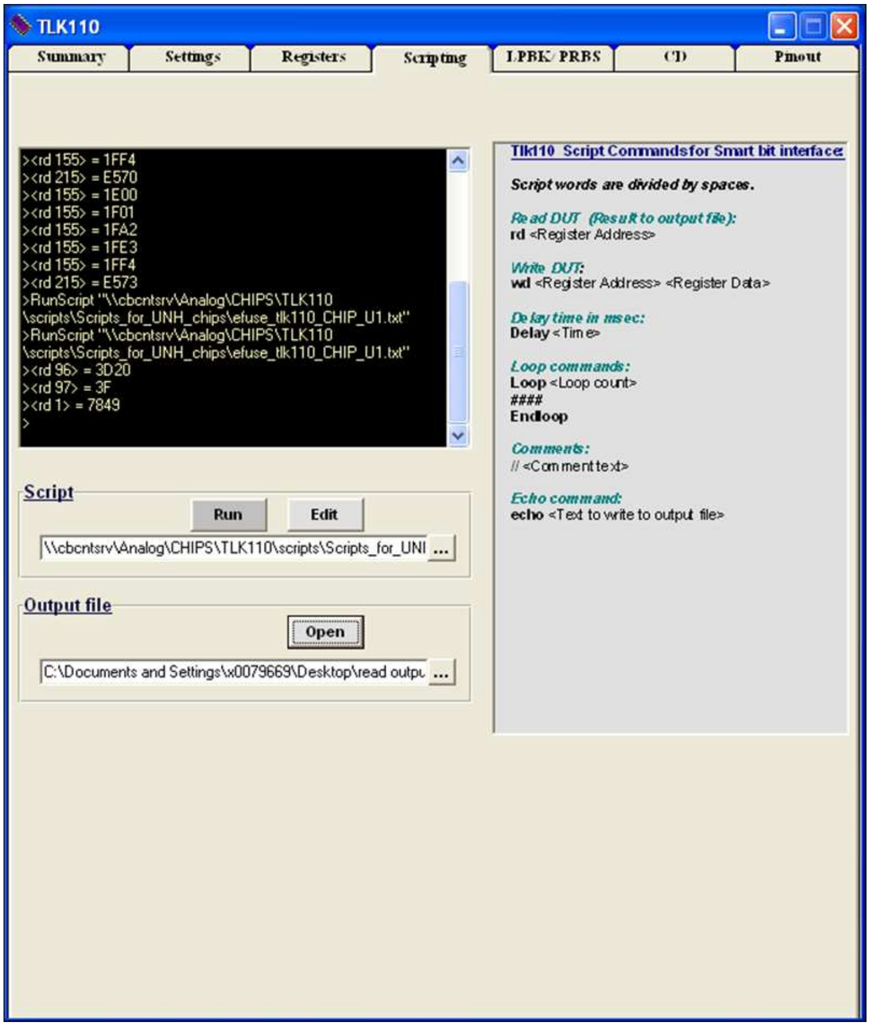

Figure 13. Scripting

The fields in this tab are:

- **Shell Window**
  1. Allows the user to input commands directly to shell window
  2. Outputs the value of registers when a read transaction is executed (script and shell).

  Syntax for script files and shell commands

Figure 14. Command Syntax

- Script

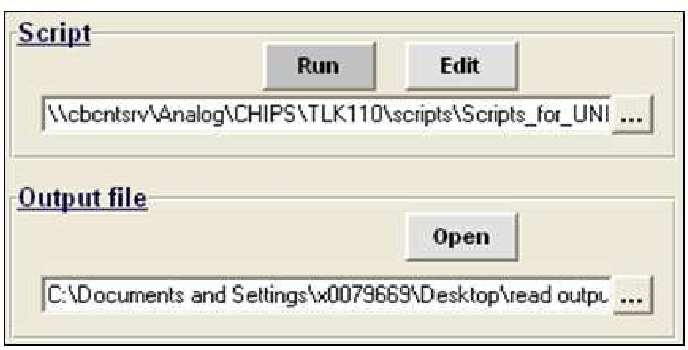

Figure 15. Script Location

  - Enter the path for script file
  - Scripts file should be of .txt format
  - Enter output file, the output file holds the value of read transactions done from script


```
// script example
/////////////////////////////////////////////////////////

wd 00 8000 // reset device
wd 10 4040 // auto mdi/-x
wd 04 0061 //advertise 10bt half duplex + full duplex abilities
wd 00 1200 // auto negotiation enable, restart auto neg

echo read from reg 4 dut

loop 2 //loop twice
Rd 4    // read register 4
endloop

wd 04 0021 //advertise 10bt half duplex abilities

echo read from reg 4
loop 2
rd 4
endloop

/////////////////////////////////////////////////////////
```

Figure 16. Script Example

The software will translate commands from shell or script to register transactions. Commands should adhere to syntax or there will be an error.

3.1.5 LPBK/PRBS Tab (Loopback/Pseudo-Random Binary Sequence)

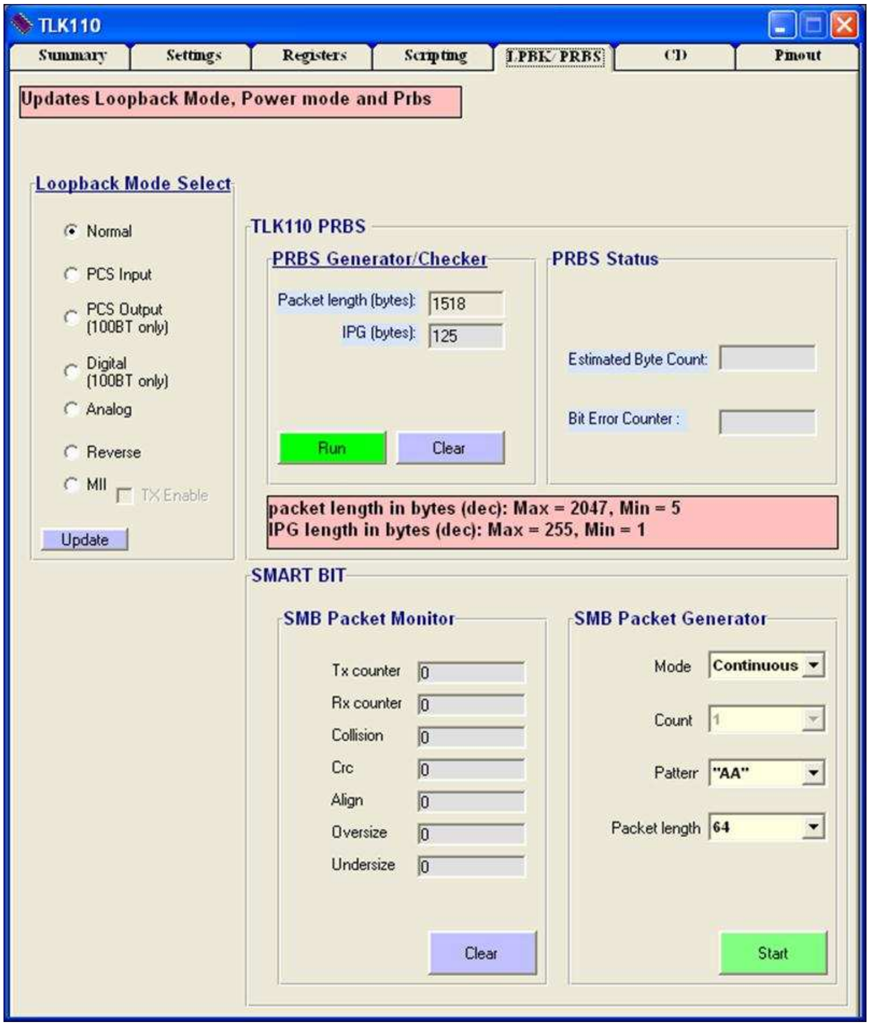

Figure 17. Loopback, Power, PRBS

The LPBK/PRBS window holds some of the more advanced functionalities of the chip. It is updated every time it is selected.

The fields in this tab are:

- Loopback mode select
- PRBS Status
- PRBS Generator/Checker
- Smart Bit Packet Monitor and Smart Bit Packet Generator

Fields Explanation:

- Loopback mode select

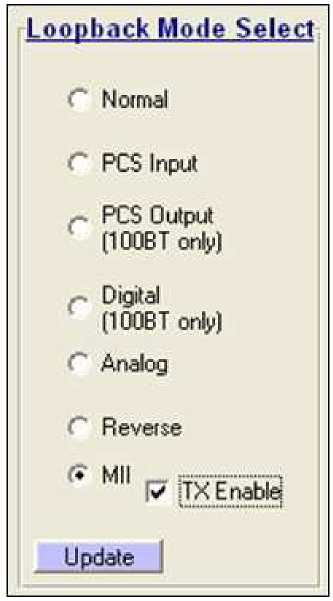

Figure 18. Loopback Mode

The TLK1xx provides several options for Loopback that test and verify various functional blocks within the Phy.

Generally, the TLK1xx may be configured to one of the Near-end Loopback modes or to the Far-end (Reverse) loopbacks.

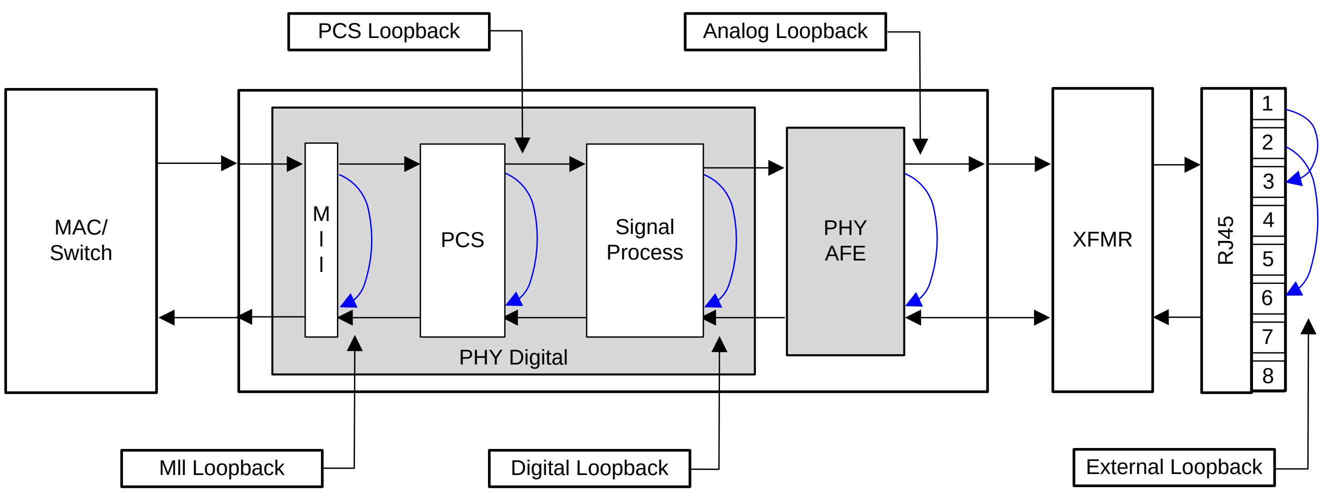

Figure 19. Loopback Scheme

- Normal: no loopback is selected
- MII – the device can establish a link with itself at 10/100BT speed using the Force link (refer to settings window)
- PCS– the device can establish a link with itself at 100BT speed using the Force link (refer to settings window)
- Digital– the device can establish a link with itself at 100BT speed using the Force link (refer to settings window)
- Analog– the device can establish a link with itself at 10/100BT speed using the Force link (refer to settings window)

- Reverse (Far-End Loopback): a special test mode to allow testing the PHY from the link partner side

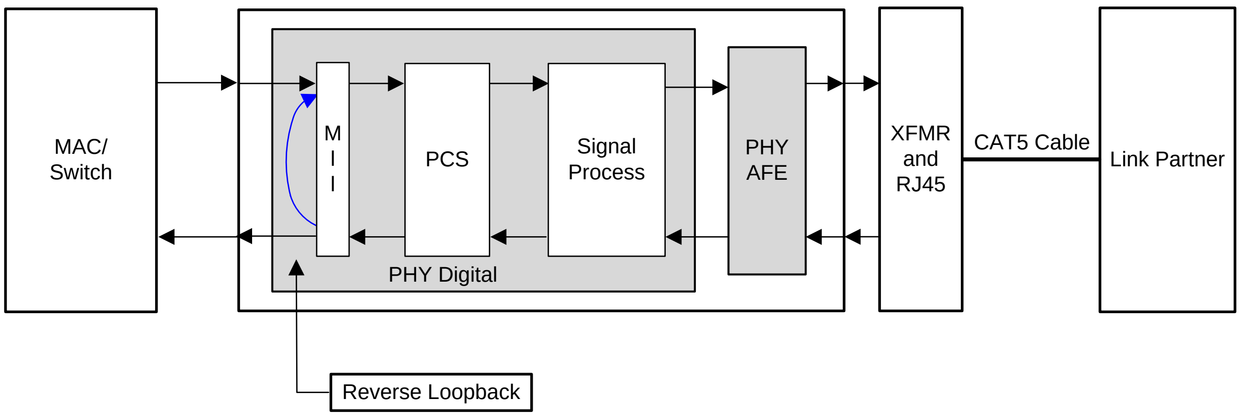

Figure 20. Reverse Loopback

- PRBS Generator/Checker and PRBS Status

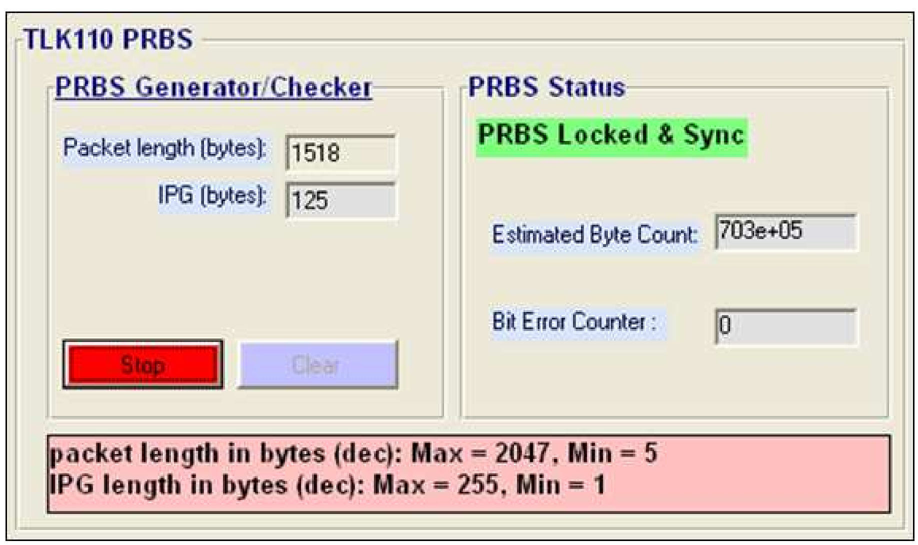

Figure 21. PRBS

To send data from the PRBS generator, establish a link and a loopback. Choose one of the inner loopbacks, force the device to establish a link with itself and then operate the PRBS generator. Another option is to configure a link with a partner and then set the partner to work in reverse loopback mode.

Mode of operation:

– Select packet length
– Choose loopback, if desired
– Click the *Run* button
– Observe the byte counters and error counters
– Click the *Clear* button to set the byte and error counters to 0
– The flashing green announcement states that the PRBS engine is locked and synchronized on the incoming data

The *Bit Error Counter* will either show a value below 256 or state that there are over 256 errors

- SMB Packet Monitor and SMB Packet Generator

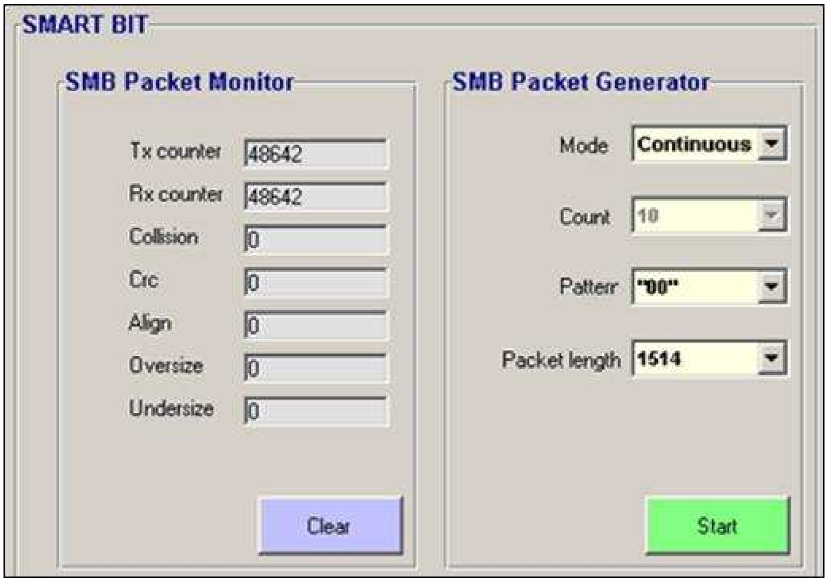

Figure 22. Smart Bit Packet Generator

- SMB Packet Monitor
  - Tx counter: packets sent
  - Rx counter: packets received
  - Collision: cumulative number of collisions that have occurred on the transmitting port of the Smartcard
  - Crc: number of packets received with a bad Crc
  - Align: An alignment error is a packet that does not end on the octet boundary (regardless of Crc)
  - Oversize: cumulative number of oversize packets (greater than 1518 octets) that have arrived on the receiving port of the Smartcard or module
  - Undersize: cumulative number of undersize packets (less than 64 bytes) that have arrived on the receiving port of the Smartcard or module
- Setup packet generator Mode
  - Single burst: Select number of packets in a single burst
  - Continuous: continuously transmit packets
  - Pattern: select from available patterns
  - Packet length: select from available lengths

3.1.6 CD (Cable Diagnostic) Tab

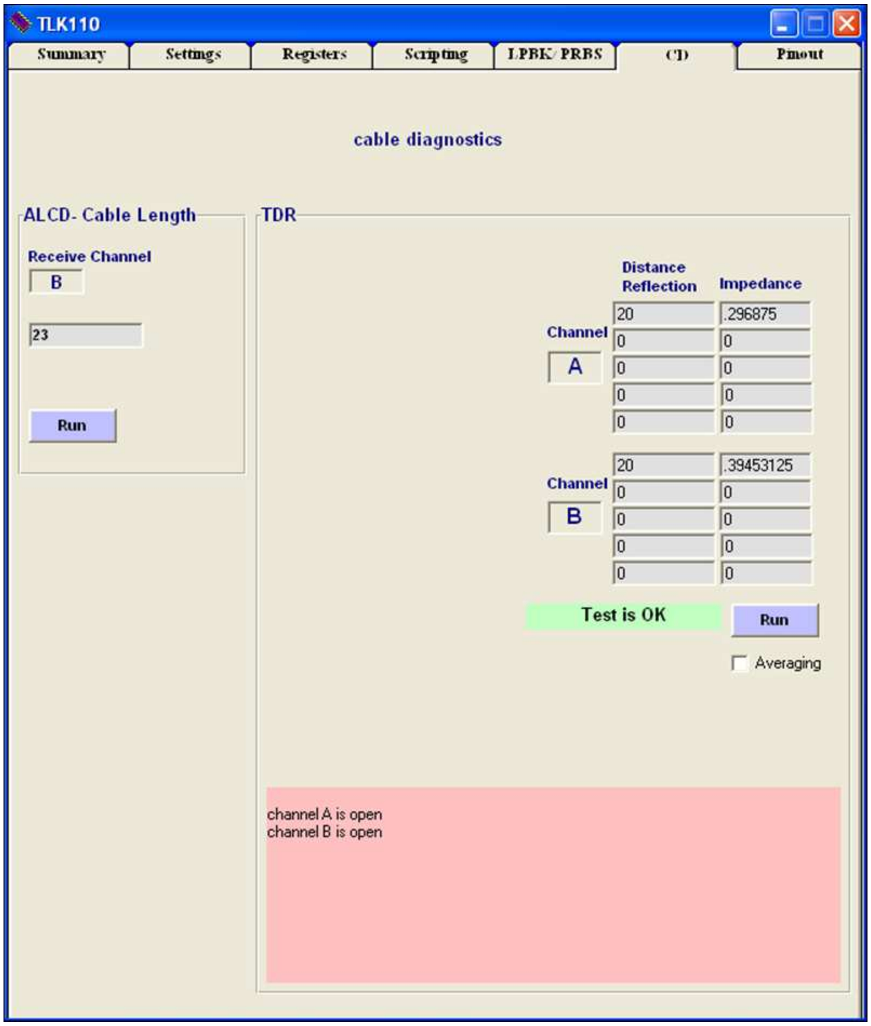

Figure 23. CD

The fields in this tab are:

ALCD - active link cable length measurement

TDR - determines the quality of the cables, connectors, and terminations in addition to estimating the cable length.

Fields Explanation:

- **ALCD** - active link cable diagnostic

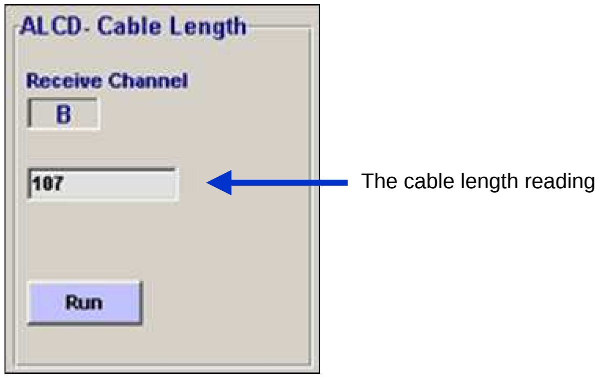

Figure 24. ALCD

The ALCD (as shown in Figure 24) offers a passive method to estimate the cable length present during an active link. It uses passive digital signal processing based on adapted data, thus enabling the measurement of cable length with an active link partner. The ALCD cable length measurement accuracy is ±5 m for the pair used in the Rx path (as a result of the passive nature of the test, only the pair on the Rx path is measured).

Mode of Operation:
Ensure the device is currently under 100BT link.
If, prior to performing ALCD the user performed TDR, It is advised to reset the device (from the *Settings* tab).

– The *Run* button initiates the test

– The *Receive Channel* window shows the current RX pair, either channel A pair: 1, 2 (MDIX) or channel B pair: 3, 6 (MDI)

- **TDR** - Time Domain Reflectometer

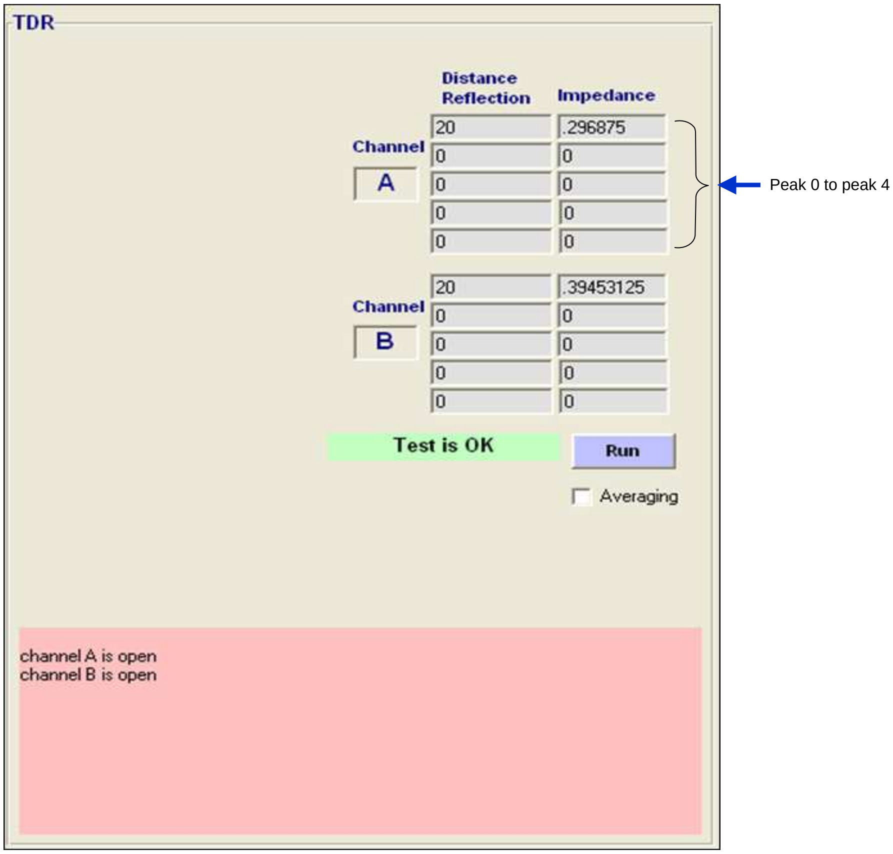

Figure 25. TDR

The TLK1xx uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, and any other discontinuities on the cable.

The TLK1xx device transmits a test pulse down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, bad connector and the end of the cable itself. After the pulse transmission, the TLK1xx measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors), and improperly-terminated cables. Run TDR while there is no link and when you suspect a cable fault. The TDR measurement Accuracy is ±1 m.

3.1.7 Pinout Tab

Figure 26 is a diagram of the device package with an interactive, pin-by-pin functional description.

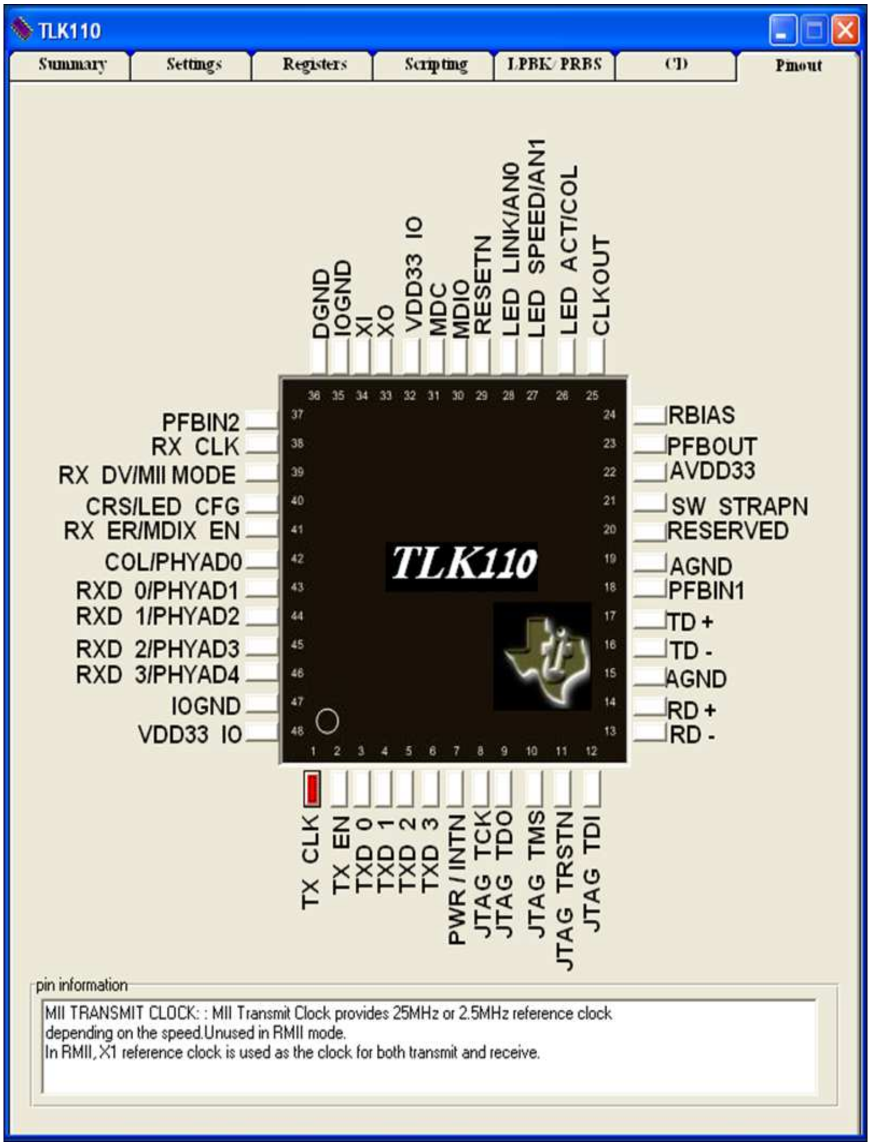

Figure 26. Pin Out

IMPORTANT NOTICE

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