User's Guide for Powering DRA829V and TDA4VM with the TPS6594-Q1 PMICs

This User's Guide can be used as a guide for integrating the TPS6594-Q1 power management integrated circuit (PMIC) into a system powering the DRA829V or TDA4VM device. This document provides the default non-volatile memory (NVM) settings, state transitions, and power sequencing for the system solution.

Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

This user's guide can be used as a guide to understand the power distribution network (PDN) between the two TPS6594-Q1 devices and the DRA829V or TDA4VM processor. This guide describes the platform power resource connections, digital control connections, and the PMIC sequencing settings to support the different state transitions of the processor. The default NVM contents are also included in this guide. This user's guide does not provide information about the electrical characteristics, external components, package, or the functionality of the PMIC or processor devices. For such information and the full register map, refer to the datasheet for each device. In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source.

2 Device Versions

There are different versions of the TPS6594-Q1 device available with unique NVM settings to support different use cases for the processor. The unique NVM settings for each PMIC device are optimized per PDN design to support different processors, processing loads, SDRAM types, system functional safety levels, and end product features - such as low power modes, processor interface levels, SD Card, and so forth. The NVM settings can be distinguished using the NVM_ID register. In this user guide, each PMIC device is distinguished by the part number, NVM_ID, and NVM_REV values listed in Table 1.

Table 1. Dual TPS6594-Q1 NVM Settings and Orderable Part Numbers

PDN USE CASE		ORDERABLE PART NUMBER	DEVICE MODE	NVM_ID	NVM_REV
1	• Up to 12 A[1] on the CORE rail • Up to 6 A[1] on the CPU rails • Up to 3.4 A[1] on the SDRAM, with support for LPDDR4 • Supports Functional Safety up to ASIL-D level • Supports low power modes, including MCU-only and suspend-to-RAM states • Supports I/O level of 3.3 V or 1.8 V • Supports use of SD card	PTPS659413F0RWERQ1	Master	0xF0	0x7
		PTPS659411F0RWERQ1	Slave	0xF0	0x7

(1) TI recommends having 15% margin between the maximum expected load current and the maximum current allowed per each PMIC output rail.

3 Processor Connection

This section details how the dual TPS6594-Q1 power resources and GPIO signals are connected to the SoC processor and other peripheral components in order to support the PDN use case.

Figure 1 shows the detailed power mapping between the processor and the TPS659413-Q1 and TPS659411-Q1 PMICs. In this configuration, both TPS6594-Q1 devices use a 3.3 V input voltage. For Functional Safety applications, there is a protection FET before VCCA that connects to the OVPGDRV pin of the master PMIC, allowing voltage monitoring of the input supply to the PMICs.

The VCCA voltage must be the first voltage applied to the PMIC devices, so VIO_IN of the PMICs must be supplied after VCCA. In this configuration, VIO_IN is supplied by the load switch that also supplies the VDDSHVx_MCU voltage domain of the processor to allow the digital components of the PMIC devices (such as GPIOs) to remain supplied in MCU-only mode. Additionally, by controlling VIO_IN of both PMICs through this load switch, the system can also reduce power consumption in suspend-to-RAM mode, since the load switch is disabled.

For SD card dual-voltage I/O support (3.3 V and 1.8 V), LDO1 of the TPS659411-Q1 device can be used, with a control signal from the processor, to switch the LDO1 voltage between 3.3 V and 1.8 V. This allows control of the LDO1 voltage without the need for the MCU of the processor to establish I2C communication with the PMICs during boot from SD card operations.

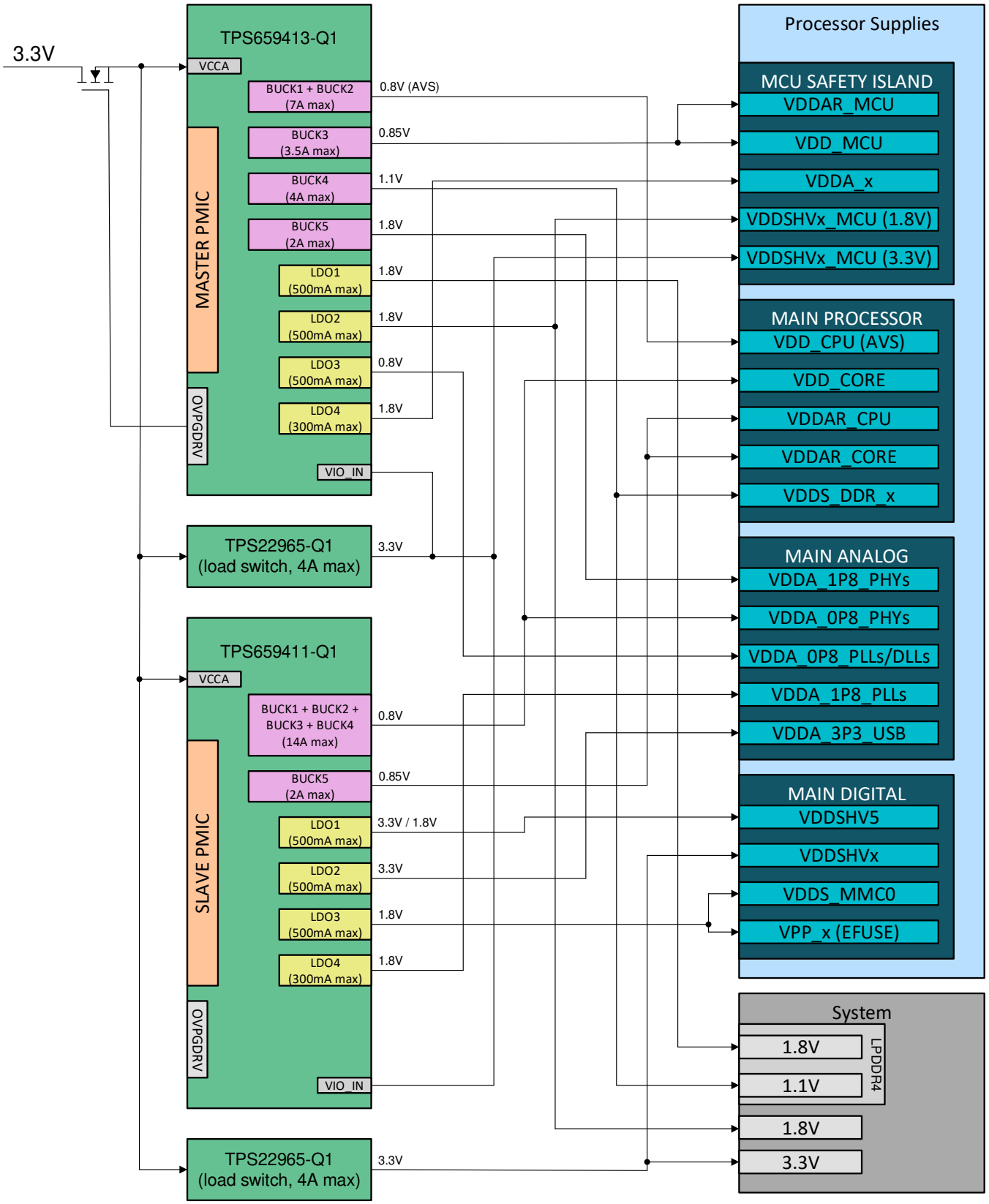

Figure 1. Power Connections with TPS659413-Q1 and TPS659411-Q1

The power connections shown in Figure 1 allow the support for features including MCU-only mode, suspend-to-RAM mode, SD-card integration, and USB interface integration. Please use Table 2 as a guide to understand which power resources are required to support different system features. If the system feature listed is not required, the power connection can be removed and the SoC voltage domains will need to be grouped into alternative power rails.

Table 2. Power Connections by System Feature

Device	PMIC Resource	System Features				
		Active SoC	MCU-only Mode	Suspend-to-RAM Mode	SD Card	USB Interface
TPS659413-Q1	BUCK12	Required				
	BUCK3	Required	Required			
	BUCK4	Required		Required		
	BUCK5	Required				
	LDO1	Required		Required		
	LDO2	Required	Required			
	LDO3	Required				
	LDO4	Required	Required			
TPS659411-Q1	BUCK1234	Required				
	BUCK5	Required				
	LDO1				Required	
	LDO2					Required
	LDO3	Required				
	LDO4	Required				
TPS22965-Q1 (MCU I/O)	Load Switch	Required	Required			
TPS22965-Q1 (MAIN I/O)	Load Switch	Required				

Figure 2 shows the digital control signal mapping between the processor and the TPS659413-Q1 and TPS659411-Q1 PMICs. For the two TPS6594-Q1 devices to work together, master PMIC and slave PMIC must establish an SPMI communication channel in order to synchronize both internal Pre-Configurable State Machines (PFSM) so that they operate as one PFSM across all power and digital resources. The GPIO_5 and GPIO_6 pins on each PMIC are assigned for this functionality. In addition, the master PMIC's LDOVINT pin must be connected to the slave PMIC's ENABLE input to correctly initiate the PFSM.

Other digital connections from the TPS6594-Q1 devices to the processor allow support for error monitoring, processor reset, processor wake up, and system low-power modes. Specific GPIO pins have been assigned to key signals in order to ensure proper operation during low power modes when only a few GPIO pins will remain operational.

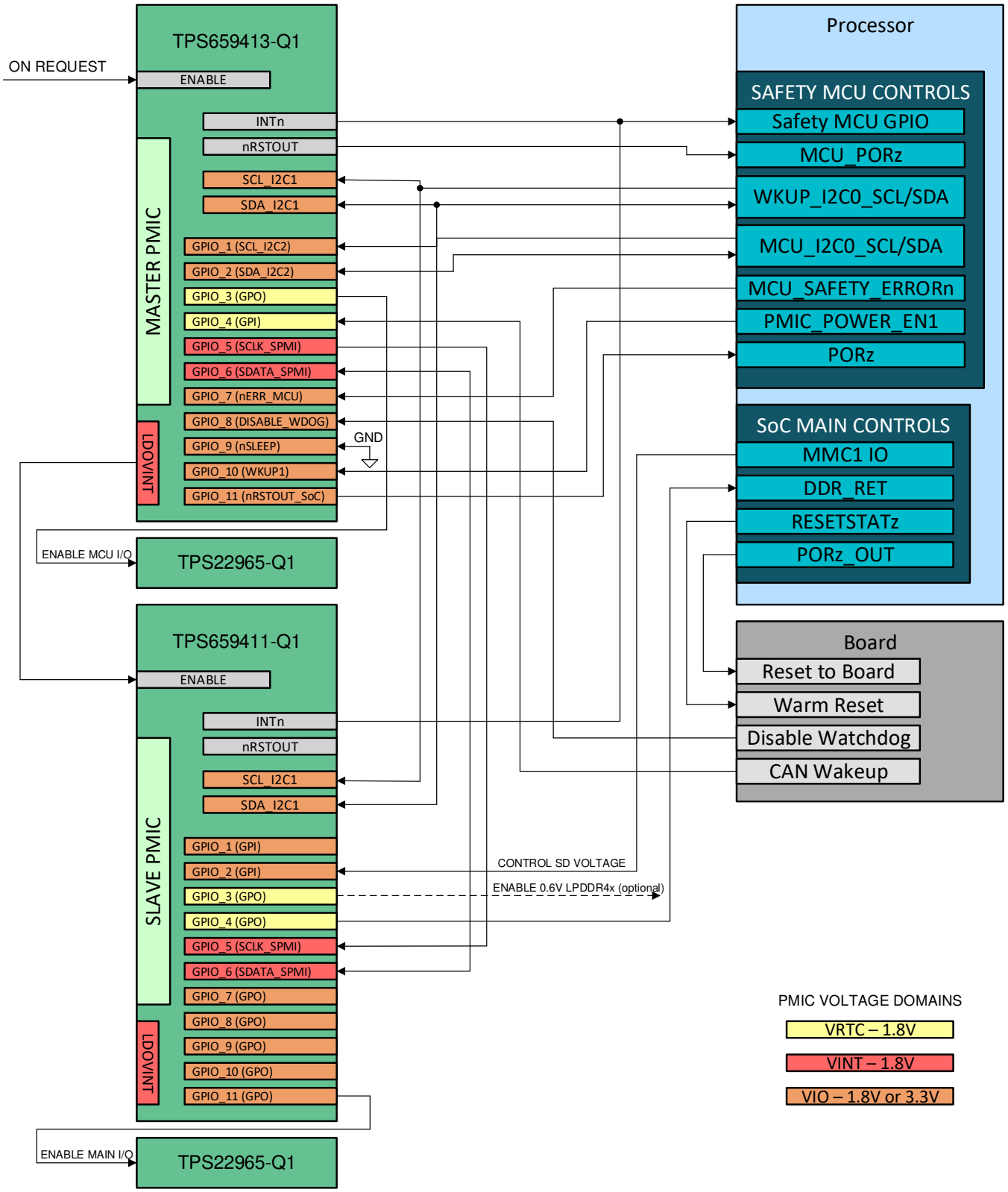

Figure 2. Digital Connections with TPS659413-Q1 and TPS659411-Q1

The digital connections shown in Figure 2 allow system features including MCU-only mode, suspend-to-RAM mode, functional safety up to ASIL-D, compliant dual voltage SD card operation, and LPDDR4x integration. Please use Table 3 as a guide to understand GPIO assignments required for these features. If the feature listed is not required, the digital connection can be removed. For details on how functional safety related connections help achieve functional safety system-level goals, see Section 4.

Table 3. Digital Connections by System Feature

Device	PMIC Digital Signal	System Features					
		Active SoC	Functional Safety	MCU-only Mode	Suspend-to-RAM Mode	SD Card	LPDDR4x
TPS659413-Q1	nPWRON/ENABLE	Required					
	INT		Required				
	nRSTOUT	Required					
	SCL_I2C1	Required					
	SDA_I2C1	Required					
	GPIO_1		Required				
	GPIO_2		Required				
	GPIO_3				Required		
	GPIO_4				Required		
	GPIO_5	Required					
	GPIO_6	Required					
	GPIO_7		Required				
	GPIO_8						
	GPIO_9						
	GPIO_10						
	GPIO_11			Required			
TPS659411-Q1	nPWRON/ENABLE	Required					
	INT		Required				
	nRSTOUT						
	SCL_I2C1	Required					
	SDA_I2C1	Required					
	GPIO_1						
	GPIO_2					Required	
	GPIO_3						Required
	GPIO_4				Required		
	GPIO_5	Required					
	GPIO_6	Required					
	GPIO_7						
	GPIO_8						
	GPIO_9						
	GPIO_10						
	GPIO_11			Required	Required		

4 Supporting Functional Safety Systems

By utilizing the dual TPS6594-Q1 solution to power the DRA829V or TDA4VM processor, the system can utilize the following PMIC functional safety features:

- Independent Power Control of MCU and Main Rails
- Independent Monitoring and Reset for MCU and Main Rails
- Input Supply Monitoring

- Output Voltage and Current Monitoring
- Question/Answer Watchdog
- Fault Reporting Interrupts
- Enable Drive Pin that provides an independent path to disable system actuators
- Error Pin Monitoring
- Internal Diagnostics including voltage monitoring, temperature monitoring, and Built-In Self-Test

Please refer to the Safety Manual of the TPS6594-Q1 device for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-D rating for a system. Additionally, these features help in achieving the functional safety assumptions utilized by the processor to achieve up to ASIL-D rating. See the DRA829/TDA4VM Safety Manual for Jacinto™ 7 Processors for a complete list of functional safety system assumptions.

4.1 Achieving ASIL-B System Requirements

To achieve a functional safety level of ASIL-B for the dual TPS6594-Q1 and SoC system, the following features are available within the PDN:

- PMIC over voltage and under voltage monitoring on the output power rails
- PMIC over-voltage monitoring and protection on the input to the PMIC (VCCA)
- Watchdog
- MCU error monitoring
- MCU reset
- I2C communication
- Error indicator for driving external circuitry (Optional)

There is the option for using an external power FET to shut off the PMICs when an over-voltage event is detected on the input to protect the system from being damaged as shown in Figure 1. Note that any power rail connected after the FET can be protected from an over voltage event. Any power connected upstream from the FET is not protected from over voltage events. In Figure 1 the load switches to power the MCU I/O and the Main I/O are connected after the FET to protect the their pins from observing greater than 6 V in the event of a short of the previous power stage.

The PMIC internal over voltage and under voltage monitoring and their respective monitoring threshold levels are enabled by default and can be updated through I2C after startup. PMIC power rails connected directly to the processor are monitored by default, however, the rails supplied through the load switches are not monitored. To monitor the load switch voltage that supplies the MCU I/O of the processor, it is recommended to use the processor's POK monitor built into the VDDSHV0_MCU voltage domain. For monitoring the load switch voltage that supplies the Main I/O, an unused feedback pin of the TPS659411-Q1 (FB_B3 or FB_B4) can be configured through I2C and connected to the output of the load switch to enable monitoring.

The PMIC's Internal Q&A Watchdog is enabled by default on the TPS659413-Q1 device. Once the device is in ACTIVE state, the trigger or Q&A watchdog settings can be configured through the secondary I2C in the device. The steps for configuring the watchdog settings can be found in the TPS6594-Q1 datasheet. GPIO_7 of the TPS659413-Q1 PMIC is configured as the MCU error signal monitoring, but will need to be enabled though the ESM_MCU_EN register bit. MCU reset is supported through the connection between the master PMIC nRSTOUT pin and the MCU_PORz of the processor. Lastly, there are 2 I2C ports between the TPS659413-Q1 and the processor which allows the watchdog monitoring to be on an independent communication channel.

There is an option to use EN_DRV of the TPS659413-Q1 PMIC to indicate an error has been detected and the system is entering SAFE state. This signal can be utilized if the system has some additional external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized, but available if needed.

4.2 Achieving up to ASIL-D System Requirements

For ASIL-C or ASIL-D systems, there are additional features to the ones described in Section 4.1 that can be utilized. These features include:

- PMIC current monitoring on all output power rails
- Isolation of the MCU and Main power domains of the processor
- SoC error monitoring
- SoC reset

The current monitoring is enabled by default for all BUCKs and LDOs for the TPS659413-Q1 and TPS659411-Q1 devices. Additionally, Figure 1 shows that the MCU domain of the processor is powered by different power resources of the PMICs than the main power domain of the processor. SoC error signal monitoring can be utilized if GPIO_3 of TPS659411-Q1 is available to be reconfigured as nERR_SoC. This feature would need to be enabled through I2C using the ESM_SOC_EN register bit. The SoC reset functionality is supported through the connection of GPIO_11 on TPS659413-Q1, configured as nRSTOUT_SoC, to the PORz pin of the processor.

5 Static NVM Settings

The TPS6594x-Q1 devices consist of fixed registers and configurable registers that are loaded from NVM. For all NVM registers, the initial NVM settings that load into the registers are provided in this section. Note that these initial NVM settings can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The full register map, including default values of fixed registers, is located in the TPS6594x-Q1 datasheet.

5.1 Application-Based Configuration Settings

In the TPS6594-Q1 datasheet, there are 7 application-based configurations for each BUCK to operate within. The following list includes the different configurations available:

- 2.2 MHz Single Phase for DDR Termination
- 4.4 MHz Multi-phase Configuration
- 4.4 MHz Single Phase Low Output Voltage
- 4.4 MHz Single Phase High Output Voltage
- 2.2 MHz Multi-phase with Full Range VIN
- 2.2 MHz Single Phase with 5.0 V VIN
- 2.2 MHz Single Phase with Full Range VIN

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 4 shows the default configurations for the BUCKs. These settings cannot be changed after device startup.

Table 4. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
	BUCK1	2.2 MHz Multi-phase with Full Range VIN	470 nH
	BUCK2		470 nH
	BUCK3	2.2 MHz Multi-phase with Full Range VIN	470 nH
	BUCK4	2.2 MHz Multi-phase with Full Range VIN	470 nH
	BUCK5	2.2 MHz Multi-phase with Full Range VIN	470 nH
	BUCK1	2.2 MHz Multi-phase with Full Range VIN	470 nH
	BUCK2		470 nH
	BUCK3		470 nH
	BUCK4		470 nH
	BUCK5	2.2 MHz Multi-phase with Full Range VIN	470 nH

5.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

Table 5. Device Identification NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
DEV_REV	SILICON_VERSION	000b		000b	
	DEVICE_ID	001b		001b	
NVM_CODE_1	NVM_ID	11110000b	0xF0	11110000b	0xF0
NVM_CODE_2	NVM_REV	000111b		000111b	
PHASE_CONFIG	MP_CONFIG	010b	2+1+1+1	000b	4+1

5.3 BUCK Settings

These settings detail the default voltages, configurations, and monitoring of the BUCK rails. All these settings can be changed though I^2C after startup.

Table 6. BUCK NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
BUCK1_CTRL	BUCK1_EN(1)	0b	BUCK regulator is disabled	0b	BUCK regulator is disabled
	BUCK1_FPWM	1b	Forced to PWM operation.	1b	Forced to PWM operation.
	BUCK1_FPWM_MP	0b	Automatic phase adding and shedding.	0b	Automatic phase adding and shedding.
	BUCK1_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	BUCK1_VSEL	0b	BUCK1_VOUT_1	0b	BUCK1_VOUT_1
	BUCK1_PLDN	1b	Enabled	1b	Enabled
	BUCK1_RV_SEL	1b	Enabled	1b	Enabled
BUCK1_CONF	BUCK1_SLEW_RATE	100b	2.5 mV/µs	100b	2.5 mV/µs
	BUCK1_ILIM	101b	5.5 A	101b	5.5 A
BUCK2_CTRL	BUCK2_EN(1)	0b	BUCK regulator is disabled	0b	BUCK regulator is disabled
	BUCK2_FPWM	1b	Forced to PWM operation.	1b	Forced to PWM operation.
	BUCK2_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	BUCK2_VSEL	0b	BUCK2_VOUT_1	0b	BUCK2_VOUT_1
	BUCK2_PLDN	1b	Enabled	1b	Enabled
	BUCK2_RV_SEL	1b	Enabled	1b	Enabled
BUCK2_CONF	BUCK2_SLEW_RATE	111b	0.31 mV/µs	111b	0.31 mV/µs
	BUCK2_ILIM	101b	5.5 A	101b	5.5 A

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

Table 6. BUCK NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
BUCK3_CTRL	BUCK3_EN[1]	0b	BUCK regulator is disabled	0b	BUCK regulator is disabled
	BUCK3_FPWM	1b	Forced to PWM operation.	1b	Forced to PWM operation.
	BUCK3_FPWM_MP	0b	Automatic phase adding and shedding.	0b	Automatic phase adding and shedding.
	BUCK3_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	BUCK3_VSEL	0b	BUCK3_VOUT_1	0b	BUCK3_VOUT_1
	BUCK3_PLDN	1b	Pull-down resistor enabled	1b	Pull-down resistor enabled
	BUCK3_RV_SEL	1b	Enabled	1b	Enabled
BUCK3_CONF	BUCK3_SLEW_RATE	100b	2.5 mV/µs	111b	0.31 mV/µs
	BUCK3_ILIM	101b	5.5 A	101b	5.5 A
BUCK4_CTRL	BUCK4_EN[1]	0b	BUCK regulator is disabled	0b	BUCK regulator is disabled
	BUCK4_FPWM	1b	Forced to PWM operation.	1b	Forced to PWM operation.
	BUCK4_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	BUCK4_VSEL	0b	BUCK4_VOUT_1	0b	BUCK4_VOUT_1
	BUCK4_PLDN	1b	Pull-down resistor enabled	1b	Pull-down resistor enabled
	BUCK4_RV_SEL	1b	Enabled	1b	Enabled
BUCK4_CONF	BUCK4_SLEW_RATE	100b	2.5 mV/µs	111b	0.31 mV/µs
	BUCK4_ILIM	101b	5.5 A	101b	5.5 A
BUCK5_CTRL	BUCK5_EN[1]	0b	BUCK regulator is disabled	0b	BUCK regulator is disabled
	BUCK5_FPWM	1b	Forced to PWM operation.	1b	Forced to PWM operation.
	BUCK5_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	BUCK5_VSEL	0b	BUCK5_VOUT_1	0b	BUCK5_VOUT_1
	BUCK5_PLDN	1b	Pull-down resistor enabled	1b	Pull-down resistor enabled
	BUCK5_RV_SEL	1b	Enabled	1b	Enabled
BUCK5_CONF	BUCK5_SLEW_RATE	011b	5.0 mV/µs	100b	2.5 mV/µs
	BUCK5_ILIM	011b	3.5 A	011b	3.5 A
BUCK1_VOUT_1	BUCK1_VSET1	00110111b	0.8 V	00110111b	0.8 V
BUCK1_VOUT_2	BUCK1_VSET2	00000000b	0.3 V	00000000b	0.3 V
BUCK2_VOUT_1	BUCK2_VSET1	00110111b	0.8 V	00110111b	0.8 V
BUCK2_VOUT_2	BUCK2_VSET2	00000000b	0.3 V	00000000b	0.3 V
BUCK3_VOUT_1	BUCK3_VSET1	01000001b	0.85 V	00110111b	0.8 V
BUCK3_VOUT_2	BUCK3_VSET2	00000000b	0.3 V	00000000b	0.3 V
BUCK4_VOUT_1	BUCK4_VSET1	01110011b	1.1 V	00110111b	0.8 V
BUCK4_VOUT_2	BUCK4_VSET2	00000000b	0.3 V	00000000b	0.3 V
BUCK5_VOUT_1	BUCK5_VSET1	10110010b	1.8 V	01000001b	0.85 V
BUCK5_VOUT_2	BUCK5_VSET2	00000000b	0.3 V	00000000b	0.3 V

Table 6. BUCK NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
BUCK1_PG_WINDOW	BUCK1_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	BUCK1_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	BUCK2_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	BUCK3_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	BUCK4_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	BUCK5_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV

5.4 LDO Settings

These settings detail the default voltages, configurations, and monitoring of the LDO rails. All these settings can be changed though I^2C after startup.

Table 7. LDO NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
LDO1_CTRL	LDO1_EN(1)	0b	LDO1 regulator is disabled	0b	LDO1 regulator is disabled
	LDO1_PLDN	01b	125 Ohm	01b	125 Ohm
	LDO1_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	LDO1_RV_SEL	1b	Enabled	1b	Enabled
LDO2_CTRL	LDO2_EN(1)	0b	LDO2 regulator is disabled	0b	LDO2 regulator is disabled
	LDO2_PLDN	01b	125 Ohm	01b	125 Ohm
	LDO2_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	LDO2_RV_SEL	1b	Enabled	1b	Enabled
LDO3_CTRL	LDO3_EN(1)	0b	LDO3 regulator is disabled	0b	LDO3 regulator is disabled
	LDO3_PLDN	11b	500 Ohm	01b	125 Ohm
	LDO3_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	LDO3_RV_SEL	1b	Enabled	1b	Enabled
LDO4_CTRL	LDO4_EN(1)	0b	LDO4 regulator is disabled	0b	LDO4 regulator is disabled
	LDO4_PLDN	01b	125 Ohm	01b	125 Ohm
	LDO4_VMON_EN	0b	OV and UV comparators are disabled	0b	OV and UV comparators are disabled
	LDO4_RV_SEL	1b	Enabled	1b	Enabled
LDOINT_CTRL	LDOINT_VMON_EN	1b	OV and UV comparators are enabled.	1b	OV and UV comparators are enabled.

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

Table 7. LDO NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
LDORTC_CTRL	LDORTC_VMON_EN	1b	UVLO comparator is enabled.	1b	UVLO comparator is enabled.
LDO1_VOUT	LDO1_VSET	011100b	1.8 V	111010b	3.3 V
	LDO1_BYPASS	0b	LDO is set to linear regulator mode.	1b	LDO is set to bypass mode.
LDO2_VOUT	LDO2_VSET	011100b	1.8 V	111010b	3.3 V
	LDO2_BYPASS	0b	LDO is set to linear regulator mode.	1b	LDO is set to bypass mode.
LDO3_VOUT	LDO3_VSET	001000b	0.8 V	011100b	1.8 V
	LDO3_BYPASS	0b	LDO is set to linear regulator mode.	0b	LDO is set to linear regulator mode.
LDO4_VOUT	LDO4_VSET	0111000b	1.8 V	0111000b	1.8 V
LDO1_PG_WINDOW	LDO1_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	LDO1_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
LDO2_PG_WINDOW	LDO2_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	LDO2_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
LDO3_PG_WINDOW	LDO3_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	LDO3_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV
LDO4_PG_WINDOW	LDO4_OV_THR	010b	+4% / +40 mV	010b	+4% / +40 mV
	LDO4_UV_THR	010b	-4% / -40 mV	010b	-4% / -40 mV

5.5 VCCA Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed though I^2C after startup.

Table 8. VCCA NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
VCCA_VMON_CTRL	VCCA_VMON_EN	1b	OV and UV comparators are enabled.	0b	OV and UV comparators are disabled
VCCA_PG_WINDOW	VCCA_OV_THR	111b	+10%	111b	+10%
	VCCA_UV_THR	111b	-10%	111b	-10%
	VCCA_PG_SET	0b	3.3 V	0b	3.3 V

5.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All these settings can be changed though I^2C after startup. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the "Digital Signal Descriptions" section in the TPS6594x-Q1 datasheet.

Table 9. GPIO NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
GPIO1_CONF	GPIO1_OD	1b	Open-drain output	0b	Push-pull output
	GPIO1_DIR	0b	Input	0b	Input
	GPIO1_SEL	001b	SCL_I2C2/CS_SPI	000b	GPIO1
	GPIO1_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO1_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	0b	Pull-up/pull-down resistor disabled
	GPIO1_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
GPIO2_CONF	GPIO2_OD	1b	Open-drain output	0b	Push-pull output
	GPIO2_DIR	0b	Input	0b	Input
	GPIO2_SEL	010b	SDA_I2C2/SDO_SPI	000b	GPIO2
	GPIO2_PU_SEL	0b	Pull-down resistor selected	1b	Pull-up resistor selected
	GPIO2_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	1b	Pull-up/pull-down resistor enabled
	GPIO2_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
GPIO3_CONF	GPIO3_OD	0b	Push-pull output	0b	Push-pull output
	GPIO3_DIR	1b	Output	1b	Output
	GPIO3_SEL	000b	GPIO3	000b	GPIO3
	GPIO3_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO3_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	0b	Pull-up/pull-down resistor disabled
	GPIO3_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
GPIO4_CONF	GPIO4_OD	1b	Open-drain output	1b	Open-drain output
	GPIO4_DIR	0b	Input	1b	Output
	GPIO4_SEL	000b	GPIO4	000b	GPIO4
	GPIO4_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO4_PU_PD_EN	1b	Pull-up/pull-down resistor enabled	0b	Pull-up/pull-down resistor disabled
	GPIO4_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
GPIO5_CONF	GPIO5_OD	0b	Push-pull output	0b	Push-pull output
	GPIO5_DIR	1b	Output	0b	Input
	GPIO5_SEL	001b	SCLK_SPMI	001b	SCLK_SPMI
	GPIO5_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO5_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	0b	Pull-up/pull-down resistor disabled
	GPIO5_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.

Table 9. GPIO NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
GPIO6_CONF	GPIO6_OD	0b	Push-pull output	0b	Push-pull output
	GPIO6_DIR	1b	Output	0b	Input
	GPIO6_SEL	001b	SDATA_SPMI	001b	SDATA_SPMI
	GPIO6_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO6_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	0b	Pull-up/pull-down resistor disabled
	GPIO6_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
GPIO7_CONF	GPIO7_OD	1b	Open-drain output	0b	Push-pull output
	GPIO7_DIR	0b	Input	1b	Output
	GPIO7_SEL	001b	NERR_MCU	000b	GPIO7
	GPIO7_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO7_PU_PD_EN	1b	Pull-up/pull-down resistor enabled	0b	Pull-up/pull-down resistor disabled
	GPIO7_DEGLITCH_EN	1b	10 us deglitch time.	0b	No deglitch, only synchronization.
GPIO8_CONF	GPIO8_OD	1b	Open-drain output	0b	Push-pull output
	GPIO8_DIR	0b	Input	1b	Output
	GPIO8_SEL	011b	DISABLE_WDOG	000b	GPIO8
	GPIO8_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO8_PU_PD_EN	1b	Pull-up/pull-down resistor enabled	0b	Pull-up/pull-down resistor disabled
	GPIO8_DEGLITCH_EN	1b	10 us deglitch time.	0b	No deglitch, only synchronization.
GPIO9_CONF	GPIO9_OD	1b	Open-drain output	0b	Push-pull output
	GPIO9_DIR	0b	Input	1b	Output
	GPIO9_SEL	100b	NSLEEP1	000b	GPIO9
	GPIO9_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO9_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	0b	Pull-up/pull-down resistor disabled
	GPIO9_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
GPIO10_CONF	GPIO10_OD	1b	Open-drain output	0b	Push-pull output
	GPIO10_DIR	0b	Input	0b	Input
	GPIO10_SEL	110b	WKUP1	000b	GPIO10
	GPIO10_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO10_PU_PD_EN	1b	Pull-up/pull-down resistor enabled	1b	Pull-up/pull-down resistor enabled
	GPIO10_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.

Table 9. GPIO NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
GPIO11_CONF	GPIO11_OD	1b	Open-drain output	0b	Push-pull output
	GPIO11_DIR	1b	Output	1b	Output
	GPIO11_SEL	010b	NRSTOUT_SOC	000b	GPIO11
	GPIO11_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	GPIO11_PU_PD_EN	0b	Pull-up/pull-down resistor disabled	0b	Pull-up/pull-down resistor disabled
	GPIO11_DEGLITCH_EN	0b	No deglitch, only synchronization.	0b	No deglitch, only synchronization.
NPWRON_CONF	NPWRON_SEL	00b	ENABLE	00b	ENABLE
	ENABLE_PU_SEL	0b	Pull-down resistor selected	0b	Pull-down resistor selected
	ENABLE_PU_PD_EN	1b	Pull-up/pull-down resistor enabled	0b	Pull-up/pull-down resistor disabled
	ENABLE_DEGLITCH_EN	1b	10 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.	1b	10 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.
	ENABLE_POL	0b	Active high	0b	Active high
	NRSTOUT_OD	1b	Open-drain output	0b	Push-pull output
GPIO_OUT_1	GPIO1_OUT(1)	0b	Low	0b	Low
	GPIO2_OUT(1)	0b	Low	0b	Low
	GPIO3_OUT(1)	0b	Low	0b	Low
	GPIO4_OUT(1)	0b	Low	0b	Low
	GPIO5_OUT(1)	0b	Low	0b	Low
	GPIO6_OUT(1)	0b	Low	0b	Low
	GPIO7_OUT(1)	0b	Low	0b	Low
	GPIO8_OUT(1)	0b	Low	0b	Low
GPIO_OUT_2	GPIO9_OUT(1)	0b	Low	0b	Low
	GPIO10_OUT(1)	0b	Low	0b	Low
	GPIO11_OUT(1)	0b	Low	0b	Low

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

5.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though I^2C after startup.

Table 10. FSM NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	10b	SOC rail group	10b	SOC rail group
	BUCK2_GRP_SEL	10b	SOC rail group	10b	SOC rail group
	BUCK3_GRP_SEL	01b	MCU rail group	10b	SOC rail group
	BUCK4_GRP_SEL	01b	MCU rail group	10b	SOC rail group

Table 10. FSM NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
RAIL_SEL_2	BUCK5_GRP_SEL	10b	SOC rail group	10b	SOC rail group
	LDO1_GRP_SEL	01b	MCU rail group	10b	SOC rail group
	LDO2_GRP_SEL	01b	MCU rail group	10b	SOC rail group
	LDO3_GRP_SEL	10b	SOC rail group	10b	SOC rail group
RAIL_SEL_3	LDO4_GRP_SEL	01b	MCU rail group	10b	SOC rail group
	VCCA_GRP_SEL	01b	MCU rail group	01b	MCU rail group
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	10b	MCU power error	10b	MCU power error
	SOC_RAIL_TRIG	11b	SOC power error	11b	SOC power error
	OTHER_RAIL_TRIG	11b	SOC power error	11b	SOC power error
	SEVERE_ERR_TRIG	00b	Immediate shutdown	00b	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	01b	Orderly shutdown	01b	Orderly shutdown

5.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though I^2C after startup.

Table 11. Interrupt NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	1b	Masked	1b	Masked
	GPIO1_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO2_FSM_MASK	1b	Masked	0b	Not masked
	GPIO2_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO3_FSM_MASK	1b	Masked	1b	Masked
	GPIO3_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO4_FSM_MASK	0b	Not masked	1b	Masked
	GPIO4_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	1b	Masked	1b	Masked
	GPIO5_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO6_FSM_MASK	1b	Masked	1b	Masked
	GPIO6_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO7_FSM_MASK	1b	Masked	1b	Masked
	GPIO7_FSM_MASK_POL	1b	Masking sets signal value to '1'	0b	Masking sets signal value to '0'
	GPIO8_FSM_MASK	1b	Masked	1b	Masked
	GPIO8_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'

Table 11. Interrupt NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	1b	Masked	1b	Masked
	GPIO9_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO10_FSM_MASK	1b	Masked	1b	Masked
	GPIO10_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
	GPIO11_FSM_MASK	1b	Masked	1b	Masked
	GPIO11_FSM_MASK_POL	0b	Masking sets signal value to '0'	0b	Masking sets signal value to '0'
MASK_BUCK1_2	BUCK1_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK1_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK1_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK2_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK2_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK2_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_BUCK3_4	BUCK3_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK3_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK3_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK4_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK4_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK4_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_BUCK5	BUCK5_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK5_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BUCK5_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_LDO1_2	LDO1_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO1_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO2_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO2_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO1_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO2_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.

Table 11. Interrupt NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
MASK_LDO3_4	LDO3_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO3_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO4_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO4_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO3_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	LDO4_ILIM_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_VMON	VCCA_OV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	VCCA_UV_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO2_FALL_MASK	1b	Interrupt not generated.	0b	Interrupt generated
	GPIO3_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO4_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO5_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO6_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO7_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO8_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO2_RISE_MASK	1b	Interrupt not generated.	0b	Interrupt generated
	GPIO3_RISE_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO4_RISE_MASK	0b	Interrupt generated	1b	Interrupt not generated.
	GPIO5_RISE_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO6_RISE_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO7_RISE_MASK	0b	Interrupt generated	1b	Interrupt not generated.
	GPIO8_RISE_MASK	0b	Interrupt generated	1b	Interrupt not generated.

Table 11. Interrupt NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
MASK_GPIO9_11	GPIO9_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO9_RISE_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO10_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO11_FALL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	GPIO10_RISE_MASK	0b	Interrupt generated	1b	Interrupt not generated.
	GPIO11_RISE_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_STARTUP	NPWRON_START_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	ENABLE_MASK	0b	Interrupt generated	0b	Interrupt generated
	FSD_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_MISC	TWARN_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	BIST_PASS_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	EXT_CLK_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_MODERATE_ERR	BIST_FAIL_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	REG_CRC_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	SPMI_ERR_MASK	0b	Interrupt generated	0b	Interrupt generated
	NPWRON_LONG_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	PFSM_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	0b	Interrupt generated	0b	Interrupt generated
	MCU_PWR_ERR_MASK	0b	Interrupt generated	0b	Interrupt generated
	SOC_PWR_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	ORD_SHUTDOWN_MASK	0b	Interrupt generated	0b	Interrupt generated
MASK_COMM_ERR	COMM_FRM_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	COMM_CRC_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	COMM_ADR_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	I2C2_CRC_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
	I2C2_ADR_ERR_MASK	1b	Interrupt not generated.	1b	Interrupt not generated.
MASK_READBACK_ERR	EN_DRV_READBACK_MASK	0b	Interrupt generated	1b	Interrupt not generated.
	NINT_READBACK_MASK	0b	Interrupt generated	0b	Interrupt generated
	NRSTOUT_READBACK_MASK	0b	Interrupt generated	1b	Interrupt not generated.
	NRSTOUT_SOC_READBACK_MASK	0b	Interrupt generated	1b	Interrupt not generated.

Table 11. Interrupt NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
MASK_ESM	ESM_SOC_PIN_MASK	0b	Interrupt generated	0b	Interrupt generated
	ESM_SOC_RST_MASK	0b	Interrupt generated	0b	Interrupt generated
	ESM_SOC_FAIL_MASK	0b	Interrupt generated	0b	Interrupt generated
	ESM_MCU_PIN_MASK	0b	Interrupt generated	0b	Interrupt generated
	ESM_MCU_RST_MASK	0b	Interrupt generated	0b	Interrupt generated
	ESM_MCU_FAIL_MASK	0b	Interrupt generated	0b	Interrupt generated

5.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I^2C after startup.

Table 12. POWERGOOD NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
	PGOOD_SEL_BUCK2	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
	PGOOD_SEL_BUCK3	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
	PGOOD_SEL_BUCK4	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
PGOOD_SEL_2	PGOOD_SEL_BUCK5	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
PGOOD_SEL_3	PGOOD_SEL_LDO1	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
	PGOOD_SEL_LDO2	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
	PGOOD_SEL_LDO3	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
	PGOOD_SEL_LDO4	10b	Powergood threshold voltage AND current limit	10b	Powergood threshold voltage AND current limit
PGOOD_SEL_4	PGOOD_SEL_VCCA	0b	Masked	0b	Masked
	PGOOD_SEL_TDIE_WARN	0b	Masked	0b	Masked
	PGOOD_SEL_NRSTOUT	0b	Masked	0b	Masked
	PGOOD_SEL_NRSTOUT_SOC	0b	Masked	0b	Masked
	PGOOD_POL	0b	PGOOD signal is high when monitored inputs are valid	0b	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	1b	Both undervoltage and overvoltage are monitored	1b	Both undervoltage and overvoltage are monitored

5.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings can be changed though I^2C after startup.

Table 13. Miscellaneous NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
PLL_CTRL	EXT_CLK_FREQ	01b	2.2 MHz	01b	2.2 MHz
CONFIG_1	TWARN_LEVEL	0b	120C	0b	120C
	I2C1_HS	0b	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.	0b	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.
	I2C2_HS	0b	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.	0b	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.
	EN_ILIM_FSM_CTRL	0b	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.	0b	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0b	NSLEEP1(B) affects FSM state transitions.	1b	NSLEEP1(B) does not affect FSM state transitions.
	NSLEEP2_MASK	0b	NSLEEP2(B) affects FSM state transitions.	1b	NSLEEP2(B) does not affect FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0b	Disabled	0b	Disabled
	BB_VEOC	00b	2.5V	00b	2.5V
	BB_ICHR	0b	100uA	0b	100uA
RECOV_CNT_REG_2	RECOV_CNT_THR	1111b		1111b	
BUCK_RESET_REG	BUCK1_RESET	0b		0b	
	BUCK2_RESET	0b		0b	
	BUCK3_RESET	0b		0b	
	BUCK4_RESET	0b		0b	
	BUCK5_RESET	0b		0b	
SPREAD_SPECTRUM_1	SS_EN	0b	Spread spectrum disabled	0b	Spread spectrum disabled
	SS_MODE	00b	No modulation	00b	No modulation
	SS_DEPTH	00b	No modulation	00b	No modulation
SPREAD_SPECTRUM_2	SS_PARAM1	0000b		0000b	
	SS_PARAM2	0000b		0000b	
FREQ_SEL	BUCK1_FREQ_SEL	0b	2.2 MHz	0b	2.2 MHz
	BUCK2_FREQ_SEL	0b	2.2 MHz	0b	2.2 MHz
	BUCK3_FREQ_SEL	0b	2.2 MHz	0b	2.2 MHz
	BUCK4_FREQ_SEL	0b	2.2 MHz	0b	2.2 MHz
	BUCK5_FREQ_SEL	0b	2.2 MHz	0b	2.2 MHz
FSM_STEP_SIZE	PFSM_DELAY_STEP	01100b		01100b	
LDO_RV_TIMEOUT_REG_1	LDO1_RV_TIMEOUT	1111b	16ms	1111b	16ms
	LDO2_RV_TIMEOUT	1111b	16ms	1111b	16ms
LDO_RV_TIMEOUT_REG_2	LDO3_RV_TIMEOUT	1111b	16ms	1111b	16ms
	LDO4_RV_TIMEOUT	1111b	16ms	1111b	16ms

Table 13. Miscellaneous NVM Settings (continued)

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
USER_SPARE_REGS	USER_SPARE_1	0b		0b	
	USER_SPARE_2	0b		0b	
	USER_SPARE_3	0b		0b	
	USER_SPARE_4	0b		0b	
ESM_MCU_MODE_CFG	ESM_MCU_EN	0b	ESM_MCU disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared	0b	ESM_MCU disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared
ESM_SOC_MODE_CFG	ESM_SOC_EN	0b	ESM_SoC disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared	0b	ESM_SoC disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared
RTC_CTRL_2	XTAL_EN	1b	Crystal oscillator is enabled	0b	Crystal oscillator is disabled
	LP_STANDBY_SEL	1b	Low power standby state is used as standby state (LDOINT is disabled).	1b	Low power standby state is used as standby state (LDOINT is disabled).
	FAST_BIST	1b	Only analog BIST is run when transitioning from LP_STANDBY to ACTIVE state.	1b	Only analog BIST is run when transitioning from LP_STANDBY to ACTIVE state.
	STARTUP_DEST	11b	ACTIVE	11b	ACTIVE
	XTAL_SEL	01b	9 pF	00b	6 pF
PFSM_DELAY_REG_1	PFSM_DELAY1	00101010b		00000000b	
PFSM_DELAY_REG_2	PFSM_DELAY2	00000000b		00000000b	
PFSM_DELAY_REG_3	PFSM_DELAY3	00000000b		00000000b	
PFSM_DELAY_REG_4	PFSM_DELAY4	00000000b		00000000b	

5.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed after device startup.

Table 14. Interface NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0b	I2C	0b	I2C
	I2C1_SPI_CRC_EN	0b	CRC disabled	0b	CRC disabled
	I2C2_CRC_EN	0b	CRC disabled	0b	CRC disabled
I2C1_ID_REG	I2C1_ID	1001000b	0x48	1001100b	0x4C
I2C2_ID_REG	I2C2_ID	0010010b	0x12	0010011b	0x13

5.12 Multi-Device Settings

These settings detail whether the device is a operating as a master or slave in the system. These settings cannot be changed after device startup.

Table 15. Multi-Device NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
SPMI_CONFIG_1	SPMI_CRC_EN	1b	SPMI CRC check enabled	1b	SPMI CRC check enabled
	SPMI_MASTER_SEL	1b	Master mode	0b	Slave mode
	SPMI_CLK_SEL	10b	5MHz	10b	5MHz
SPMI_CONFIG_2	SPMI_IF_SEL	0b	Debug feature and uses master logic to implement logical slave.	0b	Debug feature and uses master logic to implement logical slave.
	SPMI_RETRY_LIMIT	11b	Three retries in case of error detected	11b	Three retries in case of error detected
	SPMI_SLAVE_ASR_HOLD	0b	TBD	0b	TBD
	SPMI_WD_AUTO_BOOT	1b	SPMI auto boot enabled	1b	SPMI auto boot enabled
	SPMI_EN	1b	SPMI enabled	1b	SPMI enabled
	SPMI_WD_EN	0b	SPMI WD disabled	0b	SPMI WD disabled
SPMI_CONFIG_3	SPMI_WD_BOOT_ INTERVAL	1000b		1000b	
	SPMI_WD_RUNTIME_ INTERVAL	1000b		1000b	
SPMI_CONFIG_4	SPMI_WD_RESPONSE_ TIMEOUT	1000b		1000b	
	SPMI_PFSM_RESPONSE_ TIMEOUT	1111b		1111b	
SPMI_CONFIG_5	SPMI_WD_AUTO_BOOT_ TIMEOUT	00001000b		00001000b	
SPMI_CONFIG_6	SPMI_BOOT_DELAY	00000000b		00000000b	
SPMI_ID	SPMI_SID	0101b		0011b	
	SPMI_MID	01b		01b	
SLAVE_NVM_ID_1	SLAVE1_NVM_ID	00000101b		00000011b	
SLAVE_NVM_ID_2	SLAVE2_NVM_ID	00000011b		00000000b	
SLAVE_NVM_ID_3	SLAVE3_NVM_ID	00000000b		00000000b	
SLAVE_NVM_ID_4	SLAVE4_NVM_ID	00000000b		00000000b	
SLAVE_NVM_ID_5	SLAVE5_NVM_ID	00000000b		00000000b	
SLAVE_NVM_ID_6	SLAVE6_NVM_ID	00000000b		00000000b	

5.13 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though I^2C after startup

Table 16. Watchdog NVM Settings

Register Name	Field Name	PTPS659413F0		PTPS659411F0	
		Value	Description	Value	Description
WD_THR_CFG	WD_EN	1b	watchdog enabled. MCU can set ENABLE_DRV bit to 1 if:	0b	watchdog disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt status bits are cleared

6 Pre-Configurable Finite State Machine (PFSM) Settings

This section describes the default PFSM settings of the TPS659413-Q1 and TPS659411-Q1 devices. These settings cannot be changed after device startup.

6.1 Configured States

In this PDN, the following four power states are configured into the PMIC devices:

- Standby
- Active
- MCU Only
- Suspend-to-RAM (PMIC Deep Sleep Mode)

In Figure 3, the configured power states are described, along with the transition conditions required to move between configured states. Additionally, the transitions to hardware states, such as SAFE RECOVERY are described.

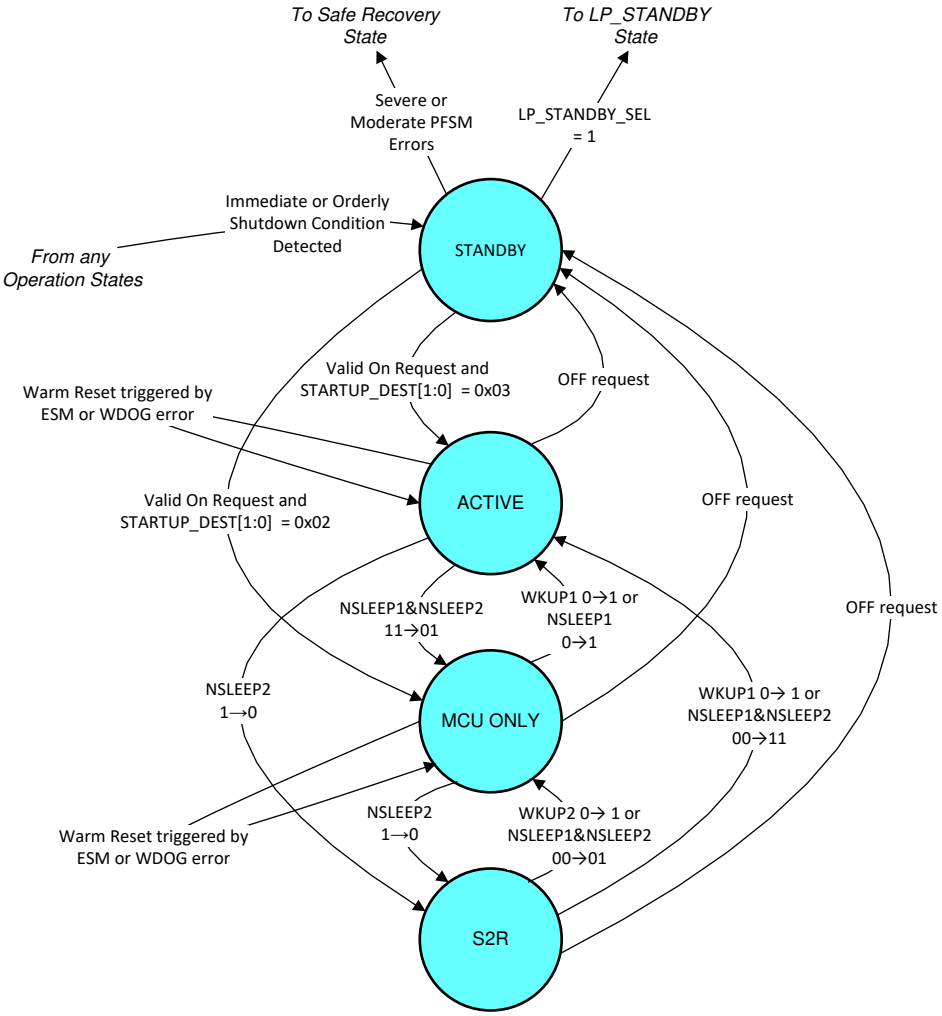

Figure 3. Dual TPS6594-Q1 PFSM States and Transitions

The definition for each power state is described below:

STANDBY— The PMICs are powered by a valid supply on the system power rail (VCCA > VCCA_UV) and waiting for a start-up event or condition. All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The processor is in the Off State, no voltage domains are energized.

ACTIVE— The PMICs are powered by a valid supply and have received a start-up event. The PMICs have full capacity to supply the processor and other platform modules. The processor has completed a recommended power up sequence with all voltage domains energized in both MCU & Main processor sections. MCU can now set the ENABLE_DRV bit high.

MCU ONLY— The PMICs are powered by a valid supply. Only the power resources assigned to the processor's MCU rails are on or in a low power mode (LPM) depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit can be set high by the MCU, or remains unchanged in this state.

Suspend-to-RAM (S2R)— The PMICs are powered by a valid supply. Only the power resources assigned to the PMIC's DEEP_SLEEP group are on or in LPM depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit is cleared by the device in this state. Only 3 SoC voltage domains (vdds_ddr_bias, vdds_ddr, and vdds_ddr_c) remain energized while all other domains are Off to minimize total system power.

6.2 State Transitions

As shown in Figure 3, there are various triggers that can enable a state transition between configured states and hardware states. Table 17 describes each trigger and its associated state transition from highest priority to lowest priority.

Table 17. State Transition Triggers

Trigger	PFSM Current State	PFSM Destination State	Power Sequence Executed
Immediate Shutdown	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	SAFE	TO_SAFE_SEVERE
MCU Power Error	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	SAFE	
Orderly Shutdown	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	SAFE	TO_SAFE_MODERATE
OFF Request	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	STANDBY	TO_STANDBY
WDOG Error	ACTIVE	ACTIVE	WARM_RESET
ESM MCU Error	ACTIVE	ACTIVE	
ESM SOC Error	ACTIVE	ACTIVE	No sequence, nRSTOUT_SOC signal is toggled to reset the SOC
WDOG Error	MCU ONLY	MCU ONLY	MCU_WARM_RESET
ESM MCU Error	MCU ONLY	MCU ONLY	
SOC Power Error	ACTIVE	MCU ONLY	TO_MCU
TPS659411-Q1 GPIO_2 goes low	ACTIVE	ACTIVE	No sequence, the TPS659411-Q1 LDO1 voltage is set to 1.8V
TPS659411-Q1 GPIO_2 goes high	ACTIVE	ACTIVE	No sequence, the TPS659411-Q1 LDO1 voltage is set to 3.3V
ON Request	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	ACTIVE	TO_ACTIVE
WKUP1 goes high	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	ACTIVE	
NSLEEP1 and NSLEEP2 are high(1)	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	ACTIVE	

(1) NSLEEP1 and NSLEEP2 can be accessed through GPIO pin or through a register bit. If either the register bit or the GPIO pin is pulled high, the NSLEEPx value will read as a "high" logic level.

Table 17. State Transition Triggers (continued)

Trigger	PFSM Current State	PFSM Destination State	Power Sequence Executed
MCU ON Request	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	MCU ONLY	TO_MCU
WKUP2 goes high	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	MCU ONLY	
NSLEEP1 goes low and NSLEEP2 goes high(1)	ACTIVE, MCU ONLY, Suspend-to-RAM (S2R)	MCU ONLY	
NSLEEP1 and NSLEEP2 go low(1)	ACTIVE, MCU ONLY	Suspend-to-RAM (S2R)	TO_S2R
NSLEEP1 goes high and NSLEEP2 goes low(1)	ACTIVE, MCU ONLY	Suspend-to-RAM (S2R)	
I2C_0 bit goes high	STANDBY, ACTIVE, MCU ONLY	STANDBY	TO_STANDBY
I2C_1 bit goes high	ACTIVE, MCU ONLY	no state change	No sequence, RUNTIME BIST executes while remaining in the same state

6.3 Power Sequences

6.3.1 TO_SAFE_SEVERE

The immediate shutdown and MCU error events both cause the PMICs to shut down all rails without delay. However, the immediate shutdown will disable the clocks and switching of the BUCKs first and rely on the pulldown resistors of the BUCKs and LDOs to discharge the rails. This is to prevent any damage of the PMICs in case of over voltage on VCCA or thermal shutdown. The MCU error will keep the BUCKs switching until they are disabled. The sequence for these triggers is shown in Figure 4.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
nRSTOUT_SOC	TPS659413-Q1		0 us	PORz
nRSTOUT	TPS659413-Q1		0 us	MCU_PORz
GPIO3	TPS659411-Q1		0 us	EN 0.6V LPDDR4x
BUCK4	TPS659413-Q1		0 us	VDDS_DDR_x
BUCK5	TPS659411-Q1		0 us	VDDAR_CPU, VDDAR_CORE
LDO3	TPS659413-Q1		0 ms	VDDA_0P8_PLLs/DLLs
BUCK1_2_3_4	TPS659411-Q1		0 us	VDD_CORE, VDDA_0P8_PHYs
BUCK1_2	TPS659413-Q1		0 us	VDD_CPU
BUCK3	TPS659413-Q1		0 us	VDD_MCU, VDDAR_MCU
LDO4	TPS659411-Q1		0 us	VDDA_1P8_PLLs
LDO3	TPS659411-Q1		0 us	VDDS_MMC0, EFUSE
BUCK5	TPS659413-Q1		0 us	VDDA_1P8_PHYs
LDO2	TPS659413-Q1		0 us	VDDSHVx_MCU (1.8V)
LDO4	TPS659413-Q1		0 us	VDDA_x
LDO1	TPS659413-Q1		0 us	LPDDR4 1.8V
LDO1	TPS659411-Q1		0 us	VDDSHV5
LDO2	TPS659411-Q1		0 us	VDDA_3P3_USB
GPIO11	TPS659411-Q1		0 us	EN_MAIN_IO
GPIO3	TPS659413-Q1		0 us	EN_MCU_IO

Figure 4. TO_SAFE_SEVERE Sequence

6.3.2 TO_SAFE_MODERATE and TO_STANDBY

If a moderate error occurs, an orderly shutdown trigger will be generated. This will shutdown the PMICs using the processor's recommended power down sequence and then transition to SAFE state to allow the devices to restart and check if the error is still present.

If an OFF request occurs, such as the ENABLE pin of the TPS659413-Q1 device being pulled low, the same power down sequence will occur, except that the PMICs will remain in STANDBY state at the end, rather than going into SAFE state. The power sequence for both of these events is shown in Figure 5.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
nRSTOUT_SOC	TPS659413-Q1		0 us	PORz
nRSTOUT	TPS659413-Q1		0 us	MCU_PORz
GPIO3	TPS659411-Q1		0 us	EN 0.6V LPDDR4x
BUCK4	TPS659413-Q1		500 us	VDDS_DDR_x
BUCK5	TPS659411-Q1		500 us	VDDAR_CPU, VDDAR_CORE
LDO3	TPS659413-Q1		2.5 ms	VDDA_0P8_PLLs/DLLs
BUCK1_2_3_4	TPS659411-Q1		2500 us	VDD_CORE, VDDA_0P8_PHYs
BUCK1_2	TPS659413-Q1		2500 us	VDD_CPU
BUCK3	TPS659413-Q1		2500 us	VDD_MCU, VDDAR_MCU
LDO4	TPS659411-Q1		3000 us	VDDA_1P8_PLLs
LDO3	TPS659411-Q1		3000 us	VDDS_MMC0, EFUSE
BUCK5	TPS659413-Q1		3000 us	VDDA_1P8_PHYs
LDO2	TPS659413-Q1		3000 us	VDDSHVx_MCU (1.8V)
LDO4	TPS659413-Q1		3000 us	VDDA_x
LDO1	TPS659413-Q1		3000 us	LPDDR4 1.8V
LDO1	TPS659411-Q1		3500 us	VDDSHV5
LDO2	TPS659411-Q1		3500 us	VDDA_3P3_USB
GPIO11	TPS659411-Q1		3500 us	EN_MAIN_IO
GPIO3	TPS659413-Q1		3500 us	EN_MCU_IO

Figure 5. TO_SAFE_MODERATE and TO_STANDBY Sequence

6.3.3 WARM_RESET

In the event of a warm reset, the nRSTOUT and nRSTOUT_SOC signals will be driven low and the recovery count will increment. Then, all BUCKs and LDOs will be reset to their default voltages. If no errors are present, the nRSTOUT and nRSTOUT_SOC signals will return to a high value and the PMICs will remain in ACTIVE state. Note that the GPIOs do not reset during the warm reset event. The sequence is shown in Figure 6.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
nRSTOUT_SOC	TPS659413-Q1		0 us	PORz
nRSTOUT	TPS659413-Q1		0 us	MCU_PORz
LDO2	TPS659411-Q1		0 us	VDDA_3P3_USB
LDO1	TPS659411-Q1		0 us	VDDSHV5
LDO1	TPS659413-Q1		0 us	LPDDR4 1.8V
LDO4	TPS659413-Q1		0 us	VDDA_x
LDO2	TPS659413-Q1		0 us	VDDSHVx_MCU (1.8V)
BUCK5	TPS659413-Q1		0 us	VDDA_1P8_PHYs
LDO3	TPS659411-Q1		0 us	VDDS_MMC0, EFUSE
LDO4	TPS659411-Q1		0 us	VDDA_1P8_PLLs
BUCK3	TPS659413-Q1		0 us	VDD_MCU, VDDAR_MCU
BUCK1_2	TPS659413-Q1		0 us	VDD_CPU
BUCK1_2_3_4	TPS659411-Q1		0 us	VDD_CORE, VDDA_0P8_PHYs
LDO3	TPS659413-Q1		0 us	VDDA_0P8_PLLs/DLLs
BUCK5	TPS659411-Q1		0 us	VDDAR_CPU, VDDAR_CORE
BUCK4	TPS659413-Q1		0 us	VDDS_DDR_x
nRSTOUT	TPS659413-Q1		300 us	MCU_PORz
nRSTOUT_SOC	TPS659413-Q1		300 us	PORz

Figure 6. WARM_RESET Sequence

6.3.4 MCU_WARM_RESET

In the event of an MCU warm reset, the nRSTOUT signal will be driven low and the recovery count will increment. Then, all the BUCKs and LDOs that are active in MCU state will be reset to their default voltages. if no errors are present, the nRSTOUT signal will return to a high logic value and the PMICs will remain in MCU state. Note that the GPIOs do not reset during the MCU warm reset event. The sequence is shown in Figure 7.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
nRSTOUT_SOC	TPS659413-Q1		0 us	PORz
nRSTOUT	TPS659413-Q1		0 us	MCU_PORz
LDO2	TPS659411-Q1		0 us	VDDA_3P3_USB
LDO1	TPS659411-Q1		0 us	VDDSHV5
LDO1	TPS659413-Q1		0 us	LPDDR4 1.8V
LDO4	TPS659413-Q1		0 us	VDDA_x
LDO2	TPS659413-Q1		0 us	VDDSHVx_MCU (1.8V)
BUCK5	TPS659413-Q1		0 us	VDDA_1P8_PHYs
LDO3	TPS659411-Q1		0 us	VDDS_MMC0, EFUSE
LDO4	TPS659411-Q1		0 us	VDDA_1P8_PLLs
BUCK3	TPS659413-Q1		0 us	VDD_MCU, VDDAR_MCU
BUCK1_2	TPS659413-Q1		0 us	VDD_CPU
BUCK1_2_3_4	TPS659411-Q1		0 us	VDD_CORE, VDDA_0P8_PHYs
LDO3	TPS659413-Q1		0 us	VDDA_0P8_PLLs/DLLs
BUCK5	TPS659411-Q1		0 us	VDDAR_CPU, VDDAR_CORE
BUCK4	TPS659413-Q1		0 us	VDDS_DDR_x
nRSTOUT	TPS659413-Q1		300 us	MCU_PORz
nRSTOUT_SOC	TPS659413-Q1		300 us	PORz

Figure 7. MCU_WARM_RESET Sequence

6.3.5 TO_MCU

Any event that triggers this sequence will allow all rails not powering the MCU domain of the processor to shutdown. It will then enable the MCU rails, in the event that they are not already active (such as the STANDBY to MCU case). There are two cases for this sequence, based off the value stored in the I2C_7 register bit of TPS659413-Q1. If the bit is low, the SRAM will be disabled. If the I2C_7 bit is high, there will be no change to the SRAM and external software will need to disable it if needed. The power sequences to transition to MCU state is shown in Figure 8.

CAUTION

When moving from ACTIVE to MCU, the power down sequence does not follow the recommendation in the DRA829 and TDA4VM datasheet. The power down sequence will be updated accordingly in the next NVM revision (NVM_REV = 0x08) orderable part number.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
GPIO3	TPS659411-Q1		0 us	EN 0.6V LPDDR4x
BUCK4	TPS659413-Q1		500 us	VDDS_DDR_x
BUCK5	TPS659411-Q1		500 us	VDDAR_CPU, VDDAR_CORE
BUCK1_2_3_4	TPS659411-Q1		2500 us	VDD_CORE, VDDA_0P8_PHYs
LDO3	TPS659413-Q1		3000 us	VDDA_0P8_PLLs/DLLs
BUCK1_2	TPS659413-Q1		3000 us	VDD_CPU
LDO4	TPS659411-Q1		3000 us	VDDA_1P8_PLLs
LDO3	TPS659411-Q1		3000 us	VDDS_MMC0, EFUSE
BUCK5	TPS659413-Q1		3500 us	VDDA_1P8_PHYs
LDO1	TPS659411-Q1		3500 us	VDDSHV5
LDO2	TPS659411-Q1		3500 us	VDDA_3P3_USB
GPIO11	TPS659411-Q1		3500 us	EN_MAIN_IO
LDO1	TPS659413-Q1		6 ms	LPDDR4 1.8V
GPIO3	TPS659413-Q1		6000 us	EN_MCU_IO
LDO4	TPS659413-Q1		7.7 ms	VDDA_x
LDO2	TPS659413-Q1		7700 us	VDDSHVx_MCU (1.8V)
BUCK3	TPS659413-Q1		8.7 ms	VDD_MCU, VDDAR_MCU
nRSTOUT	TPS659413-Q1		17.7 ms	MCU_PORz

Figure 8. TO_MCU Sequence with I2C_7=0

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
GPIO3	TPS659411-Q1		0 us	EN 0.6V LPDDR4x
BUCK5	TPS659411-Q1		0 us	VDDAR_CPU, VDDAR_CORE
BUCK1_2_3_4	TPS659411-Q1		2000 us	VDD_CORE, VDDA_0P8_PHYs
LDO3	TPS659413-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2	TPS659413-Q1		2500 us	VDD_CPU
LDO4	TPS659411-Q1		2500 us	VDDA_1P8_PLLs
LDO3	TPS659411-Q1		2500 us	VDDS_MMC0, EFUSE
BUCK5	TPS659413-Q1		3000 us	VDDA_1P8_PHYs
LDO1	TPS659411-Q1		3000 us	VDDSHV5
LDO2	TPS659411-Q1		3000 us	VDDA_3P3_USB
GPIO11	TPS659411-Q1		3000 us	EN_MAIN_IO
GPIO3	TPS659413-Q1		3000 us	EN_MCU_IO
LDO4	TPS659413-Q1		4.7 ms	VDDA_x
LDO2	TPS659413-Q1		4700 us	VDDSHVx_MCU (1.8V)
BUCK3	TPS659413-Q1		5.7 ms	VDD_MCU, VDDAR_MCU
nRSTOUT	TPS659413-Q1		14.7 ms	MCU_PORz

Figure 9. TO_MCU Sequence with I2C_7=1

6.3.6 TO_ACTIVE

When a trigger causes the TO_ACTIVE sequence to execute, all rails of the PMICs will power up in the processor's recommended power up sequence as shown in Figure 10.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
GPIO3	TPS659413-Q1		0 us	EN_MCU_IO
GPIO11	TPS659411-Q1		0 us	EN_MAIN_IO
LDO2	TPS659411-Q1		0 us	VDDA_3P3_USB
LDO1	TPS659411-Q1		0 us	VDDSHV5
LDO1	TPS659413-Q1		1700 us	LPDDR4 1.8V
LDO4	TPS659413-Q1		1700 us	VDDA_x
LDO2	TPS659413-Q1		1700 us	VDDSHVx_MCU (1.8V)
BUCK5	TPS659413-Q1		1700 us	VDDA_1P8_PHYs
LDO3	TPS659411-Q1		1700 us	VDDS_MMC0, EFUSE
LDO4	TPS659411-Q1		1700 us	VDDA_1P8_PLLs
BUCK3	TPS659413-Q1		2700 us	VDD_MCU, VDDAR_MCU
BUCK1_2	TPS659413-Q1		2700 us	VDD_CPU
BUCK1_2_3_4	TPS659411-Q1		2700 us	VDD_CORE, VDDA_0P8_PHYs
LDO3	TPS659413-Q1		2700 us	VDDA_0P8_PLLs/DLLs
BUCK5	TPS659411-Q1		3700 us	VDDAR_CPU, VDDAR_CORE
BUCK4	TPS659413-Q1		3700 us	VDDS_DDR_x
GPIO3	TPS659411-Q1		4200 us	EN 0.6V LPDDR4x
nRSTOUT	TPS659413-Q1		12700 us	MCU_PORz
nRSTOUT_SOC	TPS659413-Q1		12700 us	PORz

Figure 10. TO_ACTIVE Sequence

6.3.7 TO_S2R

Any event that triggers this sequence will disable all power rails and GPIOs that are not supplying the DDR to enter suspend-to-RAM state (S2R). The sequence is shown in Figure 11.

SEQUENCE NAME	DEVICE	DELAY DIAGRAM	TOTAL DELAY	RAIL NAME
nRSTOUT_SOC	TPS659413-Q1		0 us	PORz
nRSTOUT	TPS659413-Q1		0 us	MCU_PORz
LDO3	TPS659413-Q1		0 ms	VDDA_0P8_PLLs/DLLs
BUCK5	TPS659411-Q1		500 us	VDDAR_CPU, VDDAR_CORE
BUCK1_2	TPS659413-Q1		2 ms	VDD_CPU
BUCK3	TPS659413-Q1		2000 us	VDD_MCU, VDDAR_MCU
BUCK5	TPS659413-Q1		2500 us	VDDA_1P8_PHYs
LDO2	TPS659413-Q1		2500 us	VDDSHVx_MCU (1.8V)
BUCK1_2_3_4	TPS659411-Q1		2500 us	VDD_CORE, VDDA_0P8_PHYs
LDO4	TPS659413-Q1		2500 us	VDDA_x
LDO4	TPS659411-Q1		2500 us	VDDA_1P8_PLLs
LDO3	TPS659411-Q1		2500 us	VDDS_MMC0, EFUSE
GPIO3	TPS659413-Q1		3000 us	EN_MCU_IO
LDO1	TPS659411-Q1		3500 us	VDDSHV5
LDO2	TPS659411-Q1		3500 us	VDDA_3P3_USB
GPIO11	TPS659411-Q1		3500 us	EN_MAIN_IO

Figure 11. TO_S2R Sequence

7 Additional Resources

For additional information regarding the PMIC or processor devices, use Table 18 for helpful resources:

Table 18. Additional Documents

Title	Document Type	Devices	Link
TPS6594x-Q1 Power Management IC (PMIC) With 4-Phase 14-A Buck for Processors	Datasheet	TPS6594x-Q1	Request through mySecure
Jacinto™ DRA829 Automotive Processors Silicon Revision 1.0	Datasheet	DRA829V	Request through mySecure
TDA4VM Jacinto™ Automotive Processors for ADAS and Autonomous Vehicles Silicon Revision 1.0	Datasheet	TDA4VM	Request through mySecure
TPS6594x-Q1 Safety Manual	Safety Manual	TPS6594x-Q1	Request through mySecure
DRA829/TDA4VM Safety Manual Jacinto™ 7 Processors	Safety Manual	DRA829V, TDA4VM	Request through mySecure
TPS6594x-Q1 Schematic Checklist	Application Note	TPS6594x-Q1	Request through mySecure

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265