TI Designs

EMC-Compliant Digitally Isolated 2-Channel, Wide DC Binary Input Module

TI Designs

This TI Design showcases a cost-optimized architecture that improves measurement resolution and accuracy of DC binary input module. A microcontroller unit (MCU) with a 10-bit SAR ADC is shared between two inputs (group isolation) to minimize the cost per channel and measure DC input within ±3% accuracy. A digital isolator (basic or reinforced) is used to communicate the ADC code or root-mean-square value or status of the DC input to the host processor. The design is tested for ESD and surge as per IEC61000-4 4 Level 4.

Design Resources

TIDA-00420	Tool Folder Containing Design Files
MSP430G2332IPW20	Product Folder
ISO1541D	Product Folder
SN6501DBV	Product Folder
ISO7320C	Product Folder
ISO7820	Product Folder

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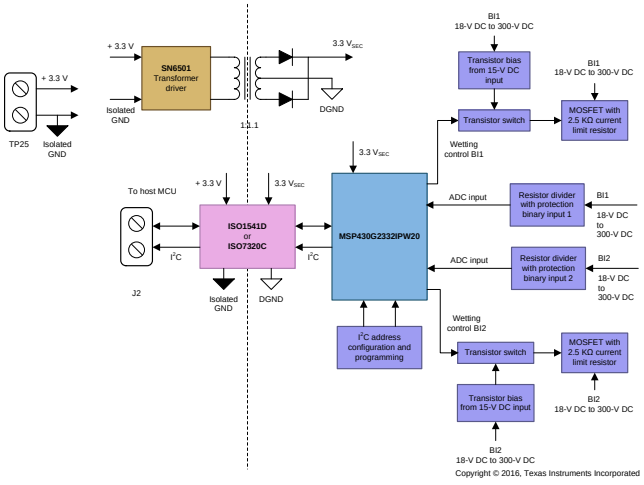
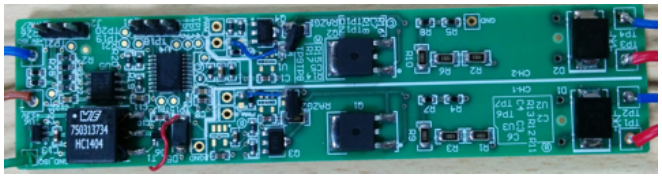


Design Features

- Accurate Sensing of Input Voltage Over Wide Temperature Range
  - Accuracy < ±3% of Measured Value ±1 V (Programming Resolution or Step Size)
- MCU-Based 2-Channel DC Binary Input Voltage Sensing
- Tested With Isolator Rated for Basic and Reinforced Isolation
- Independent Wetting Current Control for Both Inputs
- Can be Extended to Measure Four or Six Binary Inputs
- Wide DC Input Measurement: 18 to 300-V DC
- Can be Interfaced to the Host CPU Using I^{2}C Interface or Digital Output Type of Isolators
- ≥2.5-KΩ Impedance for Wetting and >300-KΩ Impedance for Binary Input
- Less Than 1-mA Consumption at 300-V DC Input
- Measurement Resolution Better Than 1 V
- PCB Width ≤ 1 Inch

Featured Applications

- Multifunction Protection Relays
- Remote Terminal Unit
- Bay Controller
- Remote I/O
- Power Quality Analyzer
- Merging Unit
- Circuit Breaker Digital Input Module
- FTU/DTU/FRTU



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1 System Description

1.1 Introduction to IED and Subsystems in Grid Applications

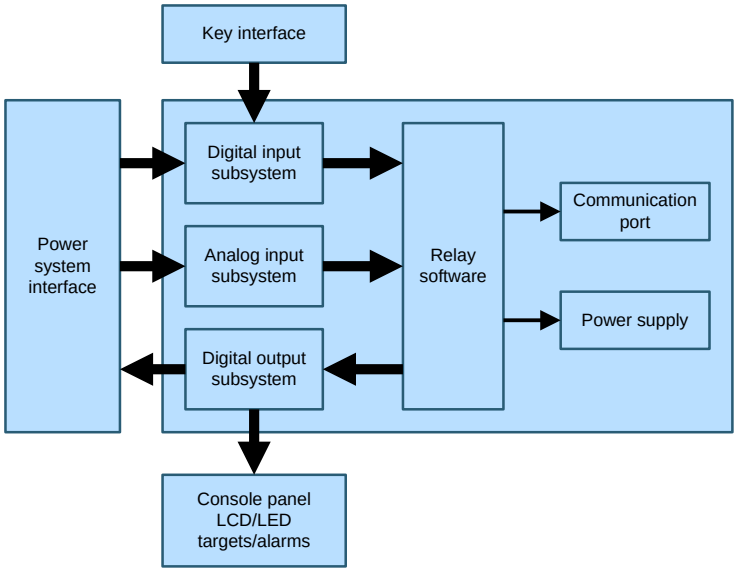

Figure 1. Generic Block Diagram of a Protection Relay

The protection relay, intelligent electronic device (IED), or substation controllers used in grid applications have the following generic subsystems. The subsystems are based on the functionality and are as follows:

- CPU or DSP module
  - This module handles all protection functions and logic. Additionally, the HMI and communication functions are also handled by this module.
- Power supply
  - Nominal auxiliary voltage: 24-V DC, 48 to 60-V DC, 110 to 125-V DC, 220-V DC, and 230-V AC, 50 or 60 Hz, ± 20%, and 40-W max admissible consumption
  - Stored energy for up to 50 ms power supply interruption
  - Dual source power supply (optional)
- AC measurement inputs
  - Nominal frequency (FNOM): 50 or 60 Hz
  - Operating range: 45 to 66 Hz
  - Accuracy: 0.2% F_S at FNOM
- CT measurements inputs
  - Nominal current: 1 or 5 A (IN)
  - Nominal consumption per phase: < 0.15 A at IN
  - Load rating: 20 A in continuous; 30 A for 3 s; 100 A for 1 s
- VT measurements inputs
  - Nominal voltage: 57.7 to 500 V
  - Nominal consumption per phase: < 0.1 VA at 130 V
  - Maximum measurable voltage: 577 V_{RMS}

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- DC analog input range (independently configurable):
  - ±1.25, ±2.5, ±5, and ±10 V
  - ±1, ±5, ±10, and ±20 mA
  - 0 to 1, 0 to 5, 0 to 10, 0 to 20, and 4 to 20 mA
- DC analog output range (independently configurable):
  - ±5, ±10, ±20 mA, and 4 to 20 mA
- Digital inputs
  - Nominal voltage: 24-V DC, 48 to 60-V DC, 110 to 125-V DC/AC and 220-V DC/AC, ±20% or multi-voltage (24 to 250-V DC/AC)
  - Power consumption per input: 2 to 6 mA, maximum power dissipation is 0.45 W ±20% per input or short peak-current (> 25 mA)
  - Groups of 4, 8, 12, 16, or 32
- Digital output relays
  - Continuous current: 5 A
  - Short-duration current: 30 A for 500 ms; 100 A for 30 ms
  - Breaking capacity: DC: 50 W resistive, 15 W inductive (L/R = 20 ms); AC: 1250 VA (cos PF = 0,7)
- Control output relays
  - Continuous current: 5 A
  - Short-duration current: 30 A for 4 s; 250 A for 30 ms
  - Breaking capacity (Double pole contacts wired in serial): DC: 100 W resistive, 30 W inductive (L/R = 40 ms); AC: 2000 VA (cos F = 0.7)
- Time synchronization
  - by an IRIG–B GPS clock (through the IRIG-B input)
  - by an Ethernet SNTP server
  - by a time telegram message issued by remote Scada (DNP3.0, IEC 60870-5-101 or IEC 60870-5-104)
- Communication capabilities
  - Ethernet communication
    - 10/100BASE-TX, auto-crossing or 100BASE-FX
    - Protocols include UCA2 or IEC 61850, IEC 60870-5-104 (multi-client) or DNP3.0 IP
    - Embedded Ethernet switch module with up to six ports (permitting a compact connection of various devices or I/O extensions)
  - Serial communication
    - Up to two SCADA or four IED links per device
    - SCADA protocol can be switched between DNP3.0, IEC 60870-5-101 and MODBUS
    - IED Protocol can be switched between DNP3.0, IEC 60870-5-103, MODBUS and IEC 60870-5-101
    - Transmission rate is configurable up to 38.4 kbps

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1.2 Binary Inputs or Digital Inputs

The inputs to the protection relay or substation controllers are called under different names:

- Binary input
- Digital input
- Control input
- Indication input

The names are based on the function performed. These inputs will be referred as binary inputs in this design guide. Binary inputs have wide applications. The binary input module specifications differ with OEMs. The binary inputs are designed as modules and based on application one or more modules are used. Below is the summary of some of the Applications, functionalities, and specifications. These inputs have galvanic isolation from internal circuits, generally opto-coupler are used for isolation. Number of binary inputs per module can vary as 4, 8, 16, or 32. *The binary inputs are organized in groups (depending upon application) with a common wire. In some of the applications the inputs are channel isolated.*

1.2.1 Binary Input Applications

Some of the grip applications use binary inputs for the following functionalities:

- Substation battery monitoring
- Bay or substation interlocking
- Breaker status indications
- General interrogations
- LED test
- Diagnostics (self-test)
- Fault indication (alarm)
- Configuration change (operated with new settings to perform different functionality)

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1.2.2 Specifications

Key Specification

- Input voltage range
- Threshold for guarantee operation
- Threshold for uncertain operation
- Response or reset time (software provides de-bounce time)
- Power consumption, energized

General Specification

- Inputs are jumper selectable for low range (nominal system voltages of up to 100 V) or high range (from 100 to 300 V)
- Tolerance: ±10%
- Common input voltage ranges:
  - 24-V DC
  - 48-V DC
  - 110-V DC
  - 230-V DC
- Contacts per common return: Four or more
- Recognition (processing of the inputs) time: ≥ 3 ms
- Inputs protected against continuous overload up to 300-V DC
- All I/O terminals protected with internal transient limiting devices
- Input de-bounce time is selectable; de-bounce time: 0.0 to 16.0 ms in steps of 0.5
- Continuous current draw: < 5 mA
- Auto-burnish impulse current: 20 to 50 mA
- Duration of auto-burnish impulse: 25 to 50 ms

1.2.3 Wetting or Auto Burnishing

The binary inputs sense a change of the state of the external device. When these external devices are located in a harsh industrial environments (either outdoor or indoor), their contacts can be exposed to various types of contamination. Normally, there is a thin film of insulating sulfidation, oxidation, or contaminates on the surface of the contacts, sometimes making it difficult or impossible to detect a change of the state. This film must be removed to establish circuit continuity; an impulse of higher than normal current can accomplish this.

The contact inputs with auto-burnish create a high current impulse when the threshold is reached to burn off this oxidation layer as maintenance to the contacts. Afterwards, the contact input current is reduced to a steady-state current. Contact inputs with auto burnishing allow currents up to 50 mA at the first instance when the change of state was sensed. Then, within 25 to 50 ms, this current is slowly reduced to 5 mA. The 50-mA peak current burns any film on the contacts, allowing for proper sensing of state changes.

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1.2.4 Miscellaneous Features

Filter

Filters prevent the input signal from being detected erroneously. The following types of input filters can be used:

- The hardware input filter is used to suppress contact bounce (1 to 64 ms).
- Change-of-state delay is used to suppress short signal interruptions.
- Chatter blocking is used to suppress huge bursts of indications in case of defective battery or intermediate relays.

Processing

The detected changes of state can be processed further in the following ways:

- Single-point indication: Each incoming or outgoing input signal causes data to be entered in the event buffer and the process image to be updated.
- Transient indication: Each change in the input signal causes the process image to be updated. However, only an incoming input signal causes data to be entered in the event buffer.
- Double-point indication: Two defined states of an operational device (for example, on/off) and two undefined states (for example, intermediate state information) can be represented with two inputs. Each change in the double-point indication causes data to be entered in the event buffer. Each new state of the two inputs is entered in the process image.
- Bit patterns: Several inputs are used to detect freely definable states of an operating device. This information can be transferred to the event buffer by an internal event signal (change in the bit pattern) or an external event signal (impulse through a fixed external input).
- Transformer tap indication: Several inputs are used to detect the states of a transformer tap generator. This information is transferred according to the moving contact. The transformer taps can be entered in variable codes.
- Metered-value acquisition: Signal changes are interpreted as metering pulses and totalized. The metered value is transferred to the event buffer by means of a transfer job.

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1.3 Isolation

Table 1. Key Methods of Isolation

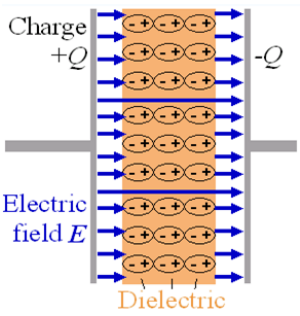
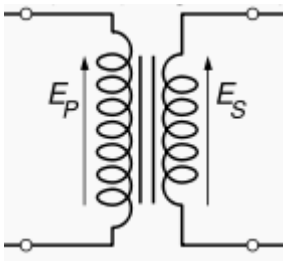
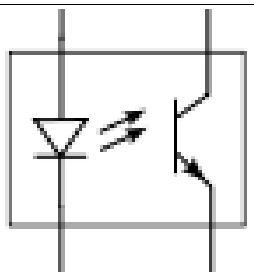
	SiO2: ISO72x; Typical BV is V_{PEAK}/µm • Inorganic • Highly stable (over temperature, moisture, time), high quality • Used extensively and for a long time as dielectric in semiconductor (low defunct rates) • Deposited in a controlled semiconductor process
	Polymide: ADI transformer core; Typical BV is 250 V_{PEAK}/µm • Organic • Retains moisture — affects lifetime especially at high voltages • Used in semiconductor mainly for stress relief and now as isolation barrier
	Epoxy: Opto-couplers; Typical BV is 50 V_{PEAK}/µm • Uses filler materials • Leaky (higher partial discharge) • Applied at packaging as mold compound • Voids and anomalies are common

Table 2. Isolation Solutions Reliability

PARAMETER	OPTO	MAGNETIC	CAPACITIVE
Signaling rate (Mbps)	50	150	150
Propagation delay time (ns)	20	32	12
Pulse width distortion (ns)	2	2	1.5
Channel-to-channel skew (ns)	16	2	1.6
Part-to-part skew (ns)	20	10	2
ESD on all pins (kV)	±2	±2	±4
CM transient immunity (kV/µs)	20	25	25
Temperature (°C)	–45 to 125	–40 to 125	–55 to 125
MTTF @ 125°C, 90% confidence (years)	8	1746	2255
FIT @ 125°C, 90% confidence	14391	65	50
Magnetic immunity @ 1 kHz (Wb/m^2)	—	10^2	10^8
Radiated electromagnetic-field immunity IEC61000-4-3 (80 to 1000 MHz) MIL-STD 461E RS103 (30 to 1000 MHz)	 — —	 Fails Fails	 Compiles Compiles
High-voltage lifetime expectancy (years)	< 5	< 10	> 28

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1.4 EMC — Transient Overvoltage Stress

In industrial applications, lightning strikes, power source fluctuations, inductive switching, and electrostatic discharge (ESD) can cause damage to binary inputs by generating large transient voltages. The following ESD and surge protection specifications are relevant to binary input applications:

- IEC 61000-4-2 ESD protection
- IEC 61000-4-5 Surge protection

The level of protection can be further enhanced when using external clamping devices, such as TVS diodes. TVS diodes are normally used to protect silicon devices, like binary inputs, from transients. The protection is accomplished by clamping the voltage spike to a limit, by the low impedance avalanche breakdown of a PN junction. TVS diodes are ideally open-circuit devices. A TVS diode can be modeled as a large resistance in parallel with some capacitance while working below its breakdown voltage. When a transient is generated and the surge voltage is larger than the breakdown voltage of the TVS, the resistance of the TVS decreases to keep the clamping voltage constant. The TVS clamps the pulse to a level that does not damage the device that it is protecting. The transients are clamped instantaneously (< 1 ns) and the damaging current is diverted away from the protected device.

1.5 TI Isolator Solutions for Binary Input Module

1.5.1 ISO72x Family of High-Speed Digital Isolators

The Texas Instruments ISO72x family of isolators use capacitive coupling. The capacitive coupling solution uses proven and cost-effective manufacturing processes and provides an inherent immunity to magnetic fields.

To provide transfer of steady-state information, the ISO72x uses both a high-signaling rate and low-signaling rate channel to communicate as shown in Figure 2. The high-signaling rate channel is not encoded and it transmits data transitions across the barrier after a single-ended-to-differential conversion. The low-signaling rate channel encodes the data in a pulse-width modulated format and transmits the data across the barrier differentially, ensuring the accurate communication of steady-state conditions (long string of 1s or 0s).

Differential transfer of the single-ended logic signal across the isolation barrier allows low-level signals and small coupling capacitance. This appears as high impedance to common-mode noise and, with the common-mode noise rejection of the receiver, gives excellent transient immunity, the primary concern in capacitive coupling of signals.

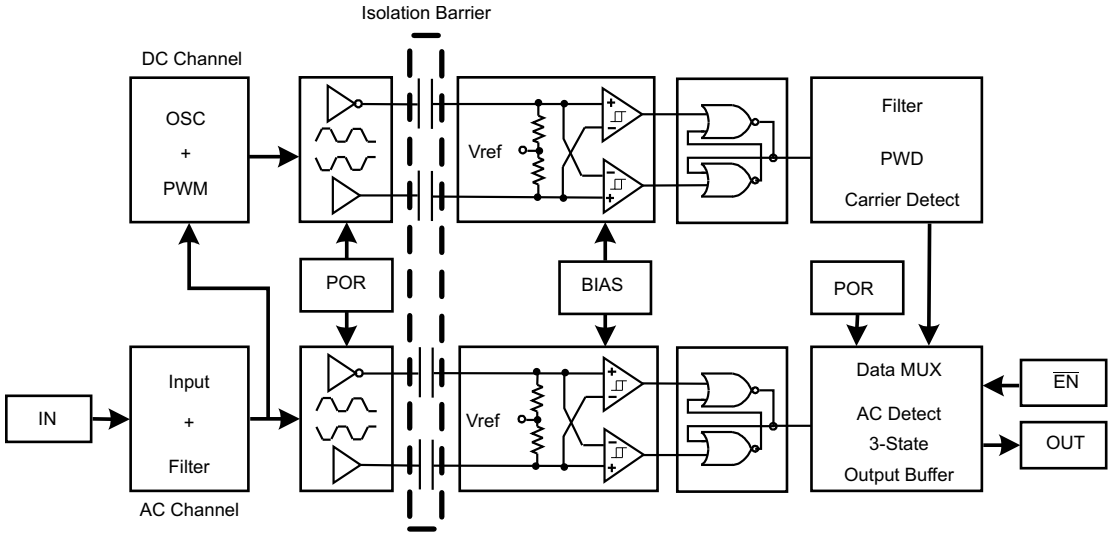

Figure 2. ISO72x Isolator Internal Diagram

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1.5.2 Power Consumption

Beyond the efficiency of the signal transfer across the barrier, the design of the input and output conditioning circuitry has the most to do with power consumption. As shown in Table 3, the opto-couplers use more power than the inductive or capacitive examples.

Table 3. Quiescent Power Supply Current Table

PART	COUPLING TECHNOLOGY	V_{CC1} AND V_{CC2} (V)	I_{CC1} (mA)	I_{CC2} (mA)	POWER (mW)
ISO721	Capacitive	5	1	11	60
		3.3	0.5	6	21.5
ADuM1100	Magnetic	5	0.8	0.06	4.3
		3.3	0.3	0.04	1.2
HCPL-0900	Magnetic	5	0.018	6	30
		3.3	0.01	4	13.2
HCPL-0721	Optical	5 only	10 (1)	9	95
HCPL-0723	Optical	5 only	10 (1)	17.5 (2)	137.5

(1) 10 mA is for the logic-low input state. When the logic input state is high, then the current consumption drops to 3 mA.
(2) 17.5 mA is for the logic-low input state. When the logic input state is high, then the current consumption drops to 16.5 mA.

1.5.3 Reliability

Mean time to failure (MTTF) is a standard measure for reliability of semiconductor devices. For digital isolators, this measure represents the reliability of both the integrated circuit and the isolation mechanism. Table 4 shows the MTTF of an optical, inductive, and capacitive digital isolator. The ISO721 is very reliable when compared to inductive and optical solutions.

Table 4. MTTF Reliability Measurement

PART	COUPLING TECHNOLOGY	AMBIENT TEMPERATURE (°C)	TYPICAL, 60% CONFIDENCE		TYPICAL, 90% CONFIDENCE	
			MTTF (Hr/Fail)	FITs (Fail/10^9 Hr)	MTTF (Hr/Fail)	FITs (Fail/10^9 Hr)
ISO721	Capacitive	125	1,246,889	802	504,408	1983
HCPL-0900	Inductive	125	288,118	3471	114,654	8722
HCPL-0721	Optical	125	174,617	5727	69,487	14.391

1.6 Isolated 2-Channel, Wide DC Binary Input Module TI Design Advantages

Some of the advantage of the DC binary input module is as follows:

- Allows for measurement of wide DC input voltage
- Uses MCU to allow flexibility in terms of input voltage processing and measurement accuracy
- Provides provision for programmable threshold on the host side
- Uses digital isolator to increase reliability
- Uses MCU capabilities to control wetting current
- Costs optimized solution
- Reduces the cost per channel with addition of more channels with common ground

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2 Design Features

The DC binary input module measures the input DC voltage and converts the measured voltage into ADC counts. The ADC counts are communicated to the host and the host converts the ADC count into voltage for further processing.

Table 5. DC Binary Input — Electrical Specifications

SERIAL NUMBER	PARAMETER	DESCRIPTION	COMMENT
1	Number of inputs	2	Both inputs share common ground.
2	Input voltage range	18-V to 264-V DC	Maximum permissible voltage input is ≤ 300-V DC.
3	Input voltage frequency	DC	
4	Measurement resolution	<1 V for input values between 24-V to 230-V DC	Binary module communicates measured voltage as ADC counts using I^2C interface to the host.
5	Input voltage measurement accuracy	±3% of measured value ±1 V (programmable step size)	
6	Voltage input resistance	≥ 300 KΩ	
7	Current drain at voltage input	< 1 mA at 300-V DC	
8	Response time	≥ 3 ms	Measurement averaged over 3 ms.
9	Binary input wetting resistance	≥ 2.5 KΩ	Default wetting is off Binary wetting pulse width is based on nominal voltage (24 V, 110 V, 230 V).
10	Isolator type	• I^2C isolator • Digital isolator (replaces I^2C isolator)	3.3-V isolated voltage is generated internally on the module.
11	Binary input contact type	External wetting type	Tested with DC input.
12	LED indication	N/A	
13	Reference temperature	25°C	
14	Isolation of binary inputs	Group isolated	
14	Electrical isolation level	> 2 kV_{RMS}	
16	Protection against ESD, surge (EMC requirements)	ESD: 2 kV, contact Surge: 2 kV , 42-Ω differential mode	

NOTE: This module must not be used to measure AC input or negative DC input.

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3 Block Diagram

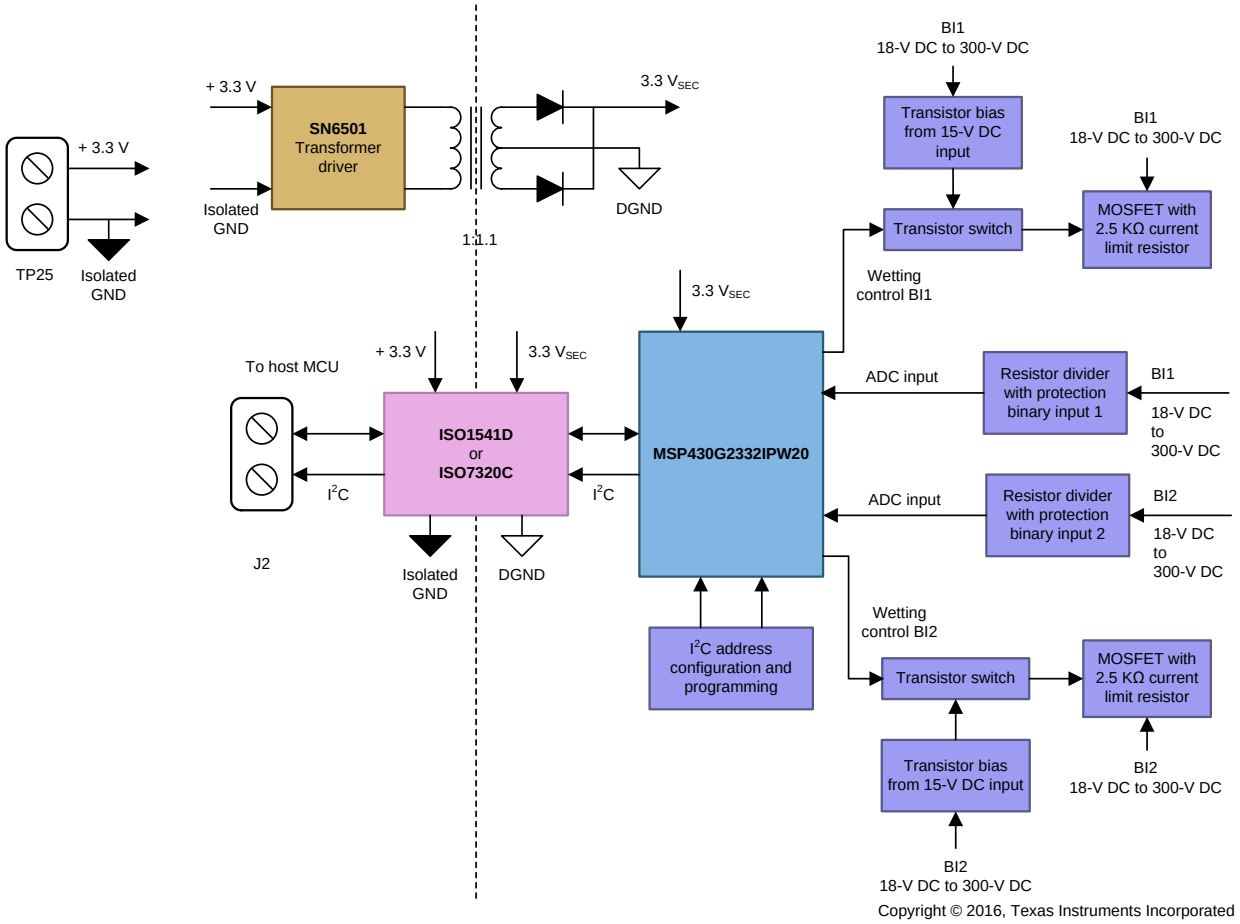

Figure 3. Block Diagram of Wide DC Binary Input Module

3.1 MCU With Internal ADC

The MSP430 family of ultra-low-power microcontrollers has been considered for this TI design. The MCU considered is MSP430G2332IPW20. The MCU has an internal 10-bit ADC.

Other features include:

- Low supply voltage range: 1.8 to 3.6 V
- Ultra-low power consumption
  - Active mode: 220 μA at 1 MHz, 2.2 V
- Internal very-low-power low-frequency (LF) oscillator
- One 16-bit Timer_A with three capture/compare registers

3.2 Digital Isolator

To meet safety requirements, the binary input module is isolated from the host interface. Digital isolators have been considered for isolation. The binary inputs status information is communicated to the host MCU using the following options:

- I^2C isolator: ISO1541D low-power bidirectional I^2C isolators The status information is communicated as ADC counts that can be converted to voltage
- Digital isolator: ISO7220ADR dual-channel digital isolators. The status information is conveyed as above (high) or below (low) a set value

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3.3 Isolated Power Supply

The isolated power for the MCU, digital isolator, and the signal conditioning circuit used for sensing the status of the binary inputs are generated using a Push-Pull Driver for Isolated Power Supplies SN6501DBV. The transformer used for this application is 750313734. The transformer package is selected to have isolation voltage of ≥ 5 kV. Choosing a bigger transformer package facilitates easy migration to reinforced isolators. Zener diode PTZTE253.9B is used for protecting the power supply against overvoltage and ESD. The Isolated power supply operates with a single 3.3-V input. The host interface provides the required power supply for the binary module operation.

3.4 Host Interface

The status of the binary output can be communicated as voltage output (I^2C output) or digital output. The status is communicated to a host MCU. Tiva™ C Series TM4C123G LaunchPad™ Evaluation Board is used as the host MCU.

NOTE: The host MCU (LaunchPad) is not part of the binary module.

3.5 Input Voltage Divider and Protection

- Input protection: TVS SMCJ400CA is used for protecting binary input module against overvoltage and transient inputs. Package selection is critical to ensure the device has low leakage with temperature variation.
- Resistor divider: The DC binary input voltage applied is divided by a resistor divider, which presents a constant resistance to the binary input. Multiple resistors are used to ensure the resistors withstand the maximum input voltage reliably. The output of the resistor divider is measured by the ADC, which is within the ADC measurement range at maximum input. A Zener diode PTZTE255.1B is used to protect the electronic circuit from overvoltage.

3.6 Wetting Current Control

3.6.1 Transistor Drive for MOSFET Gate Driver

A transistor is used to drive the MOSFET that controls the wetting current. The bias voltage of 15 V max for the MOSFET operation is generated from the binary input using a Zener regulator. The bias current for the Zener must be in µA and care should be taken during selection of the Zener. Vz versus Iz characteristics is critical.

3.6.2 Wetting Current Limiting Resistor and MOSFET

Four resistors, 10 KΩ each connected in parallel, are used as current limit for wetting current. A D-PAK MOSFET with a 600-V rating AOD2N60A is used that ensures reliability of the MOSFET. *The short time overload capability of the resistor is being used and care should be taken to not test the wetting current for test > 100 ms (typically 50 ms).*

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4 Circuit Design and Component Selection

4.1 MCU With Internal ADC

The binary input modules are highly cost sensitive and to ensure the overall solution cost is optimal, MCU with internal ADC has been selected. The internal ADC is a 10-bit SAR ADC.

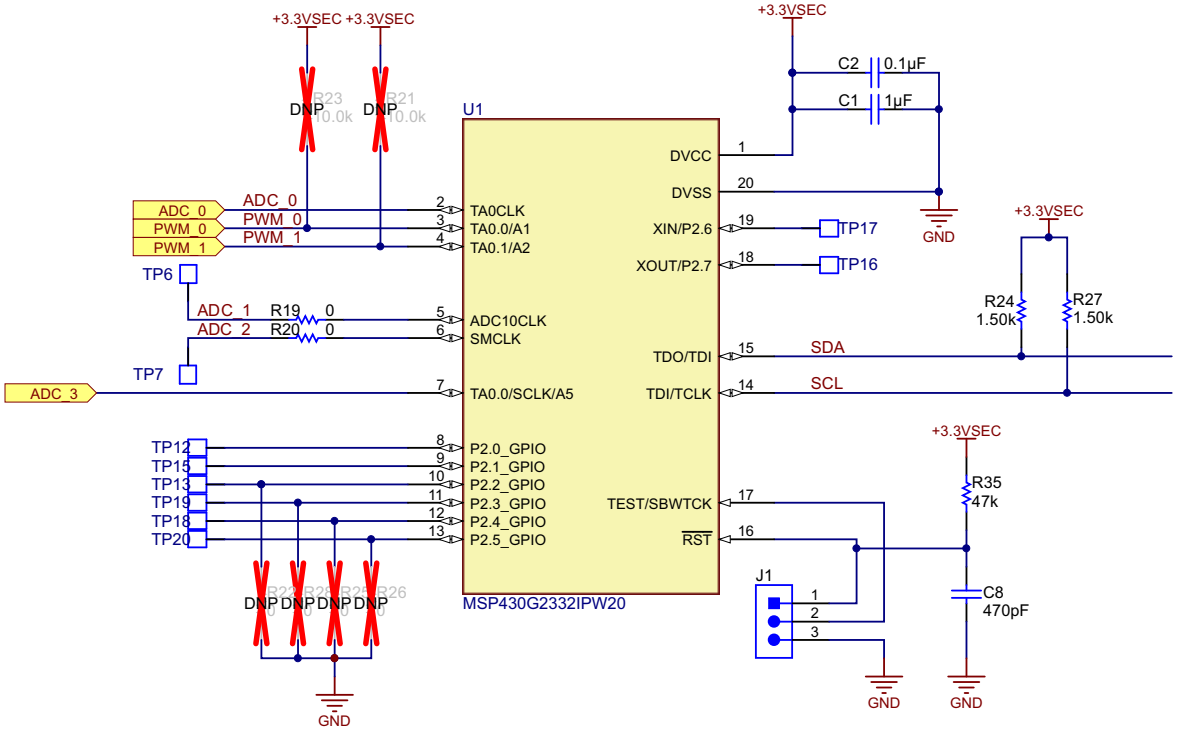

Figure 4. MCU Functionality Configuration

The MCU considered is MSP430G2332IPW20. Texas Instruments MSP430 family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2332IPW20 is a ultra-low-power mixed signal microcontroller with a built-in 16-bit timer. The device has up to 16 I/O capacitive-touch enabled pins and built-in communication capability using the universal serial communication interface. TheMSP430G2332IPW20 has a 10-bit A/D converter.

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4.1.1 Features

- Low supply voltage range: 1.8 to 3.6 V
- Ultra-low power consumption
  - Active mode: 220 μA at 1 MHz, 2.2 V
  - Standby mode: 0.5 μA
  - Off mode (RAM retention): 0.1 μA
- Five power-saving modes
- Ultra-fast wake-up from standby mode in less than 1 μs
- 16-bit RISC architecture, 62.5-ns instruction cycle time
- Basic clock module configurations
  - Internal frequencies up to 16 MHz with four calibrated frequencies
  - Internal very-low-power LF oscillator
  - 32-kHz crystal
  - External digital clock source
- One 16-bit Timer_A with three capture/compare registers
- Universal serial interface (USI) supporting SPI and I^2C
- 10-bit 200-ksps A/D converter with internal reference, sample-and-hold, and autoscan (MSP430G2x32 only)
- Brownout detector
- Serial onboard programming, no external programming voltage needed, programmable code protection by security fuse
- On-chip emulation logic with Spy-Bi-Wire interface
- Package
  - TSSOP: 20-pin

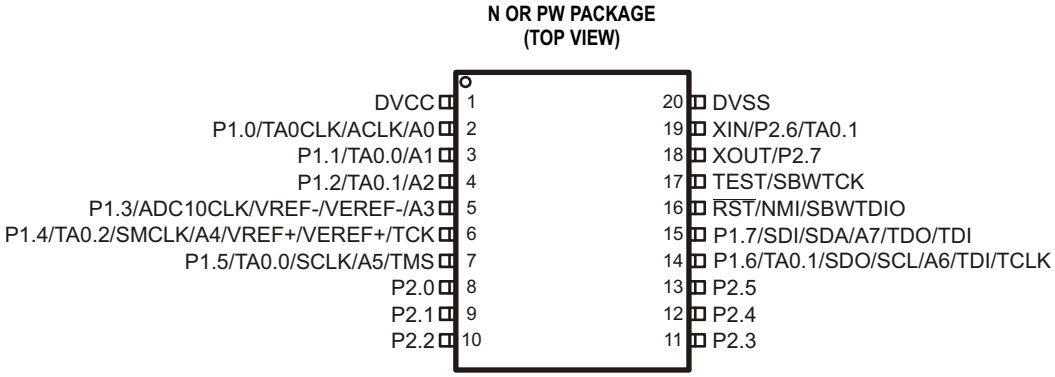

Figure 5. MCU Pinout Description

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4.1.2 MCU Resources

Table 6. MCU RAM and Flash Size

PIN NUMBER	DESCRIPTION	SIZE
1	Flash	4 KB
2	RAM	256 bytes
3	ADC10	8 channels
4	Package and pin count	20-TSSOP

4.1.3 MCU Configuration

Table 7. MCU Pin Configuration for the DC Binary Module

PIN NUMBER	PIN FUNCTION	CONFIGURATION
1	DVCC	3.3 V_{SEC}
2	A0	ADC_0 (Binary input1)
3	TA0.0	PWM_0 (Control of Binary input1 wetting current)
4	TA0.1	PWM_1 (Control of Binary input2 wetting current)
5	A3	ADC_1 (Currently not used — configured as Port)
6	A4	ADC_2 (Currently not used — configured as Port)
7	A5	ADC_3 (Binary input2)
8	P2.0	Not used – configured as output
9	P2.1	Not used – configured as output
10	P2.2	Can be used to set I^2C address — configured as output
11	P2.3	Can be used to set I^2C address — configured as output
12	P2.4	Can be used to set I^2C address — configured as output
13	P2.5	Can be used to set I^2C address — configured as output
14	SCL	I^2C clock
15	SDA	I^2C data
16	/RST	Programming
17	SBWTCK	Programming
18	P2.7	Not used – configured as output
19	P2.6	Not used – configured as output
20	DVSS	GND

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4.1.4 ADC Features

The ADC used is a 10-bit, 8-channel ADC with Autoscan and DMA capabilities.

Table 8. 10-Bit ADC, Timing Parameters (MSP430G2x32 Only)(1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 × ADC10DIV × $1/f_{ADC10CLK}$			
$t_{ADC10ON}$	Turn-on setting time of the ADC						(2)100	ns

(1) Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

(2) The condition is that the error in a conversion started after tADC10ON is les than ±0.5 LSB. The reference and input signal are already settled.

Table 9. 10-Bit ADC, Linearity Parameters (MSP430G2x32 Only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

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4.2 Digital Isolator

The binary input module is isolated from the host MCU. TI digital isolators are used to provide the required isolation. The isolator could be digital output type or I^2C interface type.

An I^2C interface type isolator provides flexibility in terms of functionality. A digital output type is recommended when cost is critical and the binary inputs are a fixed input voltage.

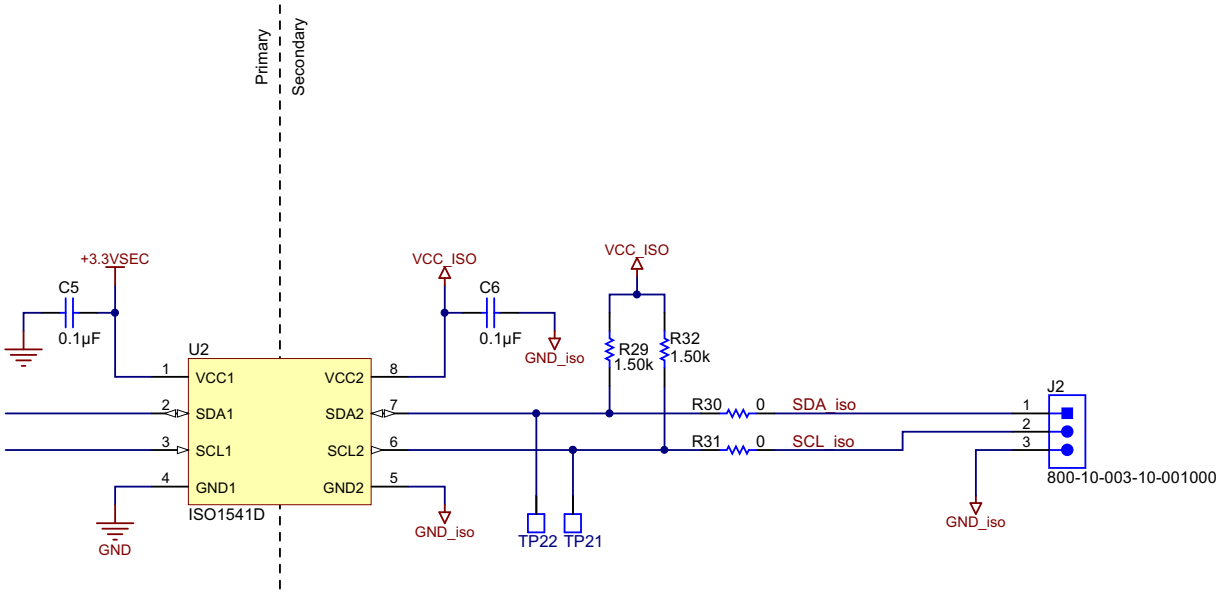

Figure 6. Digital Isolator for I^2C Interface

4.2.1 I^2C Isolator: ISO1541D Low-Power Bidirectional I^2C Isolators

The ISO1541 are low-power, bidirectional isolators that are compatible with I^2C interfaces. These devices have their logic input and output buffers separated by TI's capacitive isolation technology using a SiO2 barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to opto-couplers. The ISO1541 enable a complete isolated I^2C interface to be implemented within a small form factor. The ISO1541 is useful in applications that have a single master while the ISO1540 is ideally fit for multi-master applications.

Isolated bidirectional communications is accomplished within these devices by offsetting the Side 1 Low-Level Output Voltage to a value greater than the Side 1 High-Level Input Voltage, thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

4.2.1.1 Features

- Isolated bidirectional, I^2C compatible, communications
- Supports up to 1 MHz operation
- 3- to 5.5-V supply range
- Open drain outputs with 3.5-mA Side 1 and 35-mA Side 2 sink current capability
- –40°C to 125°C operating temperature
- ±50 kV/µs transient immunity (typical)
- HBM ESD protection of 4 kV on all pins; 8 kV on bus pins

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4.2.2 Digital Isolator: ISO7320C Dual-Channel Digital Isolators

The ISO7320C provides galvanic isolation up to 3000 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have two isolated channels comprised of logic input and output buffers separated by silicon dioxide (SiO_2) insulation barriers. The ISO7320 has both channels in the same direction while the ISO7321 has the two channels in opposite direction. In case of input power or signal loss, default output is 'low' for devices with suffix 'F' and 'high' for devices without suffix 'F'. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The ISO7320C have integrated noise filters for harsh industrial environment where short noise pulses may be present at the device input pins. The ISO7320C has TTL input thresholds and operate from 3- to 5.5-V supply levels. Through innovative chip design and layout techniques, the electromagnetic compatibility (EMC) of the ISO7320C has been significantly enhanced to enable system-level ESD, EFT, surge, and emissions compliance.

4.2.2.1 Features

- Signaling rate: 25 Mbps
- Integrated noise filter on the inputs
- Default output ‘high’ and ‘low’ options
- Low power consumption: Typical ICC per channel at 1 Mbps:
  - ISO7320: 1.2 mA (5-V supplies), 0.9 mA (3.3-V supplies)
  - ISO7321: 1.7 mA (5-V supplies), 1.2 mA (3.3-V supplies)
- Low propagation delay: 33 ns typical (5-V supplies)
- 3.3- and 5-V level translation
- Wide temperature range: –40°C to 125°C
- 65 kV/μs transient immunity, typical (5-V supplies)
- Robust EMC
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Isolation barrier life: > 25 years
- Operates from 3.3- and 5-V supplies

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4.2.3 Digital Isolator: ISO7820 Dual-Channel Digital Isolators

The ISO7820 is a high-performance, dual-channel digital isolator with 8000 V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, CQC, and TUV. The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. The ISO7820 has two forward channels and no reverse-direction channel. If the input power or signal is lost, default output is 'high' for the ISO7820 and 'low' for the ISO7820F device. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, the EMC of the ISO7820 has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

4.2.3.1 Features

- Signaling rate: Up to 100 Mbps
- Wide supply range: 2.25 to 5.5 V
- 2.25- to 5.5-V level translation
- Wide temperature range: –55°C to 125°C
- Low power consumption, typical 1.7 mA per channel at 1 Mbps
- Low propagation delay: 11 ns typical (5-V supplies)
- Industry leading CMTI (min): ±100 kV/μs
- Robust EMC
- System-level ESD, EFT, and surge immunity
- Low emissions
- Isolation barrier life: > 25 years
- SOIC-16 wide body (DW) and extra-wide body (DWW) package options

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4.3 Isolated Power Supply

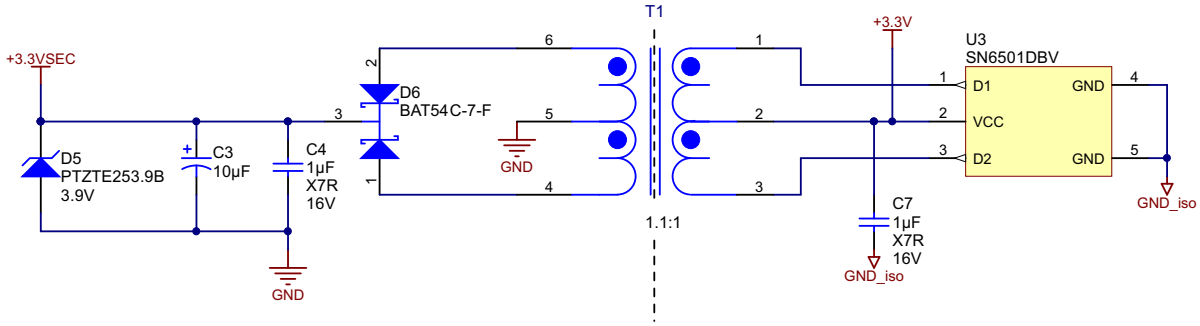

Figure 7. Isolated Power Supply

4.3.1 Push-Pull Driver for Isolated Power Supplies SN6501DBV

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches. The SN6501 is available in a small SOT-23 (5) package, and is specified for operation at temperatures from –40°C to 125°C.

4.3.1.1 Features

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (max)
  - 3.3-V supply: 150 mA (max)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

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4.3.2 Isolation Transformer

Table 10. Isolation Transformer 750313734 Specifications

PARAMETER	SPECIFICATION
Isolation voltage	6.25 kV
Operating temperature range	–40°C to 125°C
Termination style	SMD/SMT
Dimensions	9.14 × 8 × 7.62 mm (L × W × H)
Brand	Midcom / Wurth Electronics
Current rating	150 mA
Inductance	340 µH
Maximum DC resistance	0.419 Ω
Primary resistance	0.419 Ω
Product	Transformers
Secondary resistance	0.335 Ω
Series	MID-SN6501
Shielding	Unshielded
Type	Power transformer

4.3.3 Power Supply Overvoltage and ESD Protection Zener (PTZTE253.9B)

Table 11. 3.9-V Power Supply Protection Zener Diode Specification

PARAMETER	SPECIFICATION
Voltage — Zener (Nom; Vz)	4.1 V
Tolerance	±6%
Power — Max	1 W
Impedance (Max; Zzt)	15 Ω
Current — Reverse leakage @ Vr	40 µA @ 1 V
Mounting type	Surface mount
Package or case	DO-214AC, SMA
Supplier device package	PMDS

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4.4 Simulation of Host MCU Interface

To test the functionality, the host interface was simulated using an MCU-based system.

4.4.1 Tiva C Series LaunchPad Interface

The Tiva C Series LaunchPad (EK-TM4C123GXL) is a low-cost evaluation platform for ARM® Cortex™-M4F-based microcontrollers. The Tiva C Series LaunchPad design highlights the TM4C123GH6PMI microcontroller USB 2.0 device interface, hibernation module, and motion control pulse-width modulator (MC PWM) module. The Tiva C Series LaunchPad also features programmable user buttons and an RGB LED for custom applications. The stackable headers of the Tiva C Series LaunchPad BoosterPack™ XL interface demonstrate how easy it is to expand the functionality of the Tiva C Series LaunchPad when interfacing to other peripherals on many existing BoosterPack add-on boards as well as future products. Figure 8 shows a photo of the Tiva C Series LaunchPad.

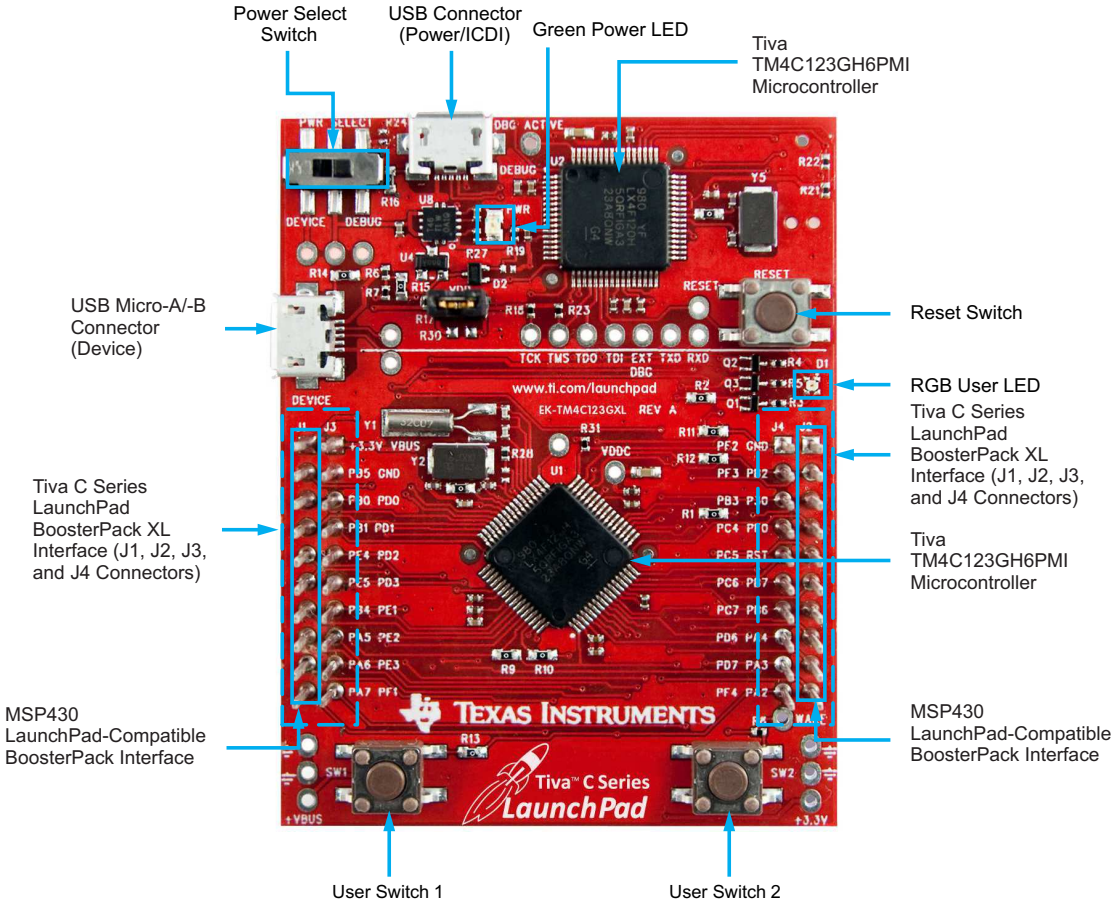

Figure 8. Tiva C Series TM4C123G LaunchPad Evaluation Board

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4.5 Input Voltage Divider, Signal Conditioning, and Protection

Note on resistor divider

The 300-KΩ resistance was increased to 500 KΩ and 1 MΩ, and voltage measurement accuracy was tested. No variation in accuracy was observed with increase in resistance. The 300-KΩ impedance has been finalized. The ratio of division has to be maintained even with an increase in total resistance.

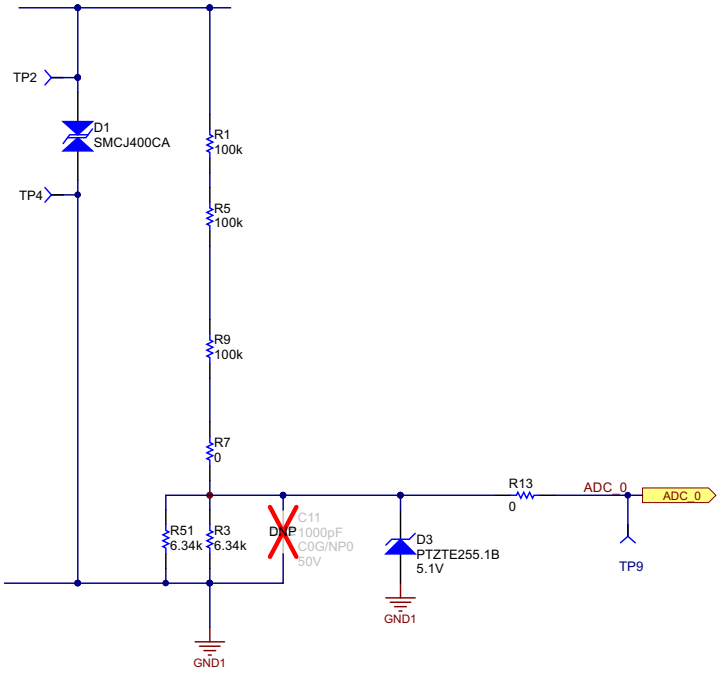

Figure 9. Analog Input

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4.5.1 Input Protection

The binary input module is protected against overvoltage and transients. The SMCJ400CA is used to achieve the required protection.

Table 12. SMCJ400 Specifications

PARAMETER	SPECIFICATION
Type	Zener
Bidirectional channels	1
Voltage — Reverse standoff (Typ)	400 V
Voltage — Breakdown (Min)	447 V
Voltage — Clamping (Max) @ I_{PP}	648 V
Current — Peak Pulse (10/1000 µs)	2.3 A
Power — Peak pulse	1500 W (1.5 kW)
Power line protection	No
Applications	General Purpose
Capacitance @ frequency	—
Operating temperature	–55°C to 150°C (T_J)
Mounting type	Surface mount
Package or case	DO-214AB, SMC

4.5.2 Resistor Divider

A 100-KΩ 1206 package resistor, which can withstand a maximum voltage of 200 V, is selected for this application. The resistor tolerance and temperature drift can be selected based on the accuracy requirement.

4.5.3 ADC Input Overvoltage Protection (PTZTE255.1B)

A Zener diode is used to protect the electronic circuit from overvoltage and ESD.

Table 13. 5.1-V Analog Input to ADC Protection Diode Specifications

PARAMETER	SPECIFICATION
Voltage — Zener (Nom; Vz)	5.4 V
Tolerance	±6%
Power — Max	1 W
Impedance (Max; Zzt)	8 Ω
Current — Reverse leakage @ Vr	20 µA @ 1 V
Mounting type	Surface mount
Package or case	DO-214AC, SMA

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4.6 Wetting Current Control

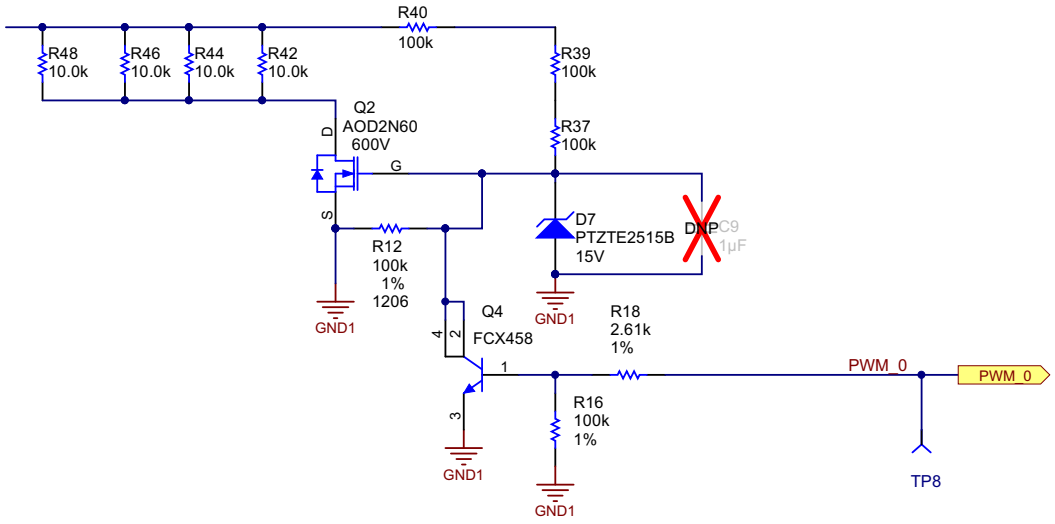

Figure 10. Wetting Current Control Circuit

4.6.1 Transistor Drive for MOSFET Gate Driver

A transistor is used to drive the MOSFET that controls the wetting current. The bias voltage of 15 V max is generated from the binary input using a Zener PTZTE2515BCT regulator.

Table 14. 15-V Transistor Bias Voltage Regulation Zener Specification

PARAMETER	SPECIFICATION
Voltage — Zener (Nom; Vz)	15.4 V
Tolerance	±6%
Power — Max	1 W
Impedance (Max; Zzt)	10 Ω
Current — Reverse leakage @ Vr	10 µA @ 11 V
Mounting type	Surface mount
Package or case	DO-214AC, SMA

Table 15. FCX458 Transistor Specifications

PARAMETER	SPECIFICATION
Transistor type	NPN
Current — Collector (Ic; Max)	225 mA
Voltage — Collector emitter breakdown (Max)	400 V
Vce Saturation (Max) @ Ib, Ic	500 mV @ 6 mA, 50 mA
Current — Collector cutoff (Max)	100 nA
DC current gain (hFE) (Min) @ Ic, Vce	100 @ 50 mA, 10 V
Power (Max)	1 W
Frequency — Transition	50 MHz
Mounting type	Surface mount
Package or case	TO-243AA

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4.6.2 Current Limiting Resistors and MOSFET AOD2N60A

Table 16. Wetting Current Control MOSFET Specifications

PARAMETER	SPECIFICATION
FET type	MOSFET N-channel, metal oxide
FET feature	Standard
Drain-to-source voltage (V_{DS})	600 V
Current — Continuous drain (Id) @ 25°C	2 A (Tc)
Rds On (Max) @ Id, Vgs	4.7 Ω @ 1 A, 10 V
$V_{GS(th)}$ (Max) @ Id	4.5 V @ 250 µA
Gate charge (Qg) @ Vgs	11 nC @ 10 V
Input capacitance (Ciss) @ V_{DS}	295 pF @ 25 V
Power (Max)	57 W
Mounting type	Surface mount
Package or case	TO-252-3, DPak (Two Leads + Tab), SC-63
Supplier device package	TO-252 (D-Pak)

Four resistors, 1206 package 10 KΩ each in parallel, are used as current limit for wetting current. A D-PAK MOSFET with a 600-V rating is used for enhanced reliability.

4.7 Hardware Design Guidelines

- Input voltage divider selection: Ensure the resistors are de-rated 30% for the maximum withstand voltage rating.
- Wetting current control resistor selection: The short time overload capability must be greater than 2.5 times the normal voltage withstand capability for one second.
- 15-V Zener selection for MOSFET switching: Vz must be constant for wide bias currents. The Zener current must be as less as possible to reduce power loss.
- Zener selection for ADC input overvoltage protection: At lower biasing, current Vz reduces and this will clip the input voltage affecting accuracy. The Vz at low bias current must be selected such that at the lowest input voltage, the voltage would be sufficient to bias the MOSFET.

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4.8 Enhancements

4.8.1 Increasing Binary Inputs

Up to six inputs can be configured as ADC to measure the binary inputs. If there is a requirement to increase number of inputs to more than two, the resistor divider and the wetting control circuit have to be added. The circuit that has to be added is shown in Figure 11.

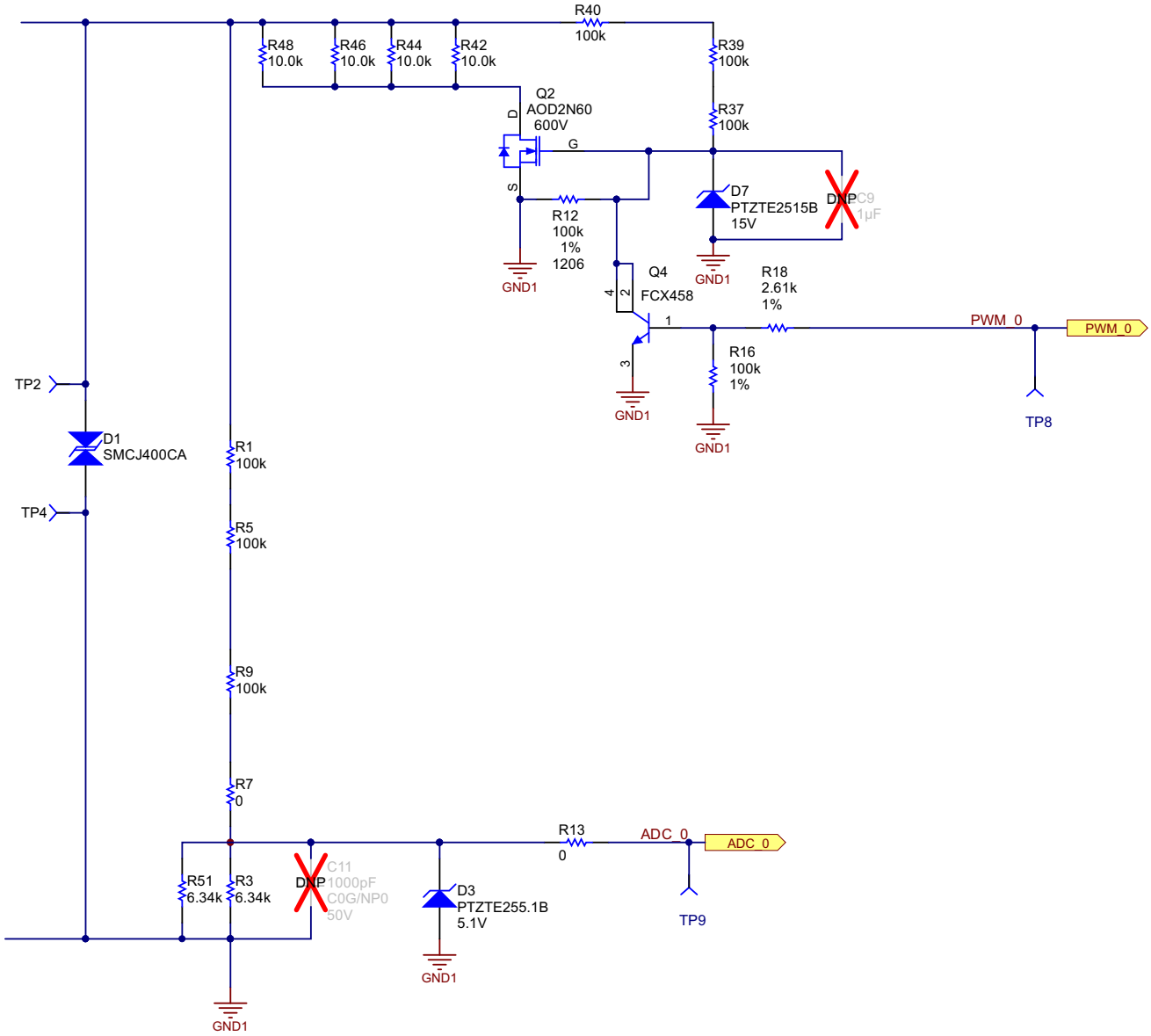

Figure 11. Circuit to Add for Binary Input Channel Expansion

4.8.2 Migration of Digital Isolator From Basic to Reinforced Isolation

TI has a reinforced isolator as part of the isolator roadmap that is package and pin compatible. With this design, the migration to reinforce would need minimal efforts of digital isolator replacement and testing. There may not be any design efforts required.

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5 Software Description

5.1 Initialization

Table 17. MCU Peripherals Initialization for DC Binary Module Functionality

FUNCTIONALITY	DESCRIPTION
MCU clock	SMCLK and DCO are initialized to 1 MHz
Timer	1. Configure the timer capture control register (TA0CCTL0) to select no capture CMx as 0, compare/capture input selected as CCIxA, output mode OUTMODx as 0 and enable compare interrupt CCIE. 2. Timer A programmed to provide interrupt every 200 µs (or any other sampling interval desired). Set the sampling interval (TA0CCR0) 3. Configure the Timer A control register (TA0CTL) to choose SMCLK, divider as 1 and up/down mode.
ADC – Four channels	1. Disable conversion. 2. Configure the following options for the ADC control register0 (ADC10CTL0): (a) Enable ADC interrupt. (b) Switch ON ADC. (c) Set the sample and hold time to 16 x ADC10CLKs. (d) Set the reference voltages for ADC: VR+ = V_{CC} and VR– = VSS ADC10CTL0, once configured, does not need to be changed to switch between different channels. 3. Configure the following options for the ADC control register0 (ADC10CTL1): (a) Set the mode to single channel single conversion. (b) Set the ADC clock to ADC1OSC. (c) Set the divider to 1. (d) Set the sampling trigger to ADC10SC bit. (e) Set the channel to be sampled. 4. Enable ADC channels ADC10AE0. 5. Enable conversion. 6. To sample multiple channels, ADC10CTL1 and ADC10AE0 registers can be updated with the other desired ADC channel. 7. Issue ADC convert sample by setting ADC10SC bit.
Ports	1. Configure the direction of the ports (P1DIR); 0 as inputs and 1 as outputs. 2. Set the default values for outputs (0 as low, 1 as high).
I^2C	1. Set the output pins for I^2C (P1.6 and P1.7) to high. 2. Enable the pull up resistors for P1.6 and P1.7 (P1REN). 3. Enable the USI function by setting the USIPE6 and USIPE7 bits in USICTL0 register. 4. Disable the USI peripheral using software reset (USISWRST bit). 5. Enable I^2C mode and USI interrupt enable. 6. Set clock polarity. 7. Disable automatic clear control (USIIFGCC bit). 8. Enable USI peripheral by clearing the (USISWRST bit). .

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5.2 Functionality

Table 18. DC Binary Module Functional Description

FUNCTIONALITY	DESCRIPTION
Power ON	1. Stop the watchdog timer. 2. Initialize the clocks to set SMCLK to 1 MHz. 3. Disable all interrupts. 4. Set the direction of port pins to default values. 5. Initialize I^2C in master mode. 6. Configure Timer A to provide an interval based interrupt using compare register. The timer interrupt can be used to periodically trigger ADC sampling. 7. Initialize ADC to sample one ADC channel. Re-initialize ADC10CTL1 and ADC10AE0 to sample a different ADC channel. 8. Enable all interrupts.
ADC sample capturing	• Samples are triggered by setting ADC10SC bit. (From the timer interrupt for the first channel) • When conversion is complete, it triggers an interrupt. The result is obtained by reading the register ADC10MEM. • Reinitialize the ADC to read the other ADC channels and issue ADC10SC trigger. Repeat this step to read the other ADC channels.
ADC samples integration	• After the value is read from ADC10MEM, the offset has to be corrected. • For each ADC channel, the sample values are added over a timer period (1 ms) and then averaged by dividing with the number of sample counts.
3- and 10-ms ADC count calculation	• The 1-ms average for each channel can be stored for a pay period of time (for example, 10 ms equals 10 values). This facilitates calculating the 3- and 10-ms sample count average.
I^2C interface for communicating ADC count to host	• The 3- and 10-ms averages can be transmitted over I^2C to the host processor. • A pre-requisite for this is to have a host processor (for example, LaunchPad) that runs as an I^2C slave. • The master sends 3- and 10-ms averages for each channel on I^2C. The slave replies with 3- and 10-ms averages for each channel on I^2C.
Digital isolator interface for testing	• Measure the input voltage in ADC counts and compare with set ADC count and indicate the input voltage as high or low.

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5.3 Calculations

Table 19. Maximum DC Input Allowed

PARAMETER	SPECIFICATION
ADC range in counts	0 to 1023
Resistor divider ratio	303.16 KΩ / 3.16 KΩ = 95.93
ADC reference	ADCref = 3.3 V
Maximum input voltage	ADCref × Resistor divider ratio = 315 V

Table 20. Converting ADC Count to Voltage

PARAMETER	SPECIFICATION
V_{CC}	3.3 V
Maximum input	315 V
ADC count for maximum input	1023
DC voltage equivalent for one ADC count	Maximum input / ADC count = 0.3076 V

5.4 Programming

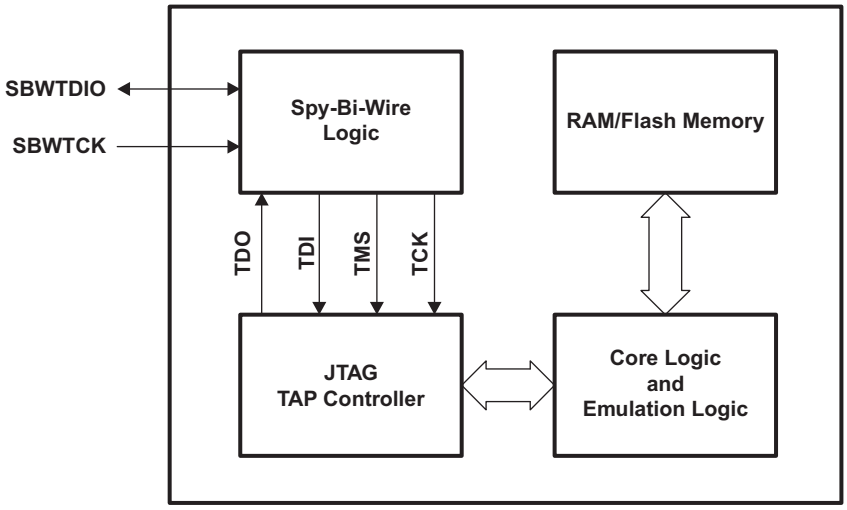

Figure 12. Spy-Bi-Wire Basic Concept

The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data I/O) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the $\overline{\text{RST}}$/NMI pin of the device.

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6 Testing

6.1 Functional Testing

Table 21. Measurements

PARAMETERS	SPECIFICATION	MEASUREMENT
Isolated supply — 3.3-V output	3.3 V	3.28 V
MCU programming	Spy-Bi-Wire	OK

6.2 Voltage Measurement Accuracy Testing

NOTE: The readings in the following tables are the measurements taken without any calibration. The errors include component tolerances and ADC error. The accuracy can be improved by introducing software calibration.

The errors observed can be further improved by doing a gain calibration. To ensure that the results are less than ±3.0% of measured value ±1 V (programmable step size), applying gain calibration is recommended. The gain calibration can be applied on the host side.

For initial testing, averaging was done for 1, 3, and 10 ms. The measurement was repeatable at 3 and 10 ms, and there was no difference observed in the measured values. In case measurements are expected to be done faster than 3 ms, characterization has be done for accuracy before implementation.

6.2.1 Testing with 3-ms Averaging

Table 22. Board 1: DC Input Voltage versus Measured Voltage Difference

DC INPUT VOLTAGE	ALLOWED DC VOLTAGE LIMIT (±V)	MEASURED VOLTAGE	DIFFERENCE B1_Ch1	MEASURED VOLTAGE	DIFFERENCE B1_Ch2
18	1.54	17.932	–0.068	17.932	–0.068
19	1.57	18.859	–0.141	18.55	–0.45
20	1.6	19.787	–0.213	19.478	–0.522
21	1.63	20.714	–0.286	20.714	–0.286
24	1.72	23.806	–0.194	23.497	–0.503
48	2.44	47.922	–0.078	47.612	–0.388
49	2.47	48.54	–0.46	48.231	–0.769
50	2.5	49.467	–0.533	49.467	–0.533
51	2.53	50.395	–0.605	50.086	–0.914
72	3.16	71.419	–0.581	71.419	–0.581
110	4.3	109.137	–0.863	108.519	–1.481
111	4.33	110.065	–0.935	109.756	–1.244
112	4.36	110.683	–1.317	110.374	–1.626
113	4.39	112.229	–0.771	111.611	–1.389
144	5.32	142.837	–1.163	142.219	–1.781
196	6.88	194.469	–1.531	193.85	–2.15
240	8.2	237.753	–2.247	236.825	–3.175
241	8.23	238.68	–2.32	238.062	–2.938
242	8.26	239.608	–2.392	238.68	–3.32
276	9.28	273.616	–2.384	272.689	–3.311
300	10	296.804	–3.196	295.877	–4.123

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Table 23. Board 2: DC Input Voltage versus Measured Voltage Difference

DC INPUT VOLTAGE	ALLOWED DC VOLTAGE LIMIT (±V)	MEASURED VOLTAGE	DIFFERENCE B2_Ch1	MEASURED VOLTAGE (V)	DIFFERENCE B2_Ch2
18	1.54	18.241	0.241	18.55	0.55
19	1.57	19.169	0.169	19.478	0.478
20	1.6	20.405	0.405	20.405	0.405
21	1.63	21.333	0.333	21.642	0.642
24	1.72	24.425	0.425	24.425	0.425
48	2.44	48.54	0.54	48.54	0.54
49	2.47	49.467	0.467	49.467	0.467
50	2.5	50.395	0.395	50.704	0.704
51	2.53	51.632	0.632	51.632	0.632
72	3.16	72.346	0.346	71.419	–0.581
110	4.3	110.374	0.374	109.447	–0.553
111	4.33	111.302	0.302	110.374	–0.626
112	4.36	112.538	0.538	110.992	–1.008
113	4.39	113.466	0.466	111.92	–1.08
144	5.32	144.383	0.383	143.455	–0.545
196	6.88	196.324	0.324	194.778	–1.222
240	8.2	240.226	0.226	238.68	–1.32
241	8.23	241.153	0.153	239.608	–1.392
242	8.26	242.39	0.39	240.226	–1.774
276	9.28	276.399	0.399	273.926	–2.074
300	10	300.205	0.205	297.732	–2.268

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6.2.2 Testing With 10-ms Averaging

Table 24. Board 1: DC Input Voltage versus Measured Voltage Difference

DC INPUT VOLTAGE	ALLOWED DC VOLTAGE LIMIT (±V)	MEASURED VOLTAGE	DIFFERENCE B1_Ch1	MEASURED VOLTAGE	DIFFERENCE B1_Ch2
18	1.54	17.932	0.068	17.932	0.068
19	1.57	18.859	0.141	18.55	0.45
20	1.6	19.787	0.213	19.787	0.213
21	1.63	20.714	0.286	20.405	0.595
24	1.72	23.806	0.194	23.497	0.503
48	2.44	47.612	0.388	47.612	0.388
49	2.47	48.849	0.151	48.54	0.46
50	2.5	49.467	0.533	49.467	0.533
51	2.53	50.395	0.605	50.086	0.914
72	3.16	71.419	0.581	71.109	0.891
110	4.3	108.828	1.172	108.519	1.481
111	4.33	110.065	0.935	109.447	1.553
112	4.36	110.992	1.008	110.374	1.626
113	4.39	111.92	1.08	111.611	1.389
144	5.32	142.837	1.163	142.219	1.781
196	6.88	194.159	1.841	193.541	2.459
240	8.2	237.753	2.247	236.825	3.175
241	8.23	238.68	2.32	237.753	3.247
242	8.26	239.608	2.392	238.68	3.32
276	9.28	273.307	2.693	272.071	3.929
300	10	296.804	3.196	295.568	4.432

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Table 25. Board 2: DC Input Voltage versus Measured Voltage Difference

DC INPUT VOLTAGE	ALLOWED DC VOLTAGE LIMIT (±V)	MEASURED VOLTAGE	DIFFERENCE B2_Ch1	MEASURED VOLTAGE	DIFFERENCE B2_Ch2
18	1.54	18.241	0.241	18.55	0.55
19	1.57	19.169	0.169	19.169	0.169
20	1.6	20.405	0.405	20.405	0.405
21	1.63	21.333	0.333	21.333	0.333
24	1.72	24.425	0.425	24.115	0.115
48	2.44	48.54	0.54	48.54	0.54
49	2.47	49.467	0.467	49.467	0.467
50	2.5	50.395	0.395	50.704	0.704
51	2.53	51.632	0.632	51.322	0.322
72	3.16	72.346	0.346	71.419	–0.581
110	4.3	110.374	0.374	109.447	–0.553
111	4.33	111.302	0.302	110.374	–0.626
112	4.36	112.229	0.229	110.992	–1.008
113	4.39	113.466	0.466	111.92	–1.08
144	5.32	144.383	0.383	143.455	–0.545
196	6.88	196.324	0.324	194.778	–1.222
240	8.2	240.226	0.226	238.68	–1.32
241	8.23	241.153	0.153	239.608	–1.392
242	8.26	242.39	0.39	240.226	–1.774
276	9.28	276.399	0.399	273.926	–2.074
300	10	300.205	0.205	297.732	–2.268

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6.2.3 Error in % of the Measured Value

Table 26. Input Voltage versus Measured Voltage Error (% of the Reading)

DC INPUT VOLTAGE @ 10 ms	BOARD 1 ERROR (%)		BOARD 2 ERROR (%)	
	B1_Ch1	B1_Ch2	B2_Ch1	B2_Ch2
18	–0.38	–0.38	1.34	3.06
19	–0.74	–2.37	0.89	2.51
20	–1.07	–2.61	2.03	2.03
21	–1.36	–1.36	1.58	3.06
24	–0.81	–2.10	1.77	1.77
48	–0.16	–0.81	1.12	1.12
49	–0.94	–1.57	0.95	0.95
50	–1.07	–1.07	0.79	1.41
51	–1.19	–1.79	1.24	1.24
72	–0.81	–0.81	0.48	–0.81
110	–0.78	–1.35	0.34	–0.50
111	–0.84	–1.12	0.27	–0.56
112	–1.18	–1.45	0.48	–0.90
113	–0.68	–1.23	0.41	–0.96
144	–0.81	–1.24	0.27	–0.38
196	–0.78	–1.10	0.17	–0.62
240	–0.94	–1.32	0.09	–0.55
241	–0.96	–1.22	0.06	–0.58
242	–0.99	–1.37	0.16	–0.73
276	–0.86	–1.2	0.14	–0.75
300	–1.07	–1.37	0.07	–0.76

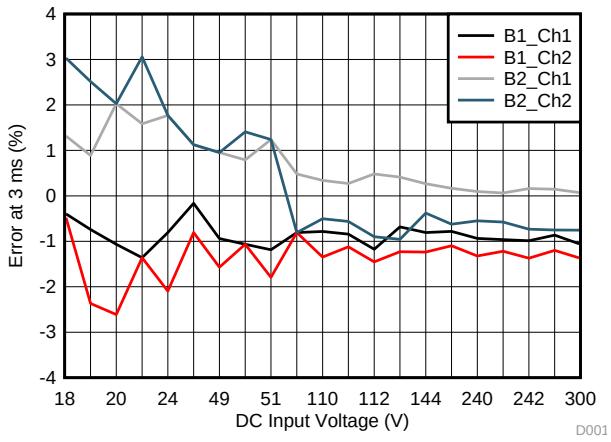

Figure 13. DC Input Voltage versus Measured Voltage Error (% of the Reading)

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Table 27. Input Voltage versus Measured Voltage Error (% of the Reading)

DC INPUT VOLTAGE @ 10 ms	BOARD 1 ERROR (%)		BOARD 2 ERROR (%)	
	B1_Ch1	B1_Ch2	B2_Ch1	B2_Ch2
18	–0.38	–0.38	1.34	3.06
19	–0.74	–2.37	0.89	0.89
20	–1.07	–1.07	2.03	2.03
21	–1.36	–2.83	1.58	1.58
24	–0.81	–2.10	1.77	0.48
48	–0.81	–0.81	1.12	1.12
49	–0.31	–0.94	0.95	0.95
50	–1.07	–1.07	0.79	1.41
51	–1.19	–1.79	1.24	0.63
72	–0.81	–1.24	0.48	–0.81
110	–1.07	–1.35	0.34	–0.50
111	–0.84	–1.40	0.27	–0.56
112	–0.90	–1.45	0.20	–0.90
113	–0.96	–1.23	0.41	–0.96
144	–0.81	–1.24	0.27	–0.38
196	–0.94	–1.25	0.17	–0.62
240	–0.94	–1.32	0.09	–0.55
241	–0.96	–1.35	0.06	–0.58
242	–0.99	–1.37	0.16	–0.73
276	–0.98	–1.42	0.14	–0.75
300	–1.07	–1.48	0.07	–0.76

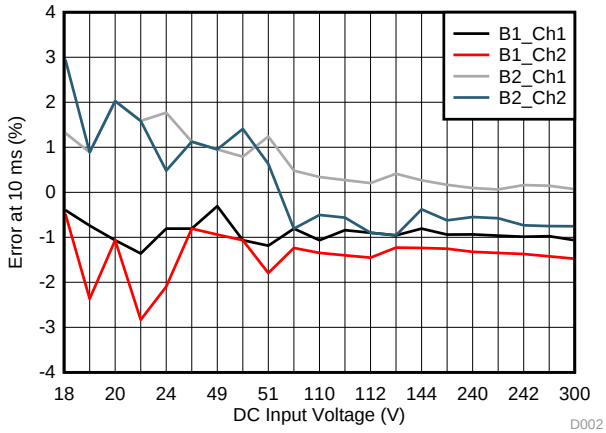

Figure 14. DC Input Voltage versus Measured Voltage Error (% of the Reading)

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6.3 Drift Due to Temperature Variation of Signal Conditioning Circuit

The signal conditioning circuit consisting of the resistor divider, 400-V input TVS, 5.1-V ADC input protection Zener was tested for temperature variation. The leakage current for 400-V TVS is < 1 µA at rated voltage for SMCJ package. The following results indicate that the effect of leakage current does not significantly influence the voltage input to ADC.

Table 28. Voltage Drift With Temperature at 300-V Input

TEMPERATURE °C	MEASURED VOLTAGE (V)	DIFFERENCE (–V)
–10	298.92	–1.082
12	299.01	–0.986
40	299.01	–0.986
70	299.11	–0.890

Table 29. Voltage Drift With Temperature at 110-V Input

TEMPERATURE °C	MEASURED VOLTAGE (V)	DIFFERENCE (–V)
–10	109.84	–0.160
10	109.74	–0.256
40	109.84	–0.160
70	109.84	–0.160

Table 30. Voltage Drift With Temperature 24-V Input

TEMPERATURE °C	MEASURED VOLTAGE (V)	DIFFERENCE (–V)
–10	23.98	–0.018
10	23.89	–0.113
40	23.98	–0.018
70	23.98	–0.018

6.4 Wetting Current Measurement

Table 31. Wetting Current Measurement at Different Voltage Inputs

DC VOLTAGE INPUT SWITCHED ON FOR 50 ms	IMPEDANCE	INPUT 1 CURRENT (mA)	DUTY CYCLE	INPUT 2 CURRENT (mA)	DUTY CYCLE
24 V	2.5 K	~9	NA	~9	N/A
110 V	2.5 K	~44	NA	~44	N/A
230 V	2.5 K	~44	50%	~44	50%

6.5 Binary Input Testing With Digital Output (ISO7220ADR)

Table 32. Results With Digital Isolator Mounted

DC INPUT V_{IN}	APPLIED VOLTAGE	TOLERANCE	BINARY INPUT 1 OBSERVATION	BINARY INPUT 2 OBSERVATION
24	22	±3% of V_{IN} ±1 V	Low	Low
24	26	±3% of V_{IN} ±1 V	High	High
110	106	±3% of V_{IN} ±1 V	Low	Low
110	114	±3% of V_{IN} ±1 V	High	High
240	230	±3% of V_{IN} ±1 V	Low	Low
240	250	±3% of V_{IN} ±1 V	High	High

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6.6 IEC Pre-Compliance Testing

The following EMC tests have been performed.

Table 33. EMC Tests

TEST	STANDARD
ESD	IEC61000-4-2
Surge	IEC61000-4-5

Table 34. Performance Criteria

CRITERIA	ACCEPTANCE (PASS) CRITERIA
A	The analog output module must continue to operate as intended. No loss of function or performance occur even during the test.
B	Temporary degradation of performance is accepted. After the test, the analog output module must continue to operate as intended without manual intervention.
C	During the test, a loss of functions accepted, but no destruction of hardware or software. After the test, the analog output module must continue to operate as intended automatically after manual restart or power off/power on.

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6.6.1 IEC61000-4-2 ESD Test

The IEC610004-2 ESD test simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. Electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the equipment under test (EUT), which can happen through direct contact with the EUT (contact discharge), or through an air-gap (air-discharge). This was applied across signal inputs only. A series of 10 negative and positive pulses were applied directly on the binary inputs during the test (contact discharge). After the test, the binary input module was attached to TM4C123GXL LaunchPad to verify functionality. The test results show the EUT was able to withstand the required discharge . The EUT was not permanently damaged.

Table 35. ESD Test Steps

TEST NUMBER	TEST MODE	OBSERVATION		
		ISO1541D	ISO7320C OR ISO7320FC	ISO7820 OR ISO7820F
1	Contact 1 kV	PASS	PASS	PASS
2	Contact –1 kV	PASS	PASS	PASS
3	Contact 2 kV	PASS	PASS	PASS
4	Contact –2 kV	PASS	PASS	PASS
5	Contact 4 kV	PASS	PASS	PASS
6	Contact –4 kV	PASS	PASS	PASS
7	Contact 6 kV	NA	PASS	PASS
8	Contact –6 kV	NA	PASS	PASS
9	Contact 8 kV	NA	NA	PASS
10	Contact –8 kV	NA	NA	PASS

Table 36. ESD Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	Binary input	±2 kV	Meets Criteria B (After the test, the module continued to operate as intended.)

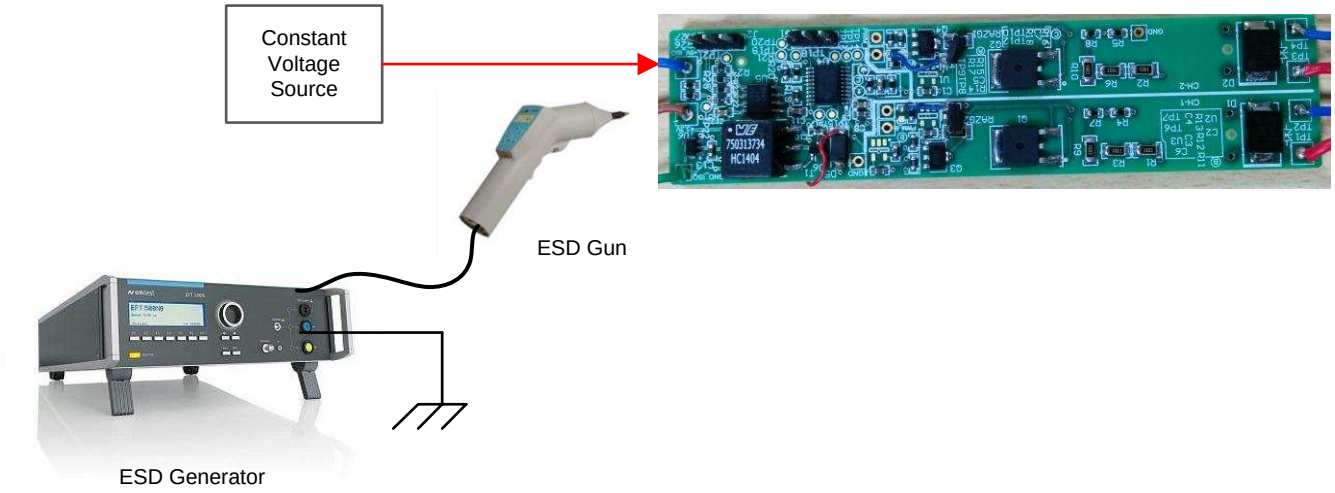

Figure 15. ESD Setup for Binary Input Module

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6.6.2 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of one minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. The test generator was configured for 1.2/50-μs surges and diode clamps were used for line-to-ground coupling. A series of five negative and positive pulses, with 10 seconds spacing between each pulse, were applied during the test. After the test, the binary input module was attached to TM4C123GXL LaunchPad to verify functionality. The test results show the EUT was able to withstand up to ±500-V bursts. The EUT was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing with Class B.

Table 37. Surge Test Steps

TEST NUMBER	TEST MODE	OBSERVATION		
		ISO1541D	ISO7320C OR ISO7320FC	ISO7820 OR ISO7820F
1	0.5 kV	PASS	PASS	PASS
2	–0.5 kV	PASS	PASS	PASS
3	1 kV	PASS	PASS	PASS
4	–1 kV	PASS	PASS	PASS
5	2 kV	PASS	PASS	PASS
6	–2 kV	PASS	PASS	PASS
7	4 kV	PASS	PASS	PASS
8	–4 kV	PASS	PASS	PASS

Table 38. Surge Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
Surge, DM	IEC 61000-4-5: 1.2/20-μs voltage waveform 8/20-μs current waveform 42-Ω impedance	Binary input	± 1 kV	Meets Criteria B (After the test, the module continued to operate as intended.)

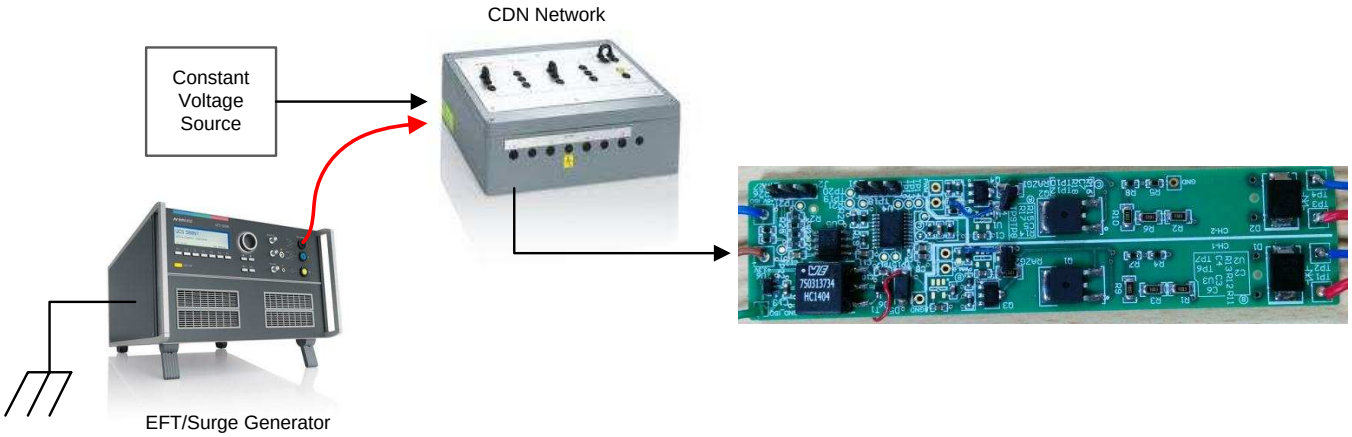

Figure 16. Surge Setup for Binary Input Module

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6.7 Test Results Summary

Table 39. Test Results Summary for DC Binary Input Module

TESTS	OBSERVATION
Power supply	OK
MCU programming	OK
Measurement of DC voltage input	OK
DC input voltage measurement accuracy	< ±3% of measured value ±1 V (programmable step size)
EMC pre-compliance tests	OK

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7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00420.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00420.

7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00420.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00420.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00420.

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8 Terminology

External clearance— The shortest distance through air between conductive input and output leads; measured in mm.

Comparative tracking index (CTI)— Outer molding material characterization in the presence of aqueous contaminants. The higher the CTI value, the more resistant the material is to electrical arc tracking. CTI is often used with creepage by safety agencies to determine working voltage.

External creepage— The shortest distance along the outside surface between input and output leads; measured in mm.

Dielectric insulation voltage withstand rating— The ability to withstand without breakdown a 60-second application of a defined dielectric insulation voltage between input and output leads.

Installation class—

1. Equipment in closed systems (for example, telecom) protected against overvoltage with devices such as diverters, filters, capacitors, and so on.
2. Energy consuming equipment (for example, appliances) supplied through a fixed installation.
3. Primarily equipment in fixed installations (for example, fixed industrial equipment).
4. Primary supply level for industrial factories.

Insulation—

- Operational — Required for correct equipment operation but not as a protection against electric shock.
- Basic — Protects against electric shock.
- Supplementary — Independently applied to basic insulation to protect against shock in the event of its failure.
- Double — Composed of both basic and supplementary.
- Reinforced — A single insulation system composed of several layers (for example, single and supplementary).

Material group (see Comparative Tracking Index) —

1. 600 < CTI
2. 400 < CTI < 600
3. 175 < CTI < 400
4. 100 < CTI <175

Partial discharge— Electric discharge that partially bridges the insulation between two electrodes. Agilent supports partial discharge measurements per VDE0884, a technique developed to evaluate the integrity of insulating materials

Pollution degree—

1. Nonconductive pollution only.
2. Only occasional, temporary conductivity due to condensation.
3. Frequent conductive pollution due to condensation.
4. Persistent conductive pollution due to dust, rain, or snow.

Rated mains voltage— Primary power voltage declared by manufacturer. Used to categorize opto-coupler maximum allowable working voltage.

Common-mode transient rejection (CMTR)— CMTR describes the maximum tolerable rate-of-rise (or fall) of a common-mode voltage (given in volts per microsecond). The specification for CMTR also includes the amplitude of the common-mode voltage (VCM) that can be tolerated. Common-mode interference that exceeds the maximum specification might result in abnormal voltage transitions or excessive noise on the output signal.

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9 References

1. Texas Instruments, *MSP430™ Programming Via the JTAG Interface*, User's Guide (SLAU320).
2. Texas Instruments, *The ISO72x Family of High-Speed Digital Isolators*, Application Report (SLLA198).

10 About the Author

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Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2015) to B Revision	Page
• Added "EMC-Compliant" to title	1
• Added design-specific description to front page	1
• Deleted ISO7220A and added ISO7320C to Design Resources	1
• Added ISO7820 to Design Resources	1
• Changed ISO7220A description and features in Section 4.2.2 and Section 4.2.2.1 and added ISO7320C description and features	18
• Added Section 4.2.3: Digital Isolator: ISO7820 Dual Channel Digital Isolators	19
• Added Section 4.2.3.1: Features	19
• Changed content in Table 35	39

Revision A History

Changes from Original (March 2015) to A Revision	Page
• Changed from preview page	1

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