TI Designs

230-V/250-W, Hi-η Sensorless Brushless DC Motor Drive With 30% Reduced Bulk Capacitor Reference Design

TI Designs

The TIDA-00472 is a discrete IGBT-based three-phase inverter for driving brushless DC (BLDC) motors rated up to 250 W using the sensorless, trapezoidal control method. Such BLDC motors are used in cooker heads, for example. The design provides software implementation to compensate for DC-bus voltage ripple resulting in a 30% reduction of the requirement in the DC bus capacitor, reducing the overall BOM cost. The cycle-by-cycle overcurrent protection feature protects the power stage from overcurrent and the board can work up to 65°C ambient. This design is a tested, ready-to-use hardware and software platform for controlling the speed of high voltage BLDC motors using sensorless trapezoidal control.

Design Resources

TIDA-00472	Tool Folder Containing Design Files
MSP430F5132	Product Folder
UCC27714	Product Folder
OPA374	Product Folder
TLV70433	Product Folder
LMT87LP	Product Folder
TPD1E10B06	Product Folder
ISO7421	Product Folder
TIDA-00473	Tool Folder
TIDA-00474	Tool Folder

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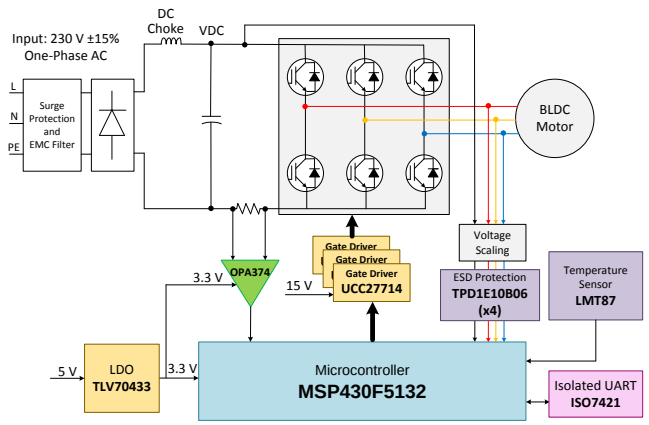
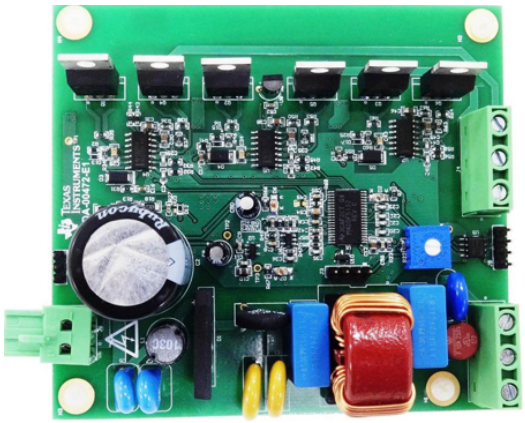
Design Features

- 250-W Mains-Powered BLDC Motor Drive With Sensorless Trapezoidal Control Using the TI InstaSPIN-BLDC Back-EMF Integration Method
- Software Implementation for DC Bus Ripple Compensation Resulting in 30 % Reduced DC Bus Capacitor
- Current Sensing Using Single Shunt Resistor on DC Bus Return With External Low Power and High Bandwidth Op Amp
- PWM Cycle-By-Cycle Current Limit and Protection Achieved Through Integrated High-Speed, High-Precision Comparator and Programmable Reference in MCU
- Highly Efficient Circuit Board Enables Working up to 200 W Without Heat Sink (up to 65ºC Ambient Temperature) Saves Heat Sink and Assembly Cost
- Hardware Design to Meet Conducted Emission Standard - EN55022 Class B, EFT Norm - IEC61000-4-4, and Surge Norm - IEC61000-4-5

Featured Applications

- Cooker Hoods (Also Known as Range Hoods or Kitchen Hoods)
- Air Conditioner Fan
- Exhaust Fans and Blowers





1 Key System Specifications

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS
Input voltage	230 ±15% V, Single-phase AC, 50/60 Hz
Rated input power	250 W
Control method	Sensorless trapezoidal
Inverter switching frequency	20 KHz
Motor electrical frequency	250 Hz (300 Hz maximum)
Feedback signals	Three motor winding voltages, DC bus voltage, low-side DC bus current
Protections	Cycle-by-cycle current limit, input undervoltage, and overtemperature
Operating ambient	–20°C to 65°C
Conducted emission	EN55022 - Class B
EFT	IEC61000-4-4
Surge	IEC61000-4-5
External auxiliary power supply required	15 ±10% V, 50 mA 5 ±10% V, 50 mA

2 System Description

A kitchen hood (also known as a range vent hood, range hood, cooker hood, and chimney) is an appliance which is mounted above the cooktop or kitchen stove and is used to extract and remove fumes, smoke, odors, heat, steam, airborne grease, combustion products, and so forth from the air by the evacuation of the air and use of filtration. The cooker hood consists of a suction fan driven by a mains-powered electric motor, lamps, and human interface or control options.

Low-end kitchen hoods use split-phase AC induction motors with tapped windings to create suction. The new generation of kitchen hoods are adaptable with brushless permanent magnet motors because these motors allow designs to achieve an A+ energy efficiency rating, a continuous and smooth speed variation (enabling automatic adjustment of suction based on the intensity of steam and the generation of gases around the kitchen hood) and operate at a lower noise.

The suction fan motors in the kitchen hood are available in different power levels from 100 W to 500 W using single-phase AC induction motors. In existing kitchen hoods, the AC motor is the part that consumes the majority of power. Brushless motors are more efficient in comparison to the single-phase AC induction motors. The performance of the BLDC motor is far better than AC motors, especially in variable speed applications.

The TIDA-00472 is a three-phase inverter drive based on a discrete insulated-gate bipolar transistor (IGBT) for driving brushless DC (BLDC) motors rated up to 250 W in kitchen hoods using the sensorless, trapezoidal control method.

One of the more costly and bulky components in the drive is the high-voltage DC bus capacitor, which provides a stable DC bus voltage with low ripple for the inverter stage. Reducing the capacitance value can help to reduce the overall size and cost of the system, but this reduction increases the DC-bus voltage ripple, creates torque ripple, and deteriorates the system performance. This TI Design helps to mitigate the challenges caused by the reduction of the DC bus capacitor. The design provides a software implementation for voltage ripple compensation in the DC bus, which results in a 30% reduction of the DC bus capacitor requirement and reduces the cost.

The motor-winding current sensing is done using a single shunt resistor on the DC bus return with an external, low-power, high-bandwidth operational amplifier (op-amp). The cycle-by-cycle overcurrent protection feature protects the power stage from large current spikes and is achieved through the integrated, high-speed high-precision comparator and programmable reference, which is built-in the microcontroller (MCU). The board can work up to 65°C ambient and the high-efficiency circuit board enables working up to 200 W without the requirement of a heat sink or external cooling.

The hardware is designed to meet the following IEC standards: surge, electrical fast transient (EFT), and conducted emission, as per EN55014. This design is a tested, ready-to-use, hardware and software platform for the speed control of high-voltage BLDC motors using sensorless trapezoidal control.

3 Block Diagram

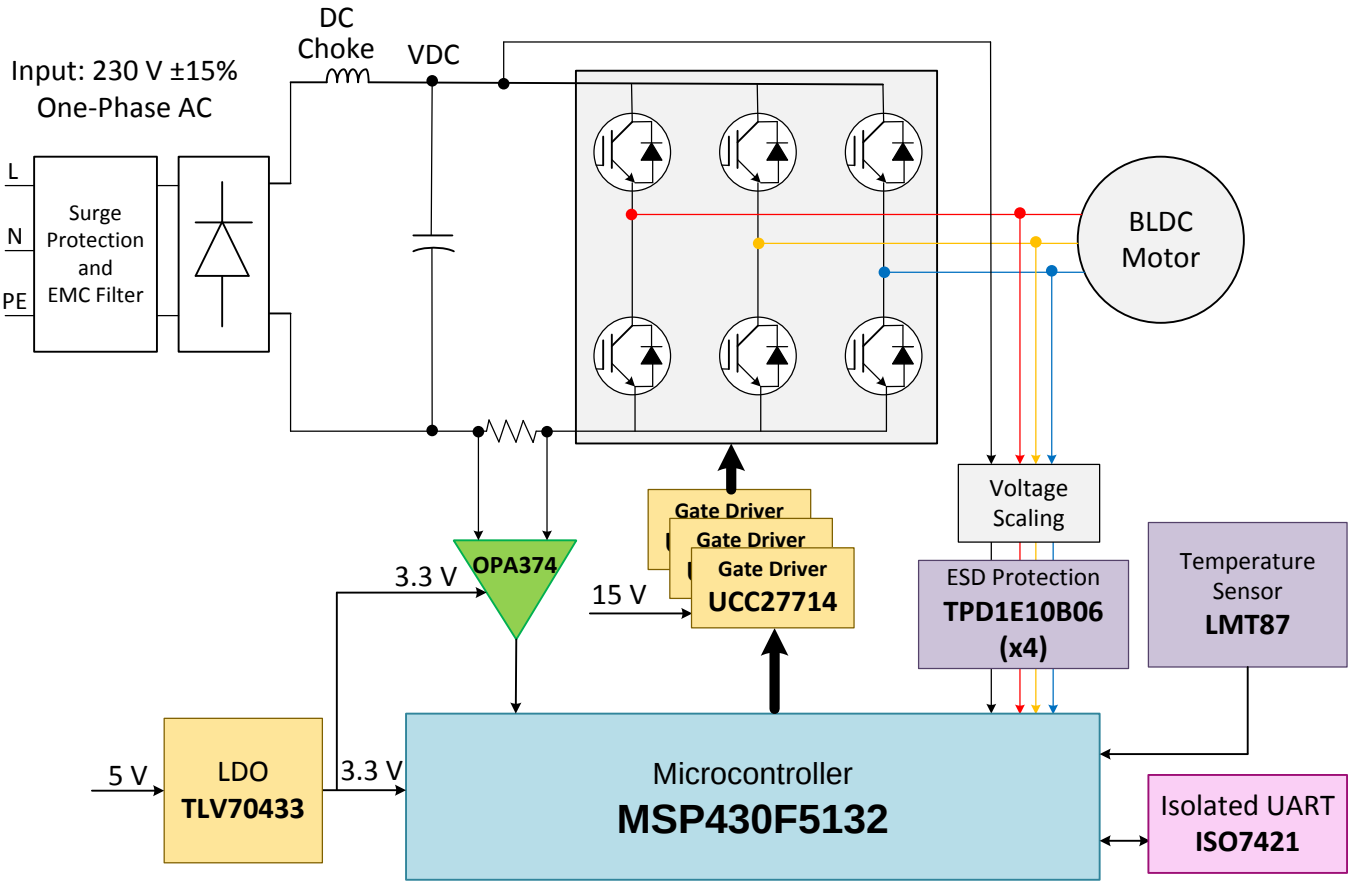


Figure 1. Block Diagram of Mains-Powered 250-W BLDC Drive (TIDA-00472)

3.1 Highlighted Products

3.1.1 MSP430F5132

The TI MSP430™ family of ultralow-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The architecture is combined with five low-power modes. The device features a powerful 16-bit reduced instruction set computing (RISC) CPU, 16-bit registers, and constant generators that contribute to the maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs. The MSP430F51x2 series are microcontroller configurations with two 16-bit high-resolution timers, two universal serial communication interfaces (USCIs) USCI_A0 and USCI_B0, a 32-bit hardware multiplier, a high-performance 10-bit 200-ksps analog-to-digital converter (ADC), an on-chip comparator, a three-channel direct memory access (DMA), 5-V tolerant I/Os, and up to 29 I/O pins. The timer event control module connects different timer modules to each other and routes the external signals to the timer modules. The device is capable of working up to a system frequency of 25 MHz. The operating temperature of the device is –40°C to 85°C.

3.1.2 UCC27714D14

The UCC27714 is a 600-V, high-side, low-side gate driver with 4-A source, and 4-A sink current capability with the purpose of driving power MOSFETs or IGBTs. The device comprises one ground-referenced channel (LO) and one floating channel (HO). The HO is designed to operate with bootstrap supplies. The device features an excellent robustness and noise immunity with the capability to maintain operational logic at negative voltages of up to –8-V DC on the HS pin (at VDD = 12 V).The device features the industry best-in-class input propagation delays and delay matching between both channels with the purpose of minimizing pulse distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control the on and off state of the output. The UCC27714 device output stage features a unique architecture on the pullup structure, which delivers the highest peak-source current when it is most required during the Miller plateau region of the power-switch turnon transition (when the power switch drain or collector voltage experiences dv/dt). The UCC27714 includes protection features at which point the outputs are held LOW when inputs are floating or when the minimum pulse-width specification of the input is not met. The driver inputs are complementary metal-oxide semiconductor (CMOS) compatible and transistor-transistor logic (TTL) compatible for easy interfacing with both digital power controllers and analog controllers. The UCC27714 driver includes an enable and disable function to enable the output gate signals. The device accepts a bias supply with a wide input range from 10 V to 20 V and offers undervoltage lockout (UVLO) protection for both the VCC and HB bias supply pins. The UCC27714 is available in an SOIC-14 package and rated to operate from –40°C to 125°C.

3.1.3 OPA374

The OPA374 families of op-amps are low power and low cost with excellent bandwidth (6.5 MHz) and slew rate (5 V/µs). The input range extends 200 mV beyond the rails and the output range is within 25 mV of the rails. These op-amps are specified for single or dual power supplies of 2.7 V to 5.5 V, an operating temperature range between –40°C to +125°C, and operation from 2.3 V to 5.5 V. These op-amps are available in micro-size packages SOT23-5, SOT23-6, SOT23-8 and DFN-10.

3.1.4 TLV704

The TLV704 series of low-dropout (LDO) regulators are ultralow, quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment to low-power MCUs, such as the MSP430. The TLV704 regulator operates over a wide operating input voltage of 2.5 V to 24 V. This wide range of input voltage makes the device an excellent choice for both battery-powered systems and industrial applications that undergo large line transients. The TLV704 series of linear regulators is available in a 3-mm × 3-mm SOT23-5 package and is specified for –40°C to 125°C.

3.1.5 LMT87

The LMT87 and LMT87-Q1 devices are precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. The device features make it suitable for many general temperature sensing applications. The LMT87/LMT87-Q1 can operate down to a 2.7-V supply with a 5.4-µA power consumption. Multiple package options including through-hole TO-92 and TO-126 packages also allow the LMT87 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations in the same application. Class-AB output structures give the LMT87/LMT87-Q1 a strong output source and sink current capability that can directly drive up to 1.1-nF capacitive loads. These features make the sensors a suitable option to drive an ADC sample-and-hold input with its transient load requirements. The LMT87/LMT87-Q1 accuracy is specified in the operating range of −50°C to 150°C. The accuracy, three-lead package options, and other features also make the LMT87/LMT87-Q1 a reasonable alternative to thermistors.

3.1.6 TPD1E10B06

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD), transient voltage suppression (TVS) diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications. The TPD1E10B06 devices are characterized for operation over a temperature range of –40°C to +125°C.

3.1.7 ISO7421

The ISO7421 digital isolator has two isolated channels. The ISO7420, ISO7420M, and ISO7421 provide galvanic isolation up to 2500 V_{RMS} for one minute per UL. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. When using the ISO7421 device in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The ISO7420 and ISO7421 family of digital isolators are characterized for operation over a temperature range of –40°C to +125°C. The suffix “M” indicates wide temperature range (–40°C to 125°C). These devices have TTL input thresholds and require two supply voltages, 3.3 V or 5 V, or any combination. All of the device inputs are 5-V tolerant when supplied from a 3.3-V supply. The ISO7420 and ISO7421 are specified for signaling rates up to 1 Mbps. These devices also transmit data with much shorter pulse widths, in most cases, because of their fast response times. Designers must add external filtering to remove spurious signals with input pulse duration < 20 ns, if desired.

4 System Design Theory

The complete system consists of the AC-DC power stage for rectification of the 230-V AC along with the EMI filter, three-phase inverter, sensing circuits, and MCU.

4.1 AC-DC Power Stage

Figure 2 shows the AC-DC power stage. This stage has the diode bridge rectifier, bulk electrolytic capacitor at the DC bus, and the necessary filters for conducted emission, surge, and EFT protection as per the standard EN55014.

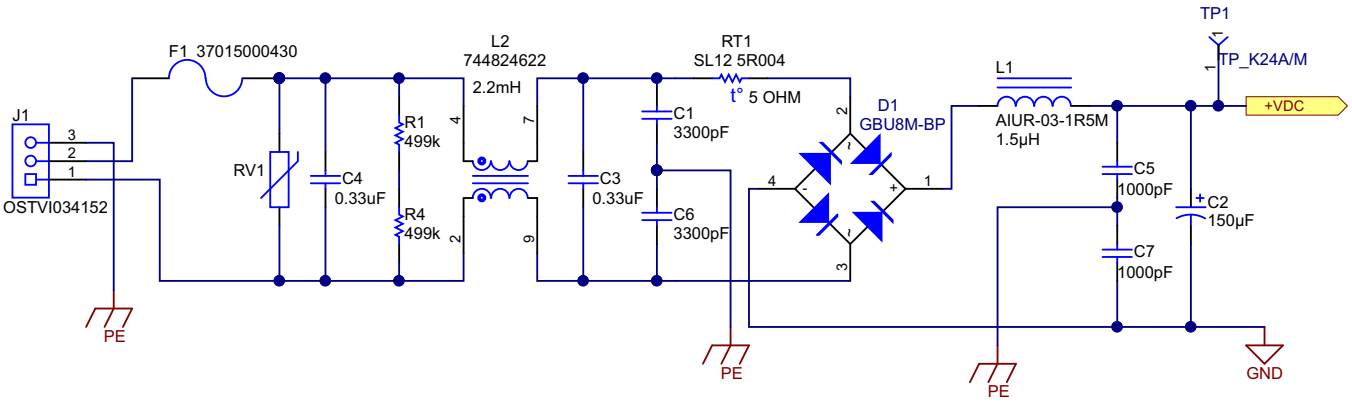


Figure 2. AC-DC Converter Schematic

In the schematic, J1 is the input connector where the single-phase supply line, neutral, and earth are provided. F1 is the protection fuse followed by the metal oxide varistor (MOV) for surge protection. A 10-mm diameter MOV with a 275-V AC rating is selected for this application. R1 and R4 form the discharge resistor for the X2 capacitors C4 and C3. The network consisting of C4, C3, C1, C6, C5, C7, and L2 forms the conducted emission filter. C4 and C3 are X2 rated capacitors; C1, C6, C5, and C7 are Y2 rated capacitors. L2 is a common-mode filter. To limit the inrush current of the bulk DC capacitors, an inrush current limiter RT1 is provided. D1 is the full bridge rectifier. L1 is the DC choke provided for meeting the line harmonic standard. C2 is the electrolytic capacitor at the DC bus.

4.1.1 Design of DC Bus Capacitor

The DC bus capacitor is important while designing the inverter-fed motor drives operating from the AC mains. The DC bus capacitor serves the following purposes:

1. The DC bus capacitor reduces the voltage ripple in the DC link and provides a stable DC link voltage for the inverter. A high DC voltage ripple can cause motor torque ripple leading to an inferior performance of the motor drive.
2. The DC bus capacitor acts as a local storage for handling the ripple current (in pulse width modulation (PWM) inverter drives, it is possible to have a huge current ripple in the DC bus).
3. The DC bus capacitor acts as a storage element for the regenerative energy from the motor. If the drive design utilizes diode bridge rectifiers, the regenerative energy cannot be fed back to the source and the absence of a proper DC bus capacitor may cause high-voltage buildup in the DC link during regeneration. This high-voltage buildup leads to a voltage breakdown of the semiconductors.

Capacitor design to limit the DC bus voltage ripple to 10%

The AC input supply specification is 230 V, 50 Hz. For a 10% DC voltage ripple the peak-to-peak DC voltage ripple is ΔV_{DC} = 32.5 V. Therefore, at the 230-V AC input, the DC bus voltage has a maximum value of 325 V and a minimum value of 292.5 V.

The discharge time of the capacitor can be calculated by equating the instantaneous AC input voltage to the minimum value of the DC bus voltage ripple, as Equation 1 shows.

$$v_m \sin \theta = 292.5 \quad (1)$$

where

- v_m is the amplitude of the AC input voltage

Substituting V_m = 325 in Equation 1 results in 325 sin θ = 292.5, which leads to θ = 1.1198 rad. Therefore, the total electrical angle during the capacitor discharging period is: $\theta_{discharge}$ = (π / 2) + 1.1198 = 2.69056 rad. The electrical angle can be expressed in terms of the angular electrical frequency (ω) and time (t) as Equation 2 shows:

$$\theta = \omega t \quad (2)$$

However, ω relates to the electrical frequency (f) in Equation 3:

$$\omega = 2\pi f \quad (3)$$

For a 50-Hz AC supply, ω = 2π × 50 = 314.16 rad/s; therefore, the discharge time of the capacitor is:

$$t_{discharge} = \frac{\theta_{discharge}}{\omega} = 8.56 \text{ ms}$$

The average DC bus voltage is V_{DC_ACVG} = 325 – (ΔV_{DC} / 2) = 308.75 V.

The average DC link current at 250 W is $I_{DC} = \frac{P_{DC}}{V_{DC\_AVG}} = \frac{250}{308.75} = 0.81$ A; therefore, the required capacitance value, C, can be calculated by the following Equation 4:

$$C \geq I_{DC} \times \frac{\Delta t}{\Delta V_{DC}} \quad (4)$$

where

- $\Delta t = t_{discharge}$ = 8.56 ms

By substituting the values of I_{DC}, Δt, and ΔV_{DC} in Equation 4, the user can obtain the value for the required DC bus capacitor C ≥ 214 µF.

Selection of the capacitor for the reference design

The TIDA-00472 design has software implementation to compensate the DC bus-voltage ripple. The algorithm for compensating the DC-bus voltage ripple allows a reduction of the DC bus capacitor value, which reduces the system size and cost. This reference design uses a 150-µF capacitor, which is a 30% reduced capacitor in comparison to the capacitor value calculated using Equation 4:

$$C_{compensated} = 0.7 \times C = 0.7 \times 214 = 150 \ \mu F \quad (5)$$

The user must also select the ripple current capacity of the capacitor. The application is a BLDC motor, which the three-phase inverter drives using trapezoidal control. In trapezoidal control, the DC link current has a huge current ripple during commutation in the motor. The DC bus capacitors must be able to handle this ripple current.

This application uses a 150-µF, 400-V electrolytic capacitor with a 1-A ripple capacity.

4.1.2 Selection of Bridge Rectifier

The voltage rating of the diode bridge rectifier must be sufficient to withstand the peak inverse voltage at 265-V AC. If a DC link choke is not used, the peak current drawn by the bulk electrolytic capacitors can be as high as 6 A at a rated input power of 250 W. This reference design uses a 1000-V, 8-A full bridge rectifier.

4.2 Three-Phase Inverter

The three-phase inverter is designed to operate from the rectified 230-V AC mains. Figure 3 shows the schematic of the three-phase inverter using discrete IGBTs. The PCB layout and minimum trace length for the power section routing is critical to minimize the switching voltage spikes across the IGBTs. Furthermore, placing the local decoupling capacitors close to each leg of the inverter is possible to minimize the voltage spikes. C25, C26, and C27 are provided for decoupling and are placed very close to each leg of the inverter (see Figure 3).

The resistor R39 is used to sense the DC bus return current. The filter network consists of C33, R43, and R44 and is used as a high-frequency differential filter. The terminal block J4 is used to connect the three-phase motor terminals.

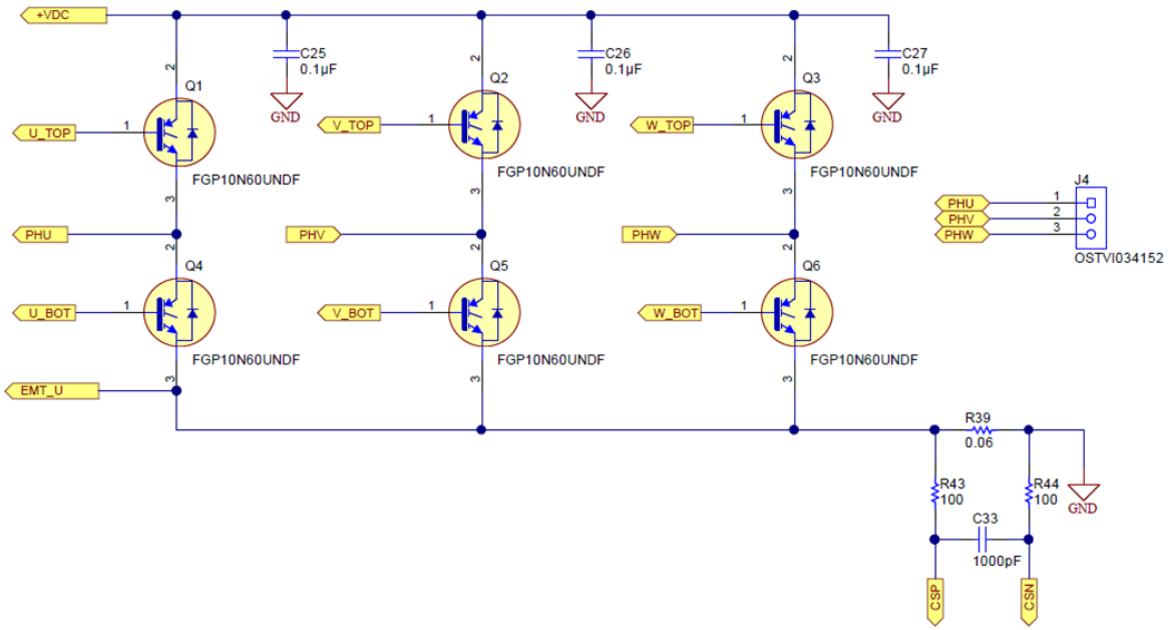


Figure 3. Three-Phase Inverter of Power Stage

4.2.1 Selection of Switching Device

The three-phase inverter is designed to operate from the rectified 230-V AC mains. The board is designed for a 230-V AC input ±15%; therefore, the peak DC bus voltage at the maximum AC input is 375-V DC (V_{DC_MAX} = 230 × 1.15 × √2 = 375 V). A switching device with a voltage rating that is 1½ times the maximum input voltage can be selected, considering the safety factor and switching spikes. A switch rated for 600 V is a suitable choice.

The current rating of the switching device depends on the peak winding current. The peak current in the motor winding depends on the motor parameters, motor rated torque, motor back-electromotive force (BEMF) profile, and so forth. In trapezoidal control (rectangular winding current), one winding of the motor is energized for two-thirds of the total electrical cycle period. For a rectangular winding current having two-thirds of the duration, the RMS and peak values relate as Equation 6 shows:

$$I_{RMS} = \sqrt{\frac{2}{3}} \times I_{PEAK} \quad (6)$$

From the specification of the motor used for testing this reference design, the RMS winding current at a rated load is 1.2 A. For an ideal rectangular current waveform, the peak current is calculated by using Equation 6, which gives I_{PEAK} = 1.47 A.

If a current control is not used, the winding current waveform cannot have a flat rectangular shape. The winding current has current ripple due to switching, which depends on the motor inductance and switching frequency. Small peak currents develop near the commutation because of the BEMF profile. Considering these factors (with a 120% overload), a peak current of 2.1 A in the motor winding can be assumed, which means that the overcurrent limit can be set to 2.1 A.

Keeping the current limit to a lower value limits the torque capability of the drive. The switching device must be rated for this current at the maximum operating junction temperature (T_J).

Assuming a safety factor of 2, the current rating of the switching device, $I_{SW} \geq 2 \times 2.1 = 4.2$ A, at T_J = 125°C; therefore, a switch with a current rating of 5 A at T_J = 125°C is a reasonable choice.

Another aspect for selecting the switching device is the switching frequency. This reference design uses a switching frequency of 20 KHz. An IGBT or MOSFET can be used in this case, based on the cost and total loss. This reference design uses a 600-V, 10-A IGBT for the inverter stage.

4.2.2 Selection of Sense Resistor

The sense resistor is used at the return path of the DC link to measure the motor winding current. During trapezoidal control of the BLDC motors, only two phases are ON at a time, which means that the DC link current is the same as the winding current. This relationship means that the user can implement different current or torque control strategies by sensing only the DC bus current. The operational amplifier OPA374 is configured as a differential amplifier to sense the DC bus return current. The power dissipation in the sense resistor is one of the major factors to consider during the selection process. A high resistance value leads to high power loss in the resistor and a very low value may reduce the available signal level (which reduces the noise immunity). This reference design uses a sense resistor followed by a differential amplifier of gain 20 and the internal comparator of a MSP430F5132 MCU to implement cycle-by-cycle control of the winding current. The reference terminal of the comparator is fed from an internal programmable reference with a setting of 2.5 V. Use Equation 7 to calculate the required sense resistor value.

$$V_{COMP\_REF} = (I_{OC} \times R_{SENSE}) \times A_{GAIN} \quad (7)$$

where

- V_{COMP_REF} is the comparator reference voltage
- A_{GAIN} is the gain of the differential amplifier
- R_{SENSE} is the sense resistor value
- I_{OC} is the overcurrent limit

To obtain an overcurrent limit I_{OC} = 2.1 A with A_{GAIN} = 20 and V_{COMP_REF} = 2.5 using Equation 7, the required R_{SENSE} must be equal to 0.06 Ω. The following Equation 8 calculates the power loss in the resistor.

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 2.1^2 \times 0.06 = 0.265 \text{ W} \quad (8)$$

A standard 2-W, 2512 package resistor can be used in this TI Design.

4.2.3 Inverter Loss Calculation

In trapezoidal control, every switch conducts for 120° in an electrical cycle. In every case, only two switches are ON, one from the high side and the other from the low side. The diode-rectified DC bus voltage is a constant with a stable 230-V AC input system. To control the average voltage applied to the motor, the pulse-width modulation (PWM) technique can be used. PWM can be used to modulate either the high side switch, low side switch, or both during this 120° conduction period. In this design, only the top side IGBTs are PWM modulated to control the voltage applied to the motor winding and the bottom side IGBTs are continuously ON for their respective 120° conduction period. This strategy reduces the switching loss from the bottom IGBTs.

The inverter losses are calculated at a 250-W output power from the inverter. Use the specifications in Table 2 to calculate the inverter losses.

Table 2. Parameters for Calculating Inverter Loss

PARAMETER	VALUE
Rated voltage of the motor (V_{M_RATED})	220 V
Nominal RMS motor current (I_{RMS})	1.2 A
Average DC bus voltage (V_{DC_AVG})	300 V
Average DC bus current (I_{DC_AVG})	0.9 A
Rated RPM	3000
Number of poles in the motor (p)	8
Motor electrical frequency at rated RPM (f_{ele})	200 Hz

4.2.3.1 Power Loss in Low Side IGBT

Conduction Loss

The user can calculate the IGBT conduction losses by using an approximate equivalent circuit that consists of a series connection of a voltage source (V_{CE0}), representing the ON-state, zero-current, collector-emitter voltage drop and the dynamic collector-emitter ON state resistance (r_c).

Figure 4 shows the typical output characteristics of an IGBT at a particular gate-to-emitter voltage (V_{GE}) and case temperature. A linear interpolation is done on the output characteristics to derive the equivalent circuit equation that the following Figure 4 shows.

$$V_{CE} = V_{CE0} + r_C \times I_{C,RMS} \quad (9)$$

where

- r_c is the equivalent dynamic resistance of the IGBT (slope of the output characteristics)
- $I_{C,RMS}$ is the RMS value of the switch current during 120° switch conduction period
- $I_{C,AVG}$ is the average switch current during 120° switch conduction period

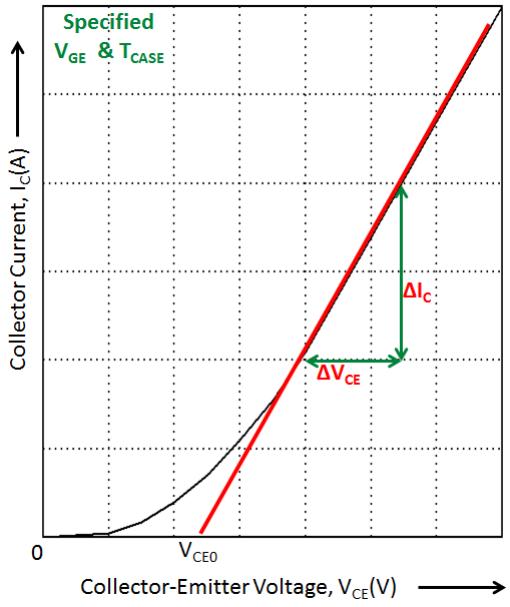


Figure 4. Modeling of IGBT for Loss Calculation

For an ideal rectangular current waveform, the RMS and average switch current during the 120° switch conduction period can be calculated in the following Equation 10 by using Equation 6:

$$I_{C,AVG} \approx I_{C,RMS} = \sqrt{\frac{3}{2}} \times I_{RMS} = 1.47 \text{ A} \quad (10)$$

Based on the above values and by using Figure 4, the conduction loss (P_C) of an IGBT can be expressed as Equation 11 shows.

$$P_C = (V_{CE0} \times I_{C,AVG}) + (r_C \times I^2_{C,RMS}) \quad (11)$$

In BLDC trapezoidal control, one switch conducts for 120°, which is one third of the total electrical cycle. Equation 12 calculates the conduction loss in one lower IGBT:

$$P_{CL} = \frac{1}{3} \times ((V_{CE0} \times I_{C,AVG}) + (r_C \times I^2_{C,RMS})) \quad (12)$$

From the output characteristics of the IGBT used in the reference design, at a case temperature of 125°C, Equation 13 shows the approximate values of the loss modeling parameters:

$$V_{CE0} \approx 1 \text{ V}$$
$$r_C \approx 0.2 \ \Omega \quad (13)$$

From the values established in Equation 13, calculate the conduction loss in one lower IGBT using Equation 14:

$$P_{CL} = \frac{1}{3} \times \left((1 \times 1.47) + \left(0.2 \times 1.47^2\right)\right) \approx 0.634 \text{ W} \quad (14)$$

Switching loss

The low side switches do not utilize PWM switching and are continuously ON for the 120° interval; however, the low side switch commutates at the motor electrical frequency.

The following Equation 15 shows the motor electrical frequency at the rated RPM:

$$f_{ele} = \frac{\text{Number of pole pairs} \times \text{RPM}}{60} = \frac{4 \times 3000}{60} = 200 \text{ Hz} \quad (15)$$

The following Equation 16 calculates the switching loss in a single, low-side IGBT:

$$P_{SWL} = f_{ele} \times (E_{ON} + E_{OFF}) \quad (16)$$

The IGBT datasheet specifies the following parameters for calculating the switching loss required to turn on and turn off the IGBT:

- Turn ON switching loss, E_{ON} = 0.22 mJ, when tested at V_{CC} = 400 V, I_C = 10 A, R_G = 10 Ω, and V_{GE} = 15 V
- Turn OFF switching loss, E_{OFF} = 0.08 mJ, when tested at V_{CC} = 400 V, I_C = 10 A, R_G = 10 Ω, and V_{GE} = 15 V

In the TIDA-00472 design, V_{GE} is equal to 15 V and the peak winding current I_{PK} is equal to 2.1 A.

Equation 17 calculates the low-side IGBT switching loss:

$$P_{SWL} = (E_{ON} + E_{OFF}) \times \left(\frac{V_{NOM} \times I_{PK}}{V_{CC(test)} \times I_{C(test)}}\right) \times f_{ele}$$
$$P_{SWL} = (0.22 + 0.08) \times \left(\frac{325 \times 2.1}{400 \times 10}\right) \times 200 = 0.01 \text{ W} \quad (17)$$

Equation 18 calculates the total loss on a single low-side IGBT:

$$P_L = P_{CL} + P_{SWL}$$
$$P_L = 0.634 + 0.01 \approx 0.65 \text{ W} \quad (18)$$

4.2.3.2 Power Loss in High-Side IGBT

Conduction Loss

The PWM is applied to high side switches. The user must consider the duty cycle of the PWM when estimating the conduction loss in the high-side IGBT

- The average DC bus voltage, V_{DC_AVG} = 300 V
- The average motor winding voltage at a rated load = 220 V (rated voltage of the motor)
- At a rated load, the PWM duty cycle, D = 220 / 300 = 0.733

Considering the preceding values, Equation 19 calculates the conduction loss in one high-side IGBT:

$$P_{CH} = \frac{1}{3} \times D \times \left(\left(V_{CE0} \times I_{C,AVG} \right) + \left(r_C \times I^2_{C,RMS} \right) \right)$$

$$P_{CH} = \frac{1}{3} \times 0.733 \times \left(\left(1 \times 1.47 \right) + \left(0.2 \times 1.47^2 \right) \right) \approx 0.465 \text{ W} \quad (19)$$

Switching loss

In the TIDA-00472 reference design, the high-side IGBT switches at 20 KHz and Equation 20 calculates the switching loss:

$$P_{SWH} = \frac{1}{3} \times (E_{ON} + E_{OFF}) \times \left(\frac{V_{NOM} \times I_{PK}}{V_{CC(test)} \times I_{C(test)}} \right) \times f_{SW}$$

$$P_{SWH} = \frac{1}{3} \times (0.22 + 0.08) \times \left(\frac{325 \times 2.1}{400 \times 10} \right) \times 20 \text{ k} \approx 0.341 \text{ W} \quad (20)$$

Equation 21 calculates the total loss on a single high-side IGBT:

$$P_H = P_{CH} + P_{SWH}$$

$$P_H = 0.465 + 0.341 \approx 0.81 \text{ W} \quad (21)$$

4.2.3.3 Diode Losses

Diode losses because of PWM switching

When the top IGBT turns off during PWM switching, the motor current is transferred to the antiparallel diode of the lower IGBT. Calculate the lower diode losses based on Equation 22.

$$P_{DIODE,SW} = \left(\frac{1}{3} \times (1 - D) \times V_F \times I_{F,AVG} \right) + \left(f_{SW} \times E_{DIODE} \right)$$

where

- E_{DIODE} is the reverse recovery switching losses in the diode
- V_F is the forward voltage drop in the diode
- $I_{F,AVG}$ is the average diode forward current (22)

Excluding the reverse recovery switching loss in the diode, Equation 22 can be simplified as in Equation 23.

$$P_{DIODE,SW} = \left(\frac{1}{3} \times (1 - D) \times V_F \times I_{F,AVG} \right)$$

$$P_{DIODE,SW} = \frac{1}{3} \times (1 - 0.73) \times 1.1 \times 1.47 = 0.143 \text{ W} \quad (23)$$

The diode loss calculated in the preceding Equation 23 is for the low-side diodes.

Diode losses because of phase commutation

During commutation, the motor winding current freewheels through the antiparallel diode of the complimentary IGBT. For example, if the top IGBT is commutating, then the winding current that was flowing through the top IGBT is transferred to the antiparallel diode of the lower IGBT. Six commutations occur in one electrical cycle of the motor current waveform. The commutation period can be defined as the duration in which the winding current of the commutation phase reduces to zero. The commutation period depends on the motor inductance and the peak winding current, which means the commutation period varies from motor to motor.

The BLDC motor used in this design has an approximate commutation time of about 100 µs at the rated load.

The commutation time, $T_{commutation}$, is approximately 100 µs.

Equation 24 shows the electrical frequency of the motor winding current for an 8-pole motor running at 3000 RPM:

$$f_{elec} = \frac{3000 \times 8}{120} = 200 \text{ Hz} \quad (24)$$

Because six commutations occur in one electrical cycle, the total diode loss because of phase commutation can be calculated as Equation 25 shows:

$$P_{DIODE,COMM} \approx 6 \times V_F \times I_{F,AVG} \times T_{commutation} \times f_{ele} \quad (25)$$

where

- V_F is the diode forward voltage drop
- $I_{F,avg}$ is the average forward current of the diode during commutation

During commutation, the current in the commutating phase reduces from the peak value to zero. In the application design, the peak winding current is 2.1 A, from which the user can derive the average forward current of the diode during commutation using the following Equation 26:

$$I_{F,avg} = \frac{2.1}{2} = 1.05 \text{ A} \quad (26)$$

From the device datasheet, the $V_{F,avg}$ is approximately 1.1 V at a diode junction temperature of 125ºC and at a forward current of 2.1 A.

Substitute the values in Equation 25 to obtain the total diode loss because of phase commutation in Equation 27:

$$P_{DIODE,COMM} \approx 6 \times 1.1 \times 1.05 \times 100 \text{ µs} \times 200 \text{ Hz} = 0.1386 \text{ W} \quad (27)$$

Equation 28 simplifies the total diode loss:

$$P_{DIODE} = \left(3 \times P_{DIODE,SW}\right) + P_{DIODE,COMM} = 0.57 \quad (28)$$

Total loss in the three-phase inverter

Equation 29 shows the total loss in the three-phase inverter.

$$P_{LOSS} = 3 \times (P_L + P_H) + P_{DIODE}$$

$$P_{LOSS} = 3\left(0.65 + 0.81\right) + 0.57 \approx 5 \text{ W} \quad (29)$$

4.2.4 Thermal Design for Three-Phase Inverter

The inverter is designed to operate without a heat sink and supports up to 65ºC ambient. The selected IGBTs have a thermal resistance from junction-to-ambient of 62.5ºC/W. One switch package has an IGBT and the antiparallel diode.

From the loss calculation that the previous subsection outlines, calculate the total loss in a high-side IGBT and antiparallel diode in Equation 30:

$$\text{Total loss in high-side IGBT and antiparallel diode} = P_H + \left(\frac{P_{DIODE,COMM}}{6}\right) = 0.83 \text{ W} \quad (30)$$

Use the preceding Equation 30 to calculate the temperature rise in the high-side switch in Equation 31:

$$\text{Temperature rise in high-side switch} = 0.83 \times 62.5 \approx 52^{\circ}\text{C} \tag{31}$$

From the loss calculation that the previous subsection outlines, calculate the total loss in a low-side IGBT and antiparallel diode in Equation 32:

$$\text{Total loss in low-side IGBT and antiparallel diode} = P_H + P_{DIODE,L} + \left(\frac{P_{DIODE,COMM}}{6}\right) = 0.81\ \text{W} \tag{32}$$

Use the preceding Equation 32 to calculate the temperature rise in the low-side switch in Equation 33:

$$\text{Temperature rise in low-side switch} = 0.81 \times 62.5 \approx 50^{\circ}\text{C} \tag{33}$$

4.3 Gate Driver Using UCC27714

The gate driver UCC27714 has the following features that makes the device suitable for this application:

- High-side low-side configuration with independent inputs
- Fully operational up to 600 V (HS pin)
- Floating channel designed for bootstrap operation
- Peak output current capability of a 4-A sink and source at VDD = 15 V
- Best-in-class propagation delay (90 ns typically, 125 ns max)
- Best-in-class delay matching (20 ns max)
- TTL and CMOS compatible logic input thresholds Independent of supply voltage with hysteresis
- VDD bias supply range of 10 V to 20 V
- Undervoltage lockout (UVLO) protection feature on the supply circuit blocks between VDD and VSS pins, as well as between HB and HS pins; the rail-to-rail drive with outputs is held low when inputs are floating
- Robust operation under negative voltage transients (logic operational up to –8 V on HS pin for VDD = 12 V); parasitic inductance in the circuit can cause negative voltage at HS relative to COM, which can cause a logic error on HO if the driver cannot handle the negative voltage of HS
- Separated grounds for logic (VSS) and driver (COM) with the capability to sustain voltage difference
- Optional enable function EN pin

4.3.1 Gate Drive Circuit Design

Figure 5 shows the circuit diagram for a half-bridge gate drive using the UCC27714 device.

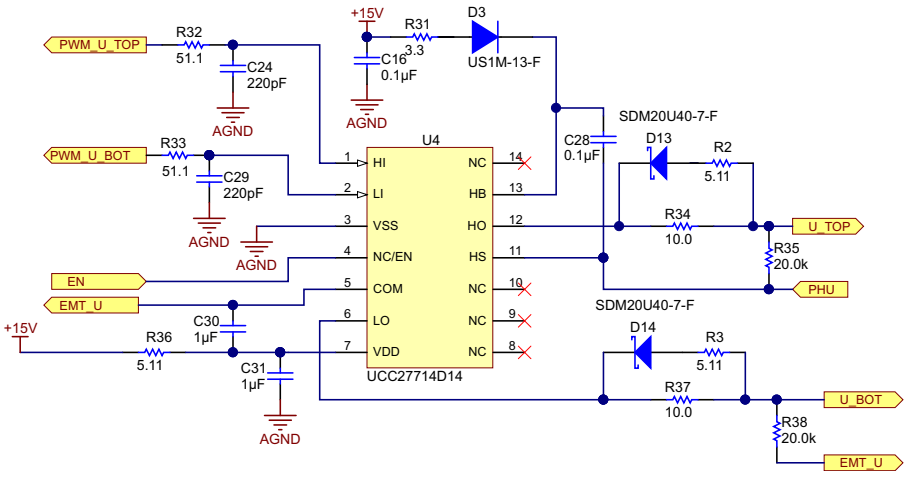


Figure 5. Gate Driver Circuit Using UCC27714

Selecting HI and LI low-pass filter components

To filter the high-frequency noise, the designer must add an RC filter between the PWM controller and the input pin of the UCC27714 device. The recommended value of the RC filter is R32 = R33 = 51 Ω and C24 = C29 = 220 pF.

Selecting bootstrap capacitor (C_{BOOT})

The bootstrap capacitor must be sized to have more than enough energy to drive the gate of the IGBT high without depleting the bootstrap capacitor more than 10%. A good guideline is to size C_{BOOT} to be at least ten times as large as the equivalent IGBT gate capacitance (C_g).

C_g must be calculated based on the voltage driving the high side gate of the IGBT (V_{GE}) and the gate charge of the IGBT (Q_g). V_{GE} is approximately the bias voltage supplied to V_{DD} after subtracting the forward voltage drop of the bootstrap diode D3 (V_{DBOOT}). In this design example, the estimated V_{GE} is approximately 14.4 V, as Equation 34 shows.

$$V_{GE} \approx V_{DD} - V_{DBOOT} = 15\ V - 0.6\ V = 14.4\ V \tag{34}$$

The IGBT in this reference design has a specified Q_g of 37 nC. The equivalent gate capacitance of the IGBT can be calculated as Equation 35 shows.

$$C_g = \frac{Q_g}{V_{GE}} = \frac{37\ nC}{14.4} \approx 2.6\ nF \tag{35}$$

After estimating the value for C_g, C_{BOOT} must be sized to at least ten times larger than C_g, as Equation 36 shows.

$$C_{BOOT} \geq 10 \times C_g = 26\ nF \tag{36}$$

For this reference design, a 100-nF capacitor has been chosen for the bootstrap capacitor, as Equation 37 shows.

$$C_{BOOT} = C28 = 100\ nF \tag{37}$$

Selecting V_{DD} bypass holdup capacitor (C_{VDD}), and R_{BIAS}

The V_{DD} capacitor (C_{VDD}) must be chosen to be at least ten times larger than C_{BOOT}. For this reference design, a 1-µF capacitor has been selected (see Equation 38). C31 is the V_{DD} capacitor.

$$C_{VDD} \geq 10 \times C_{BOOT} = 1\ \mu F \tag{38}$$

TI recommends selecting a 5-Ω resistor R_{BIAS} series with bias supply and V_{DD} pin to increase the V_{DD} ramp-up time to larger than 50 µs. The preceding Figure 5 shows how the resistor R36 is used as the R_{BIAS} resistor.

Estimating the bootstrap diode power dissipation (P_{DBOOT})

Estimate the bootstrap diode power dissipation (P_{DBOOT}) based on the switching frequency, diode forward voltage drop, and the switching frequency of the gate driver (f_{SW}). In this reference design, the switching frequency has been set to 20 KHz. Equation 39 calculates the estimated power loss for the bootstrap diode.

$$P_{DBOOT} = \frac{1}{2} \times Q_g \times f_{sw} \times V_{DBOOT} = \frac{1}{2} \times 37\ nC \times 20\ KHz \times 0.6\ V \approx 0.22\ mW \tag{39}$$

Selecting the current limiting resistor for the bootstrap diode (R_{BOOT})

Select the resistor R_{BOOT} to limit the current in D_{BOOT} and limit the ramp-up slew rate of the voltage across the HB and HS pin. TI recommends selecting an R_{BOOT} resistor between 2 Ω and 10 Ω when using the UCC27714 gate driver. This TIDA-00472 reference design uses a current-limiting resistor of 3.3 Ω. The peak bootstrap diode current ($I_{DBOOTPK}$) is limited to approximately 4.36 A (see).

$$R_{BOOT} = R31 = 3.3\ \Omega$$

$$I_{DBOOT\_PK} = \frac{VDD - V_{DBOOT}}{R_{BOOT}} = \frac{15\ V - 0.6\ V}{3.3\ \Omega} \approx 4.36\ A \tag{40}$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the bootstrap capacitor. This energy is equivalent to ½ × C_{BOOT} × V^2. This energy is also dissipated during the charging time of the bootstrap capacitor (approximately 3 × R_{BOOT} × C_{BOOT}).

The TIDA-00472 reference design uses a 3.3-Ω, 0.125-W resistor.

Selecting the bootstrap diode

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case a maximum of 375-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor to the 15-V VDD supply.

The diode must be able to carry a pulsed peak current of 4.36 A. However, the average current is much smaller and depends on the switching frequency and the gate charge requirement of the high side IGBT.

This TIDA-00472 reference design uses a 1000-V, 1-A, fast recovery diode.

Selecting the gate resistor R_{HO} and R_{LO}

The gate resistors are sized to reduce the ringing caused by parasitic inductances and capacitances and to limit the output source and sink current of the gate driver.

From the datasheet of UCC27714 (SLUSBY6):

LO and HO output pulldown resistance, R_{HOL} = R_{LOL} = 1.45 Ω

LO and HO output pullup resistance, R_{HOH} = R_{LOH} = 3.75 Ω

The TIDA-00472 reference design uses different gate resistors in the turnon and turnoff path of the IGBT. The external gate resistors used are listed below. The external gate resistance in the turnon path of the high side IGBT is R_{HO_ON} = R34 = 10 Ω.

The parallel combination of the resistors R2 and R34 form the turn OFF equivalent resistance:

- The external gate resistance in the turnoff path of the high side IGBT, R_{HO_OFF} = 3.38 Ω (10 Ω and 5.11 Ω in parallel)
- The external gate resistance in the turnon path of the low side IGBT, R_{LO_ON} = R37 = 10 Ω
- The external gate resistance in the turnoff path of low side IGBT, R_{LO_OFF} = 3.38 Ω (R3 and R37 in parallel)

The following Equation 41 calculates the maximum HO drive current (I_{HO_DR}):

$$I_{HO\_DR} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_ON} - R_{HOH}} = \frac{15\ V - 0.6\ V}{10\ \Omega + 3.75\ \Omega} \approx 1.05\ A \quad (41)$$

The following Equation 42 calculates the maximum HO sink current (I_{HO_SK}):

$$I_{HO\_SK} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_OFF} - R_{HOL}} = \frac{15\ V - 0.6\ V}{3.38\ \Omega + 1.45\ \Omega} \approx 3\ A \quad (42)$$

The following Equation 43 calculates the maximum LO drive current (I_{LO_DR}):

$$I_{LO\_DR} = \frac{V_{DD}}{R_{LO\_ON} - R_{LOH}} = \frac{15\ V}{10\ \Omega + 3.75\ \Omega} \approx 1.09\ A \quad (43)$$

The following Equation 44 calculates the maximum LO sink current (I_{LO_SK}):

$$I_{LO\_SK} = \frac{V_{DD}}{R_{LO\_OFF} - R_{LOL}} = \frac{15\ V}{3.38\ \Omega + 1.45\ \Omega} \approx 3\ A \quad (44)$$

4.3.2 Estimating UCC27714 Power Losses (PUCC27714)

Estimate the power losses of UCC27714 ($P_{UCC27714}$) by calculating the losses from several components.

The static power losses because of quiescent current (I_{QDD}, I_{QBS}) are calculated in Equation 45:

$$P_{QC} = V_{VDD} \times (I_{QDD} + I_{QBS}) \tag{45}$$

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required for the power device (usually a function of the drive voltage V_G, which is very close to the input bias supply voltage V_{DD} because of the low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

To turn on an IGBT, the gate driver must provide the sufficient gate charge. Equation 46 calculates the energy required to supply the gate charge:

$$E_G = \frac{1}{2} \times Q_G \times V_{GE}$$

where

- V_{GE} is the gate voltage supplied by the gate driver across the gate and emitter of the IGBT (46)

If the IGBT is switching at a frequency f_{SW}, then the gate power supplied by the gate driver when the IGBT turns on is calculated in Equation 47:

$$P_{G\_ON} = \frac{1}{2} \times Q_G \times V_{GE} \times f_{SW} \tag{47}$$

The same energy also dissipates when the IGBT turns off; therefore, the total gate power required to turn on and turn off one IGBT is calculated in the following Equation 48:

$$P_G = Q_G \times V_{GE} \times f_{SW} \tag{48}$$

In the TIDA-00472 reference design, only the upper IGBT is switched using PWM. The lower IGBT remains on for 120º electrical. Both the upper and lower IGBTs remain on for only one third of the electrical cycle. Equation 49 calculates the gate power required to turn on and turn off the upper IGBT:

$$P_{GH} = \frac{1}{3} \times Q_G \times V_{GE} \times f_{SW} \tag{49}$$

The gate power required to turn on and turn off the lower IGBT can be calculated based on the electrical frequency of the inverter output voltage and current. The lower IGBT switches on and off once during every electrical frequency. The electrical frequency of the motor winding voltage at 3000 RPM for an 8-pole motor is 200 Hz. Equation 50 shows the calculation of the gate power required to turn on and turn off the lower IGBT:

$$P_{GL} = Q_G \times V_{GE} \times f_{ele} \tag{50}$$

Equation 51 calculates the total power loss in a single UCC27714 device:

$$P_{UCC27714} \approx (V_{DD} \times (I_{QDD} + I_{QBS})) + \left(\frac{1}{3} \times Q_G \times V_{GE} \times f_{SW}\right) + (Q_G \times V_{GE} \times f_{ele})$$

$$P_{UCC27714} \approx (15\ V \times (750\ \mu A + 120\ \mu A)) + \left(\frac{1}{3} \times 37\ nC \times 15\ V \times 20000\ Hz\right) + (37\ nC \times 15\ V \times 200\ Hz) = 13.4\ mW \tag{51}$$

When external resistors are used in the gate drive circuit, a portion of this power loss is incurred on these external resistors and the power loss in UCC27714 is lower, allowing the device to run at lower temperatures.

The TIDA-00472 design utilizes three gate drivers, so the total power loss of the gate drive is 40.2 mW.

NOTE: The application schematic in Figure 5 shows 20-kΩ resistors across the gate and emitter terminals of the IGBTs. These resistors are a safety precaution and are placed across these nodes to ensure that the IGBTs are not turned on if the UCC27714 device is not in place or not properly soldered to the circuit board.

If using a shunt resistor between the COM and VSS pins, then bypass this pin to COM with a 1-uF surface mount device (SMD) capacitor. The TIDA-00472 reference design uses C30 (1 µF) for this purpose.

4.4 Voltage and Current Feedback

4.4.1 Motor-Winding Voltage Feedback

The motor winding voltages are fed back to the controller for sensorless control implementation. In the firmware, phase voltages are measured directly from the motor phases instead of a software estimate. The firmware works on the back electro-motive force (BEMF) integration technique. The algorithm derives the motor BEMF by sensing the winding voltages of the non-energized phase. The measured winding voltage overrides on half of the DC bus voltage (V_{DC} / 2) during the PWM ON time of the energized phases. Therefore, the BEMF is derived by subtracting (V_{DC} / 2) from the sensed winding voltages. The algorithm assumes the same scaling in the winding voltage and DC bus voltage (V_{DC}) sensing network. Therefore, maintaining the exact same scaling configuration for the BEMF voltage-sensing circuits and V_{DC} sensing circuit is important.

The winding voltages switch at a maximum voltage equal to the DC bus voltage, which can be a maximum of 375 V. Because of this high voltage, a proper scaling network is required before feeding the motor winding voltage to the controller, as Figure 6 shows.

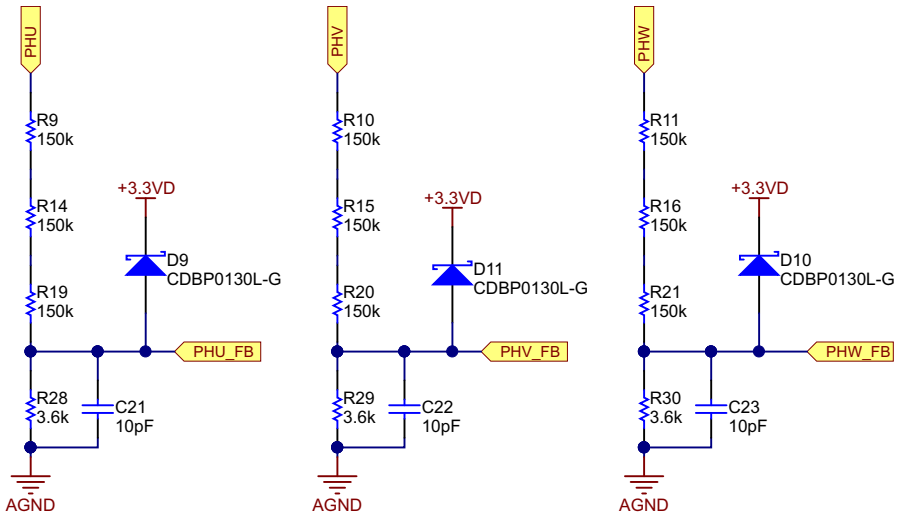


Figure 6. Motor-Winding Voltage Sensing

The maximum voltage that can be fed to the ADC terminals of the MSP430 device is 3.3 V. The maximum voltage applied to the motor terminals (V_M) is equal to the maximum available DC bus voltage V_{DC_MAX} (see Equation 52)

$$V_{DC\_MAX} = (230 + 15\%)\ V \times \sqrt{2} = 375\ V \quad (52)$$

With the established value of the maximum available DC bus voltage, consider a one-phase voltage sensing network. Equation 53 calculates the ADC input voltage to the MSP430 device (V_{ADC}):

$$V_{ADC} = V_M \times \frac{R28}{R9 + R14 + R19 + R28}$$

$$V_M = V_{ADC} \times \frac{R9 + R14 + R19 + R28}{R28}$$

$$V_M = 3.3 \times \frac{150 + 150 + 150 + 3.6}{3.6} = 416 \text{ V} \quad (53)$$

Considering a 10% headroom for this value, the maximum voltage input to the system is recommended to be 416 × 0.9 ≈ 375 V; for a motor with a maximum operating DC voltage of 375 V, this voltage feedback resistor divider is ideal.

In the circuit shown in Figure 6, the diodes D9, D10, and D11 are used as a protection clamp diode.

4.4.2 DC-Bus Voltage Feedback

Figure 7 shows the DC-bus voltage-sensing circuit. The resistors R8, R13, R18, and R27 have been selected with high values to reduce the standby current of the board. D12 is used as a protection clamp diode.

The resistors R8, R13, and R18 are designed to bring down the voltage across R27 to a maximum of 3.3 V when the DC bus voltage is at the maximum, as Section 4.4.1 explains

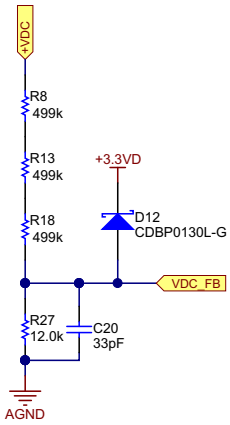


Figure 7. DC-Bus Voltage Sensing

The winding and DC-bus voltage lines are externally protected using ESD devices, as Figure 8 shows. The TPD1E10B06 diode is used for ESD protection. The TPD1E10B06 is a single-channel, ESD, transient-voltage-suppression (TVS) diode, which offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support.

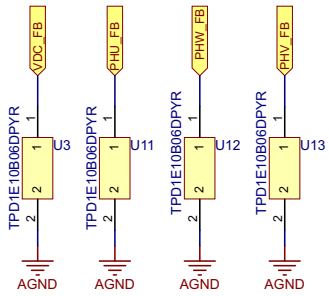


Figure 8. ESD Protection on Voltage Sensing Lines

4.4.3 Current Sense Amplifier

The low–power, high-bandwidth OPA374 op amp is used as a differential amplifier with a gain of 20 for current sensing. Two resistor-capacitor (RC) filters are provided at the output of the OPA374 op amp. The output of the first RC filter (R52 and C39) is fed to the ADC pin of the MCU to implement any current or torque control algorithm. The second RC filter (R57 and C42) is fed to the comparator input of the MSP430 MCU to implement the cycle-by-cycle current limit. The user can set a different cut-off frequency for torque control or overcurrent protection by changing the corresponding RC values. Figure 9 shows a schematic of the current sense amplifier using the OPA374 device.

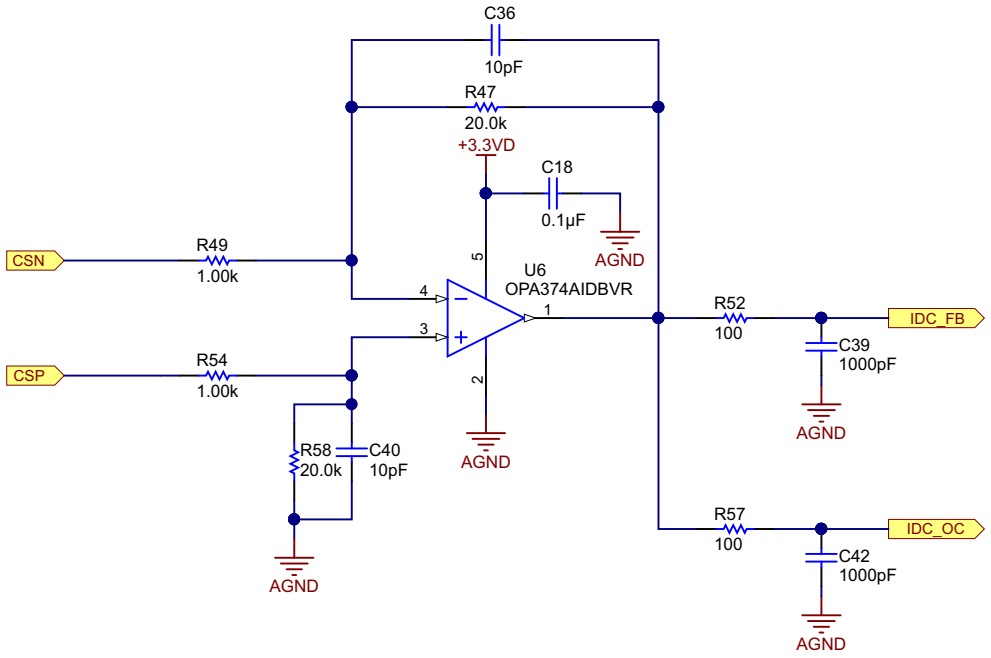


Figure 9. Current Sense Amplifier Using OPA374

4.5 MSP430F5132 Schematic

Figure 10 shows the schematic for configuring the MSP430F5132 MCU. The MSP430 MCU generates a core supply voltage, which is internally regulated and denoted as VCORE. A suitable decoupling capacitor must be connected to the VCORE pin. The datasheet recommends using a decoupling capacitor with a value of 470 nF (SLAS619). A capacitor tolerance of ±20% or better is required. The VCORE pin is only for internal device usage. Do not apply any external DC load or voltage to this pin.

The datasheet specifies a capacitor ratio of 10 between the DVCC (digital power supply) and VCORE pins. TI recommends using a 4.7-µF capacitor (minimum) at the DVCC pin. The TIDA-00472 reference design uses a 10-µF capacitor at the DVCC pin. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency. The same 10- and 0.1-µF decoupling capacitors are provided at the digital IO power supply pin (DVIO) and analog power supply pin (AVCC).

The Timer_D of the MCU is used for PWM generation. The TD1.0 instance of the MCU and the corresponding pins are mapped to the high-side switch PWM. The TIDA-00472 reference design uses unipolar, trapezoidal BLDC control with only the high side switches switching at a high frequency. The low side switches switch at the electrical frequency of the motor current, which is much lower. Gate control of the lower IGBTs is possible using the general purpose input and output (GPIO) pins of the MCU. All of the feedback voltages including the DC bus voltage, three winding voltages, current sense amplifier output, potentiometer voltage, and temperature sensor output are interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU. The provision in the schematic is provided for the universal asynchronous receiver/transmitter (UART) interface, as well (see Figure 10).

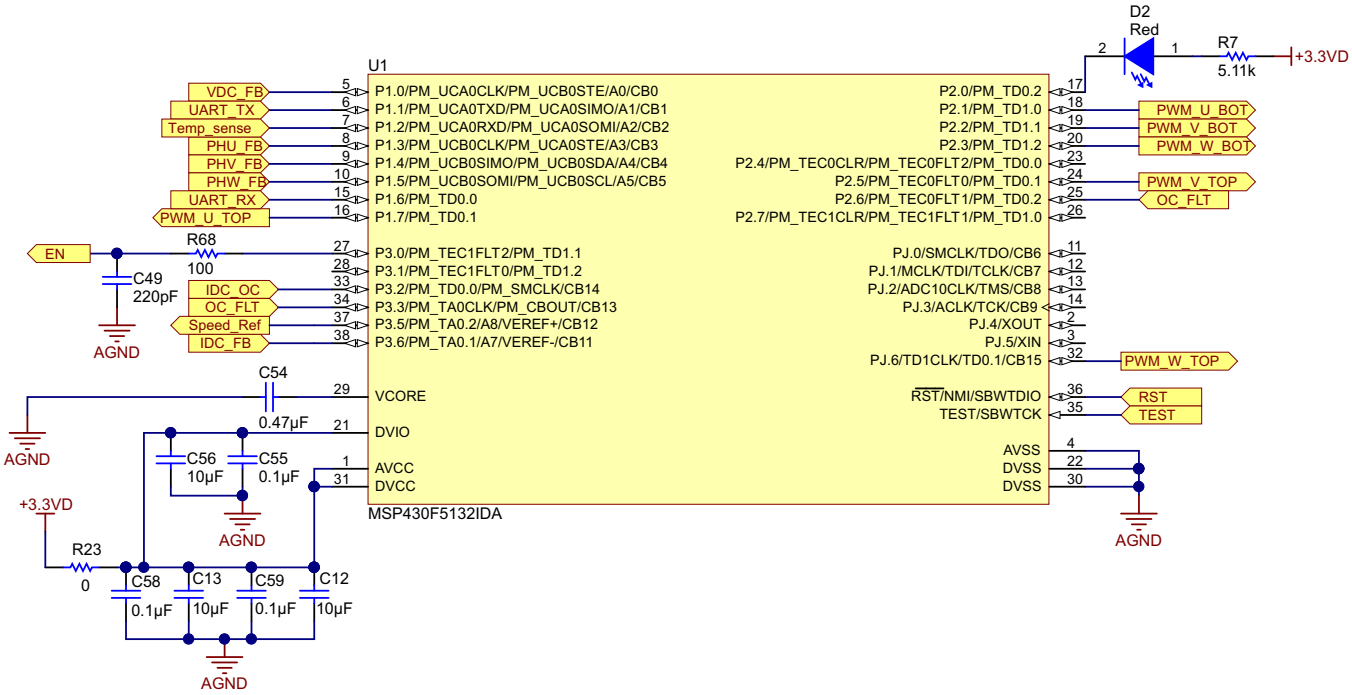


Figure 10. MSP430F5132 Schematic

4.6 DC-Bus Ripple Compensation

In the TIDA-00472 reference design, the three-phase inverter is driven by the AC-DC converter working from the 230-V, 50/60-Hz mains power. The DC bus capacitor has been generally designed to meet the DC-bus voltage ripple within 5% to 10%. The three-phase inverter requires a stiff DC bus with an ideal zero voltage ripple to obtain the best performance from the inverter and the motor. Any ripple in the DC bus voltage can cause distorted current waveforms in the motor winding. The distorted current in the motor winding generates torque ripple in the motor, which leads to vibration and noise in the motor including the attached mechanical load and systems. For a stable performance, implement a control algorithm that is capable of compensating for the DC-bus voltage ripple and providing a stable current to the motor.

Capacitors that have been designed for 5% or 10% ripple are typically bulky and costly. Reducing the capacitance value may help to reduce the overall size and cost of the system, but doing so increases the DC-bus voltage ripple, creates torque ripple, and deteriorates the system performance.

The TIDA-00472 reference design shows the performance of the board with a capacitor value reduced by 30% in comparison to the capacitor required for 10% voltage ripple.

This reference design also shows the implementation of an algorithm for DC-bus ripple compensation to compensate the voltage ripple and provide a motor winding current that is stable.

The DC bus voltage feedforward control is used in this design to provide ripple voltage compensation. This control ensures that the voltage applied to the motor is constant at any time. If $V_{DC}(t)$ is the instantaneous DC bus voltage and D is the PWM duty cycle, then the effective voltage available to the motor (V_{MOTOR}) is calculated in Equation 54:

$$V_{MOTOR} = D \times V_{DC}(t) \quad (54)$$

When powering with an AC supply, if V_{DC_AVG} is the average voltage available at the DC bus, then the average voltage applied to the motor is calculated in Equation 55:

$$V_{MOTOR} = D \times V_{DC\_AVG} \quad (55)$$

However, the DC bus has ripple over the V_{DC_AVG}. To make the voltage applied to the motor constant at any time, the designer must modulate the duty cycle by a feedforward gain factor so that the product of the $V_{DC}(t)$ and duty cycle is a constant (see Equation 56).

$$\text{Feed forward gain} = \frac{V_{DC\_AVG}}{V_{DC}(t)} \tag{56}$$

Figure 11 shows the DC-bus voltage ripple compensation using the feedforward control.

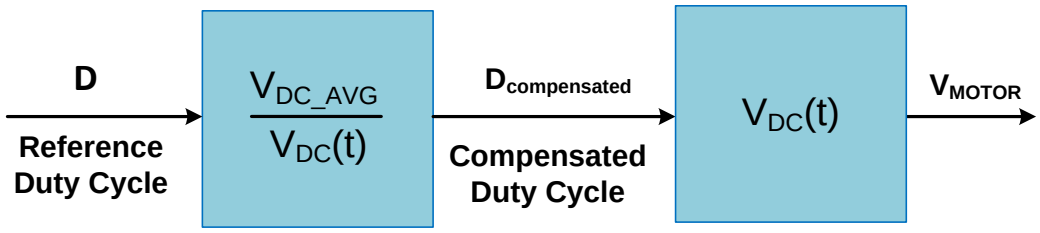


Figure 11. DC-Bus Voltage Ripple Compensation

The input D is the duty cycle command from the speed control loop or the reference duty cycle. The compensated duty cycle, $D_{compensated}$, can be expressed as Equation 57 shows.

$$D_{compensated} = D \times \left(\frac{V_{DC\_AVG}}{V_{DC}(t)} \right) \tag{57}$$

From Figure 11, the voltage across motor winding V_{MOTOR} can be expressed as Equation 58.

$$V_{MOTOR} = D_{compensated} \times V_{DC}(t) = D \times \left(\frac{V_{DC\_AVG}}{V_{DC}(t)} \right) \times V_{DC}(t) = D \times V_{DC\_AVG} \tag{58}$$

Equation 58 shows that with the compensated duty cycle (at any DC bus voltage $V_{DC}(t)$), the voltage applied across the motor winding is a constant and is equal to the reference duty cycle multiplied by the average DC bus voltage.

4.7 Overcurrent Protection Using MSP430F5132

The MSP430F5132 MCU has an integrated comparator and timer event control module, which can be configured to implement the current limit.

4.7.1 Comparator_B

The comparator_B (Comp_B) is an analog voltage comparator and features the following:

- Inverting and non-inverting terminal input multiplexer
- Software-selectable RC filter for the comparator output
- Interrupt capability
- Selectable reference voltage generator, voltage hysteresis generator
- Ultralow-power comparator mode

The comparator compares the analog voltages at the non-inverting (+) and inverting (–) input terminals. If the non-inverting terminal is more positive than the inverting terminal, the comparator output CBOUT is high. The comparator can be switched ON or OFF using the control bit CBON.

The output of the comparator can be used with or without internal filtering. When the control bit CBF is set, the output is filtered with an on-chip RC filter. The delay of the filter can be adjusted in four different steps. Selecting the output filter can reduce errors associated with comparator oscillation.

The comparator features a high-precision reference voltage level, low offset voltage, and high speed.

The CBRSEL (reference select) bit in the CBCTL2 register can be configured to obtain different thresholds. The reference voltages available are 1.5 V, 2.0 V, and 2.5 V. Refer to Section 4.2.2 for further details on the relationship between the overcurrent limit and reference voltage.

4.7.2 Timer Event Control Module

The Timer Event Control (TEC) module is the interface between the timer modules and the external events. The TEC and Timer_D modules are connected through internal signals. The TEC module contains the control registers to configure the routing between the timer modules. The TEC module also has the enable register bits, interrupt enable, and interrupt flags for external event inputs.

The TEC module features include:

- Enabling of internal and external clear signals
- Routing of internal signals (between Timer_D instances) and external clear signals
- Support of external fault input signals
- Interrupt vector generation of external fault and clear signals
- Generating feedback signals to the timer capture and compare channels to affect the timer outputs

In the TIDA-00472 reference design, the COMPB module and TEC module are used together for current limit operation. The output of the current sense amplifier is connected to the non-inverting terminal of the comparator through the input channel 14 (CB14), as Figure 10 shows. The inverting input of the comparator is internally connected to the programmable voltage reference. The output of the comparator CBOUT is externally routed to the external fault event pin TECxFLT1 of the TEC module.

Whenever the current sense amplifier output exceeds the voltage reference of the comparator, the output CBOUT and TECxFLT1 goes high, which initiates an event in the TEC module. The TEC module is programmed to disable the Timer_D output PWM during this event. This programmed function means that CBOUT goes high when the motor hits an overcurrent condition and can disable the Timer_D output (as Figure 12 shows) if CBOUT is connected to a TECxFLT input pin. When CBOUT goes low, the Timer_D output is then allowed to resume normal operation.

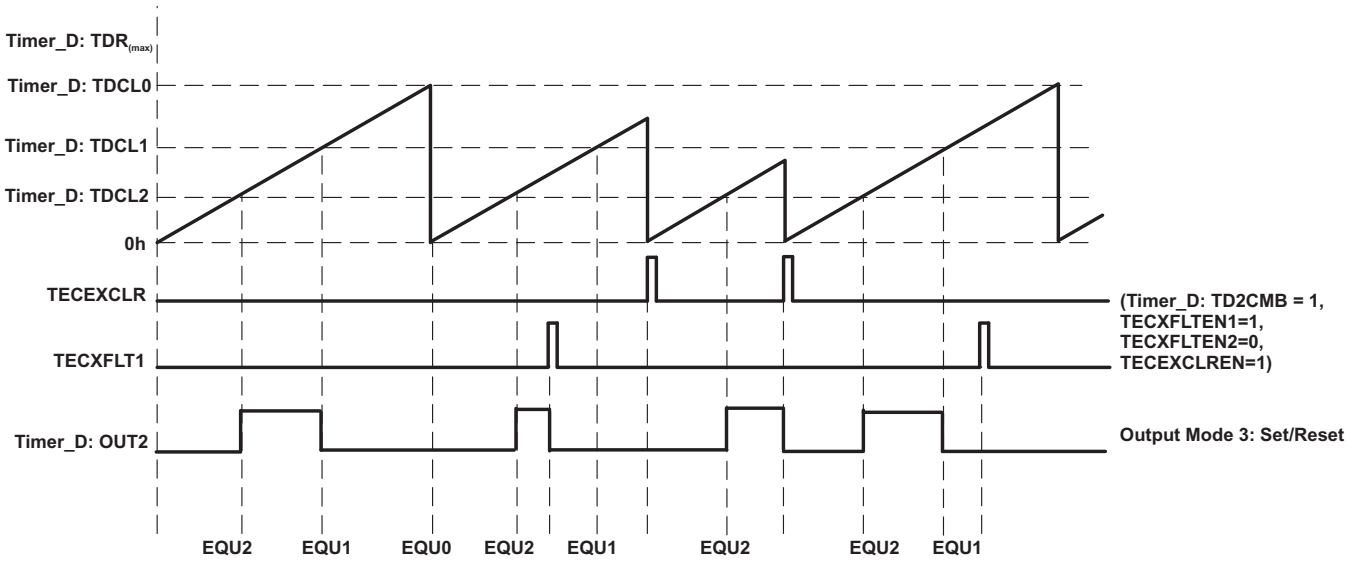


Figure 12. External Input Events Reseting Timer_D Output

NOTE: Ensure that the timer is configured in SET/RESET mode, so that during the external event, the Timer_D resets and causes the PWM output pin to go low.

4.8 3.3-V Power Supply Using LDO TLV70433

The ultralow quiescent current LDO TLV70433 is an ideal power-management device for applications where the lowest standby power consumption must be met. The following Figure 13 shows the schematic of the LDO circuit.

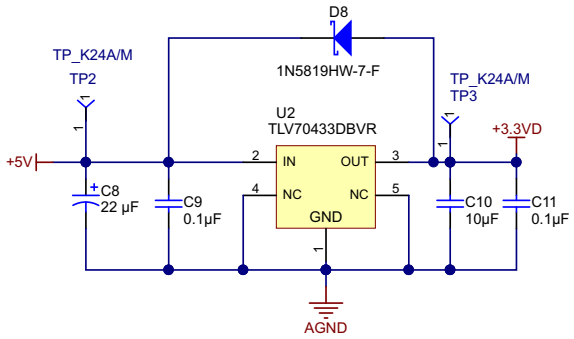


Figure 13. 3.3-V Power Supply Using LDO TLV70433

4.9 Heat Sink Temperature Sensor

Figure 14 shows the temperature sensor circuit that can be used to measure the heat sink temperature. The LMT87 is an analog output temperature sensor. The temperature sensing element comprises a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, which provides a low-impedance output source. The typical sensor gain is –13.6 mV/ºC.

Although the LMT87 is very linear, its response does have a slight umbrella parabolic shape. The output voltages at different temperatures are given in the datasheet of LMT87 in tabular form (SNIS170). For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range using the two-point equation of a line. Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

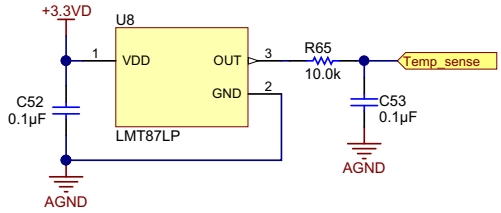


Figure 14. Heat Sink Temperature Sensor

4.10 Features and Controls Available in Board

4.10.1 Speed Control of Motor

As Figure 15 shows, a potentiometer has been provided to function as an optional speed input.

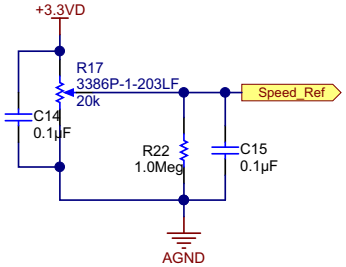


Figure 15. Potentiometer Connection for Speed Control

4.10.2 UART Communication

The TIDA-00472 board has a provision for an isolated UART interface. Figure 16 shows the schematic for this isolated UART interface. The designer can use this interface for communicating with the user interface (UI) to control the motor speed, turn the motor on and off, and so forth based on the commands received from the UI through the UART.

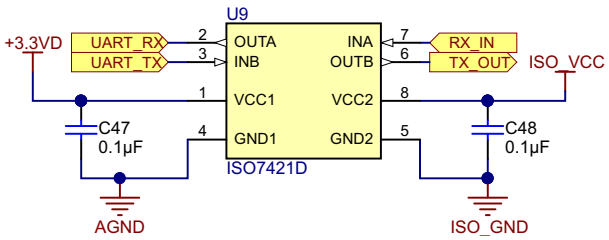


Figure 16. UART Isolated Interface

5 Getting Started Hardware

5.1 TIDA-00472 Connector Configuration

Figure 17 shows the TIDA-00472 connector configuration, which the following list details:

- **Three-pin connector J1**: This pin is used to connect the input AC supply. It has the terminals marked as L (Line), N (Neutral or Return), and PE (Earth).
- **Three-pin connector J4**: The terminals labeled MU, MV, and MW are used to connect the three-phase BLDC motor.
- **Two-pin connector J6**: This connector provides the rectified DC bus voltage. This connector can be used as an input to the external DC-DC auxiliary power supply board, which can generate the 5- and 15-V power supplies for operation of the TIDA-00472 PCB. The connector terminal labeled +VDC is the positive DC bus voltage and the return is labeled GND.
- **Three-pin connector J2**: This is the auxiliary power supply interface. For proper operation of the board, provide 15 V to pin number 1, 5 V to pin number 2, and ground reference (GND) to pin 3 following the terminal labels in Figure 17.
- **Four pin connector J3**: This is the programming connector for the MSP430F5132 MCU.
- **Four-pin connector J5**: This connector is used for the isolated UART interface.

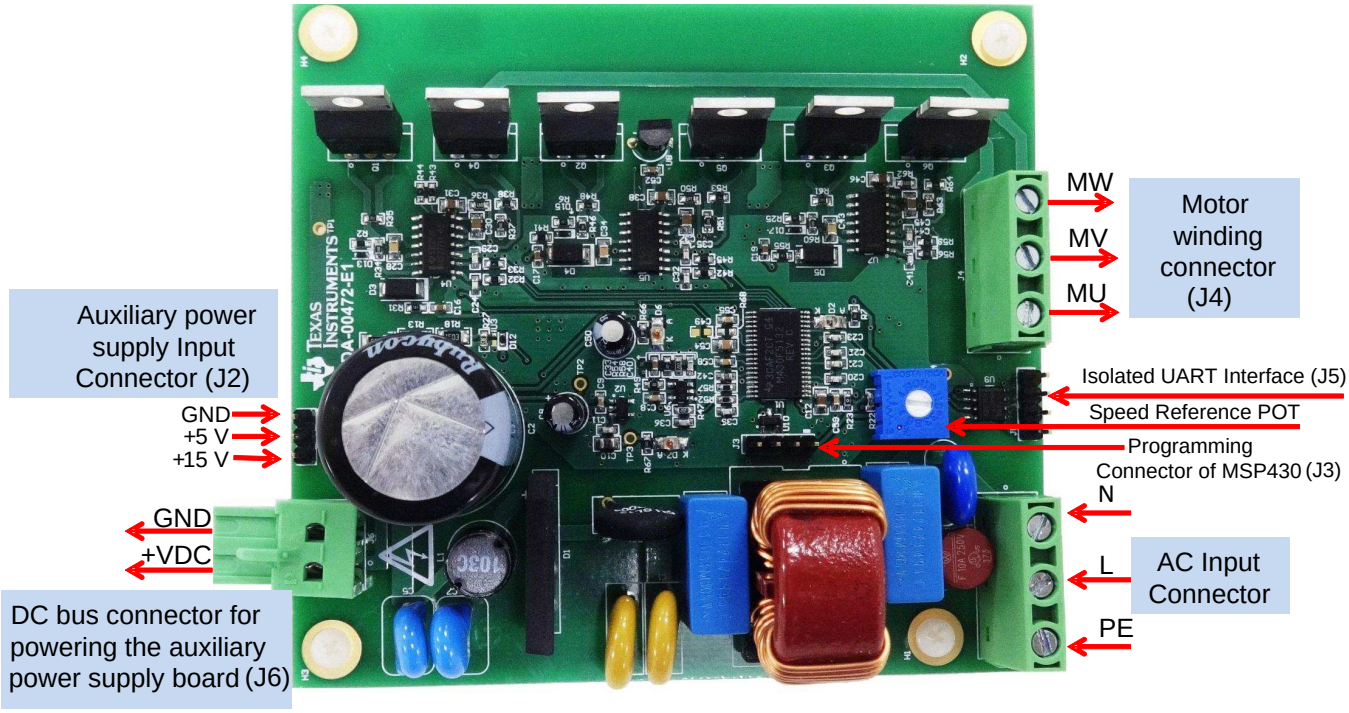


Figure 17. TIDA-00472 PCB Connectors

5.2 MSP430™ Programming

To program the MSP430F5132 MCU, the user can use the MSP-FET430UIF programming kit, which includes the MSP430 USB debugging interface. Programming the MSP430F5132 MCU also requires the use of TI's Code Composer Studio™ (CCS) software v5.5.

The MSP-FET430UIF flash emulation tool has a 14-pin JTAG connector. The two-wire Spy-Bi-Wire protocol is used to program the MSP430F5132 MCU. Figure 18 shows the four-pin programming connector provided in the TIDA-00472 board. The four-pin connector between the MSP-FET430UIF kit and MSP430F5132 MCU connects as Figure 19 shows.

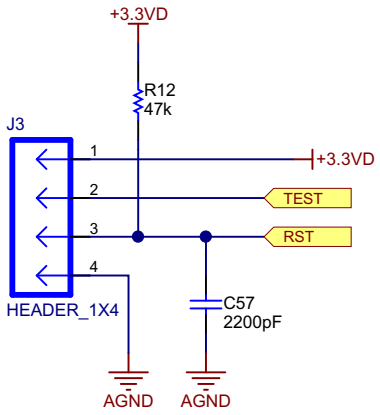


Figure 18. Four-Pin Programming Connector Provided in TIDA-00472 Board

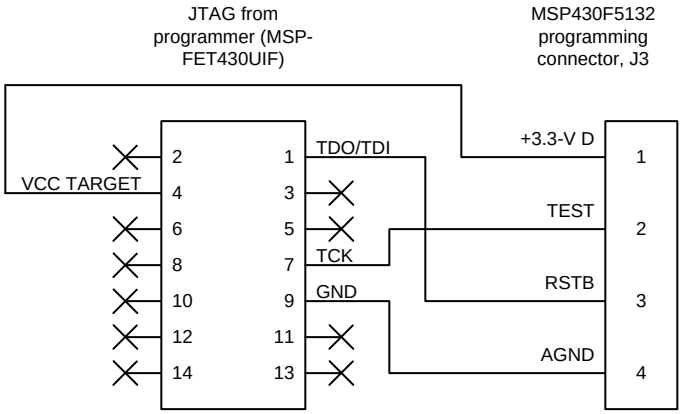


Figure 19. Programming Interface Between the Programmer Kit and MSP430F5132

The following list outlines the steps to program the MSP430F5132 MCU:

1. Switch off the mains input to the TIDA-00472 board. Wait for the DC bus voltage to ramp down to zero.
2. Power on the 5-V supply at connector J2.
3. After turning the 5-V supply on, connect the MSP430F5132 programming connector to the MSP-FET430UIF programmer.
4. Open the CCS software and then build and debug the code to program the MSP430F5132 MCU.

5.3 Board Bring-Up and Testing Procedure

The following list details the procedure for board bring-up and testing:

1. Connect the DC auxiliary power supply 15 V, 5 V, and GROUND reference of the external power supply to the connector J2. Ensure that the polarity of the connector is correct.
2. The power supply requirement from the auxiliary power supplies are 50 mA from 15 V and 50 mA from 5 V.
3. Turn on the auxiliary power supply and check the 15 V, 5 V, and 3.3 V generated in the board using a multimeter. The user can check the 3.3 V at the test point TP3.
4. If the power supply is correct, connect the programmer and program the code to the MCU. Ensure that the program is properly tuned as per the procedure in Section 6. TI recommends using a current-limited high-voltage DC source for tuning the software.
5. Turn off the auxiliary power supply and disconnect the programmer.
6. Connect the AC input terminals to J1 and connect the motor terminals to J4.
7. Ensure that the 15- and 5-V supply is off. Then turn on the AC source and slowly increase the input voltage using an auto transformer and observe the DC voltage. Note that until the software is tuned for the motor, TI recommends powering the board using an auto transformer with the necessary fuse protection or through a current-limited high-voltage DC source.
8. When the DC bus voltage is around 80 V, turn on the 15- and 5-V supplies and wait for the motor spin. The motor must start spinning within 5 s to 10 s.
9. Make sure the motor is running and then increase the input voltage further.
10. Refer to Section 6.1.1 when tuning the software to obtain the best performance by observing the motor current.
11. After properly tuning the software, start spinning and loading the motor at higher voltages.
12. Figure 20 shows the assembly of the boards TIDA-00472 and the auxiliary power supply TIDA-00473.

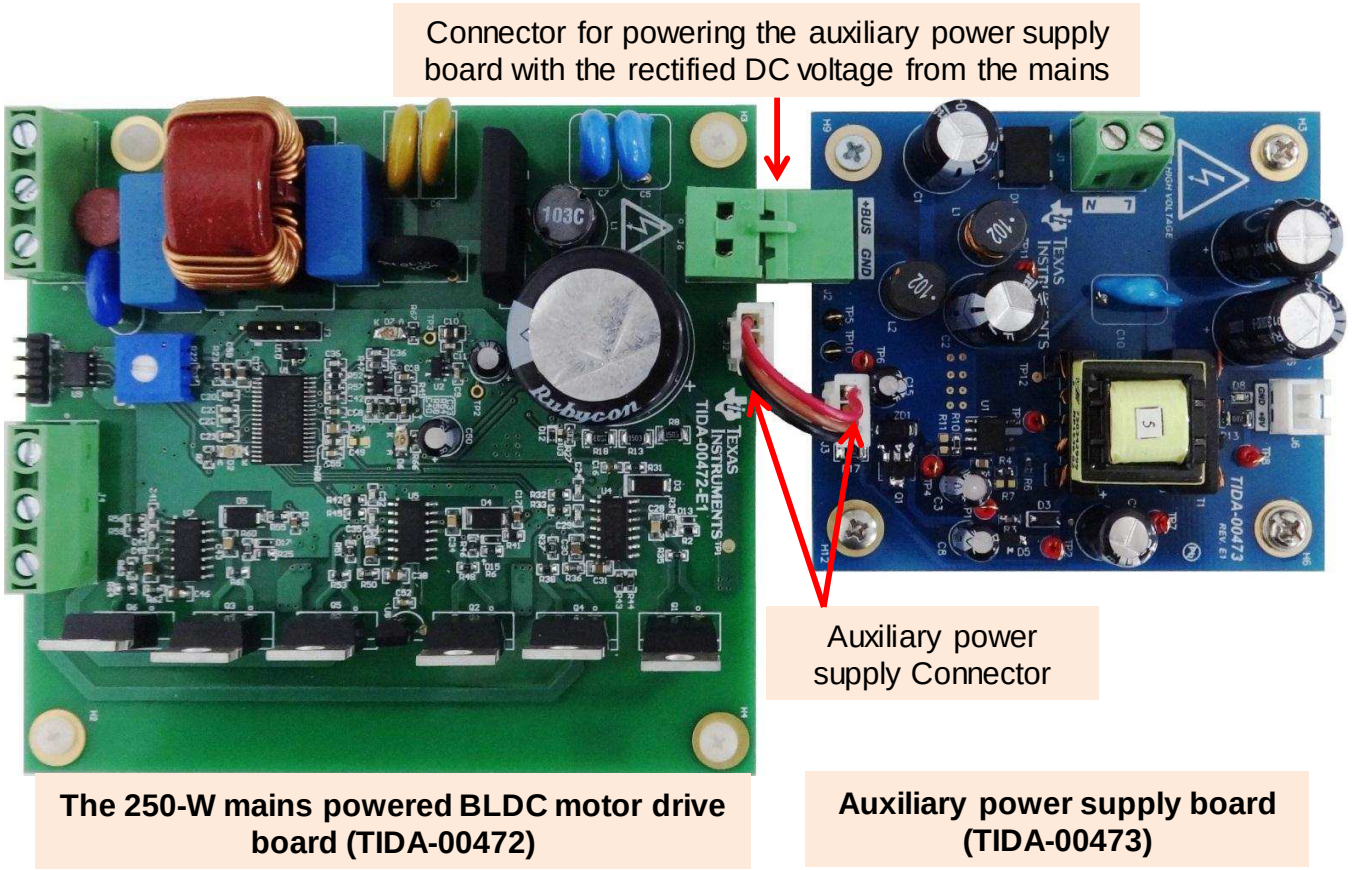


Figure 20. Interfacing TIDA-00472 and TIDA-00473

6 Getting Started Firmware

TI's InstaSPIN-BLDC solution is the core of this software implementation. The following subsection provides details for implementing an instaSPIN-BLDC solution and the subsequent Section 6.2 and Section 6.3 outline the complete implementation of the software.

6.1 InstaSPIN-BLDC

InstaSPIN-BLDC is one of TI's flagship motor control technologies that target cost-sensitive, sensorless BLDC applications. This sensorless technique uses traditional trapezoidal or 120º commutation and monitors motor flux by integrating the BEMF of the non-energized phase to determine the commutation instances. Figure 21 shows the BEMF integration area (red-shaded area). The commutation is done when the BEMF integrated value reaches the BEMF threshold set in the firmware. The BEMF threshold depends on the motor parameters (BEMF constant of the motor). Refer to Section 6.3 to understand how to set the BEMF threshold. For certain equipment types that do not require a fast, dynamic torque response, such as fans, pumps, blowers, and so forth, the implementation of InstaSPIN-BLDC is a sufficient option to meet low-cost requirements.

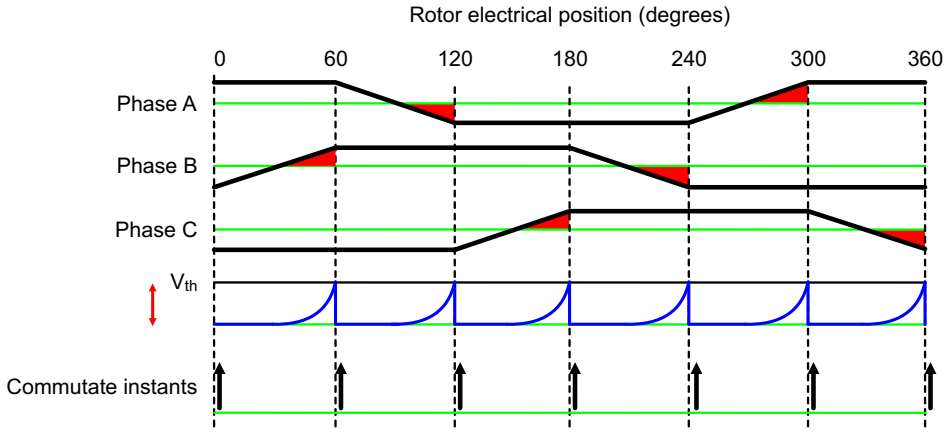


Figure 21. InstaSPIN-BLDC—BEMF Integration Method to Determine Commutation Instant

During trapezoidal control of a BLDC motor, for each 60º electrical, only two inverter legs are active and deliver the power to the motor while the third inverter leg is kept in a high-impedance state by switching OFF both high side and low side switches. In the case of a unipolar two-quadrant drive, PWM is applied only to the high side switch of one active leg while the low side switch of the other active leg remains ON continuously for one 60° electrical rotation.

The InstaSPIN-BLDC method requires precise sensing of the BEMF of the motor open phase to determine the commutation instant. As Figure 22 shows, for the 60° interval, PWM is applied only to the phase-A top switch. The phase-C bottom switch is continuously ON and the BEMF of open phase B is rising and can be measured and integrated to determine the commutation instant. During the ON-time of the PWM pulse, with the top switch of phase A connected to the VDC pin and the bottom switch of phase C connected to GND, the motor-neutral terminal potential rises to VDC / 2 with respect to the GND. The BEMF of phase B appears at the VDC / 2 level above GND. The designer can derive the actual value of the motor BEMF by capturing the absolute value of the voltage between phase B terminal and GND during the PWM ON-pulse and subtracting by VDC / 2.

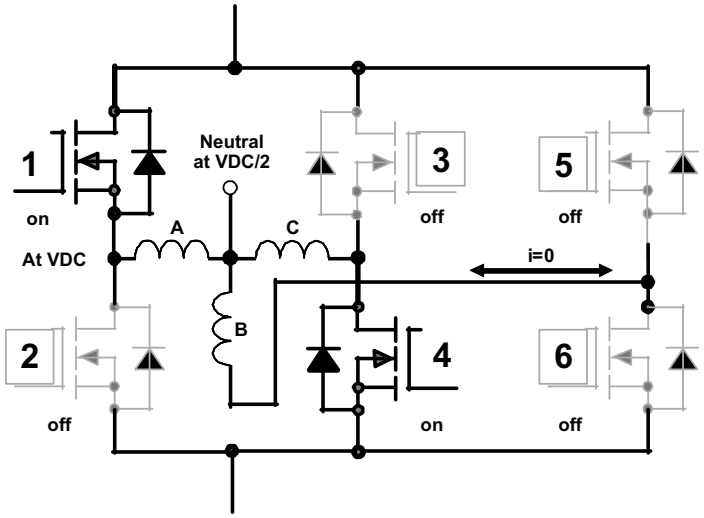


Figure 22. Motor Neutral voltage During PWM On-Period

6.1.1 Motor Tuning With Proper Flux Threshold

As Figure 21 shows, the commutation instance is derived by integrating the BEMF of the non-energized phase (obtained during each PWM on-pulse) and comparing the integrated value to a predefined threshold. The threshold is actually equivalent to the total flux of the motor and the total flux of the motor can be calculated by integrating the BEMF. The value of the flux threshold depends on the motor BEMF constant; therefore, this value must be tuned for each motor for proper commutation. An oscilloscope is typically used for the purposes of tuning to see the symmetry of the motor input voltages, motor phase current, or both. Refer to the following scope shots in Figure 23 and Figure 24 for the different flux threshold values. The scope shots show the motor input voltage and a current waveform for one phase.

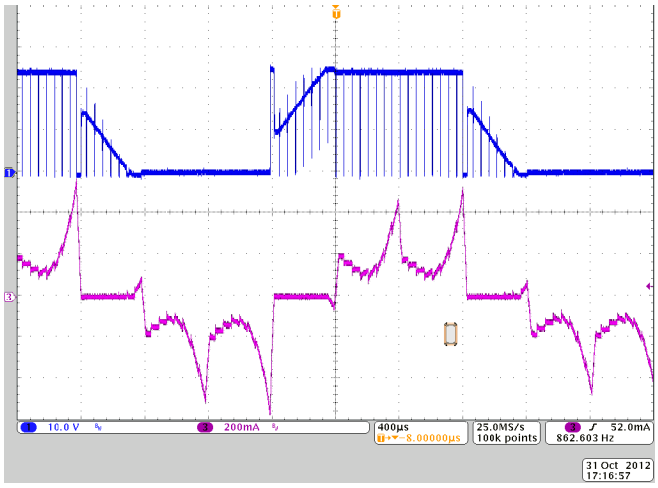


Figure 23. Typical Waveform for Higher Flux Threshold

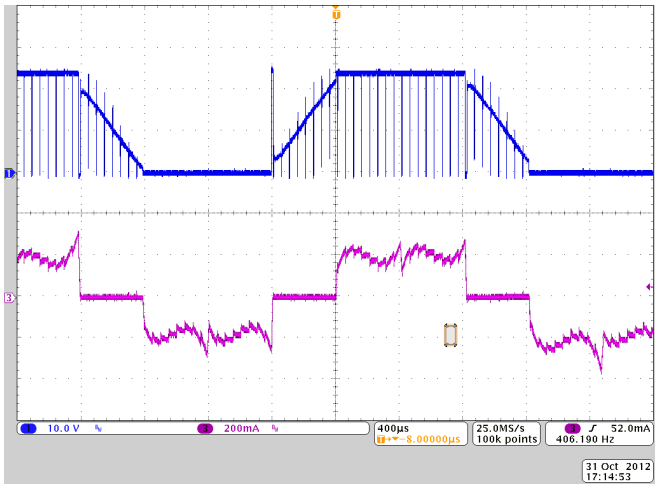


Figure 24. Typical Waveform for Optimum Flux Threshold

6.2 System Features

The TIDA-00472 firmware offers the following features and user controllable parameters:

- Trapezoidal sensorless control of BLDC motor using the BEMF integration method
- Open loop control to accelerate the motor to a certain speed so that there is sufficient BEMF for sensing and then moving to a closed loop control (which integrates the BEMF to commutate at the exact position)
- The sensorless control code is customizable based on the target motor
- Overcurrent protection using the internal comparator of the MSP430F5132 MCU

The following Table 3 shows the TIDA-00472 firmware system components.

Table 3. System Components

SYSTEM COMPONENT	SPECIFICATIONS
Development and emulation	TI's Code Composer Studio™ software v5.5
Target controller	MSP430F5132
PWM frequency	20-KHz PWM (default), programmable for higher and lower frequencies
PWM mode	Asymmetrical with no dead band
Interrupts	CPU Timer D1 – Implements 20-KHz ISR execution rate ADC interrupt
Peripherals used	TIMER D1.0 for motor control PWM ADC-A0 – DC-bus voltage sense ADC-A2 – Temperature sense ADC-A3, A4, A5 – Motor Winding voltage sensing (applicable for sensor- less control) ADC-A8 – Potentiometer voltage sensing for changing speed ADC-A7 – Current sense amplifier output COMP_B – Comparator for Current limit Protection (channel CB14) TEC0FLT1 – Overcurrent limit Fault input

6.3 Reference Code Customization

To modify the sensorless code, the end user must have CCS installed as well as the MSP430F5132 configuration files. The following section describes the different user-adjustable parameters and how to select an optimized value for a specific application.

1. Open CCS and load the reference project “TIDA-00472_sensorless_BLDC_V1.0”. Note that if this project is in a *.zip* or *.rar* compressed format, the user must extract this file.
2. Select the *config.h* file. Parameters exist at the top of the file that can be optimized and are included as the configuration variables. The following section of code in Figure 25 shows these parameters,

```
#define PWM_PERIOD          1251;      ///((25MHz/PWM Frequency)+1)
#define BEMF_THRESHOLD      300;  //Back EMF threshold
#define MAX_DUTYCYCLE       768 ; //relative to PWM_PERIOD
#define MIN_DUTYCYCLE       150 ; //relative to PWM_PERIOD
#define MAX_OPEN_LOOP_FREQ 7;    //
#define START_UP_DUTY       1;    //in percentage
#define START_UP_MAX_DUTY   4;    //in percentage
```

Figure 25. Code Section Showing Parameters

PWM_PERIOD

The PWM_PERIOD is used to set the value in capture and compare register 0 of Timer_D. Because Timer_D is used as the PWM generator, Timer_D is initialized to operate at 25 MHz; see the following Equation 59 for calculating the PWM frequency. The TIMER_D PWM is configured in *Up* mode.

$$\text{PWM frequency (Hz)} = \frac{25\ \text{MHz}}{(\text{PWM\_PERIOD} - 1)} \tag{59}$$

For example, a PWM_PERIOD = 1251 results in a PWM frequency as given in Equation 60:

$$\text{PWM frequency (Hz)} = \frac{25\ \text{MHz}}{(1251 - 1)} = 20\ \text{KHz} \tag{60}$$

MAX_DUTYCYCLE

The MAX_DUTY_CYCLE sets the maximum duty cycle available to the user. The duty cycle input command compares to the MAX_DUTY_CYCLE at every instance. If the duty cycle input command exceeds the MAX_DUTYCYCLE, the target duty cycle is set to the MAX_DUTYCYCLE. This number is relative to the PWM period.

MIN_DUTYCYCLE

The MIN_DUTYCYCLE sets the minimum duty cycle that can be applied to the motor.

BEMF_THRESHOLD

The BEMF_THRESHOLD is the only parameter that must be measured on the motor. Follow the below procedure for calculating this parameter:

1. Verify that the motor is not connected to the board.
2. Use an oscilloscope to capture the differential voltage waveform between any two phases.
3. Measure the amplitude and frequency of the BEMF (see Figure 26)
4. Calculate the BEMF constant (K_e) parameter using the following Equation 61. Note that the BEMF constant used is the phase to phase value.

$$\text{BEMF constant, } K_e \left(\frac{V}{Hz}\right) = \frac{\text{Amplitude (V)}}{\text{Frequency (Hz)}} \tag{61}$$

where

- T = Time period of the BEMF waveform
- Frequency (Hz) = 1 / T

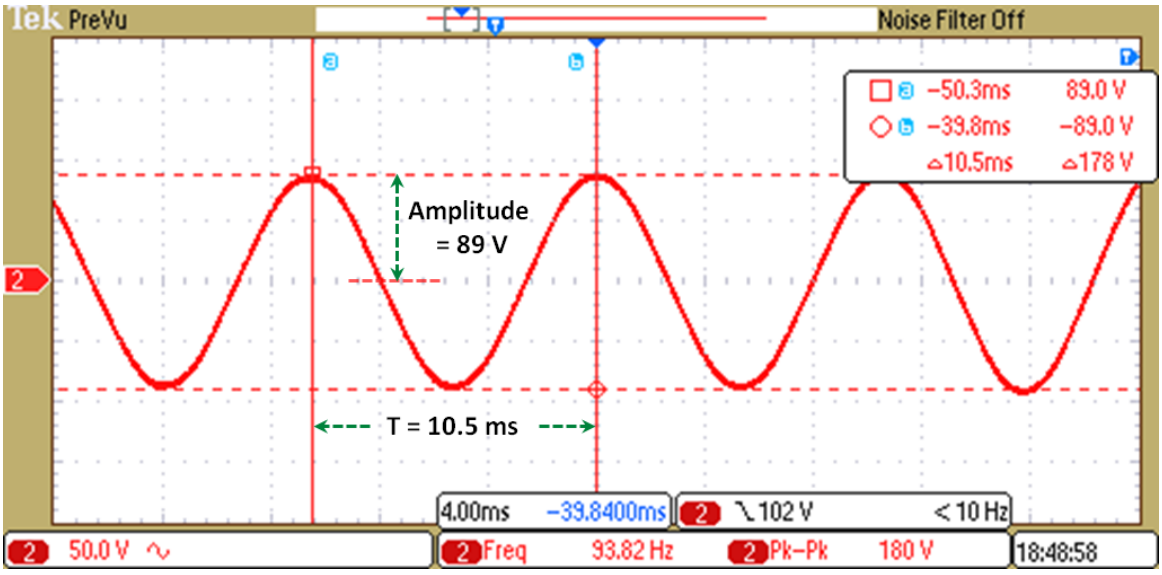


Figure 26. Example BEMF Waveform for Calculating K_e

Figure 27 shows the BEMF integration zones in the motor winding voltage waveform. The center tap voltage is V_{DC} / 2. The BEMF integration starts when the winding voltage of the non-switching phase (measured with respect to GND) crosses the center tap and continues until the integrated value reaches the BEMF threshold.

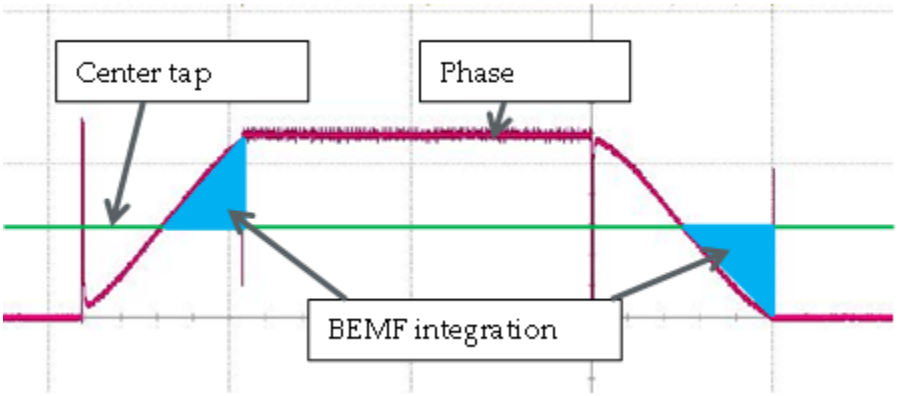


Figure 27. Phase Voltage Waveform Showing BEMF Integration Zone

Figure 28 explains how to calculate the BEMF threshold using the BEMF constant of the motor. The calculations are given in Equation 62 through Equation 69.

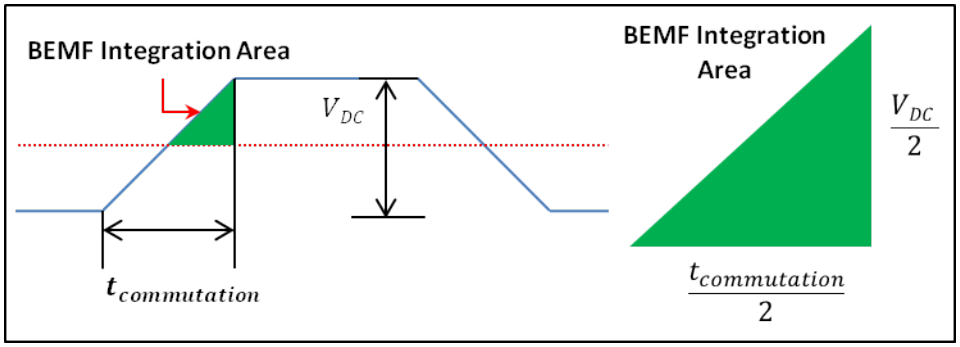


Figure 28. BEMF Integration Area

In the MCU, the ADC samples every PWM cycle. The PWM time period = (1 / PWM frequency) = 50 µs.

The full-scale output of a 10-bit ADC = 1023.

The full-scale analog input voltage to ADC = 3.3 V.

Therefore, the ADC reading for any motor winding voltage of V_M can be calculated in Equation 62 (refer to Figure 6):

$$\text{BEMF ADC reading} = \frac{V_M \times 3.6}{450 + 3.6} \times \frac{1023}{3.3} = 2.460317 \times V_M \quad (62)$$

From Figure 28, the maximum phase-to-phase BEMF (BEMF amplitude) can be V_{DC}. The $t_{commutation}$ is the time period between two commutation instances in Equation 63:

$$t_{commutation} = T / 6 \quad (63)$$

Using Equation 61, calculate the following Equation 64:

$$t_{commutation} = \frac{\text{BEMF constant}}{6 \times \text{BEMF amplitude}} = \frac{\text{BEMF constant}}{6 \times V_{DC}} \quad (64)$$

From Figure 28, calculate the following Equation 65:

$$\text{BEMF integration area} = \frac{1}{2} \times \frac{V_{DC}}{2} \times \frac{t_{commutation}}{2} \quad (65)$$

However, the ADC reads a scaled value of the BEMF, as defined in Equation 62; therefore, calculate the following Equation 66:

$$\text{Height of BEMF integration area after scaling} = \frac{V_{DC}}{2} \times 2.460317 \tag{66}$$

The ADC samples the BEMF in every PWM cycle. The PWM frequency is 20 KHz, which means the ADC is sampling the BEMF every 50 µs. The following Equation 67 calculates the number of ADC samples in a period of $t_{commutation}$ / 2:

$$\text{Number of ADC samples in a period of } \frac{t_{commutation}}{2} = \frac{t_{commutation}}{2 \times 50\ \mu s} \tag{67}$$

UsingEquation 66 and Equation 67, calculate the following Equation 68:

$$\text{Scaled software area} = \frac{1}{2} \times \frac{V_{DC}}{2} \times \frac{t_{commutation}}{2 \times 50\ \mu s} \times 2.460317 \tag{68}$$

Equating the scaled software area to the BEMF_THRESHOLD and substituting Equation 64 in Equation 68, the BEMF_THRESHOLD can be calculated using Equation 69:

$$\text{BEMF\_THRESHOLD} = \frac{\text{BEMF constant}\left(\frac{V}{Hz}\right) \times 2.460317}{6 \times 8 \times 50\ \mu s}$$

$$\text{BEMF\_THRESHOLD} = \text{BEMF constant}\left(\frac{V}{Hz}\right) \times 1025 \tag{69}$$

The parameter required in the reference code is a scaled version of the K_e expressed in V/Hz. To scale the K_e to the required BEMF_THRESHOLD value, multiply K_e by 1025. This value is the threshold of the integrated BEMF, which is measured from the center-tapped zero crossing by the ADC. If this number is not correct for the specific motor, the motor may not run as expected.

For phase advance control, this value can be adjusted as a lead angle adjustment. If the value is set lower than the measured number, the control commutates earlier. If the parameter is set greater than the calculated threshold, the commutation event is delayed.

NOTE: To further fine tune the BEMF threshold, refer to Section 6.1.1

START_UP_MAX_DUTY

The maximum start-up duty cycle is applied to align the motor to a particular position. During start-up the duty cycle is gradually increased from 1% to START_UP_DUTY_MAX (%) to complete the alignment of the motor to the start position. This number is in percentage.

MAX_OPEN_LOOP_FREQ

The MAX_OPEN_LOOP_FREQ value represents the maximum open-loop frequency of the motor before the motor is driven by the BEMF integration algorithm. A minimum speed is required to ensure the minimum BEMF for sensorless control using BEMF integration. The motor starts accelerating from zero speed to a speed indicated by the MAX_OPEN_LOOP_FREQ. Use Equation 70 to calculate the MAX_OPEN_LOOP_FREQ for a maximum open-loop RPM.

$$\text{Maximum open-loop RPM} = \frac{120 \times \text{MAX\_OPEN\_LOOP\_FREQUENCY}}{\text{Number of poles in motor}} \tag{70}$$

NOTE: To change the direction of rotation for the motor, the user may interchange any of the two motor winding connections to the board.

Overcurrent limit

The MSP430F5132 has an integrated comparator and timer event control (TEC) module, which can be configured to implement the overcurrent limit. The CBRSEL (reference select) bits in the CBCTL2 register of the MSP430F5132 can be configured to obtain different voltage thresholds in the comparator. The reference voltages settings available are 1.5 V, 2.0 V, and 2.5 V.

6.4 Running Project in CCS™ Software

To run this project in CCS:

1. Install CCS; the TIDA-00472 design requires the use of CCS v5.5 when using the MSP430F5132.
2. Import the project “TIDA-00472_sensorless_BLDC_V1.0”.
3. Refer to Section 6.3 for instructions on how to tune the control for the specific motor.
4. Power up the board with an external supply as Section 5.2 details and connect the MSP-FET430UIF to the computer and the programming pins of the MSP430F5132 device.
5. Build and debug the modified project to download the code to the MSP430F5132 device.

7 Test Setup

Figure 29 shows the load setup used in the lab to test the motor. The load is an electrodynamometer type through which the load torque applied to the motor can be controlled.

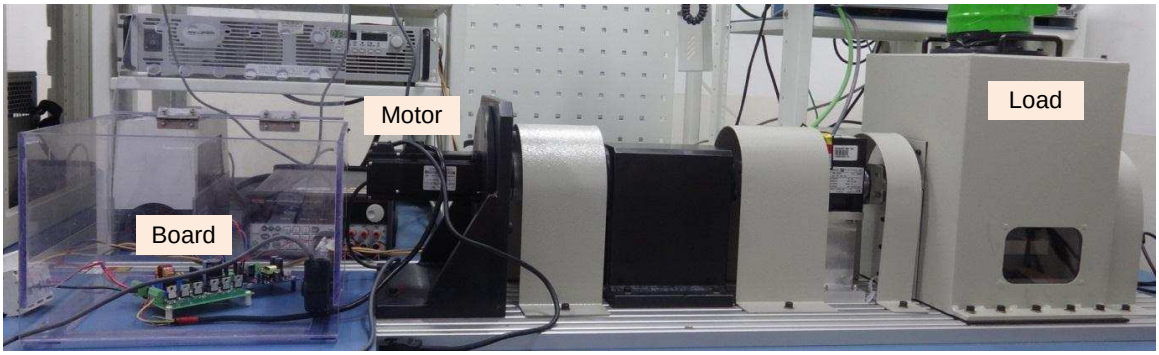


Figure 29. Test Setup for Board and Motor

8 Test Results

8.1 UCC27714 Functional Tests

The UCC27714 gate driver receives the PWM signals from the MSP430 MCU and the corresponding gate drive voltages are generated. Figure 30 shows the low-side and high-side gate drive output from the UCC27714. In the TIDA-00472 design, only the high side is modulated and is switching at 20 KHz in the 120º ON period. The low side is continuously ON for 120º.

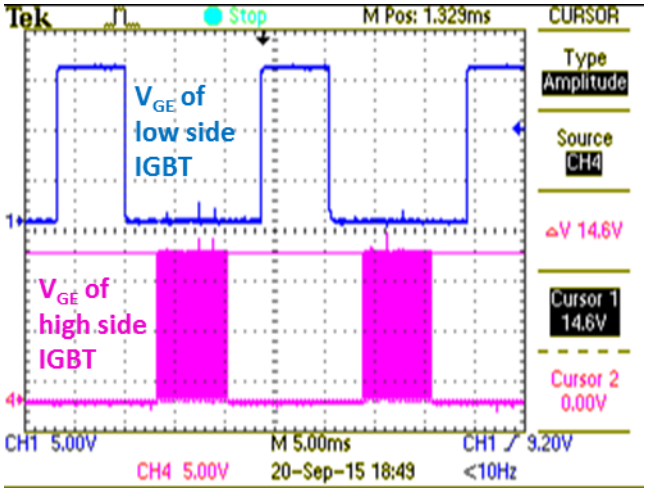


Figure 30. High-Side and Low-Side PWM Output From UCC27714

Figure 31 shows the low-side PWM input of the UCC27714 device and the corresponding low-side output of the UCC27714 device measured across the gate to the emitter (V_{GE}) of the IGBT. The low-side gate output from the UCC27714 device swings between ground and VCC (15 V) of the UCC27714.

Figure 32 shows the high-side PWM input of the UCC27714 device and the corresponding high-side output of the UCC27714 device measured across the gate to the emitter (V_{GE}) of the IGBT. The gate-to-emitter voltage is equal to VCC of the UCC27714 device minus the drop across the bootstrap diode of the high-side gate drive circuit. The waveforms show that the V_{GE} is approximately 14.6 V.

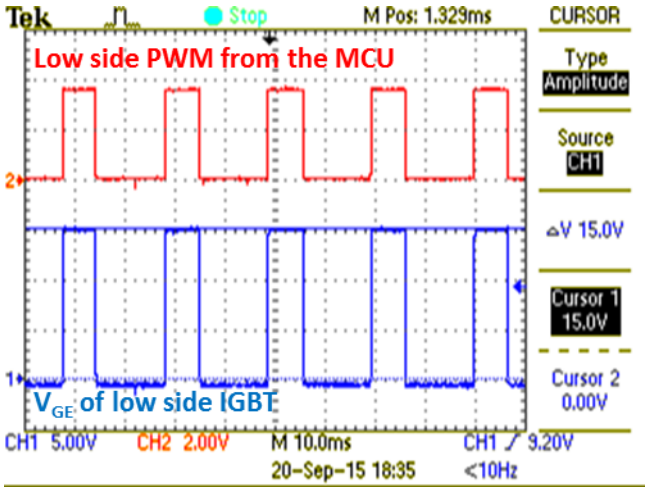


Figure 31. V_{GE} of Low Side IGBT and PWM From MCU

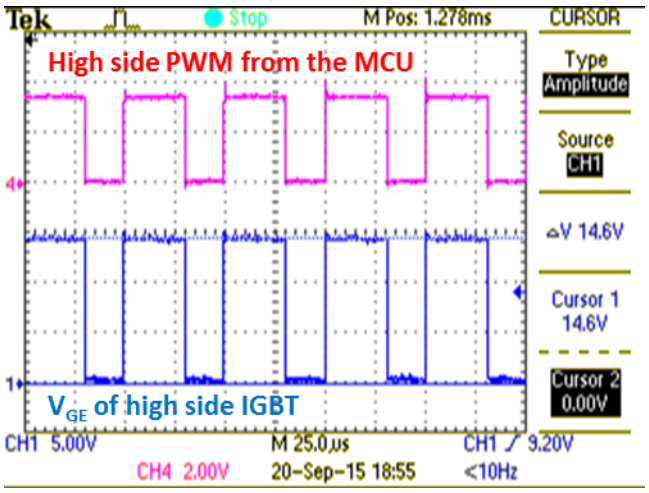


Figure 32. V_{GE} of High Side IGBT and PWM From MCU

8.2 Load Testing

8.2.1 Load Tests With DC Input

Figure 33 shows the motor winding current and winding voltage measured with respect to DC– when testing with a 300-V DC input. The winding voltage is switching at 20 KHz. Figure 34 shows the thermal image of the inverter board at 250 W when operated from 300-V DC. Note that the maximum temperature on the IGBT is 81.1ºC and has been tested at an ambient temperature of 22.9ºC.

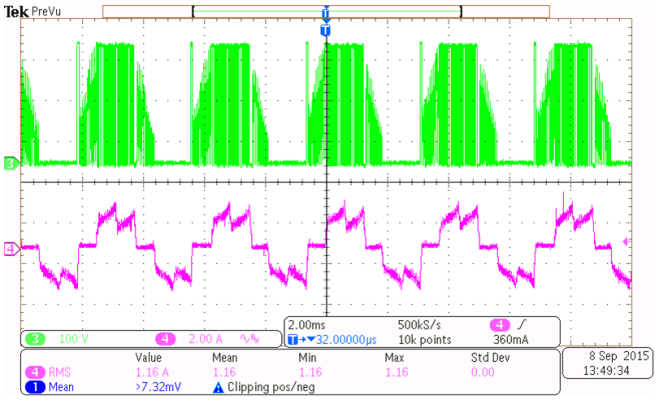


Figure 33. Winding Voltage and Winding Current of Motor at 250-W Inverter Power

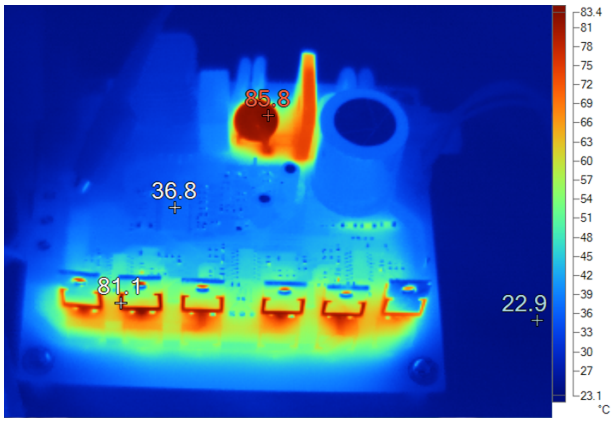


Figure 34. Thermal Image of Board at 250-W Inverter Power and 300-V DC Input

8.2.2 Load Tests With AC Input

Figure 35 shows the motor winding current and the DC-bus voltage ripple when tested with a 230-V AC input and 250-W load on the inverter. Note that the DC-bus peak-to-peak ripple voltage is approximately 54 V (approximately 17% ripple). The use of an algorithm for voltage ripple compensation allows the user to compensate for the DC bus ripple by modulating the duty cycle, which maintains a stable motor current waveform. Figure 36 shows the motor current waveform captured over one full cycle of the DC-bus voltage ripple. Figure 35 and Figure 36 show that the winding current is stable and these waveforms have the same wave shape as when testing with a pure DC voltage (zero voltage ripple), as the preceding Figure 33 shows.

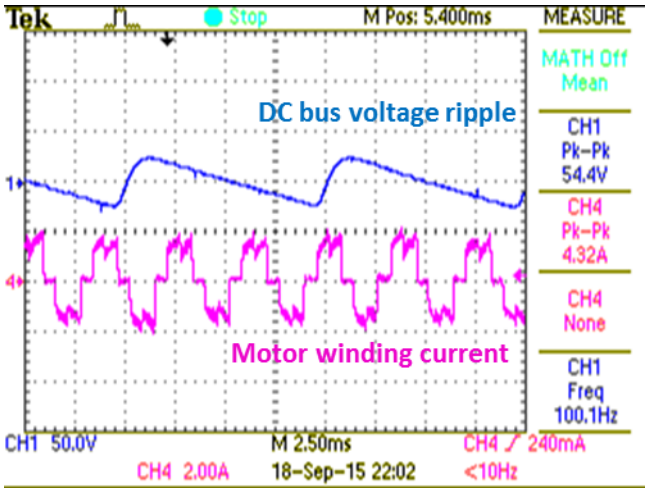


Figure 35. DC-Bus Voltage Ripple and Winding Current of Motor at 250-W Inverter Power

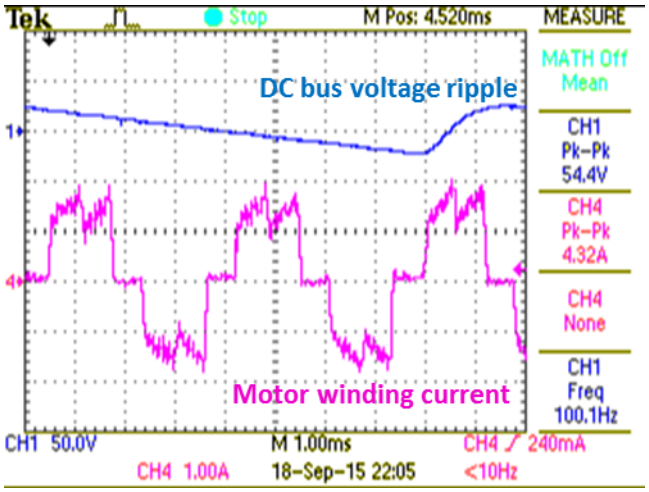


Figure 36. DC-Bus Voltage Ripple and Winding Current of Motor at 250-W Inverter Power (Zoomed-In to One Cycle of Voltage Ripple)

Figure 37 shows the thermal image of the inverter board at 250 W when operating from a 230-V AC. Note that the maximum temperature on the IGBT is 79.1ºC and has been tested at an ambient temperature of 21.1ºC.

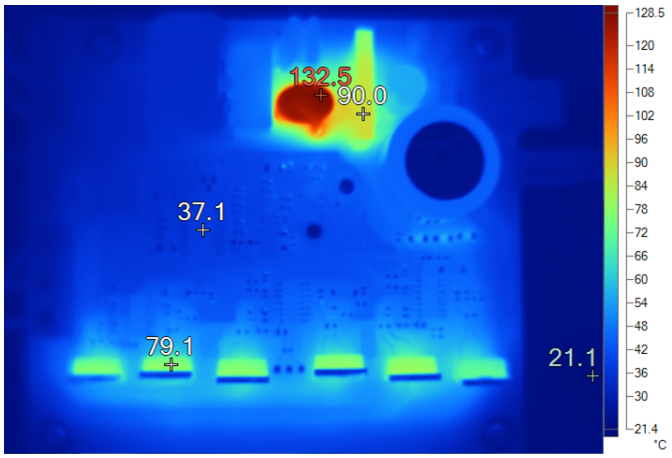


Figure 37. Thermal Image of Board at 250-W Inverter Power

Note that the maximum temperature is observed on the inrush current limiter. The user can select any other alternate part that has a larger diameter or a lower steady-state resistance. The diode bridge temperature is approximately 90ºC and has been tested at an ambient temperature of 21.1ºC without a heat sink. So without a heatsink on the diode bridge, safe operation can be guaranteed up to 45ºC ambient. TI recommends to use a heat sink for supporting the maximum operating ambient temperature of 65ºC. The designer can select a heat sink with a thermal resistance of approximately 20ºC/W.

Figure 38 shows the motor winding current and the DC-bus voltage ripple when testing at a 230-V AC input and 150-W DC bus power. Note that the DC-bus peak-to-peak ripple voltage is approximately 37.6 V. The use of an algorithm for voltage ripple compensation allows the user to compensate for the DC bus ripple by modulating the duty cycle, which maintains a proper motor current waveform.

NOTE: For situations that require a board designed for lower power levels (150 W for example), the DC bus capacitor value can be reduced further. A 82-µF capacitor is sufficient for a full-load power level of 150 W.

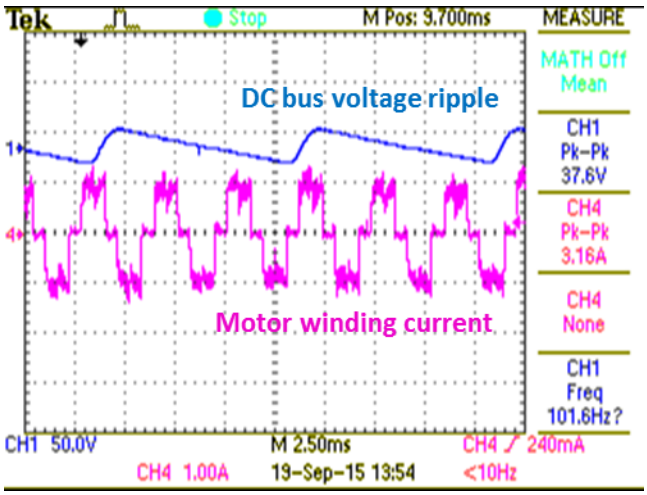


Figure 38. DC-Bus Voltage Ripple and Winding Current of the Motor at 150 W Inverter Power

Figure 39 shows the thermal image of the inverter board at 150 W when operated from a 230-V AC. Figure 40 shows the thermal image of the inverter board at 200 W when operating from a 230-V AC. Note that at 200 W the maximum temperature on the IGBT is 74.4ºC while testing at an ambient temperature of 22.8ºC. The diode bridge temperature is 78.2ºC. The board can work up to a DC bus power of 200 W without any heatsink up to an ambient temperature of 65ºC.

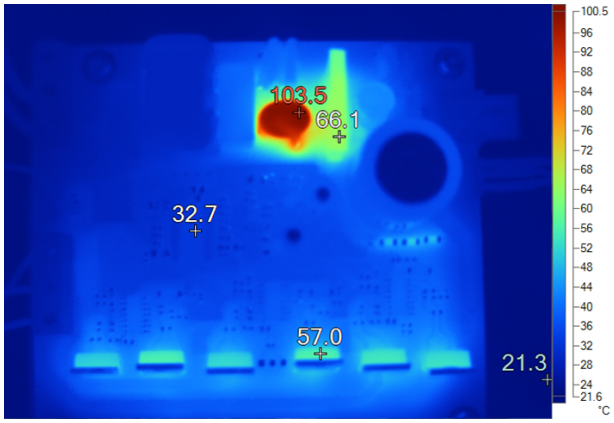


Figure 39. Thermal Image of Board at 150-W Inverter Power

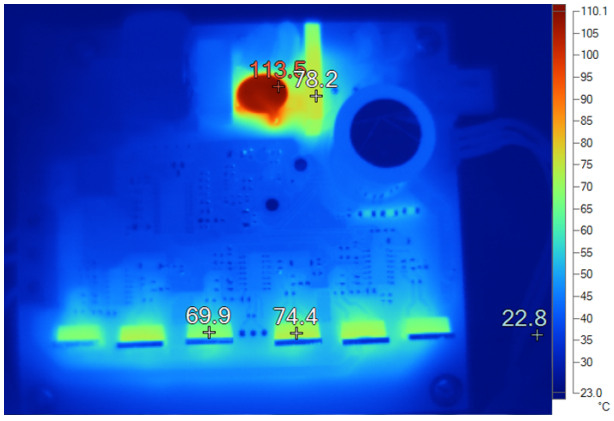


Figure 40. Thermal Image of Board at 200-W Inverter Power

Figure 41 shows the maximum IGBT temperature at the different winding current and input power levels.

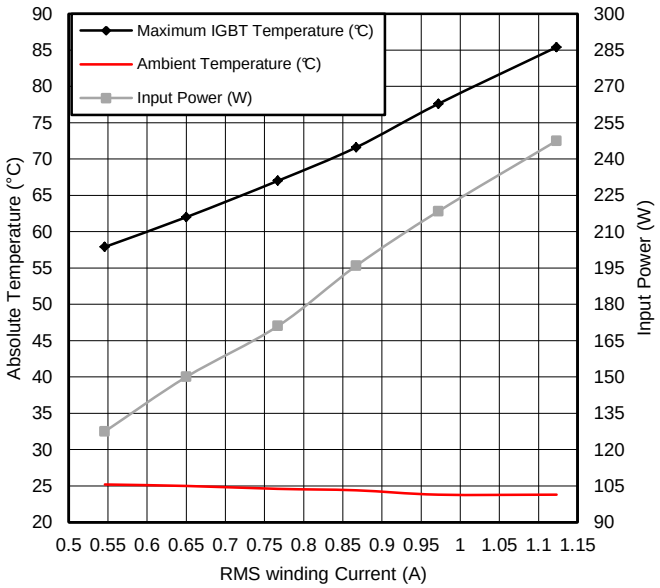


Figure 41. IGBT Temperature at Different Power Levels

8.3 Testing of Current Sense Amplifier

The TIDA-00472 reference design uses an OPA374 device configured as a differential amplifier to amplify the low-side DC bus current sensed by the sense resistor. In BLDC motors driven by trapezoidal control, the DC bus current is equivalent to the winding current. This equivalency means that the motor winding current control can be implemented by sensing the DC bus current. The high bandwidth and high slew rate of the OPA374 means that it is a suitable choice for motor current sensing and protection applications.

Figure 42 shows the winding current and the output of the OPA374.

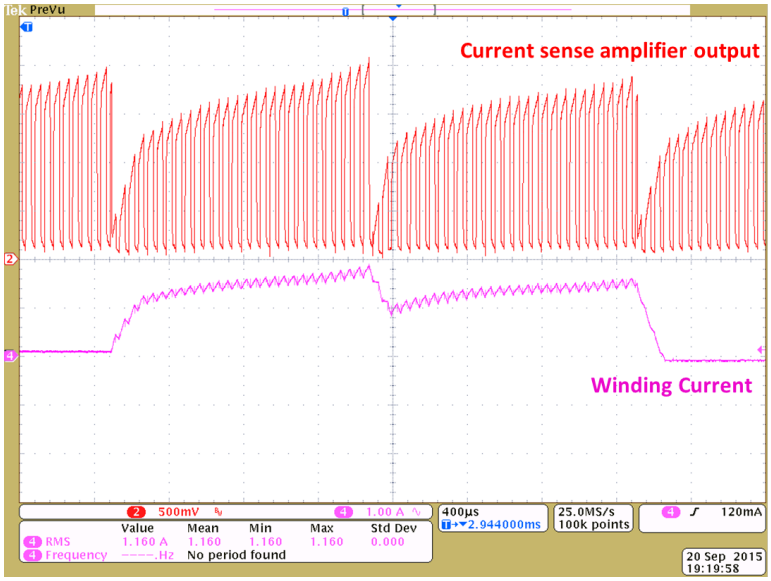


Figure 42. Motor Winding Current and Current Sense Amplifier Output

Figure 43 shows the uncalibrated output error of the current sense amplifier. The output error is plotted from a minimum DC bus current of 0.3 A to a maximum of 2.75 A, which covers the entire winding current range for an inverter rating up to 250 W. The maximum output error is less than 2.5%.

Figure 44 shows the output error of the current sense amplifier after offset calibration. The maximum offset calibrated output error is less than 0.2%, which ensures a precise current control and overcurrent protection.

Figure 43. Uncalibrated Output Error of Current Sense Amplifier

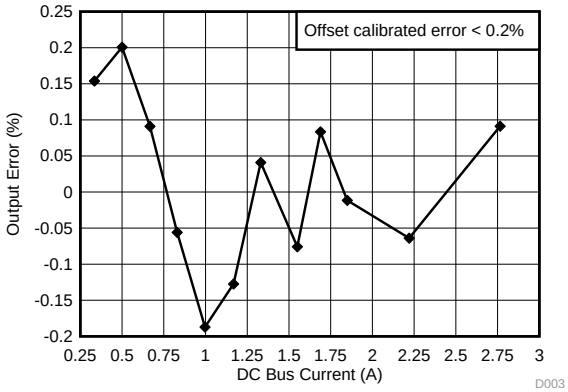


Figure 44. Offset Calibrated Output Error of Current Sense Amplifier

8.4 Overcurrent Protection

A 60-mΩ sense resistor is used to sense the DC bus current. Figure 45 shows the current limit operation when the comparator reference (V_{REF}) is set at 1.5V.

The overcurrent limit, I_{OC_LIMIT}, is equal to V_{REF} / (R_{SHUNT} × amplifier gain). At V_{REF} = 1.5 V, the I_{OC_LIMIT} is equal to 1.25 A.

Figure 46 shows the overcurrent limit protection in every PWM cycle where the current sense amplifier output is higher than the V_{REF}. The user can observe that the PWM immediately turns off when the comparator output goes high.

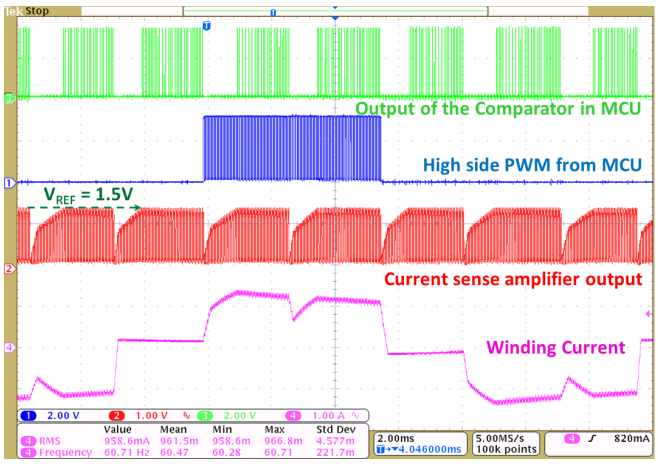


Figure 45. Cycle-By-Cycle Current Limit Using Hardware Features of MSP430F5132

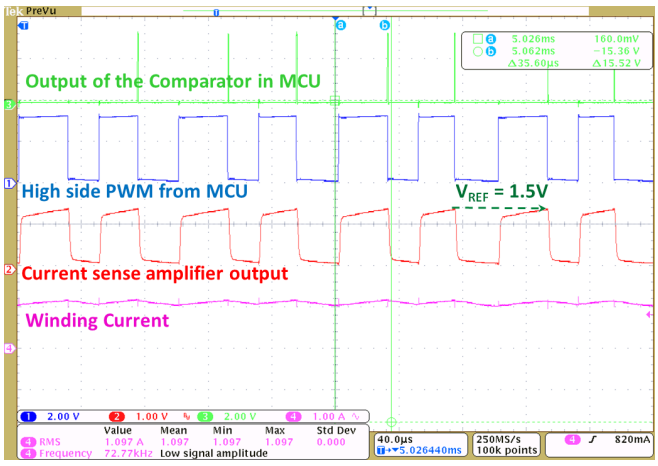


Figure 46. Cycle-By-Cycle Current Limit—PWM Shutdown With Comparator Output

Figure 47 shows the total response time of the cycle-by-cycle current limit action. The comparator reference voltage (V_{REF}) is set to 1.5 V. Figure 47 shows that the time between the current sense output is higher than 1.2 V (a lower voltage as compared to the reference 1.5 V is considered to calculate the response time, to ensure the worst case) and the PWM shutdown is approximately 356 ns. Therefore, in any case, the total response time of the current limit action is less than 1 µs.

Figure 48 shows the response time from the comparator output going high to a PWM shutdown event, which is approximately 100 ns.

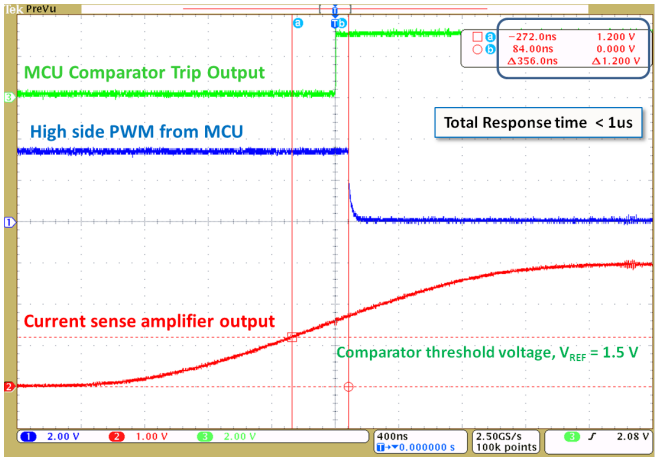


Figure 47. Total Response Time of Cycle-By-Cycle Current Limit Protection

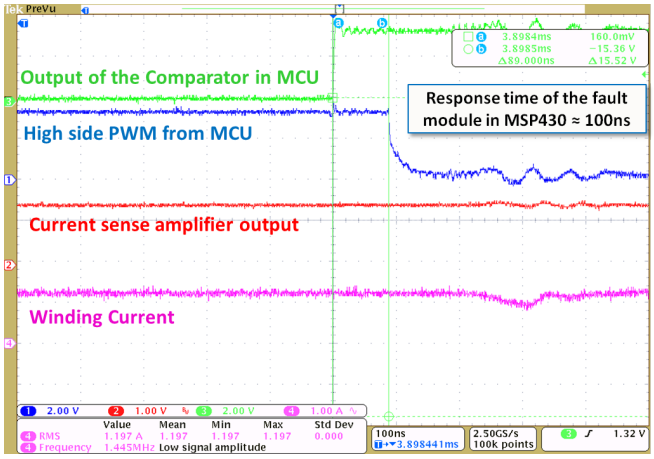


Figure 48. Response Time When Comparator Goes High to PWM Shutdown

8.5 Speed Variation

Figure 49 and Figure 50 show the winding current and winding voltage waveforms at two different speeds of 1000 RPM and 4000 RPM.

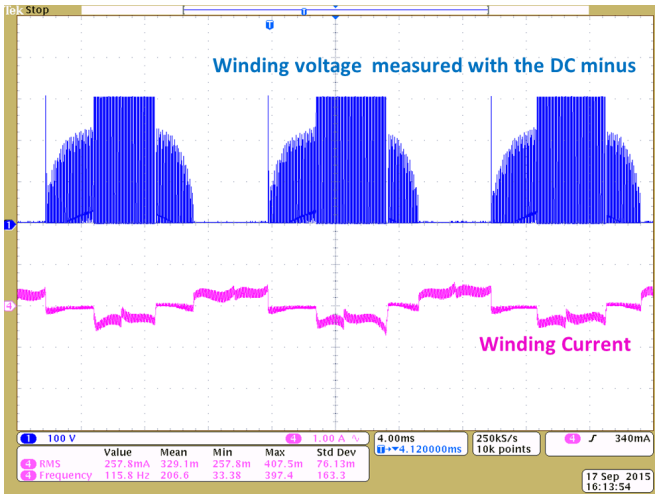


Figure 49. Winding Voltage and Winding Current of Motor at 1000 RPM

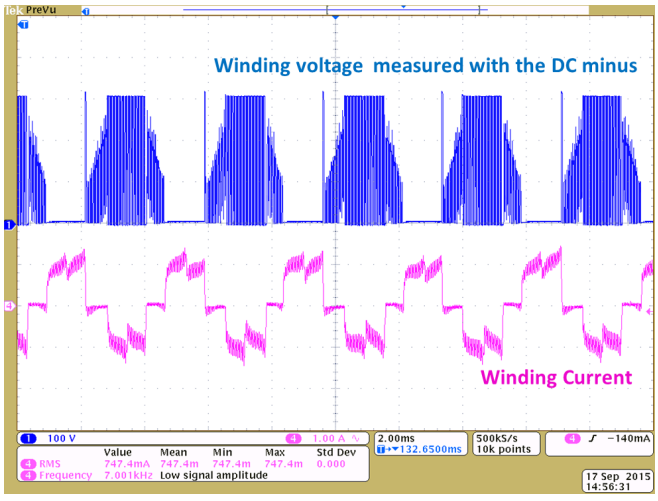


Figure 50. Winding Voltage and Winding Current of Motor at 4000 RPM

8.6 Effect of Motor Inductance on BEMF Sampling

The motor-winding inductance influences the BEMF sampling. The winding inductance causes oscillations with any parasitic capacitance in the board. Figure 51 shows the oscillations in the winding voltage feedback at the ADC input of the non-switching phase for a high inductance motor. For proper execution of the sensorless control, the BEMF must be sampled at an instant where the oscillations are damped out completely. From Figure 51, the user can observe that the BEMF can be sampled at the middle point of the PWM ON period, where the oscillations are not present. At low duty cycles, the sampling point can be moved towards 75% of the PWM ON period. Figure 52 shows the winding voltage feedback at the ADC input of the non-switching phase for a low-inductance motor. When the motor inductance is very little, the oscillations are small and dampen out very soon. So the ADC sampling can be done even at 25% of the PWM ON period.

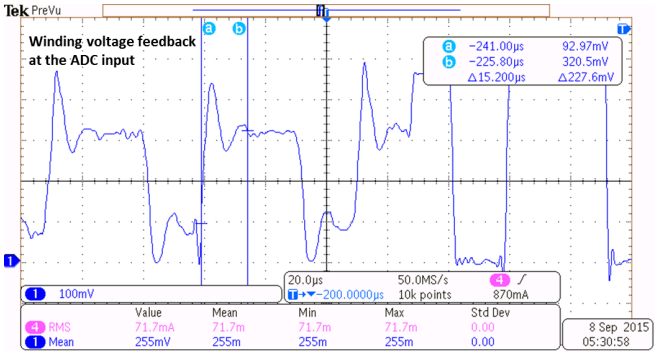


Figure 51. Oscillations in Winding Voltage Feedback for a High inductance Motor

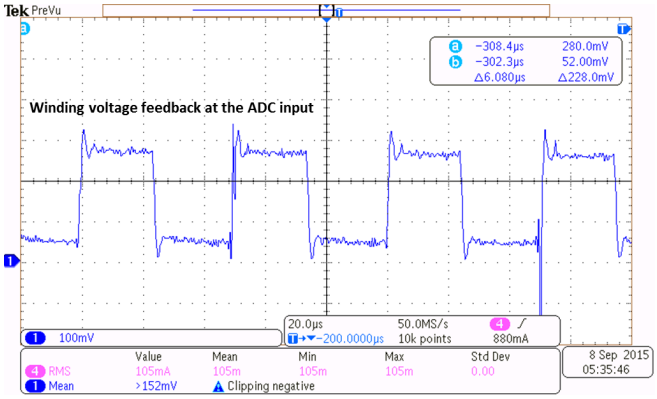


Figure 52. Oscillations in Winding Voltage Feedback for a Low inductance Motor

8.7 Conducted Emission Test

The TIDA-00472 reference design has been tested for conducted emission as per EN55022 Class B (EN55014) limits. The reference design passes EN55022 Class B with more than a 4-dB margin. The motor has been tested running at full speed (duty cycle = 73%) and without a load on the motor output. However, the actual test can be performed with a full load on the motor shaft. Figure 53 shows the conducted emission test results.

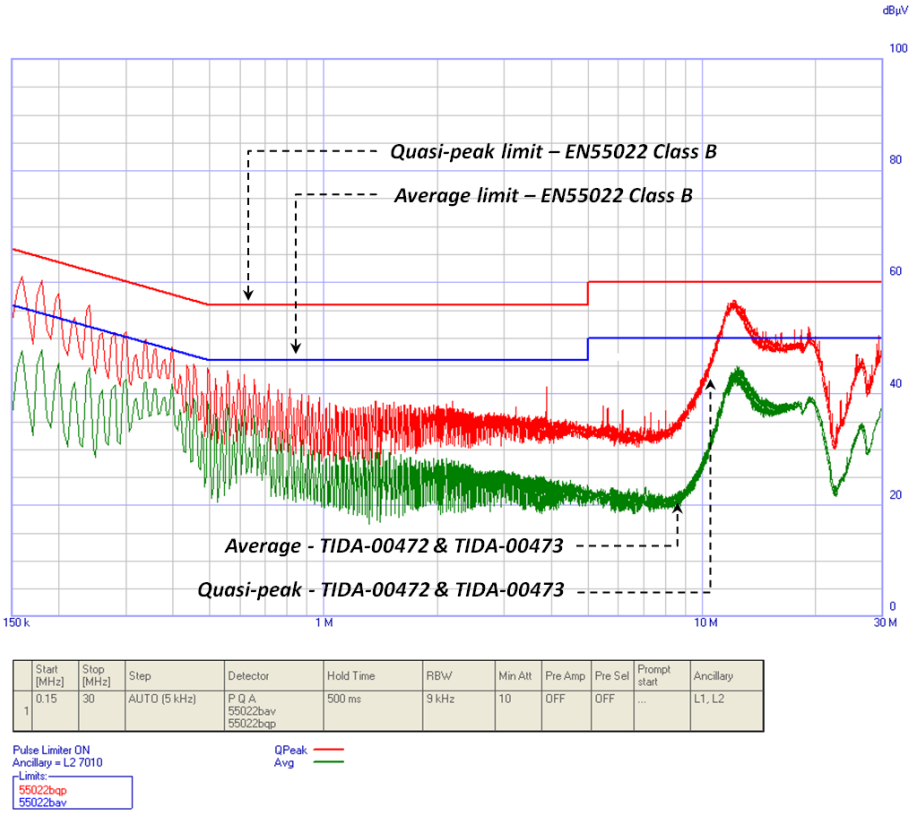


Figure 53. Conducted Emission Test Results as Per EN55022 Class B—Average and Quasi-Peak Detector Output

8.8 Surge and EFT Test

Surge and EFT testing is done on the reference design board. Table 4 shows the test conditions and test results.

Table 4. Surge and EFT Test Results

BASIC STANDARD	PORT	REQUIREMENTS – RESIDENTIAL, COMMERCIAL, AND LIGHT-INDUSTRIAL ENVIRONMENTS	PERFORMANCE CRITERION	TEST RESULT
IEC/EN 61000-4-4: Fast transients (burst)	AC input	±1 kV, 5 kHz	B	Passed
IEC/EN 61000-4-5: Surges	AC input	±2-kV line-to-earth ±1-kV line-to-line	B	Passed

9 Design Files

9.1 Schematics

To download the schematics for each board, see the design files at TIDA-00472.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00472.

9.3 Layout Prints

To download the layer plots, see the design files at TIDA-00472.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00472.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00472.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00472.

9.7 Software Files

To download the software files, see the design files at TIDA-00472.

10 References

1. Texas Instruments, *MSP430F51x2 and MSP430F51x1 Mixed-Signal Microcontrollers*, MSP430F51x2 and MSP430F51x1 Datasheet (SLAS619)
2. Texas Instruments, *UCC27714 High-Speed, 600-V High-Side Low-Side Gate Driver With 4-A Peak Output*, UCC27714 Datasheet (SLUSBY6)
3. Texas Instruments, *Sensorless Trapezoidal Control of BLDC Motors*, Application Report (SPRABQ7)

11 Terminology

SPI— Serial peripheral interface

PWM— Pulse width modulation

BLDC— Brushless DC motor

BEMF— Back electro-motive force

MCU— Microcontroller unit

FETs, MOSFETs—Metal-oxide-semiconductor field-effect transistor

IGBT— Insulated gate bipolar transistor

ESD— Electrostatic discharge

RPM— Rotations per minute

RMS— Root mean square

12 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics, analog and mixed signal designs. He has system level product design experience in permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2015) to A Revision	Page
• Changed title	1

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