TI Designs

18-Bit, 2-MSPS Isolated Data Acquisition Reference Design for Maximum SNR and Sampling Rate

TI Designs

This TI Design illustrates how to overcome performance-limiting challenges typical of isolated data acquisition system designs by:

- maximizing sampling rate by minimizing propagation delay introduced by digital isolator
- maximizing high-frequency AC signal chain performance (SNR) by effectively mitigating ADC sampling clock jitter introduced by the digital isolator

Design Resources

TIDA-00732	Design Folder
ADS9110	Product Folder
ISO7840, ISO7842, ISO1541	Product Folders
REF5045, TLV3012	Product Folders
OPA376, OPA378, OPA625	Product Folders
TPS7A4700	Product Folder
TPS70918, TPS70912	Product Folder
LMZ14203, SN6505A	Product Folders
SN74LVC1G17, SN74LVC1G08	Product Folders
LMK61E2	Product Folder
ADS9110EVM-PDK	Associated Design

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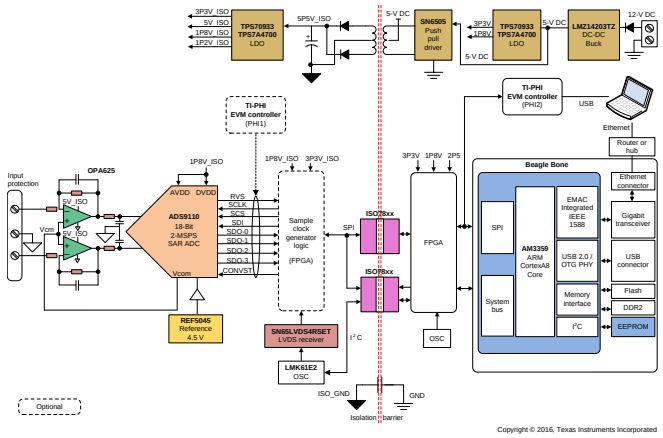
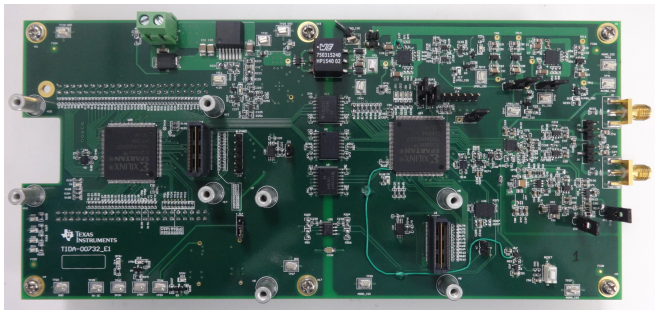
Design Features

- Isolated 18-Bit, 2-MSPS, Single-Channel, Differential Input Data Acquisition (DAQ) System
- Leverages multiSPI™ Digital Interface of ADS9110 to Achieve 2-MSPS Sampling Rate While Maintaining Low SPI CLK Speed
- ADC Clock Master Mode and Source-Synchronous SPI Data Transfer Minimizes Digital Isolator Propagation Delay and Increases Throughput
- Optimized Jitter Reduction Techniques Employed Results in 12-dB SNR Improvement (100-kHz f_{IN}, 2-MSPS)
- Includes Theory, Calculations, Component Selection, PCB Design, and Measurement Results

Featured Applications

- Modular DAQ Systems
- Data Logging
- Design Validation and Verification
- Remote Process Monitoring and Control





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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	Single
Input type	Differential
Input range	±5-V fully differential
Input Impedance	1 KΩ
Resolution	18 bits
SNR	95.5 dB at 100-kHz signal input
ENOB	15.5 bits
Power supply isolation	250-V DC (continuous) basic insulation 5000-V AC for 1 minute (withstand)
Digital channel isolation	5.7-kV_{RMS} isolation for 1 minute per UL 1577
Operating temperature	0°C to 60°C
Storage temperature	–40°C to 85°C
Connectors	Two, 60-pin Samtec high density connector for PHI module interface 2x46-pin 2.54-mm header for Beaglebone Black™ interface
Power	12- V DC, 250 mA
Form factor (L × W)	228 mm × 106 mm

2 System Description

A DAQ system measures an electrical or physical phenomenon such as voltage, current, temperature, pressure, or sound with an integrated or external host computer.

A DAQ system consists of sensors, DAQ measurement hardware-signal conditioning ADC, and an embedded or host computer with programmable software. Figure 1 shows a generic DAQ system block diagram.

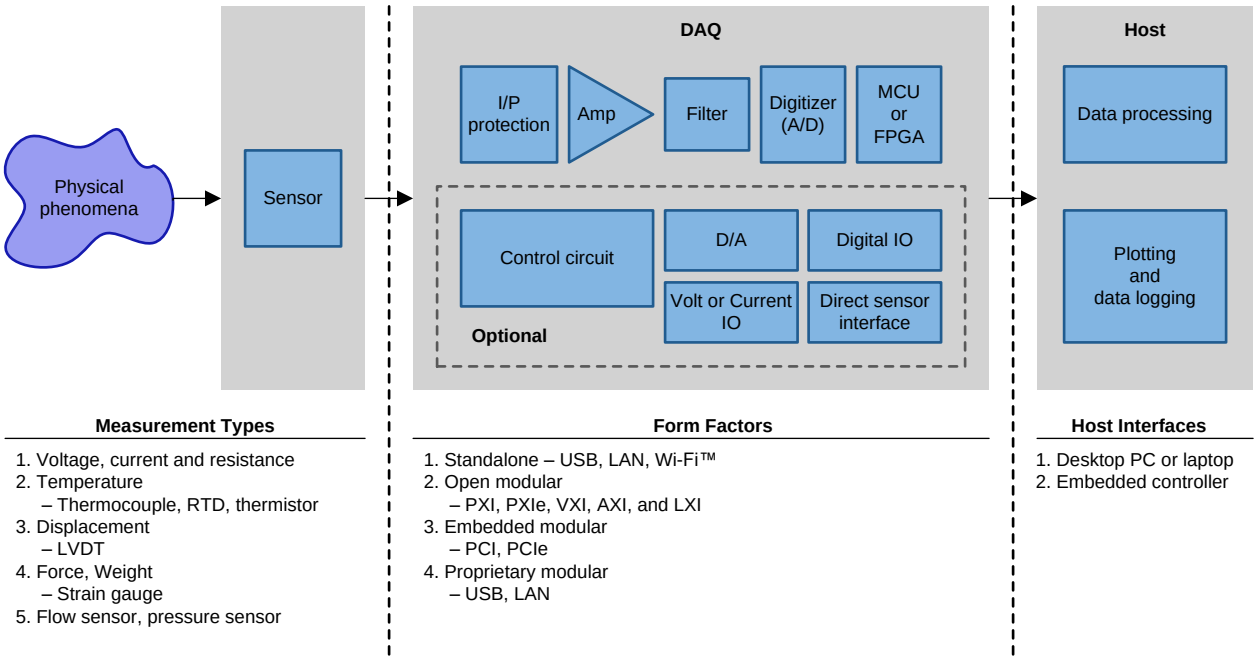

Figure 1. Generic DAQ System Block Diagram

The DAQ system can be found in following applications:

- Voltage, current, and resistance measurement
- Temperature measurement
- Force measurement
- Position, distance, or rotation
- Sound and vibration monitor

The DAQ system can be classified according to functions

- Analog input (isolated or non-isolated)
- Multifunction
- Universal input
- Direct sensor input

The TIDA-00732 is developed based on an isolated analog input type. Figure 2 shows the generic block diagram of an isolated analog input module.

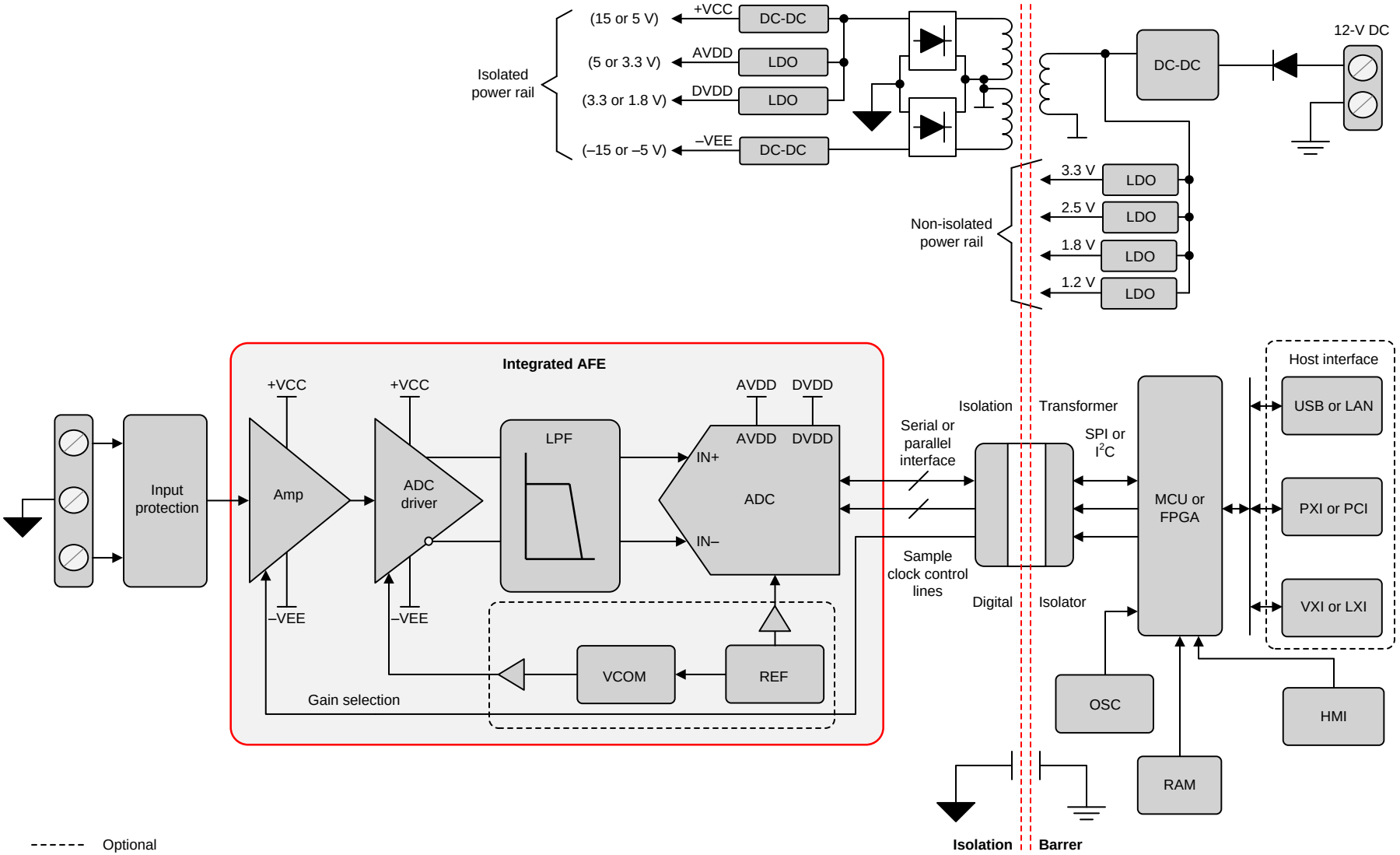

Figure 2. Generic Illustration of Isolated Analog Input DAQ Module

Sensor

As discussed earlier, the DAQ system accepts direct electrical signal or physical parameters like temperature, pressure, and force. If it is a physical parameter, an appropriate sensor can convert the physical parameter to electrical signals; these electrical signals (volt or current) can be used as input to DAQ system.

Analog Front-End

This device contains an input protection circuit at the front end, which protect inputs from surge voltage and feeds to a programmable gain amplifier that scales signals to the required level of the ADC dynamic range. Followed by PGA, signals are fed to an anti-aliasing low-pass filer through the ADC driver. Here, anti-aliasing filters remove unwanted signals and limits input bandwidth of the analog front-end.

The ADC converts the time varying analog input to either a serial or parallel binary bit stream. These bit streams are processed by a local embedded controller (MCU) or FPGA.

The ADC has onboard voltage reference, which provides high precision and low noise. Some versions of ADCs have integrated voltage reference as well.

In isolated DAQ systems, the isolation can be accomplished either with an analog or digital end depending on system requirements. Typically, digital ends can isolate due to low costs and easy implementation compared to analog isolation. In Figure 1, ADC data lines pass through the digital isolator and are connected to embedded controller.

Host Computer Interface

The host or embedded controller is interfaced with ADC through a serial or parallel interface. The acquired data are processed and displayed in a physical format.

The embedded controller has a human machine interface (HMI) with an embedded GUI for local monitoring and data logging. The DAQ module also supports LXI, VXI, PCI, and PXI open architecture platforms and USB interface, which can be used for further monitoring and analysis.

2.1 DAQ Signal Chain Design Challenges

DAQ systems use isolation in the signal chain because it breaks ground loops, thereby improving measurement accuracy and safety. The isolation can be either at the analog input side or can be at the digital interface. Analog isolation typically decides (and limits) the signal chain performance (analog isolation typically has an A/D-digital isolation-D/A chain). The digital isolator works fine for medium resolution and medium sampling rates. However, for higher resolution (>16 bits), higher speed (>1 MSPS), and higher input BW (>100 kHz), the digital isolators present few design challenges to be considered to match the ADC performance with the complete signal chain performance.

2.1.1 Isolated Analog Input Module Signal Chain Design Challenges

DAQ systems typically use digital isolators at the serial peripheral interface (SPI) of the ADC for functional isolation. The digital isolator presents two main design challenges: propagation delay and additive jitter. The propagation delay of the isolator limits the maximum clock of the SPI and hence limits the sampling rate of the ADC. The digital isolator adds jitter to the sampling clock that is generated at the host side. The SNR degradation of the signal chain due to jitter in sampling clock is proportional to the input signal frequency.

2.1.1.1 Propagation Delay in Digital Isolator

The SPI bus is a synchronous, full duplex, serial data link commonly used for onboard short distance data exchange between a master device, such as a microcontroller unit (MCU) or FPGA, and one or multiple slave devices, such as data converters, digital I/O devices, temperature sensors, and power management controllers.

In SPI communication, data transfer transmission and reception happens on the same clock period. In isolated systems, the digital isolator is placed in between master and slave devices. The round trip propagation delay of the digital isolator results in the delayed receive of ADC data at MCU. The round-trip propagation delay must be less than the half serial clock period to ensure an error-free data transfer.

$$t_{SCLK\_min} = 2 \times \left(2 \times t_{ISO\_pd} + t_{ADC\_CKDO}\right) \quad (1)$$

Figure 3 shows the isolator propagation delay affecting the SPI receive timing.

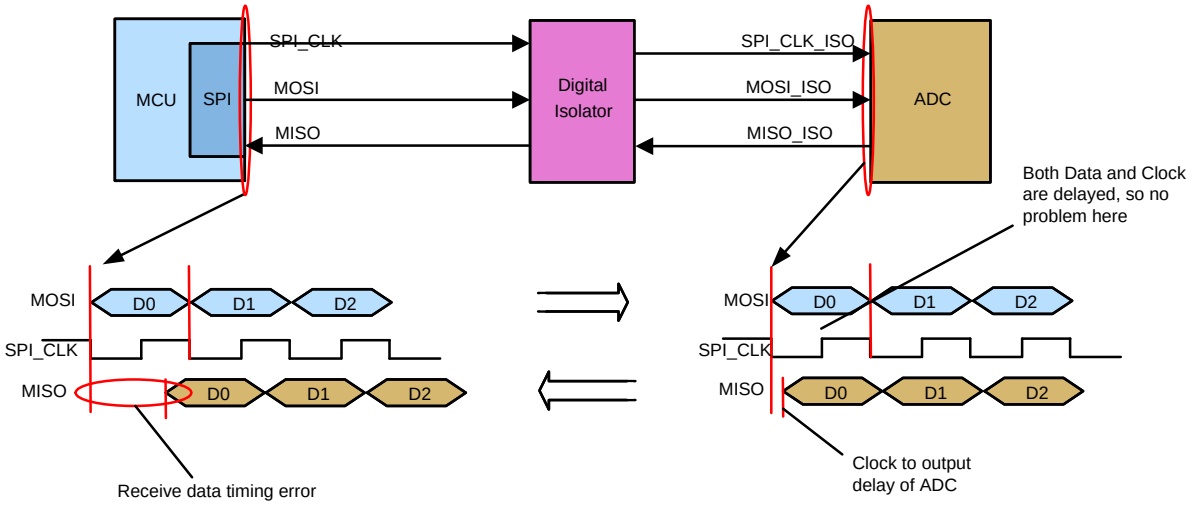

Figure 3. Propagation Delay Affecting SPI Receive Timing

ISO7842 and ADS9110 Example

Consider a signal chain with the ADS9110 and ISO7842 for an 18-bit, 2-MSPS sampling rate DAQ system.

- ISO7842: t_{ISO_pd} = 16 ns max
- ADS9110: t_{ADC_CKDO} = 6.5 ns max and 20 SCLKs per sample
- f_{SCLK_max} limited by isolator will be $\frac{1}{2 \times (2 \times 16 + 6.5)} \cong 13$ MHz

For one MISO SPI, 13 MHz of SCLK results in $\left(\frac{1}{\left(\frac{20}{13} + 0.2\right)}\right) \cong 570$ kHz of ADC sampling rate, where $\left(\frac{20}{13}\right)$ is the data transfer time and 0.2 µs is the acquisition time for the ADC.

Any delay added in the SPI data path will further reduce the sampling rate. Therefore, at system level, the maximum sampling rate is limited by the delays and not by the ADC.

To achieve the sampling rate of 2 MHz, the SCLK should be at least $\left(\frac{0.3}{20}\right)$ or ~67 MHz, which requires an isolator propagation delay of ~4 ns max.

One way to relax the isolator's propagation delay requirement is to use multiple SDO lines on the ADC. By using all four SDO lines of the ADS9110, the max throughput can be increased to $\frac{1}{\left[\left(\frac{5}{13}\right) + 0.2\right]} = 1.7$ MSPS —still lesser than the 2 MSPS rated throughput of the ADS9110. However, three additional channels of isolation are required, and the host needs to support four SDI lines.

Another approach is to use the multi-SPI digital interface Clock Master Mode to perform a source-synchronous data transfer. In this mode, the ADC generates the SCLK signal on the RVS pin so that it is in sync with the data on the SDO pins, eliminating the effect of the isolator induced timing delays (see the ADS9110 datasheet (SBAS629) or watch the multiSPI overview video for more details). To use this mode, the host side must support a SPI slave operation.

In summary, the propagation delay of the isolator affects the SPI receive data timing and limits the SCLK of the SPI. Limiting the SCLK, results in lower ADC sampling rate. The propagation delay could be handled by using lower SCLK for SPI. Slower SCLK is possible by using more SDO lines for SPI. The propagation delay can also be addressed by using source-synchronous mode of data transfer from ADC.

2.1.1.2 ADC Sampling Clock Jitter

The SNR performance of the ADC at a higher input signal frequency is affected by the jitter in the sampling clock of the ADC. The sampling clock, which is the conversion start signal (CONVST), is typically generated by the host. Since the CONVST signal is passed through the isolator, jitter gets added to the CONVST signal. The data convertor uses the convert start signal (CONVST) to sample the input signal, and any deviation in sample point creates a measurement error and increases the noise floor, which results in SNR degradation (see Figure 4 and Figure 5).

An acceptable clock jitter depends on the targeted system SNR, frequency of the input signal, and over sampling ratio (OSR) for sigma-delta ADC.

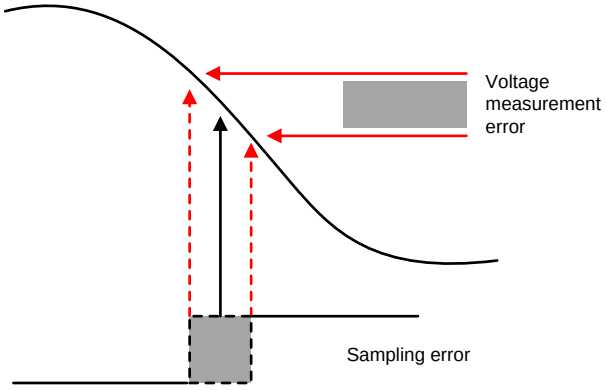

Figure 4. Error due to Jitter on Sampling Clock—Data

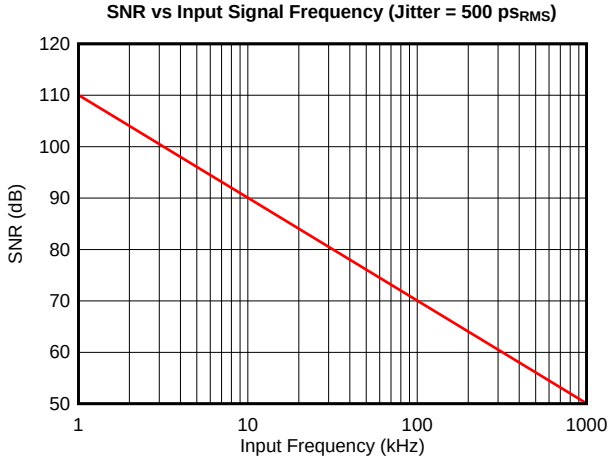

Figure 5. Error due to Jitter on Sampling Clock—Graph

The SNR of the ADC with sampling clock jitter can be expressed as,

$$SNR = -20\log\left(2\pi f_{IN} \times t_{JITTER}\right) + 10\log\left(OSR\right) \quad (2)$$

where

- f_{IN}: Input signal frequency
- t_{JITTER}: Total jitter of ADC (internal clock + external clock)
- OSR: Over sampling ratio (only for sigma-delta ADC)

The datasheet SNR performance of the ADS9110 at 100-kHz input signal is 95.5 dB. The maximum allowed sampling clock jitter to achieve desired SNR can be calculated as shown in Table 2.

Table 2. Allowed Jitter-Desired SNR

PARAMETER	VALUE	UNIT
Input frequency	100	kHz
Target SNR	95.5	dBc
Aperture jitter	100	fs rms
Total jitter	26.72	ps rms
Sample clock jitter	26.72	ps rms

Equation 2 clearly shows that the SNR of the signal chain will be limited if the jitter introduced by an isolator on the sample clock is greater than 27 ps rms.

2.2 Possible Solutions

2.2.1 Compensating the Propagation Delay

The ADS9110 has a multiSPI digital interface that allows the host controller to operate at slower SPI SCLK and still achieve the required sampling rate. The multiSPI module offers the following options to reduce SCLK speed:

1. Option to increase the width of the output data bus: 1, 2, and 4 SDO lines
2. Source-synchronous mode

The multiSPI option allows the SPI SCLK to be reduced and thus reducing the impact of propagation delay on the sampling rate. If the reduced SCLK rate is still above the loopback delay, then source-synchronous mode will be useful.

In source-synchronous mode, the SCLK from the host is looped back by the ADC along with the data. The clock and data are synchronous in source-synchronous mode; therefore, the propagation delay of the isolator has no impact on the data rate.

As Figure 6 shows, in ADC-master or source-synchronous mode, the device provides asynchronous output clock (on the RVS pin) along with the output data (on the SDO-x pins). The ADC-master or source-synchronous mode completely eliminates the effect of isolator delays and the clock-to-data delays, which are typically the largest contributors in the overall delay.

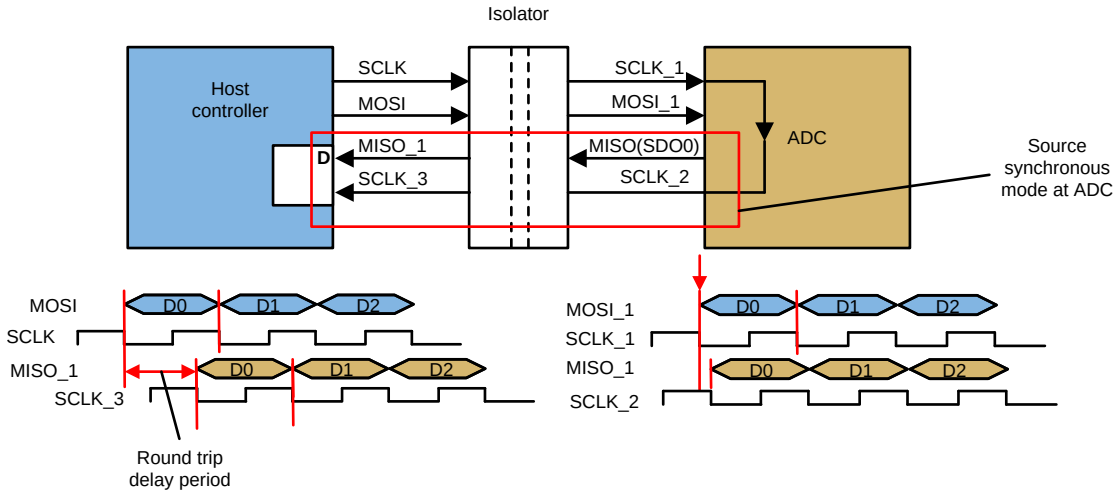

Figure 6. ADS9110 SPI Source-Synchronous Mode With Host and Slave End Timing Waveform

2.2.2 Mitigating SNR Degradation due to Jitter

As per the analysis, the jitter on the conversion clock "CONVST" signal degrades the performance of ADC SNR at higher input signal frequency and will impact the system performance.

As shown in Figure 7, the ADC sample clock CONVST is generated locally using CPLD or FPGA, and this signal is sent back to host for synchronization. Further, this CONVST signal is synchronized with low jitter oscillator, which eliminates the jitter on the CONVST signal generated by CPLD or FPGA.

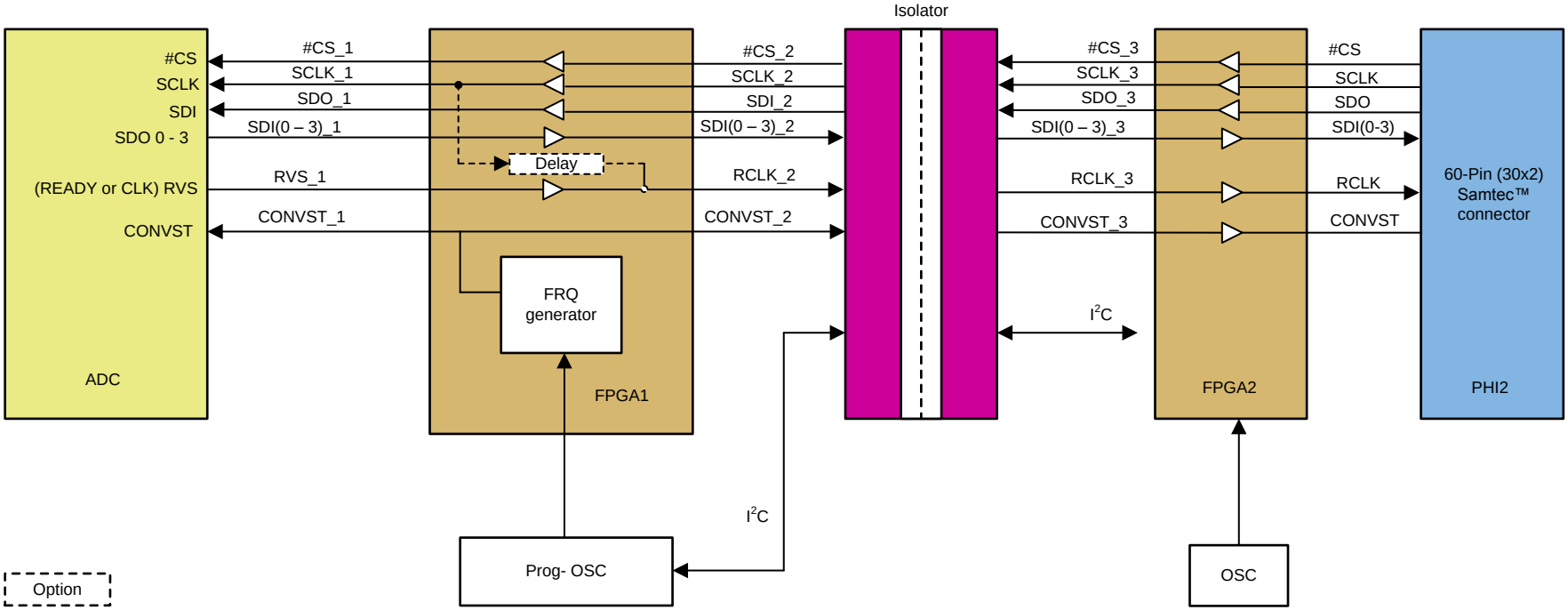

Figure 7. Jitter Mitigation by Sampling CONVST With Ultra-low Jitter Clock

2.3 TIDA-00732 Solution

The solution discussed in Section 2.2 is implemented in the TI Design TIDA-00732 and showcases the following features:

- Compares SNR performance of the ADC side generated CONVST with the host generated CONVST
- Demonstrates that the ADC side generated CONVST signal with low jitter clock has better SNR performance for high frequency input signal
- Confirms that the host generated CONVST SNR performance is limited by digital isolator jitter

3 Block Diagram

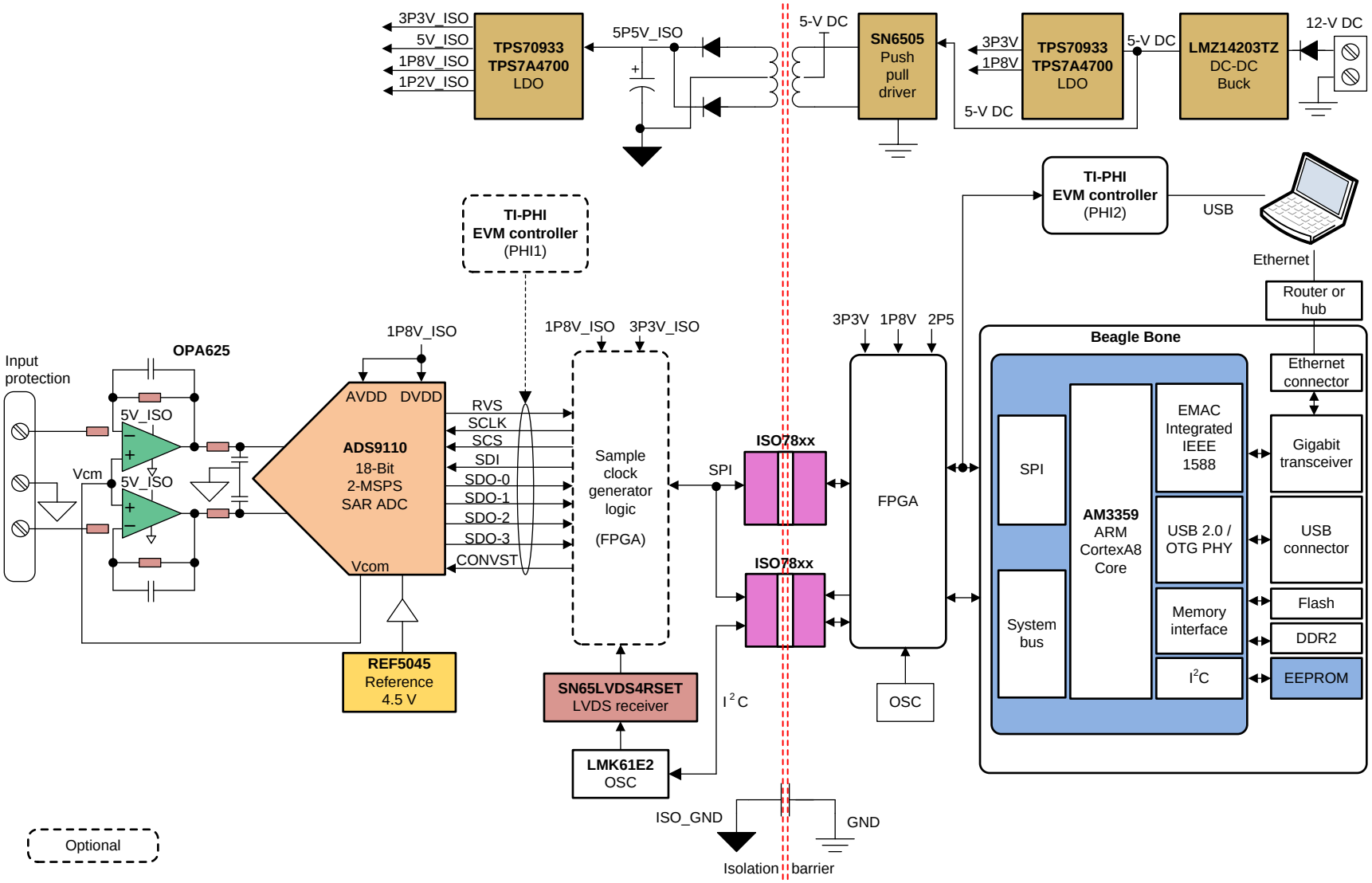

Figure 8. TIDA-00732 System Block Diagram

3.1 Highlighted Products

The system contains the following highlighted parts, which determine the overall system performance.

These parts can be grouped as flowing sections:

- Signal chain
- Clock
- Power

3.1.1 Signal Chain

- OPA625
  The OPAx625 is designed to drive precision (16-bit and 18-bit) SAR ADCs at sample rates up to 1 MSPS. The combination of low output impedance (1 Ω at 1 MHz), low THD, low noise, and fast settling time (4-V step, 16-bit levels with 280 ns) make the OPAx625 the ideal choice for driving both the SAR ADC inputs and the reference input to the ADC.
- ADS9110
  The module has a single-channel differential analog input and uses the ADS9110, 18-bit, 2-MSPS SAR ADC.
- REF5045
  The onboard reference REF5045 (ultra-low noise, low drift, and high precision) followed by low noise, low temperature drift, and low output impedance buffer provide a 4.5-V reference to ADC core.
- ISO784x and ISO1541
  The digital isolation for the host SPI and control signal is achieved using the ISO7840 and ISO7842 digital isolators. The host controller communicates with the LMK61E2-SIAR (ultralow programmable clock oscillator) through the ISO1541, which isolates the I^2C bus.

3.1.2 Clock

The LMK61E2 programmable oscillator has the following features:

- Ultralow noise, high performance (90-fs RMS jitter at > 100 MHz)
- Frequency tolerance ±50 ppm
- Frequency output 10 MHz to 1GHz
- I^2C interface

3.1.3 Power

- SN6505
  The isolated power supply power is generated using the SN6505, low-noise, low-EMI push-pull transformer driver.
- DC-DC and LDO
  The power supply rail for both the isolated and non-isolated sections is generated by the DC-DC convertor and LDO, which are shown in Table 3.

Table 3. Supply Rails

SINO	TYPE	PART NO	SUPPLY RAIL
1	DC-DC	LMZ14203	5.5 V
2	LDO	TPS7A4700RGWR	5 V, 3.3 V
3	LDO	TPS709XXDBVT	1.8 V, 1.2 V

4 Circuit Design

The DAQ analog front-end consists of the high-speed signal chain and the power supply section. This section describes various circuit blocks, performance requirement, and the component selection methodology.

4.1 Signal Chain Circuit Design

One of the major and essential building blocks for DAQ is the analog front-end, which consists of the input driver followed by an anti-aliasing filter, an ADC, and reference circuit. The TI Precision Design *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power* is taken as a reference, and all the design equations can be referred to the same (SLAU513).

The TIDA-00732 highlights the signal chain design challenges in an 18-bit, 2-MSPS DAQ system. This design uses TI's 18-bit, 2-MSPS SAR ADC, ADS9110. The ADS9110 is a fully differential SAR ADC with excellent dynamic performance and low power. The device consumes only 15 mW of power when operating at the full 2 MSPS throughput. The ADS9110 features the new multiSPI digital interface, which reduces the SPI clock rate for the full sample rate.

To optimize the performance of the 18-bit, 2-MSPS DAQ system, the input buffer, anti-aliasing filter, and reference driver must be designed in such a way that the performance is equal to or greater than the ADC performance.

To meet the performance goals of the AFE design, follow these steps:

1. Select an appropriate amplifier with sufficient small-signal bandwidth and low power, which minimally degrades the noise and distortion performance of the ADC.
2. Design a low-pass anti-aliasing RC filter to band-limit the noise contribution from the front-end circuitry while paying attention to the stability of the driving amplifiers.
3. Design a high precision reference driver circuit, which should provide the required value of V_{REF} with low offset, drift, and noise contributions.

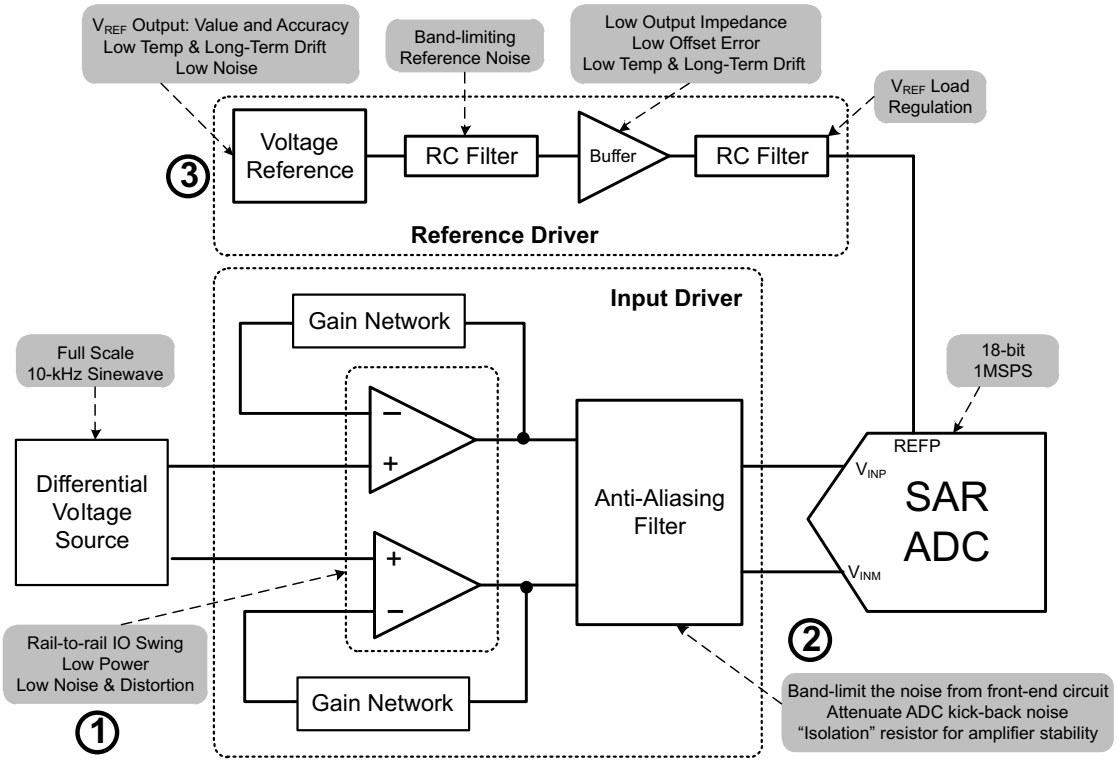

Figure 9. Analog Front-End Circuit of DAQ

4.1.1 Input Driver Circuit

4.1.1.1 Input Buffer Amplifier

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input signal, and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Carefully design the front-end circuit to meet the linearity and noise performance of the ADS9110.

The input op amp must support following key specifications:

1. Rail-to-rail input and output (RRIO)
2. Low power, low noise
3. High small-signal bandwidth with low distortion at high frequencies

The OPAx625 is designed to drive precision (16-bit and 18-bit) SAR ADCs at sample rates up to 2 MSPS. The combination of low output impedance (1 Ω at 1 MHz), low THD, low noise (2.5 nV/√Hz), and fast settling time (4-V step, 16-bit levels with 280 ns) make the OPAx625 the ideal choice for driving both the SAR ADC inputs as well as the reference input to the ADC.

Settling Time

For DC signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier datasheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA™-SPICE simulations before selecting the amplifier.

Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher-frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called aliasing. Therefore, an analog antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, where the 3-dB bandwidth is optimized based on specific application requirements.

For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the signal at the inputs of the ADC during the small acquisition time window.

For AC signals, keep the filter bandwidth low to band-limit the noise fed into the input of the ADC, thereby increasing the SNR of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected from each input pin of the ADC to the ground (as shown in Equation 3 and Figure 10).

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 15 times the specified value of the ADC sampling capacitance. For the ADS9110, the input sampling capacitance is equal to 60 pF, thus it is recommended to keep C_{FLT} greater than 900 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (3)$$

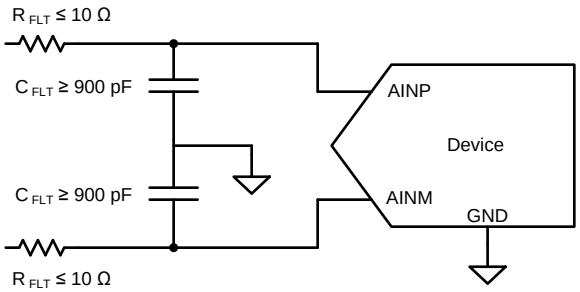

Figure 10. Anti-aliasing Filter Configuration—Diagram

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For the ADS9110, limiting the value of R_{FLT} to a maximum of 10 Ω is recommended to avoid any significant degradation in linearity performance. The tolerance of the selected resistors must be kept less than 1% to keep the inputs balanced. The driver amplifier must be selected such that its closed-loop output impedance is at least five times lesser than the R_{FLT}.

4.1.1.2 RC Filter Passive Components Selection

The critical passive components are resistor (R_{FLT}) and capacitor (C_{FLT}) for RC filter. The resistor tolerance must be 1% because use of differential capacitor at input balances the effect due to any resistor mismatch. The type of capacitor should be COG (NPO) because it has high Q and low temperature coefficient and stable electrical characteristics over voltage and frequency and time variations.

To Select C_{FLT}

The input capacitance for the ADS9110 is 60 pF. The filter capacitor C_{FLT} should be 20 times greater that sampling capacitor of ADC.

$$C_{FLT} \geq 20 \times C_{SH} = 20 \times 60\ pF = 1.2\ nF \tag{4}$$

For common mode, the capacitor value selected was 10 nF for optimum design performance.

To select R_{FLT}

The output resistance of OPA625 is R_O = 1 Ω and substituted in following formula:

$$R_{FLT} \geq \frac{R_O}{9} = \frac{1\ \Omega}{9} = 0.111 \tag{5}$$

So, the value of R_{FLT} can be chosen greater than 0.1 Ω.

The R_{FLT} and C_{FLT} are calculated for 7-MHz, –3-dB cutoff frequency with above R and C value consideration. For the RC filter cut-off frequency:

$$F_{-3dB\_RC\_CUTOFF} = \frac{1}{2 \times \pi \times R_{FLT} \times C_{FLT}} \quad (6)$$

where

- C_{FLT} = 10 nF
- $F_{-3dB\_RC\_CUTOFF}$ = 7 MHz

$$R_{FLT} = \frac{1}{2 \times \pi \times F_{RC\_CUTOFF} \times C_{FLT}} \quad (7)$$

$$= \frac{1}{2 \times \pi \times 2 \times 10^{6} \times 10 \times 10^{-9}} = 2.27\ \Omega$$

4.1.1.2.1 Input Low-Pass Band Limiting Filter

The overall input signal bandwidth is limited by the input buffer amplifier configured as 160-kHz anti-aliasing filter formed 1-kΩ resistor and 1-nF capacitor at amplifier feedback.

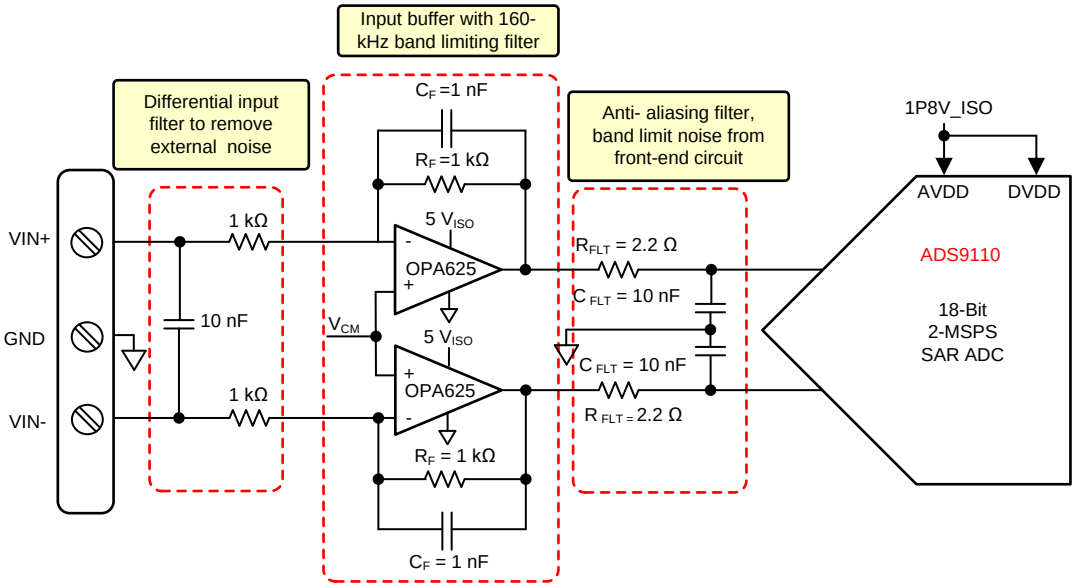

Figure 11. TIDA-00732 Analog Front-End

4.1.2 Common-Mode Voltage (V_{CM})

The onboard reference REF5045 (ultra-low noise, low drift and high precision) generates both ADC common-mode voltage and ADC reference voltage.

To exercise the complete dynamic range of the ADS9110, the common-mode voltage at the ADS9110 inputs is established at a value of 2.25 V (4.5 V / 2) by using the non-inverting pins of the OPA625 amplifier's on-board reference REF5045 (ultra-low noise, low drift, and high precision) used to generate 4.5 V.

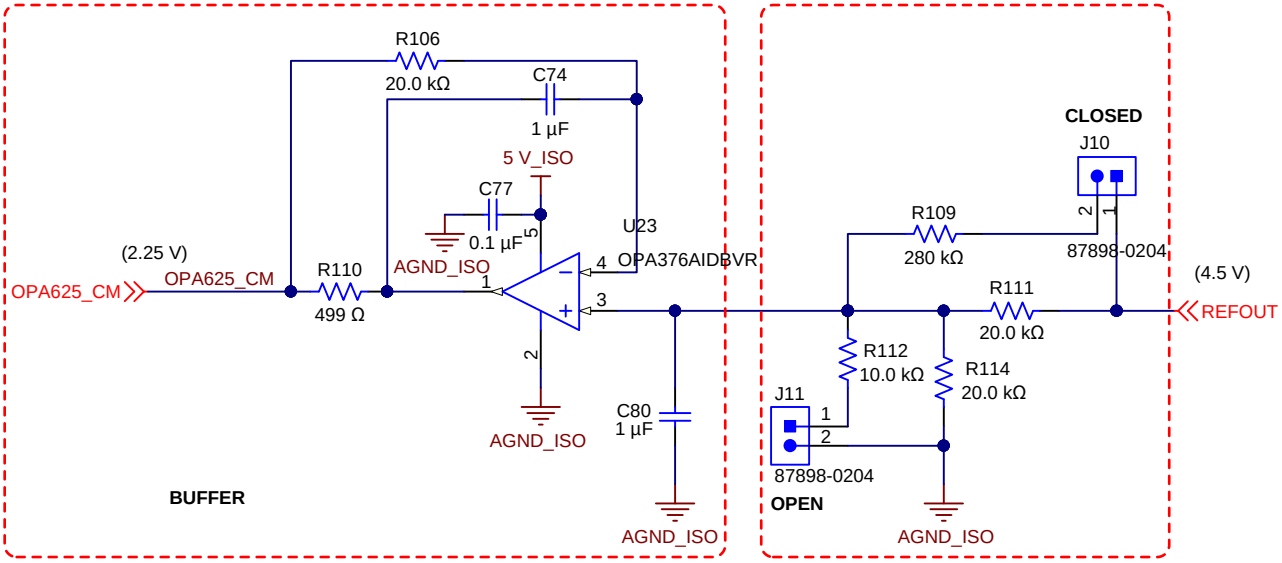

Figure 12. Common-Mode Voltage

4.1.3 Reference Buffer Circuit

The reference driver circuit, illustrated in Figure 13, generates a voltage of 4.5-V DC using a single 5-V supply. This circuit is suitable to drive the reference of the ADS9110 at higher sampling rates up to
2 MSPS. The reference voltage of 4.5 V in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

The reference buffer is designed with the OPA625 and OPA378 in a composite architecture to achieve superior DC and AC performance at a reduced power consumption, compared to using a single high-performance amplifier. The OPA625 is a high-bandwidth amplifier with a very low open-loop output impedance of 1 Ω up to a frequency of 1 MHz. The low open-loop output impedance makes the OPA625 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The relatively higher offset and drift specifications of the OPA625 are corrected by using a DC-correcting amplifier (OPA378) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA378.

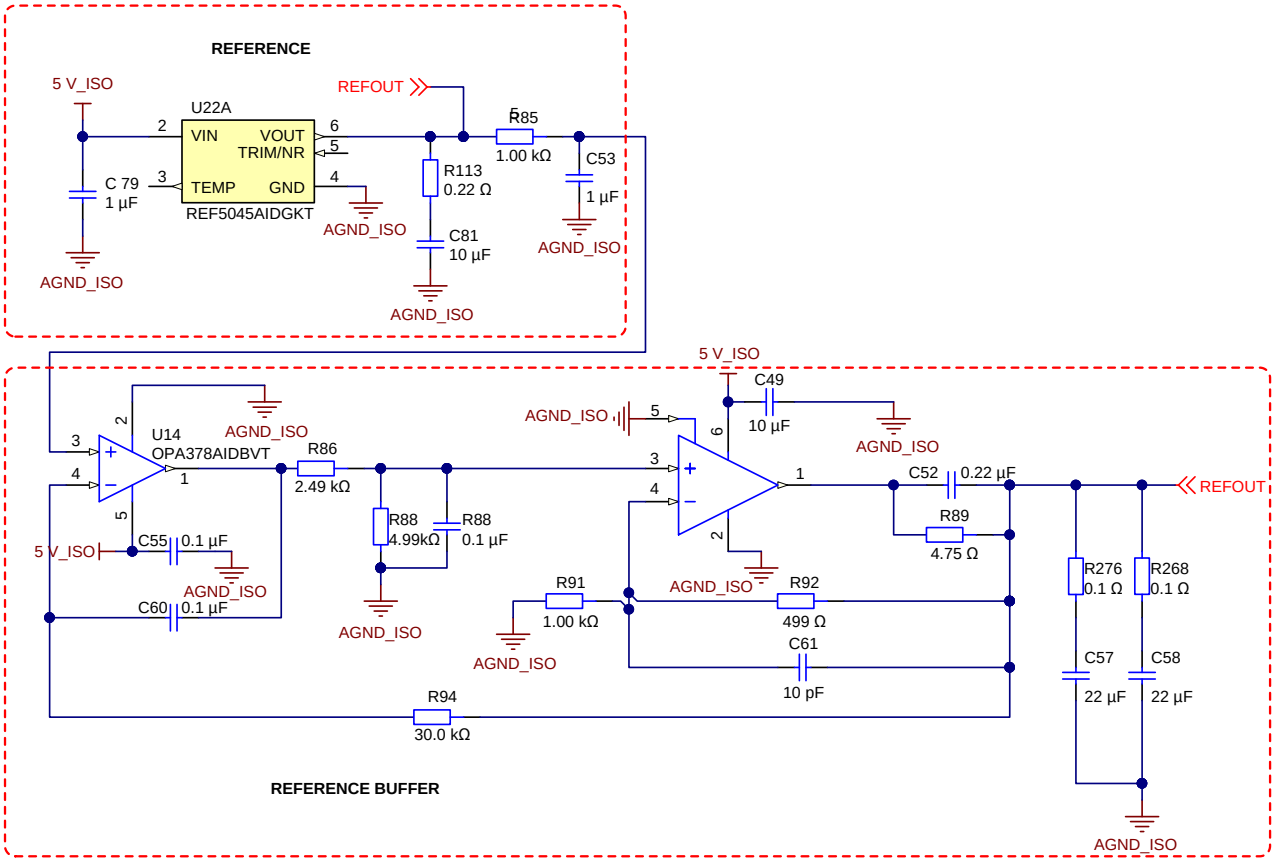

Figure 13. Reference Buffer Circuit

4.1.4 ADC SPI (multiSPI)

The ADS9110 has a integrated multiSPI that is backward compatible with the traditional SPI and configurable SDO lines (1, 2, and 4) . The configurable feature simplifies board layout, timing and firmware and achieves high throughput at lower clock speeds, thus allowing easy interface with embedded microcontrollers, digital signal processors (DSPs), and field programmable gate arrays (FPGAs). Figure 14 shows multiSPI and detailed information can be found in ADS9110 datasheets.

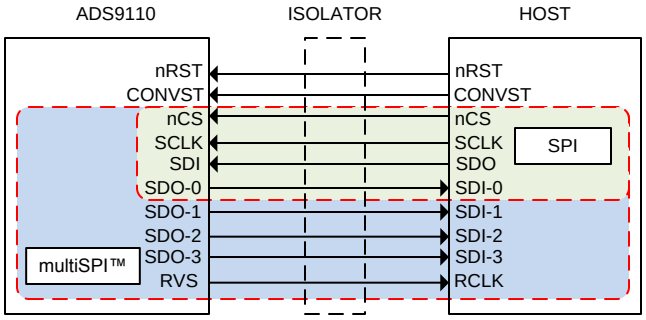

Figure 14. multiSPI

4.2 Clock Circuit Section

The clock source is an essential component in signal chain specifically when driving the sample clock input of ADC. The clock optimization is a big challenge in system design.

The clock jitter directly impacts ADC SNR performance greatly at higher input signal frequency. Therefore, select the right clock source to optimize signal chain performance.

This design has two master clock sources that can be used for ADC sample clock generation, jitter cleaner logic, and host interface synchronization:

1. Crystal oscillator (3.3 V, 125 MHz, 50 ppm, low jitter, 1.9-ps jitter)
2. LMK61E2: Programmable crystal oscillator (3.3 V, 150 MHz, 90-fs jitter)

Table 4 shows resistor jumpers selecting one of these clock sources:

Table 4. Master Clock Selection

SLNO	MASTER CLOCK	RESISTOR MOUNTING	REMARKS
1	Crystal oscillator	R167 — Populate R269 — Do not populate	3.3 V, 125 MHz, 50 ppm, low jitter, 1.9-ps jitter
2	Programmable crystal oscillator	R167 — Do not populate R269 — Populate	3.3 V, 150 MHz, 90-fs jitter (Frequency of oscillator must be programmed to 125 MHz through I^2C interface)

4.3 Isolator Section

The TIDA-00732 uses TI's ISO784x and ISO1541 series isolators to establish digital isolation in the system. The ISO784x series supports signaling rate up to 100 Mbps with typically low propagation delay (11 ns) and wide supply voltage (2.25 to 5.5 V). These isolators are reinforced with very high immunity and a 5.7-kV_{RMS} isolation voltage with very low jitter.

The system requires six isolation channels for standard SPI communication and ten isolation channels for multiSPI.

The ISO784x isolators used for SPI, ADC control lines and ISO1541 bi-directional isolator is used for I^2C isolation.

4.4 Power Section

The design requires isolated and non-isolated power rails to various components. The block diagram in Figure 15 describes the power supply tree for both isolated and non-isolated sections.

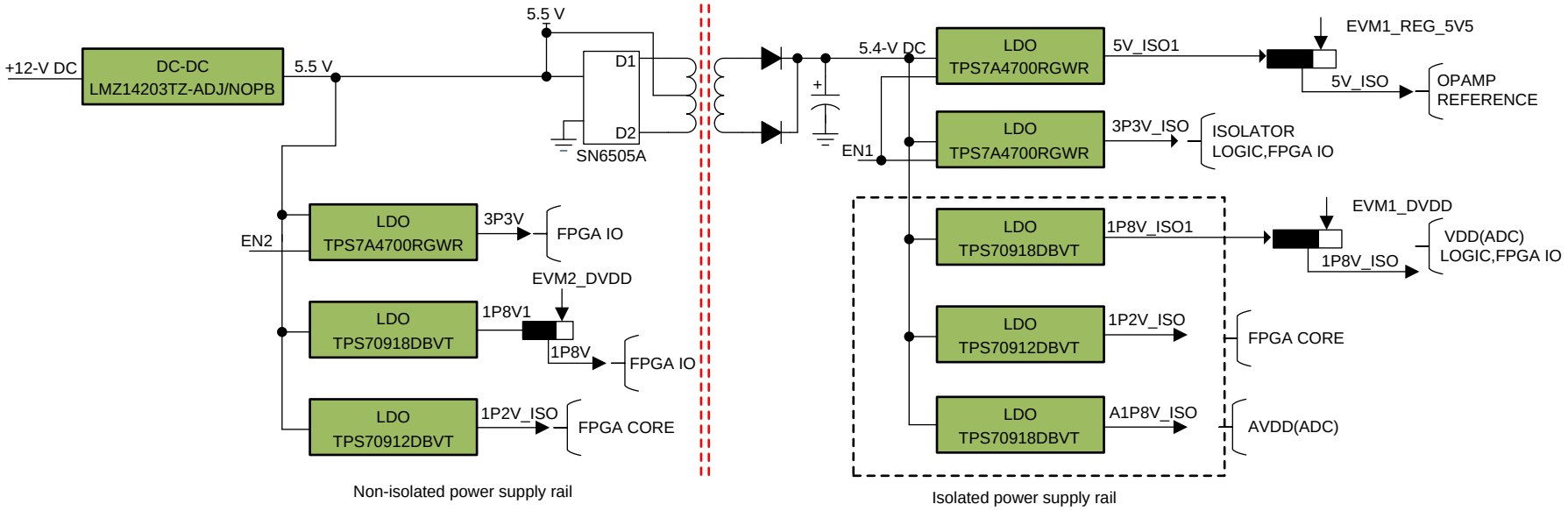

Figure 15. Power Supply Block Diagram of TIDA-00732

4.4.1 DC-DC

4.4.1.1 LMZ14203TZ-ADJ

The LMZ14203TZ-ADJ simple switcher is capable of accepting 6- to 46-V DC input and deliver a 0.8- to 6-V output with 90% efficiency. The undervoltage lockout is selected at 7.97 V, which helps to enable the LMZ4203TZ-ADJ.

To Set 5-V Output Voltage

The resistor RFBT (R220) and RFBB (R223 + R225) decide the output voltage of the LMZ14203TZ-ADJ.

For a 5-V output, the ratio for

$$\frac{RF_{BT}}{RF_{BB}} = \left(\frac{5}{0.8}\right) - 1 = 5.25 \quad (8)$$

Select $RF_{BT} = \frac{5.62K}{5.25} = 1.07K$

So R220 = 5.62K , R223 = 1.07K, and R225 = 0 Ω

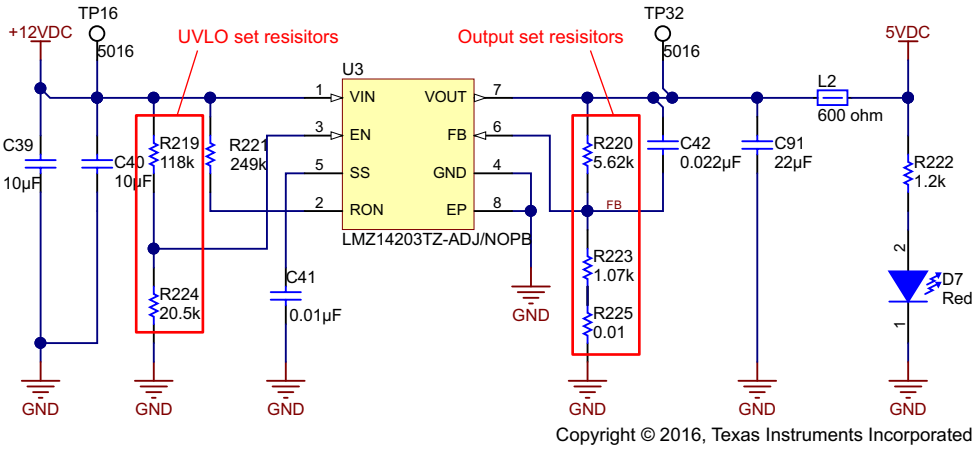

Figure 16. DC-DC Power Supply

4.4.2 LDO

4.4.2.1 TPS7A4700RGWR

The TPS7A4700 is a positive voltage (36 V), ultralow-noise (4 μV_{RMS}) LDO capable of sourcing a 1-A load. The TPS7A470x is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering op amps, ADCs, DACs, and other high-performance analog circuitry.

The TPS7A4700RGWR has ANY-OUT™ programmable pins to program desired output voltage. The sum of the internal reference voltage (V_{REF} = 1.4 V) plus the accumulated sum of the respective voltages is assigned to each active pins.

The ANY-OUT™ pins (Pin8, Pin1, and Pin12) are programmed to active low to get 3.3 V at output.

4.4.2.2 TPS7091XDBVT

The TPS709 series of linear regulators are ultralow, quiescent current devices designed for power sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. The TPS709 series accepts 2.7- to 30-V input voltage and deliver fixed output voltage 1.2 to 6.5 V with maximum 200-mA output current. The TPS70918DBVT and TPS70912 generate 1.8 V and 1.2 V, respectively, from 5-V DC of the LMZ14203TZ-ADJ DC-DC.

These supply rails power up both FPGA cores and IOs of the isolated and non-isolated section.

4.4.3 Transformer (750315240) and Push-Pull Transformer Driver (SN6505A)

The SN6505 is a transformer driver designed for low-cost, small form-factor, isolated DC-DC converters using push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals that alternately turn the two output transistors on and off.

The SN6505 transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 3 to 5.5 V. While converter designs with higher output voltages are possible, take care that higher turns ratios do not lead to primary currents that exceed the SN6505 specified current limits.

The TIDA-00732 uses the recommended transformer inform the SN6505A datasheet. For transformer selection and isolation power supply design, see the SN6505A datasheet. Table 5 shows key parameters of the transformer.

Table 5. Transformer Specification (Part No: 750315240, Mfr: WE)

PARAMETER	VALUE
Voltage-time	23 µs
Turns ratio	1.1:1 ±2%
Switching frequency	150 kHz min
Di-electric	6250 RMS, 1 sec

4.5 Host Interface

This design supports the following host interfaces to evaluate system performance:

- Precision host interface (PHI)
  PHI is TI's SAR ADC evaluation platform, which supports the entire TI SAR ADC family. By using PHI, the TIDA-00732 easily communicates with the host PC using a USB interface. PHI supports the ADS9110 multiSPI and onboard configuration I^2C EEPROM interface.

  PHI GUI software can be used to evaluate both AC and DC parameter of the ADS9110. For more information on PHI, refer to ADS9110 EVM-PDK.
- Beaglebone Black interface
  The TIDA-00732 has Beaglebone Black interface, which can be used to interface the Sitara™ ARM® embedded processor and make the DAQ system with an embedded platform.

5 Getting Started Hardware

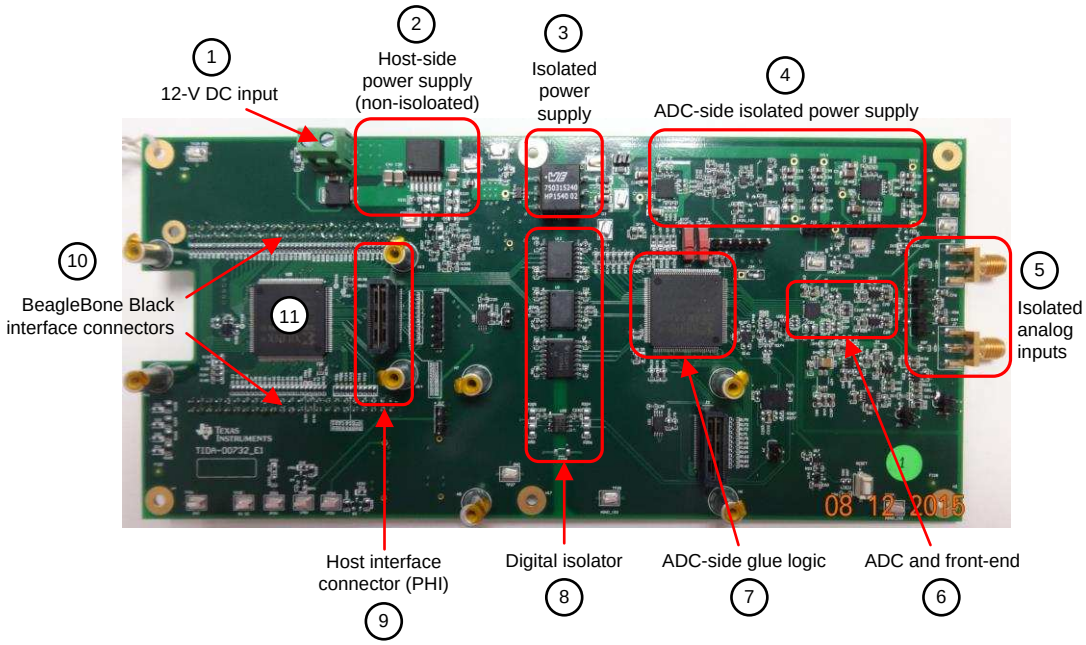

Figure 17. TIDA-00732 Hardware

5.1 Hardware Functional Block

Figure 17 shows various hardware functional blocks of the TIDA-00732 and function of each block:

1. 12-V DC power supply input connector accepts 9- to 12-V DC input to power the TIDA-00732.
2. The host side DC-DC buck convertor generates 5 V from the 12-V input.
3. An isolation transformer for power supply isolation and isolated power is generated with the SN6506 push pull transformer driver.
4. Isolated power supply rails block that generates 5-V, 3.3-V, 1.8-V and 1.2-V power rails.
5. Differential analog inputs connector.
6. Analog front-end circuits (ADC ADS9110, OPA625, REF4505).
7. FPGA that holds CONVST signal generation logic and glue logic for the interface.
8. Digital isolator for data isolation (SPI and I^2C).
9. PHI interface connector, which uses the TIDA-00732 to communicate with the host through USB interface.
10. Beaglebone Black interface, which allows the TIDA-00732 to communicate with the embedded platform.
11. FPGA to implement glue logic for PHI and Beaglebone Black interface selection.

5.2 Headers and Jumper Setting

The TIDA-00732 has a number of jumpers that must be selected properly before powering up the module.

1. Input common-mode jumper (see Table 6)

Table 6. Input Common-Mode Selection

J10	J11	DESCRIPTION
CLOSE	OPEN	2.25-V select (default)
CLOSE	CLOSE	See the ADS9110 EVM (Section 2.2.2) for other common-mode settings. EVM Jumper reference J10 and J11 corresponding to TIDA-00732 reference of J1 and J2, respectively.
OPEN	CLOSE	
OPEN	OPEN	

2. Power supply jumper (see Table 7)

Table 7. Power Supply Selection

REFERENCE	DEFAULT	DESCRIPTION
J17	2,3	1P8V source selection
		Pin 1,2—From PHI board
		Pin 2,3—Onboard
J12	2,3	5-V source selection
		Pin 1,2—From PHI
		Pin 2,3—Onboard
J13	2,3	1P8V_ISO—Source selection
		Pin 1,2—From PHI
		Pin 2,3—Onboard
J24	2,3	FPGA (U24C)—IO Bank0 voltage selection
		Pin 1,2—3.3 V
		Pin 2,3—1.8 V
J4	OPEN	EEPROM (U21)—Write protect enable
		OPEN—Write protect enable
		CLOSE—Write protect disable
J21	OPEN	EEPROM (U28)—Write protect enable
		OPEN—Write protect enable
		CLOSE—Write protect disable

3. Mode selection jumper

   This mode selection jumper configures the TIDA-00732 in any one of the modes shown in Table 8.

Table 8. Mode Selection Switch

J16	J22	DESCRIPTION
1,2	1,2	PHI without jitter logic (default)
1,2	2,3	Reserved
2,3	1,2	PHI with jitter
2,3	2,3	Reserved

4. Programming header

   The programming of Xilinx FPGA can be done using the 6-pin header listed in Table 9.

Table 9. FPGA Programming Header

REFERENCE	DESCRIPTION
J14	FPGA(U24) JTAG Header
J19	FPGA(U25) JTAG Header

6 Getting Started Firmware

6.1 PHI GUI Panel

The PHI GUI software, which is based on the LabView™ platform, validates the TIDA-00732. Figure 18 shows the available test options in PHI GUI.

Figure 18. PHI GUI Demonstrate AC Parameter—Spectral Analysis

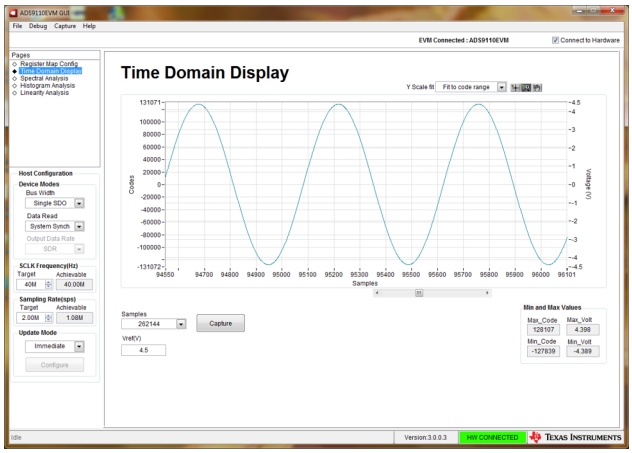

Figure 19. PHI GUI Demonstrate AC Parameter—Time Domain Display

The PHI GUI can be used to validate the following system key specifications:

1. Linearity analysis
   - DNL
   - INL
   - Accuracy
2. Histogram analysis
   - Effective resolution
3. Spectral analysis
   - SNR
   - THD
   - SFDR
   - SINAD
   - ENOB

PHI GUI software can be found at http://www.ti.com/product/ADS9110/toolssoftware.

7 Test Setup

Figure 20 shows the TIDA-00732 test setup to validate complete signal chain performance of isolated high-speed, high SNR (18-bit, 2-MSPS) analog input DAQ module.

The test needs to evaluate the performance of a high-speed (2-MSPS) and high-resolution (18-bit) system that is compliant with testing requirements. The setup has a DS360, Standard Research Systems precision ultralow distortion waveform generator, which is capable of generating a sine pattern with a signal frequency range of 10 mHz to 200 kHz. The device needs high precision with very low ripple power supply to power entire system. This design requires 9- to 12-V DC at 250 mA with high precision and low ripple power. The 12-V DC voltage is generated using Keithley triple output power supply (2230G). It is capable of generating up to 30 V with 0.03% voltage accuracy and 0.1% current accuracy with simultaneous voltage and current indication.

The data capturing is established using USB 2.0 interface. The testing computer must have one USB port and support USB 2.0 specification.

Sometimes the signal source may also have noise on top of the signal while generating a sine wave with 100 kHz. To remove this unwanted noise, a 100-kHz differential band pass filler is connected in between the signal source and TIDA-00732 input connector. This will attenuate input noise at a 100-kHz band.

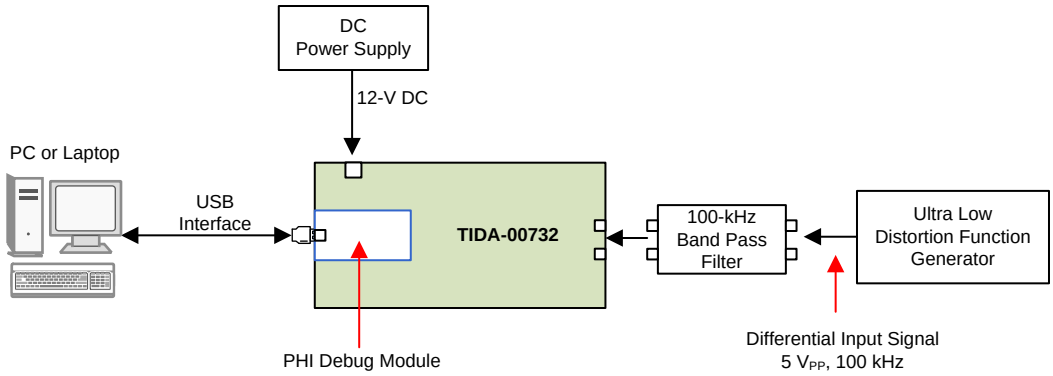

Figure 20. TIDA-00732 Test Setup

The PHI GUI software must be installed in the host computer before testing.

1. Plug the PHI interface board to the Samtec connector (J18).
2. Connect 12-V DC of power to the J5 connector. Ensure the positive terminal is connected to the positive input (Pin 2 of J5) and the negative terminal is connected to the negative input (Pin 1 of J5).
3. Connect the differential output of function generator to the differential input terminal (J7 and J8 SMA connector) of the TIDA-00732 board (for a 100-kHz input signal frequency, connect the 100-kHz band pass filter in between signal source and the TIDA-00732 board). Also, make sure both differential signals are balanced and configure as shown in Table 10.
4. Connect the PHI module to the PC or laptop using microUSB cable.
5. Switch on the power supply.
6. Switch on the signal source and set the signal source parameter. Then, enable the output.
7. Run the PHI GUI software, go to spectrum analysis tab and capture result with various input signal frequency.

Table 10. Test Conditions

FUNCTION GENERATOR	
Pattern	Sine
Voltage	7.23 V_{PP} (Adjust to cover full input dynamic range)
Frequency	2 kHz and 100 kHz
Source impedance	150 Ω
POWER SUPPLY	
12-V DC at 250 mA	

To evaluate jitter mitigation and SNR performance improvement in the TIDA-00732, the following test cases were created:

1. Configure the TIDA-00732 as no jitter cleaning mode by using mode switch (J16, J22).
2. Generate a sine wave with 7.32 V_{PP} (adjust to cover full input dynamic range), 2 kHz.
3. Run PHI software in debug mode.
4. Go to the FFT tab and capture SNR, THD, ENOB.

The test results are taken for both 2-kHz and 100-kHz input frequency with and without jitter cleaner mode.

NOTE:

1. While testing with a 100-kHz input signal frequency, bandpass filter is used in between the signal source and the TIDA-00732 module.
2. Load the corresponding FPGA MCS file for with or without jitter mode.

8 Test Data

Table 11 shows test results for with and without jitter cleaning mode with input signal frequencies of 2 kHz and 100 kHz. The datasheet SNR performance of the ADS9110 at a 100-KHz input signal is 95.5 dB. Table 10 shows that the SNR performance of the host generated CONVST (without jitter cleaning mode) is 82 dB while the locally generated CONVST (with jitter cleaning mode) is 94.34 dB, which is close to the datasheet's specification. This result shows that signal chain performance degraded due to isolator jitter, and the solution provided in the TIDA-00732 gives almost a 12-dB improved SNR performance.

Also, the serial data rate of SPI can be reduced to 49 MHz by using multiSPI while operating the ADS9110 with a maximum sample rate of 2 MSPS.

Table 11. Test Result Comparison

PARAMETER	TIDA-00732 TEST RESULT				
	HOST GENERATED CONVST (WITHOUT JITTER CLEANING)		LOCALLY GENERATED CONVST (WITH JITTER CLEANING)		
f_{IN} (kHz)	2	100	2	100	100
SCLK (MHz)	49	49	49	49	49
MODE	QSDO	QSDO	QSDO	QSDO	QSDO
Sample rate (MSPS)	1.64	1.64	1.64	1.64	2
SNR (dB)	98.89	82.00	99.32	94.34	94.28
THD (dB)	121.01	112.64	120.78	113.86	113.72
ENOB	15.61	13.32	16.20	15.37	15.36

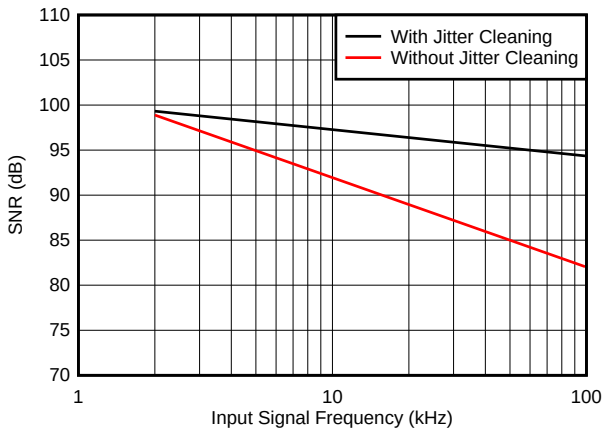

Figure 21. SNR Performance Comparison

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00732.

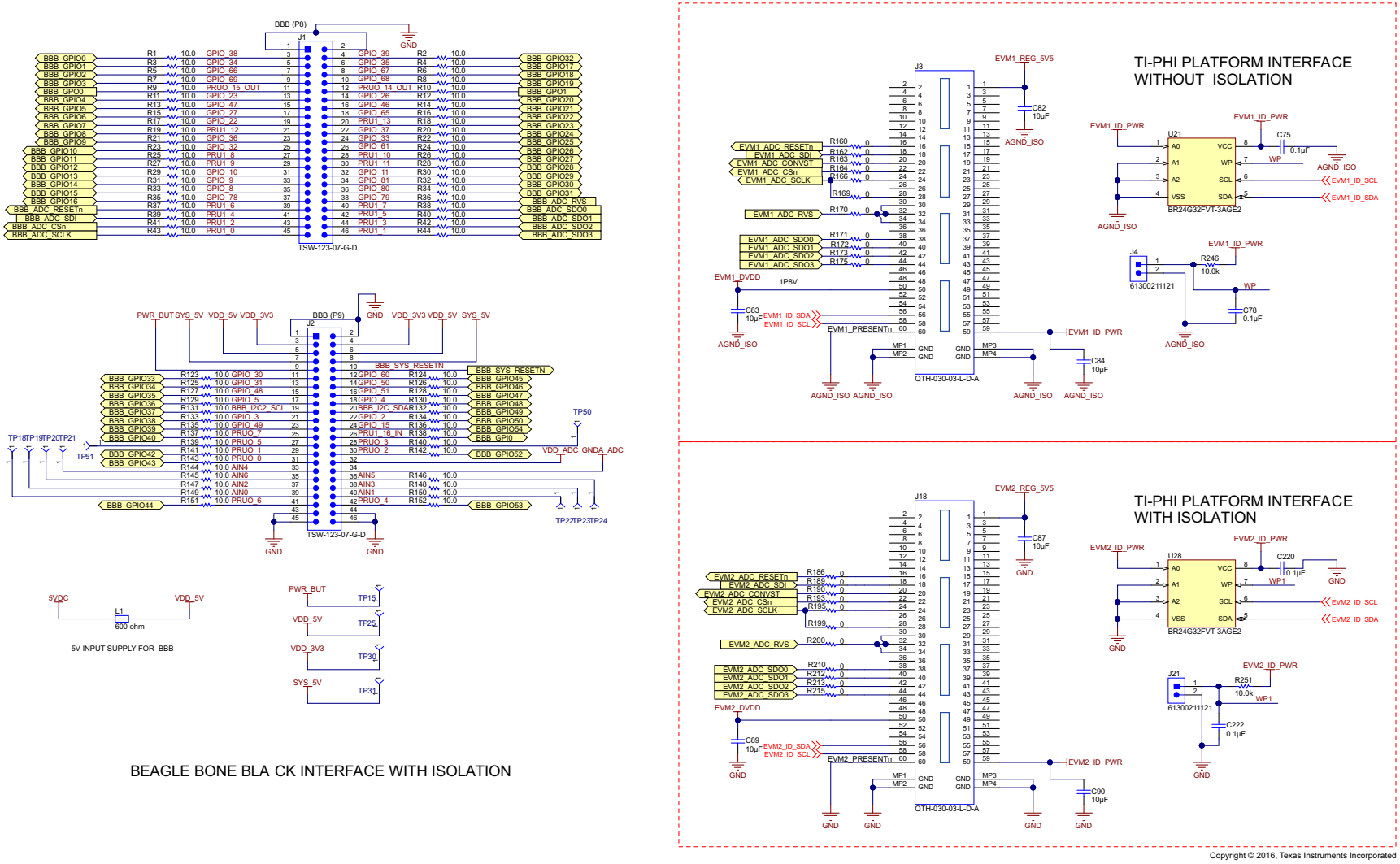

Figure 22. Connector Schematic

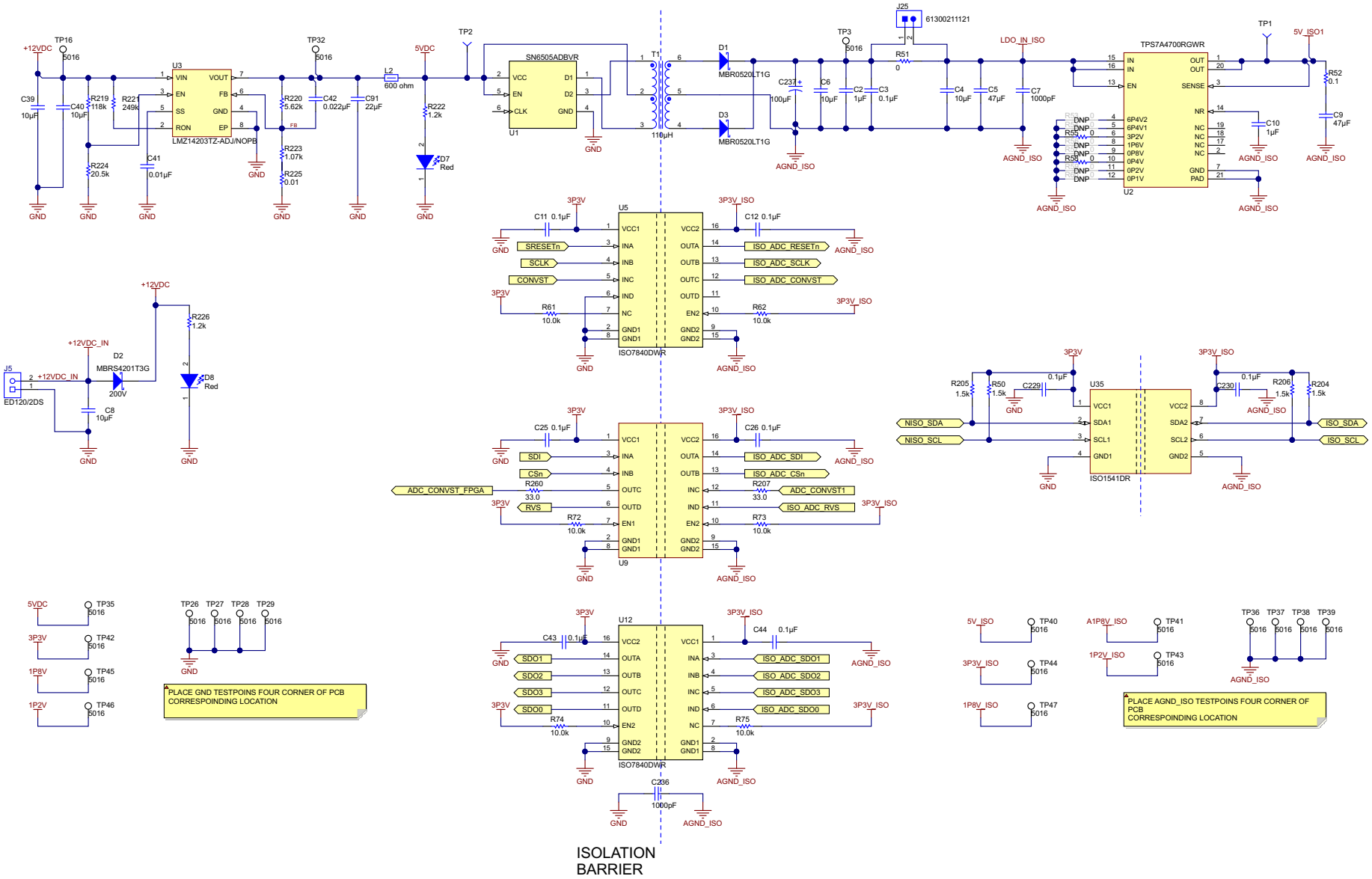

Figure 23. Power and Isolators Schematic

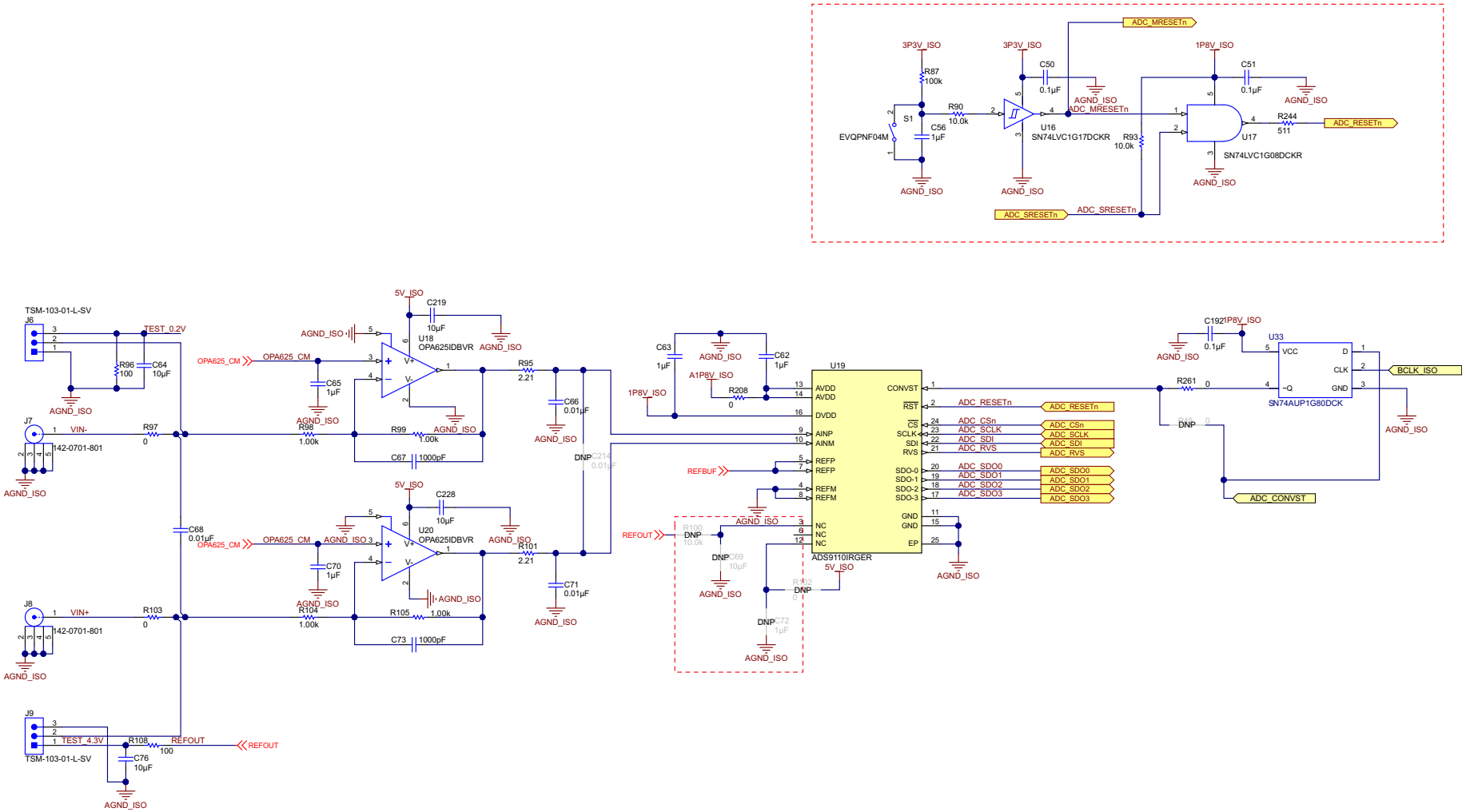

Figure 24. Analog Front-End and ADC Schematic

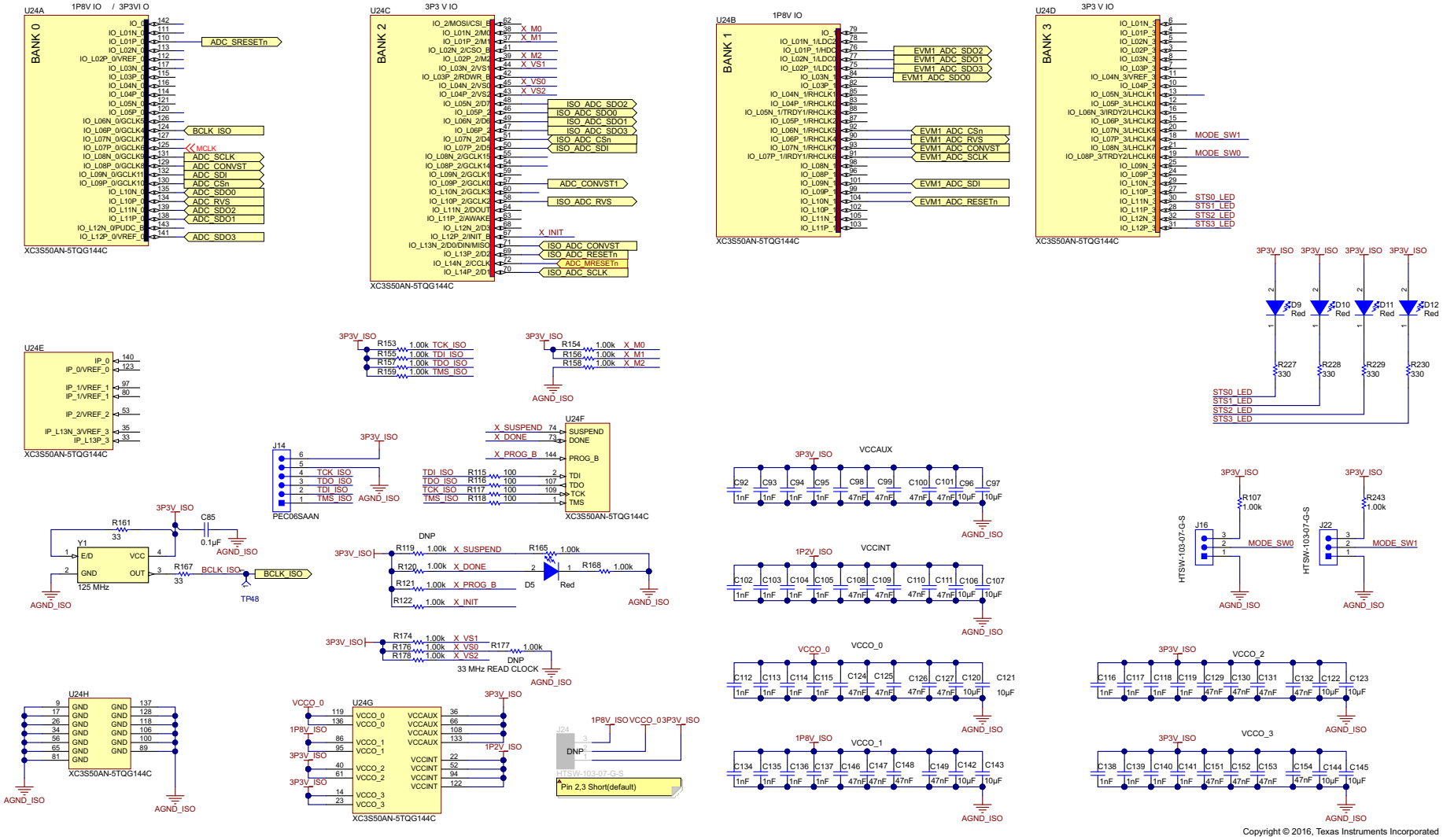

Figure 25. FPGA 1—Isolated End Schematic

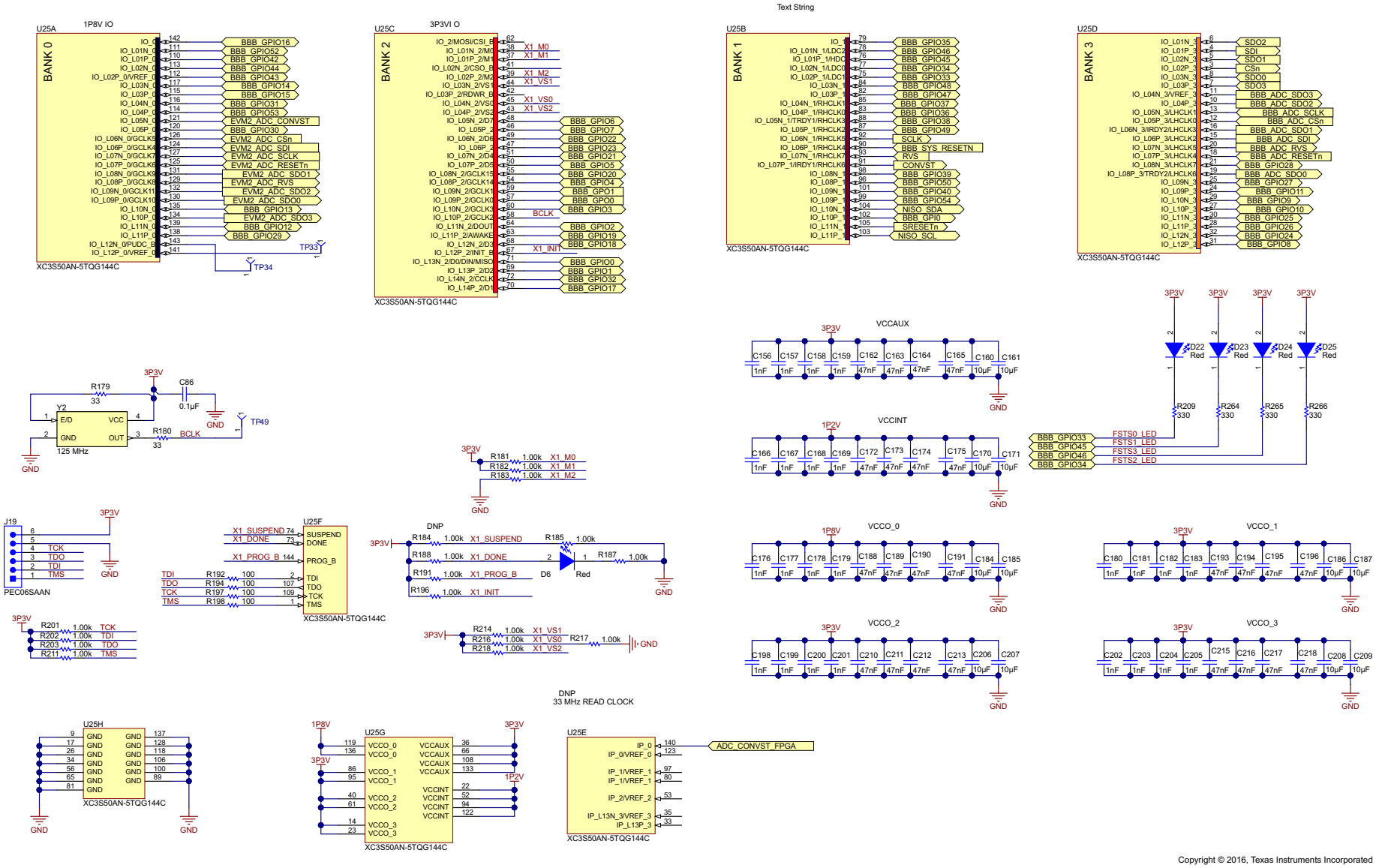

Figure 26. FPGA 2—Non-Isolated End Schematic

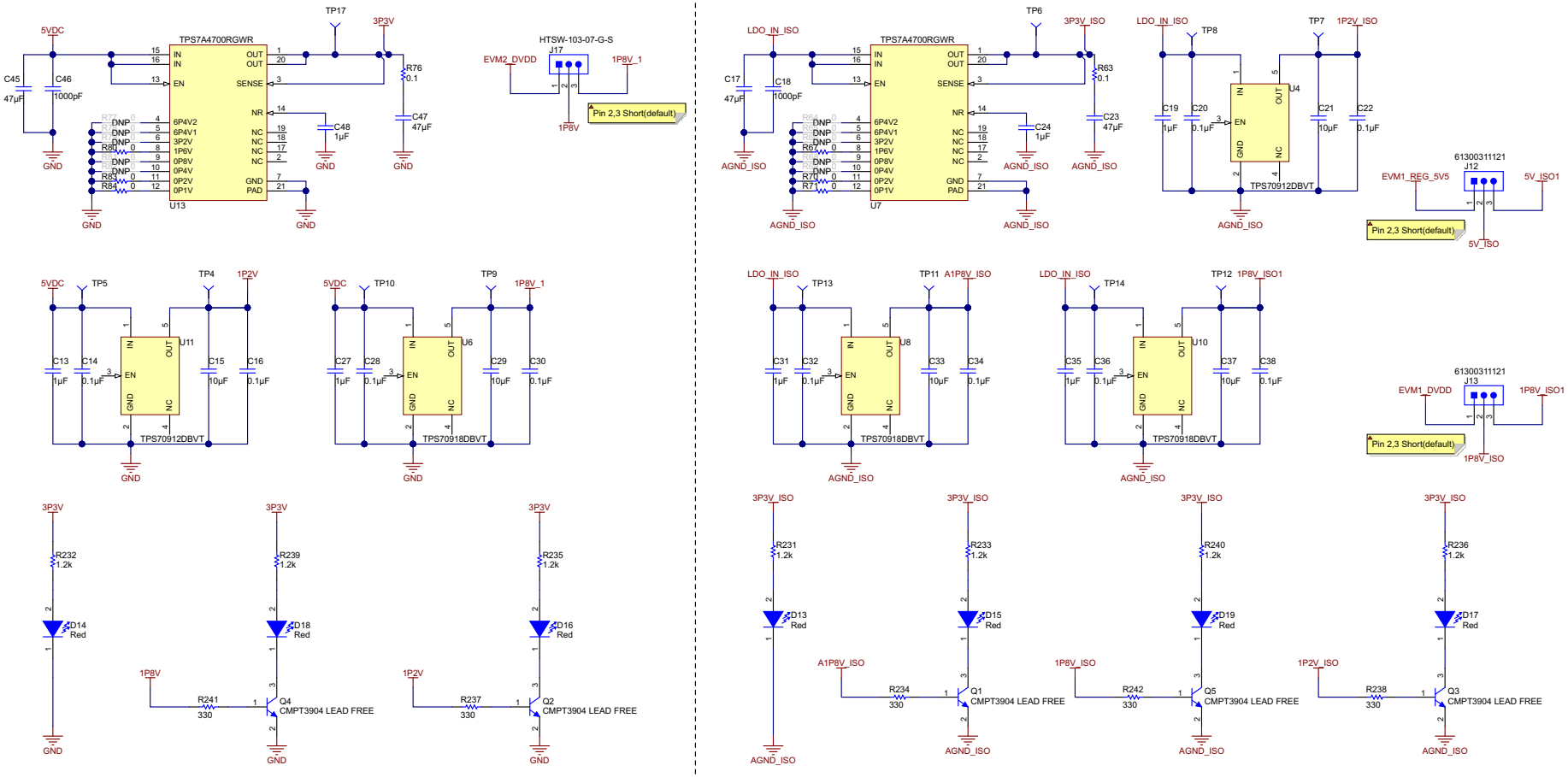

Figure 27. Isolated and Non-Isolated LDOs Schematic

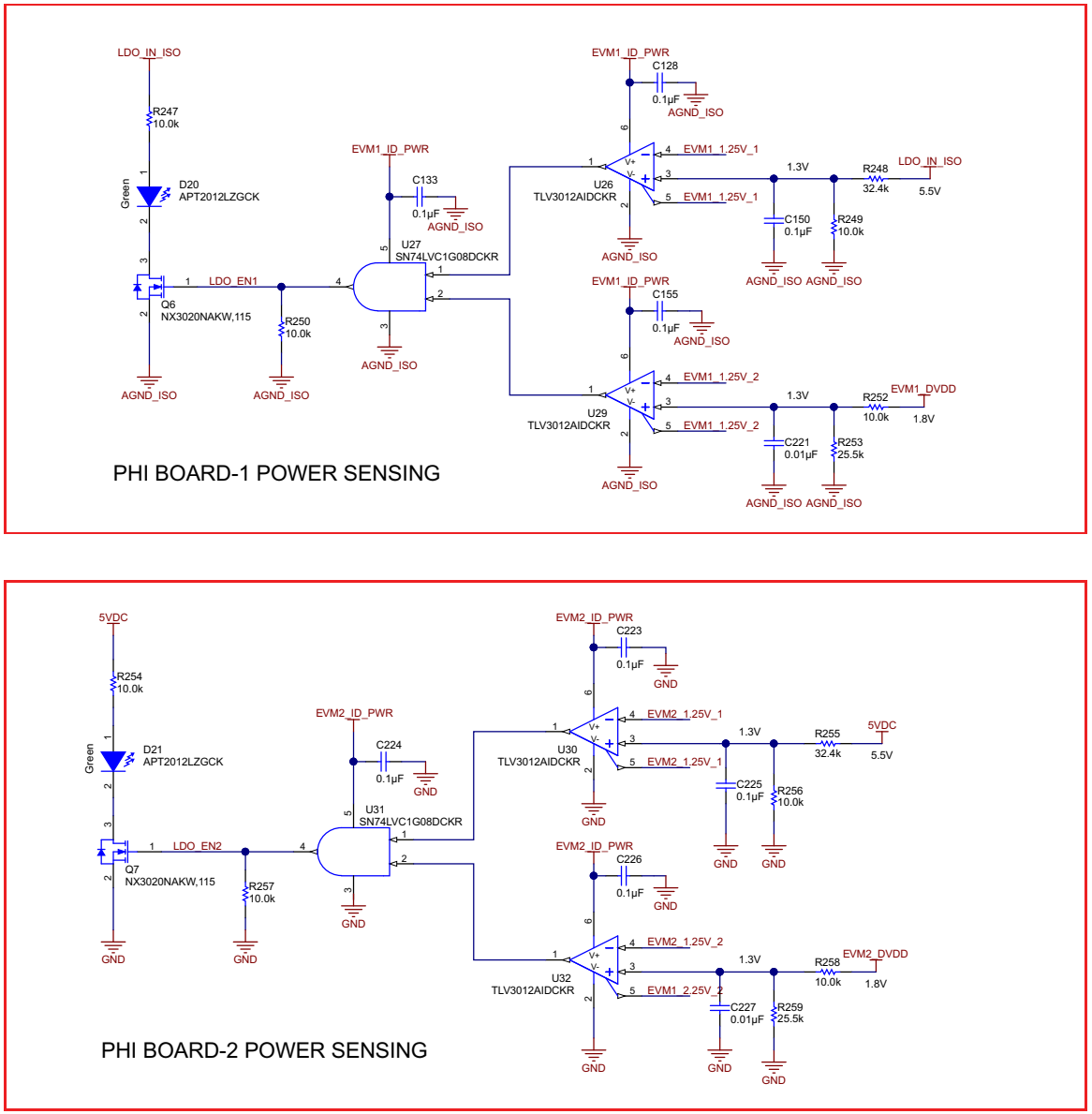

Figure 28. Power Sense—PH1 and PH2 Interface Schematic

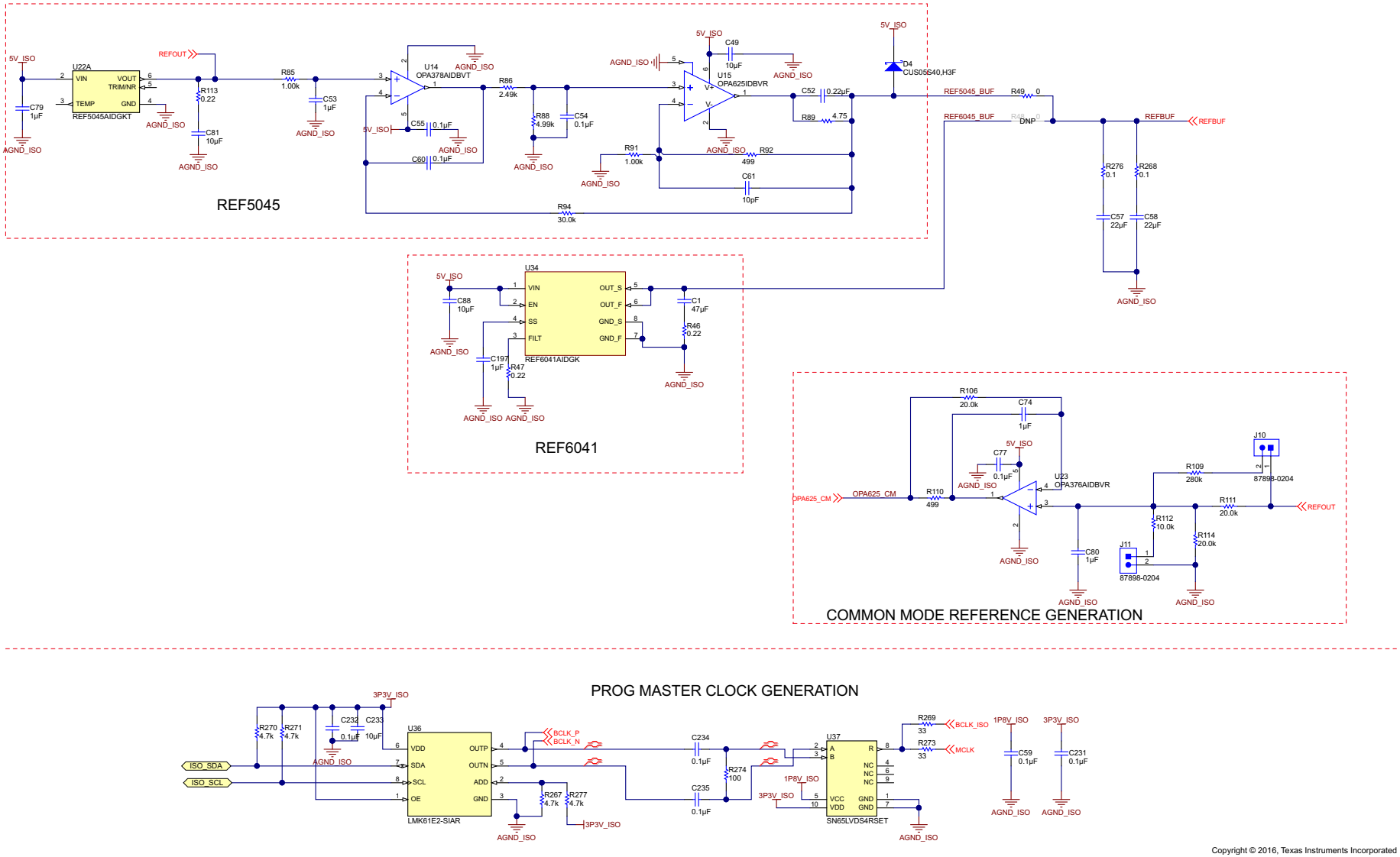

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Figure 29. ADC Reference Selection Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00732.

Table 12. BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB1	1		TIDA-00732	Any	Printed Circuit Board	
2	C1	1	47uF	GRM32ER71A476KE15L	MuRata	CAP, CERM, 47 µF, 10 V, +/- 10%, X7R, 1210	1210
3	C2, C10, C24, C48, C53, C56, C62, C63, C65, C70, C74, C79, C80	13	1uF	GRM188R71E105KA12D	MuRata	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603
4	C3, C11, C12, C25, C26, C43, C44, C51, C59, C75, C78, C85, C86, C128, C133, C150, C155, C192, C220, C222, C223, C224, C225, C226, C229, C230, C231	27	0.1uF	GRM155R71C104KA88D	MuRata	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402	0402
5	C4, C64, C76, C81, C82, C83, C84, C87, C89, C90	10	10uF	GRM21BR71A106KE51L	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805	0805
6	C5, C9, C17, C23, C45, C47	6	47uF	C3216X5R1E476M160AC	TDK	CAP, CERM, 47 µF, 25 V, +/- 20%, X5R, 1206_190	1206_190
7	C6, C8	2	10uF	C3216X7R1E106M160AE	TDK	CAP, CERM, 10 µF, 25 V, +/- 20%, X7R, 1206_190	1206_190
8	C7, C18, C46, C67, C73	5	1000pF	GRM1885C1H102FA01J	MuRata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603
9	C13, C19, C27, C31, C35	5	1uF	08055C105KAT2A	AVX	CAP, CERM, 1uF, 50V, +/- 10%, X7R, 0805	0805
10	C14, C16, C20, C22, C28, C30, C32, C34, C36, C38	10	0.1uF	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, 0603	0603
11	C15, C21, C29, C33, C37	5	10uF	0805YD106MAT2A	AVX	CAP, CERM, 10uF, 16V, +/- 20%, X5R, 0805	0805
12	C39, C40	2	10uF	UMK325AB7106KM-T	Taiyo Yuden	CAP, CERM, 10 µF, 50 V, +/- 10%, X7R, 1210	1210
13	C41	1	0.01uF	C0603C103J5RACTU	Kemet	CAP, CERM, 0.01uF, 50V, +/- 5%, X7R, 0603	0603
14	C42	1	0.022uF	08055C223KAT2A	AVX	CAP, CERM, 0.022uF, 50V, +/-10%, X7R, 0805	0805

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
15	C49, C96, C97, C106, C107, C120, C121, C122, C123, C142, C143, C144, C145, C160, C161, C170, C171, C184, C185, C186, C187, C206, C207, C208, C209, C219, C228, C233	28	10uF	ZRB18AD71A106KE01L	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7T, 0603	0603
16	C50	1	0.1uF	0603YC104JAT2A	AVX	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0603	0603
17	C52	1	0.22uF	0805YC224JAT2A	AVX	CAP, CERM, 0.22 µF, 16 V, +/- 5%, X7R, 0805	0805
18	C54, C55, C60, C77, C232	5	0.1uF	C0603C104J3RACTU	Kemet	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603	0603
19	C57, C58	2	22uF	GRM188R60J226MEA0J	MuRata	CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603	0603
20	C61	1	10pF	C0603C100F5GAC7867	Kemet	CAP, CERM, 10 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603
21	C66, C71, C221, C227	4	0.01uF	GRM155R71H103KA88D	MuRata	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0402	0402
22	C68	1	0.01uF	C0805C103F1GACTU	Kemet	CAP, CERM, 0.01 µF, 100 V, +/- 1%, C0G/NP0, 0805	0805
23	C88	1	10uF	GRM21BR71A106KE51L	MuRata	CAP, CERM, 10uF, 10V, +/- 10%, X7R, 0805	0805
24	C91	1	22uF	C3225X5R1A226M	TDK	CAP, CERM, 22uF, 10V, +/- 20%, X5R, 1210	1210
25	C92, C93, C94, C95, C102, C103, C104, C105, C112, C113, C114, C115, C116, C117, C118, C119, C134, C135, C136, C137, C138, C139, C140, C141, C156, C157, C158, C159, C166, C167, C168, C169, C176, C177, C178, C179, C180, C181, C182, C183, C198, C199, C200, C201, C202, C203, C204, C205	48	1000pF	C1005X7R1H102M	TDK	CAP, CERM, 1000 pF, 50 V, +/- 20%, X7R, 0402	0402

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
26	C98, C99, C100, C101, C108, C109, C110, C111, C124, C125, C126, C127, C129, C130, C131, C132, C146, C147, C148, C149, C151, C152, C153, C154, C162, C163, C164, C165, C172, C173, C174, C175, C188, C189, C190, C191, C193, C194, C195, C196, C210, C211, C212, C213, C215, C216, C217, C218	48	0.047uF	GRM155R61A473KA01D	MuRata	CAP, CERM, 0.047 µF, 10 V, +/- 10%, X5R, 0402	0402
27	C197	1	1uF	GRM188R71A105KA61D	MuRata	CAP, CERM, 1uF, 10V, +/- 10%, X7R, 0603	0603
28	C234, C235	2	0.1uF	GRM155R61E104KA87D	MuRata	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X5R, 0402	0402
29	C236	1	1000pF	202R18W102KV4E	Johanson Technology	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, 1206_190	1206_190
30	C237	1	100uF	293D107X9020E2TE3	Vishay-Sprague	CAP, TA, 100 µF, 20 V, +/- 10%, 0.5 ohm, SMD	7343-43
31	D1, D3	2	20V	MBR0520LT1G	ON Semiconductor	Diode, Schottky, 20 V, 0.5 A, SOD-123	SOD-123
32	D2	1	200V	MBRS4201T3G	ON Semiconductor	Diode, Schottky, 200V, 4A, SMC	SMC
33	D4	1	40V	CUS05S40,H3F	Toshiba	Diode, Schottky, 40 V, 0.5 A, SOD-323	SOD-323
34	D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D22, D23, D24, D25	19	Red	150060RS75000	Wurth Elektronik	LED, Red, SMD	LED_0603
35	D20, D21	2	Green	APT2012LZGCK	Kingbright	LED, Green, SMD	LED_0805
36	FID4, FID5, FID6, FID7, FID8	5		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
37	H1, H2, H3, H4, H17, H18, H21, H22, H23, H24, H25, H26, H27, H28, H29	15		PMSSS 440 0025 PH	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4"
38	H5, H6, H7, H8, H13, H14, H15, H16	8		9774050360R	Wurth Elektronik	ROUND STANDOFF M3 STEEL 11MM	ROUND STANDOFF M3 STEEL 11MM
39	H9, H10, H11, H12, H19, H20, H30	7		1902C	Keystone	Standoff, Hex, 0.5"L #4-40 Nylon	Standoff
40	J1, J2	2		TSW-123-07-G-D	Samtec	Header, 2.54 mm, 23x2, Gold, TH	Header, 2.54 mm, 23x2, TH

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
41	J3, J18	2		QTH-030-03-L-D-A	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT
42	J4, J21, J25	3		61300211121	Wurth Elektronik eiSos	Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH
43	J5	1		ED120/2DS	On-Shore Technology	TERMINAL BLOCK 5.08MM VERT 2POS, TH	TERM_BLK, 2pos, 5.08mm
44	J6, J9	2		TSM-103-01-L-SV	Samtec	Header, 100mil, 3x1, Gold, SMT	Samtec_TSM-103-01-X-SV
45	J7, J8	2		142-0701-801	Johnson	Connector, End launch SMA, 50 ohm, SMT	End Launch SMA
46	J10, J11	2		87898-0204	Molex	Header, 2.54 mm, 2x1, Gold, R/A, SMT	Header, 2.54 mm, 2x1, R/A, SMT
47	J12, J13	2		61300311121	Wurth Elektronik eiSos	Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH
48	J14, J19	2		PEC06SAAN	Sullins Connector Solutions	Header, 100mil, 6x1, Tin, TH	TH, 6-Leads, Body 608x100mil, Pitch 100mil
49	J16, J17, J22	3		HTSW-103-07-G-S	Samtec	Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH
50	L1	1	600 ohm	HZ0805E601R-10	Laird-Signal Integrity Products	Ferrite Bead, 600 ohm @ 100 MHz, 0.5 A, 0805	0805
51	L2	1	600 ohm	MPZ2012S601A	TDK	Ferrite Bead, 600 ohm @ 100MHz, 2A, 0805	0805
52	LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W
53	Q1, Q2, Q3, Q4, Q5	5	40 V	CMPT3904 LEAD FREE	Central Semiconductor	Transistor, NPN, 40 V, 0.2 A, SOT-23	SOT-23
54	Q6, Q7	2	30V	NX3020NAKW,115	NXP Semiconductor	MOSFET, N-CH, 30 V, 0.18 A, SOT-323	SOT-323

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
55	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152	74	10.0	CRCW040210R0FKED	Vishay-Dale	RES, 10.0, 1%, 0.063 W, 0402	0402
56	R46, R47	2	0.22	ERJ-3RQFR22V	Panasonic	RES, 0.22 ohm, 1%, 0.1W, 0603	0603
57	R49, R97, R103	3	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
58	R50, R204, R205, R206	4	1.5k	CRCW08051K50JNEA	Vishay-Dale	RES, 1.5 k, 5%, 0.125 W, 0805	0805
59	R51	1	0	CRCW12060000Z0EA	Vishay-Dale	RES, 0, 5%, 0.25 W, 1206	1206
60	R52, R63, R76	3	0.1	ERJ-3RSFR10V	Panasonic	RES, 0.1, 1%, 0.1 W, 0603	0603
61	R55, R58, R67, R70, R71, R80, R83, R84, R160, R162, R163, R164, R166, R169, R170, R171, R172, R173, R175, R186, R189, R190, R193, R195, R199, R200, R208, R210, R212, R213, R215	31	0	ERJ-2GE0R00X	Panasonic	RES, 0, 5%, 0.063 W, 0402	0402
62	R61, R62, R72, R73, R74, R75, R90, R93, R247, R250, R254, R257	12	10.0k	ERJ-2RKF1002X	Panasonic	RES, 10.0 k, 1%, 0.1 W, 0402	0402
63	R85, R91, R98, R99, R104, R105	6	1.00k	RG1608P-102-B-T5	Susumu Co Ltd	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603
64	R86	1	2.49k	RG1608P-2491-B-T5	Susumu Co Ltd	RES, 2.49 k, 0.1%, 0.1 W, 0603	0603
65	R87	1	100k	CRCW0402100KFKED	Vishay-Dale	RES, 100 k, 1%, 0.063 W, 0402	0402
66	R88	1	4.99k	RG1608P-4991-B-T5	Susumu Co Ltd	RES, 4.99 k, 0.1%, 0.1 W, 0603	0603
67	R89	1	4.75	CRCW06034R75FKEA	Vishay-Dale	RES, 4.75, 1%, 0.1 W, 0603	0603
68	R92, R110	2	499	RG1608P-4990-B-T5	Susumu Co Ltd	RES, 499, 0.1%, 0.1 W, 0603	0603

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
69	R94	1	30.0k	RG1608P-303-B-T5	Susumu Co Ltd	RES, 30.0 k, 0.1%, 0.1 W, 0603	0603
70	R95, R101	2	2.21	CRCW06032R21FKEA	Vishay-Dale	RES, 2.21, 1%, 0.1 W, 0603	0603
71	R96, R108, R115, R116, R117, R118, R192, R194, R197, R198	10	100	RG1608P-101-B-T5	Susumu Co Ltd	RES, 100, 0.1%, 0.1 W, 0603	0603
72	R106, R111, R114	3	20.0k	RG1608P-203-B-T5	Susumu Co Ltd	RES, 20.0 k, 0.1%, 0.1 W, 0603	0603
73	R107, R119, R120, R121, R122, R153, R154, R155, R156, R157, R158, R159, R165, R168, R174, R176, R177, R178, R181, R182, R183, R184, R185, R187, R188, R191, R196, R201, R202, R203, R211, R214, R216, R217, R218, R243	36	1.00k	RC0603FR-071KL	Yageo America	RES, 1.00 k, 1%, 0.1 W, 0603	0603
74	R109	1	280k	RG2012P-2803-B-T5	Susumu Co Ltd	RES, 280 k, 0.1%, 0.125 W, 0805	0805
75	R112, R249, R252, R256, R258	5	10.0k	RG1608P-103-B-T5	Susumu Co Ltd	RES, 10.0 k, 0.1%, 0.1 W, 0603	0603
76	R113	1	0.22	ERJ-3RQFR22V	Panasonic	RES, 0.22, 1%, 0.1 W, 0603	0603
77	R161, R167, R179, R180, R269, R273	6	33	CRCW040233R0JNED	Vishay-Dale	RES, 33, 5%, 0.063 W, 0402	0402
78	R207, R260	2	33.0	RC0603FR-0733RL	Yageo America	RES, 33.0, 1%, 0.1 W, 0603	0603
79	R209, R227, R228, R229, R230, R234, R237, R238, R241, R242, R264, R265, R266	13	330	RC0603JR-07330RL	Yageo America	RES, 330, 5%, 0.1 W, 0603	0603
80	R219	1	118k	RT0805BRD07118KL	Yageo America	RES, 118k ohm, 0.1%, 0.125W, 0805	0805
81	R220	1	5.62k	RT0805BRD075K62L	Yageo America	RES, 5.62 k, 0.1%, 0.125 W, 0805	0805
82	R221	1	249k	CRCW0805249KFKEA	Vishay-Dale	RES, 249k ohm, 1%, 0.125W, 0805	0805
83	R222, R226, R231, R232, R233, R235, R236, R239, R240	9	1.2k	CRCW06031K20JNEA	Vishay-Dale	RES, 1.2 k, 5%, 0.1 W, 0603	0603
84	R223	1	1.07k	RT0805BRD071K07L	Yageo America	RES, 1.07 k, 0.1%, 0.125 W, 0805	0805
85	R224	1	20.5k	CRCW080520K5FKEA	Vishay-Dale	RES, 20.5 k, 1%, 0.125 W, 0805	0805
86	R225	1	0.01	WSL0805R0100FEA18	Vishay-Dale	RES, 0.01, 1%, 0.25 W, 0805	0805

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
87	R244	1	511	RC0603FR-07511RL	Yageo America	RES, 511, 1%, 0.1 W, 0603	0603
88	R246, R251	2	10.0k	CRCW060310K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.1 W, 0603	0603
89	R248, R255	2	32.4k	RG1608P-3242-B-T5	Susumu Co Ltd	RES, 32.4 k, 0.1%, 0.1 W, 0603	0603
90	R253, R259	2	25.5k	RG1608P-2552-B-T5	Susumu Co Ltd	RES, 25.5 k, 0.1%, 0.1 W, 0603	0603
91	R261	1	0	CRCW04020000Z0ED	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402	0402
92	R267, R270, R271, R277	4	4.7k	CRCW04024K70JNED	Vishay-Dale	RES, 4.7 k, 5%, 0.063 W, 0402	0402
93	R268, R276	2	0.1	ERJ-2BSFR10X	Panasonic	RES, 0.1, 1%, 0.125 W, 0402	0402
94	R274	1	100	CRCW0402100RJNED	Vishay-Dale	RES, 100, 5%, 0.063 W, 0402	0402
95	S1	1		EVQPNF04M	Panasonic	Switch, Tactile, SPST-NO, 0.05A, 12V, SMD	SMD, 2-Leads, Body 6x4mm
96	T1	1	110uH	750315240	Wurth Elektronik	Transformer, 110 uH, SMT	10.41x12.32mm
97	TP1, TP2, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP17	14	STD	STD	STD	Test Point 40mil pad 20mil drill	
98	TP3, TP16, TP26, TP27, TP28, TP29, TP32, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP46, TP47	20	SMT	5016	Keystone	Test Point, Compact, SMT	Testpoint_Keystone_Compact
99	TP15, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP30, TP31, TP33, TP34, TP48, TP49, TP50, TP51	17	STD	STD	STD	Test Point, O.025"	
100	U1	1		SN6505ADBVR	Texas Instruments	LOW-NOISE 1A TRANSFORMER DRIVERS FOR ISOLATED POWER SUPPLIES, DBV0006A	DBV0006A
101	U2, U7, U13	3		TPS7A4700RGWR	Texas Instruments	36-V, 1-A, 4.17-µVRMS, RF LDO Voltage Regulator, RGW0020A	RGW0020A
102	U3	1		LMZ14203TZ-ADJ/NOPB	Texas Instruments	3A SIMPLE SWITCHER® Power Module with 42V Maximum Input Voltage, 7-pin TO-PMOD, Pb-Free	TZA07A
103	U4, U11	2		TPS70912DBVT	Texas Instruments	IC REG LDO 1.2V 0.15A SOT23-5	DBV0005A

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
104	U5, U12	2		ISO7840DWR	Texas Instruments	High-Performance, 8000 VPK Reinforced Quad-Channel Digital Isolator, DW0016B	DW0016B
105	U6, U8, U10	3		TPS70918DBVT	Texas Instruments	IC REG LDO 1.8V 0.15A SOT23-5	DBV0005A
106	U9	1		ISO7842DWR	Texas Instruments	High-Performance, 8000 VPK Reinforced Quad Channel Digital Isolator, DW0016B	DW0016B
107	U14	1		OPA378AIDBVT	Texas Instruments	Low-Noise, 900 kHz, RRIO, Precision Operational Amplifier, Zerø-Drift Series, 2.2 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS & no Sb/Br)	DBV0005A
108	U15, U18, U20	3		OPA625IDBVR	Texas Instruments	High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers, DBV0006A	DBV0006A
109	U16	1		SN74LVC1G17DCKR	Texas Instruments	SINGLE SCHMITT-TRIGGER BUFFER, DCK0005A	DCK0005A
110	U17, U27, U31	3		SN74LVC1G08DCKR	Texas Instruments	Single 2-Input Positive-AND Gate, DCK0005A	DCK0005A
111	U19	1		ADS9110IRGER	Texas Instruments	18-Bit, 2-MSPS, 20-mW, SAR ADC with Enhanced Serial Interface, RGE0024H	RGE0024H
112	U21, U28	2		BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8
113	U22	1		REF5045AIDGKT	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin MSOP (DGK), Green (RoHS & no Sb/Br)	DGK0008A
114	U23	1		OPA376AIDBVR	Texas Instruments	Precision, Low Noise, Low Iq Operational Amplifier, 2.2 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS & no Sb/Br)	DBV0005A
115	U24, U25	2				Spartan-3AN Non-Volatile FPGA, 108 User I/Os, 144-Pin TQFP, Standard Performance, Commercial Grade	TQ144

Table 12. BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
116	U26, U29, U30, U32	4		TLV3012AIDCKR	Texas Instruments	Nanopower, 1.8V, Comparator with Voltage Reference, DCK0006A	DCK0006A
117	U33	1	SN74AUP1G 80DCK	SN74AUP1G80DCK	TI	IC, Single Positive-Edge-Triggered D-Type Flip-Flop	SC-70
118	U34	1		REF6041AIDGK	Texas Instruments	High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A	DGK0008A
119	U35	1		ISO1541DR	Texas Instruments	Low-Power Bidirectional I2C Isolators, D0008A	D0008A
120	U36	1		LMK61E2-SIAR	Texas Instruments	Ultra-Low Jitter Programmable Oscillator with Internal EEPROM, SIA0008B	SIA0008B
121	U37	1		SN65LVDS4RSET	Texas Instruments	500 Mbps High-Speed Differential Line Driver / Receivers with LVDS Input and LVTTL / LVCMOS Output, 1 Rx, -40 to +85 degC, 10-pin UQFN (RSE), Green (RoHS & no Sb/Br)	RSE0010A
122	Y1, Y2	2		ASTMLPE-125.000MHZ-LJ-E-T	ABRACON	OSC, 125 MHz, 3.3V, SMD	3.2x2.5mm
123	C69	0	10uF	GRM21BR71A106KE51L	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805	0805
124	C72	0	1uF	GRM188R71E105KA12D	MuRata	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603
125	C214	0	0.01uF	GRM155R71H103KA88D	MuRata	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0402	0402
126	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
127	J24	0		HTSW-103-07-G-S	Samtec	Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH
128	R45	0	0	CRCW04020000Z0ED	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402	0402
129	R48	0	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
130	R53, R54, R56, R57, R59, R60, R64, R65, R66, R68, R69, R77, R78, R79, R81, R82, R102	0	0	ERJ-2GE0R00X	Panasonic	RES, 0, 5%, 0.063 W, 0402	0402
131	R100	0	10.0k	ERJ-2RKF1002X	Panasonic	RES, 10.0 k, 1%, 0.1 W, 0402	0402

9.3 Layout Prints

To download the layer plots, see the design files at TIDA-00732.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00732.

9.5 Layout Guidelines

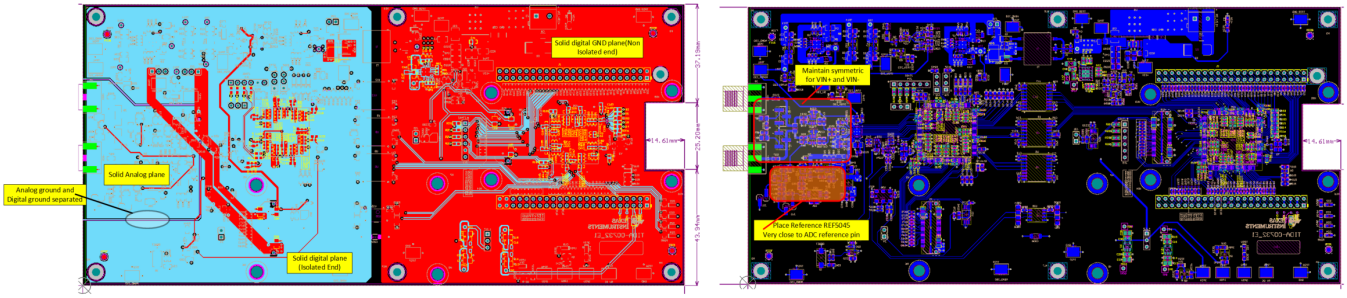

Figure 30. Board Layout Guidelines

9.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00732.

9.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00732.

10 Software Files

To download the software files, see the design files at TIDA-00732.

11 References

1. Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*, TIPD115 Design Guide (SLAU515)

12 About the Author

ANBU MANI is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Anbu has fifteen years of experience in analog circuit design and digital circuit design for the Automatic Test Equipment in Modular platform. He is also engaged with the design and development of embedded products.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• Changed from preview page	1

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