TI Designs

8-ch Isolated High Voltage Analog Input Module Reference Design

TI Designs

TIDA-00764 reference design is a high-voltage analog input module with eight channels. Each channel can be used for both, voltage and current measurement. The TI Design uses the 16-bit analog-to-digital converter (ADC) ADS8681 that can handle input voltages of up to ±12.288 V. This makes any preprocessing of standard input voltages in the industrial space unnecessary. In addition, four channels of the design are able to handle common-mode (CM) voltages of up to ±160 V. Therefore, there is no need to worry about ground loops or compensation currents flowing between the connected inputs.

Design Resources

TIDA-00764	Design Folder
ADS8681	Product Folder
OPA192	Product Folder
MUX36S08	Product Folder
TPS55010	Design Folder
SN74AHC594	Product Folder
TS5A23157	Product Folder
ISO714x	Product Folder
LP2985	Product Folder

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Design Features

- High Voltage Inputs of up to ±12.288 V
- Voltage and Current Measurement
- 4 Channels With CM of up to ±160 V
- -85dB Crosstalk Rejection for Adjacent Channels
- 100 MΩ Input Impedance
- Surge Transient Immunity According to EN 61000-4-5 Class 2 (±1kV, 24A)
- BeagleBone Compatible

Featured Applications

- PLC
- Analog Input Modules

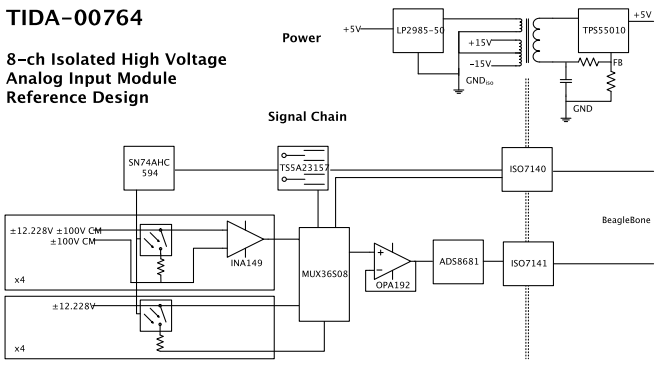


Figure 1. Block Diagram

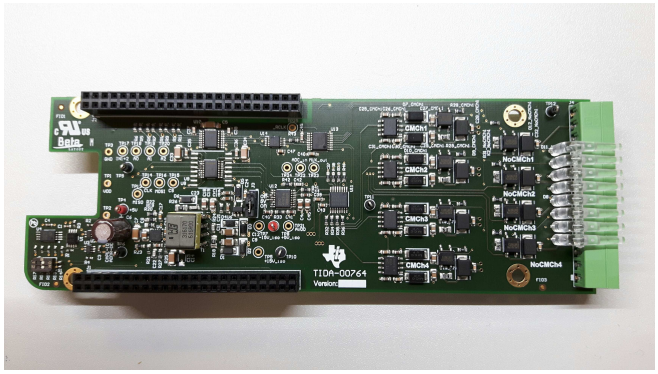


Figure 2. Board Design

1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION			DETAILS
	MIN	TYP	MAX	
Supply voltage	3.5 V	5 V	5.5 V	Section 3.1
Power consumption isolated side			600mW	
Channels	8 isolated overall			Section 3.2
	4 with CM support of ±160 V			Section 3.2.1
Input voltage	Max. ±12.288 V			
Input current	0 mA – 24 mA			
Surge transient immunity	EN 61000-4-5 class 2 (±1 kV, 24 A)			Section 3.2.2
Resolution	16-bit ADC			Section 3.3
Input Ranges / V	±2.56, ±5.12, ±6.144, ±10.24, ±12.288			
	0–5.12, 0–6.144, 0–10.24, 0–12.288			
Input impedance	100 MΩ			Section 3.3.2
Crosstalk	-85dB for adjacent channels			Section 6.4
Channel settling time	52 µs for -12.288 V to 12.288 V			Section 6.5
Operating Temperature	-40°C – 85°C			
Form Factor	158.75 mm x 54,51 mm			

2 System Description

TIDA-00764 is an isolated 8 channels high voltage analog input module that can handle input voltage of up to ±12.288 V without any signal preprocessing necessary. Although the analog-to-digital converter (ADC) ADS8681 used for this design has only one input channel, the design has eight input channels overall. This is achieved by combining the ADS8681 with the multiplexer (MUX) MUX36S08. The MUX36S08 can switch voltages in the range of ±18 V; the maximum input range of the ADS8681 is ±12.288 V. That's why no preprocessing of the incoming voltage signals is necessary.

Four input channels of the design can handle input signals with a common-mode (CM) range of up to ±160 V in respect to the ground potential of the board. For this, an INA149 is put in front of the MUX inputs for each of the four channels.

Furthermore, every channel of the design can also be used for current measurement in the range of 0 mA – 20 mA. To switch between voltage and current measurement the SN74AHC594, a serial-in, parallel-out register, can be programmed with two isolated control lines. The eight outputs of the SN74AHC594 then control one optical switch each. If the switch is turned on, the current is flowing through a shunt resistor and the voltage drop across the shunt is measured by the ADC. To indicate that a channel is configured for current measurement, a light emitting diode (LED) is turned on for the specific channel. The LEDs are placed at the input connector of the design, so that the channel status can also be seen by the user.

The board is BeagleBone compatible, which means that it can be directly put onto a BeagleBone. Communication between the AM3359 processor of the BeagleBone and the ADC of the design is using the Serial Peripheral Interface (SPI) interface. SPI and further necessary control lines for MUX switching and programming of the SN74AHC594 are isolated from the BeagleBone using a ISO7140 and a ISO7141 isolator.

To power the isolated side of the board, TIDA-00764 uses the Fly-Buck™ topology, built up with the TPS55010 regulator and a transformer with two separate windings on the secondary side. These separate windings are needed to create +5 V, needed for the ADC, ISO714x, SN74AHC594 and one analog switch, as well as ±15 V, needed for the MUX and the INA149, directly. This saves cost that would be necessary for further power devices on the secondary side otherwise. The design can be powered directly from a 5-V rail and works down to 3.5 V. This makes it suitable for 5 V backplanes.

3 System Design Theory

3.1 Isolated Power Supply

Besides a standard 24 V supply rail, programmable logic controller (PLC) systems often also have a 5 V backplane that can be used to power modules. To address this, TIDA-00764 can be powered from a 5 V supply. The power supply of TIDA-00764 is shown in Figure 16.

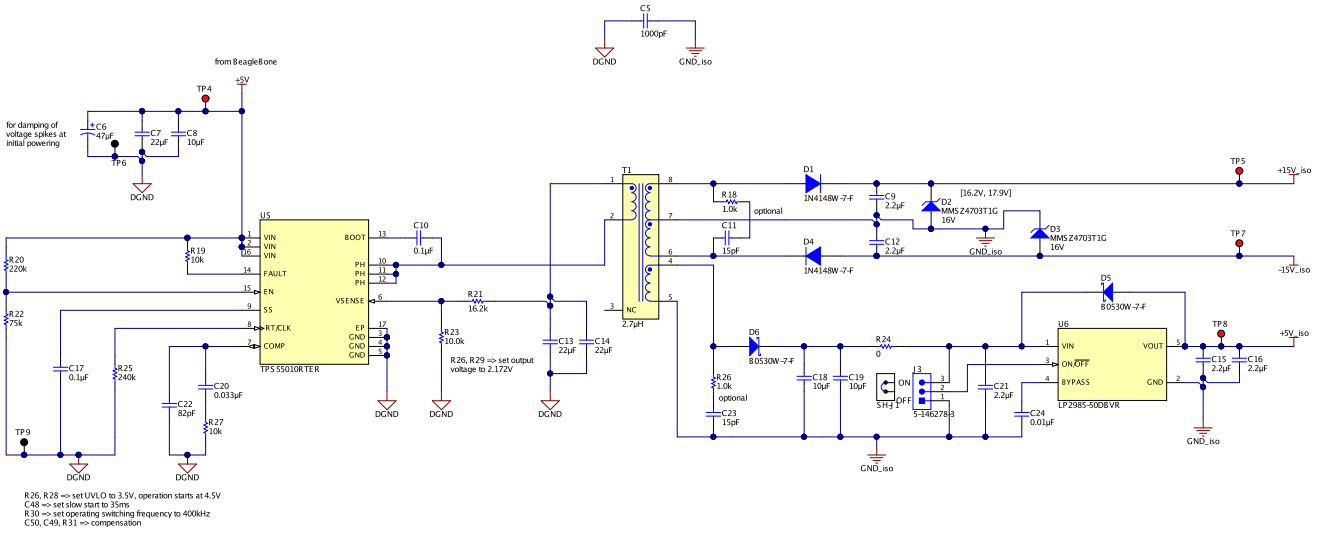


Figure 3. TIDA-00764 - Power Supply

Because the 5 V rail in a PLC system might suffer from voltage drops, TIDA-00764 works down to 3.5 V, before it shuts down. The working range of the design is set by the under- and overvoltage lockout of the TPS55010. The board powers up if the supply voltage is above 4.5 V and keeps operating as long as the supply voltage does not drop below 3.5 V.

The TPS55010 is rated for an input voltage of maximum 6 V and can withstand 7 V at most. However, the board is not protected against too high input voltages. If this is needed, using a Zener diode that clamps the input voltage to 6 V will protect the device.

The maximum power consumption on the isolated side of the design is expected to be around 570 mW, see Table 2. Power losses are caused by non-perfect coupling of the transformer windings, the rectifying diodes on the secondary side, the two snubber circuits on the secondary side, the voltage drop across the linear dropout regulator (LDO) for the isolated 5 V supply line and general power losses like switching and conducting losses. Still, the overall power consumption of the power supply is expected to stay below the maximum output power of 2W of the TPS55010. The low-power requirements also enable the use of the Fly-Buck topology, which is primary side regulated and facilitates the power design.

Table 2. TIDA-00764 - Power Consumption of Isolated Side

DEVICE	V_{IN}	I_{IN}	NUMBER	Pin,sum
ADS8681	5 V	10 mA	1	50 mW
ISO7140	5 V	25 mA	1	125 mW
ISO7141	5 V	10 mA	1	50 mW
SN74AHC594	5 V	32 mA	1	160 mW
TS5A23157	5 V	1 mA	1	5 mW
MUX36S08	±15 V	1 mA	1	30 mW
OPA192	±15 V	1 mA	1	30 mW
INA149	±15 V	1 mA	4	120 mW
			$P_{in,total}$	570 mW

Figure 4 shows a simplified schematic of a Fly-Buck design. The primary side voltage V_{pri} is regulated like in a standard buck converter and given by the duty cycle D.

$$D = \frac{V_{pri}}{V_{in}} = \frac{t_{on}}{t_{on} + t_{off}} \quad (1)$$

Where t_{on} is the time when switch S_1 is closed and switch S_2 is open and t_{off} is the time when switch S_1 is open and switch S_2 is closed. The output capacitor C_{out} is charged during t_{on}. Power is transferred to the secondary side during t_{off}. For a fixed frequency $f = (t_{on} + t_{off})^{-1}$ this means that for an increasing duty cycle, or longer t_{on} time, there is less time left to transfer power to the secondary side. Hence, high duty cycles lead to high peak currents on the secondary side. One effect of higher currents is for example a higher voltage drop across the Diode D_1. As a result the output regulation of the secondary voltage V_{sec} gets worse. Also, the internal switches of the regulator must be able to withstand those peak currents. This is why for a Fly-Buck duty cycles of more than 50% should be avoided. The relation between increasing duty cycle D and ratio of primary current I_{pri} to secondary current I_{sec}, assuming a transformer with a turn ratio N=1, is also shown in Figure 5. It can be seen that for a duty cycle of 50% I_{pri} equals I_{sec}. However, for a duty cycle of 80% I_{pri} is already 4 times higher than I_{sec}. This effect is increased further for systems using a transformer with a turn ratio of $N_{sec}/N_{pri} > 1$.

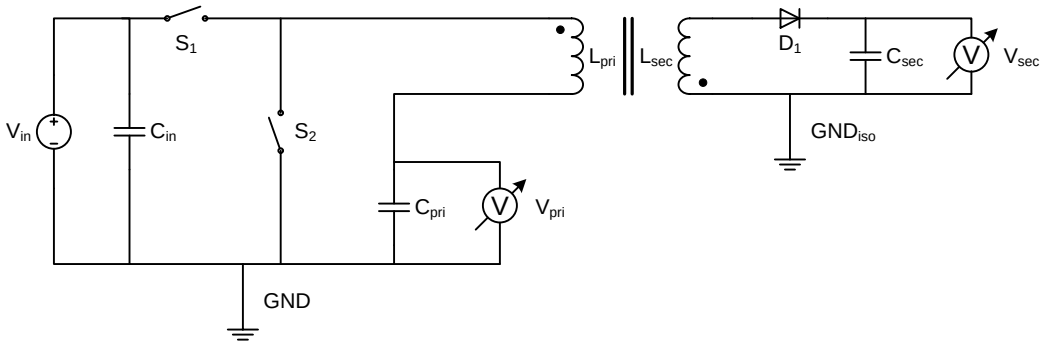


Figure 4. Simplified Schematic of Fly-Buck Topology

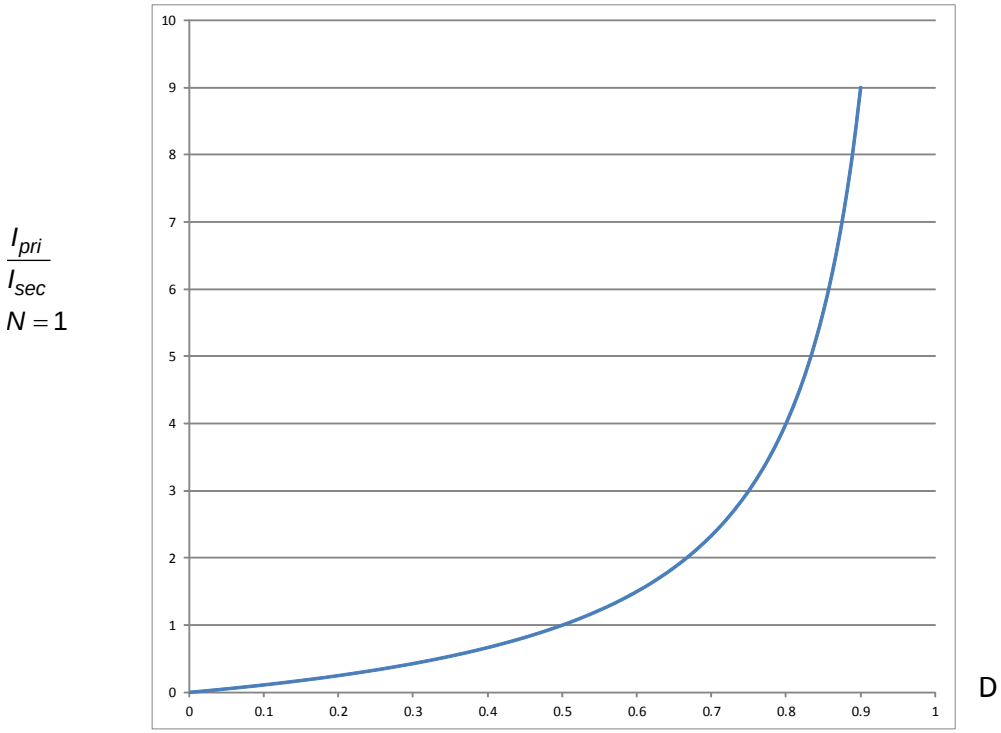


Figure 5. Relation of D to I_{pri}/I_{sec} With N=1

The input range of the design is defined from 3.5 V to 5 V. To achieve a reasonable range for the duty cycle D, the primary output voltage is regulated to 2.172 V. This results in a duty cycle from 40% to 62%. The switching frequency is set to 400 kHz. This results in a good ratio of conduction to switching losses. Furthermore, the harmonics of 400 kHz (800 kHz, 1.2 MHz, ...) do not interfere with the sampling frequency of 1MSPS of the ADS8681.

On the secondary side three output voltages, all to be created directly from the transformer, are required: - 15 V, +15 V, +5 V. Therefore, the transformer has two windings on the secondary side. One with a turn ratio of 1:16 for the ±15 V supplies that also has a third connection pin after 8 turns and a second one with a turn ratio of 1:3. The final output voltages on secondary side, after the rectification diodes, will be around ±17 V and +6 V.

This improves the following:

- The CM range of the INA149
- The switching speed of the MUX36S08
- Leaves enough voltage headroom for the LP2985-5.0 to regulate the 5 V supply for the ADS8681

The supplies of the MUX36S08 and the INA149 are rated for a maximum of ±18 V. To ensure that this voltage is not exceeded, two Zener diodes are placed from the respective supply rail to GND.

3.2 Analog Front End

TIDA-00764 realizes its eight input channels by combining the single channel ADC ADS8681 with the 8:1 MUX MUX36S08. Four of these channels can handle input signals of ±12.288V plus an additional CM voltage of ±160 V in respect to the isolated GND of the board. The other four channels can handle input voltages of ±12.288 V in respected to the isolated GND. In the following sections, “CM channel 1-4” refers to the CM channels and “no CM channel 1-4” refers to channels that do not support CM.

Figure 6 shows a picture of an input channel without CM support, Figure 7 with CM support.

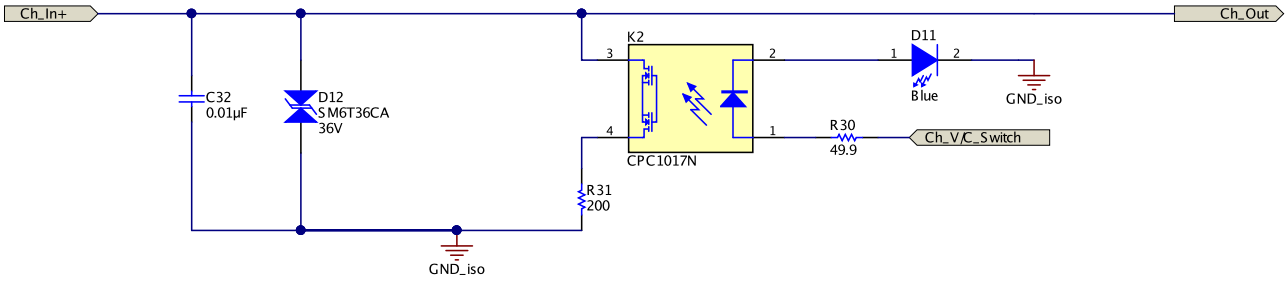


Figure 6. Input Channel Without CM Support

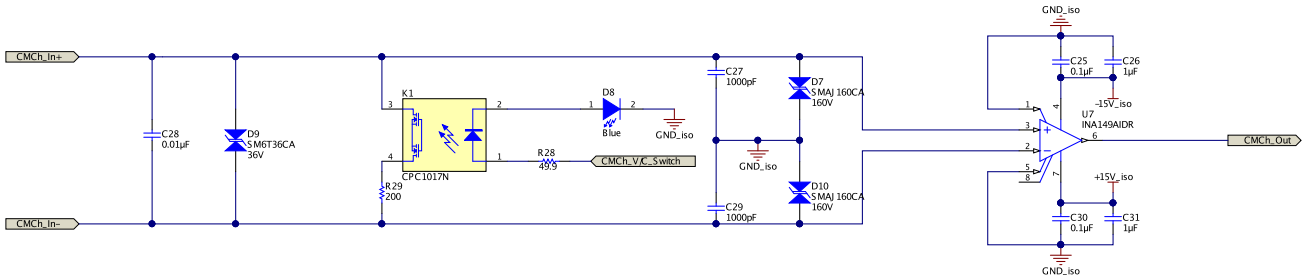


Figure 7. Input Channel With CM Support

3.2.1 Input Channel With CM support

In an industrial application it is often that several sensor outputs are connected to one multichannel input module. These sensors can be located at different positions, can be powered from different sources and can suffer from different disturbing sources. All these effects result in different GND potentials for the different sensors. If all these sensors were now connected to one common ground large compensation currents would flow between the different GND potentials and as a result may destroy the sensors. To solve this problem, TIDA-00764 has four CM input channels, in the following referred to as CM channels, that can handle CM voltages of up to ±160 V in respect to the isolated GND of the analog input module.

To handle the different CM voltages, every CM channel uses an INA149. A block diagram of the device is shown in Figure 8.

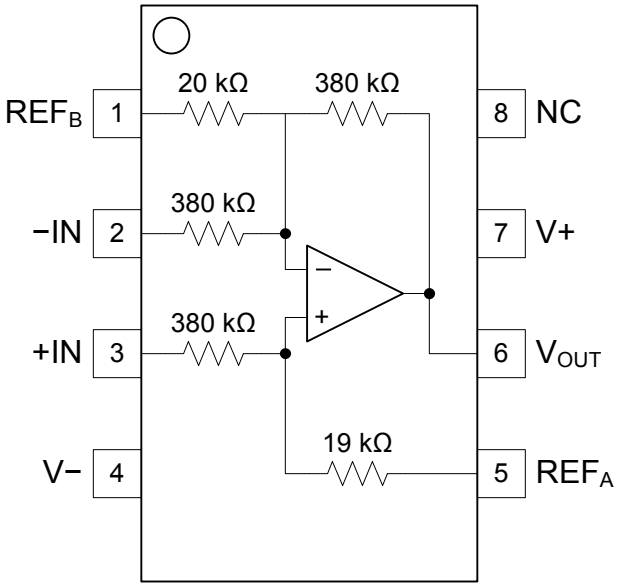


Figure 8. Block Diagram of INA149

The INA149 works like a standard differential amplifier. Its transfer function is given in Equation 2.

$$V_{OUT} = (+IN) - (-IN) + 20 \cdot REF_A - 19 \cdot REF_B \quad (2)$$

The device has two inputs (+IN) and (–IN), which are connected to the output terminals of the design and one output V_{OUT} that is connected to the MUX input. The INA149 is supplied by the ±15-V rails. Higher supply voltages enable the support of higher CM ranges. For supply voltages of ±16.5 V, the supported CM range goes up to ±300 V. However, the design is only rated for a CM range of ±160 V because of the clamping diodes used in the design: SMA160CA. These diodes have a reverse stand-off voltage V_R of 160 V and a maximum breakdown voltage V_{BR} of 197 V. Worst case scenario, the clamping voltage V_C of these diodes is 259 V.

The curve characteristics of the diodes are shown in Figure 9.

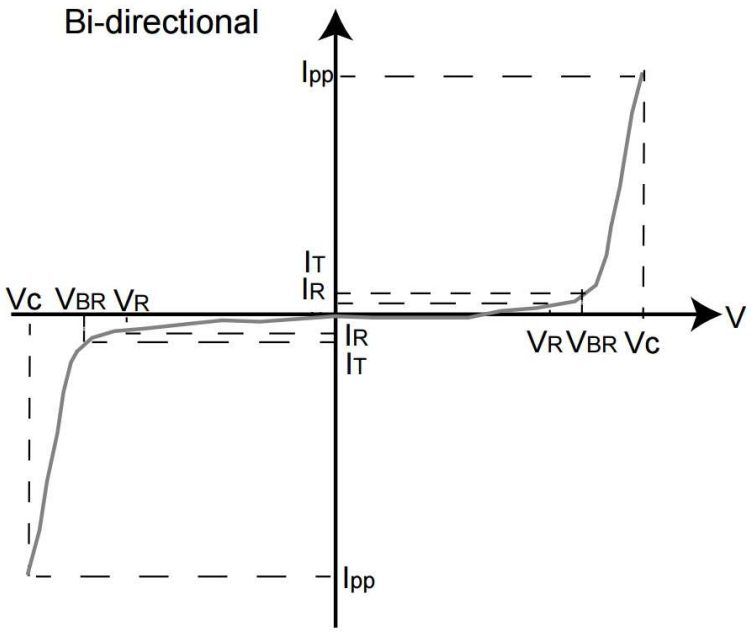


Figure 9. Curve Characteristics of Clamping Diode SMAJ160CA

The output of the device can be referenced to different voltages REF_A and REF_B. In TIDA-00764, the output is only referenced to the isolated GND of the design, meaning REF_A = REF_B = GND_{iso}. In this configuration, the INA149 acts as a simple unity-gain amplifier. Therefore, its output voltage V_{OUT} is given by Equation 3.

$$V_{OUT} = (+IN) - (-IN) + 20 \cdot GND_{iso} - 19 \cdot GND_{iso} = (+IN) - (-IN) \quad (3)$$

3.2.2 Input Protection

Every MUX input channel is protected against surge events according to EN61000-4-5. The goal is that the board can withstand class 2 surges: ±1kV with a current of 24A. To achieve this TVS diodes with a clamping voltage of 36V are placed after every channel input. In addition, a capacitor is placed in parallel to the diode so that steep pulses can be suppressed better.

In case of a surge event, the diode will clamp the voltage to 36 V. However, the dynamic resistance RD of the TVS diode must be considered, too. The dynamic resistance of the diode is 0.427 Ω. The resulting clamping voltage V_C is given by Equation 4.

$$V_C = V_{BR} + R_D \cdot I_{peak} = 36V + 0.427\Omega \cdot 24A = 48.05V \quad (4)$$

If the design is supposed to be used in environments with 125°C ambient temperature, this breakdown voltage can increase to 50.04 V.

The design uses optocouplers to switch between voltage and current sensing. The optocouplers can withstand voltage differences of up to 60 V between their switch connections. That is why no TVS diode with higher breakdown voltage can be chosen.

In case of a surge event, the inputs of the MUX36S08 must be protected, too. The internal ESD diodes of the MUX start conducting, if the input voltage raises more than 0.3V above or falls more than -0.3 V below the supply voltages. It is assumed that the ESD diodes can handle currents of maximum 10 mA. To protect the inputs a 5.11kΩ resistor is placed in front of every MUX input. In case of a surge event, this results in a maximum current of $\frac{(50.04V - 0.3V - 15V)}{5.11k\Omega} = 6.8mA$ flowing through the ESD diodes.

Every diode has a certain leakage current that will result in a measurement error. As an example, an input voltage of 12.288 V at an ambient temperature of 85°C is assumed. According to the device-specific data sheet, the leakage current of the diode is about 10 nA for a standoff voltage of 30.8 V and an ambient temperature of 85°C. For a 0 mA – 24 mA current signal the maximum voltage drop across the 200 Ω shunt is 4.8 V. The leaking 10 nA would cause a voltage drop of 2 µV across the shunt resistor. However, the corresponding voltage range of the ADC is 0 to 5.12 V with a resolution of 78.125 µV. This means that the "missing" voltage drop across the shunt is not measurable by the ADC.

3.2.3 Switching Between Voltage and Current Sensing

Every channel can be used for voltage and current sensing. To ensure isolation, an optocoupler is used to switch between the two modes. If the optocoupler is turned on, the current is flowing through the optocoupler plus the connected 200 Ω precision shunt resistor. The resulting voltage drop is measured by the ADC. The resistor is rated for a maximum power of 125 mW. Equation 5 shows that input currents of up to 24 mA can be measured.

$$200\,\Omega \cdot (0.024\,mA)^2 = 0.1152\,mW \tag{5}$$

The shunt resistor has a variance 0.02% and a temperature drift of ±25 ppm/°C, which ensures a stable and linear resistor value for the current measurement. However, note that not only the voltage drop across the shunt resistor, but also the optocoupler itself is measured. The resistance of the optocoupler varies over temperature and current. To compensate these effects, measure the ambient temperature of the system and calculate these additional voltage drops out in software.

To save cost for isolated signals, all eight optocouplers are controlled by the serial in parallel out register SN74AHC594, which is programmed with two isolated data lines. Figure 10 shows the register and how it is connected on the board.

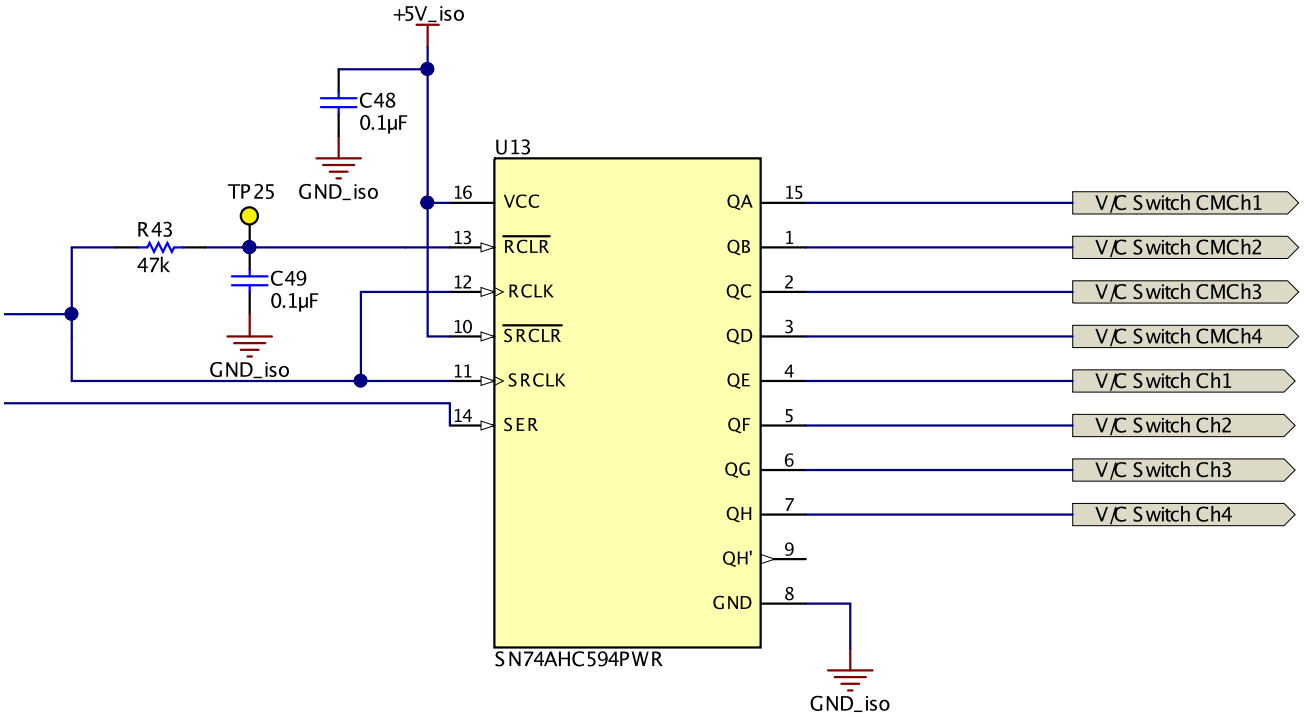


Figure 10. Serial In Parallel Out Register

Normally, the analog switch TS5A23157 of the design is set in the way that the two inputs are directed to the channel selection input pins of the MUX36S08 by setting the inputs IN1 and IN2 high, see Figure 15. To program the register these inputs are set low. This also puts the ADC in a reset state, which means that no measurements can be done during the programming of the register. It is not expected that the user wants to measure any input signals, while the inputs are still configured. Instead, the standard procedure is to first program the inputs, and second, start the actual measurement procedure.

The programming of the SN74AHC594 is done in the same way as in TIDA-00550. To start, the $\overline{\text{RCLR}}$ pin of the SN74AHC594 must be pulled to zero. This clears the current status of the outputs. Then, 8 data bits, 1/on or 0/off for every channel, must be written into the register. Next, the outputs must be activated by providing one more clock signal on SRCLK. After the programming is done, the $\overline{\text{RCLR}}$ signal line must be pulled and hold high. Pulling $\overline{\text{RCLR}}$ high will also enable the ADC again.

The complete programming of the register works as follows:

1. Set input of $\overline{\text{RCLR}}$ and SRCLK low to discharge the RC network
2. Wait until $\overline{\text{RCLR}}$ is low and the outputs are cleared.
3. Put in new data byte on SER line and provide clock signal on SRCLK line; make sure that data is put in fast enough so that RC network does not charge and therefore, $\overline{\text{RCLR}}$ stays low.
4. Set input of $\overline{\text{RCLR}}$ and SRCLK high to charge RC network.
5. Wait until $\overline{\text{RCLR}}$ is high.
6. Clock SRCLK once more to activate outputs.
7. Keep $\overline{\text{RCLR}}$ high until the next programming procedure.

By putting the RC filter in front of the $\overline{\text{RCLR}}$ input pin, only two general purpose in out (GPIO) signal lines from the BeagleBone are needed to program the SN74AHC594. Figure 11 shows an example of the programming procedure. Therein, C1 is the SRCLK signal, C2 the $\overline{\text{RCLR}}$ signal and C3 the SER signal.

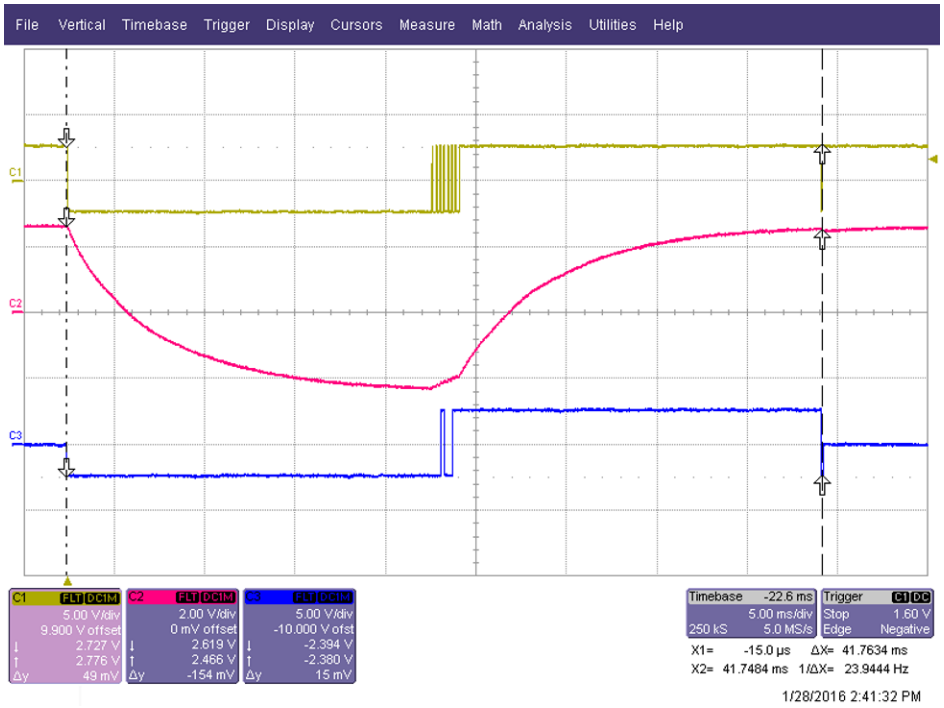


Figure 11. SN74AHC594 – Example of Programming Procedure

To indicate whether a channel is configured for voltage or current measurement, eight blue LEDs are placed at the terminal inputs of the design. If a LED is turned on, the channel is used for current measurement. From the left to the right the LEDs represent the following channels:

- CM Channel 4, CM Channel 3, CM Channel 2, CM Channel 1, No CM Channel 4, No CM Channel 3, No CM Channel 2, No CM Channel 1.

Figure 12 shows an example configuration where CM Channel 3, No CM Channel 3 and No CM Channel 2 are configured for current measurement.

NOTE: It is important to always set the current channels first and then configure the ADC. Otherwise, the programming of the SN74AHC594 will put the ADC into reset. After the programming the ADC will restart with his standard configuration.

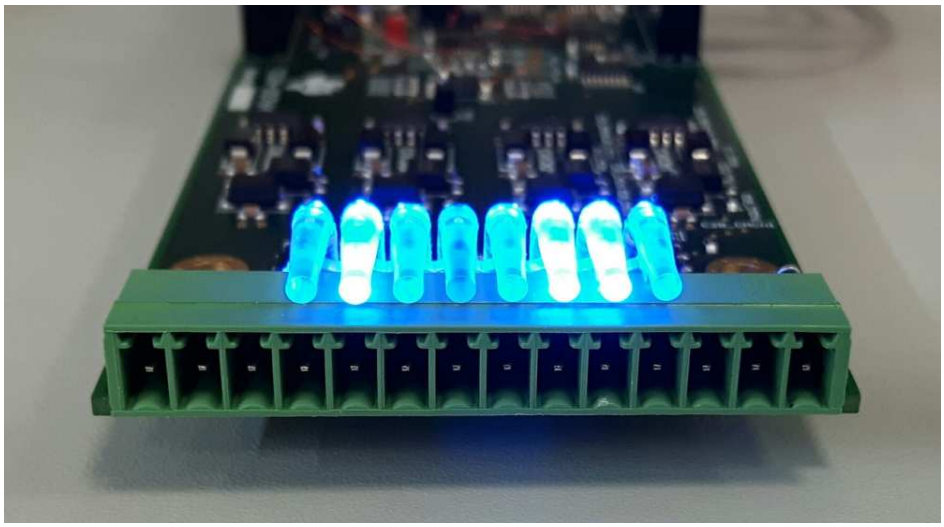


Figure 12. Input Terminals With Current Measurement Configuration for CMCh 3, NoCMCh 3, NoCMCh 2

3.3 Analog Digital Converter ADS8681

The ADS8681 is a 16-bit successive-approximation register (SAR) ADC with a sampling rate of 1 mega-sample-per-second (MSPS). The ADS has an internal reference of 4.096 V that can be scaled up to three times so that the device is able to cover an input range of up to ±12.288 V. This allows the user to sense all common input voltages in the industrial space without any preprocessing of the input signal necessary. If a smaller input range is preferred, the input range can also be set down to ±2.56 V or 0 V – 5.12 V.

For an input range of ±12.288 V, the ADC has a signal-to-noise ratio (SNR) of 90.25dB. According to Equation 2, wherein N equals the number of bits, this results in a theoretical effective number of 14.7 bits. For an input range of 0 V – 5.12 V, the SNR goes down to 87.5dB, which results in a theoretical effective number of bits of 14.24 bits.

$$SNR\left(dB\right) = 6.02 \cdot N + 1.76$$

$$\Rightarrow N = \frac{90.25 - 1.76}{6.02} = 14.70 \tag{6}$$

3.3.1 Input Filter

The ADS8681 has an internal second order filter with a cutoff frequency f_c of 15 kHz. To achieve a damping of at least 16 * 6.02 + 1.76 = 98.08dB at a frequency of 1 MHz, a RC filter is put in front of the impedance converter, realized with a OPA192, preceding the ADC. The resistor value of the RC filter is already given by the signal chain of the system: 5.11 kΩ in front of the MUX + minimum MUX channel resistance of 100 Ω = 5.21 kΩ. Simulation results show that a cutoff frequency of about 37 kHz result in a damping of the system of about -101dB at 1 MHz. This also leaves some margin for resistor and capacitor value inaccuracy of up to 5%. Finally, Equation 7 gives 820 pF as the next standard value for capacitor C.

$$f_c = \frac{1}{2\pi \cdot R \cdot C}$$

$$\Rightarrow C = \frac{1}{f_c \cdot 2\pi \cdot R} = \frac{1}{37\,kHz \cdot 2\pi \cdot 5.21k\Omega} = 825pF \Rightarrow 820\,pF \tag{7}$$

The resulting alternating current (AC) transfer characteristic of the system is shown in Figure 13. Therein, the green line shows the AC transfer characteristic of the internal second order filter of the ADC only and the blue line shows complete AC transfer characteristic of the system. Figure 14 shows the schematic section that includes the RC filter.

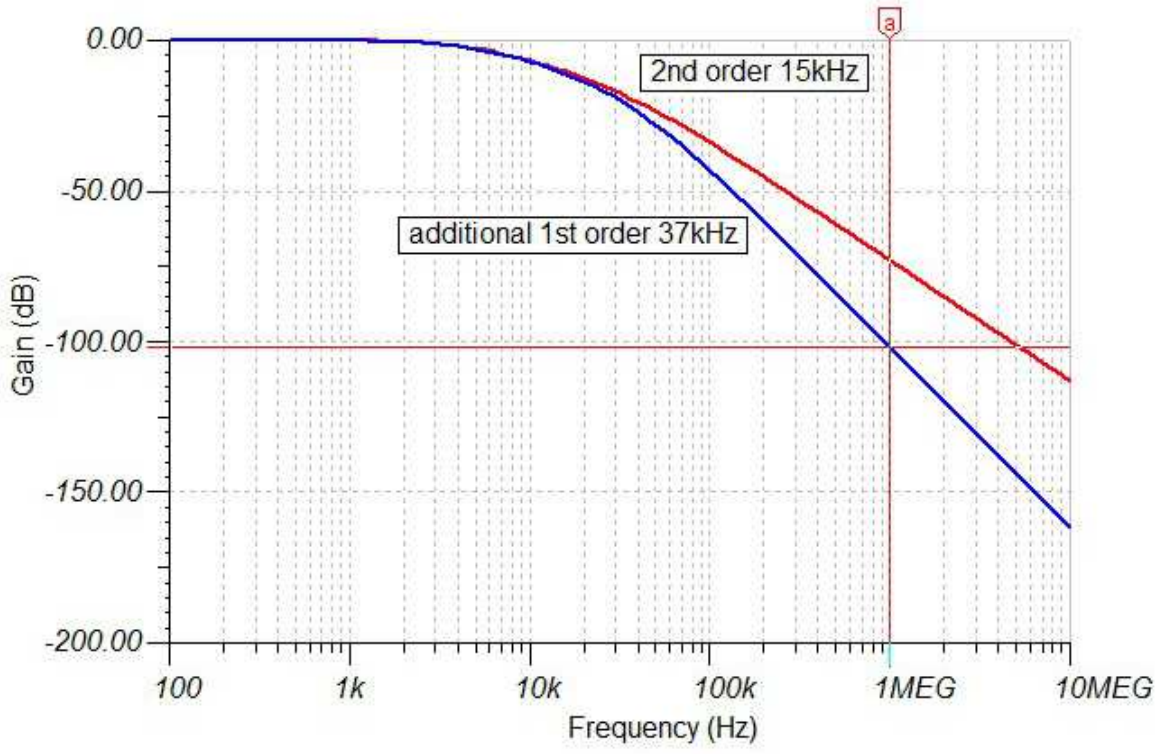


Figure 13. AC Transfer Characteristic of ADS8681 Plus External RC Filter

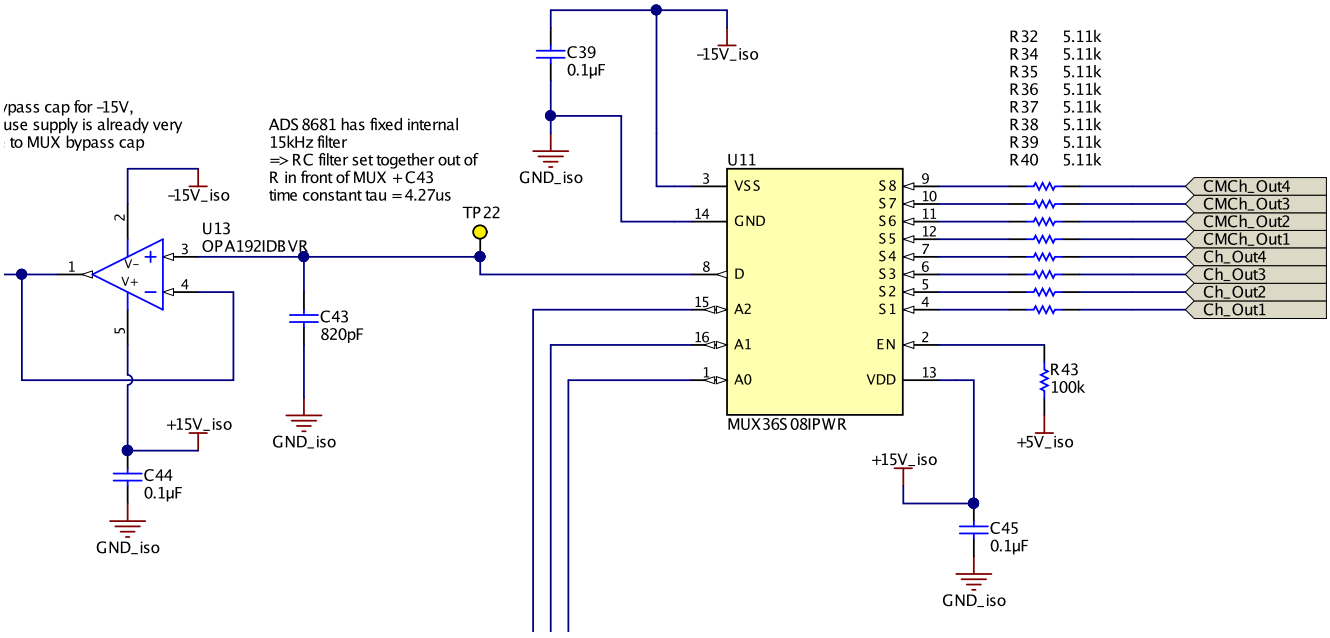


Figure 14. RC Filter in Front of OPA192

3.3.2 Impedance Converter

The output of the MUX is not connected directly to the ADC input, but is connected to an impedance converter, built up with an operational amplifier (OpAmp) OPA192. This OpAmp can be seen as an optional part of the design which has its advantages and disadvantages. The disadvantages are that the OPA192 will add noise into the system, adds cost to the signal chain and makes the needed board space bigger. However, the advantage is that it facilitates the voltage measurement and makes post processing of the measured signal easier. This is because of the much higher input impedance of the OPA192 compared to the ADS8681.

Exemplary, the following situation is assumed: At the input terminals of a no CM channel, there is a 10 V DC input signal in respect to board GND. The ADS8681 is set to an input range of 0 V – 10.24 V, which results in a resolution of 156.25 µV. For this input range, the ADC has an input impedance of down to 1.02 MΩ. The signal path to the input pin of the ADC consists out of the channel resistance of the MUX, maximum 250 Ω, plus the input protection resistors for the MUX of 5.11kΩ. For a 10V input signal, this means that there is already a voltage drop of 2.4375 mV across the MUX and a voltage drop of 50 mV across the input resistor, see Equation 8. This equates to 15.6 LSB and 320 LSB, respectively. The error introduced by these resistors must then be estimated and calculated in software, so that the final result is more accurate. However, it will not be possible to compensate effects like slightly different resistor values due to manufacturing or MUX channel mismatches.

$$\frac{10V}{5.11k\Omega + 250 + 1.02M} = 9.75\,\mu A$$

$$250\Omega \cdot 9.75\,\mu A = 2.4375\,mV$$

$$5.11k\Omega \cdot 9.75\,\mu A = 50\,mV$$

$$\frac{2.4375\,mV}{\frac{10.24V}{2^{16}}} = 15.6\,\text{LSB}$$

$$\frac{50\,mV}{\frac{10.24V}{2^{16}}} = 320\text{LSB} \tag{8}$$

In case the OPA192 is placed in front of the ADC, the situation is as follows: The OPA192 has an input impedance of 100 MΩ and an input bias current of maximum ±5 nA and a maximum input offset current of ±2 nA. Now, the voltage drop across the MUX and in the input resistor is only 2.5 µV and 51.1 µV, see Equation 9. Hence, the combined voltage drop is a lot smaller than the ADC resolution of 156.25 µV. This eliminates the need to calculate the estimated voltage drop of the signal path.

$$\frac{10V}{511k\Omega + 250\Omega = 100M\Omega} = 10\,nA$$

$$250\Omega \times 10\,nA = 2.5\,\mu V$$

$$5.11k\Omega \times 10\,nA = 51.1\,\mu V \tag{9}$$

3.3.3 Sampling Speed

The actual voltage value U_C of a capacitor C of an RC filter that is charged is given by Equation 10, wherein, $U_C(t)$ is the actual capacitor voltage after time t, U_0 is the voltage applied to the capacitor, ΔU is the difference between the capacitor voltage $U_{C,t0}$ at time t_0 and the applied voltage U_0 and τ is the time constant of the RC filter.

$$U_C(t) = U_0 + \Delta U \cdot e^{-\frac{t}{\tau}} = U_0 + \left(U_{C,t_0} - U_0\right) \cdot e^{-\frac{t}{\tau}} \tag{10}$$

As mentioned in Section 3.3.1, the RC filter is put in front of the OPA192; therefore, the ADC, has the time constant $\tau = R \cdot C = 5.21\ k\Omega \cdot 820\ pF = 4{,}27\ \mu s$. Equation 10 can be used to calculate the wait time *t* until ΔU is less than 1/2 LSB of the ADC. Only after this time has elapsed, the sampled value will be correct.

It is assumed that at time t_0, the capacitor is charged to a value of +12.288 V. Then, the applied voltage changes to -12.288 V.

The calculation steps are shown in Equation 11 and Equation 12.

$$\frac{1}{2}LSB\left(ADS8681\right)=\frac{1}{2}\cdot\frac{12.288V\cdot 2}{2^{16}}=\frac{12.288V}{2^{16}} \tag{11}$$

$$U_C\left(t\right)-U_0=\left(U_{C,t_0}-U_0\right)\cdot e^{-\frac{t}{\tau}}<\frac{1}{2}LSB\left(ADS8681\right) \tag{12}$$

Combine Equation 11 and Equation 12 to produce Equation 13.

$$\left(U_{C,t_0}-U_0\right)\cdot e^{-\frac{t}{\tau}}<\frac{12.288V}{2^{16}}$$

$$-\frac{t}{\tau}<ln\left(\frac{12.288V}{2^{16}\cdot\left(U_{C,t_0}-U_0\right)}\right)$$

$$t>-ln\left(\frac{12.288V}{2^{16}\cdot\left(U_{C,t_0}-U_0\right)}\right)\cdot\tau$$

$$\Rightarrow t>-ln\left(\frac{12.288V}{2^{16}\cdot\left(12.288V-\left(-12.288V\right)\right)}\right)\cdot\tau=-\ln\left(\frac{1}{2^{17}}\right)\cdot\tau=11.78\cdot\tau \tag{13}$$

It is shown that for a voltage difference that is less than 1/2 LSB, the capacitor of the RC filter must be charged for about 12τ. For τ = 4.27 µs, this results in a charge or waiting time t of at least 51.24 µs after the MUX has switched to a new channel.

3.3.4 Communication Interface and External Controlling

Communication between the ADC and the BeagleBone is done via standard 4-wire SPI. In case the user wants to reset the ADC, this can be done with another isolated control line coming from the BeagleBone that is connected to the reset pin of the ADC. This control line is also used to control the analog switch TS5A23157, see Table 3 and Figure 15.

Table 3. TS5A23157 - Logic Table

IN1+IN2_iso = high	COM1 + COM2 connected to MUX
IN1+IN2_iso = low	COM1 + COM2 connected to register

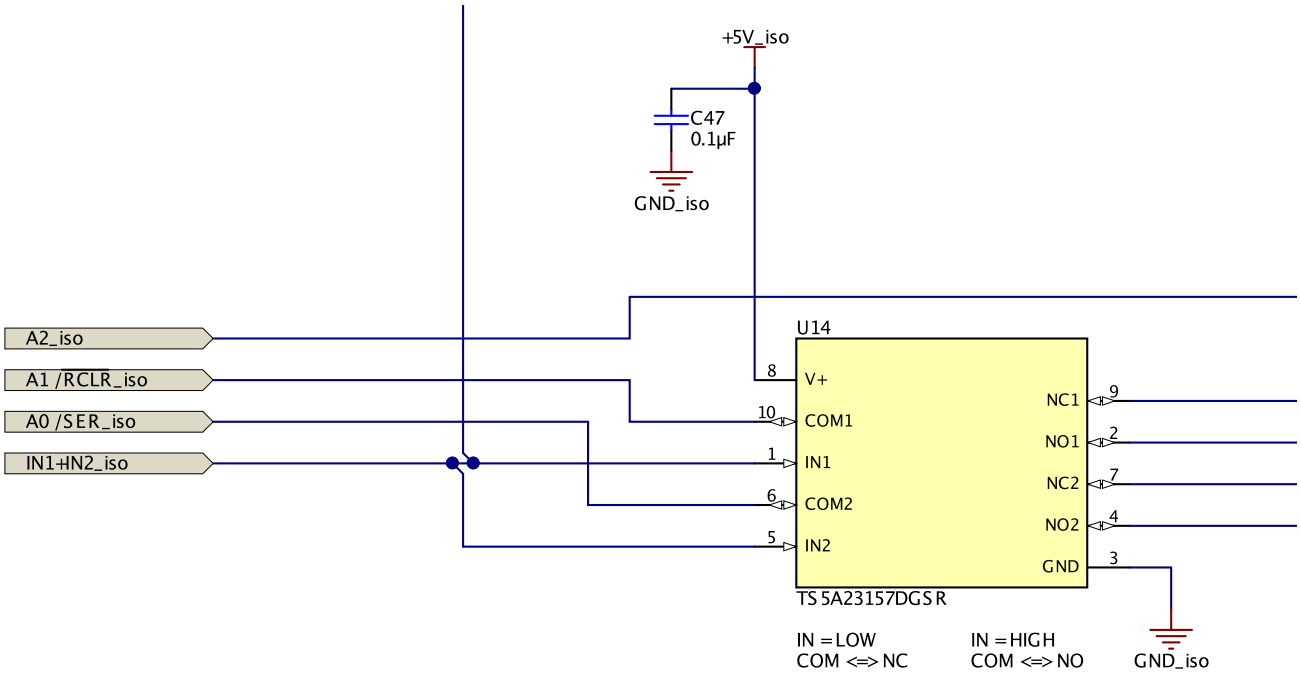


Figure 15. TS5A23157- Connections

4 Block Diagram

Figure 16 shows the block diagram of TIDA-00764. The four channels with CM capabilities (upper block) as well as the four channels without CM capabilities (lower block) are both just showed once, as the corresponding channels are built up identically.

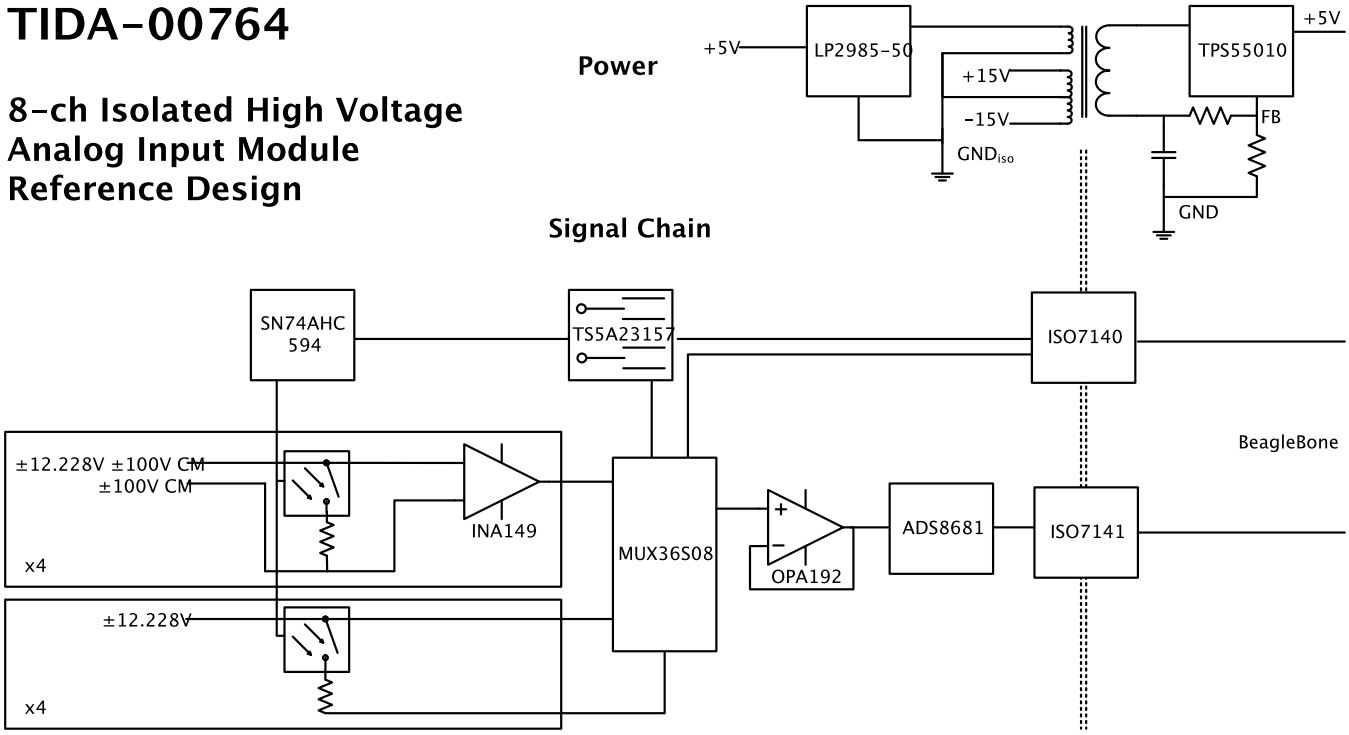


Figure 16. Block Diagram

4.1 TPS55010

The TPS55010 is a transformer driver designed to provide isolated power. The device operates from 6 V down to 2.95 V. The device uses fixed frequency current mode control and half bridge power stage with primary side feedback to regulate the output voltage for power levels up to 2W. The switching frequency is adjustable from 100 kHz to 2000 kHz so solution size, efficiency and noise can be optimized. The switching frequency is set with a resistor or is synchronized to external clock using the RT/CLK pin. To minimize inrush currents, a small capacitor can be connected to the soft-start pin. The EN pin can be used as an enable pin or to increase the default input under-voltage-lockout voltage from 2.6 V.

Table 4. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS55010	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4.2 LP2985

The LP2985 family of fixed-output, low-dropout regulators offers exceptional, cost-effective performance for both portable and nonportable applications. Available in voltages of 1.8 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.3 V, 5 V, and 10 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

Table 5. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2985	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4.3 ISO714x

ISO7131, ISO7140, and ISO7141 devices provide galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. ISO7131 has three channels with two forward and one reverse-direction channels. ISO7140 and ISO7141 are quad-channel isolators; ISO7140 has four forward channels, ISO7141 has three forward and one reverse-direction channels. These devices are capable of 50-Mbps maximum data rate with 5-V supplies and 40-Mbps maximum data rate with 3.3-V or 2.7-V supplies, with integrated filters on the inputs for noise-prone applications. The suffix F indicates that default output state is low.

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7-V, 3.3-V, and 5-V supplies. All inputs are 5-V tolerant when supplied from a 2.7-V or 3.3-V supply.

Table 6. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7131CC	SSOP (16)	4.90 mm × 3.90 mm
ISO7140CC		
ISO7140FCC		
ISO7141CC		
ISO7141FCC		

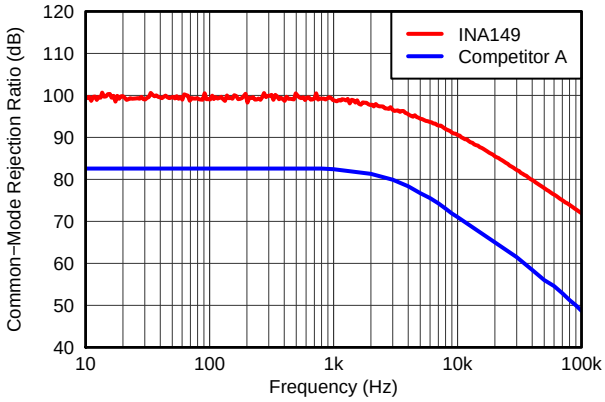
(1) For all available packages, see the orderable addendum at the end of the datasheet.

4.4 INA149

The INA149 is a precision unity-gain difference amplifier with a very high input common-mode voltage range. It is a single, monolithic device that consists of a precision op amp and an integrated thin-film resistor network. The INA149 can accurately measure small differential voltages in the presence of common-mode signals up to ±275 V. The INA149 inputs are protected from momentary common-mode or differential overloads of up to 500 V.

In many applications, where galvanic isolation in not required, the INA149 can replace isolation amplifiers. This ability can eliminate costly isolated input side power supplies and the associated ripple, noise, and quiescent current. The excellent 0.0005% nonlinearity and 500-kHz bandwidth of the INA149 are superior to those of conventional isolation amplifiers.

The INA149 is pin-compatible with the INA117 and INA148 type high common-mode voltage amplifiers and offers improved performance over both devices. The INA149 is available in the SOIC-8 package with operation specified over the extended industrial temperature range of –40°C to +125°C.



4.5 ADS8681

The ADS8681 is an integrated data acquisition system based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC), operating at a throughput of 1 MSPS. The device features a high precision SAR ADC, integrated analog front-end (AFE) input driver circuit, overvoltage protection circuit up to ±20 V, and an on-chip 4.096-V reference with extremely low temperature drift. Operating on a single 5-V analog supply, the ADS8681 can support true bipolar input ranges of ±12.288 V, ±6.144 V, ±10.24 V, ±5.12 V, and ±2.56 V, as well as unipolar input ranges of 0 V to 12.288 V, 0 V to 10.24 V, 0 V to 6.144 V, and 0 V to 5.12 V. The gain and offset errors for the AFE circuit are accurately trimmed within the specified values for each input range to ensure high dc precision. The input range selection is done by software programming of the device internal registers. The device offers a high resistive input impedance (≥ 1 MΩ) irrespective of the selected input range.

The ADS8681 offers an enhanced SPI-compatible serial interface (multiSPI™) to the digital host and also supports daisy-chaining of multiple devices. The digital supply can operate from 1.65 V to 5.25 V, enabling direct interface to a wide range of host controllers.

Table 7. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8681	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4.6 OPA192

The OPA192 is an integrated data acquisition system based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC), operating at a throughput of 1 MSPS. The device features a high-precision SAR ADC, integrated analog front-end (AFE) input driver circuit, overvoltage protection circuit up to ±20 V, and an on-chip 4.096-V reference with extremely low temperature drift. Operating on a single 5-V analog supply, the OPA192 can support true bipolar input ranges of ±12.288 V, ±6.144 V, ±10.24 V, ±5.12 V, and ±2.56 V, as well as unipolar input ranges of 0 V to 12.288 V, 0 V to 10.24 V, 0 V to 6.144 V, and 0 V to 5.12 V. The gain and offset errors for the AFE circuit are accurately trimmed within the specified values for each input range to ensure high dc precision. The input range selection is done by software programming of the device internal registers. The device offers a high resistive input impedance (≥ 1 MΩ) irrespective of the selected input range.

The OPA192 offers an enhanced SPI-compatible serial interface (multiSPI) to the digital host and also supports daisy-chaining of multiple devices. The digital supply can operate from 1.65 V to 5.25 V, enabling direct interface to a wide range of host controllers.

Table 8. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA192	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4.7 MUX36S08

The MUX36S08 and MUX36D04 (MUX36xxx) are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers (muxes). The MUX36S08 offers 8:1 single-ended channels; whereas, the MUX36D04 offers differential 4:1 (8:2) channels. The MUX36S08 and MUX36D04 work equally well with either dual supplies (±5 V to ±18 V) or a single supply (10 V to 36 V). They also perform well with symmetric supplies (such as V_{DD} = 12 V, V_{SS} = –12 V), and unsymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). All digital inputs have TTL-logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

The MUX36S08 and MUX36D04 have very low on and off leakage currents, allowing these multiplexers to switch signals from high input impedance sources with minimal error. A low supply current of 45 µA enables use in portable applications.

Table 9. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MUX36S08IPW	TSSOP (16)	5.00 mm × 4.40 mm
MUX36D04IPW		

(1) For all available packages, see the package option addendum at the end of the data sheet.

4.8 TS5A23157

The TS5A23157 device is a dual single-pole double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

Table 10. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23157DGS	VSSOP (10)	3.00 mm × 3.00 mm
TS5A23157RSE	UQFN (10)	2.00 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4.9 SN74AHC594

The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{SRCLR}$, $\overline{RCLR}$) inputs are provided on the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Table 11. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC594	SOIC (16)	9.90 mm × 3.91 mm
	SSOP (16)	6.20 mm × 5.30 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOP (16)	12.60 mm × 5.30 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

5 Test Setup

The test setup for functionality and performance testing of TIDA-00764 is shown in Figure 17.

The design is powered by a GW Instek power supply that supplies the actual design with 5 V and the necessary BeagleBone components with 3.3 V. The input signal is provided by a KEYSIGHT B2912A precision source which has an accuracy of 100 nV and 10 fA.

Switching of the MUX channels and programming of the SN74AHC594 is controlled by an MSP430FR5969 placed on a MSP430FR5969 launchpad, see http://www.ti.com/tool/msp-exp430fr5969#0. SPI Communication to the board is also done with the launchpad. The MSP430FR5969 on the launchpad acts as the master for the SPI interface. The launchpad itself is connected with universal serial bus (USB) cable to a laptop on the test bench. The test routines for TIDA-00764 are called from code composer studio (CCS). Data from the launchpad to the laptop is sent over the universal asynchronous receiver transmitter (UART) interface of the MSP430FR6969 which is then displayed on a console running on the laptop.

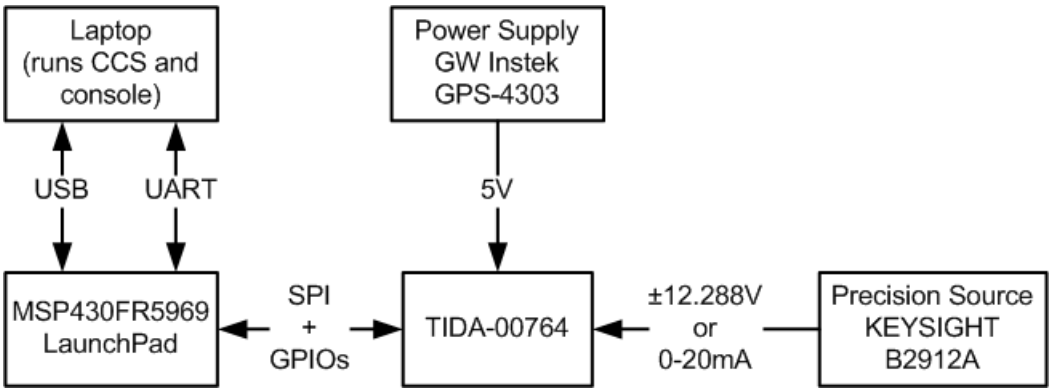


Figure 17. TIDA-00764 - Test Setup

6 Test Data

To characterize TIDA-00764, different test with different DC signals are done. It is differentiated between no CM channels and CM channels. The test procedure is as follows: First, the DC signal is applied to the input of the ADC, then, 4096 samples are recorded and plotted in a histogram. Out of the recorded values the standard deviation σ is calculated. With known σ, the characterizing DC parameters can be calculated, see Equation 15 to Equation 17. The values in V can be converted to bit values by dividing the V value by the corresponding resolution for this value.

$$V_{noise,\ RMS} = \sigma \tag{14}$$

$$V_{noise,pp} = V_{noise,\ RMS} \cdot 6.6 = \sigma \cdot 6.6 \tag{15}$$

$$\sigma(\text{bit}) = \frac{\sigma(V)}{\frac{\text{full scale range}(V)}{2^N}} \tag{16}$$

$$N_{eff} = log_2\left(\frac{2^N}{\sigma(\text{bit})}\right) = log_2\, 2^N - log_2\left(\sigma(bit)\right) = N - log_2\left(\sigma(bit)\right) \tag{17}$$

$$N_{noise\ free} = log_2\left(\frac{2^N}{\sigma(\text{bit}) \cdot 6.6}\right) = N_{eff} - log_2\left(6.6\right) = N_{eff} - 2.722 \tag{18}$$

$V_{noise,RMS}$ represents the rout-mean-square noise of the system. The peak-to-peak noise $V_{noise,pp}$ represents the range of bits wherein 99.9% of all recorded samples are included. It equals 6.6 times VRMS. N_{eff} equals the effective number of bits of the system, meaning the ADC plus the complete signal chain. $N_{noise\ free}$ is the effective resolution of the system.

The applied DC signal is either grounded or is coming from a decoupled voltage source. KEYSIGHT B2912A is used for this precision source. The precision source has an accuracy of 100 nV and 10 fA.

6.1 Channel Offsets

This section describes the test to measure the channel offset for both, no CM channel and CM channels. The input signals to the channels are applied at the input terminals of the board. That means that not the performance of the ADC alone, but the performance of the complete system is characterized.

The on-resistance mismatch between the eight MUX channels is 11Ω maximum, for a maximum temperature of 125°C. This channel mismatch is dominated by the 5.11kΩ resistor in front of the MUX. That is why the following tests are just done for one no CM channel and one CM channel.

6.1.1 No CM Channel Offset in Voltage Mode

To test the offset of the no CM channels for voltage sensing, the input of no CM channel 1 is shorted to GND at the input terminal. All other channels are left open. The input range of the ADC is set to ±2.56 V. The MUX is set to no CM channel 1. The results are listed in Table 12 and shown as a histogram in Section 6.1.4.

The offset for no CM channel 1 in voltage mode varies from -0.3125 mV to 0 mV. Most samples have an offset voltage of -0.15625 mV.

Table 12. Test Results for no CM Channel 1, Voltage Mode, Shorted

CHANNEL	σ/BITS	N_{eff}	N_{noise} FREE	V_{noise}, RMS / mV	V_{noise}, pp / mV
No CM ch1	0.743	16.428	13.705	0.058	0.383

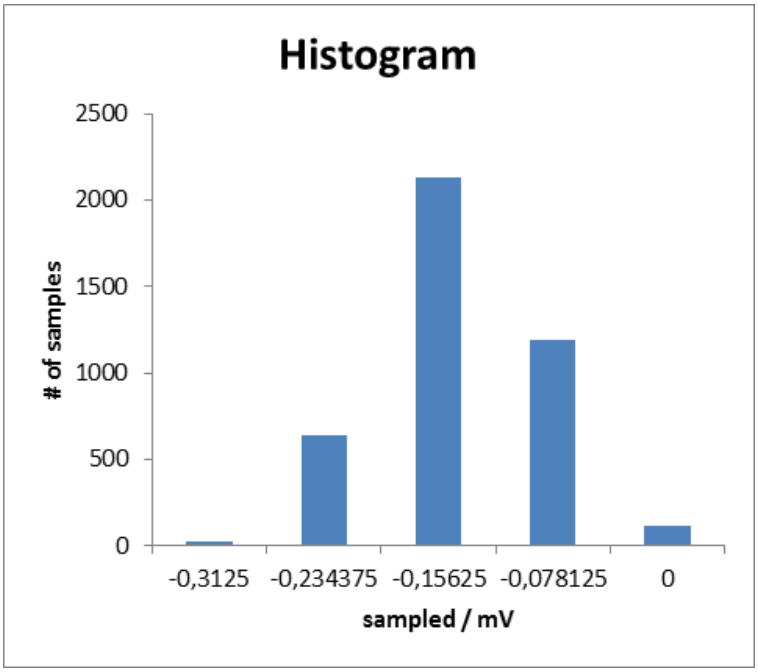


Figure 18. Histogram of Test Results for no CM Channel 1, Voltage Mode, Shorted

6.1.2 No CM Channel Offset in Current Mode

To test the offset of the no CM channels in current mode, the input of no CM channel 1 is shorted at the input terminal. All other channels are left open. No CM channel 1 is set to current mode. The input range of the ADC is set to ±5.12 V. This results in a resolution of 156.25 µV. The MUX is set to no CM channel 1.

The results are listed in Table 14 and shown as a histogram in Figure 19.

The offset for no CM channel 1 in current mode varies from -0.46875 mV to 0.15625 mV. Again, most samples have an offset voltage of -0.15625 mV.

Table 13. Test Results for No CM Channel 1, Current Mode, Shorted

CHANNEL	σ/BITS	N_{eff}	N_{noise} FREE	V_{noise}, RMS / mV	V_{noise}, pp / mV
No CM ch1	0.592	16.756	14.033	0.092	0.611

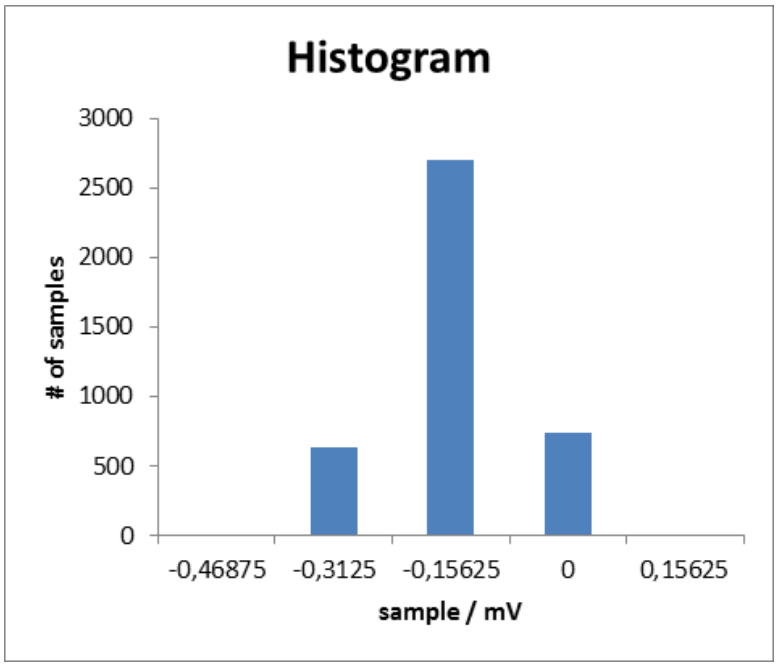


Figure 19. Histogram of Test Results for No CM Channel 1, Current Mode, Shorted

6.1.3 CM Channel Offset in Voltage Mode

To test the offset of the CM channels for voltage sensing, the input of CM channel 1 is shorted to GND at the input terminal. All other channels are left open. The input range of the ADC is set to ±2.56 V. The MUX is set to CM channel 1. The results are listed in Table 14 and shown as a histogram in Figure 20.

The offset for CM channel 1 in voltage mode varies from -1.015625 mV to -0.3125 mV. Most samples have an offset voltage of either -0.703125 mV or -0.625 mV.

Table 14. Test Results for CM Channel 1, Voltage Mode, Shorted

CHANNEL	σ/BITS	N_{eff}	N_{noise} FREE	V_{noise}, RMS / mV	V_{noise}, pp / mV
No CM ch1	1.162	15.783	13.061	0.091	0.599

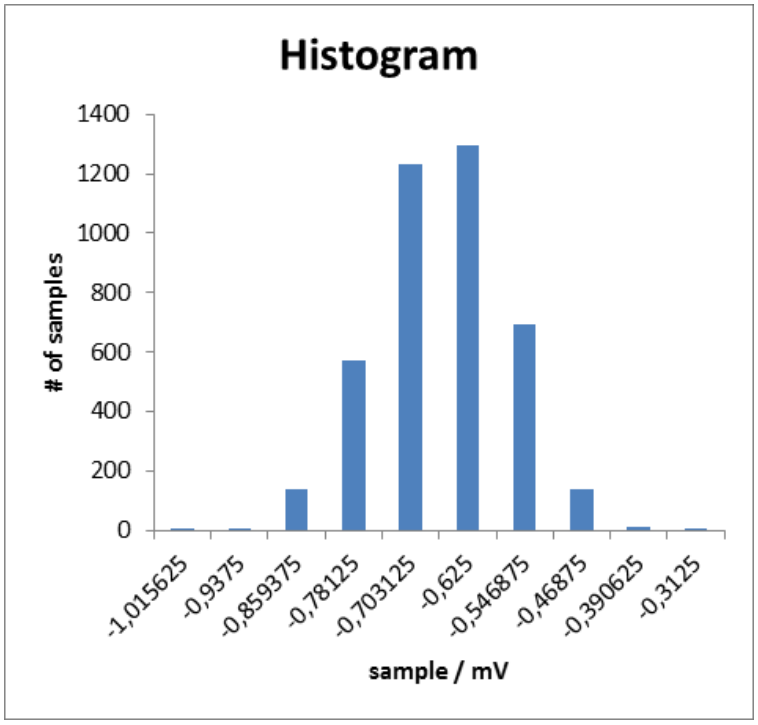


Figure 20. Histogram of Test Results for CM Channel 1, Voltage Mode, Shorted

6.1.4 CM Channel Offset in Current Mode

To test the offset of the CM channels in current mode, the input of CM channel 1 is shorted at the input terminal. All other channels are left open. CM Channel 1 is set to current mode. The input range of the ADC is set to ±2.56 V. The MUX is set to CM channel 1. The results are listed in Table 15 and shown as a histogram in Figure 21.

The offset for CM channel 1 in current mode varies from -1.09375 mV to -0.3125 mV. Again, most samples have an offset voltage of either -0.703125 mV or -0.625 mV.

Table 15. Test Results CM Channel 1, Current Mode, Shorted

CHANNEL	σ/BITS	N_{eff}	N_{noise} FREE	V_{noise}, RMS / mV	$V_{noise,}$ pp / mV
No CM ch1	1.162	15.783	13.061	0.091	0.599

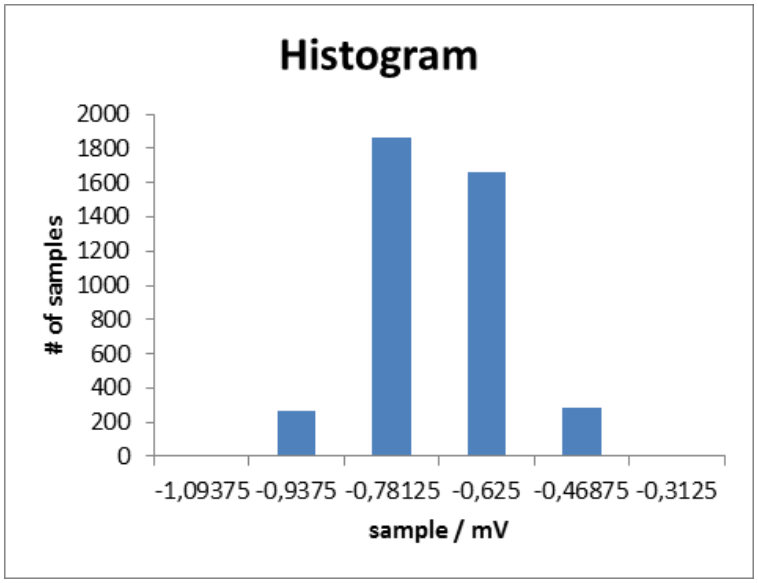


Figure 21. Histogram of Test Results for CM Channel 1, Current Mode, Shorted

6.1.5 Channel Offsets Conclusion

It is shown that both no CM channel and CM channel have a stable offset voltage for both, voltage and current mode. In current mode, the samples are spread wider and accordingly $V_{noise,\ pp}$ is bigger. The additional noise is introduced by the optocoupler plus the current sense resistor across which the voltage is measured.

Moreover, the no CM channel is less noisy compared to the CM channel. This is due to the noise introduced by the INA149 in the CM channel signal chain.

As explained in Section 3.3.2, it is also possible to remove the impedance converter and connect the MUX output directly to the ADC input. However, this only improves the system performance, slightly. Exemplarily, test results for no CM channel 1, voltage mode, shorted to board GND with and without impedance converter are shown in Table 16. The table shows that the impedance converter introduces only little noise in the system, so that the system performance is a bit worse than without impedance converter. Of course, this is always dependent on the OpAmp being used. If an OpAmp with worse performance is chosen, this introduces more noise into the signal chain and lower the overall system performance significantly.

Table 16. Comparison for CM Channel 1, Voltage Mode, Shorted With and Without Impedance Converter

CHANNEL	σ / BIT	N_{eff}	N_{noise} FREE	V_{noise}, RMS / mV	V_{noise}, pp / mV
No CM ch1 w/ OPA192	0.743	16.428	13.705	0.058	0.383
No CM ch1 w/o OPA192	0.731	16.452	13.730	0.057	0.377

6.2 Voltage Measurement Performance

To test the channel performance for voltage mode for both, no CM and CM channel, successively 0 V, 5 V and 10 V are applied at the input terminals. For 0 V, the input is shorted; for 5 V and 10 V, the voltage is supplied by the precision source. The input range and therefore the resolution are adjusted for the different input voltages. Then, 4096 samples are done and plotted in a histogram. Afterwards, σ, N_{eff}, N_{noise} free, $V_{noise,\ RMS}$ and $V_{noise,\ pp}$ are calculated. Table 17 shows the results for no CM channel 1, Table 18 the results for CM channel 1.

Table 17. No CM Channel 1 Performance Over Voltage

V_{input} /V	Range/V	Res./µV	σ/BIT	N_{eff}	$N_{noise\ free}$	$V_{noise,\ RMS}$/mV	$V_{noise,\ pp}$/mV
0	±2.56	78.125	0.743	16.428	13.705	0.058	0.383
5	±5.12	156.25	0.965	16.051	13.328	0.146	0.995
10	±10.24	312.50	0.577	16.791	14.069	0.104	1.191

Table 18. CM Channel 1 Performance Over Voltage

V_{input} /V	Range/V	Res./µV	σ/BIT	N_{eff}	$N_{noise\ free}$ free	$V_{noise,\ RMS}$ /mV	$V_{noise,\ pp}$/mV
0	±2.56	78.125	1.162	15.783	13.061	0.106	0.599
5	±5.12	156.25	0.987	16.019	13.29	0.042	0.379
10	±10.24	312.50	0.623	16.683	13.961	0.121	1.284

The results show that with increasing resolution the effective number of bits is increasing as well. This is the case for every ADC because the input noise is the same, but the resolution is higher.

Table 18 shows that other than the no CM channel, for the CM channel $V_{noise,\ pp}$ is get smaller from 0 V to 5 V, then bigger from 5 V to 10 V. This is because the error introduced by the INA149 is minimal for output voltages that are higher than 0 V, see Figure 22. As a result, the CM channel shows best performance for input signals higher than 0 V.

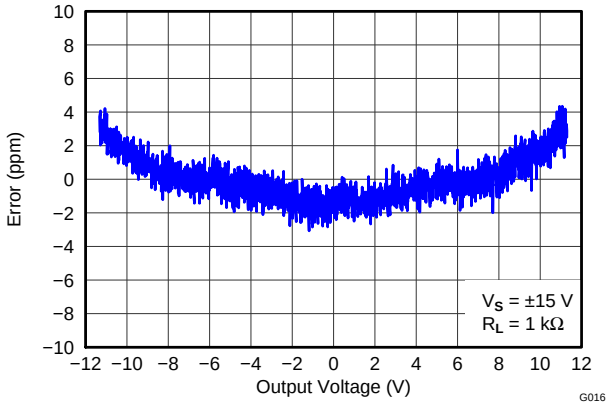


Figure 22. Gain Nonlinearity of INA149

6.3 Current Measurement

Both, no CM and CM channels are tested for increasing input current. The input current is increased from 0 mA to 20 mA. The current signal is supplied by the precision source. The maximum expected voltage drop across the shunt resistor and the optocoupler is (200 Ω + 16 Ω) · 20 mA = 4.32 V. Therefore, the input range is set to ±5.12 V. The histograms for the eight measurements are not shown in this design guide. The results are shown in Table 19 and Table 20.

Table 19. No CM Channel 1 - Current Measurement

I_{in}/mA	σ/BIT	N_{eff}	$N_{noise\ free}$	$V_{noise,\ RMS}$/mV	$V_{noise,\ pp}$/mV
0	0.592	16.756	14.034	0.093	0.611
5	0.798	16.326	13.603	0.124	0.823
10	0.622	16.684	13.963	0.097	0.641
20	2.646	14.596	11.873	0.413	2.728

Table 20. CM Channel 1 - Current Measurement

I_{in}/mA	σ/BIT	N_{eff}	$N_{noise\ free}$ free	$V_{noise,\ RMS}$ /mV	$V_{noise,\ pp}$/mV
0	0.734	16.446	13.723	0.115	0.757
5	0.781	16.355	13.633	0.122	0.806
10	0.788	16.343	13.620	0.123	0.813
20	2.82	14.577	11.854	0.419	2.766

The results show that the current measurement is stable for the input range of 0 mA – 10 mA. The reason for the huge increase of σs for the 20 mA measurement is the used precision source. The precision source lowers its resolution if the output current is set to a bigger value than 10 mA. Therefore, the system is working fine up to 20 mA, but is limited due to the used current source.

6.4 Channel Crosstalk

According to its data sheet, the MUX36S08 has a channel-to-channel isolation of -85dB for adjacent channels. To test this on TIDA-00764, the following test is done.

The sampling frequency for the test setup is 17.3 kHz. The input range of the ADC is set to ±10.24 V. The MUX is set to no CM channel 1. No CM channel 1 is shorted to GND. To no CM channel 2, the disturbing ±10 V, 4.325 kHz signal is applied. This frequency is chosen, because it is 1/4th of the sampling frequency. Then, 4096 measurements are recorded.

Afterwards, the recorded samples are divided by 2^{16} to normalize them to the resolution of the ADC. Then, a Fourier analysis is done with the 4096 samples and the absolute values of the imaginary numbers, resulting from the Fourier analysis, are calculated. These values are then plotted over the frequency range of 0 kHz to 8.65 kHz in steps of 17.3 kHz/4096. The resulting plot is shown in Figure 23.

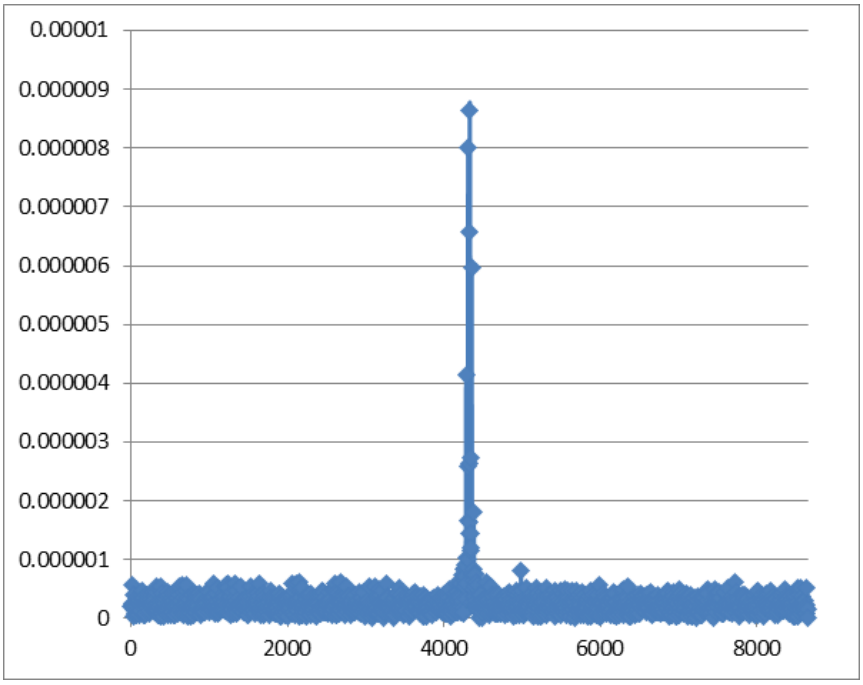


Figure 23. Results for Crosstalk Test

The plot shows the normalized amplitude of the disturbing signal. Its maximum is $8.63378 \cdot 10^6$ at 4.325 kHz. The disturbing signal is not always exactly at 4.325 kHz, but deviates a bit. Therefore, all samples in the range of 4.225 kHz to 4.425 kHz with amplitude of more than $1 \cdot 10^6$ are added up. These add up to $5.36534 \cdot 10^5$. Using Equation 19, it can be calculated that the signal has been attenuated by -85.4dB.

$$Attenuation(dB) = 20 \cdot log\left(5.36534 \cdot 10^{-5}\right) = -85.4dB \quad (19)$$

6.5 Channel Switching

Figure 24 shows the charging curve of the RC-filter in front of the ADC. The input signal changes from -12.25 V to +12.25 V. It shows that the calculated charging time t of 51.24 µs, see Section 3.3.3, complies with the recorded signal.

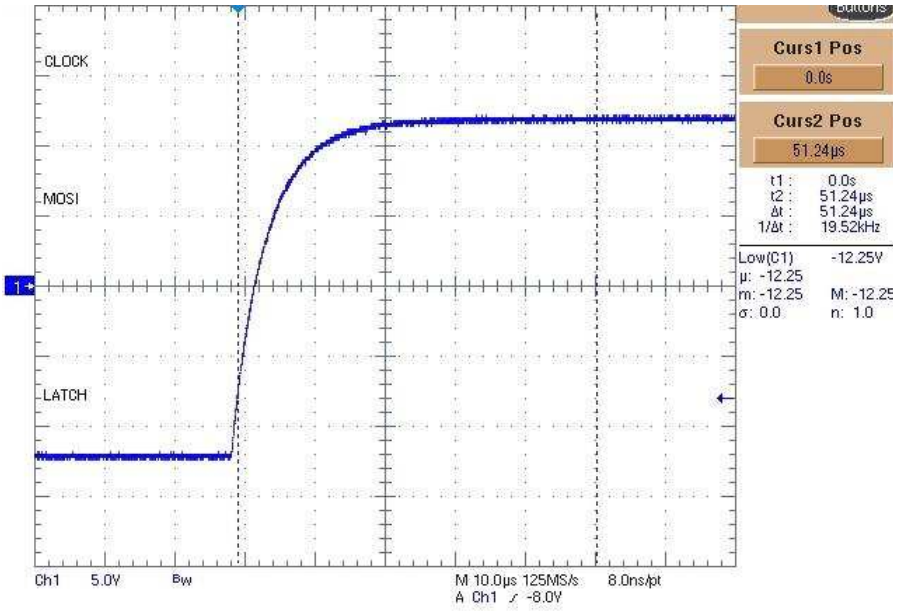


Figure 24. MUX Switching From -12.25 V to +12.25 V

Figure 25 shows the charging curve of the RC-filter in front of the ADC for eight switching cycles. It was shown previously that the charging time of the RC-filter is 51.24 µs until its charged value is less than 1/2 bit different to its final value. However, the complete switching sequence for all eight channels takes 460 µs, which is more than 8·51.24 µs = 409.84 µs. This is due to the time that is needed to switch between the MUX channels. In this test, the switching is controlled by the MSP430FR5969 that is running at a speed of 8 MHz.

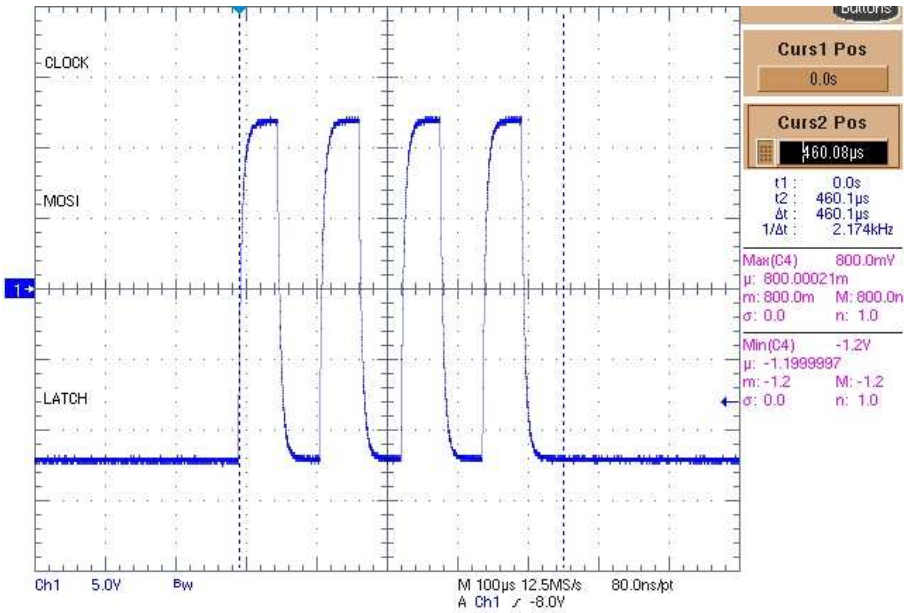


Figure 25. Timing of Eight MUX Switching Cycles

A total cycle time of around 410 µs results in a maximum theoretical input signal frequency of 2.4 kHz over eight channels. But, it must be considered that the system also needs time for SPI communication between the MCU and the ADC that will reduce the system bandwidth further, depending on the speed of the SPI communication.

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00764.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00764.

7.3 PCB Layout Recommendations

Any additional note you think the customer would need to layout this board; also add details on the reasoning behind your layout (form factor, heat distribution, and so forth).

7.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00764

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00764.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00764.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00764

8 References

1. TIDA-00550 – Dual Channel-to-Channel Isolated Universal Analog Input Module for PLC Reference Design

9 About the Author

TOBIAS PUETZ is a systems engineer in the Texas Instruments Factory Automation and Control team, where he is working on PLC modules. Tobias brings to this role his expertise in different sensing technologies, power design, and wireless charging as well as software design. Tobias earned his master's degree in electrical engineering and information technology at the Karlsruhe Institute of Technology (KIT), Germany in 2014.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to A Revision	Page
• From preview mode to active mode	1

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