TI Designs

Wideband Receiver with 66AK2L06 JESD204B Attach to ADC32RF80 Reference Design

Description

TIDEP0081 reference design demonstrates a wide-band receiver design using TI's 66AK2L06 SoC and TI's ADC32RF80 and DAC38J84 high performance wide-band data converters. This design highlights the 66AK2L06's JESD204B and Digital Front-End (DFE) capabilities to directly attach to JESD204B enabled data converters and provides an efficient signal processing solution for Test and Measurements, Avionics and Defense, and Industrial Applications.

Resources

TIDEP0081	Design Folder
66AK2L06	Product Folder
ADC32RF80	Product Folder
DAC38J84	Product Folder
LMK04828	Product Folder

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Features

- Easy Integration of Signal Processor to Data Converters Over JESD204B
- Multichannel Sampling Rates up to 368 Msps Complex With up to 150 MHz of Processing Bandwidth (2x75 Mhz or 1x100 Mhz)
- Digital Front End (DFE) Processing for Filtering, Down Sampling, or Up Sampling
- System Optimized for Test And Measurement, Avionics and Defense, and Industrial Applications
- Wideband Sampling With JESD204B Attached Signal Processing Solution Including DSP, Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC) Boards, Demo Software, Configuration Graphical User Interface (GUI), and Getting Started Guide

Featured Applications

- Test and Measurement
- Avionics and Defense
- Industrial Applications

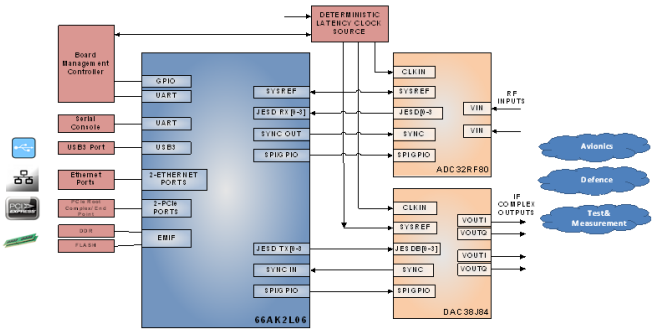

Figure 1. Block Diagram

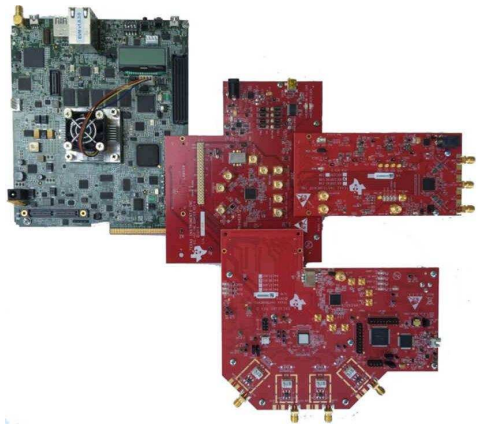

Figure 2. Board Design

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1 System Overview

1.1 System Description

This design guide demonstrates performance of the high-speed JESD204B connectivity between the 66AK2L06 System-on-Chip (SoC) with industry-leading high-speed data converters. This design also demonstrates the signal-processing capabilities of 66AK2L06 hardware co-processors (FFTC), DSP CorePacs, and control processing power using ARM CorePacs. The hardware block diagram shown in Figure 3 explains high-level connectivity of the 66AK2L06 device with ADC32RF80 and DAC38J84 for different applications. The ADC/RF sampling ADC that best matches the requirements of each industry application with JESD 204B data-output is selected. The analog input is digitized, signal processing is applied, and then the data is transported to the 66AK2L06. The 66AK2L06 receives the data, performs signal processing, and then other internal hardware co-processors are utilized. The 66AK2L06 can receive or send data out through any of the available interfaces including Ethernet, or PCIe. The 66AK2L06 develops transmit signals that are transmitted over JESD204. The DAC38J84 converts the digital transmit stream into analog outputs. There are additional JESD204B DAC devices that can be selected to best match the transmit (Tx) requirements.

The 66AK2L06 DSP+ARM Processor JESD204B Attach to ADC32RF80, DAC38J84 is well suited for applications such as:

- Communications test: Mobile handset testers, radio communication analyzer, base station analyzer, RF test cards
- General-purpose test: Spectrum analyzers, vector or signal analyzer, vector or signal generator, oscilloscopes
- High-speed data acquisition and generation
- Electronic warfare and communications: Military radar, civilian radar, synthetic-aperture radar (SAR), signals intelligence (SIGINT/ELINT), countermeasure
- Missiles and ground defense: Missile guidance and control systems, missile compute platforms, monitoring systems
- Military aircraft and general aviation: Unmanned systems, munitions, surveillance or mobility aircraft

1.2 Key System Level Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Multiple processors in SoC	4, 1.2-Ghz floating-point DSP, 2, 1.2-Ghz floating-point A15 ARM™, multiple hardware accelerators	Section 1.4.1
DFE, and 4 lane Tx and receiver (Rx) JESD204B	Channel and stream processing for DFE, 1, 2, or 4 Tx and Rx streams transcoded to JESD204B interface, 1 or 2 stream 368.64 Msps complex rate.	Section 1.4.1, Section 1.5
Multiple peripherals for communications	2, 1.25-Ghz SGMII Ethernet, 2, 2.5/5G PCIe interfaces. 1, USB 3.0	Section 1.4.1
Multiple peripherals for control	Two multi-CS (chip select) 4 wire serial peripheral interface (SPI), two universal asynchronous receiver/transmitter (UART), two inter-integrated circuit (I2C), 16 general-purpose input/output (GPIO)	Section 1.4.1
Multiple busses for RAM and Flash	Support for DDR3-1600, EMIF 16-bit flash	Section 1.4.1
RF sampling ADC, multiple streams	Two RF sampling ADCs, up to 3 Gsps, with two digital down converters for each ADC, JESD204B transport, two digital down converters for digital processing	Section 1.4.2, Section 1.5
IF sampling DAC, Multiple streams	Two IQ stream to digital IF to complex analog outputs up to 1 Gsps, two digital up converters, JESD204B transport, one/two upsampling complex DAC, with analog outputs up to 1Gsps	Section 1.4.3, Section 1.5

1.3 Block Diagram

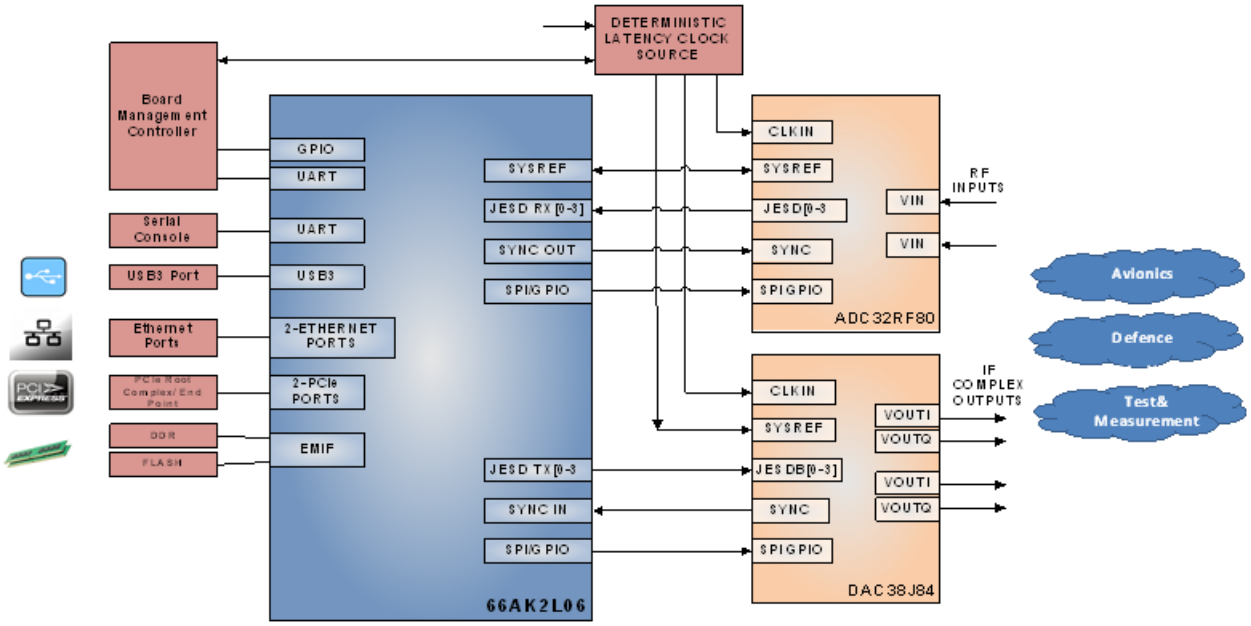

Figure 3. Block Diagram

1.4 Highlighted Products

1.4.1 66AK2L06

The 66AK2L06 is a member of the C66x family based on TI's new Keystone™ II Multicore SoC architecture. The SoC is a lower power, smaller size, and lower-cost solution with four transmit and four receive lanes of the JESD204B interface to meet the requirements of test and measurement, avionics and defense, industrial, and medical applications. The device's ARM and DSP cores deliver exceptional processing power for platforms needing high signal and control processing. The Keystone II architecture provides a programmable platform integrating various subsystems (ARM CorePacs, C66x CorePacs, IQN, DFE, FFTC, 4- Port Ethernet Switch, and so on) and uses a queue-based communication system that allows the SoC resources to operate efficiently and seamlessly. This unique SoC architecture also includes a TeraNet switch that enables a wide mix of system elements, from programmable cores to dedicated co-processors and high-speed I/O, to allow each of them to operate at maximum efficiency with no blocking and stalling. The 66AK2L06 SoC is part of TI's scalable multicore SoC architecture solution that provides developers with a range of software-compatible and hardware-compatible devices to minimize development time and maximize reuse across all applications. The following are some of the key features that enable the SoC to be used in the test and measurement, avionics and defense, medical, and industrial applications:

- JESD204A/B Compliant Four Tx and Four Rx lanes supporting speeds up to 7.37 Gbps
- 2× FFT Co-processor with support for maximum FFT size 8192
- Two-Gigabit Ethernet SGMII ports
- Two shared Gigabit Ethernet SGMII/PCie ports
- Four C66x CorePacs and two ARM CorePacs operating up to 1.2 GHz
- DFE with channel and stream signal processing, filtering, sample rate conversion, frequency translation

For more information, see the 66AK2L06 product page.

NOTE: The (*) indicates a shared SERDES interface.

For additional information, see Figure 3.

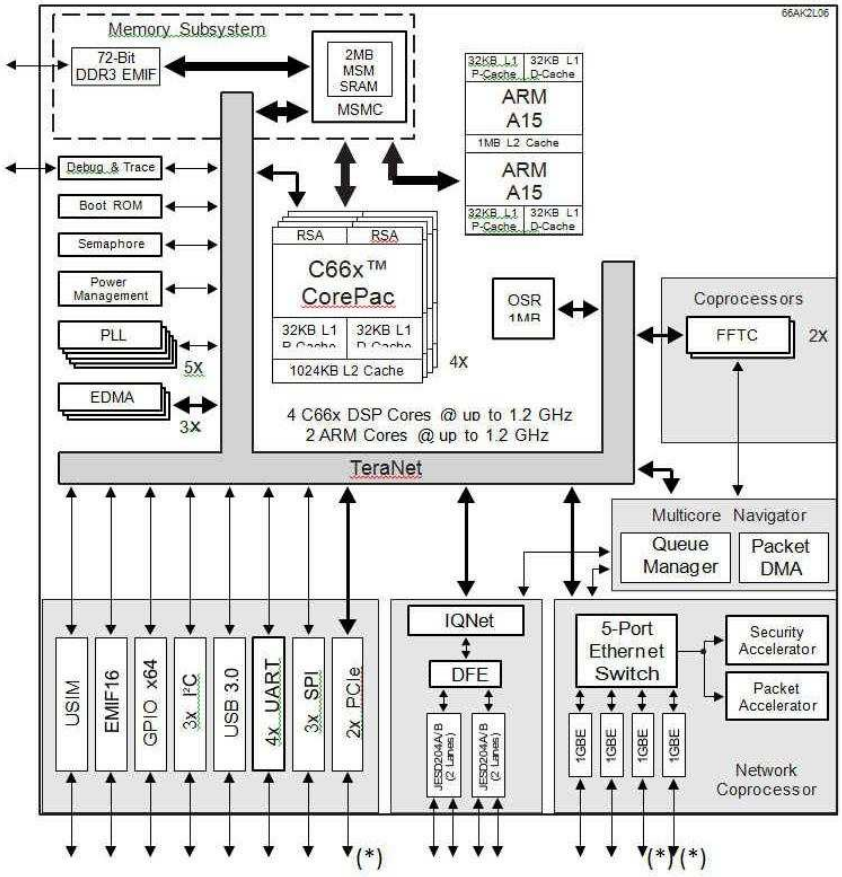

Figure 4. 66AK2L06 Block Diagram

1.4.2 ADC32RF80

ADC32RF80 is an RF sampling ADC with multiple ADC and digital down converters. There are two sets of ADCs, two digital down converters (DDC) for each ADC, signal switching, and JESD204B data transport. Each ADC set provides gigasample digitization of the analog input. Each ADC has two DDCs. The DDC contains a digital numerically controlled oscillator (NCO), half complex mixer, finite impulse response filters (FIR), and a decimation block. The single or dual DDC architecture can be used to select different ADC Rx streams and sample rates to be transported over the JESD204B interface. The ADC32RF80 supports a maximum sampling rate of 3000 Msps. There are additional ADC32RF4x RF sampling ADCs that have a lower sample rate or for lower cost applications.

For more information, see the ADC32RF80 product page

1.4.3 DAC38J84

DAC38J84 is a low-power, 16-bit, quad-channel, 2.5-GSPS DAC with a JESD204B interface. The JESD204B interface output is selectable for the 4 I or Q streams. The signal processing in the DAC38J84 provides for interpolation (1 – 16x), frequency translation with an NCO and complex mixer, quadrature mirror correction (QMC) for IQ correction, and digital combiner signal processing. The device can have one or two complex transmit streams. The transmit stream is then converted to analog DAC outputs. The DAC38J82 is available as a single complex transmit stream device.

For more information, see the DAC38J84 product page.

1.5 Design Considerations

The combination of the ADC32RF80 RF sampling ADC, and the 66AK2L06 provide for a heterodyne radio down-conversion architecture.

- First stage down conversion, ADC32RF80
- Second and third stage down conversion in 66AK2L06 DFE

The ADC32RF80 provides the first RF → IF or RF → zero IF frequency translation. The digital front end (DFE) in the 66AK2L06 provides further digital down conversion of the receive stream and channel processing.

The DFE 66AK2L06 and DAC38J84 provide a heterodyne radio up conversion architecture.

- First stage and second up conversion is provided by the 66AK2L06-DFE
- Third stage is provided by the DAC38J84

DFE in the 66AK2L06 provides for channel and stream digital up conversion for the transmit streams. The DAC38J84 provides the final up conversion to IF frequency. Future DAC architectures, with higher interpolation and different signal processing, will support direct IQ to RF output within the same JESD204B transport to 66AK2L06.

The Design 4 example has 1 transmit stream or 2 transmit streams. The complex transmit architecture and JESD204B interface can support 1, 2, or 4 Tx streams. The Design 4 example has 2 receive streams. The complex receive architecture and JESD204B interface can support 1, 2, or 4 Rx streams (see Figure 5).

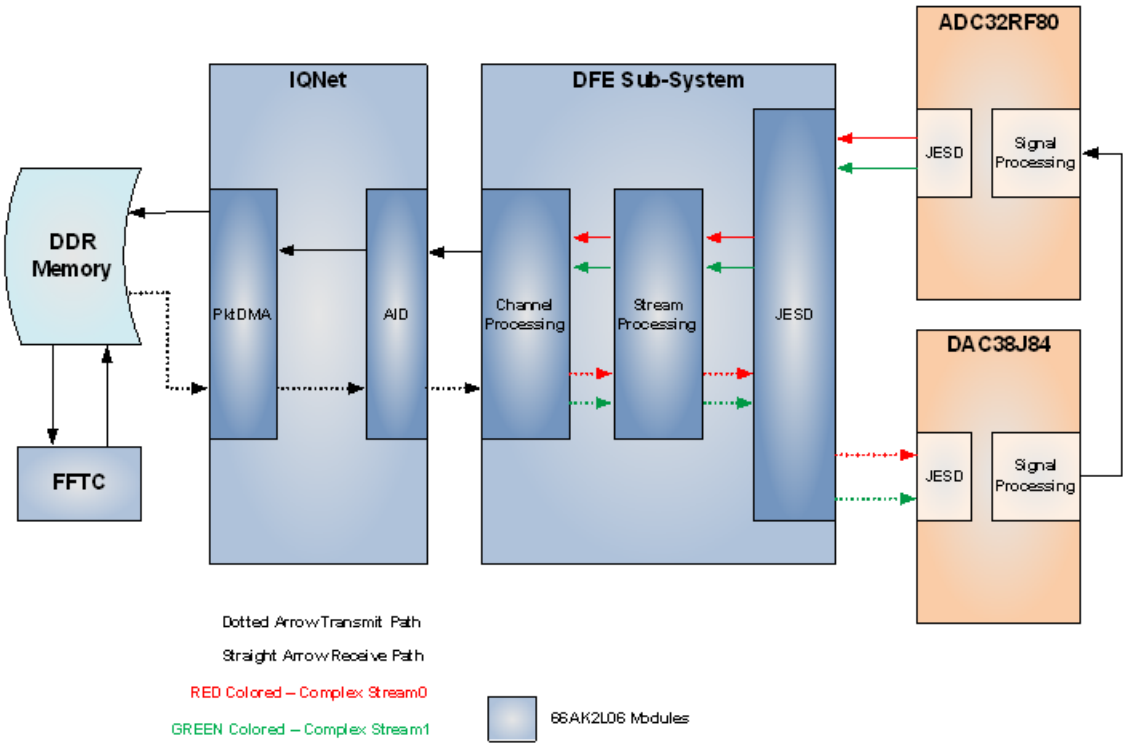

Figure 5. Tx and Rx Data Flow for Design 4

1.5.1 DFE Baseband Data

The 66AK2L06 utilizing the DDR memory can store output-complex data for transmission in the DFE radio up conversion. The baseband data is transported within the 66AK2L06 in a DMA method, moving the data from DDR3 to MSMC, then to IQNet. IQNet reformats the packet-based information to a 4 sample packet time packet, and forwards to DFE. The data is stored in a 10 ms framed format. For the DSP to IQNet data flow, see Figure 5.

The DDR memory has a BBTx (transmit) set of channel-frame-IQ data, that can be updated by you or the software application, to send to Tx processing.

The 66AK2L06 utilizing the DDR memory can receive store-complex data for reception in the DFE radio down conversion. The DFE sends four samples per channel packets to IQNet. The baseband data is transported within the 66AK2L06 in a DMA method, moving the data from IQNet to MSMC, to DDR, then to FFTC. The data is stored in a 10 ms framed format.

The DDR memory has a BBRx (receive) set of channel-frame-IQ data, that can be read by you or the software application, received from Rx processing.

NOTE: The customer application replaces the DDR data movement with DSP and or ARM buffers for further processing. In advanced applications, there may be additional data transported to PCIe, SGMII, or USB.

1.5.2 Transmit Data From 66AK2L06 Over JESD204 to DAC38J84

The packet (PktDMA) engine inside the I/Q Network (IQNet) module reads the pre-defined input data stream from DDR memory and transfers it to the Antenna Interface for DFE.

The DFE baseband logic (BB) converts the 4 sample packet to channel in time samples. The BBTx channel data is received at a 92.16 Msps complex rate.

The digital down up converter (DDUC) performs the channel up conversion. The DDUC provides a programmable FIR filter (PFIR), fractional and integer interpolation, and channel numerically controlled oscillator (NCO)/complex mixer for each channel (1-24 channels, in this example 2 channels). The channel up conversion filters the BBTx channel data with the PFIR for a 75 Mhz channel bandwidth.

The SumChain combines the channels into Tx streams (1-4 Tx streams, in this example 2 streams). The Crest Factor Reduction (CFR) block can provide further interpolation. The CFR DPD fractional resampler (CDFR) and transmit block (Tx) provide two additional stages of digital up conversion.

NOTE: In the 66AK2L06 DFE Tx, the DPD sub block is not utilized.

In the CDFR block, the transmit streams from 92.16 to 368.64 Msps are further interpolated. Each Tx stream has frequency translation applied, IF NCO (-45 and 45Mhz), and then the two streams are combined to a single Tx stream. The Tx stream has a 368.64 Msps complex rate, with a 294 Mhz passband. The Tx streams in the Tx block can have 1 combined or 2 individual streams.

The JESD204B transport takes the complex data, and converts this to a frame based, multi-lane serial signal. The 16bit I or Q data is 8B/10B encoded, framed with JESD204B synchronization and error detection, and transported over a SERDES interface. This is synchronized and transported from DFE to the DAC38J84. This example has 1 IQ stream over two lanes. We could also support 2 IQ streams over 4 lanes.

The DAC38J84 receives the serial streams, JESD204B two lanes at 7.3728Gbps, switches the stream I and Q components to specific transmit stream complex sets (in this example complex channel A). The DAC38J84 provides the further interpolation, stream IF NCO mixing, and then provides for additional IQ QMC correction, and digital combining. The DAC38J84 provides an interpolation of 2, 737.28Msps complex rate and the coarse mixer/NCO fine mixer provides the IF frequency conversion (184.32 Mhz for this application), see Figure 6.

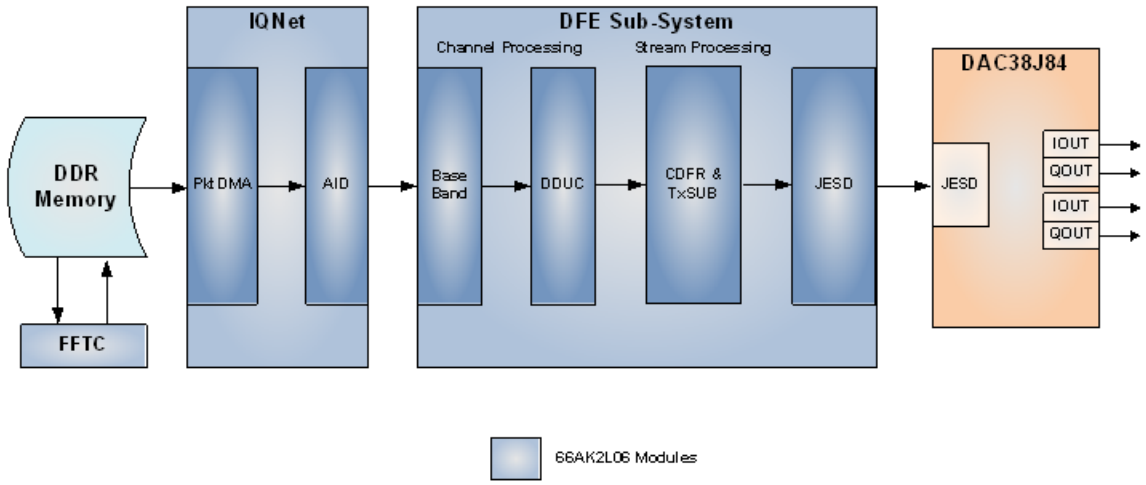

Figure 6. Tx Data Path

1.5.3 Receive Data From ADC32RF80 Over JESD204B to 66AK2L06

The ADC input through a low-pass or band-pass filter, to provide attenuation of unwanted IF or RF signals. The ADC32RF80 is operated in the first Nyquist zone (DC to sample clock/2) for this test. The ADC32RF80 has two ADCs, the ADC-B is being used, and DDC-B0 and DDC-B1 signal processing blocks. The ADC32RF80 digitizes the analog input signal at the sampling frequency (DEVCLK) of 2949.12 MHz, see Figure 7.

The ADC digitized signal is routed to NCO1 and NCO2. In this example, each NCO is set to down convert an IF frequency, the bandwidth of each NCO/decimator block is set by (DEVCLK * .8)/decimation ratio. The NCOs are set to 139.32 (-1*(-45+184.32)) and 229.32 (-1*(45+184.32)). The single ADC stream is digital down converted to 2 Rx output streams. Each Rx output stream produces a zero-IF based output. The NCO output is routed to the digital filter, and then decimated to the desired IQ rate. The digital filter and decimator provide an 80% bandwidth at the DEVCLK/decimation IQ rate. The decimation is set to 8, each Rx stream is 368.64 Msps complex sample rate, 294 MHz bandwidth.

The 368.64 Msps IQ stream, is serialized and output at 7.3728 Gbps. The 66AK2L06 receives the 4 JESD204B lanes of data from the 2 Rx streams. In the 66AK2L06 the JESD204 data is converted to parallel IQ at the 368.64 Msps rate for each stream. The JESD block routes Rx stream 0 to the Rx block, and Rx stream 1 to the Feedback block in DFE. This Rx stream routing increases the stream bandwidth that can be processed (if two streams were routed to the Rx block, the IQ rate would be 184.32 Msps).

The Rx and Feedback blocks in DFE provide the stream block down conversion capability. In this example, since the ADC32RF80 performed RF to zero IF translation, the stream processing processing NCOs are set to 0. The Rx stream input (368.64 Msps rate) bandwidth is 294 Mhz. The Rx and FDBK each process an Rx stream, frequency, translation ± 45 Mhz, and decimate by 2 filtering (184.32 Msps rate). The Rx stream output bandwidth is 80% of 184.32 Msps complex rate, 147 MHz.

The DDUC is used as the channel down conversion, has a signal selection, NCO, integer and fractional decimation filters, and a PFIR filter. The DDUC PFIR decimates by 2, to provide the 92.16 Msps (75 Mhz bandwidth) complex baseband sample rate. There is one BBRx output for each stream.

The PktDMA in IQNet sends the data to DDR memory. The DDR memory data is stored to a file, used with the web page for visualization, sent to the FFTC co-processor for further processing, or the DDR data is saved to a file. For more information, see Figure 4 or Figure 7.

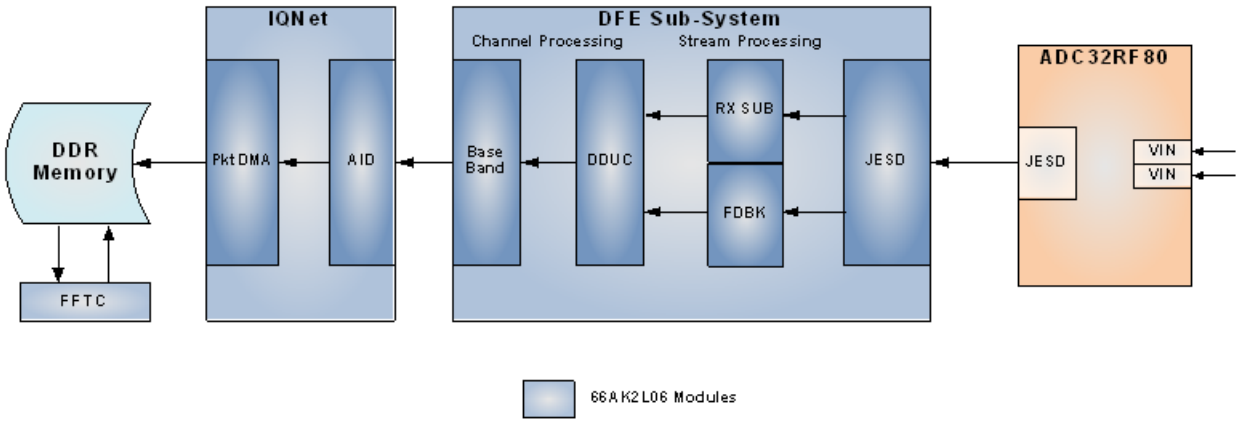

Figure 7. RX Data Path

1.5.4 JESD204B Capabilities and Configurations

The JESD204B module is capable of the following:

- Four transmit lanes with up to 7.37 Gbps each
- Four receive lanes with up to 7.37 Gbps each
- Alignment across multiple lanes within a single converter or multiple converters
- Support for subclass 0 and 1

In the demo application, the 66AK2L06 communicates with the ADS32RF80 over 4 lanes operating at a link rate of 7.37 Gbps. The 66AK2L06 communicates with the DAC38J84 over 2 lanes operating at a link rate of 7.37Gbps (note can be expanded to 2 Tx streams using 4 lanes).

SYSREF is a special synchronization signal for JESD204B subclass 1. In this example, it is A JESD subclass 1 configuration is used with a SYSREF frequency of 120 Khz. Data scrambling is not used in this application. Table 2 shows the JESD link-parameters configuration.

Table 2. JESD Link Parameters

JESD PARAMETER	66AK2L06 CAPABILITY	PARAMETERS USED IN DEMONSTRATION	
		ADC32RF80 66AK2L06	66AK2L06 DAC38J84
M – (Number of Converters per Device)	The M is limited by the number of lanes L and supported formats F	4	4, 2 4 - for 2 streams
N – (Resolution of Converters)	We process this as 16bit signed integer. Can zero lower bits not used.	14	16
N' - (JESD Word Size)	Limited to 16 bits	16	16
L - (No of Lanes)	numLanes limited to 4 for 66AK2L06	2	2 (or 4 - for 2 streams)
F - (No of Octets per Frame)	Calculated based on other parameters 2,4,8 for 66AK2L06	2	2
K - (No of Multiframes)	Limited to 32 in 66AK2L06	16	16
S - (Samples per Converter per Frame)	Limited to 1 in 66AK2L06	1	1

1.5.5 FFT Processing

The FFT co-processor (FFTC) modules in 66AK2L06 provides the following features:

- IFFT and FFT operations
- Maximum FFT size of 8192
- Processing up to 1200 Msps for a FFT size of 1024
- 77-dB SNR—dynamic and programmable scaling modes
- Support for FFT shift (switch left and right halves)
- Support for cyclic prefix addition or removal

2 Getting Started Hardware

The 66AK2L06 DSP+ARM Processor JESD204B Attach to ADC32RF80 and DAC38J84 utilizes the three EVMs, and a deterministic latency card K2L-HSP FMC (DLC) for hardware. The software is part of the RFSDK 2.0.6 software release. For the 66AK2L06 RFSDK software, there is additional GUI software programmation for the ADC32RF80 EVM GUI, DLC GUI, and DAC38J84 EVM GUI.

The DLC and RFSDK 2.0.6 software are requested on the TI web link: http://www.ti.com/tool/rfsdk. Figure 8 shows that the 66AK2L06 EVM, ADC32RF80 EVM, and DAC38J84 EVMs are connected through the DLC board that provides signal routing and data converter clocks.

The DLC card uses SYSCLK provided by 66AK2L06 as an input reference clock for generating sampling clocks. The card also generates a common SYSREF clock for deterministic latency using the common input SYSCLK. The K2L-HSP FMC Adapter board routes the JESD lanes and SYNC signals from one Lamarr FMC to two data converter FMC connectors: one for ADC and one for DAC. This process allows the 66AK2L06 EVM board to communicate with both ADC and DAC EVMs over the JESD204B interface.

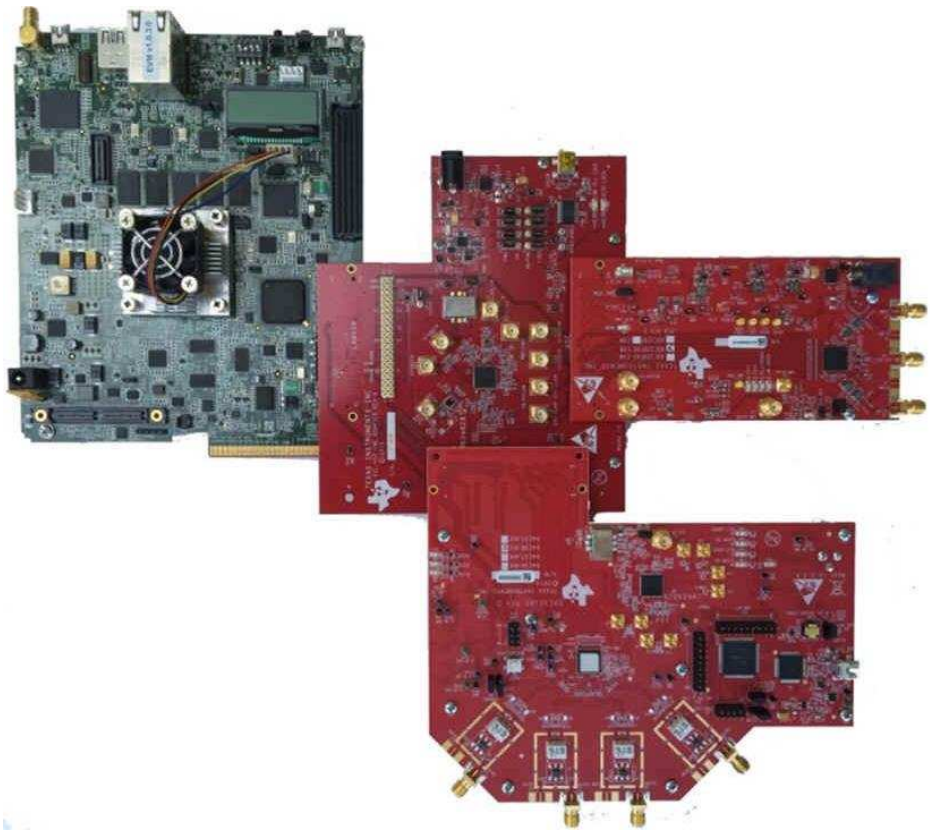

Figure 8. 66AK2L06 DSP+ARM Processor JESD204B Attach to ADC32RF80 DAC38J84 Example

2.1 Getting Started Software

The 66AK2L06 DSP+ARM Processor JESD204B Attach to ADC32RF80 and DAC38J84 Design provides a Linux application developed using software development kits available from Texas Instruments. The ADC32RF80, DAC38J84, and DLC cards have additional GUI control software.

For additional information on the 66AK2L06 EVM, see http://ti.com/tool/xevmk2lx.

For additional information on ADC32RF80 EVM, see http://www.ti.com/tool/adc32rf80evm.

For additional information on DAC38J84 EVM, see http://www.ti.com/tool/dac38j84evm.

NOTE: The DLC EVM information, contact your TI representative.

2.1.1 Multicore Software Development Kit (MCSDK)

The MCSDK provides foundational software for TI KeyStone II devices. The MCSDK encapsulates a collection of software elements and tools intended to enable customer application development and migration. The foundational components include:

- TI-RTOS real-time embedded operating system on DSP cores
- Linux high-level operating system running on ARM A15 cluster (SMP mode)
- DSP chip-support libraries, DSP/ARM drivers, and basic platform utilities
- Interprocessor communication for communication across cores and devices
- Bootloaders and boot utilities, power-on-self test

2.1.2 RF Software Development Kit (RFSDK)

The RFSDK is an integrated software solution that simplifies leveraging all the components of the 66AK2L06 digital front-end (DFE) module. The RFSDK aims to provide an integrated environment to transmit, receive, process, and visualize signals.

- Provides an integrated solution requiring a minimal amount of software development to enable the JESD data converters
- Provides tools for evaluation and debug of integrated solution with 66AK2L06 devices and data converters

2.1.3 Design Linux Application

The 66AK2L06 DSP+ARM® Processor JESD204B Attach to ADC32RF80 DAC38J84 Design Linux application has the following features:

- The application configures the operation of IQN2 and DFE (and required infrastructure such as Navigator, Serdes, DDR, and others) for Tx and Rx according to a particular configuration.
- Pre-defined distinct signal patterns can be loaded in the Tx buffers (DDR memory) to continuously transmit known data patterns on both carriers. Data patterns are 10 msec (one frame) IQ samples and are loaded into memory from where they are played out.
- Tx data can be looped back to Rx at multiple loop points (IQN2, JESD, or external). External Rx data can also be supplied to the receiver to capture external Rx signal (for example, from a signal generator).
- When requested, playback can capture 10 msec worth of samples at a receiver-in-capture buffer in DDR.

3 Testing and Results

3.1 Test Setup

Figure 8 shows the EVM hardware used for this test. Figure 9 shows the connectivity of the various boards. For more information about the test setup, see the Wideband Receiver Using 66AK2L06 JESD204B Attach to ADC32RF80 Design GSG Getting Started Guide.

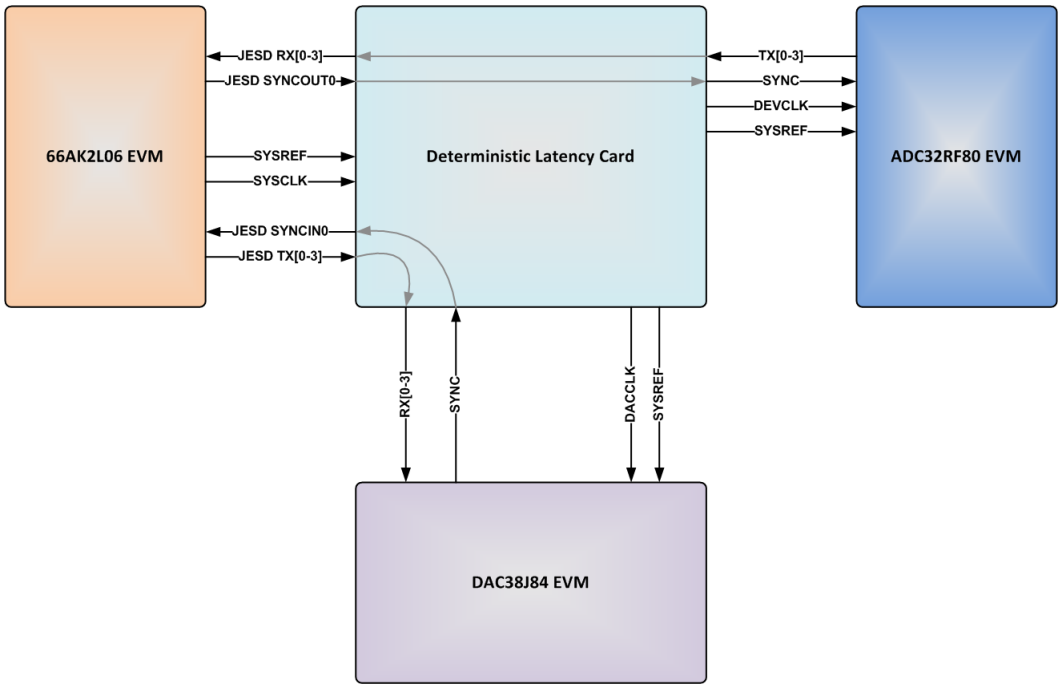

Figure 9. Hardware Connectivity Diagram

- JESD Tx[0-3] – Four 66AK2L06 JESD transmit lanes connecting with Rx[0-3] through DLC card
- Rx[0-3] – Four DAC38J84 JESD input lanes
- JESD Rx[0-3] – Four 66AK2L06 JESD receive lanes connecting with DS[0-3] through DLC card
- Tx[0-3] – Four ADC32RF80 JESD output lanes
- JESD SYNCIN0 – 66AK2L06 SYNC input connected with DAC38J84 SYNC through DLC card
- JESD SYNCOUT0 – 66AK2L06 sync output connected with ADC32RF80 SYNC through DLC card
- SYSCLK – 122.88-MHz SYSCLK from 66AK2L06 routed through and back to DLC as clock input source for generating sampling clock and SYSREF clock for ADC and DAC
- DEVCLK – 2949.12-MHz sampling clock generated by DLC card for ADC32RF80
- DACCLK – 737.28-MHz sampling clock generated by DLC card for DAC38J84
- SYSREF – The separate EVMs each have a different SYSREF; in an actual application on one board, a single frequency would be used. The ADC32RF80 would receive SYSREF from the JESD204B clock solution.

3.2 Test Data

The EVM hardware, combined with the RFSDK software, DLC GUI software, DAC38J84 GUI software, and ADC32RF80 GUI software is used for configuration.

There are several places the DFE to DAC Tx and ADC to DFE Rx signals can be monitored. To check for proper operation, external equipment to monitor the analog signals can be used.

3.2.1 Tx Signal Monitor

There are several places the BBTx to stream Tx to analog output can be monitored. Standard monitoring internal to 66AK2L06 is provided in the provided in the *RFSDK User's Guide* included in the RFSDK release.

- RFSDK BBTx at DSP webpage display (see Section 3.2.1.1)
- RFSDK Tx Signal Capture at DFE webpage display
- DAC output with test equipment (see Section 3.2.1.1)

3.2.1.1 BBTx Data Monitor

Figure 10 shows the BBTx data captured from DDR memory. In this example the -1,2Mhz dual tone is selected for loading in BBTx0, and the 240 tone signal is selected for loading in BBTx1. The Tx data captured with the RFSDK visualization tools. This data is the raw baseband data that is processed by the 66AK2L06 DFE Tx and converted by the DAC to an analog output.

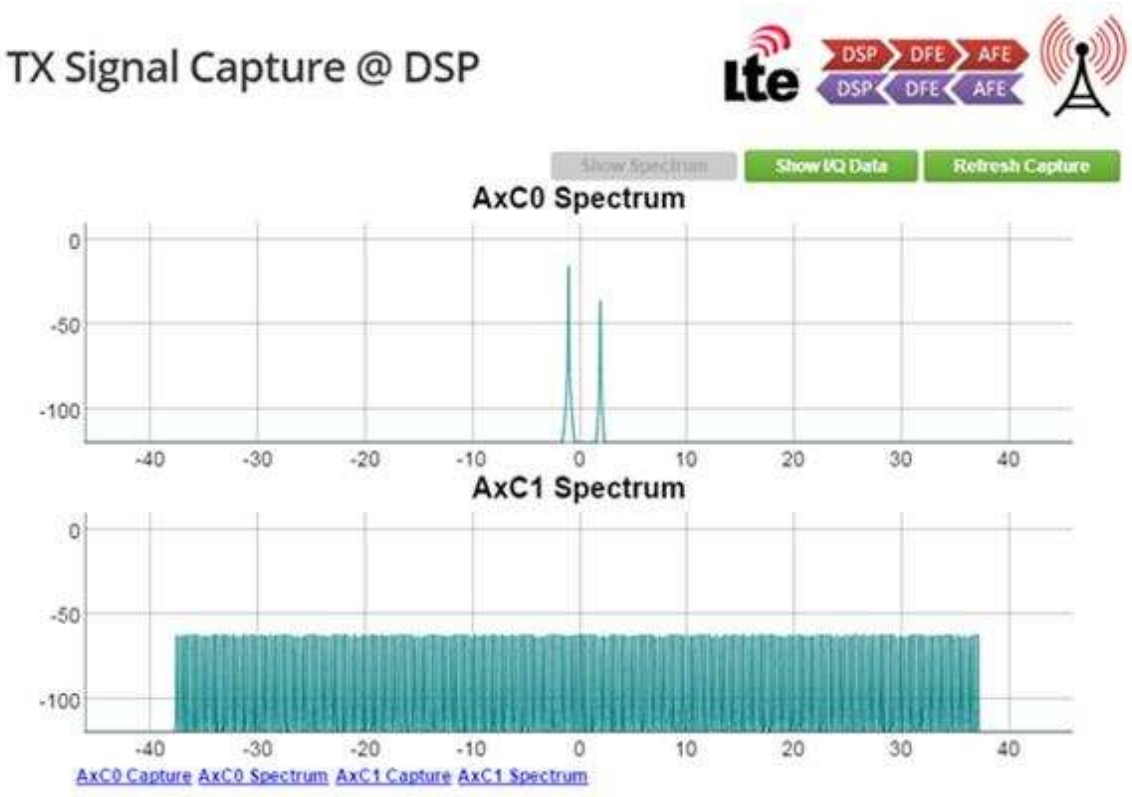

Figure 10. Tx Data - Dual Tone and Multitone Signal

3.2.1.2 DAC Tx Analog Output Monitoring

Figure 11 shows the Tx data captured with a spectrum analyzer. This data has been processed by the Tx path of the 66AK2L06 DFE and converted by the DAC. The data is captured at the output of the DAC. The two 92.16 Msps BBTx channels are frequency mixed and summed to a single output stream to represent a digitally combined stream, sampled at 368.64Msps. The DAC further interpolates by 2, and provides the 184.32 Mhz IF NCO frequency shift. This was measured at the DAC EVM output with a spectrum analyzer.

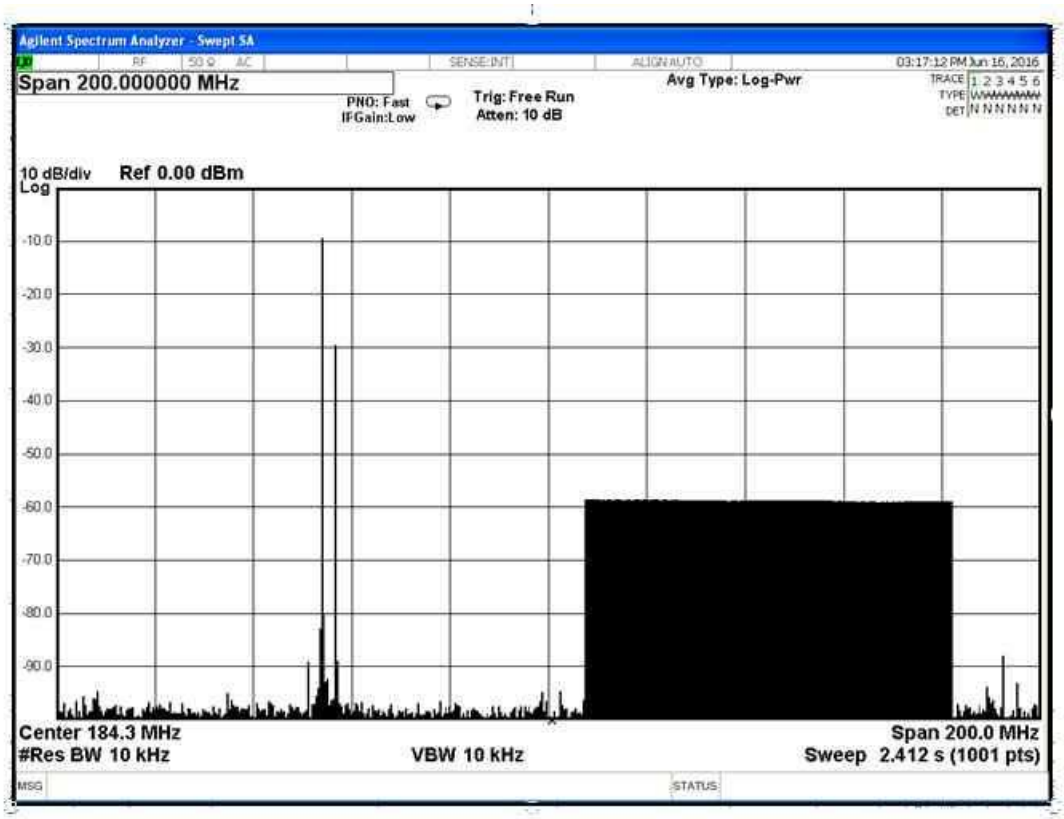

Figure 11. DAC38J84 I_{OUT} Spectrum Analyzer Measurement

3.2.2 Rx Signal Monitor

There are several places the Rx analog input stream to Rx or Feedback stream processing to BBRx channel output can be monitored. Standard monitoring internal to 66AK2L06 is provided in the RFSDK.

- ADC input after Anti-alias/bandpass filter, similar to Figure 11
- RFSDK feedback signal capture at DFE web age display – after JESD Rx data is decoded and stream processed in DFE Feedback.
- RFSDK Rx signal capture at DFE web page display – after JESD Rx data is decoded and stream processed in DFE Rx.
- RFSDK Rx signal capture at DSP web page display – the BBRx data after channel processing, sent through IQN to PktDMA to DDR memory, the data can be visualized, see Figure 12

NOTE: In the Rx stream to BBRx channel processing, the two channels are split into two streams at the ADC32RF80 mixer and decimation filter. If displayed, the Rx signal capture at DFE or feedback signal capture at DFE, the two different down converted stream data at 0IF can be seen.

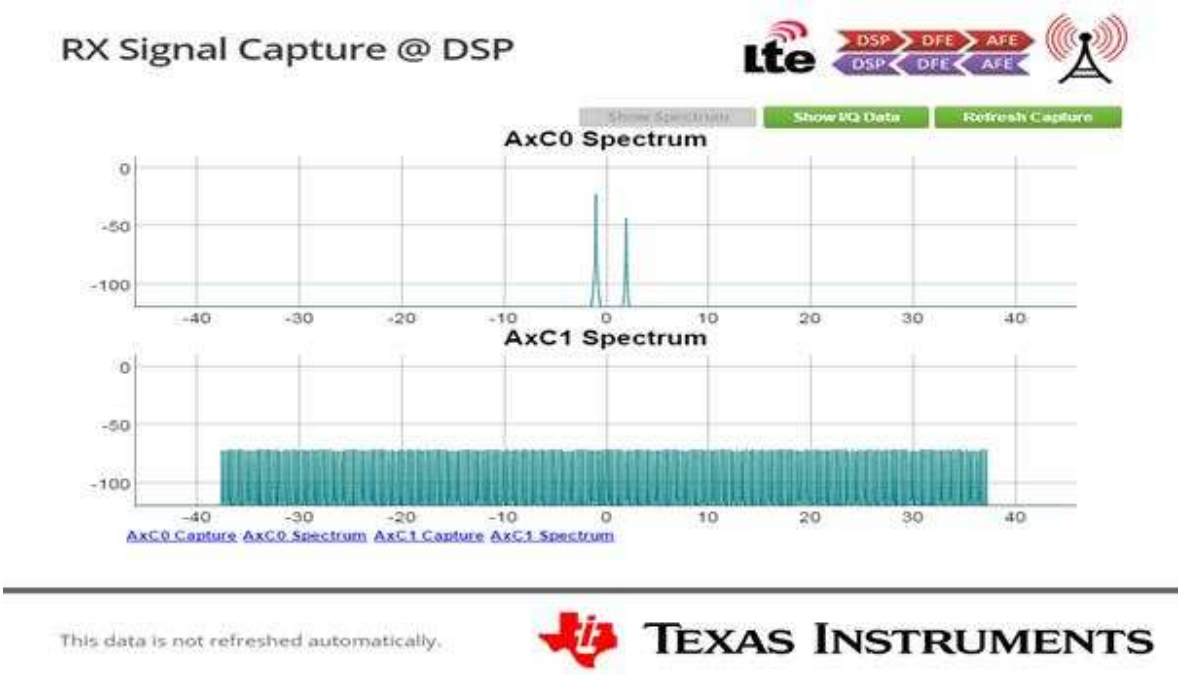

Figure 12. RFSDK, BBRx Capture at DSP Showing Two BBRx Channels

3.2.3 Stress Testing

The 66AK2L06, DLC, 32ADC80, and DAC38J84 boards were configured, initially tested, and retested after 24 hours. The DFE JESD status registers reported no errors, the spectrum analyzer Tx, and BBRx capture was the expected result.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDEP0081.

A reference schematic and bill of materials has been created which demonstrates a consolidated JESD204B interface and deterministic clocking solution between the 66AK2L06 multi-core SoC and the ADC32RF45 and DAC38J84 data-converter devices. This reference design is based on the EVM environment described above. This reference design schematic consolidates the design to demonstrate the fundamental interfaces between these devices without the existing EVM architecture. In an actual, integrated, design with these devices, many of the supporting EVM components and connectors become irrelevant. Because of this, the reference design JESD204B, SPI, GPIO, power and clocking tree are much more simplified when compared to the multi-board EVM architectures.

Proposed system, power and clocking block diagrams are included with the schematic to provide an overall system context for the proposed integrated design.

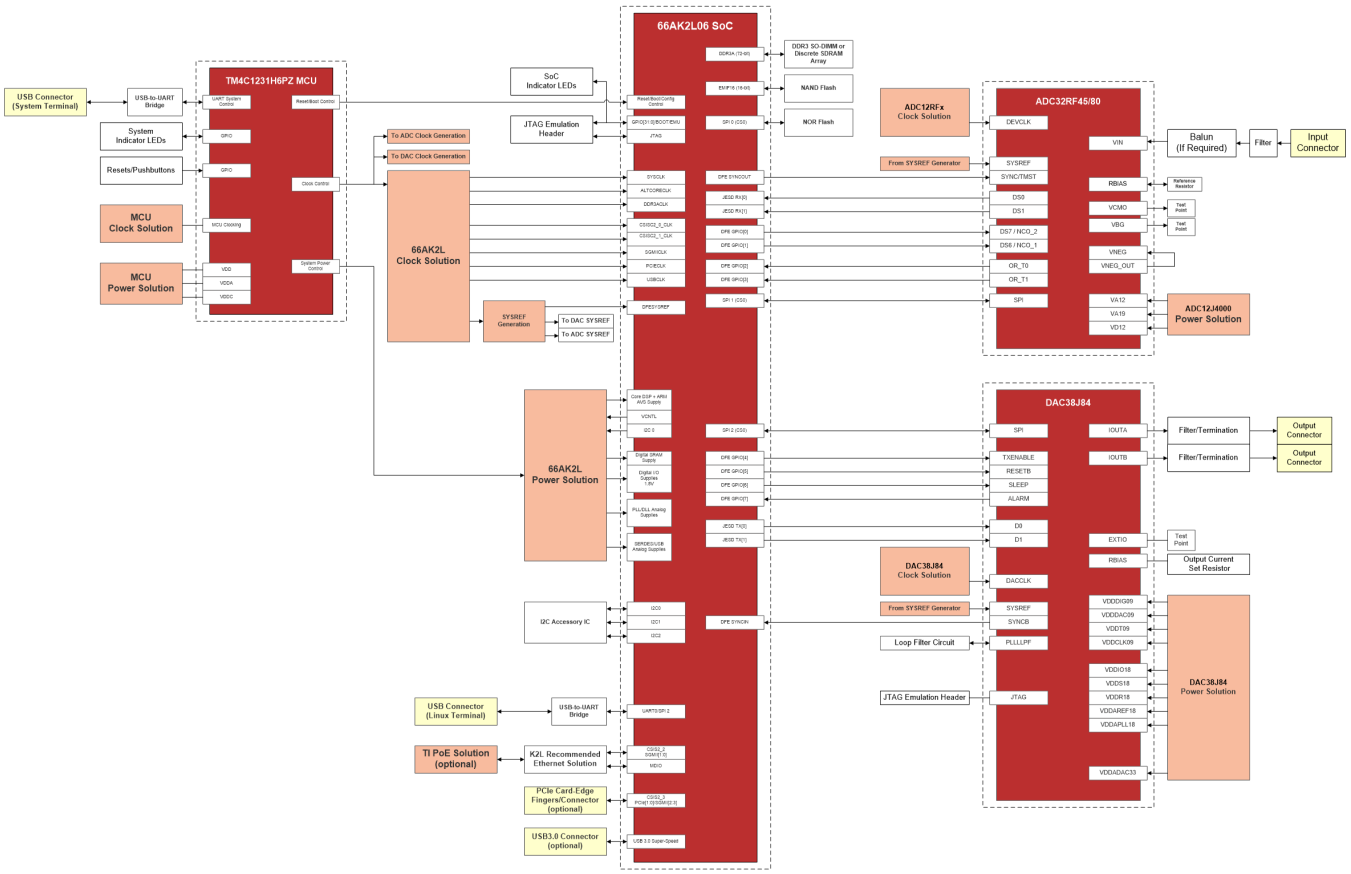

Figure 13. 66AK2L06, ADC32RF45 and DAC38J84 System Block Diagram

The major sections of the system are shown in the above block diagram:

- 66AK2L06 Multi-Core SoC mastering the ADC32RF45 and DAC38J84 data-converters over a JESD204B high-speed SERDES link, SPI serial link and multiple GPIO control and status pins
- Proposed utilization of many of the 66AK2L06 peripherals
- The consolidated JESD204B reference clock and synchronization solution
- The consolidated system power distribution
- TM4C1231 ARM® Cortex®-M4 MCU system management controller

The schematics detail out the following sections:

- K2L base system schematic with full power, decoupling, boot, JTAG/emulation, DDR3 and USB peripheral utilization shown
  - K2L JESD204B
  - USB3.0 reference schematic
  - EMIF16 NAND flash reference schematic
  - DDR3 SDRAM reference schematic
- ADC32RF45/80 schematic power, configuration, JESD and input signal conditioning blocks taken from EVM design
- DAC38J84 schematic power, configuration, JESD and output signal conditioning blocks from EVM design
- LMK04828 JESD clock tree setup shown
- CDCM6208 PLL schematic for the remainder of the K2L peripheral clocks not supported by the LMK04828 JESD system clock

- Includes the TPS544B24 for the K2L Smart-Reflex (AVS) CVDD power net
- Dual TPS65200 and Dual TPS54620 buck converter designs which service the K2L, DAC, ADC, LMK, CDCM and BMC power nets

4.2 K2L JESD204B, SPI and GPIO Interface to Data-Converters

The 66AK2L06 SoC masters the ADC32RF45 ADC through SPI port 0. It is recommended that the selected SPI port be dedicated to the task of supporting the attached ADC such that any commands to or feedback from the ADC can be serviced with the highest possible bandwidth.

The ADC32RF45 JESD SERDES transmit channel, SO± is routed to the 66AK2L06 SERDES receiver channel JESDRX0P/N, which is a subset of the 2-port SHARED_SERDES_0 block. The remainder JESD transmitter and receiver channels of the 66AK2L06 JESD interface are left unconnected in this use-case. The SERDES reference clock inputs of the SHARED_SERDES_1 block are properly left unconnected along with all of the unused transmitter and receiver differential pairs.

4.3 Power Distribution

The proposed power distribution tree consists of a single TPS544B24 buck converter, a pair of TPS65400 quad buck-converters a pair of TPS54620 buck converters and a single TPS51200 push-pull converter. The basic connectivity of the system can be seen in Figure 14.

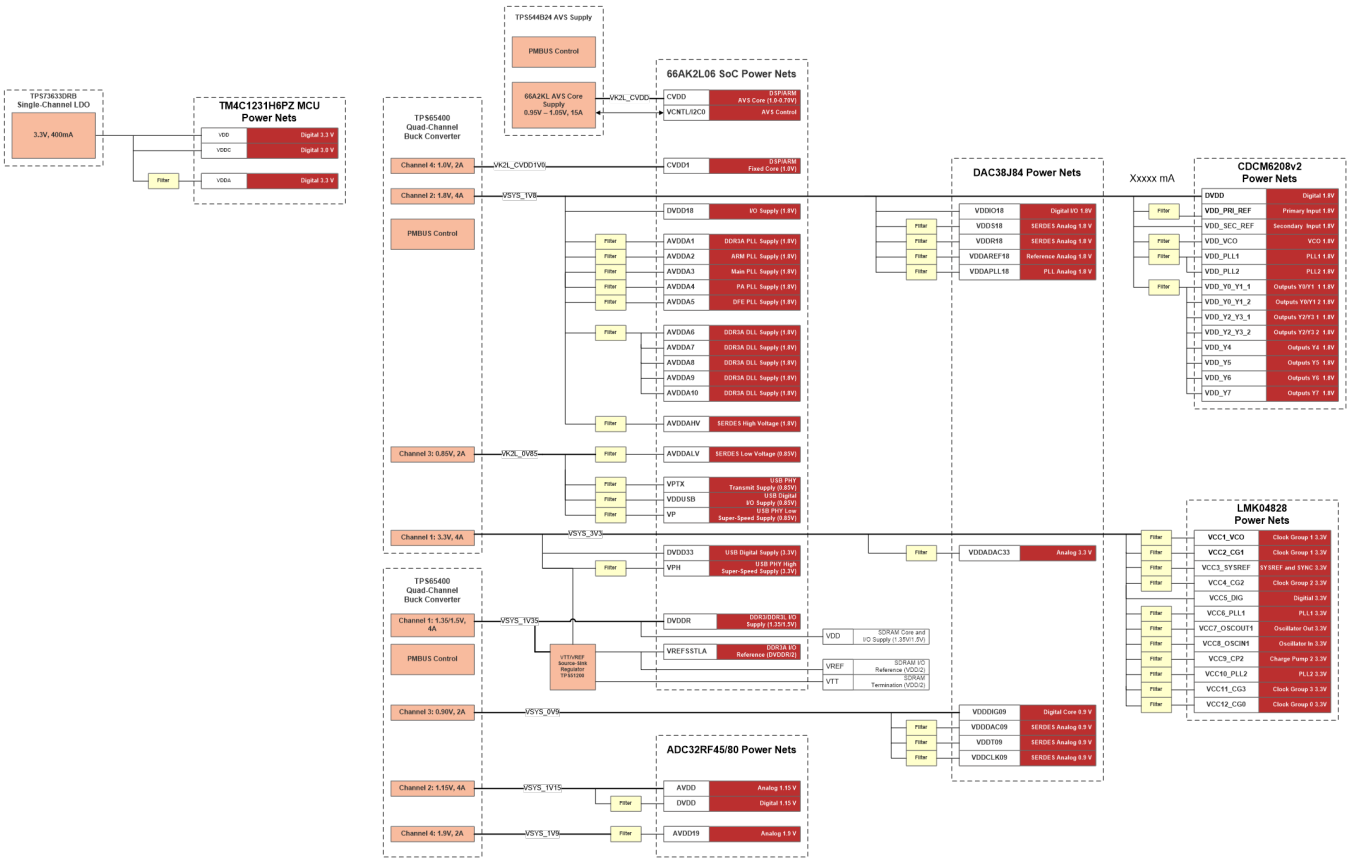

Figure 14. 66AK2L06, ADC32RF45 and DAC38J84 System Power Distribution Block Diagram

- TPS544B24 buck converter
  - Used to generate the high-current, high-transient CVDD Smart-Reflex (AVS) power net for the K2L SoC
- Used to generate the high-current, high-transient CVDD Smart-Reflex (AVS) power net for the K2L SoC
  - Channel 1: System 3.3 V
  - Channel 2: System 1.8 V
  - Channel 3: K2L 0.850 V
  - Channel 4: K2L 1.0 V
- TPS65400 Quad Buck Converter #2
  - Channel 1: K2L and SDRAM 1.35 V
  - Channel 2: System 1.15 V
  - Channel 3: System 0.9 V
  - Channel 4: System 1.9 V
- TPS54620 Buck Converter #1
  - Used to generate an auxiliary, “always-on” 3.3V domain for any board management controller, like the proposed TM4C1231 MCU
- TPS54620 Buck Converter #2
  - Used to generate a 5.0V USB3.0 VBUS power net
- TPS51200 Push-Pull Converter
  - Used to generate both the VTT termination and SSTL I/O VREF power nets for the K2L DDR3 controller and the SDRAM DDR3 array

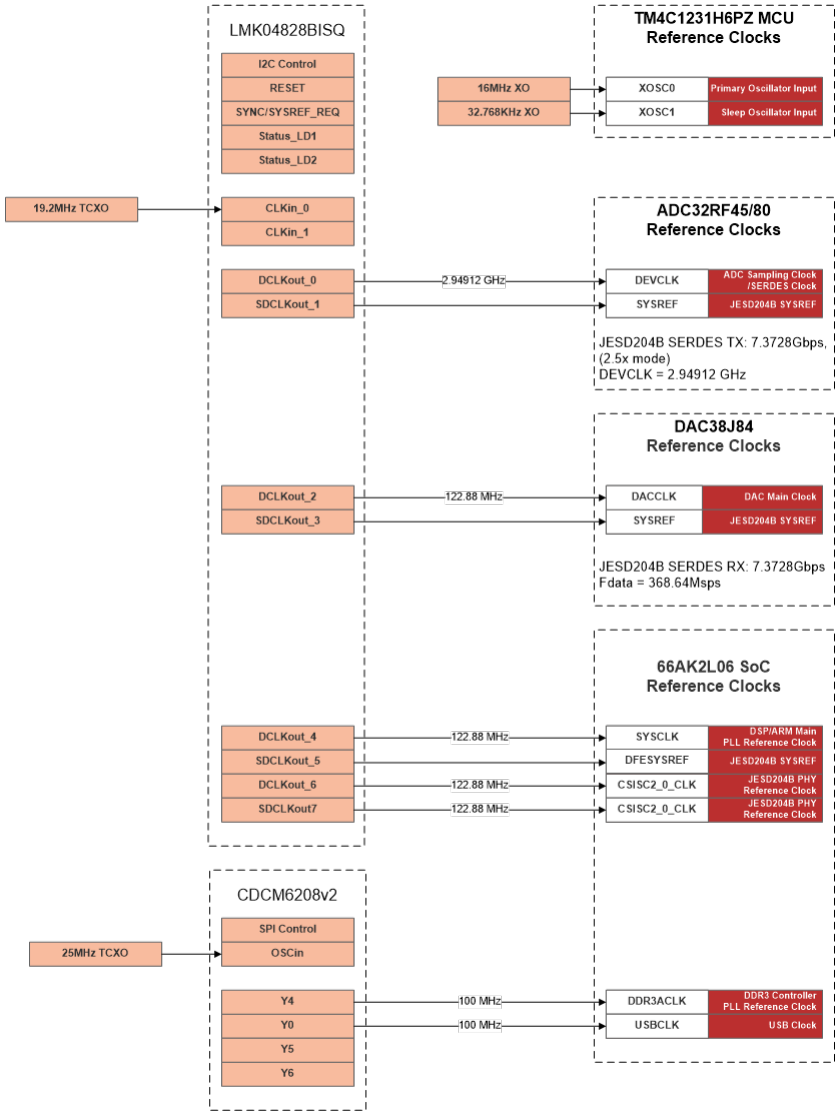

Figure 15. 66AK2L06, ADC32RF45 and DAC38J84 System Clock Distribution Block Diagram

4.4 System Debug and Test

Throughout the schematics, numerous oscilloscope probe test-points (reference designator K*) have been added to areas which have been shown to be key points of interest in past hardware bring-up efforts. Not all signals of interest can be probed due to the impact the test point might have on signal integrity. However, it is recommended that the test points shown in this schematic be added to any hardware to accelerate hardware debug and test.

In addition to the various probe points, the K2L, ADC32RF45 and DAC38J84 JESD204B high-speed serial transmitters and receivers also include pattern generator and verifier functions which allow system designers to check signal integrity of these channels in hardware. The K2L PDK released as part of the Processors SDK includes example programs which show how to utilize the pattern generator, pattern verifier, bit error rate (BER) and on-die eye-scan functionality of the K2L JESD transmitters and receivers.

4.5 Clock Distribution

The LMK04828 JESD204B clock synthesizer is utilized to provide the device clock and periodic SYSREF pulses for the 66AK2L06 and ADC14X250 devices. The LMK04828 is also utilized to provide the SERDES reference clocks for the 66AK2L06. The LMK04828 dual PLL architecture and high output frequency limit allows, along with programmable SYSREF and delayed reference clocks allows this single device to provide a low-jitter, deterministic reference clock source to all data acquisition and processing elements, SERDES transmitters, receivers and baseband processing elements within this JESD204B system.

A CDCM6208 low-jitter PLL is also included in the design to DDR3 and USB reference clocks. This reference design only makes use of two of the eight available low-jitter reference clock outputs of the CDCM6208. It is recommended that the PCIe and SGMII reference clocks also utilize this low-jitter clock source in systems where those peripherals are also required.

4.6 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0081.

4.7 PCB Layout Recommendations

Any additional note you think the customer would need to layout this board; also add details on the reasoning behind your layout (form factor, heat distribution, and so forth).

- See the 66AK2L06 JESD204B specific section in the Serializer/Deserializer (SerDes) for KeyStone II Devices User's Guide.
- See the 66AK2L06 JESD204B specific section in the Hardware Design Guide for KeyStone II Devices.
- See the layout section of the LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs Data Sheet .

4.7.1 Layout Prints

To download the layer plots, see the design files at TIDEP0081.

5 Software Files

To download the software files, see the design files at TIDEP0081.

- The MCSDK can be downloaded from bioslinuxmcsdk.
- The RFSDK software can be requested through MySecureSoftware at: http://www.ti.com/tool/rfsdk.

6 References

1. *KeyStone II Architecture Serializer/Deserializer (SerDes) User's Guide* (SPRUHO3)
2. *Hardware Design Guide for KeyStone II Devices* (SPRABV0)
3. *DAC3xJ84 Quad-Channel, 16-Bit, 1.6/2.5 GSPS, Digital-to-Analog Converters with 12.5 Gbps JESD204B Interface Data Sheet* (SLASE17)
4. *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs Data Sheet* (SNAS605)
5. *ADC32RF80 Dual-Channel, 14-Bit, 3.0-GSPS, RF Sampling Wideband Receiver and Feedback IC Data Sheet* (SBAS774)

7 About the Author

MICHELLE LIU is a senior applications engineer in TI's Embedded Processing organization. She has worked at TI since 2009. She has been working on digital front end of remote radio head and system integration in wireless communications. She also worked on software development of TCI6630K2L SOC small cell application. Her recent roles focus on developing solutions based on interfacing the 66AK2L06 SOC to JESD204B High Speed Data Converters.

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