All testing performed with a 48V input, 3A load and 20MHz bandwidth unless otherwise noted.

**Efficiency**

![Efficiency Graph]

<table>
<thead>
<tr>
<th>Iout</th>
<th>Vout</th>
<th>Vin</th>
<th>J3</th>
<th>Conv</th>
<th>Conv</th>
<th>PoE</th>
<th>PoE</th>
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<th>Eff</th>
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<td>24.14</td>
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<td>47.66</td>
<td>0.0%</td>
<td>48.00</td>
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<td>47.57</td>
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<td>48.00</td>
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<td>0.336</td>
<td>74.8%</td>
<td>47.53</td>
<td>75.6%</td>
<td>48.00</td>
<td>0.330</td>
<td>76.2%</td>
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<td>0.75</td>
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<td>48.00</td>
<td>0.465</td>
<td>81.1%</td>
<td>47.51</td>
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<td>48.00</td>
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<td>47.32</td>
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</tbody>
</table>
Ripple and Noise

Output Ripple (J13), 50mV/div, 2usec/div
Measured 97mVpp:

Input Ripple (C68), 10mV/div, 2usec/div
Measured 15.3mVpp:

Dynamic Loading

Output response to load step
1.5A to 3.0A load step
1V/div, 1A/div, 500usec/div
Slew Rate = 300mA/usec
Measured 2.5Vpp across J13:
**Turn On Response**

3.0A load, 5V/div, 5msec/div

0A load, 5V/div, 5msec/div

**Waveforms**

Drain to source, Q16, 38V input, 3.0A load
20V/div, 2usec/div, 750MHz bandwidth
Measured 126.7V peak:
Drain to source, Q13, 38V input, 3.0A load
20V/div, 2usec/div, 750MHz bandwidth
Measured 90.0V peak:

Drain to source, Q15, 57V input, 3.0A load
20V/div, 2usec/div, 750MHz bandwidth
Measured 94.0V peak:

Drain to source, Q16, 48V input, 3.0A load
20V/div, 2usec/div, 750MHz bandwidth
Measured 113.3V peak:
Drain to source, Q13, 48V input, 3.0A load
20V/div, 2usec/div, 750MHz bandwidth
Measured 64.0V peak:

Drain to source, Q15, 48V input, 3.0A load
20V/div, 2usec/div, 750MHz bandwidth
Measured 76.0V peak:

Loop Stability

Bandwidth= 4.2 kHz  Phase Margin=59 degrees  Gain Margin=18dB
Thermal Plot

Top:

Bottom:
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