Direct RF conversion: From vision to reality

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An emerging class of high-performance RF-sampling data converters sets out to finally deliver on the promise of true software-defined radio (SDR).

Receiver system designers are seeing a change from the widely adopted heterodyne architecture to a direct RF-sampling approach. In the traditional receiver, the designer selects the analog-to-digital converter (ADC) based on key specifications, such as signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). In a direct RF-sampling receiver, designers focus instead on how the RF ADC impacts the receiver system noise figure (NF). A key concern is its performance in a blocking environment for which the heterodyne architecture has been optimized for many years.

This paper explains the differences between a traditional heterodyne receiver and the modern RF-sampling data converter. It then compares some key design aspects, particularly for the complete signal chain line-up.

In a direct RF-sampling architecture, the data converter digitizes a large chunk of frequency spectrum directly at RF and hands it off to a signal processor to dissect the available information. This is a paradigm shift that takes what has traditionally been handled by analog processing (mixers, local oscillators and their attendant filters and amplifiers) into the digital domain.

A new class of direct RF-sampling ADCs is being designed in advanced CMOS processes that allow much higher conversion rates with lower power than some previous generations. Furthermore, this design approach also enables more digital integration, which is used for a low-power, multi-gigabit serial interface and on-chip digital-down conversion (DDC). Combined, they make for a very size- and power-efficient digital interconnect between the data converter and digital processor.

Receiver chain components

In a heterodyne receiver, the input signal, which resides at an RF frequency, is down-converted to a lower intermediate frequency (IF). It is then digitized prior to digital filtering and demodulation. Depending on the application, the input signal can range from ~700 MHz to several GHz, while IF typically ranges from about zero to 500 MHz.

Figure 1 shows a classic heterodyne receiver block diagram. It consists of bandpass filters (BPFs), a low-noise amplifier (LNA), mixer and local oscillator (LO), an IF amplifier, and ADC anti-aliasing filter (AAF). In a direct-conversion receiver, the RF-sampling ADC replaces the signal chain from the mixer, which greatly simplifies the overall receiver design.

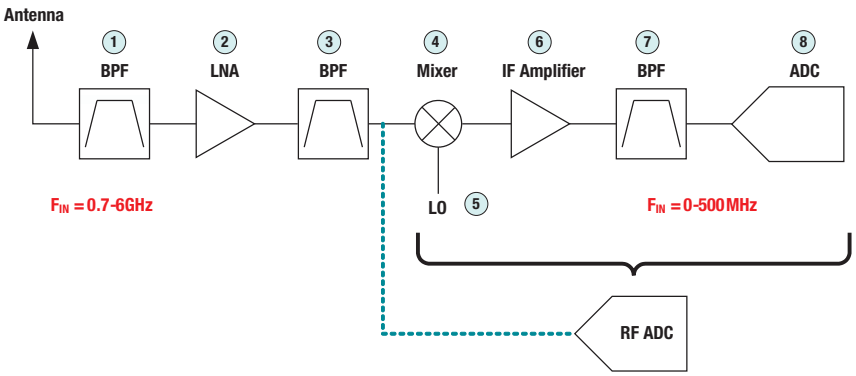

Figure 1. Traditional heterodyne architecture versus an RF-sampling ADC

1. First bandpass filter

   The first RF BPF is typically a wideband, low-loss, pre-select filter, providing most of the out-of-band rejection. It prevents signals that are far from the actual passband from saturating the analog front end (AFE).

2. Low-noise amplifier

   This front-end RF amplifier increases the amplitude of weak signals. The lower its noise figure, the less it degrades the overall noise figure of the receiver based on the cascaded noise figure equation.

3. Second bandpass filter

   The second RF filter is a narrow-band filter prior to the mixer – typically a surface acoustic wave (SAW) type. It suppresses nearby out-of-band interferers at the mixer image locations (m*LO ±n*RF) that would fall into the IF passband.

4. Mixer

   The mixer translates the RF signal to IF frequencies. The RF and LO signals mix to produce a difference frequency known as IF frequency (fIF = |fRF – fLO|). Undesired spurs and images (for example, a half IF) need to be filtered out either before or after the mixer stage. It also can be used to convert the single-ended input signal to a differential signal for the ADC.

5. Local oscillator

   The LO is tuned to the desired frequency spacing above or below the RF signal and is injected into the mixer. In a direct RF-sampling system, the LO essentially turns into the ADC's sampling clock. However, similar to the IF-sampling converter, the RF ADC clock also requires very good phase noise.

6. Intermediate frequency amplifier

   The IF amplifier adds gain to the input signal by reducing the ADC's impact to the receiver noise figure.

   Additionally, it compensates for the bandpass filter's gain loss (attenuation). It can also be used as a buffer to drive the ADC's capacitive load. In many cases, this stage has multiple gain steps that are digitally controlled to provide an automated gain control loop, which enhances the system's dynamic range.

7. Anti-aliasing filter

   The AAF limits noise and distortion contribution from the IF amplifier. More importantly, however, it filters the ADC's alias bands. This filter may need a sharp rolloff. The implementation is more feasible at IF than RF because the ratio of alias frequency to the desired signal is larger. Thus, aliasing frequencies are further away from the filter cut-off frequency.

8. Analog-to-digital converter

   The ADC digitizes the input signal. It needs a fast sampling rate to allow room for filter rolloffs – typically at least three to five times the signal bandwidth. Its SNR needs to be good to ensure minimal impact on the receiver noise figure. SFDR also needs to be sufficient so that spurs caused by in-band and out-of-band interferers do not dominate the noise budget.

System design considerations

When evaluating a transition from an IF-sampling-based to a direct-RF-sampling-based receiver design, one must examine the overall impact to the receiver sensitivity, as well as performance in a blocking condition. Since the RF-sampling ADC replaces the signal chain from the mixer onward, the comparisons provided are focused at the mixer input, assuming the same analog front end for both designs. The parameters also can be calculated for the antenna input for a given LNA in the same fashion using the respective gains and losses of the amplifier and filters.

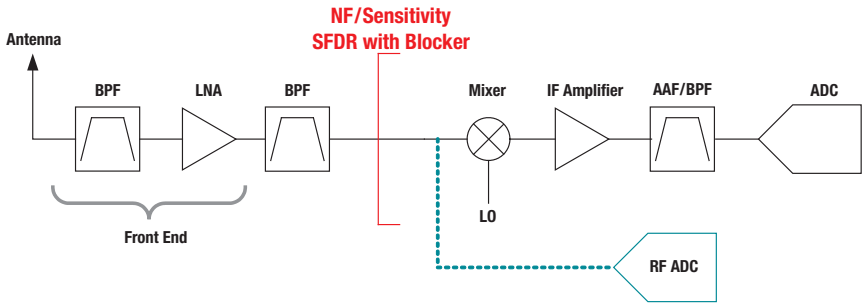

Figure 2. Performance comparison between heterodyne and direct RF-sampling receivers

Receiver sensitivity

Receiver sensitivity is a measure of how well it can recover and process very small input signals. Weak input signals cannot be demodulated if the receiver noise within the demodulated bandwidth is larger than the received signal itself. Oftentimes the transmitter and receiver are completely independent. Thus, raising the desired signal amplitude above the noise floor is not always possible (for example, a radar receiver). The only option to improve receiver sensitivity is to reduce its noise floor or, in other words, improve its noise figure.

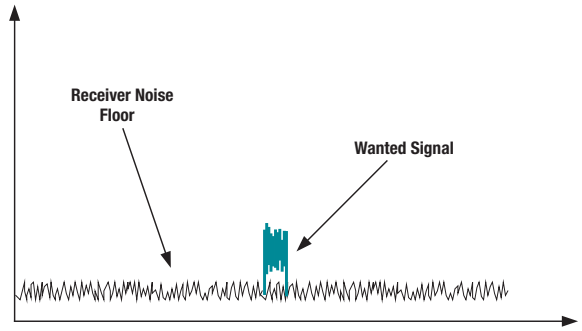

Figure 3. Small wanted signal in sensitivity case

The cascaded noise figure at the input of the mixer can be calculated, as shown in ***Figure 4*** and equations (1-2):

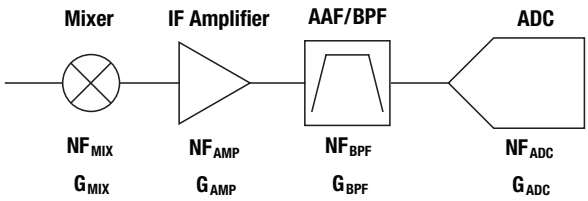

Figure 4. Cascaded signal chain line up

Noise figure (linear)

$$F = F_{MIX} + \frac{F_{AMP}-1}{G_{MIX}} + \frac{F_{BPF}-1}{G_{MIX}\cdot G_{AMP}} + \frac{F_{ADC}-1}{G_{MIX}\cdot G_{AMP}\cdot G_{BPF}} \quad (1)$$

Using

$$F = 10^{\frac{NF[dB]}{10}} \quad (2)$$

$$G = 10^{\frac{G[dB]}{10}}$$

The noise figure (dB) then calculates to

$$NF = 10\cdot\log(F) \quad (3)$$

Calculating the ADC's noise figure is a little more involved:

$$NF_{ADC} = P_{FULLSCAE}[dBm] - kTB - NSD_{ADC} =$$

$$P_{FULLSCAE}[dBm] + 174dBm - SNR_{ADC} - 10\cdot\log\left(\frac{FS}{2}\right)$$

$$P_{FULLSCAE}[dBm] = 10\cdot\log\left(1000\cdot\frac{(Vpp)^2}{8\cdot Z_{IN}}\right) \quad (4)$$

Using these formulas, the equivalent noise figure can be calculated for modern day IF-sampling and RF-sampling ADCs. Examples include the ADS4149 and ADC12J4000, respectively.

Parameter	IF-sampling ADC ADS4149	RF-sampling ADC ADC12J4000
Sampling rate (FS)	250 MSPS	4 GSPS
Input fullscale (Vpp)	2 Vpp	0.8 Vpp
Signal-to-noise ratio	71.9 dB	55 dB
Input impedance (Z_{IN})	200 Ω (external)	100 Ω (internal)
Calculated noise figure	25.1 dB	25 dB

On paper, the noise figures for both ADCs are nearly identical. However, the IF-sampling-based approach has additional gain from the mixer and the IF amplifier (minus the loss of the BPF), which substantially reduces the impact of the ADC noise figure to the receiver sensitivity. Therefore, the RF-sampling ADC requires additional front-end gain (additional LNA) that is approximately equivalent to $G_{MIX} + G_{AMP} + G_{BPF}$. This should achieve a total noise figure that is similar to the IF ADC-based option.

Blocker environment

In the sensitivity condition, the receiver operates at maximum gain. In the presence of a strong blocker/interferer, the gain needs to be reduced in order to avoid saturation of the input (desensitization). Therefore, the receiver noise figure will be much larger, which impacts the minimum signal that can be recovered in a blocking condition.

In addition to the impact on the noise figure, the interferer itself can generate several different noise impairments that can overlap with the wanted signal. This interferer needs to be considered when doing the noise budget analysis and designing the overall filter profile (***Figure 5***).

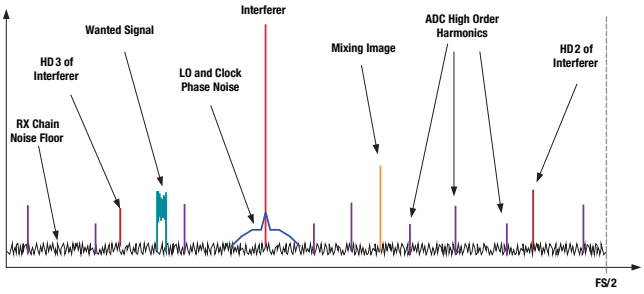

Figure 5. Different noise impairments due to interferer (illustrated with single-tone interferer)

Mixer

The images from the mixer at m*LO ±n* RF can fall into a band of interest that requires adequate filtering at RF. This ensures that an out-of-band blocker at the image locations does not generate a mixing product in-band. Furthermore, the phase noise of the LO itself also gets mixed with the RF signal (interferer). This increases the noise power with in-band blockers, increasing the amount of noise leaking from the blocker into the wanted carrier bandwidth.

Amplifier

The IF gain amplifier generates HD2 and HD3 products from the strong interferer, which can fall in-band of the signal band of interest. Typically, these low-order harmonics are either frequency planned out by choosing an appropriate IF frequency, or attenuated by the following bandpass filter.

Analog-to-digital converter

Several impairments come from the data converter:

- Similar to the IF amplifier, the ADC generates strong low-order harmonics (HD2 and HD3) from the blocker. The IF frequency can be chosen so that these harmonics alias out-of-band for an in-band blocker. For an out-of-band blocker, adequate external filtering should be provided.
- High-order harmonics set a spur floor that cannot be planned around and needs to be taken into consideration.
- The phase noise of the sampling clock (jitter) also mixes with the interferer. It scales with 20*log(FS/F_{IN}), so the higher the input frequency range (IF) with a fixed ADC sampling rate, the larger its impact on the noise budget.
- The RF-sampling ADC may achieve its fast clock rate using interleaving techniques. In this case, the interleaving spurs need to be considered for the noise analysis with in-band blockers, but also for the filter design for out-of-band interferers.

Filter design analysis

IF sampling solution

As can be seen from the previous section, the out-of-band blocker scenario requires well-thought-out filtering. The following example further illustrates this:

A 250-MSPS ADC digitizes a 60-MHz wideband filter located at 2.3 GHz. Next, a mixer with a 2112.5-MHz LO down converts the band to a high IF of 187.5 MHz.

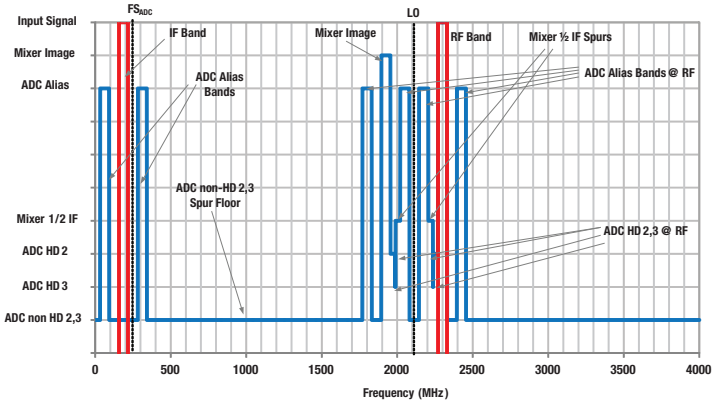

Figure 6. Filter mask showing frequency band locations from different impairment sources – heterodyne receiver

The actual amount of filter attenuation needed depends on out-of-band blocker power, as well as the mixer's spur level performance, IF amplifier and ADC. However, spur locations can be calculated regardless of power levels.

The RF band centered at 2.3 GHz is down-converted to a high IF of 187.5 MHz (centered in the middle of the ADC Nyquist zone).

It is important to design the combined IF+RF filter response to provide sufficient attenuation at the mixer image and alias locations. This is because any out-of-band blocker at these frequencies directly falls into the IF band location. It is difficult to design a RF filter with very sharp rolloff for very close-in images and alias band locations. Therefore, the filter attenuation can be split between the RF and IF bandpass filter.

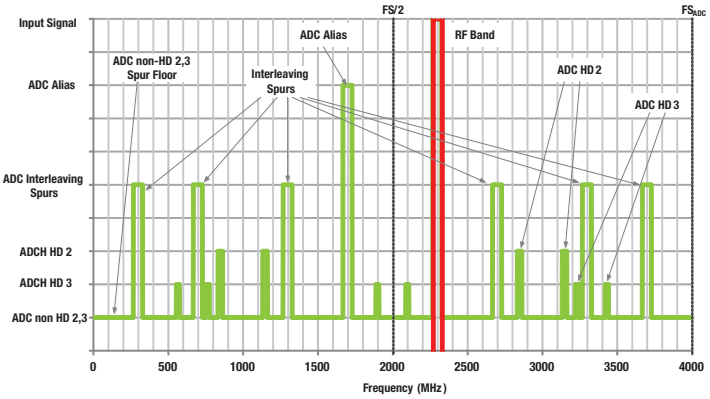

Figure 7. Filter mask shows frequency band location from different impairment sources, such as a direct RF-sampling receiver

Additionally, the out-of-band blocker (after down-conversion) also generates an HD2 and HD3 component that can fall in-band. These interferer HD2,3 alias locations also require filter attenuation, commonly at IF, as they are fairly close to the IF band of interest.

Since the mixer image and ADC alias are down-converted without any attenuation by the mixer and ADC, the external filters need to provide all the attenuation to meet the SFDR requirement. On the other hand, the ADC and mixer also create harmonics and spurs with some attenuation, thus, requiring less external filter attenuation. This is illustrated in ***Figure 6***. The mixer image and ADC alias bars are larger (requiring larger attenuation), while the bars of the ADC and mixer spurs are smaller (requiring less attenuation).

Direct RF-sampling solution

Overall filter mask requirements change with direct-RF-sampling. Since no mixer is involved, there are no mixing images to worry about, nor LO spurs. Furthermore, the RF ADC typically operates at a much faster sampling rate than the IF-sampling ADC. Thus, the ADC alias frequency bands can be spaced much further away from the RF band of interest with proper sampling frequency choice. However, flexibility in RF-ADC clock frequency may not always be available.

When designing the filter mask for the direct RF-sampling receiver, the following components should be considered.

ADC alias

Every ADC has alias frequency bands in the adjacent Nyquist zones. The interferer in the alias band folds directly into the band of interest during the sampling instant. The ADC sampling rate should be chosen to ensure there is enough space at the edge of the Nyquist zone to allow for filter rolloff (similar to IF-sampling ADCs).

Interleaving spurs

Most RF-sampling ADCs are interleaved to achieve a fast sampling rate – the ADC12J4000 is interleaved four times, producing three interleaving spurs (FS/2 - F_{IN}, FS/4 ± F_{IN}). The interleaving spur performance of modern RF-sampling ADCs meets the requirements of many applications already, and no special filtering may be required.

As the RF bands are increasing in bandwidth, the interleaving spur bands increase by the same amount as well. This quickly closes the gap in between. Hence, frequency planning around the interleaving spurs for a specific input frequency range may require more flexibility on the sampling clock frequency.

ADC HD2,3

Out-of-band blockers get sampled by the ADC and create HD2 and HD3 spurs during the sampling instant. These spurs can then fall into the wanted RF band or one of its aliases, thus, requiring filtering. The HD2 and HD3 markers in ***Figure 7*** indicate the frequency location of such an out-of-band blocker whose HD2 and HD3 alias into the wanted RF band.

ADC non-HD2,3

Based on the maximum out-of-band blocker power, the high-order harmonic spurious performance of the RF ADC determines the minimum broadband filter mask.

Similar to the heterodyne receiver, the ADC alias bands require the full amount of filter rejection. This is because a blocker in that band directly falls on top of the wanted band during the sampling process. Meanwhile, the remaining ADC spurious products all have inherent attenuation, which require far less attenuation (***Figure 7***).

Filter comparison

The filter masks for IF- and RF-sampling-based signal chains can be superimposed to observe the differences. At first glance, the close-in filter design for the RF-sampling receiver appears more relaxed, as there are fewer critical spur locations close by and fewer bands requiring the full filter rejection amount. However, a flexible RF-ADC-sampling clock frequency is necessary when the RF band approaches the edge of the Nyquist zone or the interleaving spur locations.

Alternatively, the heterodyne receiver requires more stop-band attenuation close to the band of interest. Now the attenuation can be weighted towards the anti-alias bandpass filter for the IF frequencies.

In-band blocker

The receiver performance in the presence of a strong, in-band interferer is independent of the filter mask, but is primarily limited by the active receiver components (mixer, IF amplifier and ADC). With some frequency planning, the low-order harmonics HD2, HD3, and even the interleaving spurs, may be avoided. However, the spur floor from the higher order harmonics will always be present.

Some systems – like multi-carrier (MC) GSM that have very strong, narrowband blocker requirements and demand 16-bit, IF-sampling ADCs with typical

Parameter	IF-sampling ADC ADS4149	RF-sampling ADC ADC12J4000
Sampling rate (FS)	250 MSPS	4 GSPS
HD2 (typ)	84 dBc (@ F_{IN} = 170 MHz)	79 dBc (@ F_{IN} = 2400 MHz)
HD3 (typ)	82 dBc (@ F_{IN} = 170 MHz)	76 dBc (@ F_{IN} = 2400 MHz)
Interleaving spur (typ)	n/a	57 dBc (@ F_{IN} = 2400 MHz)
Non-HD2, 3 (typ)	88 dBc (@ F_{IN} = 170 MHz)	75 dBc (@ F_{IN} = 2400 MHz)

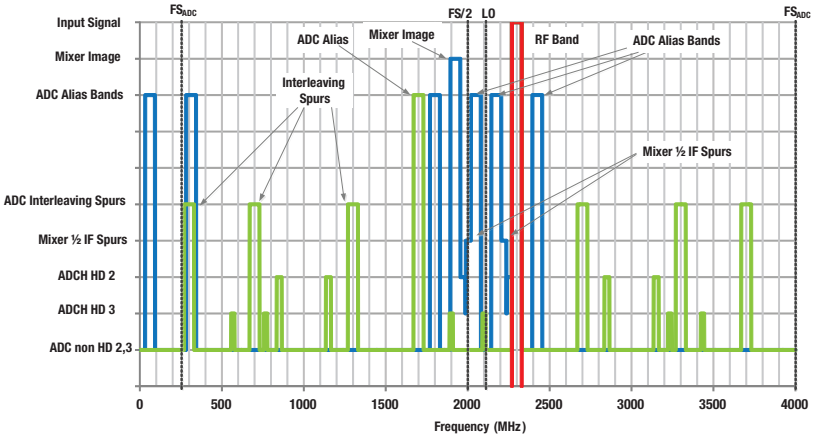

Figure 8. Filter mask comparison between heterodyne and direct RF-sampling receiver

non-HD2,3 spur levels of 100 dB – are still out of reach for current-generation RF ADCs. However, some wideband systems, such as LTE, are becoming feasible.

Summary

Most system designers are eager to examine the viability of RF sampling-based systems to meet the ongoing demand for smaller radio form factors. RF-sampling ADCs provide a higher level of integration, because they reduce both active signal chain components and supporting elements, such as different power rails and control signals.

As the communications industry moves towards multi-band radios, the direct RF-sampling architecture is gaining even more support, because it enables the transition from one heterodyne receiver per band to one RF-sampling ADC per radio.

Furthermore, the power-efficient, on-chip decimation filters of GSPS RF-sampling ADCs make the digital output interface look more like that of the IF-sampling data converter – and are no longer a barrier for multi-channel receivers. Plus, the external filter requirement for RF-sampling ADCs doesn't appear to be tougher than those for IF-sampling-based systems.

Advanced CMOS direct-RF-sampling ADCs, like the ADC12J4000, are being adopted in a wide range of designs and applications. This is because they reduce the overall receiver signal chain while the fast sampling rate gives plenty of space for frequency planning. Additionally, the technology enables very wide-bandwidth signals to be captured directly at RF.

Texas Instruments is continuing to push the limits of technology with our next generation of RF-sampling ADCs, which will deliver enhanced AC performance, among other advancements. These products will enable the direct RF-sampling architecture to finally deliver on the promise of software-defined radio and become the preferred approach of radio designers.

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