Accounting for delay from multiple sources in delta-sigma ADCs

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Delta-sigma ADCs introduce delays into the signal chain, but all of the delays can be calculated with reasonable accuracy – allowing system designers to account for them in time-sensitive applications.

In time-sensitive applications, such as grid infrastructure electronic systems where measurement of grid voltages and currents may need to be timestamped with significant temporal accuracy, it is important to characterize the sources of delay in the signal chain. A delta-sigma ADC creates a calculable time delay between the analog input signal and digital output. This paper discusses these sources of delay in depth.

The delta-sigma ADC employs oversampling as a means to reduce noise in the band of interest. In the process of doing so the data is effectively filtered, introducing a linear phase response. This phase response of the digital filter is responsible for most of the delay in delta-sigma data converters.

Additionally, many delta-sigma ADCs integrate a programmable-gain amplifier (PGA) to drive the inputs of the delta-sigma modulator. Like all amplifiers, these PGAs have a phase response which is characterized by delay between input and output. However, I will prove that the delay introduced by the PGA is negligible for the input frequencies of interest.

Finally, some delta-sigma ADCs feature a variety of digital signal-processing and system-monitoring functions, which also may delay the output. To address this concern, I will also discuss the common features and associated timing.

Typical functional blocks in delta-sigma ADCs

A basic delta-sigma ADC requires a delta-sigma modulator to digitize analog input signals, a digital decimation filter to suppress high-frequency noise, and an interface to transmit data to the host.

It is common for a delta-sigma ADC to have integrated features beyond a delta-sigma modulator, digital filter, and digital interface. For example, many delta-sigma ADCs have an integrated amplifier front-end to drive the input sampling structure and provide gain. This block introduces an analog phase shift to the entire system, which manifests as a delay. The device may also perform digital logic functions unrelated to filtering with each output sample as part of the interface or as part of some other device feature. This logic also may delay signal output.

Typical delta-sigma ADC functional blocks are shown in **Figure 1**. Each block may or may not introduce delay into the system.

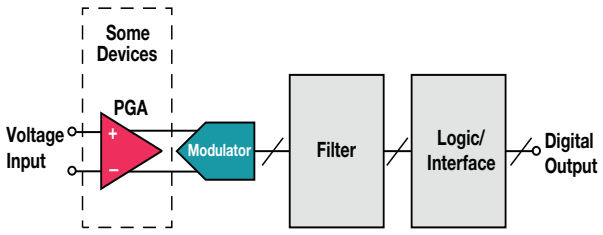

Figure 1: *Typical functional blocks of a delta-sigma ADC.*

Sources of delay in a delta-sigma ADC

Programmable gain amplifier (PGA)

The purpose of the programmable gain amplifier in a delta-sigma ADC is threefold:

1. Drive the inputs of the delta-sigma modulator
2. Provide analog gain to better utilize the full-scale range of the data converter
3. Provide anti-aliasing (in some cases)

As with all amplifiers, the PGA in a delta-sigma ADC is described by a transfer function which determines, among other things, the amount of phase shift between input and output signals for a given frequency. The definition of phase response is illustrated in **Equation 1**.

$$\phi(\omega) \equiv arg\{H(\omega)\} \quad (1)$$

where $H(\omega)$ is the transfer function of the PGA and ω is the angular frequency $2\pi f$

A phase shift between the input and output can be thought of as a time delay. The amount of time delay for a given frequency can be found to be the frequency derivative of the phase response. The definition of PGA delay is shown in **Equation 2**.

$$Delay(\omega) \equiv -\frac{d\phi(\omega)}{d\omega} \quad (2)$$

The negative sign appears in the definition to indicate that a negative change in phase shift corresponds to a positive time delay.

As mentioned, one of the functions of the PGA is to band limit input signals to reduce aliasing. In order to place a pole at a low enough frequency to attenuate out-of-band signals significantly, a strategy known as "pole splitting" is used. This is performed by placing a compensation capacitor, C_C, in the amplifier's feedback loop. The result is that the first pole of the amplifier appears at a much lower frequency than the higher order poles.

The –3 dB frequency corresponding to the first pole of the amplifier is found according to **Equation 3**.

$$\omega_{C1} = \frac{\beta g_m}{C_C} \quad (3)$$

where β is the feedback factor of the PGA, which is the inverse of its amplifier's DC gain; and g_m is the small signal transconductance of the input differential transistor pair. For simplicity, only MOSFET architectures are discussed in this paper.

Since the first pole is at a much lower frequency than all the others, the frequency response resembles that of an RC low-pass filter where the cutoff frequency is ω_{C1}. **Equation 4** shows the calculation of delay for the single-pole model of the PGA.

$$Delay(\omega) = \frac{\omega_{C1}}{\omega_{C1}^2 + \omega^2} \quad (4)$$

It is clear from this calculation that delay for the amplifier is not constant across frequency. Further, the bandwidth of the amplifier is subject to tolerance due to temperature and process variations. This variability may be disconcerting, but a few key observations show this to be relatively insignificant.

First, consider the delta-sigma ADC as a system. Once the data is sampled using a delta-sigma ADC, it will be digitally filtered and decimated to the output data rate. Therefore, a relevant discussion of the PGA frequency response can be limited to the Nyquist bandwidth, which is half of the user-configured output rate.

Second, if the delay in the band of interest is small with small variation, then delay from the PGA can be either ignored or accounted for by a simple approximation. We consider the "worst case" PGA-induced delay variation to be exhibited when the gain of the PGA is the highest (or lowest bandwidth) and the data rate to be the highest such that the largest possible change in delay is observed.

For example, consider the PGA in the ADS131E08, a delta-sigma ADC optimized for grid infrastructure applications which tend to have strict timing requirements. The highest possible gain in that device is 12, with an according amplifier bandwidth of f_C=32 kHz. The largest data rate is 64 kSPS, which results in a Nyquist bandwidth of 32 kHz. **Figure 2** shows a delay versus frequency for a PGA gain of 12 (worst case). **Equation 4** is plotted using $\omega_C = 2\pi f_C = 64 \times 10^3\ \pi$ rad/s. At DC, $\omega = 0$, the delay 4.97 µs. At $\omega = 2\pi f_{Nyquist} = 64 \times 10^3\ \pi$ rad/s, the delay is 2.49 µs. To put these times into perspective, it is helpful to know the delay caused by the digital decimation filter for the 64 kSPS rate is nearly 22 µs. Delay from the digital filter will be discussed in an upcoming section.

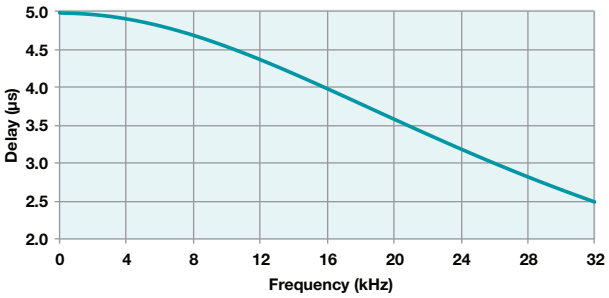

Figure 2: *Delay versus frequency for PGA gain of 12 (worst case).*

From this analysis we can expect the settings where the PGA's contribution to total delay is minimized to be when the amplifier bandwidth is at its widest (lowest gain) and the data rate to be at its slowest. In the best case for the ADS131E08 PGA (gain of 1, data rate of 1 kSPS), the largest PGA delay is 672 ns where the digital filter delay for that data rate is nearly 1.5 ms.

There are special implications from PGA-induced phase shift for simultaneous sampling multi-channel ADCs. If all PGA gains are the same from channel-to-channel, total delay from input to output is the same. However, if different PGA gains are used for different channels, then the delays between channels would be different even though data is output to the user at the same time for all channels. Still, because the delay from the PGA is usually small relative to the group delay of the digital filter, this channel-to-channel difference does not present a major challenge to design. Digital filter group delay is the same from channel-to-channel since the data rate is the same from channel-to-channel.

Since PGA bandwidth depends on the tolerance of analog circuit elements, delay exhibits a relationship with temperature. As temperature increases, the amplifier bandwidth decreases, thus, the delay increases. For example, if a PGA is configured to have a gain of 12, it is reasonable to expect a 15 percent decrease in bandwidth at very high temperature. This increases delay in the PGA from its nominal DC value of 4.49 µs to 5.85 µs at high temperature.

Delta-sigma modulator

The delta-sigma modulator is the electronic functional block in a delta-sigma ADC that does the work of taking an analog waveform and converting it to a bitstream. For our purposes, functionality can be divided into two steps. The first is to sample the input signal with a "sample-and-hold" circuit using a network of switches and capacitors. The second is to convert the sampled voltage.

The sample-and-hold circuitry is best thought of as a resistor-capacitor (RC) network with a very high bandwidth. The high bandwidth is necessary because the input voltage must reach steady state by the time sampling takes place. In the case of ADCs with integrated input drive amplifiers, the RC time constant at the input can be approximated out of calculations because it is likely that the designer built the amplifier to charge the sample-and-hold circuit very quickly.

Even in systems with no integrated drive amplifier, it is likely that the sampling circuit will charge very fast to meet the sampling timing requirement. It is then the

role of the system designer to choose a drive amplifier with a bandwidth that can meet the demands of the sampling circuit. In the interest of simplicity, no mathematical proof will be given as to the timing specification of the sampling circuit.

The modulator may come in several different forms with varying amounts of delay from input to output. In general, the delta-sigma modulator architectures will be closely guarded industry secrets, but some general statements can be made. First of all, any delay between the sample-and-hold circuit and the bitstream output will never be larger than a few modulator clock cycles. A delay of a few modulator clock cycles is significantly smaller than the group delay of the integrated digital decimation filter.

For some architectures such as the one used in the ADS131E08, there is essentially no delay. This can be thought of as a one modulator clock cycle delay from when the voltage is sampled by the sample-and-hold circuitry to when the corresponding bit(s) are output to the digital filter.

Digital decimation filter

Discrete systems are not immune to frequency-dependent delay. Linear time-invariant (LTI) systems exhibit delay associated with their phase response. Group delay is defined as the number of samples in delay as a function of frequency. The mathematical definition is:

$$Group\ delay\ (\omega) \equiv -\frac{d\phi\,(\omega)}{d\omega} \qquad (5)$$

where $\phi\,(\omega)$ the phase response of the system, and ω is the angular frequency measured in radians per sample.

The minus sign in front of the expression on the right indicates that negative changes in the phase angle correspond to positive group delays.

For delta-sigma ADCs, decimation is used as a method to increase accuracy through weighted averaging. The output from the digital decimation filter of a delta-sigma ADC will be the weighted average of a number of points specified by the data converter's oversampling ratio (OSR). The result is a low-pass filter with a sinc ($\sin x/x$) function response in the frequency domain. (Some ADCs have an additional filter stage to flatten the passband, but for simplicity those filters are not discussed here.) Many devices allow users to choose from multiple OSRs, which change the frequency response of the device and the rate at which the device outputs samples to the host.

An important property of sinc filters is that they are linear-phase filters, meaning that their phase response is linear as a function of frequency. Group delay of a linear-phase filter will be constant across frequency because group delay is proportional to the derivative of phase with respect to frequency. This means that no matter what the input frequency is to a given linear-phase filter, the output will be delayed by the same number of samples.

Let's examine the digital filter of the ADS131E08. That device samples data at the modulator frequency of 1.024 MHz, passes the data through a third-order sinc filter, down-samples the data, and outputs it at the device data rate. In this scenario we chose an OSR of 128, which provides an output data rate of 8 kSPS. **Figure 3** illustrates the magnitude and phase response, as well as the group delay plot, for this filter.

When the ADC outputs data, it only outputs one data point every 128 modulator samples as specified by the OSR. To get the delay in terms of the output data rate, divide the digital filter sample group delay by 128. Because the filter group delay is 190.5 modulator samples, the ADC output will have a delay of approximately 1.5 output samples.

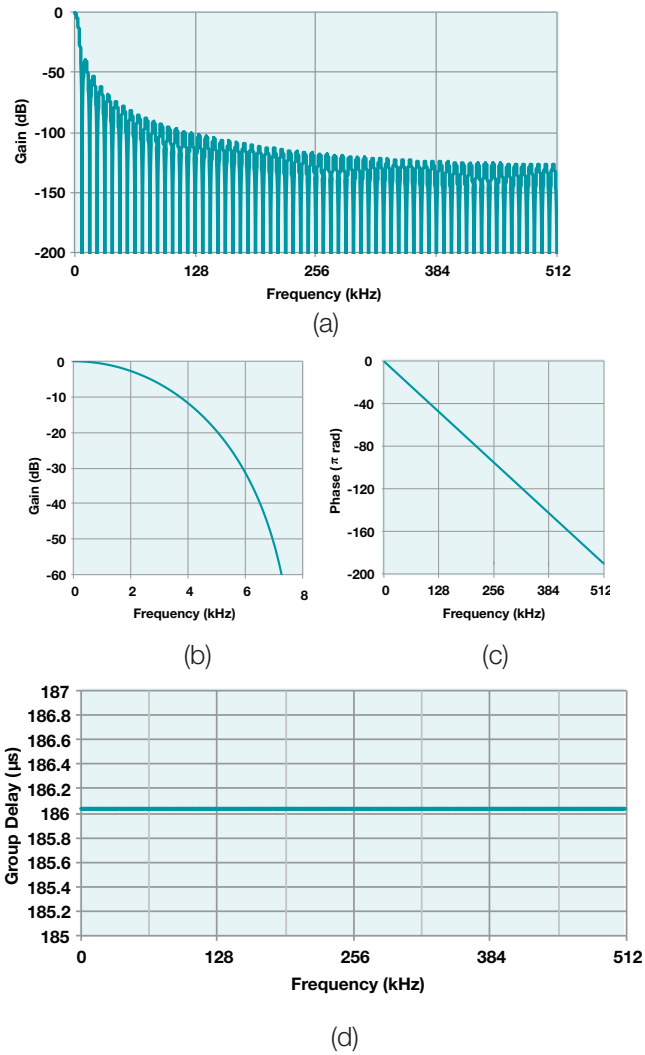

Figure 3: *Magnitude, phase and group delay plots for the third-order sinc response ADC configured with an OSR of 128. Plots (a) and (c) show the magnitude and phase responses, respectively, of the filter through the Nyquist rate for the modulator. Plot (b) shows the magnitude response to the output data rate selected. The group delay for this filter is 190.5 modulator samples, which corresponds to roughly 186 µs, as shown in Plot (d).*

We can see this in the time domain by overlaying a 1 kHz analog input signal with both the digital filter output and the decimated data device output. The plot in **Figure 4** validates the calculated delay.

The delay calculated from the filter response corresponds to the delay shown in this plot. The output appears attenuated with respect to the input. This is a result of the magnitude response of the filter.

Table 1 gives the delay of a sinc^3 digital filter in output samples for some common OSRs.

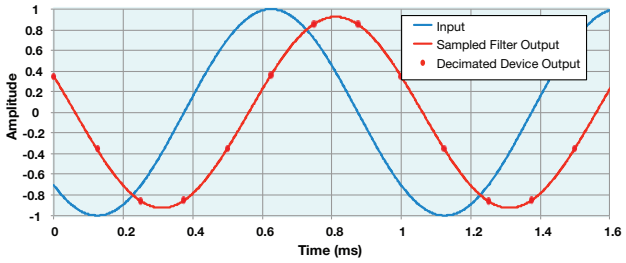

Figure 4: *Analog input (blue), sampled digital filter output (red), and decimated device output (red dots).*

Over-sampling ratio	32	64	128	256	512	1024	2048	4096
Delay (samples)	1.4531	1.4766	1.4883	1.4941	1.4971	1.4985	1.4993	1.4996

Table 1. *Sinc^3 filter group delay in output samples (post decimation) for various OSRs*

Digital logic

Before the digital filter output is obtained by the host, a few steps of logic must occur. For example, a check must be performed to set out-of-bounds filter outputs to the saturation values for the converter. If the device contains an integrated offset and/or gain calibration feature, that logic must also be performed. A device may also insert an extra system clock cycle to prevent a setup or hold time violation caused by propagation delay. Sophisticated devices may have interface integrity checks that require a sample is delayed by an entire conversion cycle.

For example, the delay caused by digital logic in the ADS131E08 is four-master clock cycles, or roughly 2 µs. In the ADS131A04, a 4-channel simultaneous sampling delta-sigma ADC, the device has complex logic to determine whether its conversions are synchronized with other ADCs. In this case, the digital filter output is placed in a buffer for an entire conversion cycle before it is output.

Note that this does not include the time it takes for the host to retrieve the data from the device. Such latency is user-dependent.

Summary

In this white paper I demonstrate that delays in delta-sigma ADCs are deterministic and calculable. This allows for accurate time stamping because the delay will be consistent for given PGA gain, modulator clock, and output sample rate settings.

Examples

As examples, I calculated delays using two different devices with a 24-bit, analog front-end for power monitoring, control and protection. They differ in that the ADS131E08 has eight simultaneous-sampling channels, each with front-end PGAs, and the ADS131A04 has four simultaneous-sampling channels, but does not include a PGA front-end.

The ADS131A04 does not have a programmable gain amplifier, but there is an entire conversion cycle delay from logic execution. Most of the delay on this device is introduced by the phase response of the sinc^3 digital filter. The rate at which the device samples is highly flexible, so Tables 2 and 3 only give delays for two modulator frequencies.

Additional information

- Download these data sheets: ADS131E08, ADS131A04.
- Learn more about TI's Precision ADC portfolio.

ADS131E08		PGA Gains									
		1		2		4		8		12	
		Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
Data Rates (kSPS)	1	1,501	1,501	1,502	1,050	1,502	1,502	1,504	1,504	1,506	1,506
	2	751	751	752	752	752	752	754	754	756	756
	4	376	376	377	377	377	377	379	379	381	380
	8	189	189	189	189	190	190	191	191	193	193
	16	95	94	95	95	96	96	98	96	99	99
	32	48	48	49	48	49	49	51	50	52	51
	64	25	25	25	25	26	25	27	26	29	26

Table 2: *Nominal delay to nearest microsecond for different data rates and PGA settings at DC and Nyquist.*

ADS131A04		f_{mod} (MHz)	
		2.048	4.096
Oversampling ratio	4096	4,999	2,500
	2048	2,499	1,250
	1024	1,249	625
	800	976	488
	768	937	468
	512	624	312
	400	488	244
	384	468	234
	256	312	156
	200	243	122
	192	234	117
	128	156	78
	96	116	58
	64	77	39
	48	58	29
	32	38	19

Table 3: *Delay to nearest microsecond for two possible modulator frequencies and all possible oversampling ratios.*

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