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Comparing TI's TMS320C6671 DSP with ADI's ADSP-TS201S TigerSHARC® Processor

Abstract

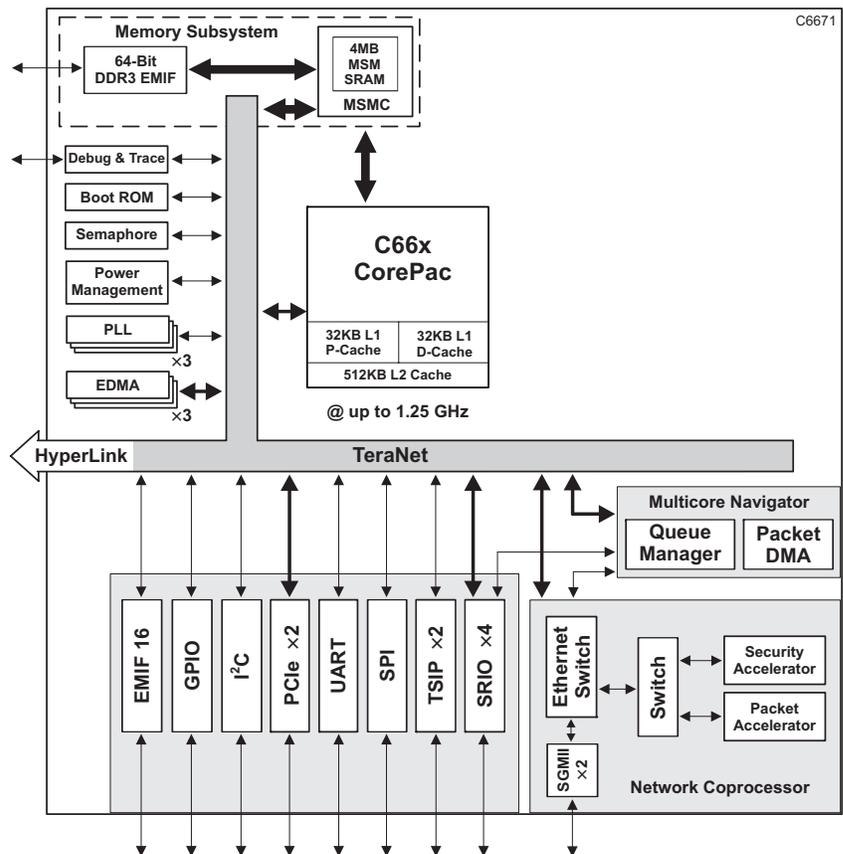
Texas Instruments' new TMS320C6671 digital signal processor (DSP)—based on the TMS320C66x DSP generation—brings fixed- and floating-point computational capability to the industry's fastest single-core DSP.

This makes TI's C6671 a viable alternative for designs based on existing single-core floating-point DSPs in the industry, such as Analog Devices' (ADI) TigerSHARC® processor family.

TI's C6671 DSP not only provides hardware features to implement system-level functions, but goes much further by providing multiple options for implementing additional functions that make it a significantly more powerful single-core DSP than ADI's ADSP-TS2012 TigerSHARC processor.

Although every application is unique, there are some common system-level functions that every DSP-based system design must have: a sufficiently powerful core; an adequately high-bandwidth memory interface for connecting SDRAMs, EPROMs, and FLASH memory; the ability to connect with other DSPs, host processors, and FPGAs/CPLDs; and the right number and types of input/output interfaces. All DSPs have hardware features that enable these primary functions. Because DSP-based systems are inherently software programmable, they come with software development tools that need to be supported by hardware features. Throughout this white paper, some of the key features found in ADI's ADSP-TS201S processor, one of the fastest TigerSHARC processors currently available, are compared and contrasted with features of TI's C6671 DSP, the industry's highest-performing single-core DSP.

Figure 1 High-Level Block Diagram of TI's TMS320C6671 DSP



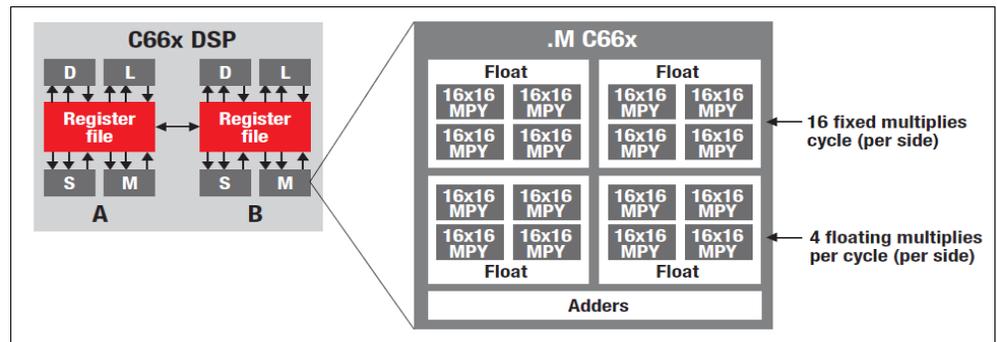
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Selecting a DSP with Sufficient Computational Capability

The ADSP-TS201S TigerSHARC processor has two computation blocks that support both fixed- and floating-point processing. ADI's TigerSHARC architecture lets the DSP execute up to four 32-bit instructions (128-bit VLIW) per cycle with a 10-deep pipeline and has 64- and 32-bit registers. Operating at a maximum speed of 600 MHz, the ADSP-TS201S processor's core has a 1.67-ns instruction cycle time that performs eight 16-bit MACs per cycle and two 32-bit MACs per cycle. This translates into 4.8 GMACs (16-bit) and 1.2 GMACs (32-bit). The core can also perform six single-precision floating-point operations per cycle, which translates into 3.6 GFLOPs. The ADSP-TS201S processor has 3MB of internal memory divided into six different memory blocks, each of which is 16KB, for a total of 96KB of cache.

The C6671 DSP, based on TI's new C66x DSP core and KeyStone multicore architecture, is the industry's highest performing fixed- and floating-point single-core DSP. This device can run at a maximum core speed of up to 1.25 GHz (0.8-ns instruction cycle time). The C66x DSP ISA is an eight-issue machine, executing eight 32-bit instructions (256-bit VLIW) per cycle with an 11-deep pipeline and 64 internal registers. TI's C66x DSP can execute eight single-precision, floating-point MAC operations per cycle and can also perform double- and mixed-precision operations. The C66x DSP core also incorporates 90 new instructions targeted for floating-point and vector-math-oriented processing, compared to TI's previous TMS320C64x+ DSP fixed-point core. The C66x core's raw computational performance is an industry-leading 32 MACs per cycle and 16 FLOPs per cycle, which at 1.25 GHz can perform 40 GMAC/s (TS 4.8 GMACs) and 20 GFLOP/s (TS 3.6 GFLOPs). Internal memory architecture of TI's C66x DSP has L1 program and L1 data cache, each of which is 256KB, including (32KB) 4.5MB of internal Unified L2 SRAM, that can partially be configured as RAM or cache memory (up to 512KB configurable as cache). The error correction and checking (ECC) functions at L1 and L2 on-chip memory enhances system reliability.

Figure 2 High-level View of the Execution Unit Within TI's C66x DSP Core with Respect to Multiply Operations



These enhancements yield sizeable performance improvements in popular DSP kernels used in signal processing, mathematical, and image-acquisition functions. The C66x DSP's ISA is fully backward compatible with TI's TMS320C6000 family of fixed- and floating-point DSPs. The overall performance improvement based on these changes manifests itself in the BDTImark2000™ score on the independent BDTI

DSP Kernel Benchmarks™, which provide a summary measure of signal processing speed. BDTImark2000 and BDTIsimMark2000™ scores for both fixed- and floating-point processors are shown in Figure 3 and Figure 4 (visit www.BDTI.com for more information).

Figure 3 Floating-point Speed Scores for the BDTI DSP Kernel Benchmarks

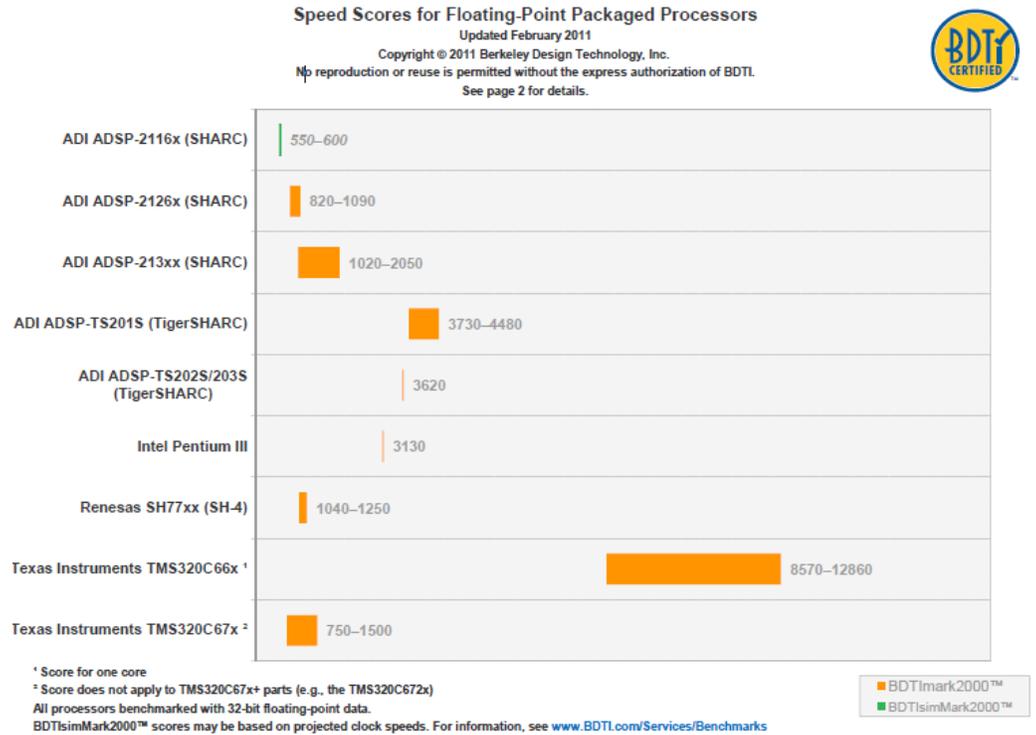


Figure 4 Fixed-point Speed Scores for the BDTI DSP Kernel Benchmarks

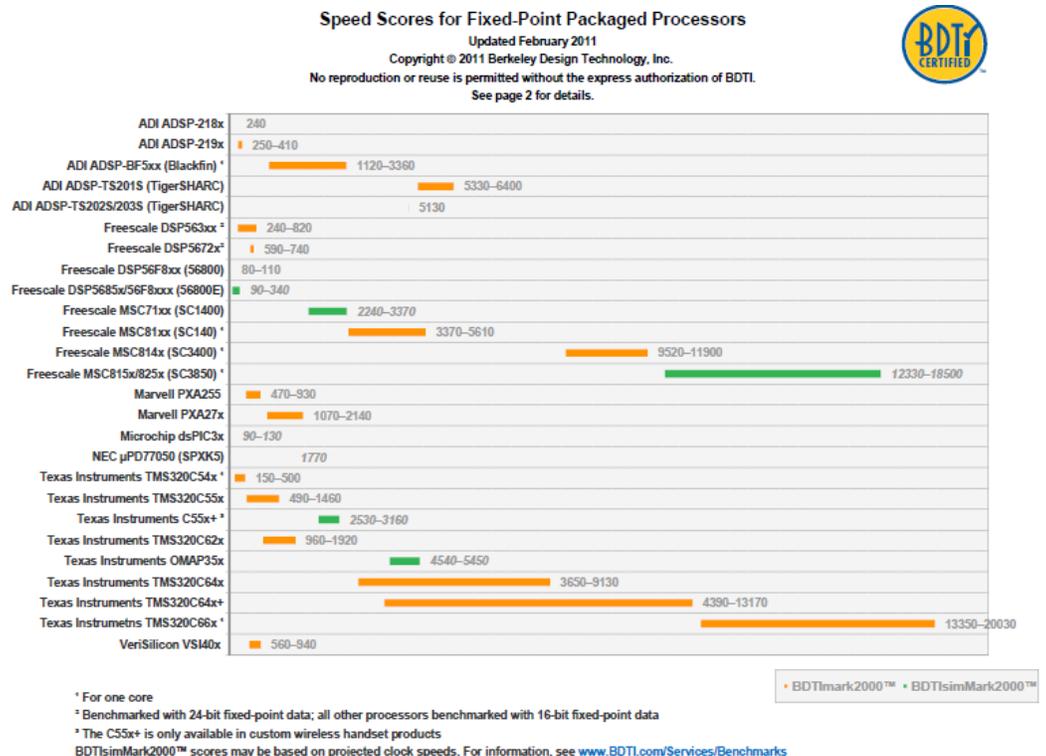


Table 1 General-Purpose Algorithm Benchmarks on TI's C66x DSP Core at 1.25 GHz¹

Benchmark	Speed	Clock Cycle
32-bit algorithm		
1k point FFT (Radix 4)	5.47 μ s	6840
64k point FFT (Radix 4)	0.58 ms	696588
FIR filter (per real tap)	0.2 ns	0.25
[8x8][8x8]matrix multiply (complex floating point)	1.06 μ s	1327
16-bit algorithm		
256 point complex FFT (Radix 4)	0.6 μ s	752

1. Comparison benchmark numbers for these algorithms are also available on the ADSP-TS201S TigerSHARC processor's datasheet, published on Analog Devices' website.

Interfacing with External Memory

Overall system performance depends heavily on the performance of external memory connectivity options provided by DSPs. More often than not, neither the data nor the program fit completely into the internal/cache memory and must be stored externally; this slows system operation considerably. The performance here is a combination of many factors such as bus width, speed, and addressable memory. The ADSP-TS201S processor and C6671 DSP have different ways of implementing similar external memory interfacing requirements as described below.

The ADSP-TS201S processor's external port provides the DSP's interface to off-chip memory through the integrated SDRAM controller, which can connect up to one gigabyte of memory and can transfer 32- or 64-bits of data per clock cycle. The external port supports data transfer rates of one gigabyte per second over the external bus. It is also used to connect to EPROM for booting purposes. Alternate ways to boot the system include boot by an external master (host or another ADSP-TS201S processor), boot by a link port, or no boot, running from memory address.

In contrast, TI's C6671 DSP provides a 64-bit DDR3 external memory interface that can operate at 800 mega transfers per second (MTS), 1033 MTS, 1333 MTS, and 1600 MTS; this provides a raw bit rate of 12.8GB. It can also operate in 16-, 32-, and 64-bit modes. An on-chip multicore shared memory controller (MSMC) provides an address translation block that expands the addressable memory to 8GB of addressable space and a DDR3 memory controller with ECC functionality that enhances system reliability. MSMC is the same IP used in single and multicore DSPs. A prefetch mechanism implemented in MSMC acts as a caching mechanism for external memory; prefetching reduces the quantum of external memory accesses and improves system performance. The MSMC enables the processing core to access on-chip memory directly without drawing from TeraNet (the on-chip communication switching fabric). This prevents the on-chip data communication from being blocked by memory accesses.

The serial peripheral interconnects (SPI) module provides an interface between the DSP and other SPI-compliant devices. The primary purpose of this interface is to enable connection to a SPI ROM for boot. The EMIF16 and I²C module provide alternative interfaces between DSP and external memories, such as NAND/NOR flash and EEPROM.

The C6671 DSP can be booted in multiple ways through EMIF16, SRIO, Ethernet, PCIe, I²C, SPI, and Hyperlink.

High-Speed On-chip Communication and Data Transfers

Direct Memory Access (DMA)

In most systems, on-chip memory is not sufficient for storing the program code or the data in its entirety. This means DSPs must provide an efficient DMA mechanism to transfer code and data back and forth between external memory and internal memory, as well as between peripherals and accelerators. DMA is a feature that enables independent DMA controllers to transfer data between different memories, accelerators, and interfaces without the intervention of the CPU and software. This allows the CPU to execute programs simultaneously with data transfer over the data bus.

The ADSP-TS201S processor's on-chip DMA controller provides 14 DMA channels. The DMA controller performs DMA transfers between the following:

- Internal memory and external memory
- Memory-mapped peripherals
- Internal memory of other DSPs on a common bus, a host processor, or link port I/O
- External memory and external peripherals or link port I/O
- External bus master and internal memory or link port I/O

DMA chaining operations enable applications to automatically link one DMA transfer sequence to another for continuous transmission.

EDMA3 is one of the DMA systems implemented in TI's C6671 DSP. The EDMA3 services software-driven paging transfers, such as data movement between external memory and internal memory, performs sorting or subframe extraction of various data structures, services event driven peripherals, and offloads data transfers from the device CPU.

There are three EDMA channel controllers on the C6671 DSP, providing a total of 144 channels between all three controllers. These controllers also support performance-enhancing features, such as support for two addressing modes: constant addressing and increment addressing mode. The controllers also support transfers in three dimensions array, frame and block, linking mechanism for ping-pong buffering, circular buffering and repetitive/continuous transfers, all without CPU intervention, debug visibility (Queue watermarking/threshold) and error and status recording. TI's C6671DSP also has a separate DMA mechanism called IDMA that transfers data and code between on-chip RAM and L1 program and L1 data caches.

Additional C6671 DSP On-chip Communication Features

TI's KeyStone multicore architecture, the foundation of the C66x DSP generation, provides a high-performance structure for integrating DSP cores with application specific coprocessors and I/O. The KeyStone architecture is the first of its kind that provides adequate internal bandwidth for non-blocking access to all processing cores, peripherals, coprocessors, and I/O. Two of the main hardware elements enabling the KeyStone architecture are TI's *Multicore Navigator* and *TeraNet*.

Multicore Navigator is an innovative hardware IP, implementing a packet-based message transfer mechanism, with 8192 hardware queues and six DMA channels for transferring messages. When tasks are allocated to the queues, the Multicore Navigator provides a hardware-accelerated dispatch that directs tasks to the appropriate available hardware. This is a very high-speed interprocess communication (IPC) and peripheral/accelerator interfacing mechanism that significantly simplifies the software architecture and reduces CPU processing needs for these functions.

The packet-based system-on-chip (SoC) uses the two Tbps capacity of the *TeraNet* switched central resource to move packets. The TeraNet switch fabric interconnects the C66x DSP cores and their local memories, external memory, the enhanced DMA v3 (EDMA3) controllers, on-chip coprocessors, and high-speed I/O. The TeraNet switch allows each of these to operate at maximum efficiency with no blocking or stalling. It allows for concurrent transfers between non-conflicting master/slave pairs and can support a very high total data rate across any endpoint. Because external memory access through the MSMC no longer routes through the TeraNet, it further reduces the chances of the switching fabric being a communication bottleneck.

Connecting to an External World—Multiprocessor Design and High-Speed I/O

In many embedded systems, there is a need for high-speed interfaces to enable interconnecting multiple DSPs or to connect DSPs to other components like CPLDs and FPGAs. Connecting multiple DSPs is often a way to increase system processing capability, whereas CPLD/FPGAs implement preprocessing functions and often act as glue logic to connect to interfaces and peripherals that are not on the DSP. There is almost always a need for high-speed I/O to transfer user data in and out of the DSP.

The external connectivity needs in an ADSP-TS201S processor are fulfilled primarily by *external port* and *link ports* that offer powerful features tailored to multiprocessing DSP systems. This multiprocessing capability provides the highest bandwidth for interprocessor communication including:

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point-to-point communication

The external port and link ports provide integrated, glueless multiprocessing support and enable direct interprocessor accesses of each ADSP-TS201S processor's internal memory and registers.

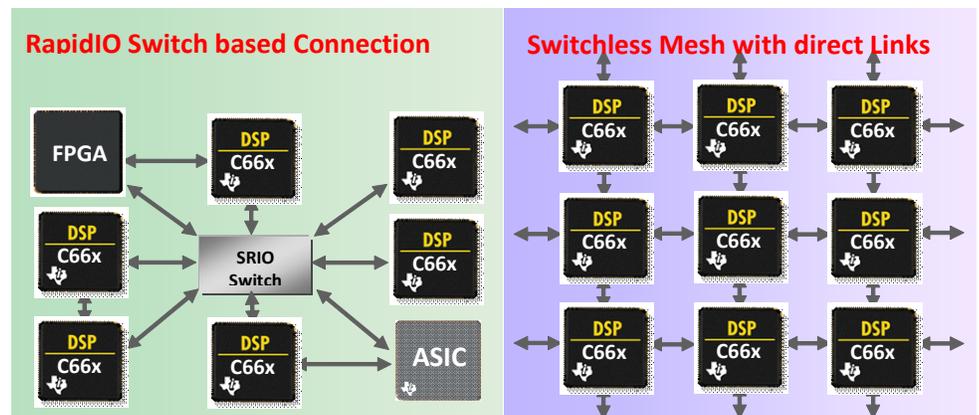
External port is a multifunction block that can be used to connect the on-chip SoC bus to different external devices, such as host processors, SDRAM memory, and EPROM for boot and, at the same time, to connect *multiple* DSPs together. The DSP's *four full-duplex link ports* each provide additional four-bit receive and four-bit transmit I/O capability, using low voltage differential-signal (LVDS) technology. Each link port can support up to 500MB per second, per direction, for a combined maximum throughput of 4GB per second. The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications.

The C6671 DSP is *pin-for-pin compatible* with TI's C66x DSPs available in two, four, and eight core versions, the TMS320C6672, TMS320C6674, and TMS320C6678, respectively. This allows scalable hardware design that can go from a 1.25 GHz single core DSP design all the way to an effective 10 GHz DSP design, the C6678. For systems that need to interconnect multiple DSPs, the C6671 DSP provides multiple high-speed interface options for DSP-to-DSP, DSP-to-FPGA/CPLD, networking interface, backplane communication, and other interfacing requirements. The following paragraphs give descriptions of different interfaces and their features.

Hyperlink is a TI-developed four-lane SerDes interface designed to operate at 12.5 Gbps per lane that provides a 50 Gbps chip-level interconnect that allows SoCs to work in tandem. Its low-protocol overhead and high throughput make Hyperlink an ideal interface for chip-to-chip interconnections. The C6671 DSP includes a Hyperlink interface for companion chip/die connectivity, such as connecting two C6671 or C6672, C6674, or C6678 DSPs to each other, glueless, or connecting an FPGA/CPLD to the DSP. Working with Multicore Navigator, Hyperlink dispatches tasks to tandem devices transparently and executes tasks as if they are running on local resources and provides connectivity between DSPs at the switching fabric level.

The *Serial RapidIO (SRIO) v2.3* port on the C6671 device is a four-lane (5 Gbps/lane) serial interface, high-performance, low-pin-count interconnect aimed for embedded markets. The use of RapidIO interconnect in a board design can create a homogeneous interconnect environment leading to lower system cost by providing lower latency, reduced overhead packet data processing, and higher system bandwidth. RapidIO is rapidly being accepted as a standard for backplane communication in chassis-based systems, such as ATCA. For more information on RapidIO, visit www.rapidio.org.

Figure 5 On-board Connectivity using Serial RapidIO



PCI Express (PCIe Gen II) supports two lanes on the C6671 DSP and provides an interface between the DSP and other PCIe-compliant devices, creating boards for chassis supporting PCIe in the backplane, and creating PC pluggable PCIe cards and more. The PCI Express module has low-pin count, high reliability, and high-speed data transfer at rates of 5 Gbps per lane on the serial links (an overall 10 Gbps link). For more information, visit www.pcisig.com/specifications/pcieexpress.

SGMII Gigabit Ethernet Interface + Ethernet Switch and the compliant Ethernet Media Access Controller (EMAC) modules provide an efficient interface between the C6671 DSP and the networked community. The EMAC supports 10 Mbps, 100 Mbps and 1000 Mbps in full-duplex mode. It also supports hardware flow control and quality-of-service (QoS). The C6671 DSP also has an on-chip three-port gigabit Ethernet (GigE) switch that supports IEEE 1588 timing protocol. An additional benefit of the SGMII interface standard is that it allows devices to interconnect without the need for an Ethernet PHY.

The GigE and Ethernet Switch work closely with an on-chip network co-processor, which provides L2 to L4 classification functionalities. It supports classification for Ethernet, virtual LAN (VLAN), multiprotocol label switching (MPLS) over Ethernet, IPv4/6, generic route encapsulation (GRE) over IP, and other session identifications over IP, such as TCP and UDP ports. The GigE and Ethernet Switch also provide checksum capabilities and QoS capabilities. It can process up to 1.5 million packets per second and provide wire-speed processing on 1 Gbps Ethernet traffic on IPsec, Secure Real Time Protocol (SRTP), and other security protocols.

The SGMII interface is another convenient way to connect host processors to DSPs. Two *Telecom Serial Interface Ports* provide large bandwidth (two, four, and eight lanes at 32.768, 16.384, and 8.192 Mbps per lane and up to 1024 DS0s) to support audio- and telephony-centric applications. The C6671 DSP also provides many other low speed interfaces, such as SPI, I2C, GPIOs, and UARTs.

Software Development Tools

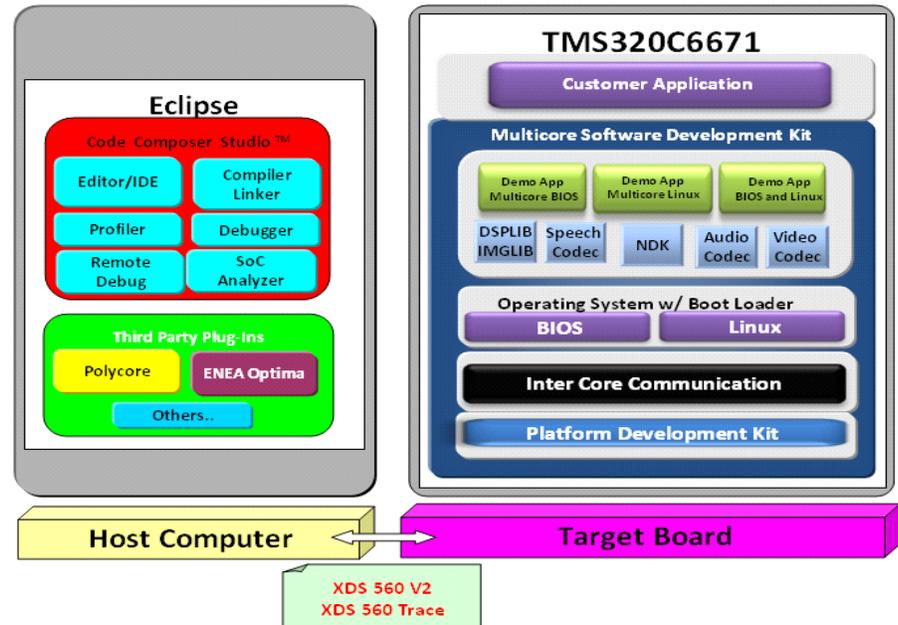
Developing embedded systems based on DSPs requires a comprehensive set of tools, which both Analog Devices and Texas Instruments provide.

ADI's ADSP-TS201S processor is supported by CROSSCORE® software and hardware development tools including emulators and a VisualDSP++® development software environment. The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management and is a realtime operating system (RTOS). ADI's DSP emulators use the IEEE 1149.1 JTAG test access port of the ADSP-TS201S processor.

TI's C6671 DSP is supported by Code Composer Studio™ integrated development environment (CCS Studio IDE), TI's integrated software and hardware development toolset. CCS includes compilers, source code editor, project build environment, debugger, profiler, simulators, and many other features. These features have been enhanced to support multicore software development and debugging, such as support for OpenMP language constructs. OpenMP is a popular open source multicore programming framework. CCS is based on the Eclipse open source software framework which offers an excellent software framework for building software development environment tools and is becoming a standard framework used by many embedded software vendors. CCS and emulators make use of hardware debugging features provided by TI's C6671 DSP, like advanced event triggering (AET) for enabling hardware breakpoints and trace buffers for tracing code execution. The primary emulation interface is IEEE 1149.1 JTAG.

Along with development tools, a multicore software development kit (MCSDK) is also available from TI. The MCSDK includes the SYS/BIOS realtime operating system, as well as Linux ported natively to TI's C66x architecture. The MCSDK includes various functional libraries, such as DSPLib, IMGLib, codecs, and TCP/IP stack.

Figure 6 TI's Multicore Software Development Kit (MCSDK)



Summary

TI's C6671 DSP provides system designers with an alternative to ADI's ADSP-TS201S TigerSHARC® processor, especially for applications requiring floating-point capability. As shown throughout this white paper, TI's C6671 DSP provides more fixed- and floating- point performance compared to ADI's TigerSHARC® family of processors, including the ADSP-TS201S processor. The C6671 DSP also has many more hardware features that can further improve performance. The features of the C6671 DSP include availability of a network coprocessor, Multicore Navigator for IPC, and support for realtime system software, such as semaphores and timers. TI's C66x family of pin-for-pin compatible DSPs allows scalable hardware design with options for interconnecting multiple DSPs if system architecture demands such an expansion.

ADI's ADSP-TS201S TigerSHARC® processor requires a FPGA/CPLD to meet most application-interfacing requirements. TI's C6671 DSP provides multiple on-chip interfaces, such as SRIO, GigE, and PCIe, which reduce the need for discrete interface chips; this results in lower board-level device count, simplified system design, and overall lower-cost BOM.

Table 2 Comparison of Available Options for Solving Typical Hardware Design Issues

Function	TS2015	TMS320C6671
Connecting Multiple DSPs on a board	Four Link Ports @1GB/sec per port (32 Gbps total)	Multiple Options: <ul style="list-style-type: none"> • Four lanes of HyperLink glueless pt-to-pt (50 Gbps link) • Four lanes of SRIO via SRIO switch (20 Gbps link) • Two lanes of PCIe via PCIe switch (10 Gbps link) • Two GigE interfaces via Ethernet switch (2 Gbps)
External Memory Interface	External Bus - SDRAM Controller	64-bit 1600MHz DDR3
FLASH Memory Connectivity	External Bus	Multiple Options: <ul style="list-style-type: none"> • SPI • EMIF16
CPLD/FPGA connectivity	Four Link Ports @1GB/sec per port (32 Gbps total)	Multiple Options: <ul style="list-style-type: none"> • GPIO • SPI • SGMII • Serial RapidIO • PCIe • HyperLink
High-Speed I/O e.g. GigE/PCIe/SRIO	Discrete FPGA/ASIC connected via Link Port or External Bus	Multiple On-Chip Interfaces: <ul style="list-style-type: none"> • Gigabit Ethernet • Serial RapidIO • PCIe • HyperLink

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