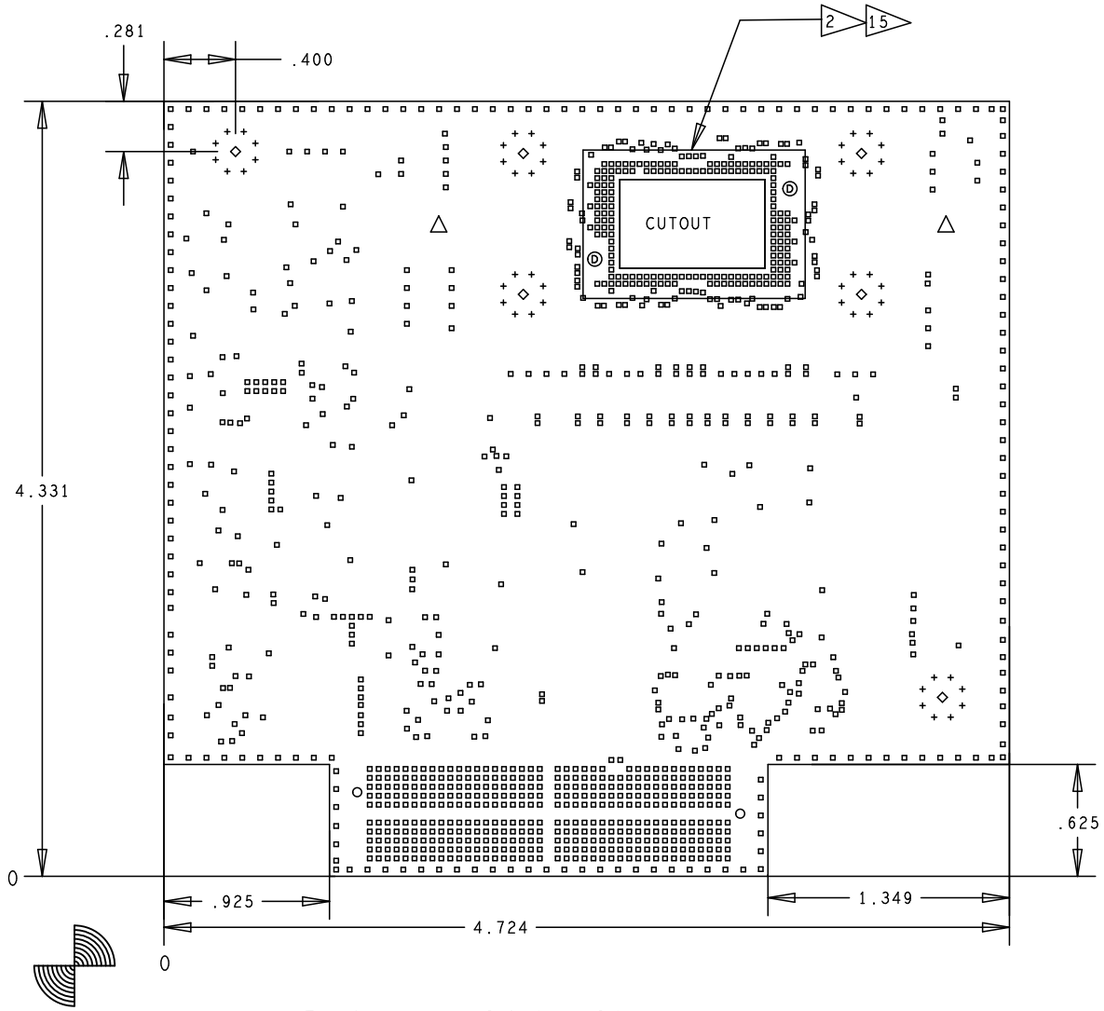
| DRILL CHART: TOP to BOTTOM | | | | |
|---|---|---|---|---|
| ALL UNITS ARE IN MILS | | | | |
| FIGURE | SIZE | TOLERANCE | PLATED | QTY |
| ▫ | 12.0 | +3.0/-12.0 | PLATED | 1184 |
| + | 14.0 | +3.0/-3.0 | PLATED | 48 |
| ▫ | 24.0 | +3.0/-3.0 | PLATED | 16 |
| ◇ | 189.0 | +3.0/-3.0 | PLATED | 6 |
| ○ | 50.0 | +3.0/-3.0 | NON-PLATED | 2 |
| ⓟ | 78.74 | +2.0/-2.0 | NON-PLATED | 2 |
| △ | 276.0 | +3.0/-3.0 | NON-PLATED | 2 |




Primary Side Shown

FAB NOTES:

1. ALL DIMENSIONS ARE IN INCHES. UNLESS OTHERWISE NOTED. ALL BOARD OUTLINE DIMENSION TOLERANCES ARE +/- .010"
2. THE PWB SHALL BE FABRICATED TO IPC-6011 AND IPC-6012, CLASS 2, TYPE 3. WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2. CURRENT REVISIONS.
3. BOARD MATERIAL SHALL BE 180 Tg/340 Td ISOLA FR-370HR OR EQUIVALENT, RoHS COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED IPC-4101B. RoHS CERTIFICATE OF CONFORMANCE SHALL BE DELIVERED WITH EACH LOT.
4. ALL BOARDS MUST MEET OR EXCEED UL94V-0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER.
5. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANNULAR RING OF .001 INCH.
6. OVERALL BOARD THICKNESS TO BE .071 +/- .0062 AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.
7. ALL LAYERS TO BE 1/2 OZ. COPPER.
8. MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
9. MAXIMUM RATED VOLTAGE BETWEEN CONDUCTORS SHALL BE 65 VOLTS PEAK.
10. NO BREAKOUT ALLOWED ON PLATED THROUGH HOLES.
11. FOIL OUTER OPTIONAL.
12. INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
13. TEARDROP VIAS AS NECESSARY.
14. THIEVING ALLOWED ON INNER LAYERS ONLY.
15. VIA-IN-PADS SHALL BE FILLED WITH NON-CONDUCTIVE EPOXY, POLISHED FLAT, AND PLATED SHUT SUITABLE FOR BGA SOLDERING.

PROCESS NOTES:

1. EXCEPT AS NOTED BELOW, ALL EXPOSED CONDUCTORS ON BOTH SIDES PWB SHALL BE ELECTROPLATED GOLD (5-15 MICROINCHES) OVER ELECTROPLATED NICKEL (MINIMUM 50 MICROINCHES).
2. PLATE INDICATED AREA WITH ELECTROPLATED GOLD (30 MIN MICROINCHES) OVER ELECTROPLATED NICKEL (MINIMUM 50 MICROINCHES).
3. APPLY LPI SOLDERMASK. COLOR: RED. SOLDERMASK SHALL CONFORM TO IPC-SM-840, CLASS H. CURRENT REV.
4. FABRICATION VENDOR IS ALLOWED TO INCREASE SOLDERMASK COMPONENT PADS BY A MAXIMUM 1 MIL ON EACH SIDE OVER THE COPPER PAD IN ORDER TO MEET TOOLING REQUIREMENTS WHILE MAINTAINING WEBBING BETWEEN ADJACENT PADS.
5. APPLY LPI SILKSCREEN OR EQUIVALENT PER THE ARTWORK BOTH SIDES. COLOR: WHITE.
6. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED IPC-D-356 NETLIST.

| LAYER STACKUP | CONTROLLED IMPEDANCE +/- 10% 50 OHMS SINGLE ENDED | 100 OHMS DIFFERENTIAL |
|---|---|---|
| LAYER 1 - PRIMARY SIDE | .009 | .0044 TRACE .0056 SPACE |
| LAYER 2 - SIGNAL | .005 | .0038 TRACE .0062 SPACE |
| LAYER 3 - GND PLANE | | |
| LAYER 4 - SIGNAL | .005 | .0038 TRACE .0062 SPACE |
| LAYER 5 - GND PLANE | | |
| LAYER 6 - SIGNAL | .005 | .0038 TRACE .0062 SPACE |
| LAYER 7 - GND PLANE | | |
| LAYER 8 - SIGNAL | .005 | .0038 TRACE .0062 SPACE |
| LAYER 9 - GND PLANE | | |
| LAYER 10 - SIGNAL | .005 | .0038 TRACE .0062 SPACE |
| LAYER 11 - GND PLANE | | |
| LAYER 12 - SIGNAL | .005 | .0038 TRACE .0062 SPACE |
| LAYER 13 - GND PLANE | | |
| LAYER 14 - SECONDARY SIDE | .009 | .0044 TRACE .0056 SPACE |

LIBRA INDUSTRIES

| TI | | |
|---|---|---|
| BOARD NAME: DLP079-00X S410 DMD Board | DESCRIPTION: FABRICATION DRAWING | |
| PROJECT #: DLP-30345-02 | DATE: 16 AUG 2023 | REVISION: |