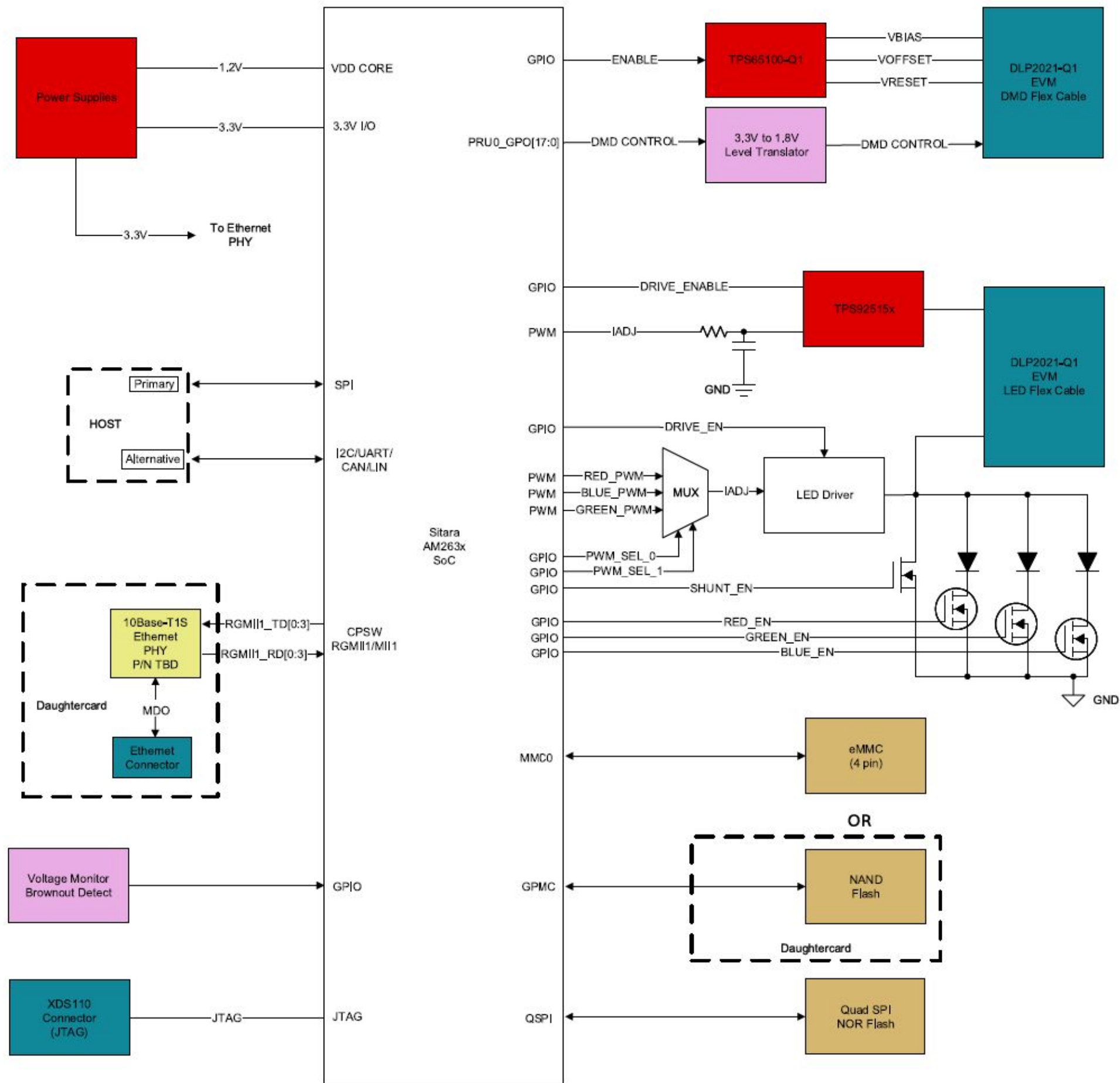


A

B

C

D



A

B

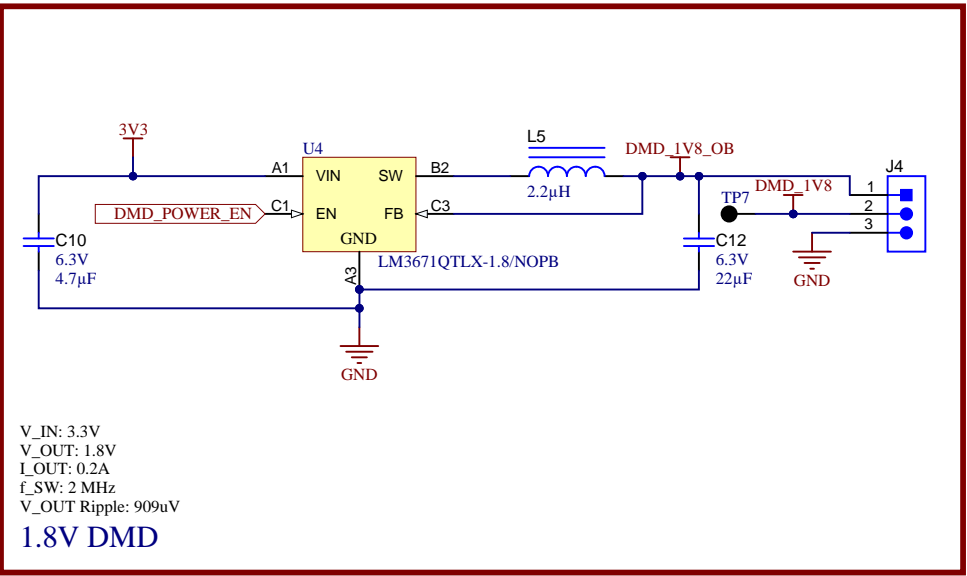
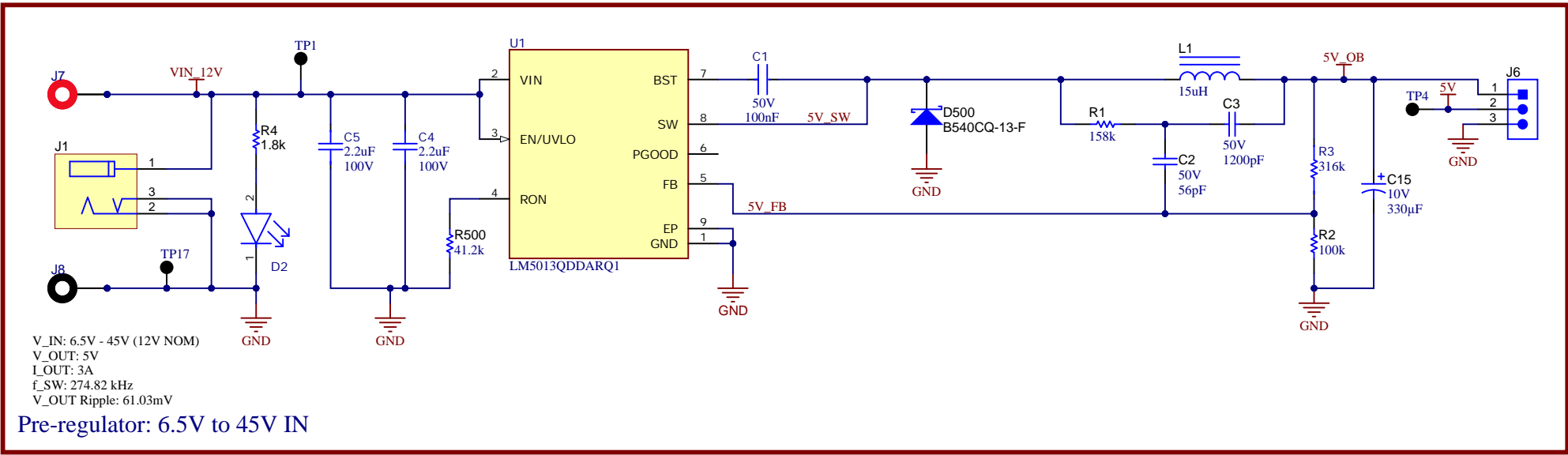
C

D

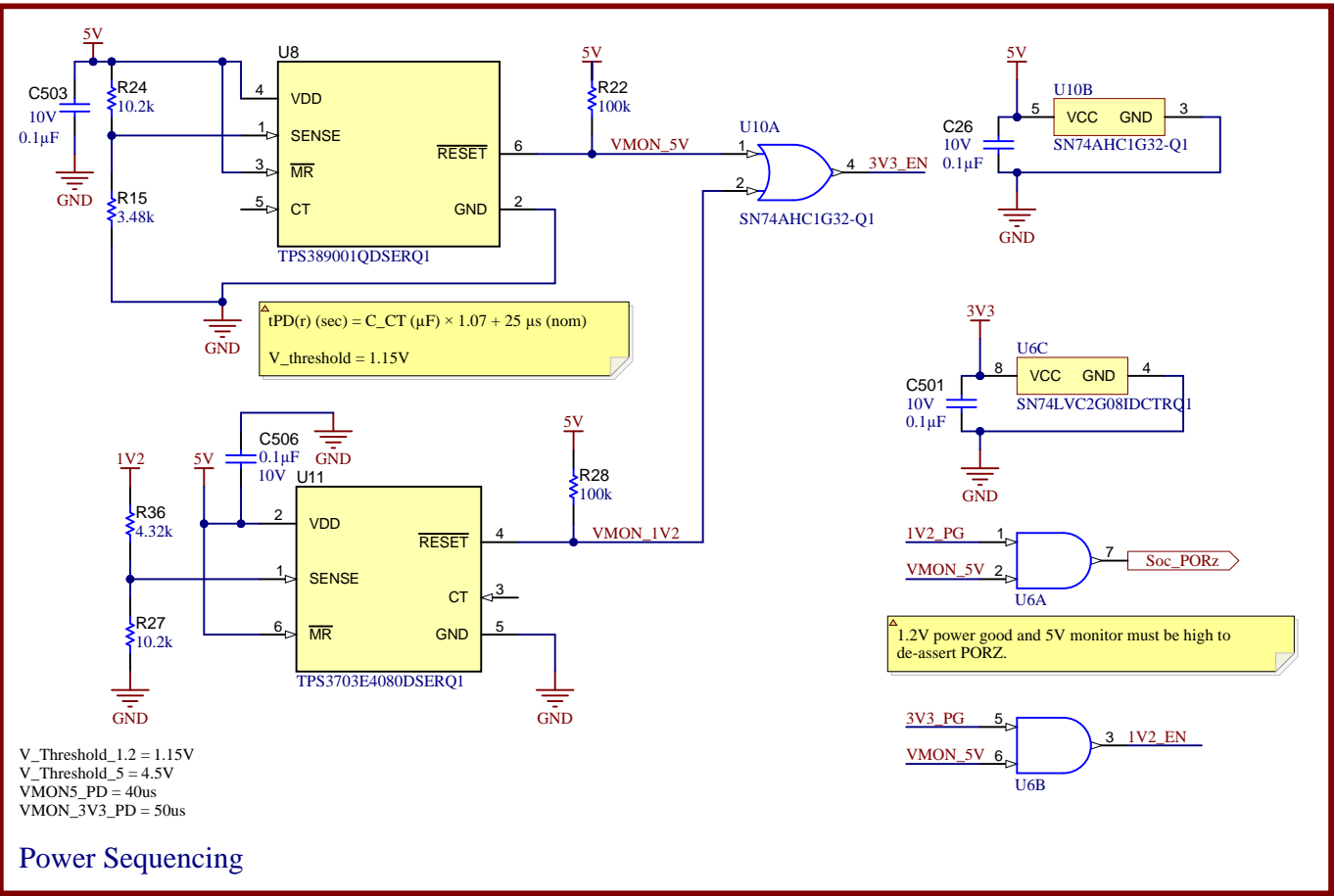
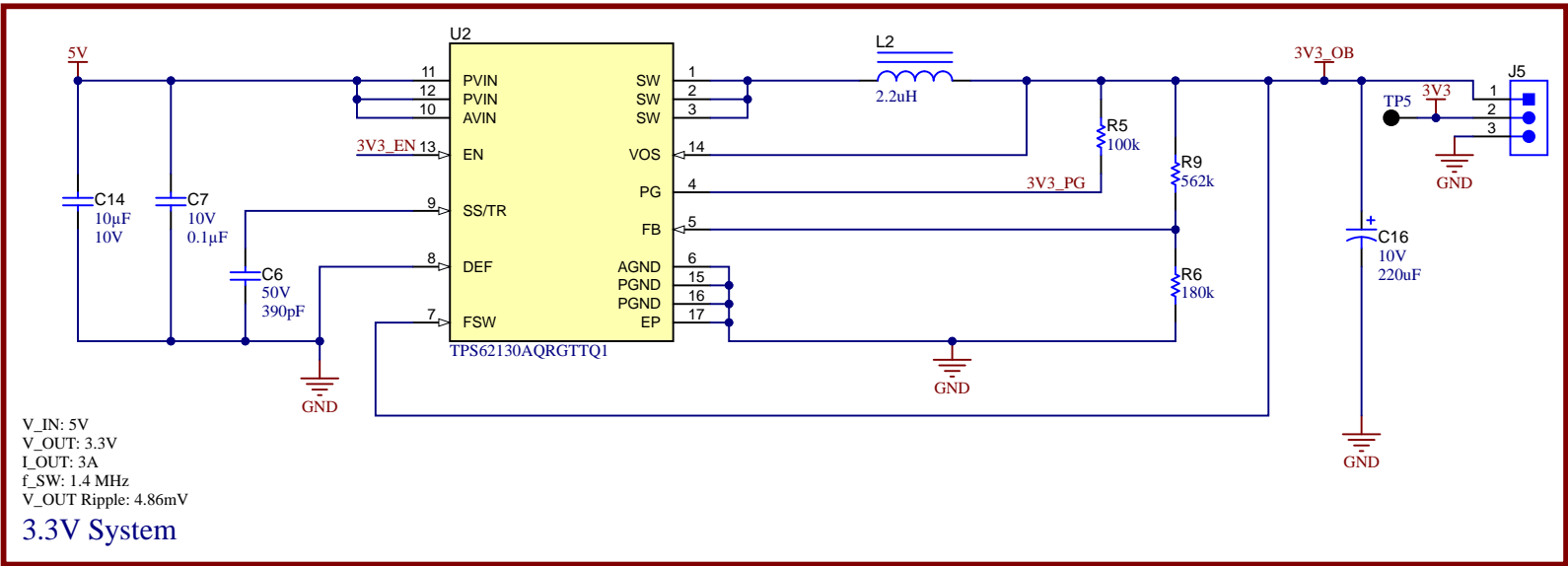
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.



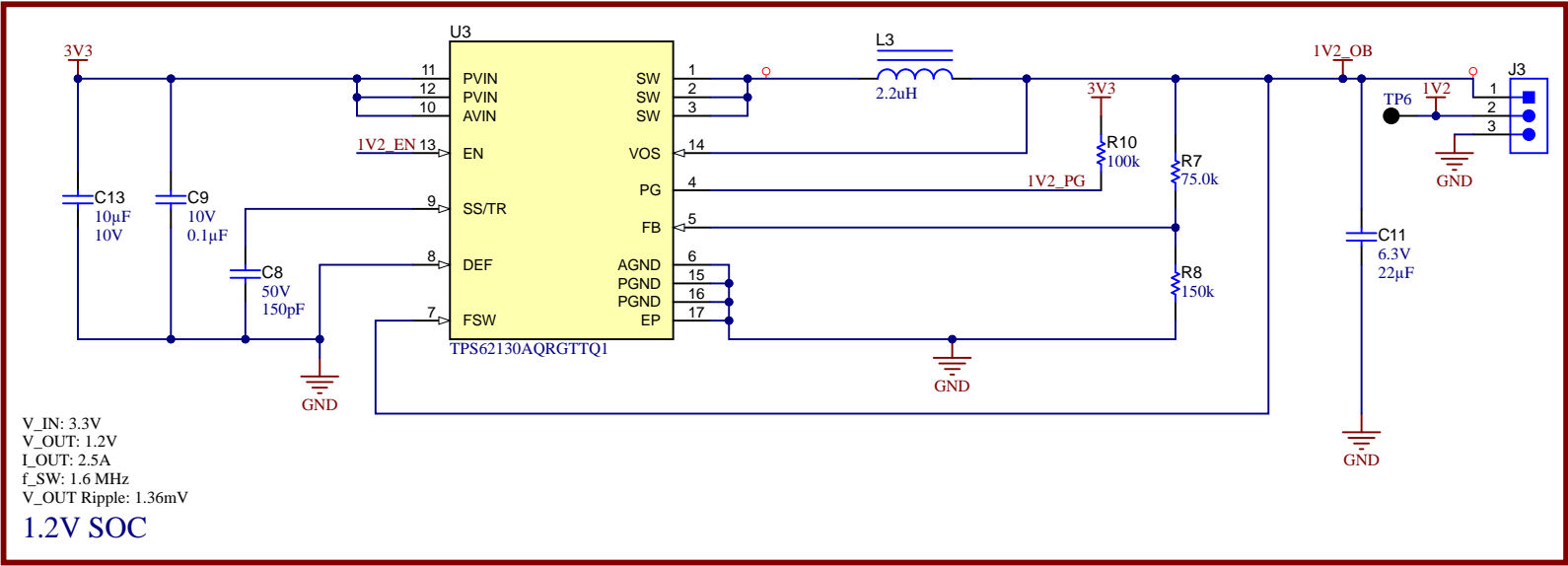
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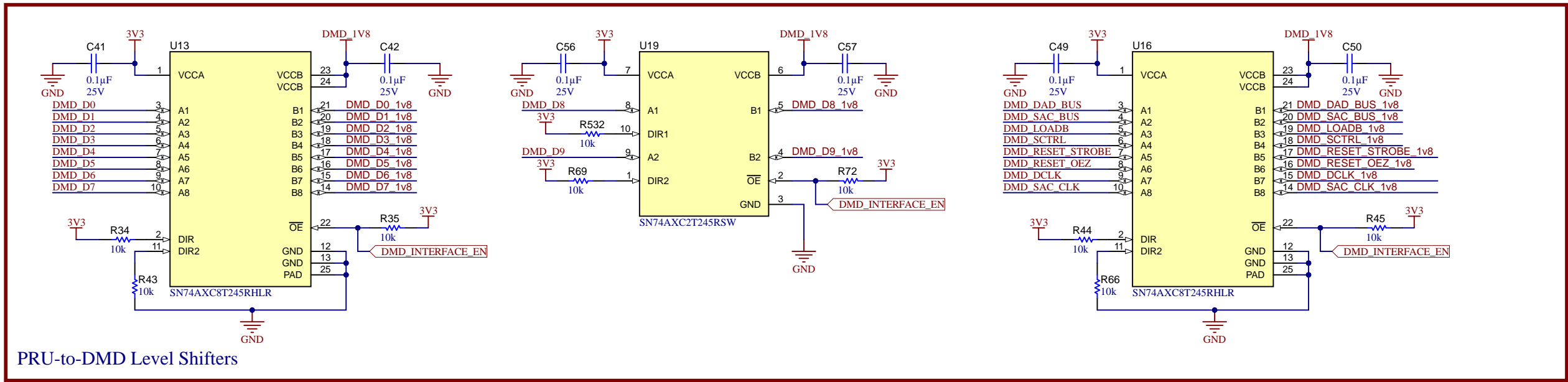
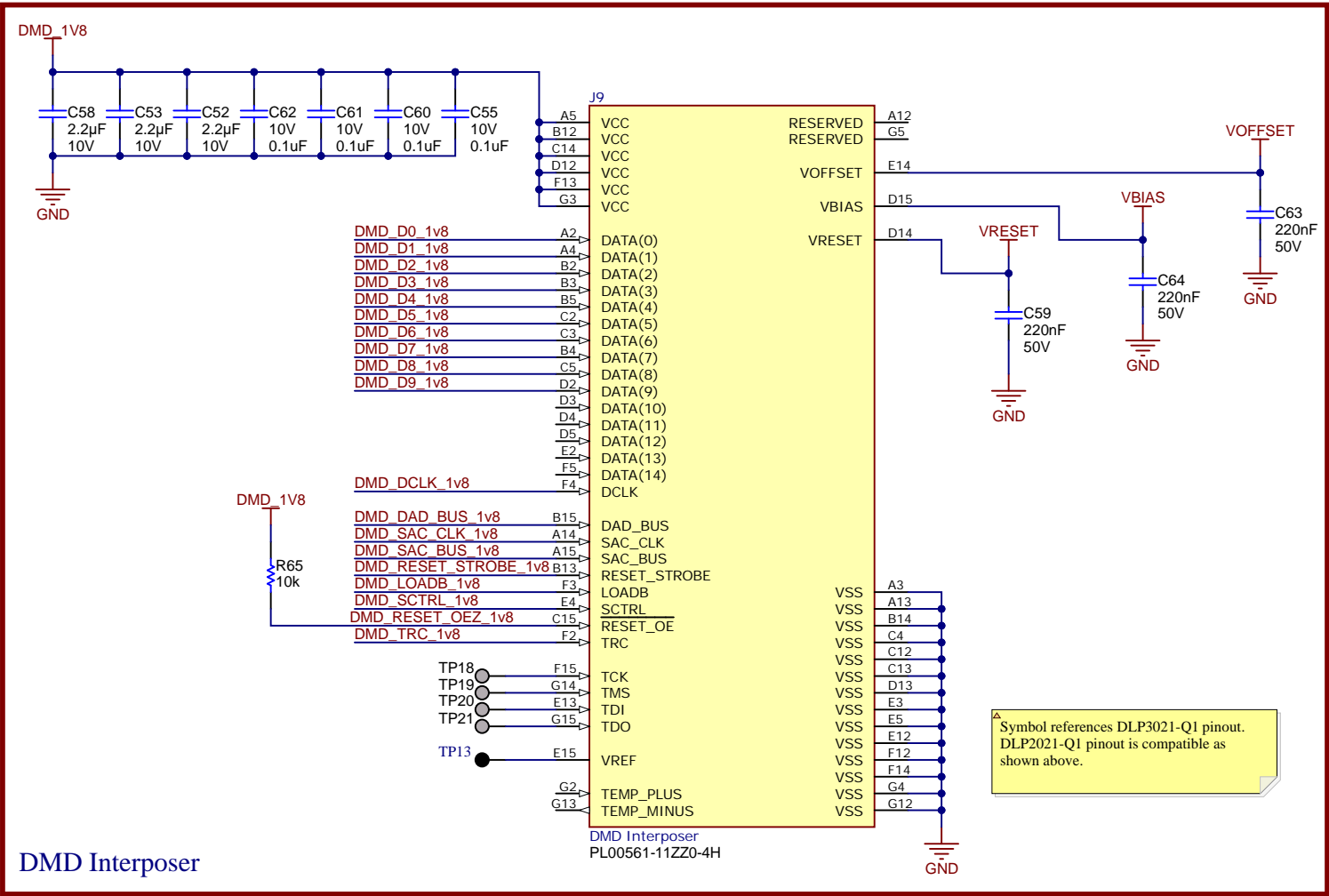
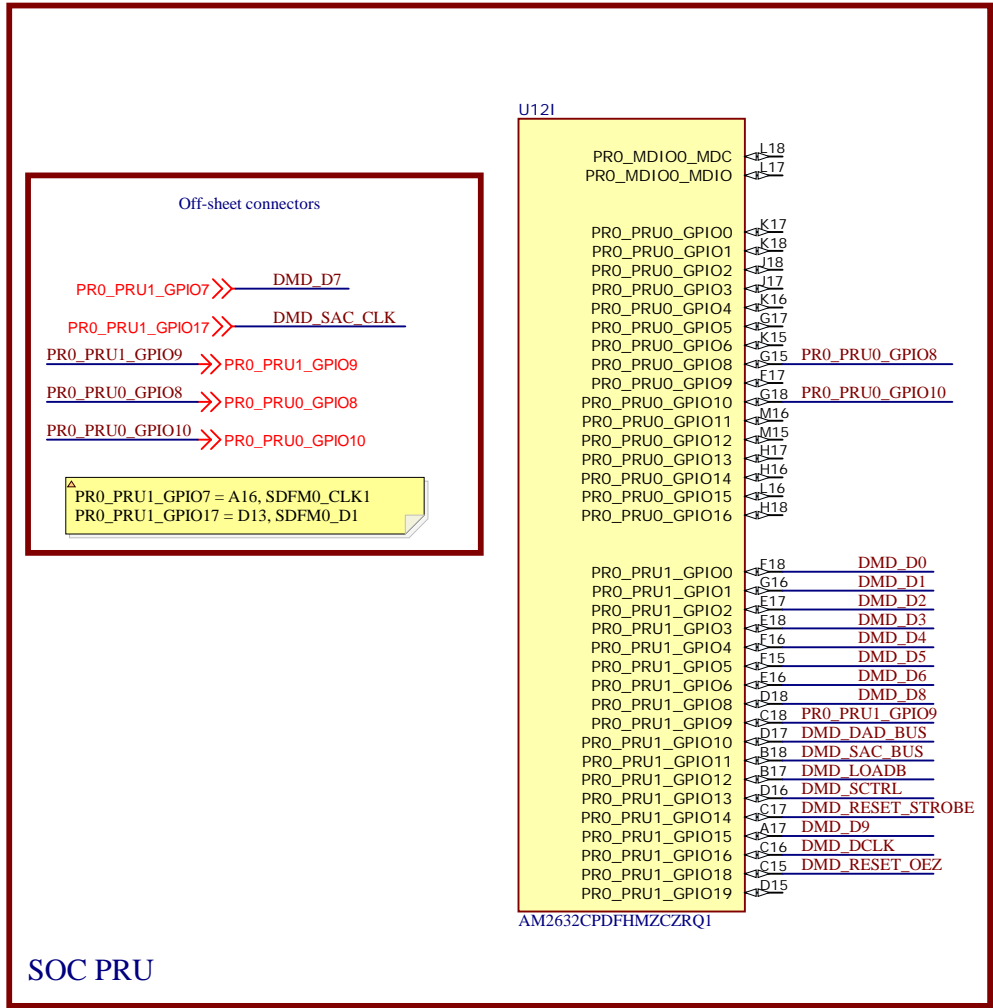
D

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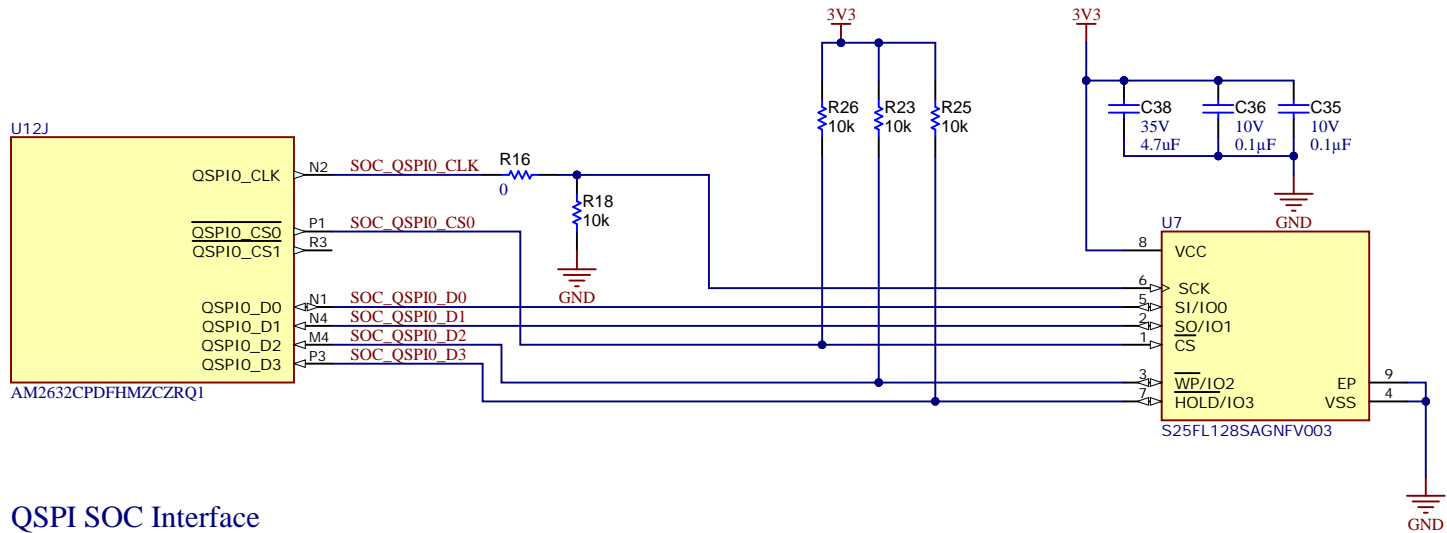
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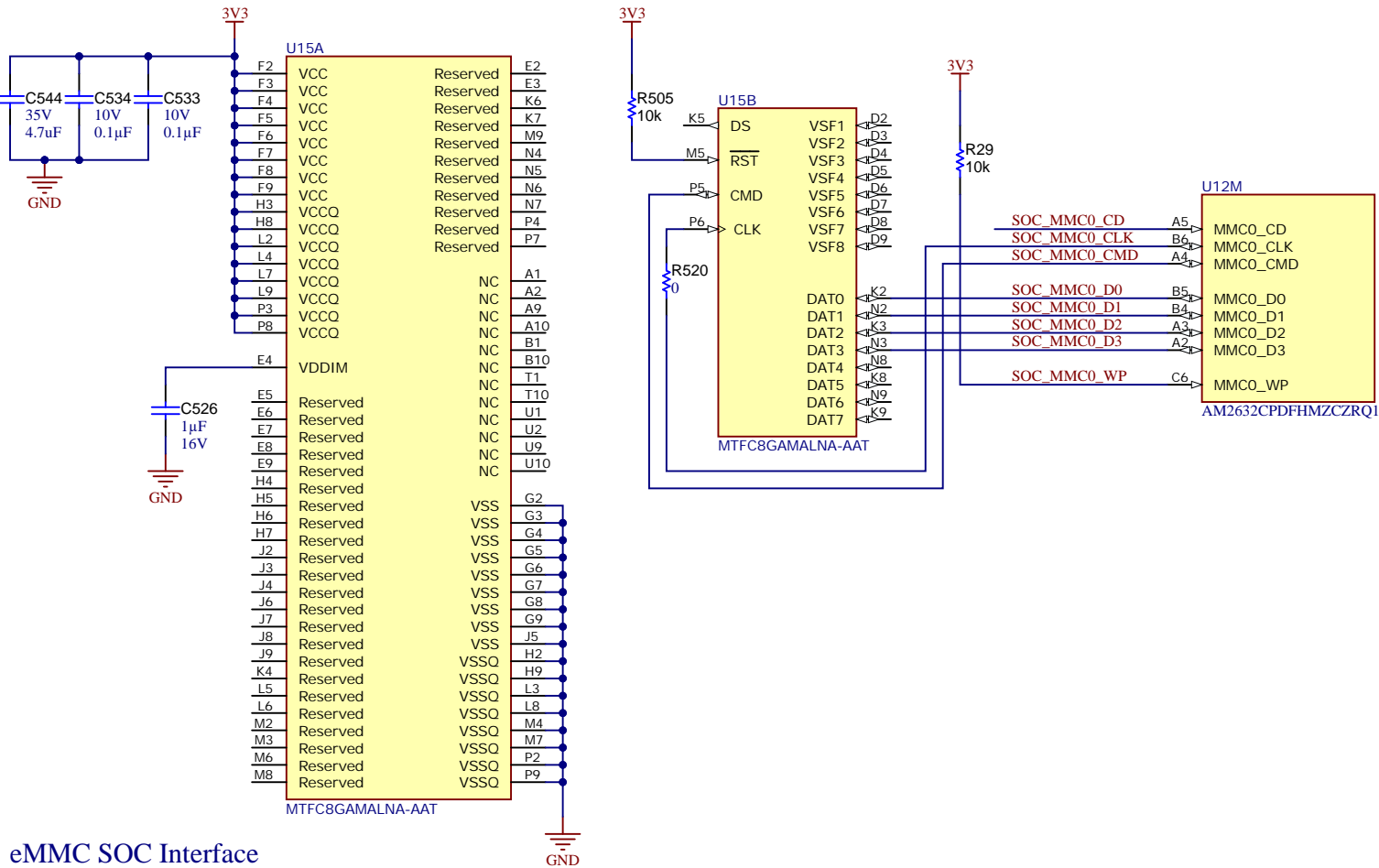
B

C

D



QSPI SOC Interface



eMMC SOC Interface

PORz RC Delay:  
- Creates GND to 3.0V delay of 1ms  
- Designed to leave Soc\_PORz (after RC filtering) low such that U18 drives SOP[3:0] state for >tSOP.hold time after PORz

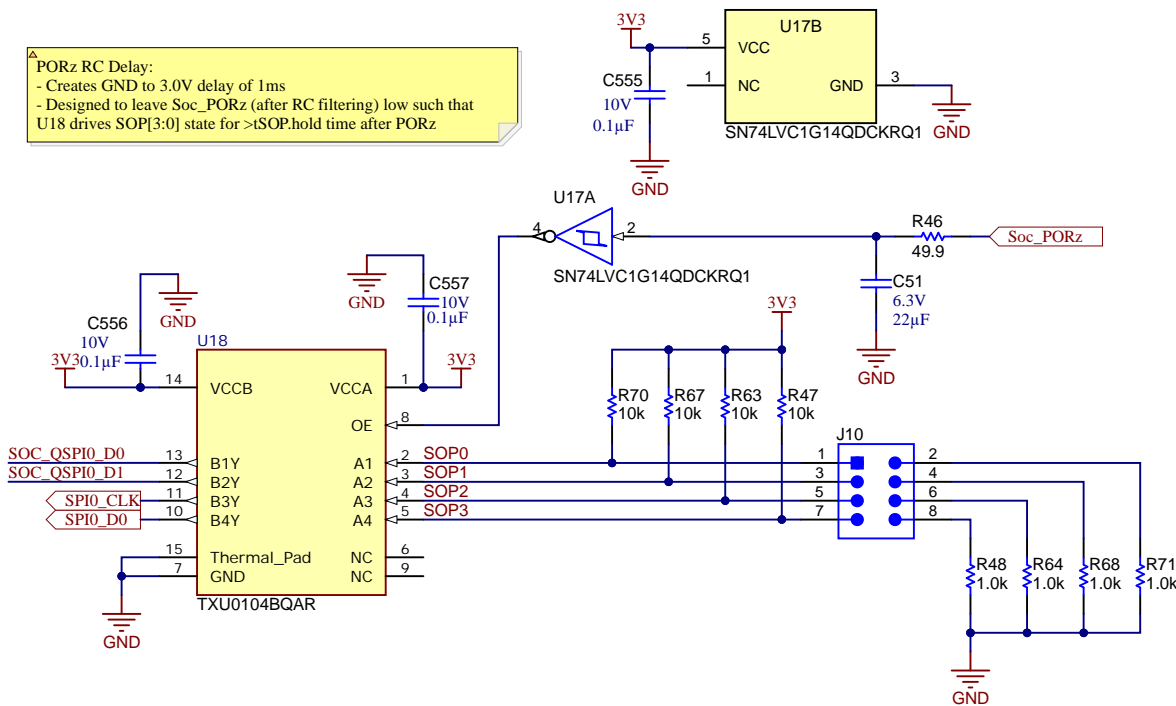


Table 5-2. BOOTMODE Pin Mapping

Boot Mode	SPI0_D0_pad (SOP3)	SPI0_CLK_pad (SOP2)	QSPI_D1 (SOP1)	QSPI_D0 (SOP0)
QSPI (4S) - Quad Read Mode	0	0	0	0
UART	0	0	0	1
QSPI (1S) - Single Read Mode	0	0	1	0
QSPI (4S) - Quad Read UART Fallback Mode	0	1	0	0
QSPI (1S) - Single Read UART Fallback Mode	0	1	0	1
DevBoot	1	0	1	1
Unsupported Boot Mode	All other combinations not defined above			

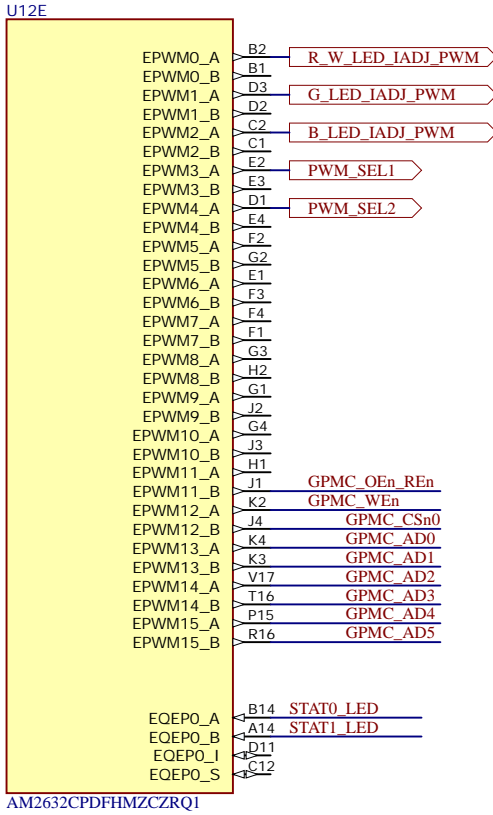
SOC BOOT MODE

A

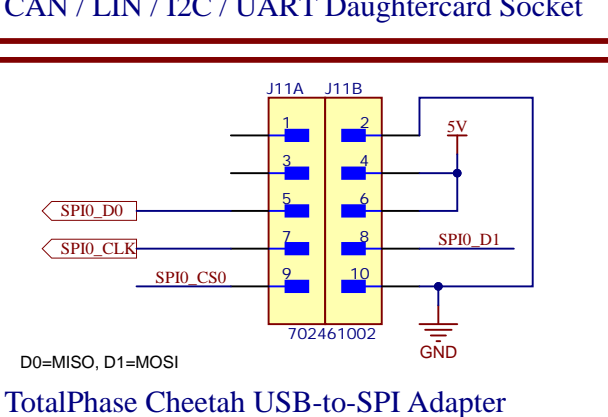
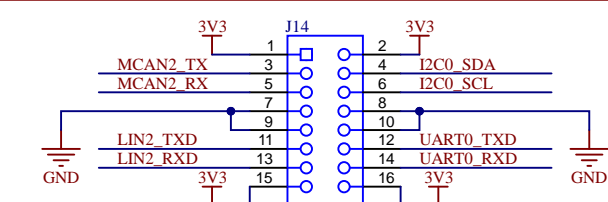
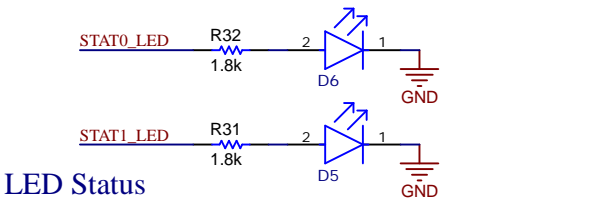
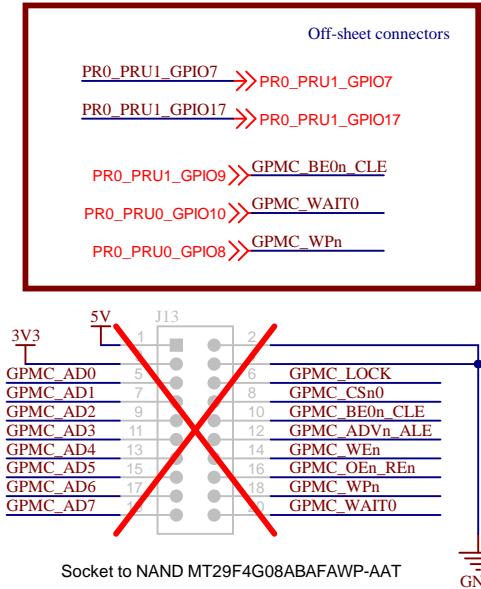
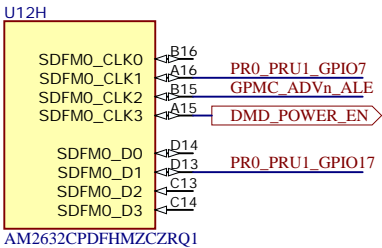
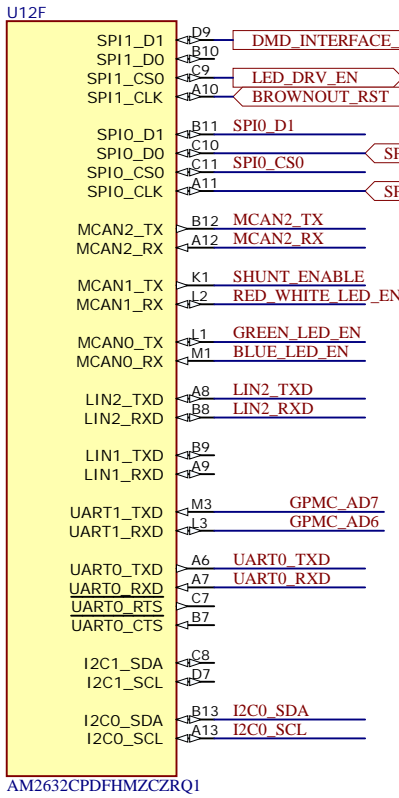
B

A

B

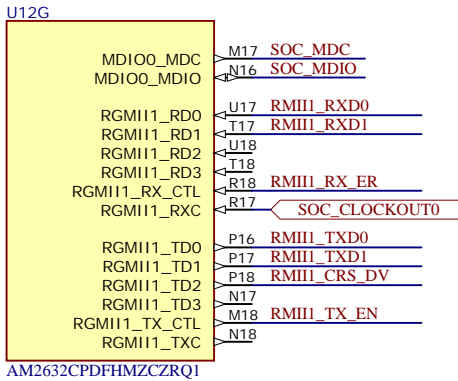


Raw ONFI NAND Daughtercard Socket



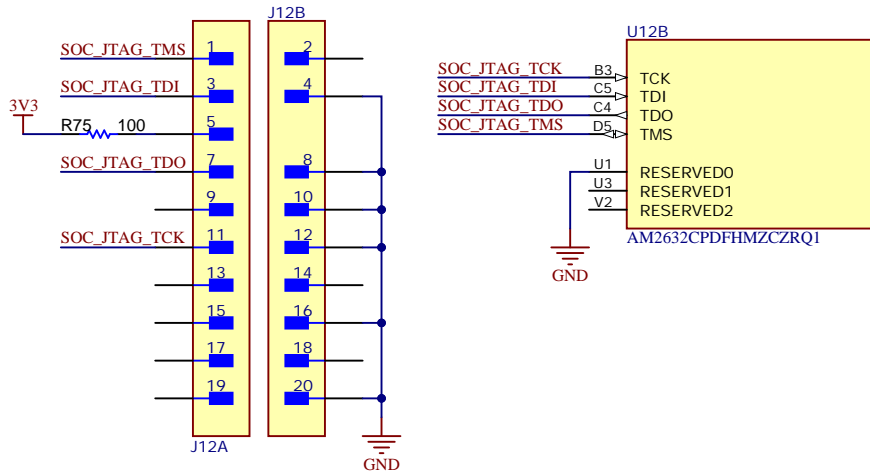
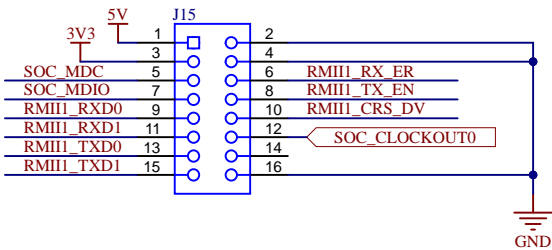
C

C



Socket for Ethernet RMII e.g. DP83TD510E (10BASE-T1L / 10BASE-T1S PHY shown only as example of AM263x expected connections)

Ethernet RMII Daughtercard Socket



D

D



