TPS628680A PSpice Transient Model Features and Limitations

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* Model Usage Notes:
* A. The following features have been modeled
*      a. RON and variation with VIN
*      b. Peak, Valley current limit
*      c. Output discharge functionality
*      d. Output voltage Programmability.
*      e. Power Save Mode or Forced PWM Mode.
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* B. Features have not been modeled
*      1. Operating Quiescent Current
*      2. Shutdown Current
*      3. Temperature dependent characteristics
*      4. SCL and SDA pin functionalities.
*      5. Ground pins have been tied to 0V internally. Therefore, this model cannot be used for inverting topologies.
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* C. Application Notes
*      1. The parameter STEADY_STATE has been used to reach the steady state faster.
*         Keep STEADY_STATE = 0 to observe startup behaviour
*         Keep STEADY_STATE = 1 for faster Steady state.
*      2. SOFTWARE_ENABLE= 0 - Disable the device. All registers values are still kept.
*         SOFTWARE_ENABLE= 1 - Re-enable the device with a new startup without the tDelay.
*      3. If ENABLE_FPWM_DURING_VOUT_CHANGE=1 and ENABLE_FPWM=0, and if the device goes from CCM to DCM,
*         128 cycles of FPWM is activated. After that the device goes to PFM.
*         If ENABLE_FPWM_DURING_VOUT_CHANGE= 0,then ENABLE_FPWM takes control.
*      4. The ramp speed is defined by VOUT_RAMP_SPEED(0->20mV/us,1->10mV/us,2->5mV/us,3->1mV/us)
*      5. ENABLE_HICCUP= 1 - Enable HICCUP, Disable latching protection.
*         ENABLE_HICCUP= 0 - Disable HICCUP. Enable latching protection.
*      6. When ENABLE_OUTPUT_DISCHARGE=1, VOUT discharges through Discharge Resistor.
*         Else discharge is only through load.
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