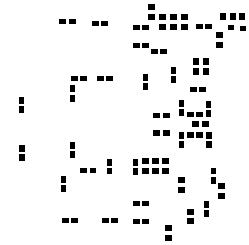
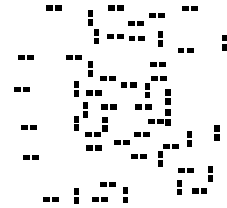
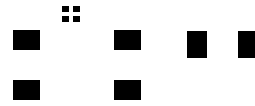


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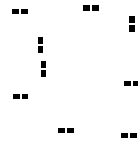
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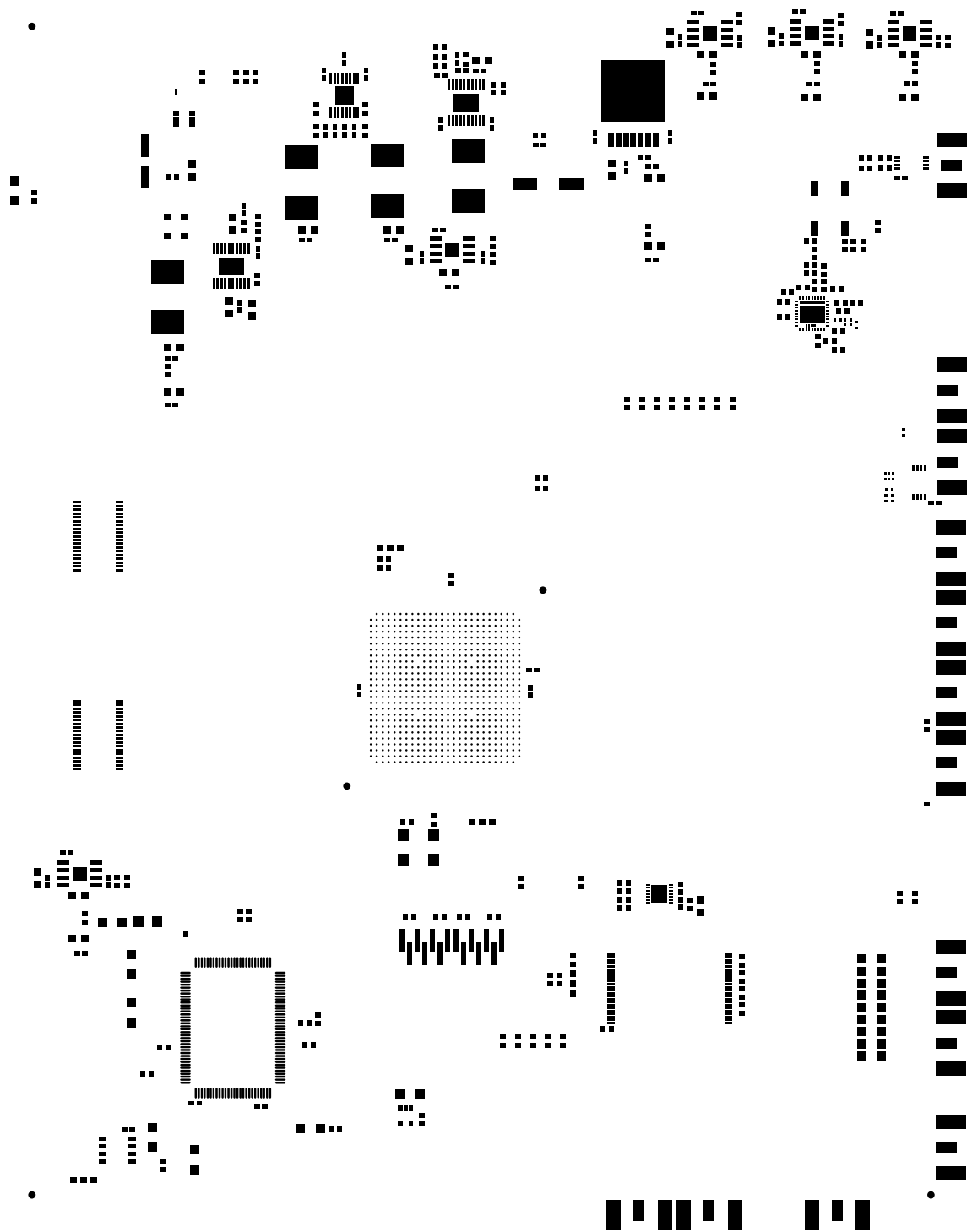


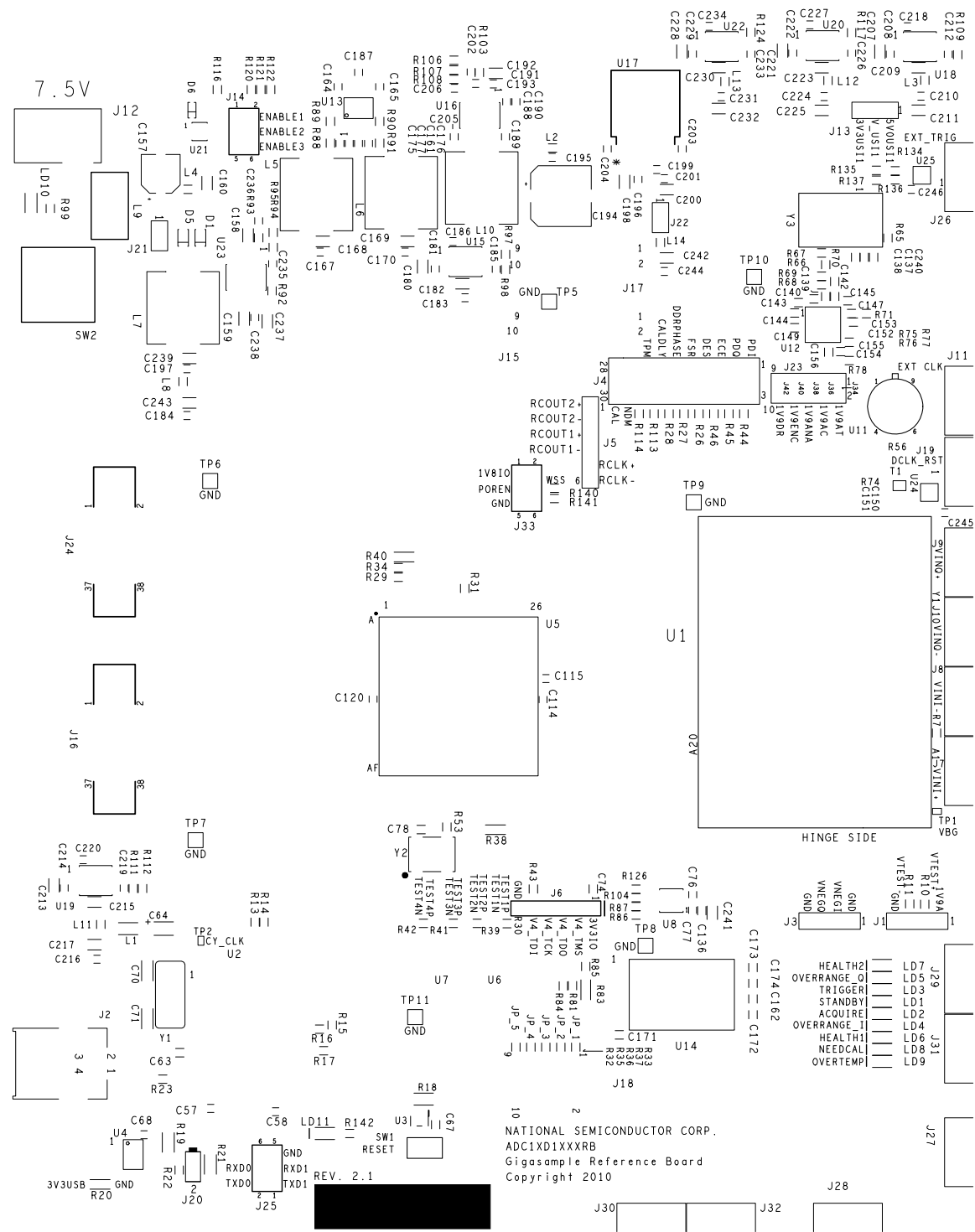
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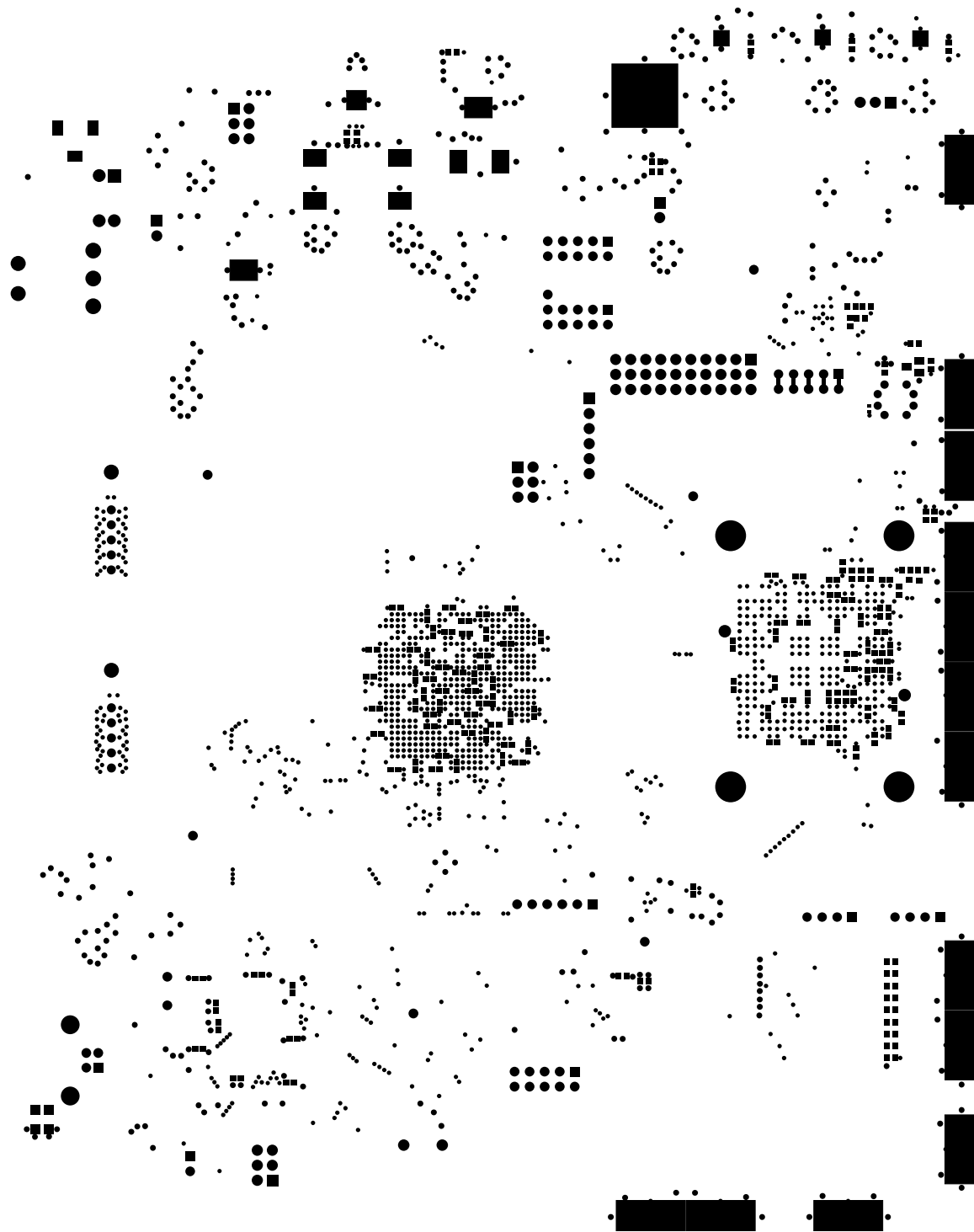


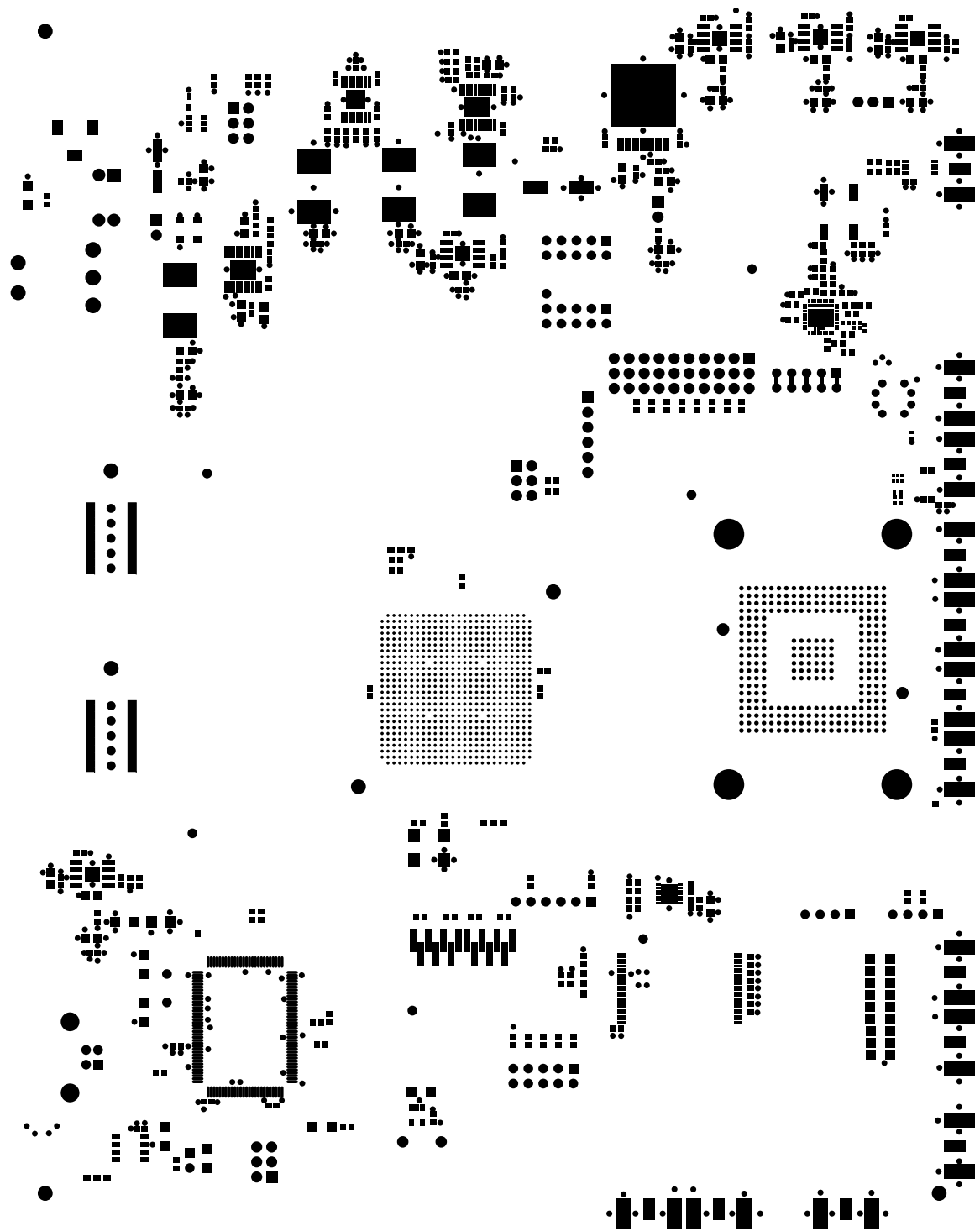


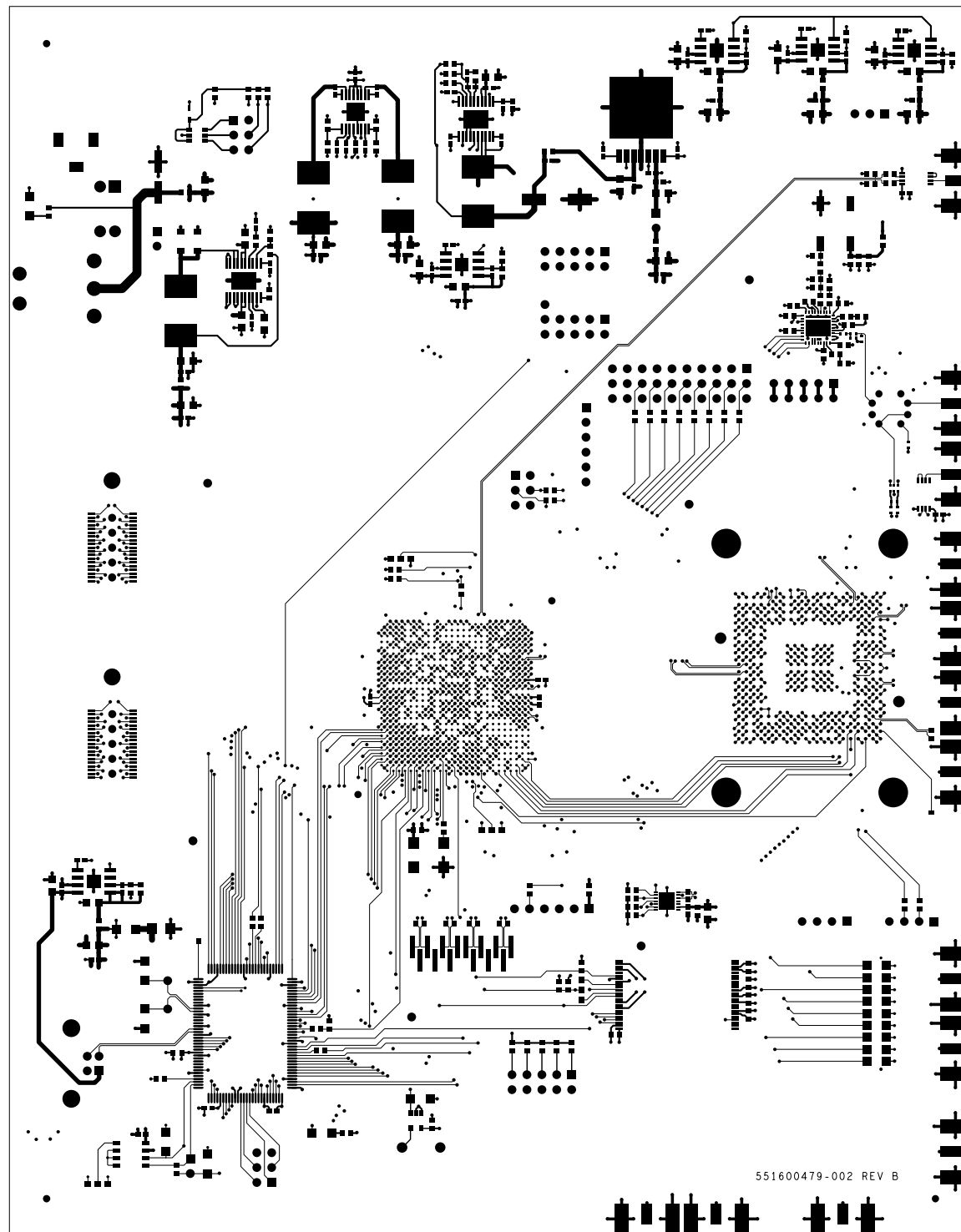


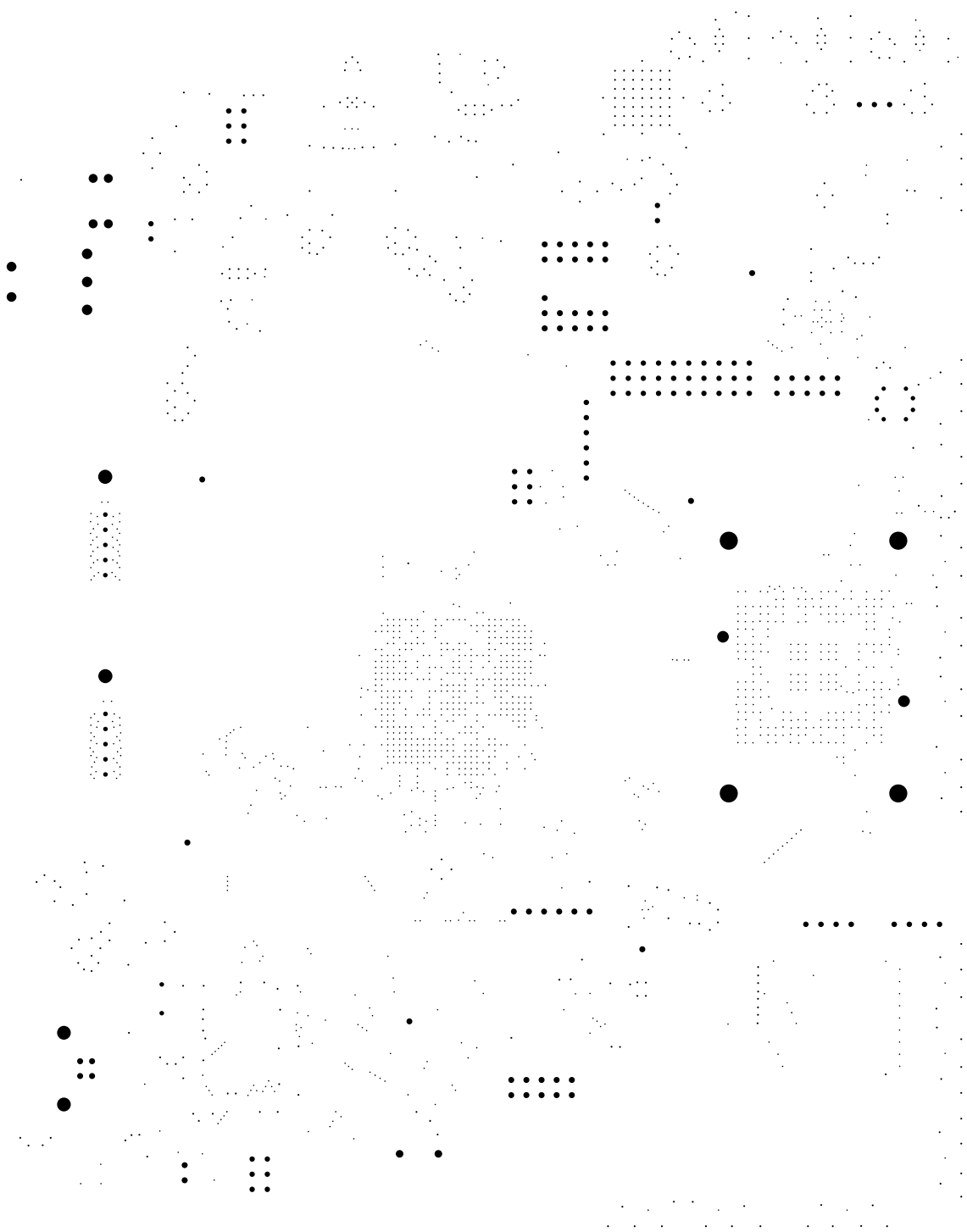
REV. 2.1

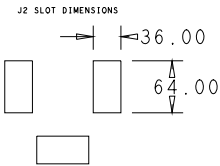
NATIONAL SEMICONDUCTOR CORP.
ADC1XD1XXXRB
Gigasample Reference Board
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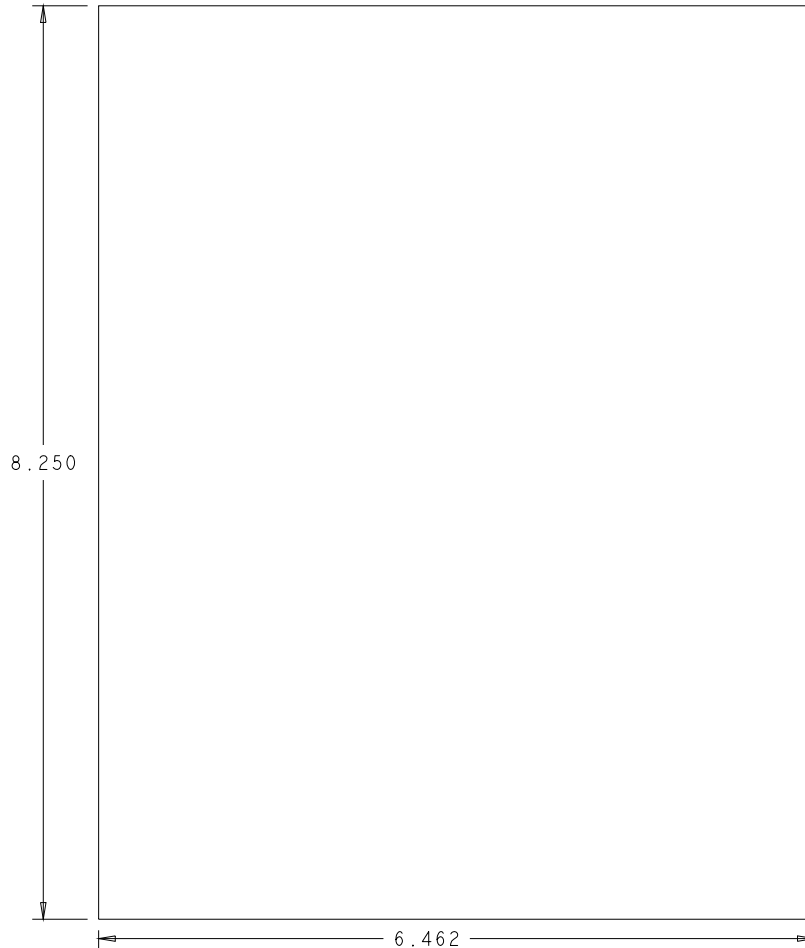








- FAB NOTES:
1. MATERIAL: NP 4000-6 UL 94V-0.
TOTAL MATERIAL THICKNESS OVER MASK: .062 INCHES +/- 10%
COPPER WEIGHT: 1 OZ INTERNAL LAYERS AND 1/2 EXTERNAL LAYERS.
 2. NUMBER OF LAYERS: 10
 3. COPPER PLATE HOLES WITH A MINIMUM OF .001 INCHES.
 4. FINISH: HARD (ELECTROLYTIC) NICKEL(150 MICRO INCHES) & GOLD BODY(20-30 MICRO INCHES) PLATED OVER COPPER SURFACE.
 5. GREEN SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE SOLDER MASK (LPI).
SOLDERMASK MAY BE MODIFIED TO HELP PREVENT BRIDGING ON FINE PITCH DEVICES.
 6. SILKSCREEN BOTH SIDES WITH WHITE EPOXY NON CONDUCTIVE INK.
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
 7. VENDOR MAY REMOVE ALL NON FUNCTIONAL PADS FROM THE INTERNAL SIGNAL LAYERS.
 8. LOCATE VENDOR MARKINGS AND DATE CODE ON BOTTOM SOLDER SIDE (OR BOTTOM SOLDERMASK).
 9. FREE FROM ANY METAL ENTITY.
 9. IMPEDANCE CONTROL SHALL BE AS FOLLOWS:
A. SEE STACKUP REPORT P22339A
 - VENDOR MAY MODIFY TRACE WIDTH AND DIELECTRIC HEIGHTS BY 20% WITHOUT WRITTEN APPROVAL.
 10. BARE BOARD ELECTRICAL TEST TO BE DONE WITH REFERENCE TO SUPPLIED NETLIST XXXX.TXT.
 11. IMPEDANCE REPORT, TEST CERTIFICATION AND CROSS SECTION REPORT TO ACCOMPANY EVERY LOT SHIPPED.
 12. PROVIDE LEAD FREE SYMBOL ON PCB.
 13. COPPER THIEVING PATTERN MAY BE ADDED ON LAYERS 1 AND 10 FOR PLATING UNIFORMITY.



LAYER INDICATOR

.062" +/- .006"
(NOM)

