ADC1xDxxxx(RF)RB Reference Board

REFERENCE DESIGN

Board ID:	SV600863
EVM Assembly	Variant
ADC10D1500RB	-001
ADC12D1600RB	-002
ADC12D1600RFRB	-003
ADC12D1800RB	-004
ADC12D1800RFRB	-005
ADC12D2000RFRB	-006
ADC12D800RFRB	-007

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

Texas Instruments reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.

Print Instructions:
- To create a readable printout, we recommend to use A3 or 11x17" paper size.
- When printing from this PDF file, make sure to check the "Shrink to fit" box.

PRELIMINARY

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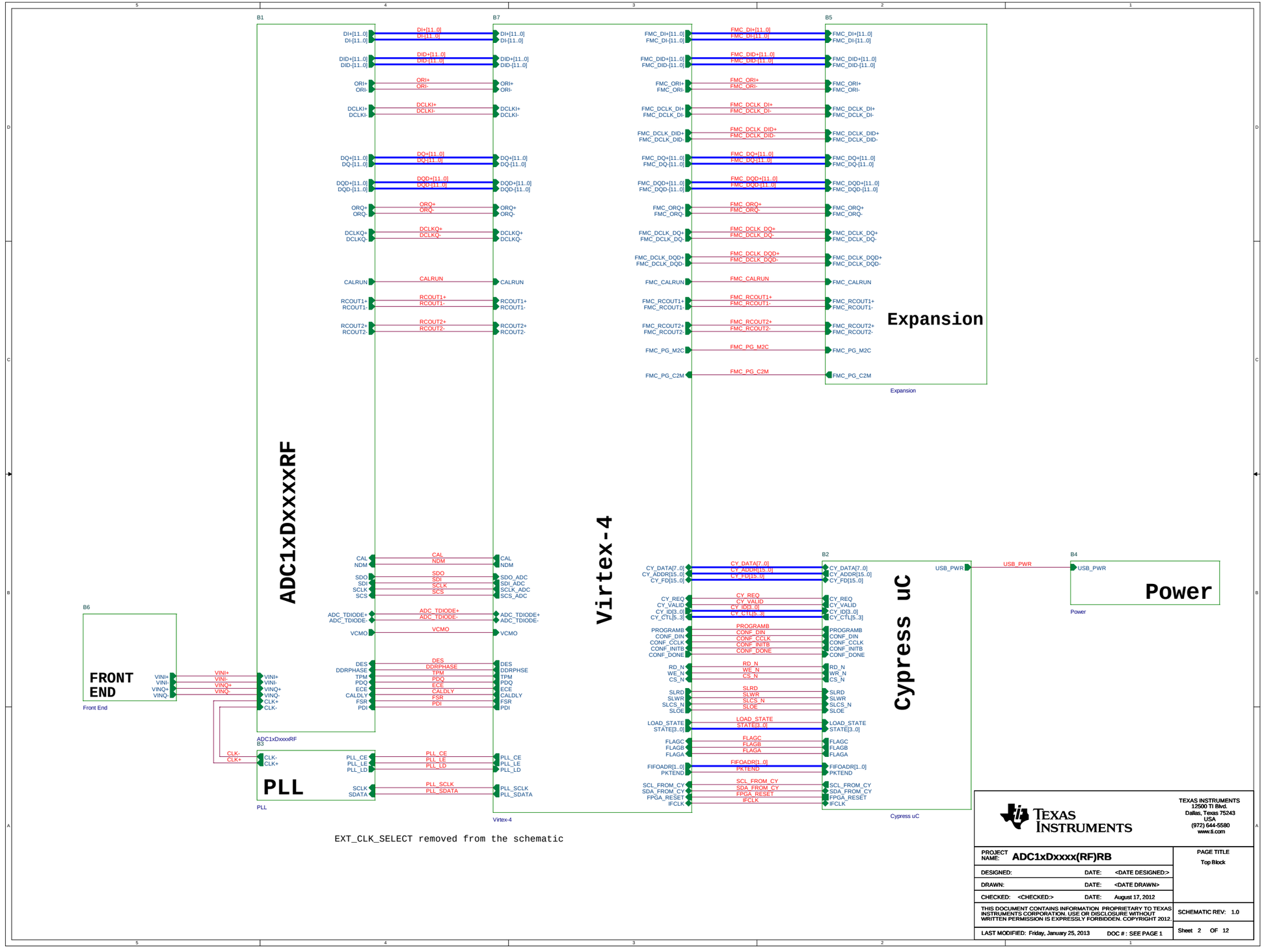
B1
B7
B5
ADC1xDXXXRF
Virtex-4
Expansion
Expansion
B6
FRONT END
Front End
ADC1xDxxxxRF
B3
PLL
PLL
Virtex-4
B2
Cypress uC
Cypress uC
B4
Power
Power
EXT_CLK_SELECT removed from the schematic
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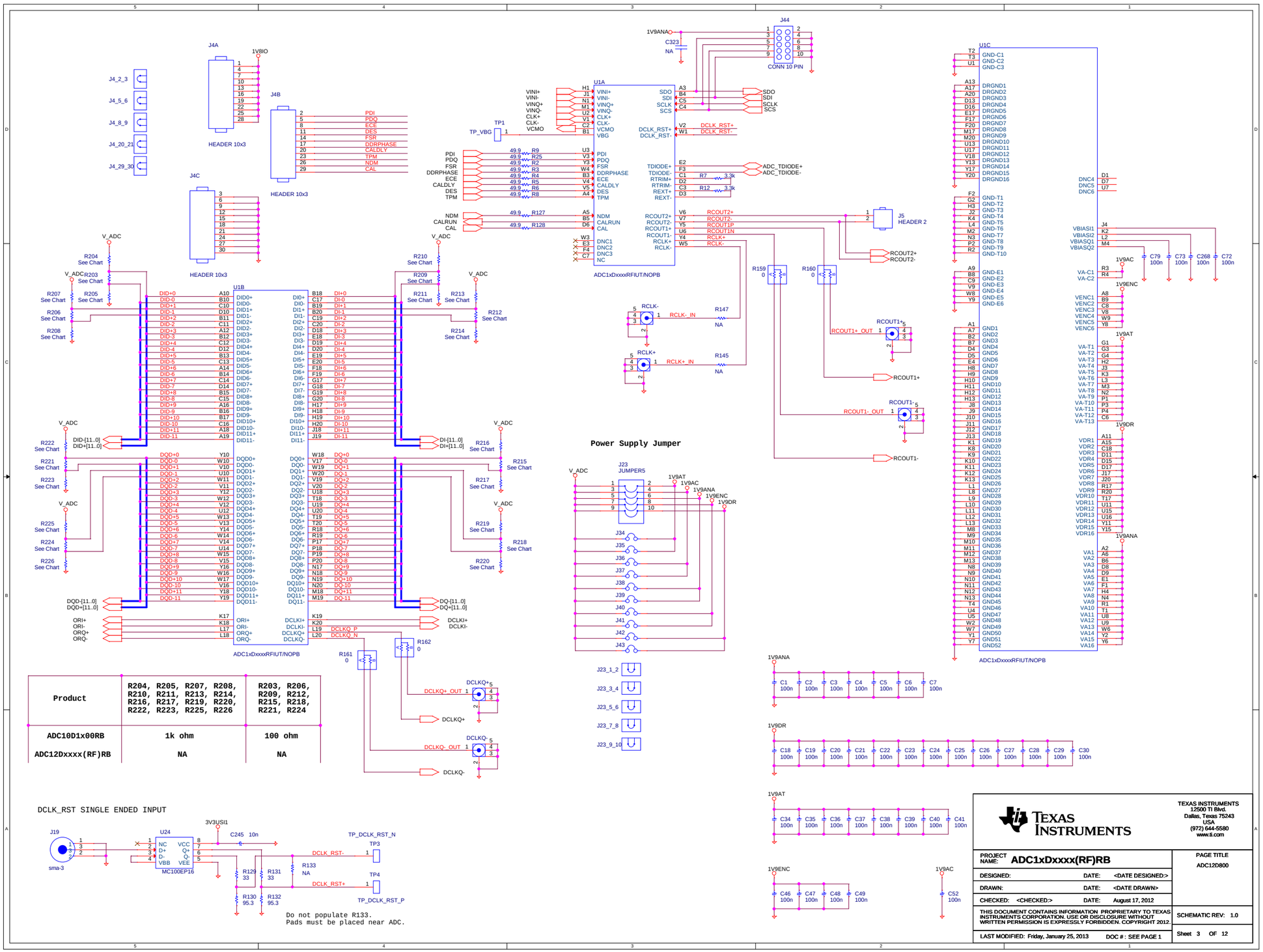

Product	R204, R205, R207, R208, R210, R211, R213, R214, R216, R217, R219, R220, R222, R223, R225, R226	R203, R206, R209, R212, R215, R218, R221, R224
ADC10D1x00RB	1k ohm	100 ohm
ADC12Dxxxx(RF)RB	NA	NA

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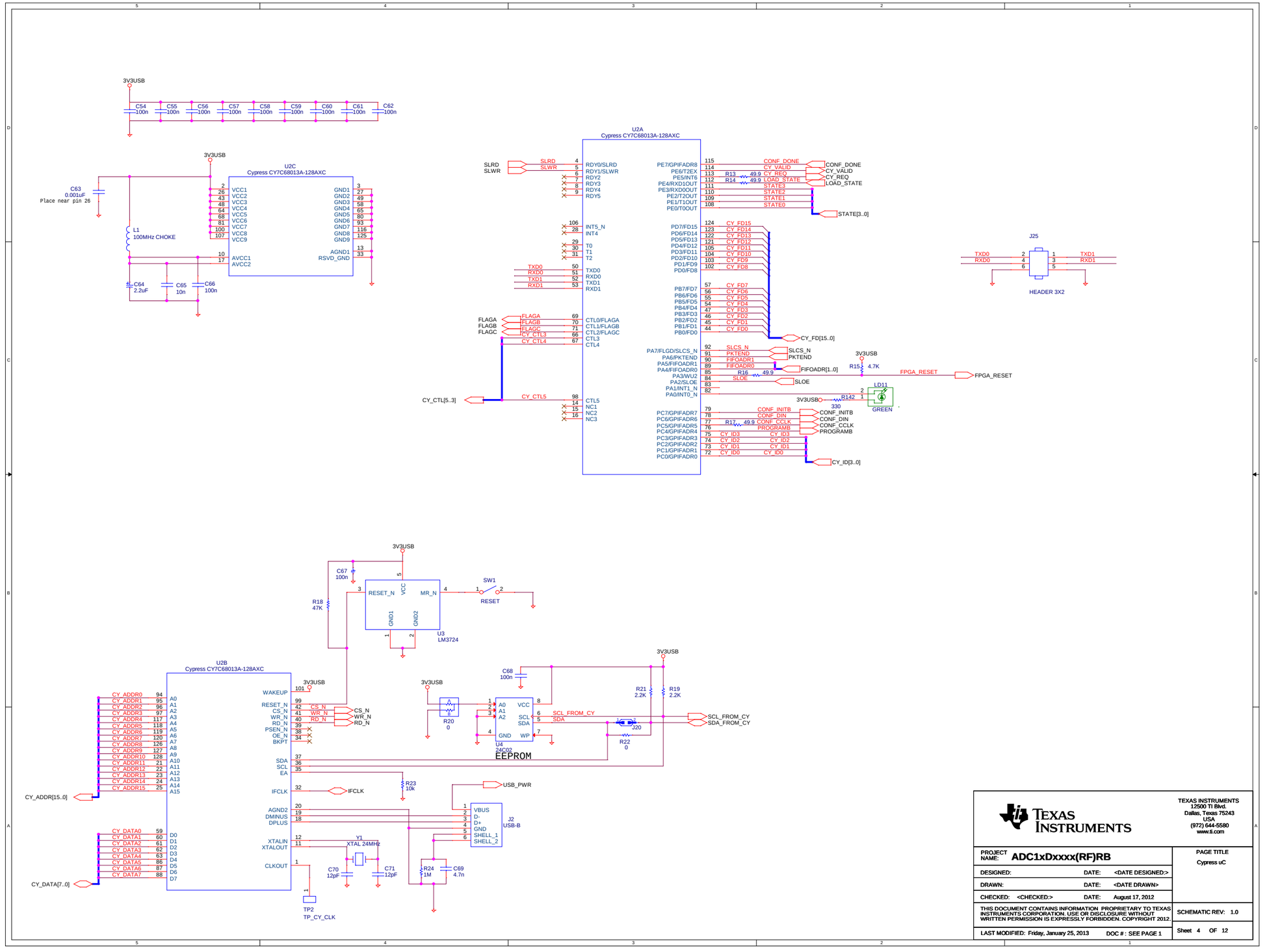

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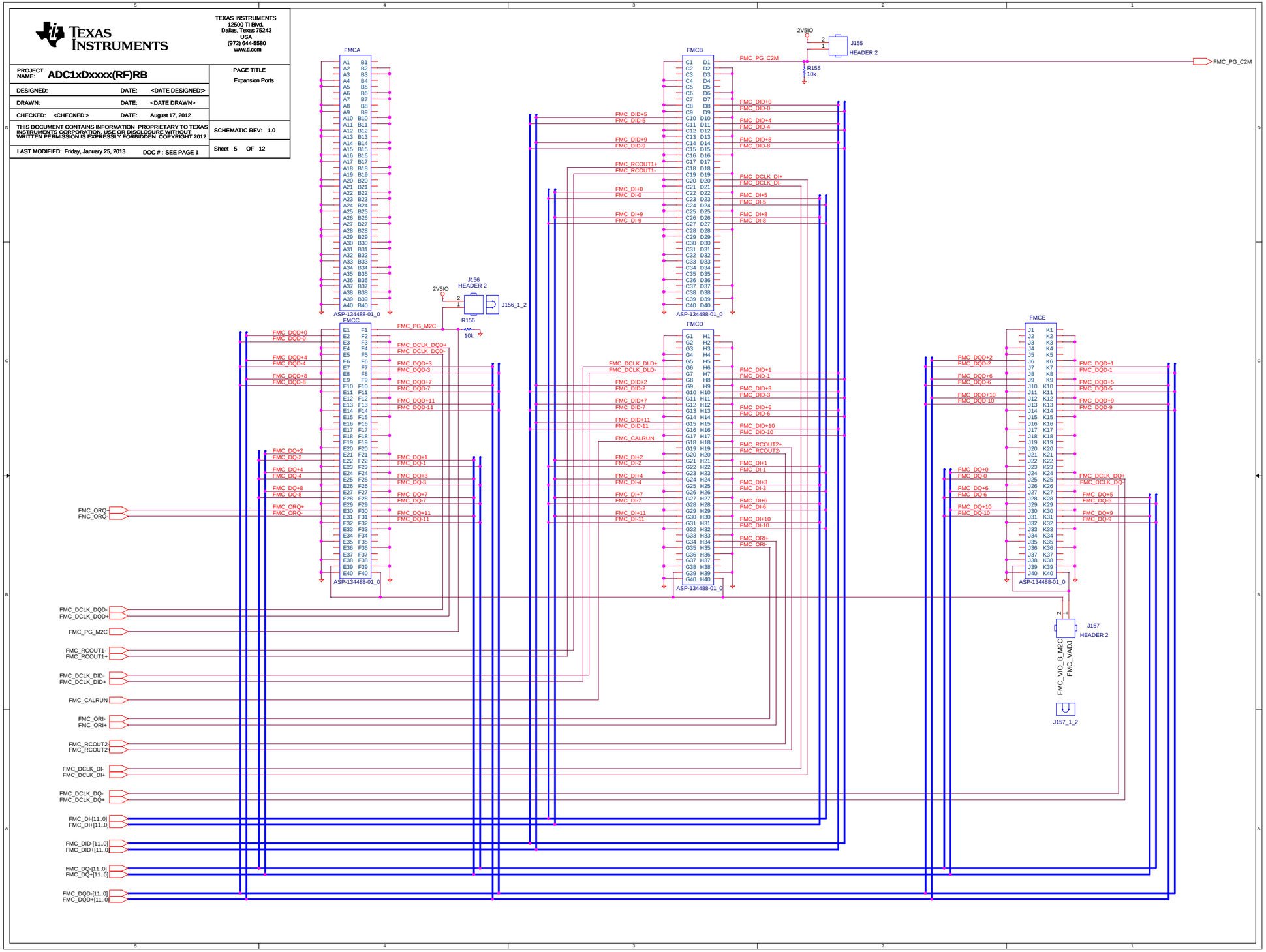

BANK 9 - 2.5 V I/O (LVDS)

U5J
XC4VLX25-11FFG668

DI+[11..0]
DI-[11..0]
DID+[11..0]
DID-[11..0]

ORI+
ORI-

FMC_RCOUT1+
FMC_RCOUT1-
FMC_RCOUT2+
FMC_RCOUT2-

BANK 5 - 2.5 V I/O (LVDS)

U5F
XC4VLX25-11FFG668

PLL_CE
PLL_LE

EXT_TRIG+
EXT_TRIG-

ORQ+
ORQ-
DQ+[11..0]
DQ-[11..0]
DQD+[11..0]
DQD-[11..0]

BANK 7 - 1.8 V I/O

U5H
XC4VLX25-11FFG668

PDI
PDQ
ECE
DES
FSR
DDRPHSE
CALDLY
TPM

SDI_ADC
SDO_ADC
NDM
SDI_ADC
SDO_ADC

CALRUN

SCS_ADC
SCLK_ADC

CAL

V_ADC
ADC_PWR

R58 1k
R59 10k

U5D
XC4VLX25-11FFG668

DCLKI+
DCLKI-
DCLKO+
DCLKO-
RCOUT1+
RCOUT1-
RCOUT2+
RCOUT2-

BANK 3 - 2.5V LVDS (GCLK)

U5I
XC4VLX25-11FFG668

FPGA_RESET
CS_N
WE_N
RD_N
FLAGA
FLAGB
FLAGC
CY_REQ
CY_VALID
SLCS_N
SLRD
SLWR
SLOE
PKTEND

7 LED_ECM_ENA
7 LED_RCOUT_ENA

CY_DATA[7..0]
CY_ID[3..0]
LOAD_STATE
FIFOADR[1..0]
CY_ADDR[15..0]
CY_FD[15..0]

BANK 8 - 3.3 V I/O

FMC_DQD+[11..0]
FMC_DQD-[11..0]
FMC_ORQ+
FMC_ORQ-
PLL_SDATA
PLL_SCLK
FMC_DCLK_DQD+
FMC_DCLK_DQD-
FMC_CALRUN
PLL_LO
FMC_DCLK_DQ+
FMC_DCLK_DQ-
FMC_DQ+[11..0]
FMC_DQ-[11..0]

U5G
XC4VLX25-11FFG668

BANK 6 - 2.5V I/O

J26
sma-3

U25
MC100EP16
3V3USI1
C246 10n
R134 33
R136 33
R135 95.3
R137 95.3

EXT_TRIG-
EXT_TRIG+

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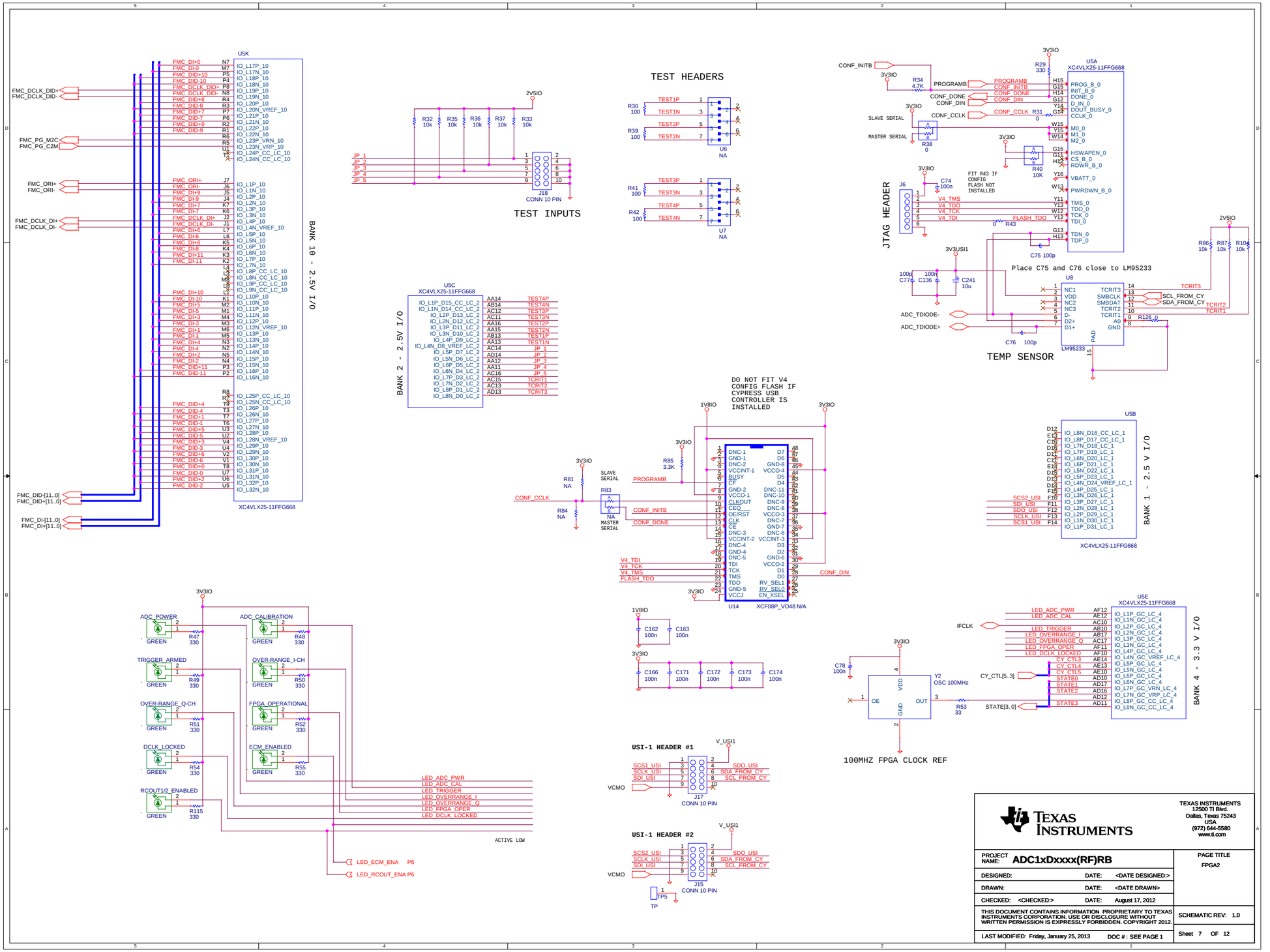

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BANK #	BANK SUPPLY	INTERFACE
1	2V5IO	USI-1 Header
2	2V5IO	Test Headers, Temp. Sensor
3	2V5IO	ADC DCLK
4	3V3IO	Cypress, LEDs, 100 MHz oscillator
5	2V5IO	ADC Q-Channel (LVDS)
6	2V5IO	Clock generator
7	1V8IO	ADC Control
8	3V3IO	Cypress, LEDs
9	2V5IO	ADC I-Channel (LVDS)
10	2V5IO	Logic Analyzer Header

U5L
XC4VLX25-11FFG668

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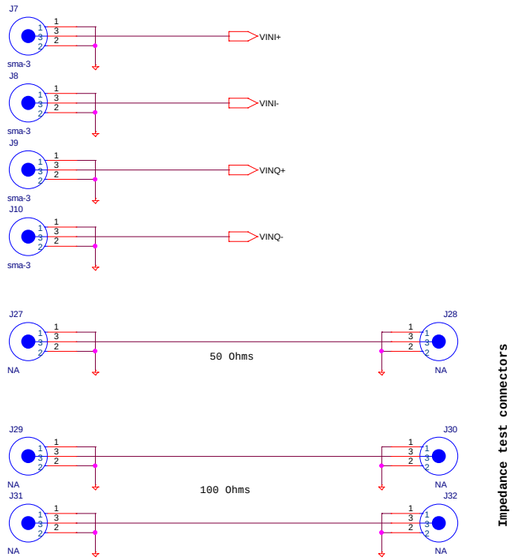

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Product	Frequency	Clock part no.	Loop filter component values		
			R2_LF (ohm)	C1_LF (nF)	C2_LF (nF)
ADC10D1500	1500 MHz	LMX2541SQ3030E	820	0.039	3.3
ADC12D800RF	800 MHz	LMX2541SQ3320E	680	0.047	3.9
ADC12D1600/1600RF	1600 MHz	LMX2541SQ3320E	680	0.047	3.9
ADC12D1800/1800RF	1800 MHz	LMX2541SQ3740E	680	0.047	3.9
ADC12D2000RF	2000 MHz	LMX2541SQ2060E	820	0.22	2.7

LMX2541 clock part number and loop filter component values are different based on clock frequency. Please refer to the table above for correct clock part number and loop filter components.

LAYOUT NOTE: FOR CLOCK ROUTING DO NOT USE VIAS (LMX2541 RFOUT, EXT CLK) ALL THE WAY TO VIAS AT SOCKET EDGE. AVOID STUBS AND CHOOSE SERIES COMPONENTS TO BE 0402 SIZE WHERE POSSIBLE.

LAYOUT NOTE: Use as short traces as possible from LMX2541-RFout (pin 36) and External Clock Input to VIAs at socket edge

LAYOUT NOTE: FOR CLOCK ROUTING DO NOT USE VIAS (LMX2541 RFOUT, EXT CLK) ALL THE WAY TO VIAS AT SOCKET EDGE. AVOID STUBS AND CHOOSE SERIES COMPONENTS TO BE 0402 SIZE WHERE POSSIBLE.

GROUP JUMPERS TOGETHER ON BOARD LAYOUT

GROUP JUMPERS TOGETHER ON BOARD LAYOUT

EXTERNAL CLOCK INPUT

U27 LMX2541SQxxxxE

Y6 N/A

Y7 CVHD-950-100.000

B0430J50100AHF

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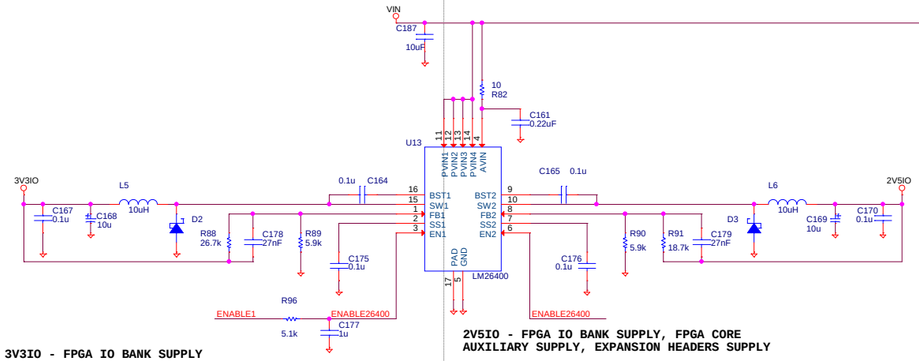
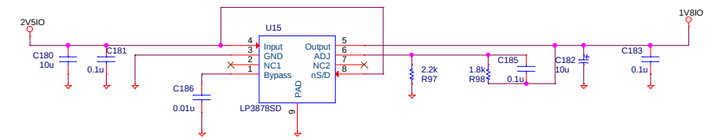
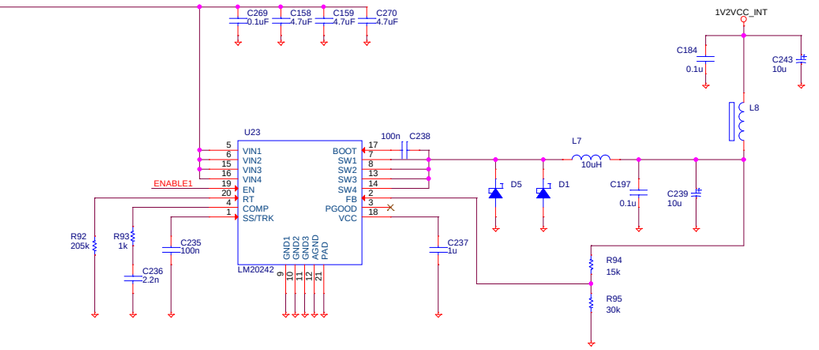


3V3IO - FPGA IO BANK SUPPLY

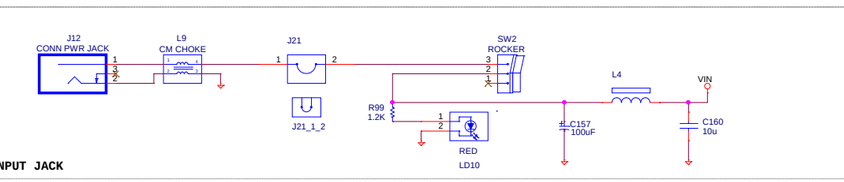
2V5IO - FPGA IO BANK SUPPLY, FPGA CORE AUXILIARY SUPPLY, EXPANSION HEADERS SUPPLY



1V8IO - ADC IO SUPPLY, FPGA IO BANK SUPPLY



1V2VCC_INT - FPGA CORE SUPPLY



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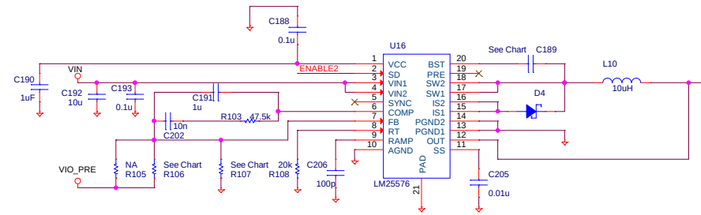
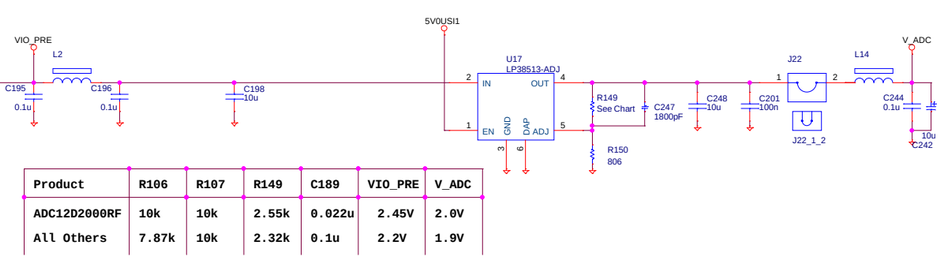
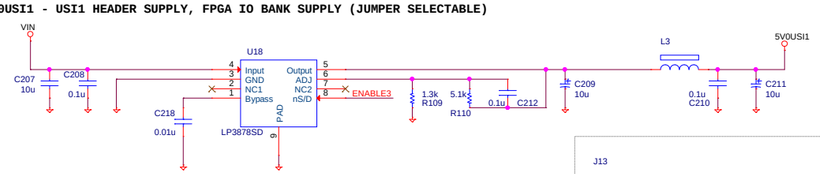


2V2IO/2V_PRE - NOT USED (INTERMEDIATE SUPPLY ONLY)

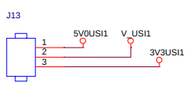


ADC ANALOG SUPPLY

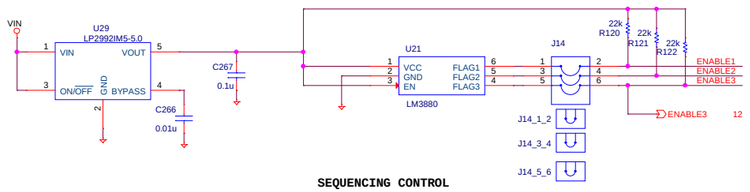
Product	R106	R107	R149	C189	VIO_PRE	V_ADC
ADC12D2000RF	10k	10k	2.55k	0.022u	2.45V	2.0V
All Others	7.87k	10k	2.32k	0.1u	2.2V	1.9V



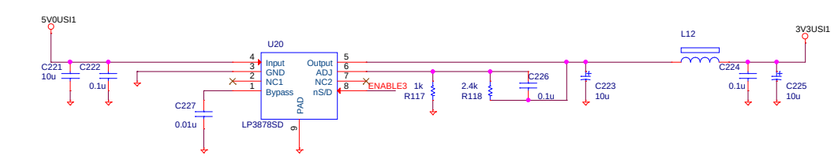
5V0USI1 - USI1 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)



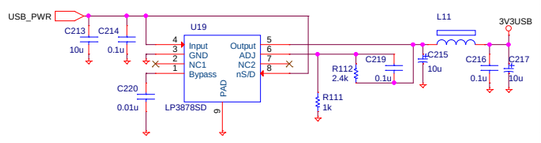
MAIN USI1 SUPPLY SELECTION



SEQUENCING CONTROL



3V3USI1 - USI1 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)



3V3USB - CYPRESS uC & EEPROM USB SUPPLY

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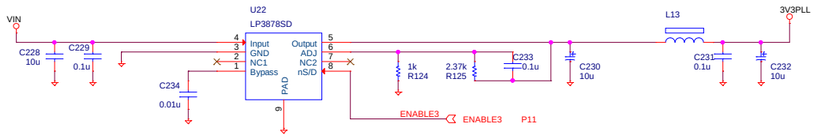

3V0PLL - LMX2541 CLOCK GENERATOR SUPPLY

TP6 TP7 TP8 TP9 TP10 TP11

BOARD MOUNTING HOLES

MT1 MT2 MT3 MT4 MT5

HOLES FOR FMC CONNECTOR

FMC1 FMC2

H2 H3 H4 H5 H6 — MECH — Rubber Feet

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