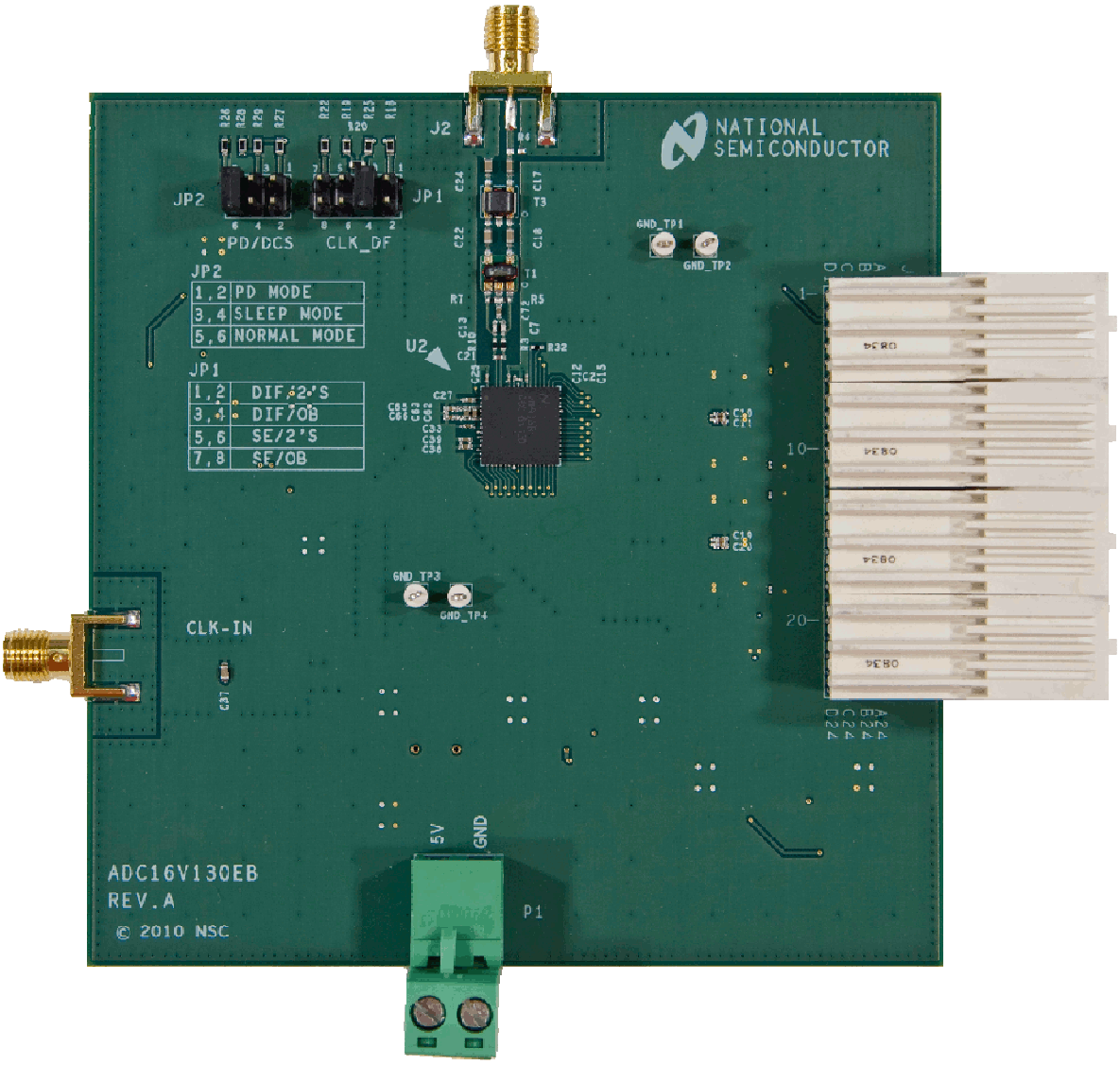
ADC16V130 Evaluation Board
16-bit, 130 MSPS Analog to Digital Converter

User's Guide



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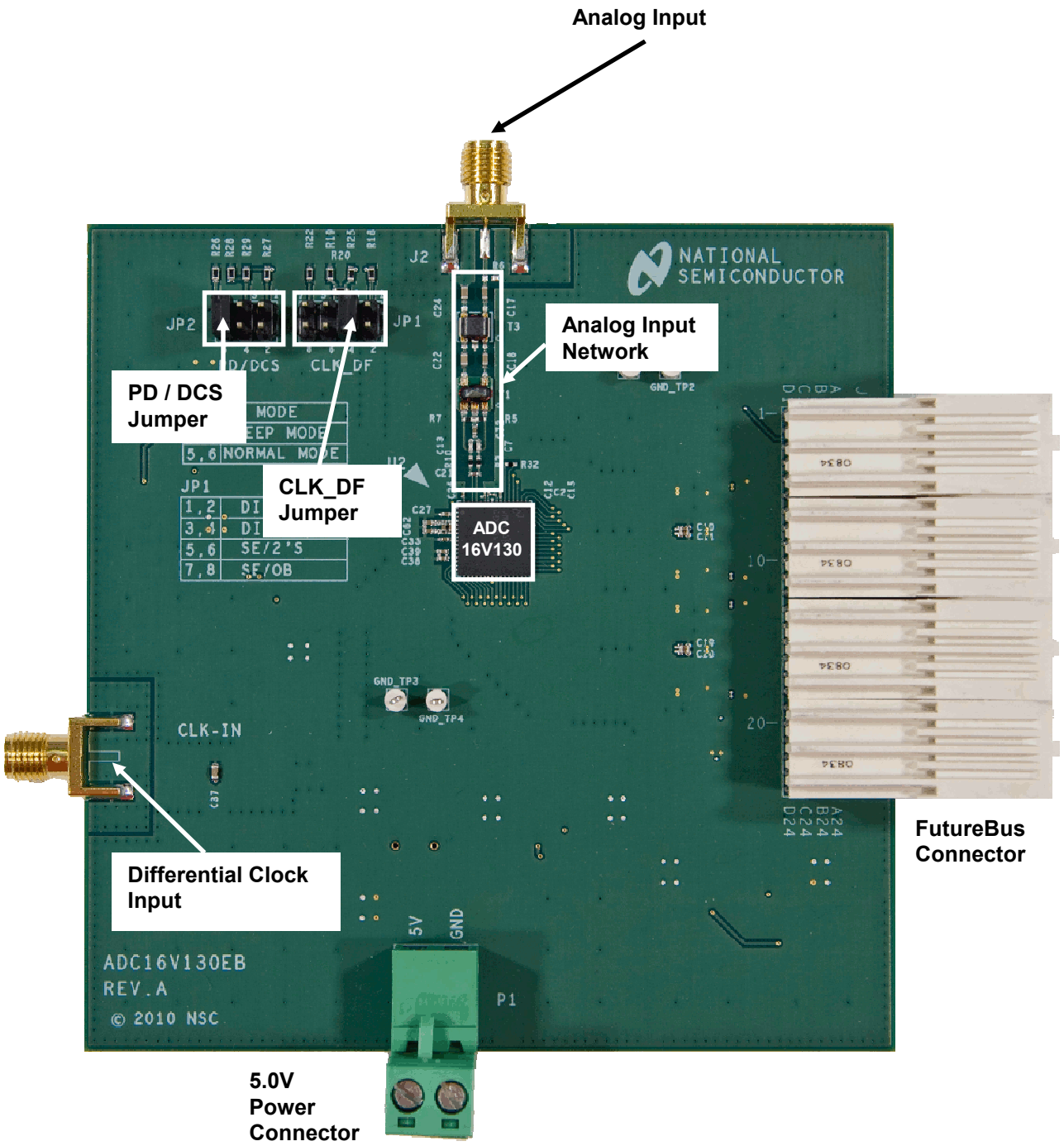

Figure 1a. ADC16V130 (Front) Component, Connector and Jumper Locations

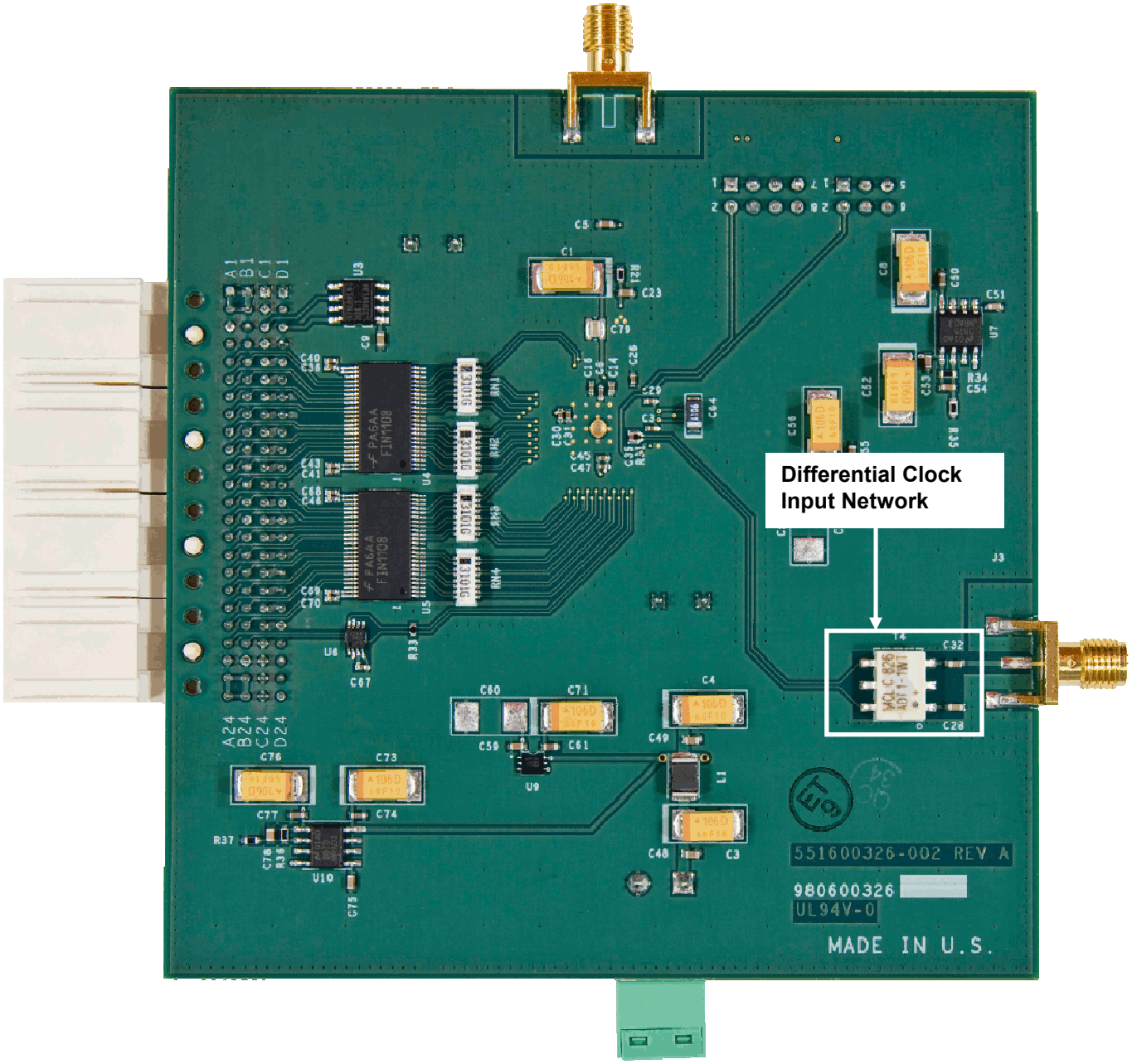

Figure 1b. ADC16V130 (Back) Component, Connector and Jumper Locations

1.0 Introduction

The ADC16V130 Evaluation Board is designed to support the ADC16V130 16-bit 130 Mega Sample Per Second (MSPS) Analog to Digital Converter.

2.0 Data Capture

The digital data from the ADC16V130 reference design board can be captured with a suitable instrument such as a logic analyzer or with National Semiconductor's WaveVision signal path data acquisition hardware and software platform. The ADC16V130 board can be connected to the data acquisition hardware through the FutureBus connector.

The ADC16V130 is compatible with National Semiconductor's WaveVision 5.1 Signal Path Digital Interface Board and associated WaveVision software. Please note that the ADC16V130 board is not compatible with previous versions of the WaveVision hardware (WaveVision 4.x Digital Interface Boards).

The WaveVision hardware and software package allows fast and easy data acquisition and analysis. The WaveVision hardware connects to a host PC via a USB cable and is fully configured and controlled by the latest WaveVision software. The WaveVision 5.1 Signal Path Digital Interface hardware is available through the National Semiconductor website (part number: WAVEVSN 5.1).

3.0 Board Assembly

Each evaluation board from the factory is configured for differential clock operation and is populated with an analog input network which has been optimized for analog input frequencies less than 160 MHz. Please refer to the input circuit configuration described in the Analog Input Section (5.2) of this guide.

The location and description of the components on the ADC16V130 evaluation board can be found in Figure 1 as well as Section 6.0 (Schematic) and Section 8.0 (Bill of Materials) of this user's guide.

4.0 Quick Start

4.1 WaveVision Software and Hardware Installation

⚠ The WaveVision software must be installed before connecting the WaveVision hardware.

1. Begin by installing the latest version of the WaveVision software which is on the web at http://www.national.com/analog/adc/wavevision5. Do not start the WaveVision software application at this point.
2. Connect the WaveVision 5.1 Digital Interface Board to your PC through the supplied USB cable and apply power to the WaveVision 5.1 board through the +12V AC-DC power adapter included in the WaveVision 5.1 kit. The connection diagram is shown in Figure 2.
3. If this is the first time connecting a WaveVision 5.1 board to your PC, follow the on-screen instructions for installing the drivers for the hardware.
4. Once the WaveVision software and hardware have been installed, the WaveVision software application can be opened.

For more information on installing the WaveVision data acquisition hardware or software, please refer to the Quick Start Guide in the WaveVision User's Guide which can be found on the National Semiconductor website (http://www.national.com/appinfo/adc/evalboards_dataccapture.html).

Please note that the ADC16V130 is only compatible with National Semiconductor's WaveVision 5.1 Digital Interface board.

4.2 Evaluation Board Jumper Positions

The ADC16V130 board jumpers should be configured as follows. Please refer to Figures 1a and 1b for the exact jumper locations.

1. The **PD/DCS jumper** places the ADC16V130 into either power-down, sleep mode or normal mode. Previous version of the ADC16V130EB also gave control over the internal Duty Cycle Stabilizer (DCS) feature of the ADC16V130 but this feature is no longer accessible. Table 1 below shows how to select between the power-down modes.

PD/DCS Jumper Setting	Power Mode
1-2	Power Down
3-4	Sleep
5-6*	Normal

* As assembled from factory.

Table 1. PD/DCS Selection Table

2. The **CLK_DF jumper** selects the output data format (2's complement or offset binary) and clock mode (single-ended or differential). Table 2 below shows how to select between the clock modes and output data formats. The ADC16V130 evaluation board is delivered with the ADC16V130 configured for differential clock operation and Offset Binary output data format (Jumper 3-4).

CLK_DF Jumper Setting	Clock Mode	Output Data Format
1-2	Differential	2's Complement
3-4*	Differential	Offset Binary
5-6	Single-Ended	2's Complement
7-8	Single-Ended	Offset Binary

* As assembled from factory.

Table 2. CLK_DF Selection Table

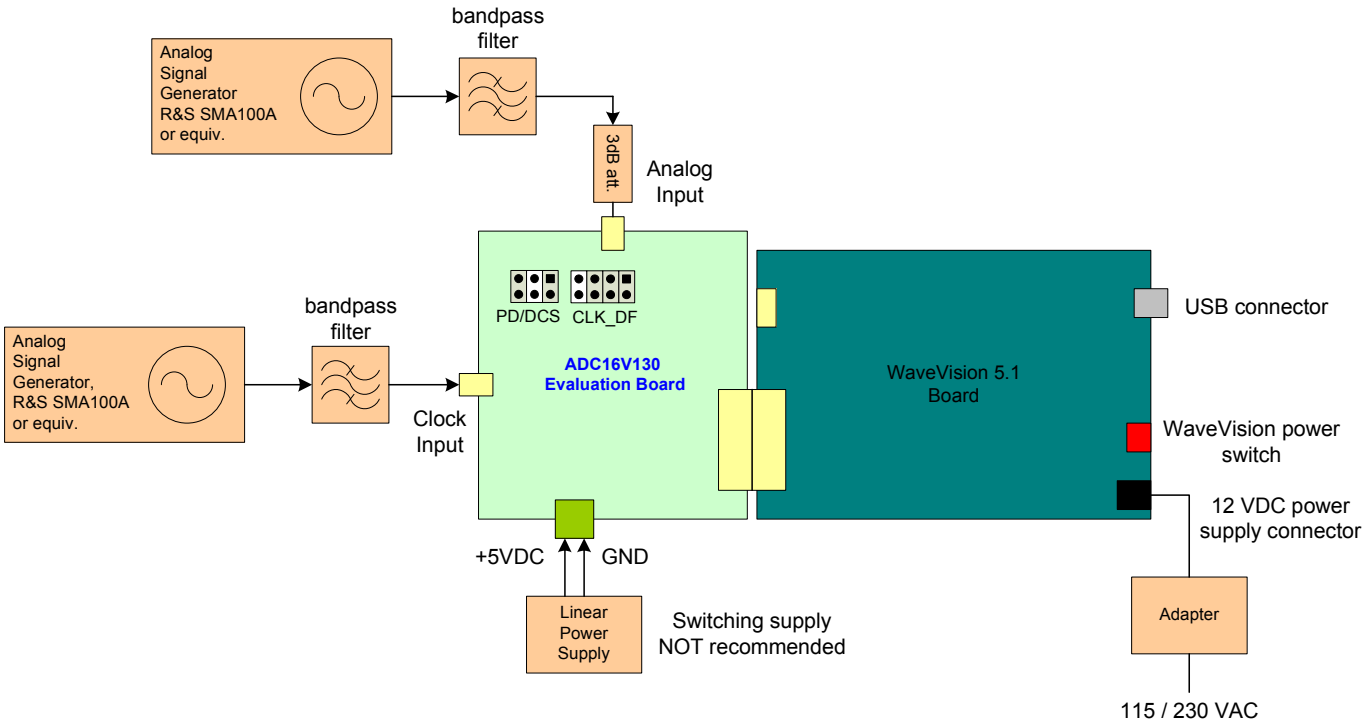

Figure 2. Connection Diagram for ADC16V130EB and WaveVision 5.1 Data Capture Hardware

4.3 Connecting Power and Signal Sources

1. With the WaveVision software running, power-up the WaveVision 5.1 board.
2. Connect the ADC16V130 reference board to the WaveVision 5.1 board through the FutureBus connector as shown in Figure 2. The ADC16V130 evaluation board should not be powered up, as the WaveVision hardware does not support hot-swapping of boards.
3. Connect a 5.0V power supply capable of supplying up to 500mA to the green power connector which is located along the bottom edge of the ADC16V130 board. This is shown in Figure 2. Ensure that the polarity of the wires going to the green power connector match the "+5V" and "GND" labels in Figure 2 above. Turn on the 5V supply.
4. Connect the signal source through the "INPUT" SMA connector and the clock source through the "CLK_DIFF" SMA connector as shown in Figure 1a and Figure 2. Recommended signal generators are the HP8644B (HP/Agilent) or the SMA100A (Rohde & Schwarz). A bandpass filter between the signal generator outputs and the ADC16V130EB SMA connectors is required to measure the true performance of the ADC16V130. A 3 dB attenuator is also recommended between the Analog Input SMA connector and bandpass filter. See Figure 2.
5. Set the analog input source and clock source frequencies and amplitudes to the desired values. The analog input signal generator amplitude will need to be adjusted during evaluation to obtain the desired signal amplitude at the ADC input.
6. In the WaveVision software, click the Reset Hardware button to get the WaveVision software to load the appropriate firmware to allow data capture from the ADC16V130. The ADC16V130EB may also be detected automatically by the software.
7. Capture the data and display the FFT of the captured data with the WaveVision software.

5.0 Functional Description

5.1 Clock Input

The ADC16V130 can accept either a single-ended or a differential clock input. The ADC16V130 evaluation board has a single ended clock input but converters the clock to a differential signal using a flux transformer (Mini-Circuits ADT1-1WT+) to provide a differential clock to the ADC16V130.

To achieve the best noise performance (best SNR), a low jitter clock source with total additive jitter less than 150 fs should be used. A low jitter crystal oscillator is recommended, but a sinusoidal signal generator with low phase noise, such as the SMA100A from Rohde & Schwarz or the HP8644B (discontinued) from Agilent / Hewlett Packard, can also be used with a slight

degradation in the noise performance. The clock signal generator amplitude is typically set to +16.0 dBm to produce the highest possible slew rate. When using a low phase noise clock source, the SNR is primarily degraded by the broadband noise of the signal generator. Placing a bandpass filter between the clock source and the clock input SMA connector will further improve the noise performance of the ADC by filtering out the broadband noise of the clock source. All results in the ADC16V130 datasheet are obtained with a tunable bandpass filter made by Trilithic, Inc. in the clock signal path.

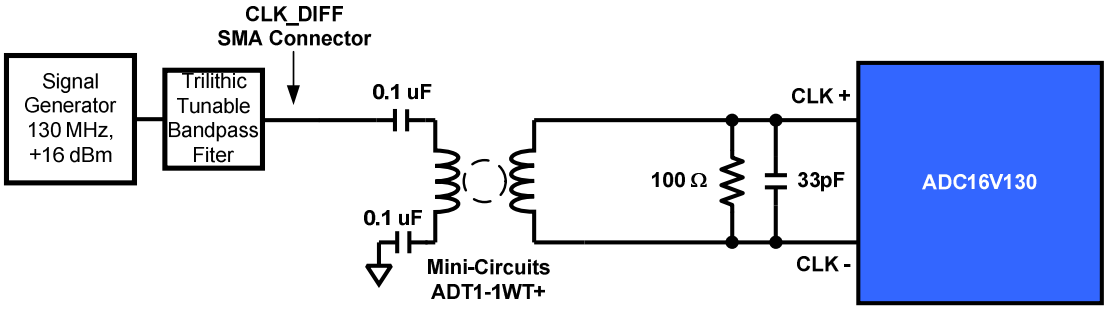

Figure 3a. Clock Input Circuit for Differential Clock Mode (as assembled from factory)

5.2 Analog Input

To obtain the best distortion results (best SFDR), the analog input network on the evaluation board must be optimized for the signal frequency being applied.

The ADC16V130 evaluation board is delivered from the factory with the analog input network optimized for analog input frequencies less than 160 MHz. The component values on the board as assembled are shown in Figure 4 below. The 22pF differential capacitor and 10pF capacitors to ground act as a low pass filter with a corner frequency of approximately 160 MHz. To allow input signals greater than 160 MHz to pass through un-attenuated, the circuit in Figure 4 can be modified by reducing the size of the capacitors at the input of the ADC16V130.

A low noise signal generator such as the HP8644B is recommended to drive the signal input of the ADC16V130 evaluation board. The output of the signal generator must be filtered to suppress the harmonic distortion produced by the signal generator and to allow accurate measurement of the ADC16V130 distortion performance. A low pass or a bandpass filter is recommended to filter the analog input signal. In some cases, a second low pass filter may be necessary. The bandpass filter on the analog input will further improve the noise performance of the ADC by filtering the broadband noise of the signal generator. Data shown in the ADC16V130 datasheet was taken with a tunable bandpass filter made by Trilithic in the analog signal path.

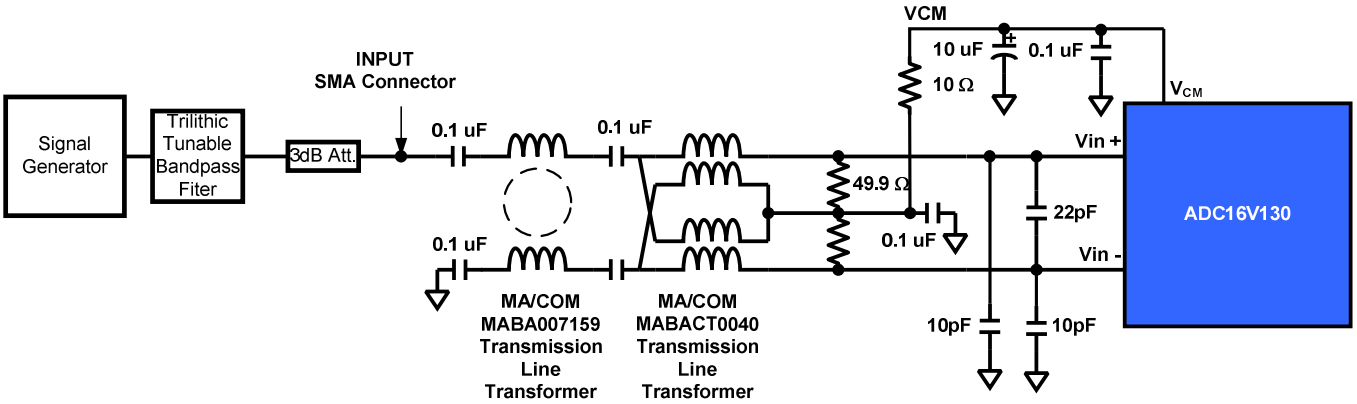

Figure 4. ADC16V130 Analog Input Circuit (as assembled from factory)

5.3 ADC Reference

The internal 1.2V reference on the ADC16V130 is used to acquire all of the results in the ADC16V130 datasheet. It is recommended to use the internal reference on the ADC16V130. However, if an external reference is required, the ADC16V130 is capable of accepting an external reference voltage of 1.2V or less.

It is recommended to use the voltage at the V_{CM} pin (pin 58) of the ADC16V130 to provide the 1.15V common mode voltage required for the differential analog inputs V_{IN+} and V_{IN-}. The ADC16V130 evaluation board is factory-assembled with V_{CM} connected to the transformer center-tap through a 10Ω resistor and the center tap of the second casecaded transformer (MA/COM MABACT0040) to provide the necessary common mode voltage to the differential analog input.

5.4 Board Outputs

The digitized 16-bit output word from the ADC16V130 evaluation board is presented in parallel LVDS format. The digital output from the ADC16V130 evaluation board consists of 36 lines which are arranged into 18 LVDS pairs. These 18 pairs of lines carry the 16-bit output data (16 pairs), the Data Clock Out signal (OUTCLK+/-) which should be used to capture the output data (1 pair) and the Data Over-Range bit (OR+/-) which indicates that the digital output has exceeded the maximum digitizable signal (1 pair).

The 16-bit digital output word is available on the FutureBus connector at pins A5/B5 (MSB +/-) through A12/B12 and A14/B14 through A21/B21 (LSB +/-) of the FutureBus connector. The DRDY signal which should be used to capture the digital data is also in LVDS format and it is available at pins A13/B13 (OUTCLK +/-) on the FutureBus connector. The rising edge of the OUTCLK signal should be used to capture the digital data from the ADC16V130. The over-range bit (OR) is not available on the FutureBus connector, but it can be measured on the evaluation board across resistor R32 on the top side of the board.

Please see the Evaluation Board schematic in Section 6.0 and the ADC16V130 datasheet for further details.

5.5 Power requirements

Power to the ADC16V130 evaluation board is supplied through the green power connector labeled "+5V" which is located along the left edge of the board. Voltage and current requirements are:

- +5V capable of providing up to 500mA (ADC16V130 evaluation board only)

6.0 Evaluation Board Schematic

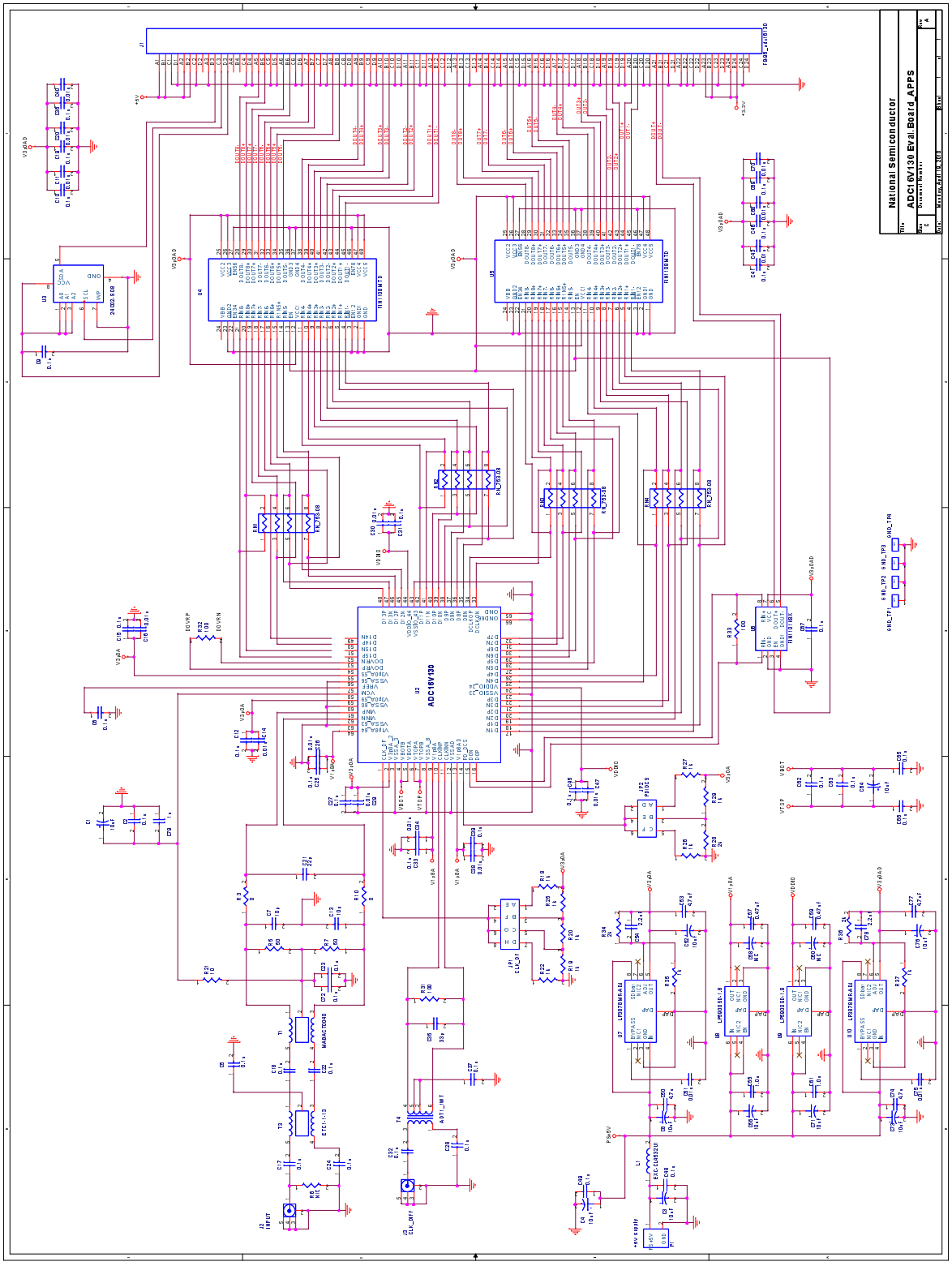

Figure 5

7.0 Evaluation Board Layout

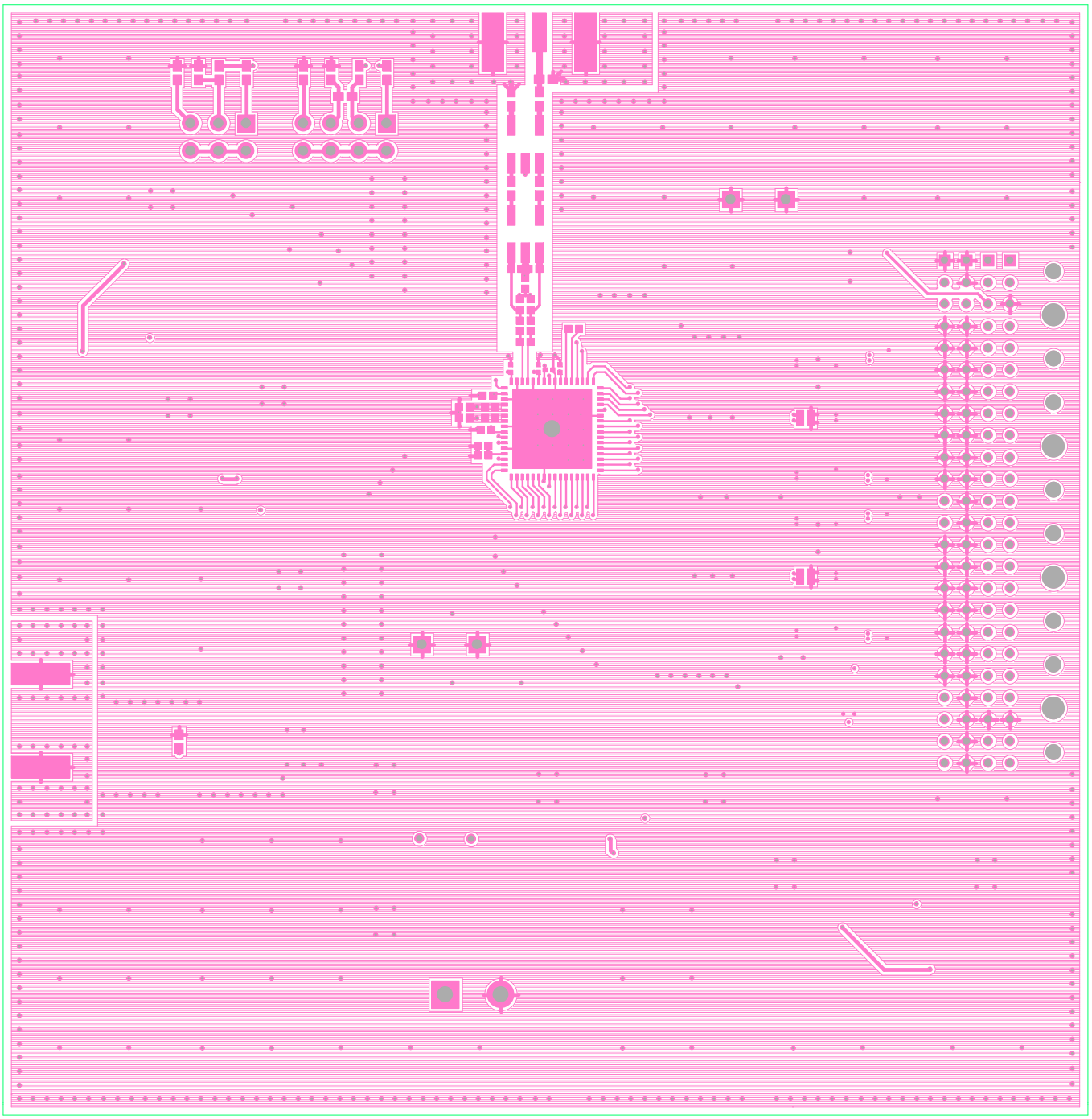

Figure 6. Layer 1 - Signal

7.0 Evaluation Board Layout (cont.)

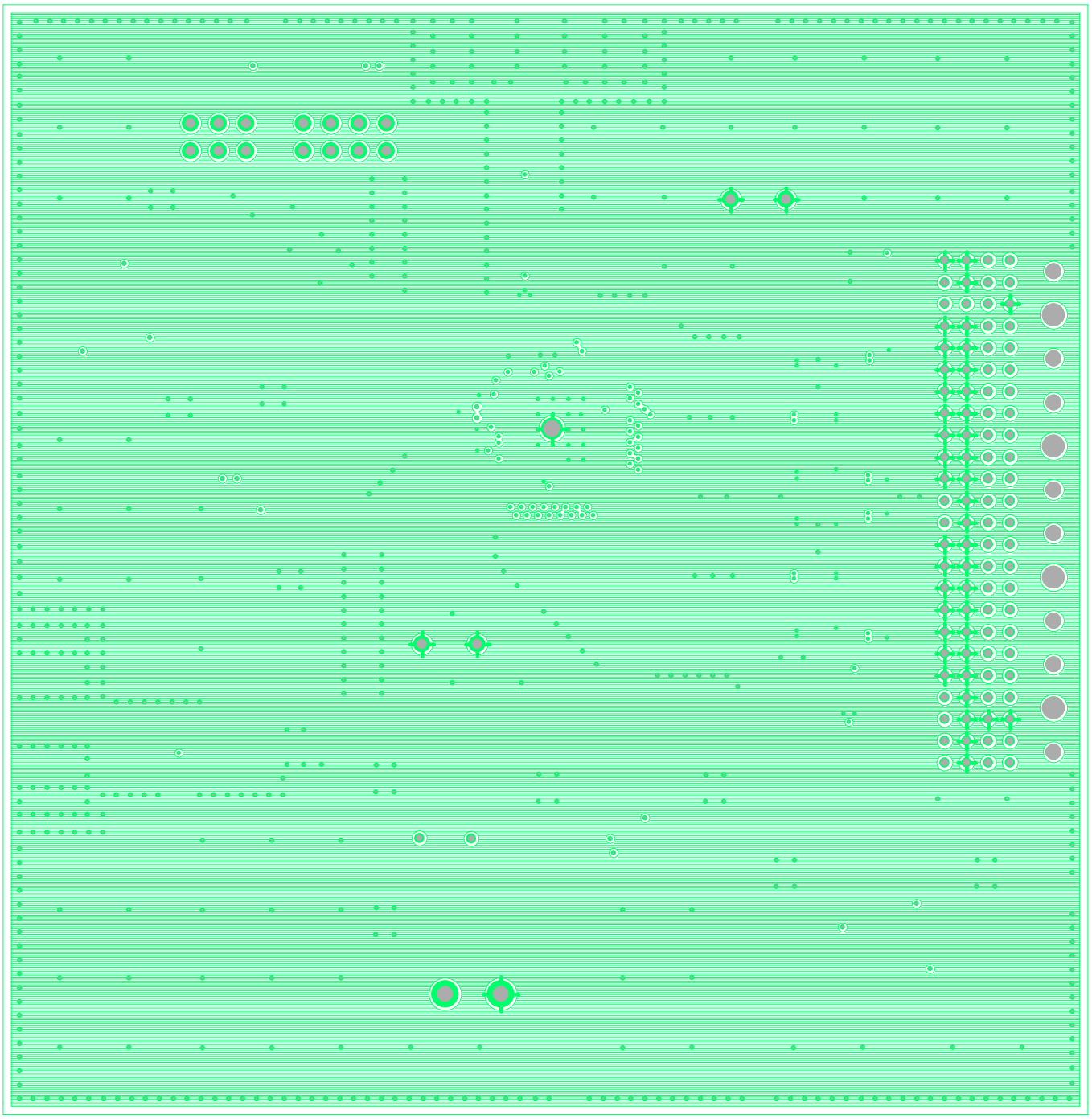

Figure 7. Layer 2 - Ground

7.0 Evaluation Board Layout (cont.)

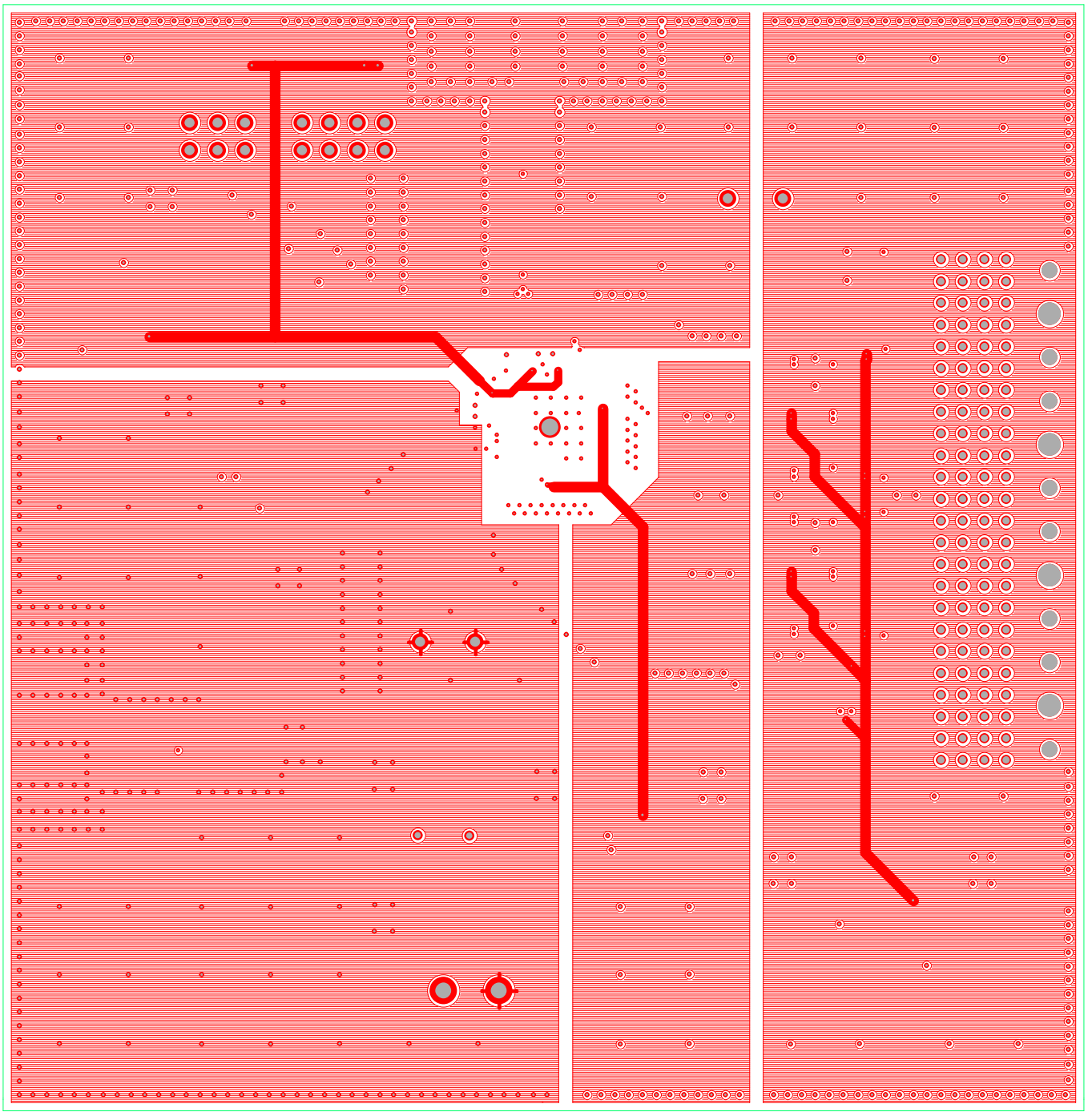

Figure 8. Layer 3 - Power

7.0 Evaluation Board Layout (cont.)

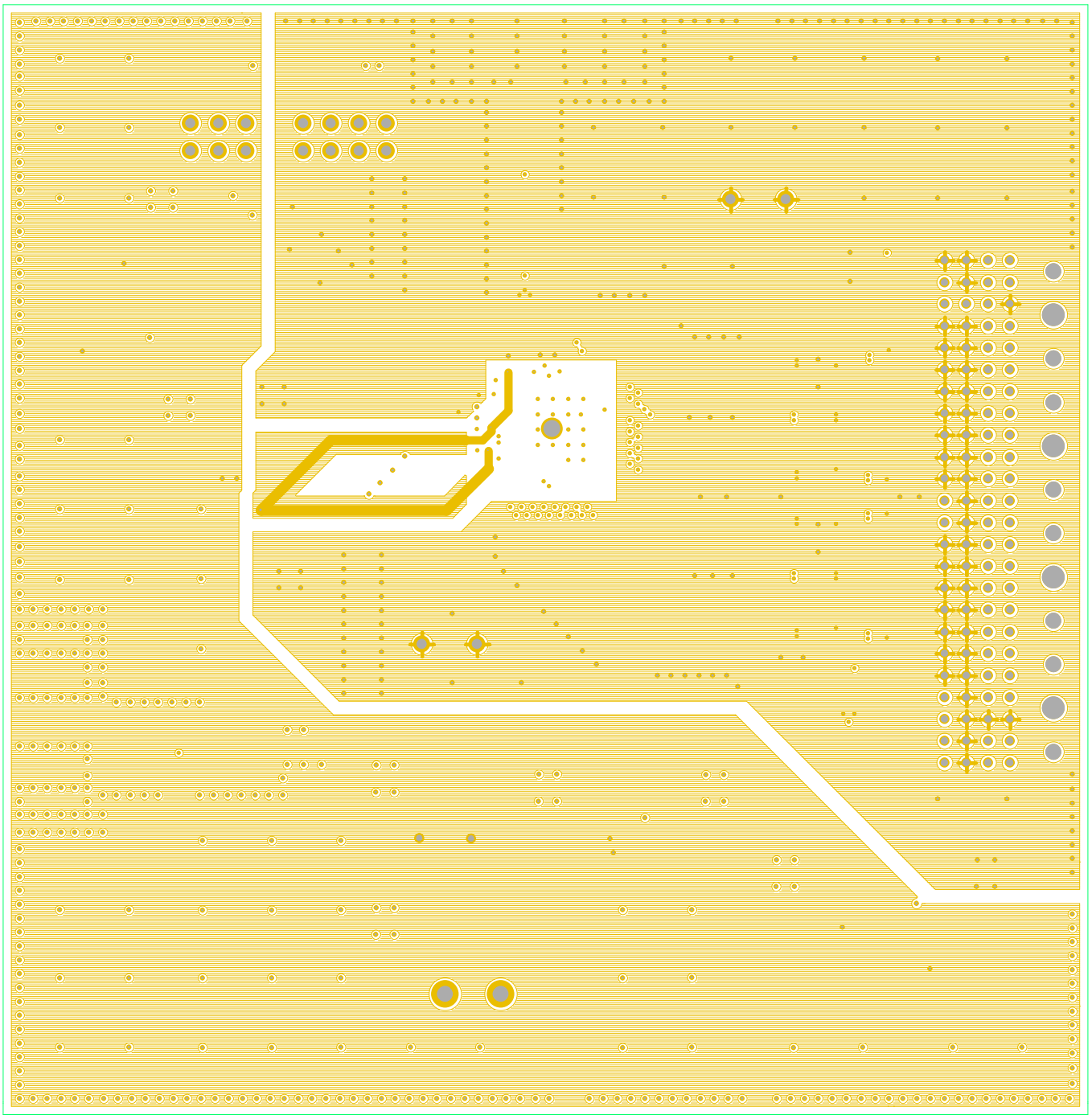

Figure 9. Layer 4 - Power

7.0 Evaluation Board Layout (cont.)

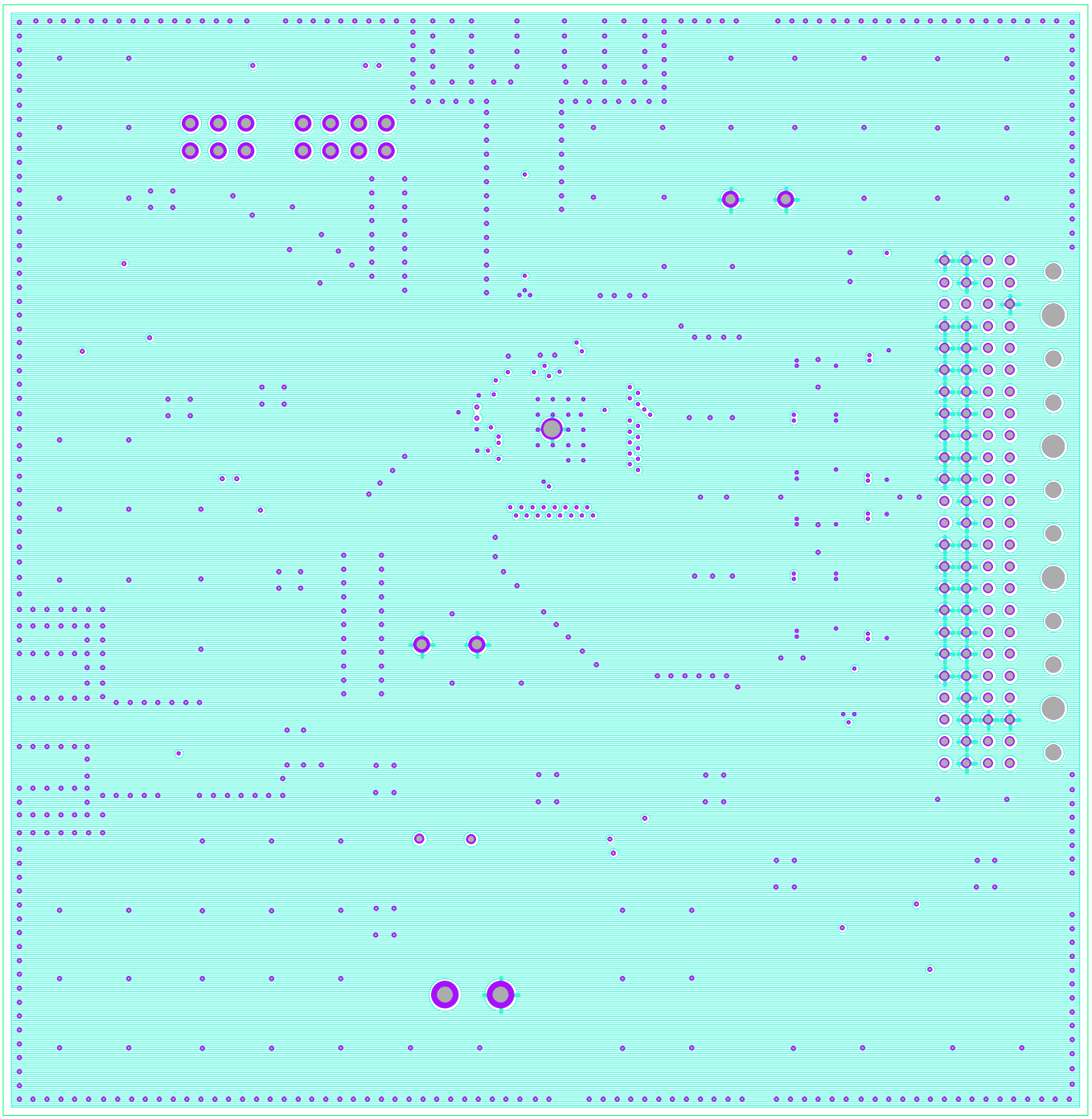

Figure 10. Layer 5 - Ground

7.0 Evaluation Board Layout (cont.)

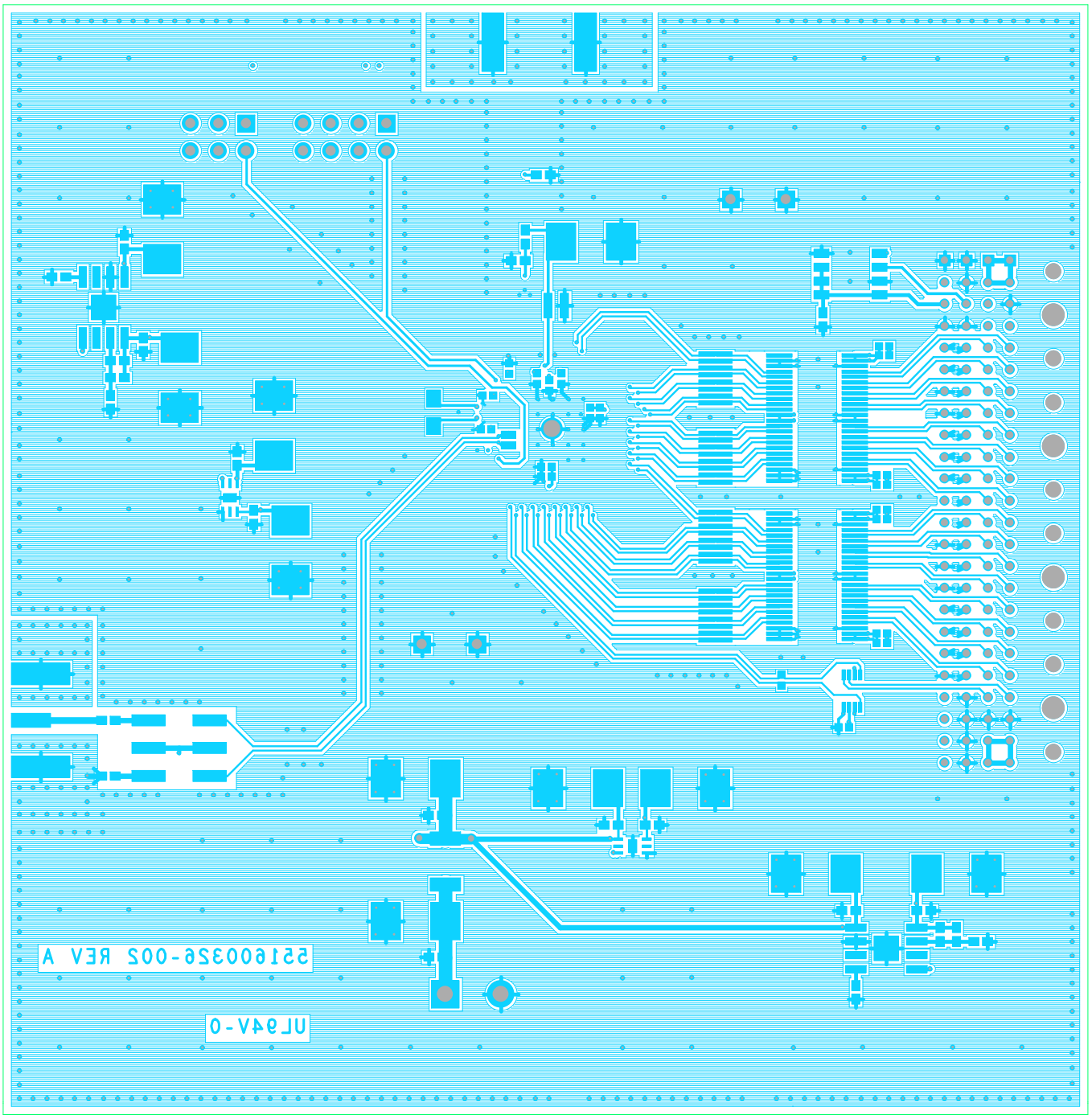

Figure 11. Layer 6 - Signal

8.0 Evaluation Board Bill of Materials

ADC16V130_APPS Evaluation Board Rev: A

Bill Of Materials Dec 3, 2008

Item	Quantity	Reference	Part	PCB Footprint	Manufacturer	Manufacturer P/N
	9	C1, C3, C4, C8, C52, C56, C71, C73, C76	10µF	cap_c-case	AVX	TAJC106K020R
	2	C58, C60	N/C	cap_c-case	AVX	TAJC106K020R
	4	C2, C12, C15, C25	0.1µF	0201	Murata	GRM033R60J104KE19D
	12	C5, C9, C17, C18, C22, C23, C24, C28, C32, C37, C48, C49	0.1µF	0603	Murata	GRM188R71C104KA01D
	2	C57, C59	0.47µF	0603		
	2	C53, C77	4.7µF	0603		
	18	C6, C10, C19, C27, C31, C33, C36, C39, C41, C45, C46, C62, C63, C65, C66, C67, C69, C72	0.1µF	0402	Murata	GRM155R61A104KA01D
	2	C7, C13	10pF	0402	Murata	GRM1555C1H100JZ01D
	14	C11, C14, C16, C20, C26, C29, C30, C34, C38, C40, C43, C47, C68, C70	0.01µF	0402	Murata	GRM155R71H103KA88D
	1	C21	22pF	0402	Murata	GRM1555C1H220JZ01D
	1	C35	33pF	0402	Murata	GRM1555C1H330JZ01D
	2	C50, C74	4.7µF	0603	Panasonic	ECJ-1VB0J475M
	2	C51, C75	0.01µF	0603	Panasonic	ECJ-1VB1H103K
	2	C54, C78	2.2nF	0603	Panasonic	ECJ-1VB1H222K
	2	C55, C61	1.0µF	0603	Murata	GRM188R71C105KA12D
	1	C64	10µF	cap_a-case	Nichicon	F931A106MAA
	1	C79	1.0µF	0508	Panasonic	ECY-29RA105KV
	4	GND_TP1, GND_TP2, GND_TP3, GND_TP4	TestPoint	hdr-1x1-100		
	1	JP1	CLK_DF	hdr-2x4-100		
	1	JP2	PD/DCS	hdr-2x3-100		
	1	J1	CONN_FB-96		AMP/Tyco	223514-1
	1	J2	INPUT	conn_sma-edge	JOHNSON	142-0701-851
	1	J3	CLK_DIFF	conn_sma-edge	JOHNSON	142-0701-851
	1	L1	EXC-CL4532U1			
	1	P1	+5V Supply	tb-2pos_plug	Phoenix Contacts	1759017
	4	RN1, RN2, RN3, RN4	753083101gtr		CTS	753083101GTR
	2	R3, R10	0Ω	0402		
	2	R5, R7	50Ω	0402		
	1	R6	N/C	0603		
	10	R18, R19, R20, R22, R25, R26, R27, R29, R35, R37	1kΩ	0603		
	1	R21	10Ω	0603		
	3	R28, R34, R36	2kΩ	0603		
	3	R31, R32, R33	100Ω	0402		
	1	T1	MABACT0040		MA-COM	MABACT0040
	1	T3	ETC1-1-13		MA-COM	ETC1-1-13
	1	T4	ADT1_1WT		Mini-Circuits	ADT1_1WT
	1	U2	ADC16130			
	1	U3	24C02-SO8		Atmel	AT24C02AN-10SU-2.7
	2	U4, U5	FIN1108MTD		Fairchild	FIN1108MTD
	1	U6	FIN1101K8X		Fairchild	FIN1101K8X
	2	U7, U10	LP3878MR-ADJ		NSC	LP3878MR-ADJ/NOPB
	2	U8, U9	LP5900SD-1.8		NSC	LP5900SD-1.8/NOPB

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