

- 1

2

3

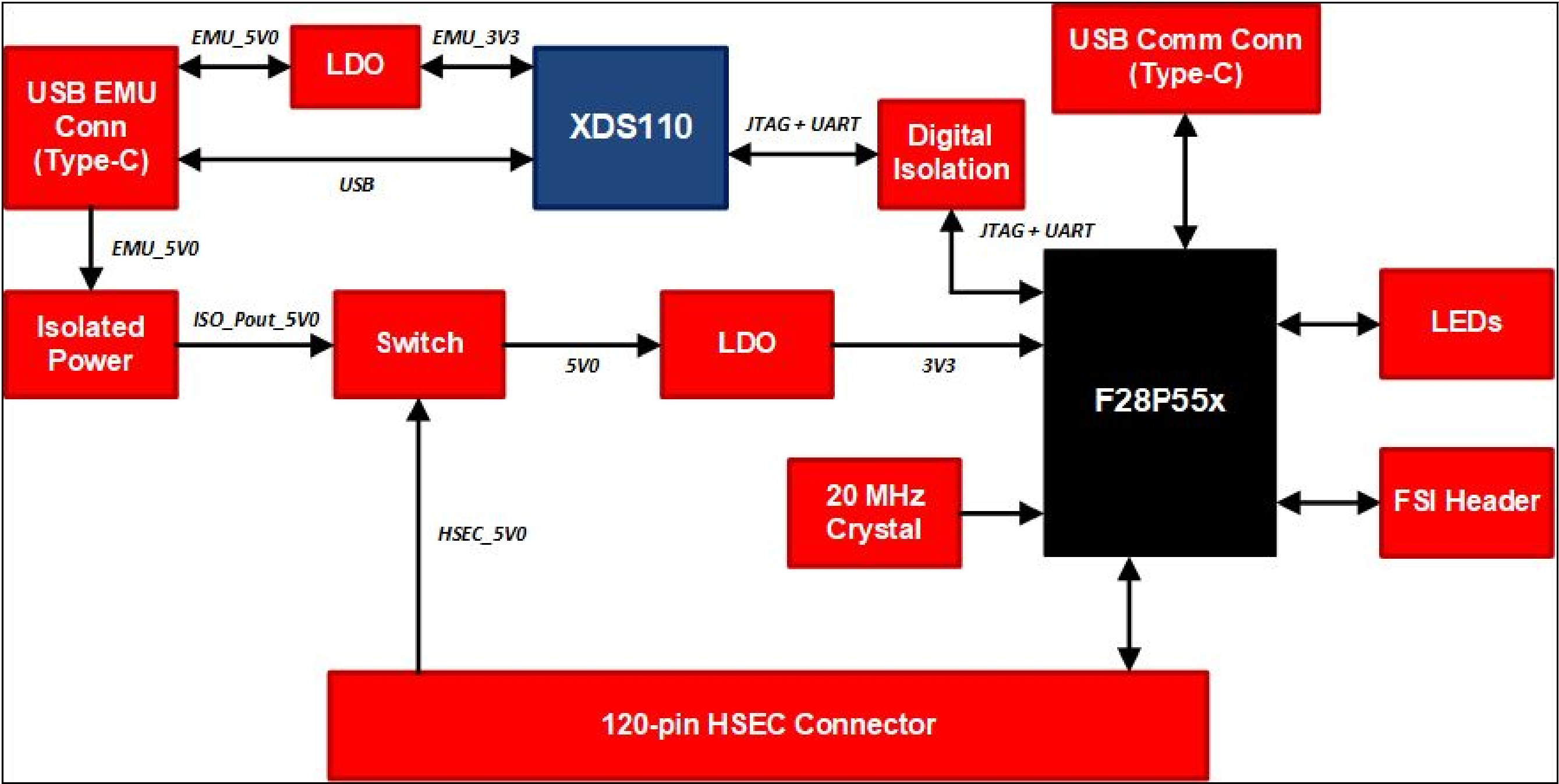
4

5

6
- 1) USB Differential Pairs - 90 Ohm  
(A) XDS\_D\_P and XDS\_D\_N  
(B) USB\_D\_P (GPIO41) and USB\_D\_N (GPIO23)

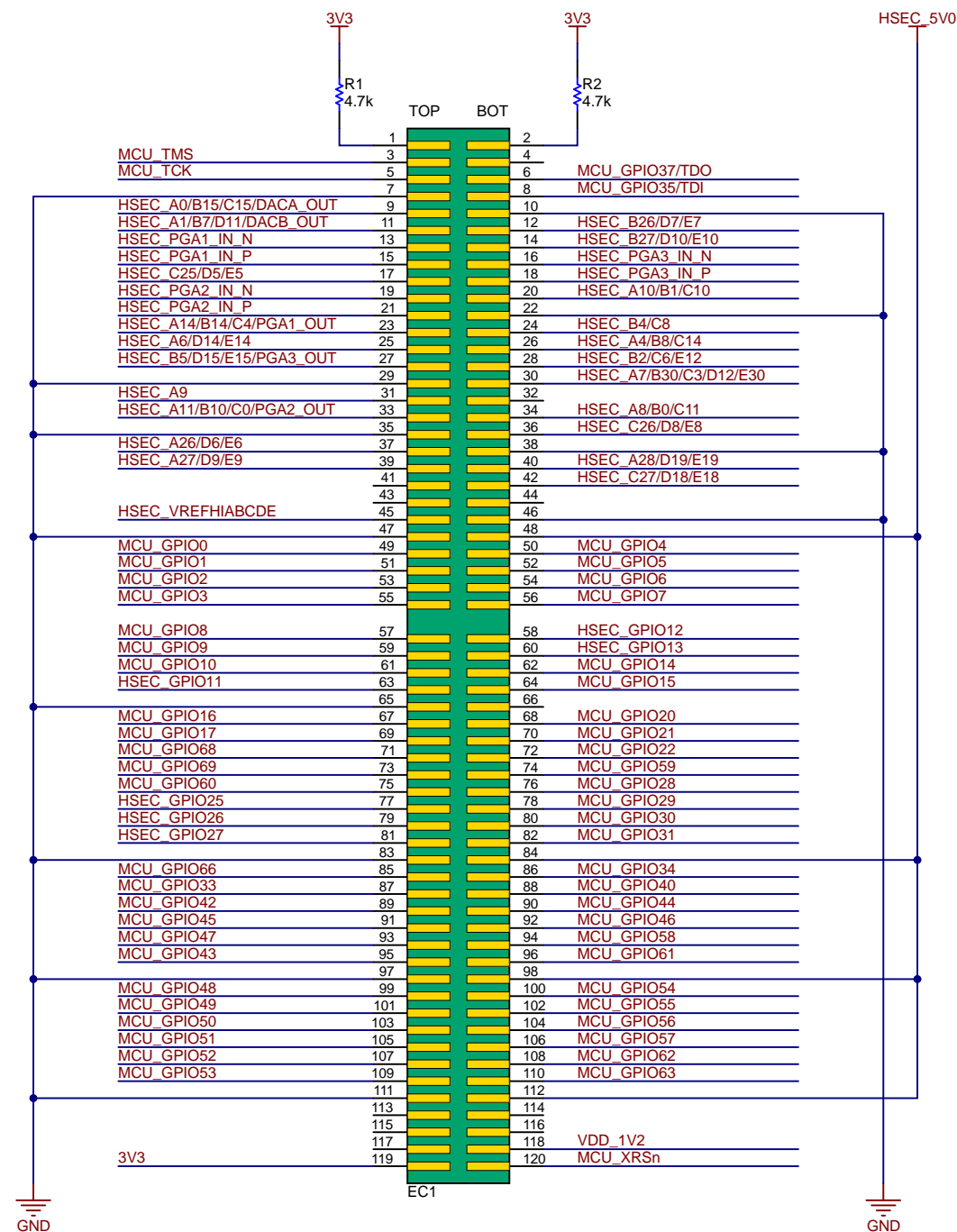
2) ADC PGA Differential pair Impedance Matching - 90 Ohm  
(A) HSEC\_PGAx\_IN\_P pins should match with HSEC\_PGAx\_IN\_N, where x is between 1-3  
(B) MCU\_PGAx\_IN\_P pins should match with MCU\_PGAx\_IN\_N, where x is between 1-3

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	Sept 13, 2023	PL	Initial Draft
A	N/A	Jan 29, 2024	PL	Added Test Point for 5V0 and 3V3 Dampening resistor tuned per characterization Switched U1 from PBK to PDT package Minor changes to silkscreen and GND pour Adjustments to analog signal routing

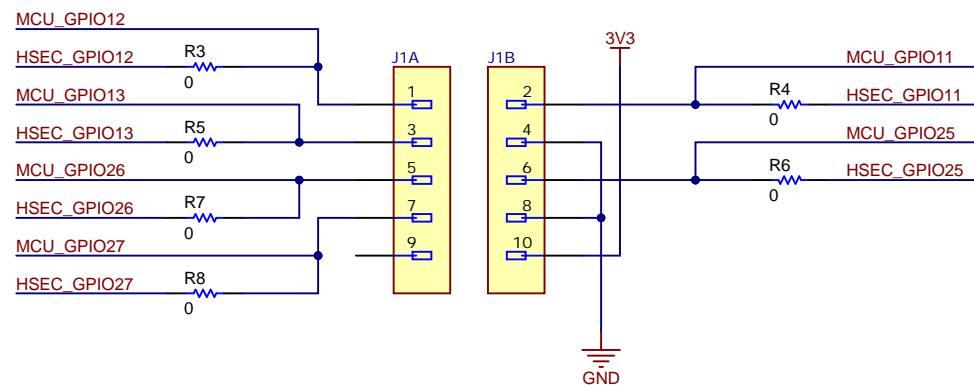


Power to the MCU is either supported by the USB-C on the left or through the HSEC

J1 has been updated over previous designs. Pins 9 and 10 were added enabling power to the connector. Additionally Pins 2 and 6, previously GND, have been repurposed to enable the full 3 pin FSI communication. The user can shunt HSEC GPIO11 and HSEC GPIO25 to ground if backwards compatibility is required.

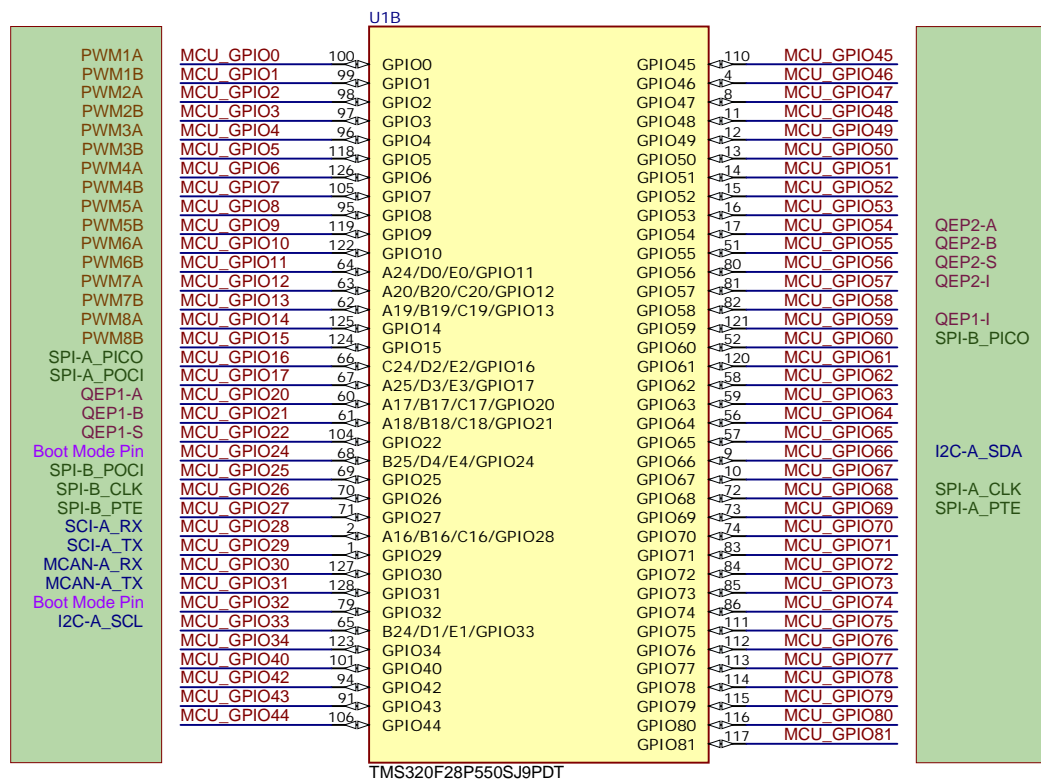


## 10-pin FSI Connector



- |   |           |    |             |
|---|-----------|----|-------------|
| 1 | FSI-RX0   | 2  | FSI-RX1/GND |
| 3 | FSI-RXCLK | 4  | GND         |
| 5 | FSI-TX0   | 6  | FSI-TX1/GND |
| 7 | FSI-TXCLK | 8  | GND         |
| 9 | KEY       | 10 | 3V3         |

Pin 9 of J1 is cutoff to key the connector



A

B

C

D

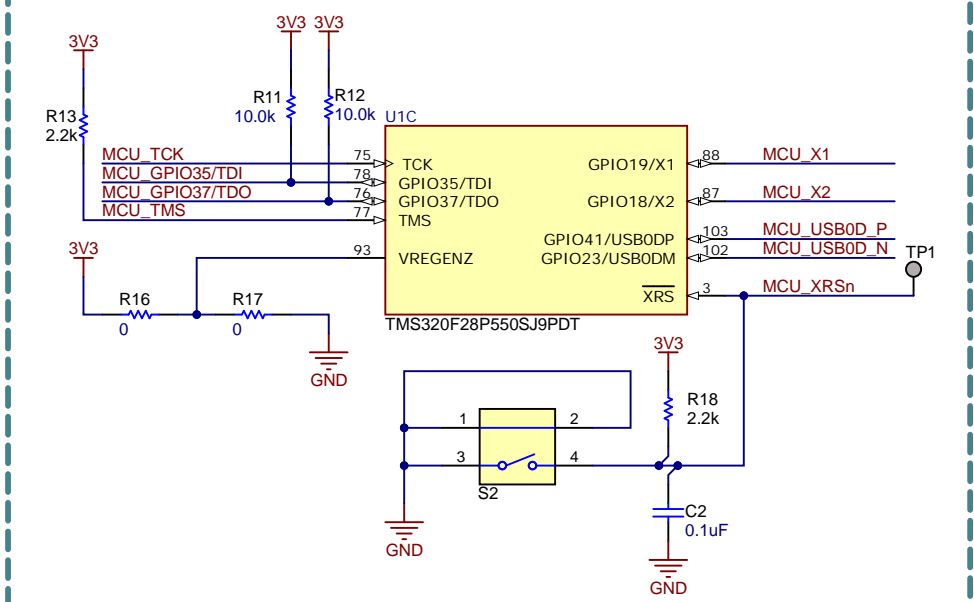
A

B

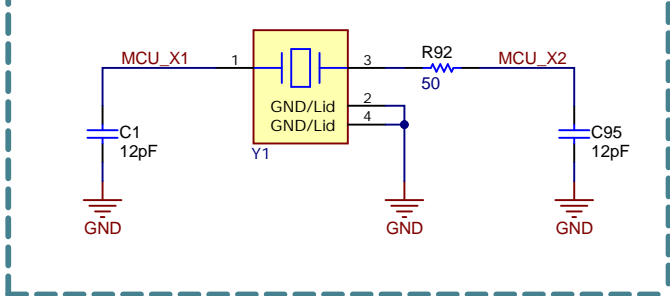
C

D

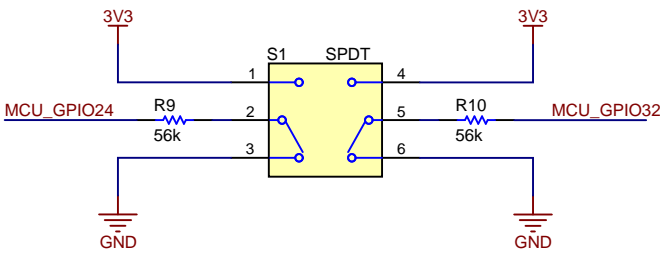
JTAG and Reset



20 MHz External Crystal



Boot Mode Switch

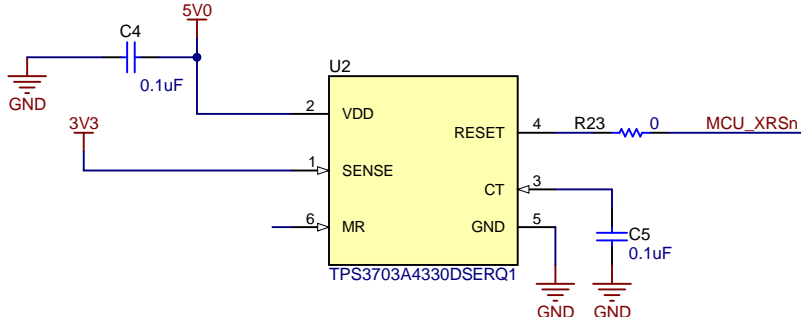


Boot Mode Selection Chart

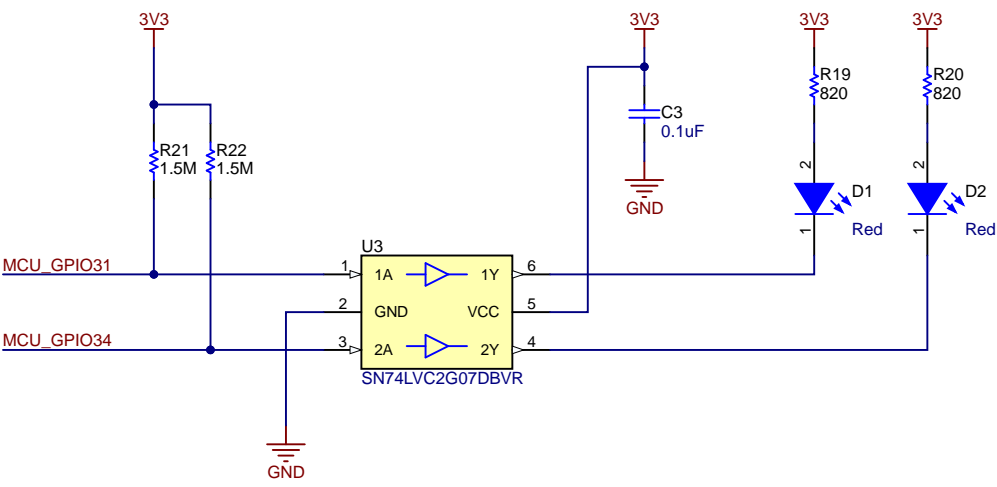
(S2: UP is '1', DOWN is '0')

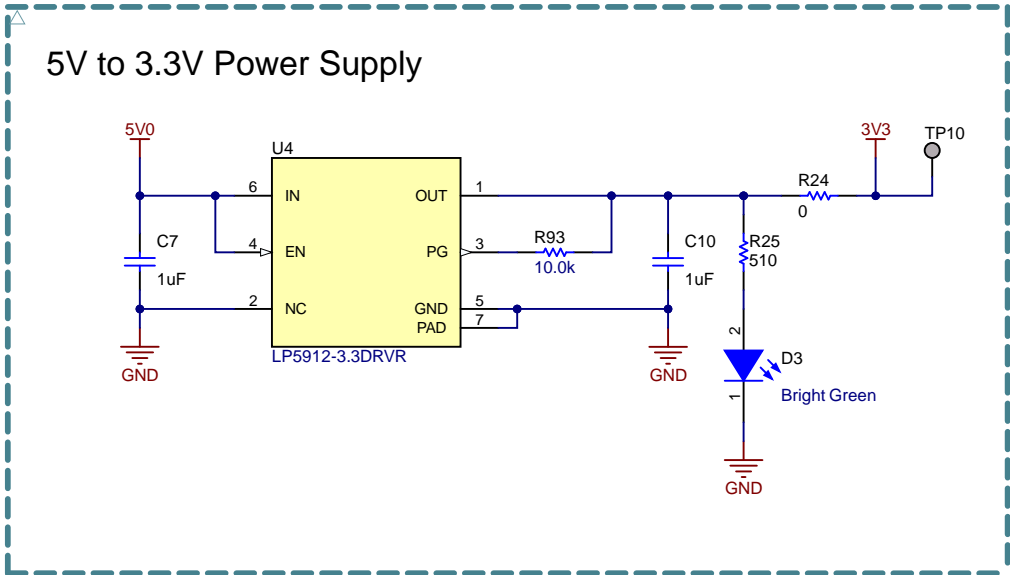
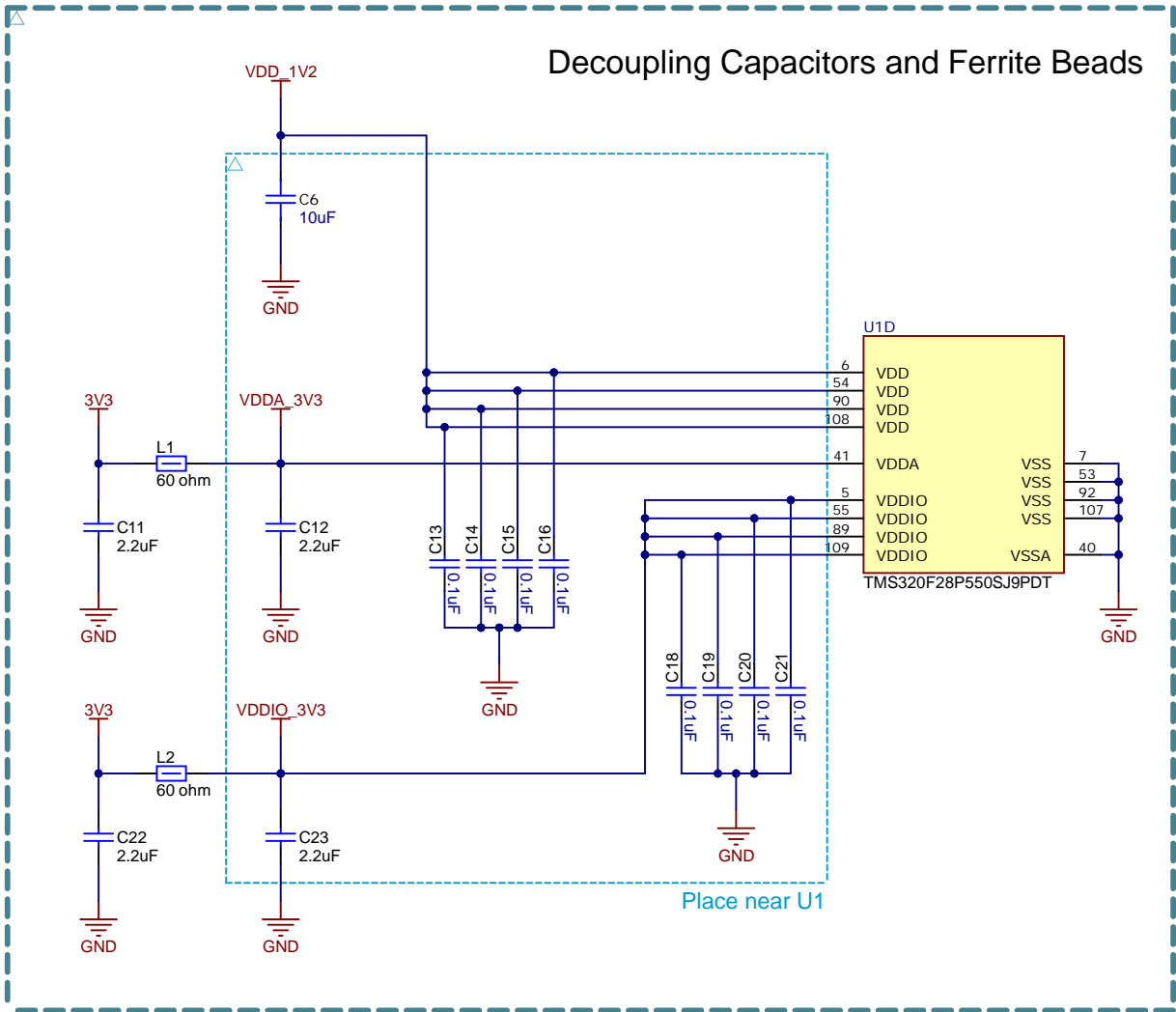
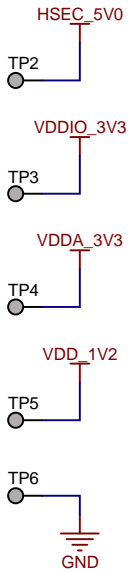
Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN (MCAN-NONFD)
03	1	1	Boot from Flash (USB)

System Supervisory Circuitry



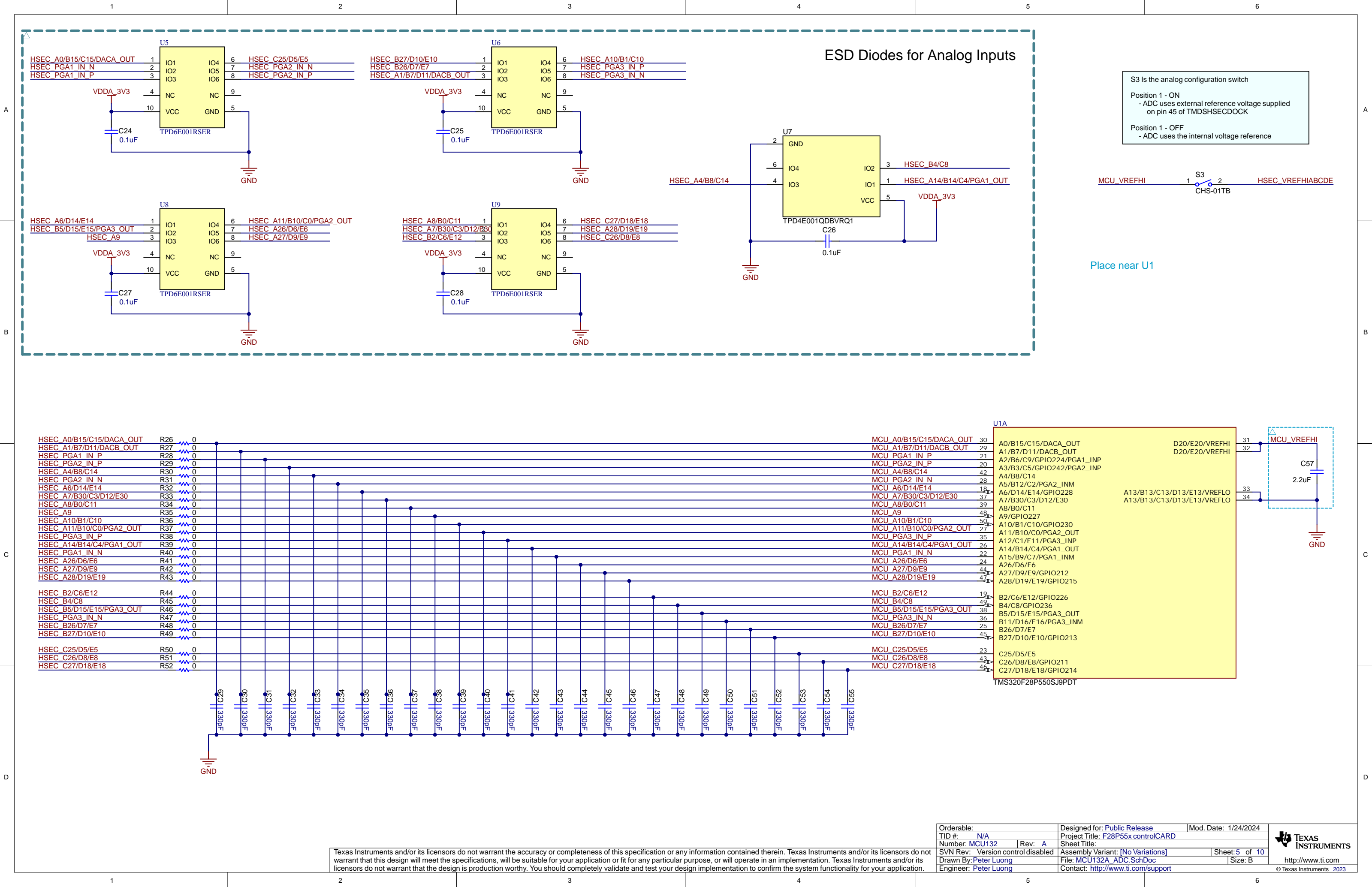
LEDs





The F28P55x controlCARD uses the internal VREG to generate the 1.2V voltage rail for VDD.

For custom boards using external VREG mode, recommend to use dual-output DC-DC (e.g., TPS62441) to generate both 3.3V and 1.2V supplies.

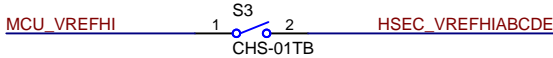


ESD Diodes for Analog Inputs

S3 is the analog configuration switch

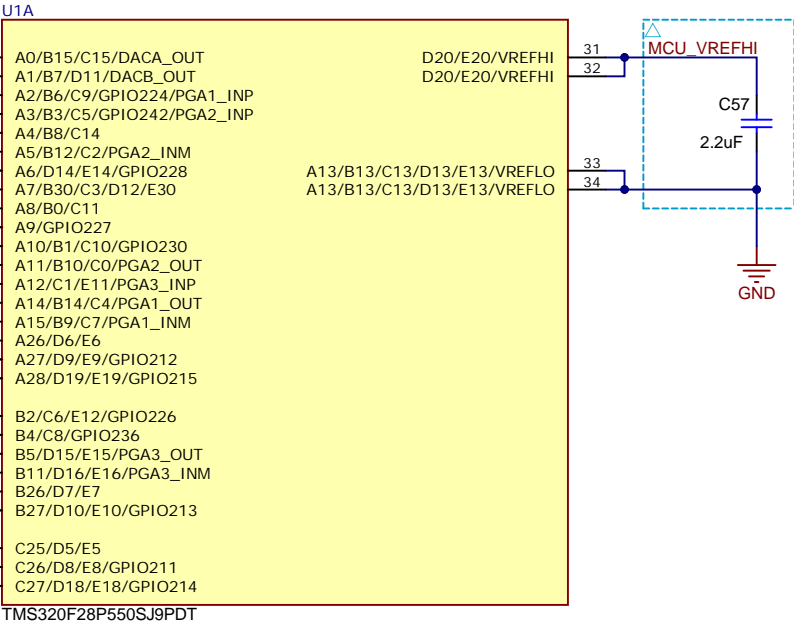
Position 1 - ON  
- ADC uses external reference voltage supplied on pin 45 of TMDSHSECDOCK

Position 1 - OFF  
- ADC uses the internal voltage reference



Place near U1

HSEC_A0/B15/C15/DACA_OUT	R26	0	MCU_A0/B15/C15/DACA_OUT	30
HSEC_A1/B7/D11/DACB_OUT	R27	0	MCU_A1/B7/D11/DACB_OUT	29
HSEC_PGA1_IN_P	R28	0	MCU_PGA1_IN_P	21
HSEC_PGA2_IN_P	R29	0	MCU_PGA2_IN_P	20
HSEC_A4/B8/C14	R30	0	MCU_A4/B8/C14	42
HSEC_PGA2_IN_N	R31	0	MCU_PGA2_IN_N	28
HSEC_A6/D14/E14	R32	0	MCU_A6/D14/E14	18
HSEC_A7/B30/C3/D12/E30	R33	0	MCU_A7/B30/C3/D12/E30	37
HSEC_A8/B0/C11	R34	0	MCU_A8/B0/C11	39
HSEC_A9	R35	0	MCU_A9	48
HSEC_A10/B1/C10	R36	0	MCU_A10/B1/C10	50
HSEC_A11/B10/C0/PGA2_OUT	R37	0	MCU_A11/B10/C0/PGA2_OUT	27
HSEC_PGA3_IN_P	R38	0	MCU_PGA3_IN_P	35
HSEC_A14/B14/C4/PGA1_OUT	R39	0	MCU_A14/B14/C4/PGA1_OUT	26
HSEC_PGA1_IN_N	R40	0	MCU_PGA1_IN_N	22
HSEC_A26/D6/E6	R41	0	MCU_A26/D6/E6	24
HSEC_A27/D9/E9	R42	0	MCU_A27/D9/E9	44
HSEC_A28/D19/E19	R43	0	MCU_A28/D19/E19	47
HSEC_B2/C6/E12	R44	0	MCU_B2/C6/E12	19
HSEC_B4/C8	R45	0	MCU_B4/C8	42
HSEC_B5/D15/E15/PGA3_OUT	R46	0	MCU_B5/D15/E15/PGA3_OUT	38
HSEC_PGA3_IN_N	R47	0	MCU_PGA3_IN_N	36
HSEC_B26/D7/E7	R48	0	MCU_B26/D7/E7	25
HSEC_B27/D10/E10	R49	0	MCU_B27/D10/E10	45
HSEC_C25/D5/E5	R50	0	MCU_C25/D5/E5	23
HSEC_C26/D8/E8	R51	0	MCU_C26/D8/E8	43
HSEC_C27/D18/E18	R52	0	MCU_C27/D18/E18	46

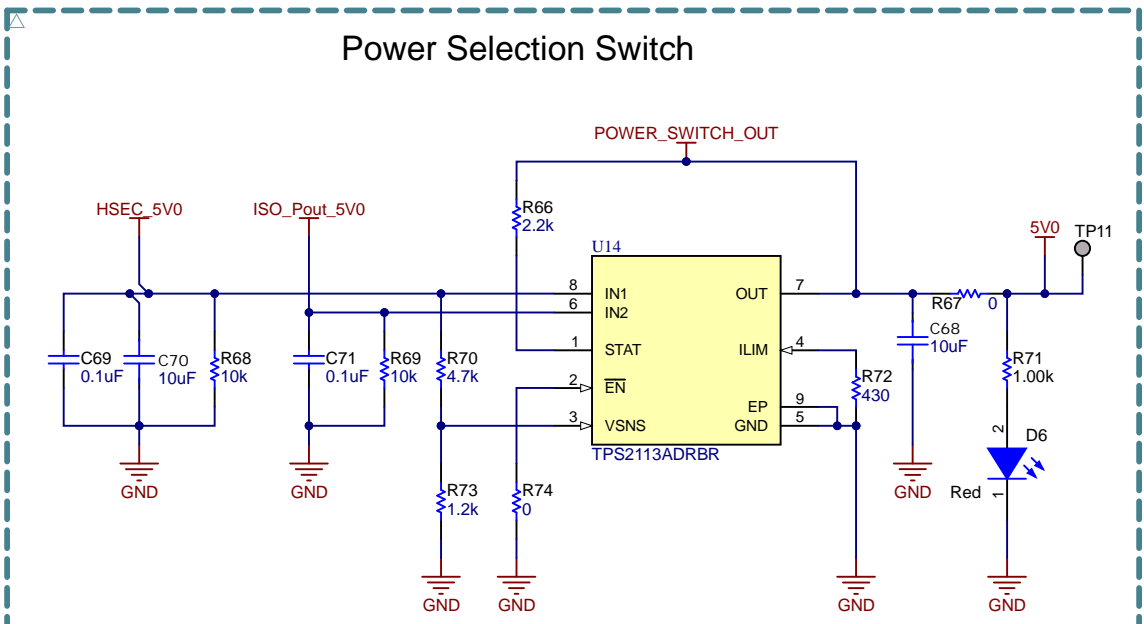
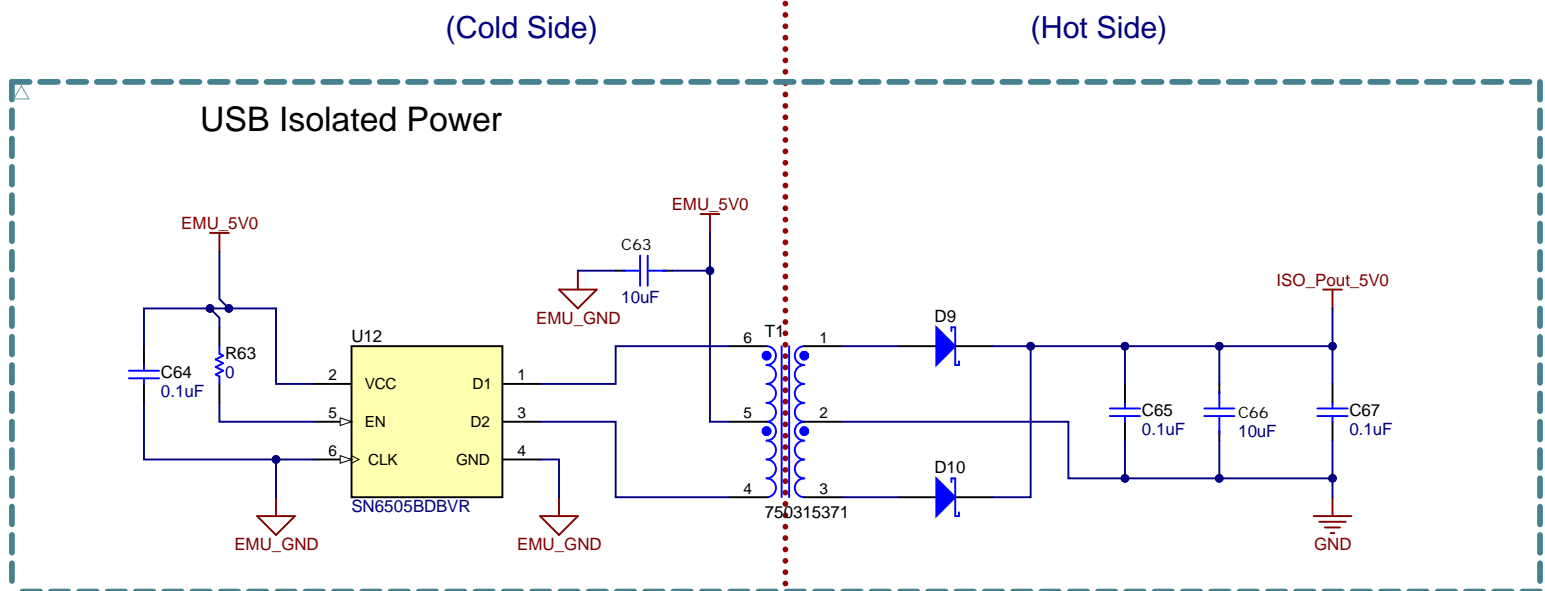
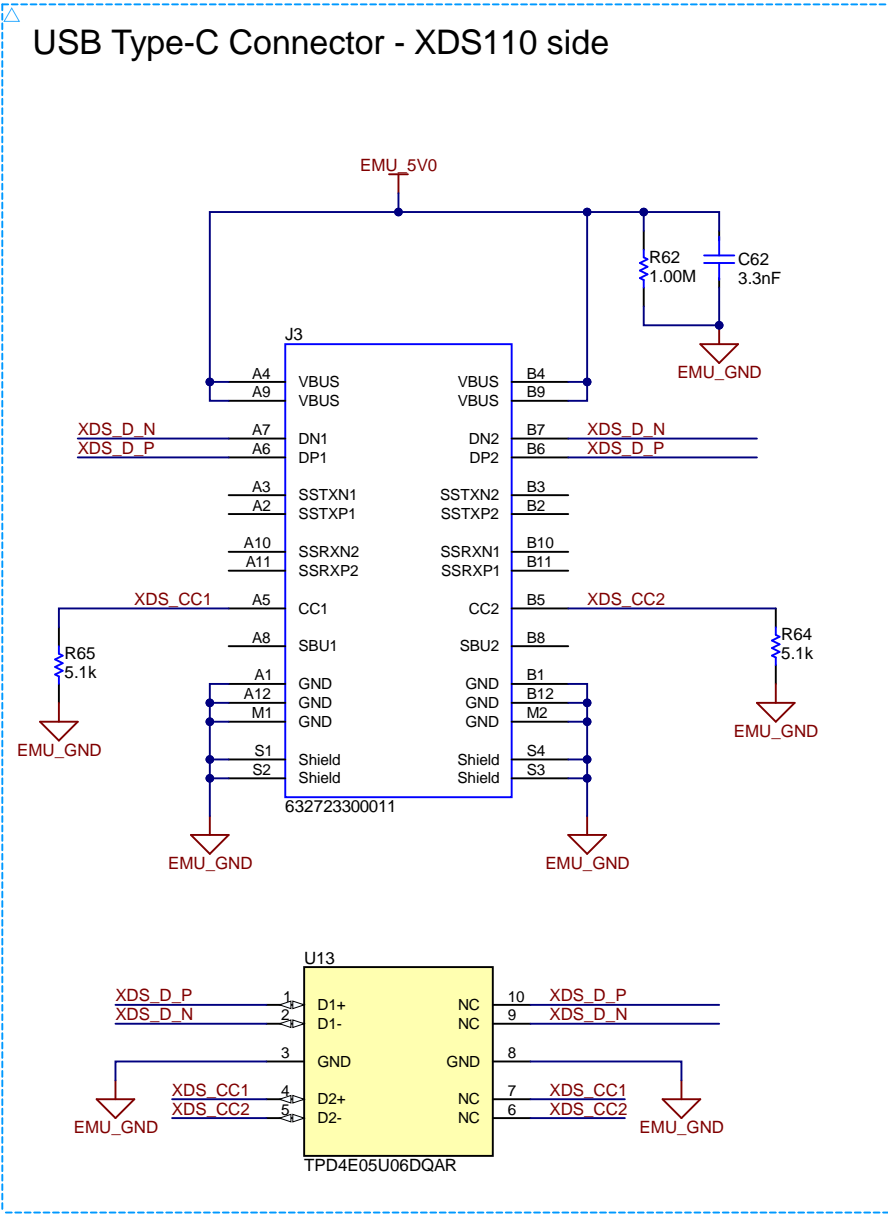


Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

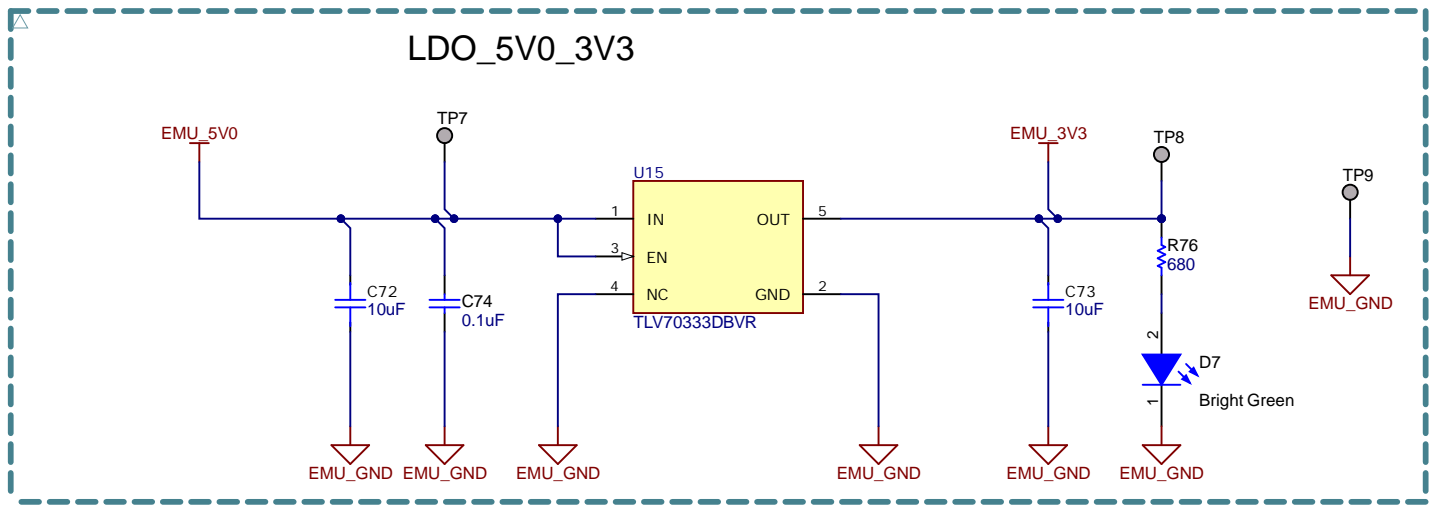
Orderable:	Designed for: Public Release	Mod. Date: 1/24/2024
TID #: N/A	Project Title: F28P55x controlCARD	
Number: MCU132	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 5 of 10
Drawn By: Peter Luong	File: MCU132A_ADC.SchDoc	Size: B
Engineer: Peter Luong	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



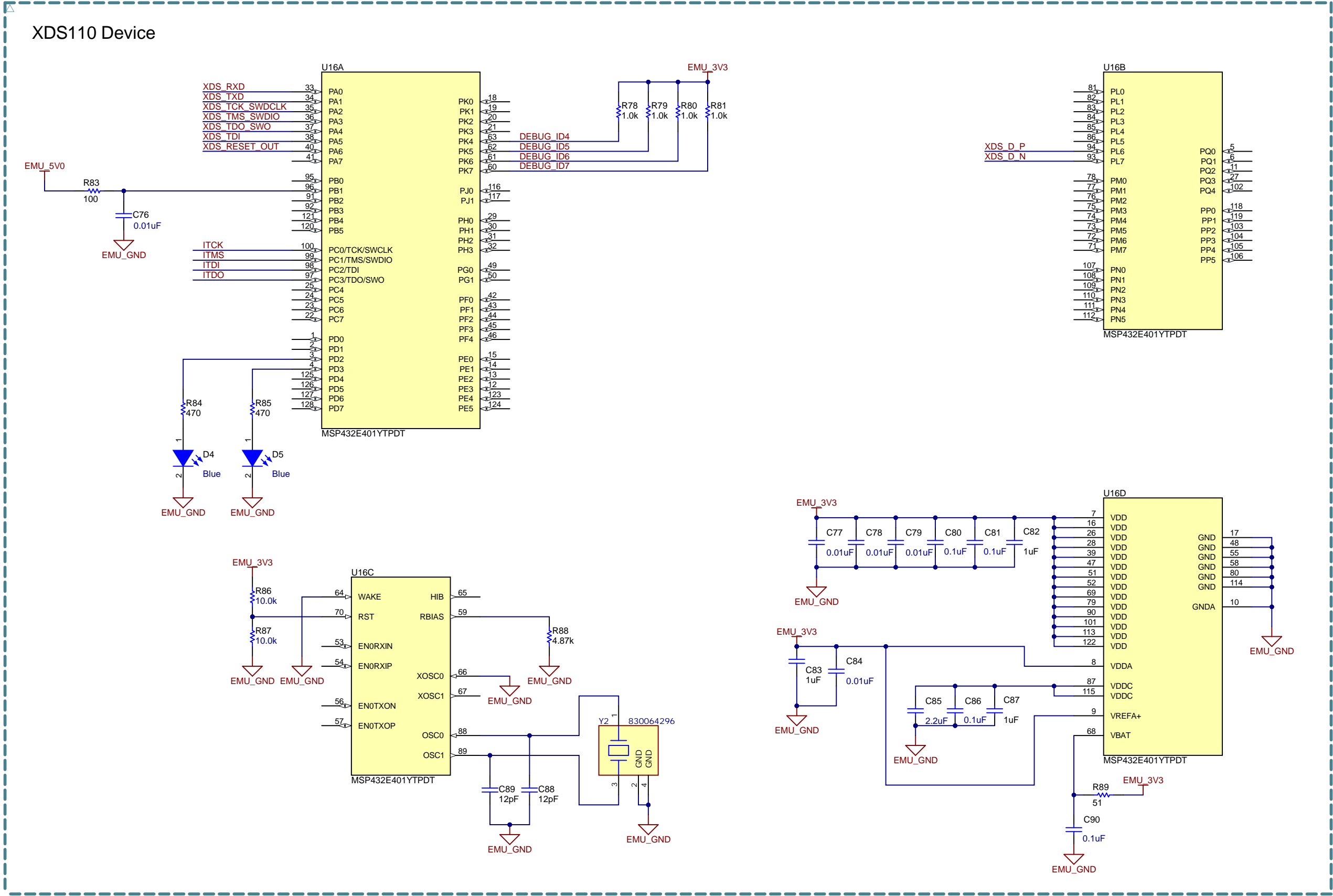




Switch Truth Table		
HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable:	Designed for: Public Release	Mod. Date: 10/9/2023
TID #: N/A	Project Title: F28P55x controlCARD	
Number: MCU132	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 8 of 10
Drawn By: Peter Luong	File: MCU132A_XDS110_MCU.SchDoc	Size: B
Engineer: Peter Luong	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



A

B

C

D

A

B

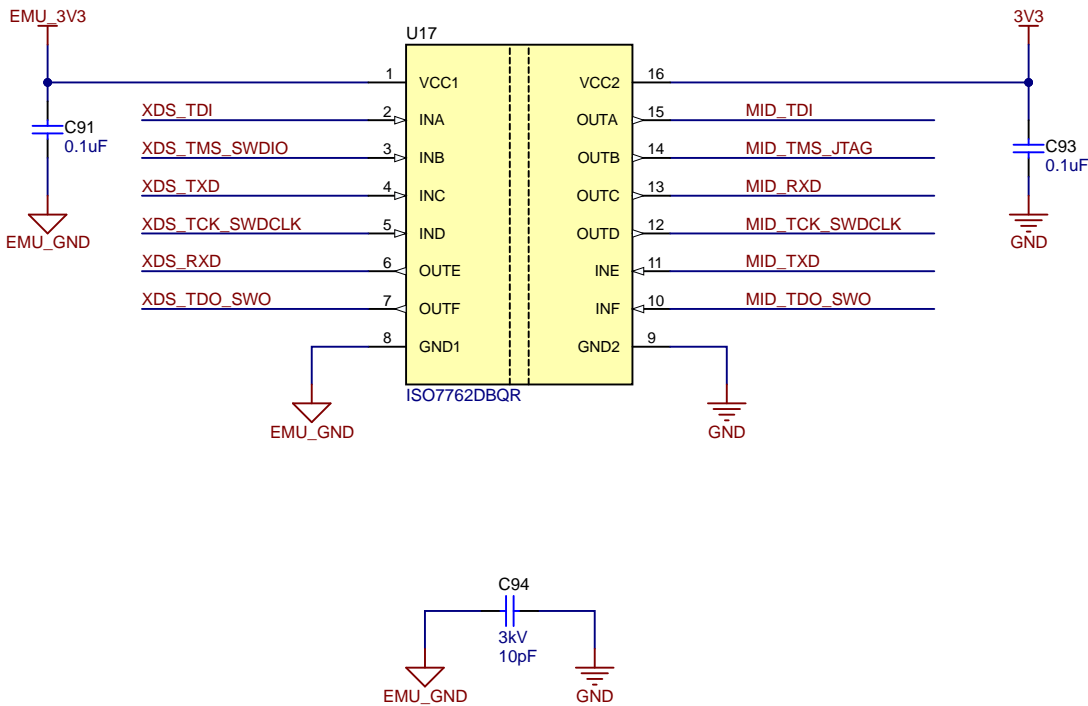
C

D

NOTE: Because the JTAG signals are isolated, cJTAG is not supported on this controlCARD.

(Cold Side)

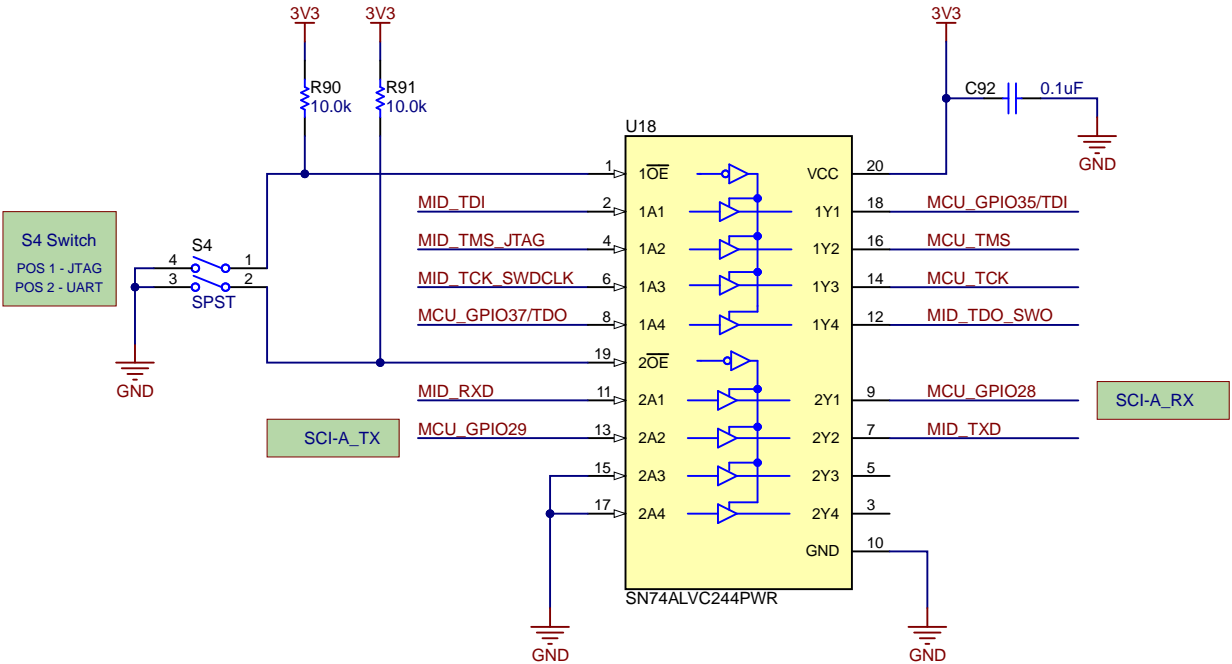
(Hot Side)



WARNING: To avoid potential shock hazard in high-voltage settings, leave the Y cap (C94) unpopulated from the EVM.

S4 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD  
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard  
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator  
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins





PCB Number: MCU132  
PCB Rev: A



LBL1  
PCB Label  
THT-14-423-10  
Size: 0.65" x 0.20 "

ZZ1  
Label Assembly Note  
This Assembly Note is for PCB labels only

ZZ2  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5  
Assembly Note  
Clip off KEY pin 9 of J1 connector header

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable:		Designed for: Public Release	Mod. Date: 10/10/2023
TID #:		Project Title: F28P55x controlCARD	
Number: MCU132	Rev: A	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]		Sheet: 10 of 10
Drawn By: Peter Luong	File: MCU132A_Hardware.SchDoc		Size: B
Engineer: Peter Luong	Contact: http://www.ti.com/support		