

Low-power sensor measurements: 3.3-V, 1-ksps, 12-bit, single-ended, dual-supply circuit

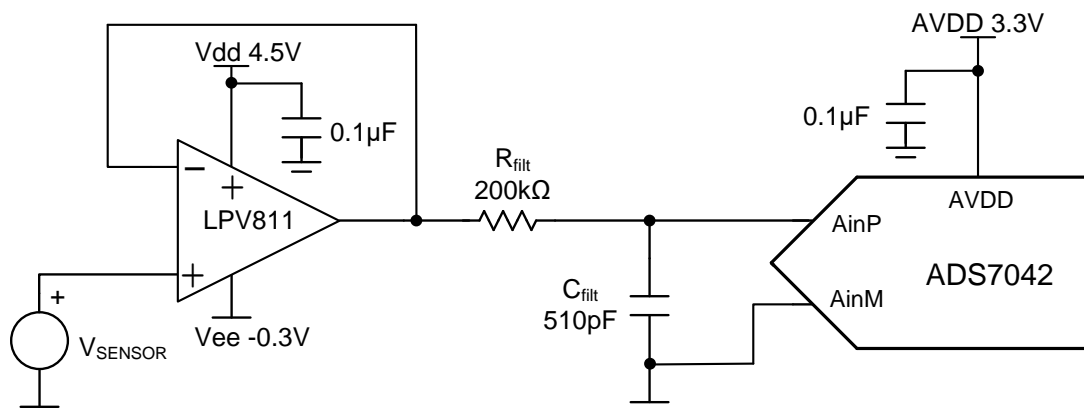
Reed Kaczmarek

| Input | ADC Input | Digital Output ADS7042 |
|--------------------|------------------------------|------------------------|
| $V_{inMin} = 0V$ | $AIN_P = 0V, AIN_M = 0V$ | 000_H or 0_{10} |
| $V_{inMax} = 3.3V$ | $AIN_P = 3.3V, AIN_M = 0V$ | FFF_H or 4096_{10} |

| Power Supplies | | |
|----------------|----------|----------|
| AVDD | V_{ee} | V_{dd} |
| 3.3V | -0.3V | 4.5V |

Design Description

This design shows an low-power amplifier being used to drive a SAR ADC that consumes only nW of power during operation. This design is intended for systems collecting sensor data and require a low-power signal chain which only burns single-digit μW of power. [PIR sensors](#), [gas sensors](#), and [glucose monitors](#) are a few examples of power-sensitive systems that benefit from this SAR ADC design. The values in the component selection section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. [Low-Power Sensor Measurements: 3.3 V, 1 ksps, 12-bit Single-Ended, Single Supply](#) shows a simplified version of this circuit where the negative supply is grounded. The -0.3-V negative supply in this example is used to achieve the best possible linear input signal range. See [SAR ADC Power Scaling](#) for a detailed description of trade-offs in low-power SAR design.



Copyright © 2017, Texas Instruments Incorporated

Specifications

| Specification | Calculated | Simulated | Measured |
|--------------------------------------|--|--------------------|---------------------|
| Transient ADC Input Settling (1ksps) | $< 0.5 \times \text{LSB} = 402\mu\text{V}$ | 41.6 μV | N/A |
| AVDD Supply Current (1ksps) | 230nA | N/A | 214.8nA |
| AVDD Supply Power (1ksps) | 759nW | N/A | 709nW |
| VDD OPAMP Supply Current | 450nA | N/A | 431.6nA |
| VDD OPAMP Supply Power | 2.025 μW | N/A | 1.942 μW |
| AVDD + VDD System Power (1ksps) | 2.784 μW | N/A | 2.651 μW |

Design Notes

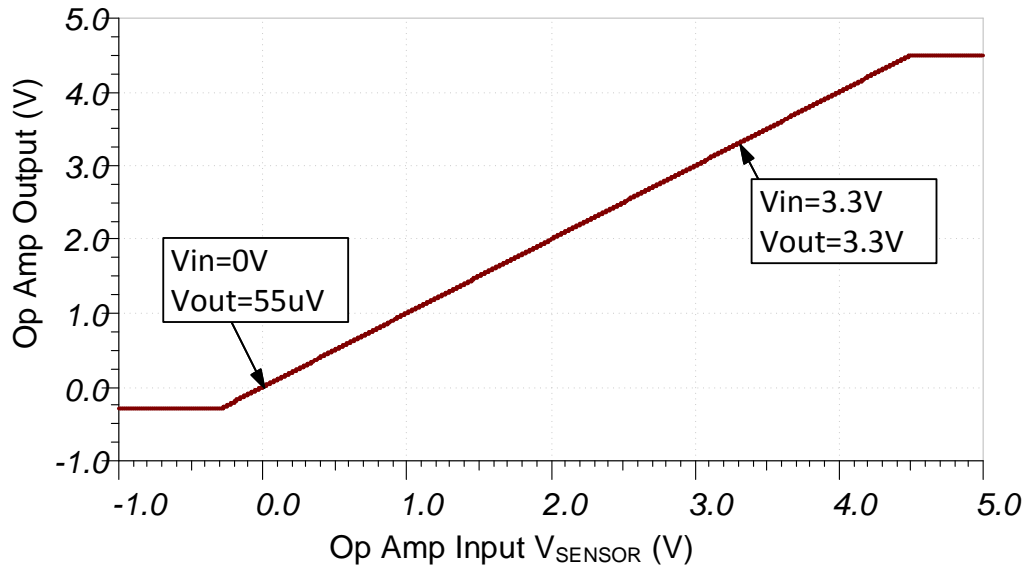
1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the component selection section.
2. Select a COG (NPO) capacitor for Cfilt to minimize distortion.
3. The [TI Precision Labs – ADCs](#) training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt (see [Introduction to SAR ADC Front-End Component Selection](#)). These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify the design you will need to select a different RC filter.

Component Selection

- Select a low-power op amp:
 - Supply current < 0.5μA
 - Gain bandwidth product > 5kHz (5 times the sampling rate)
 - Unity gain stable
 - LPV811 – 450-nA supply current, 8-kHz gain bandwidth product, unity gain stable
- Find op amp maximum and minimum output for linear operation:
 - $V_{ee} + 0V < V_{out} < V_{dd} - 0.9V$ from LPV811 V_{cm} specification
 - $V_{ee} + 10mV < V_{out} < V_{dd} - 10mV$ from LPV811 V_{out} swing specification
 - $V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V$ from LPV811 Aol linear region specification
- Typical power calculations (at 1ksps) with expected values. See [SAR ADC Power Scaling](#) for a detailed description of trade-offs in low-power SAR design:
 - $P_{AVDD} = I_{AVDD_AVG} \times AVDD = 230nA \times 3.3V = 759nW$
 - $P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 450nA \times (4.5V - (-0.3V)) = 2.16\mu W$
 - $P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.16\mu W = 2.919\mu W$
- Typical power calculations (at 1ksps) with measured values:
 - $P_{AVDD} = I_{AVDD_AVG} \times AVDD = 214.8nA \times 3.3V = 708.8nW$
 - $P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 431.6nA \times (4.5V - (-0.3V)) = 2.071\mu W$
 - $P_{total} = P_{AVDD} + P_{LPV811} = 708.8nW + 2.071\mu W = 2.780\mu W$
- Find Rfilt and Cfilt to allow for settling at 1ksps. Refer to [Refine the Rfilt and Cfilt Values](#) (a *Precision Labs* video) for the algorithm to select Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

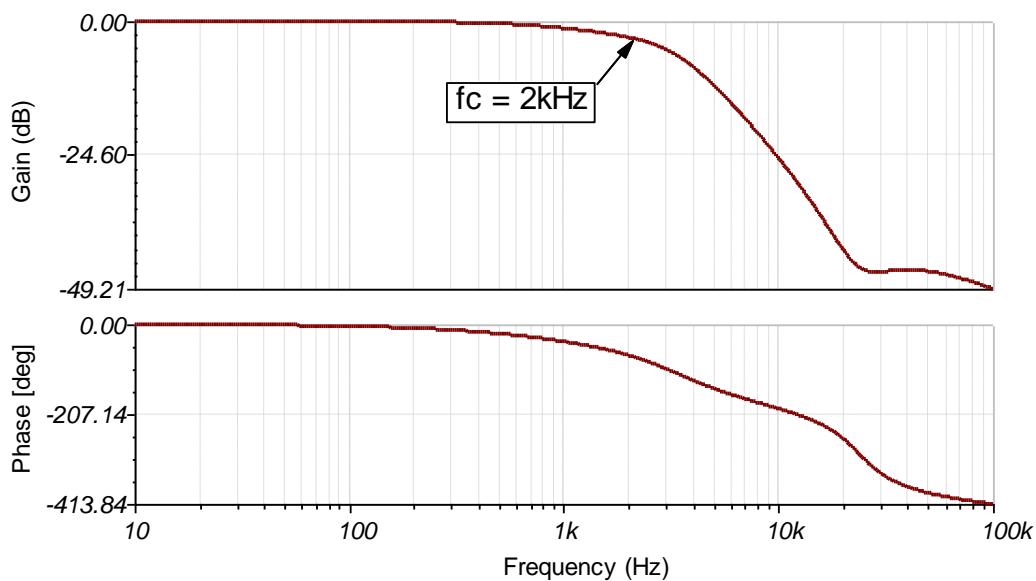
The following graph shows a linear output response for inputs from 0 to 3.3V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to [Determining a SAR ADC's Linear Range when using Operational Amplifiers](#) for detailed theory on this subject.



AC Transfer Characteristics

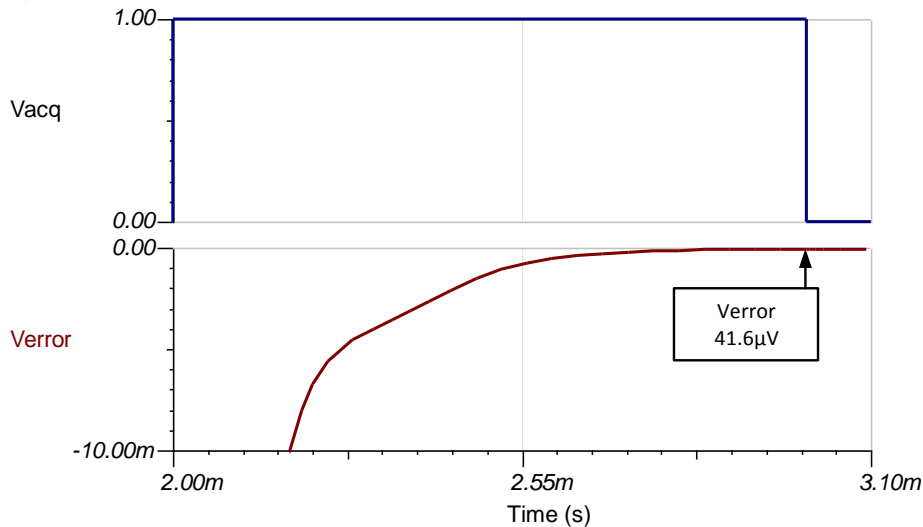
The bandwidth simulation includes the effects of the amplifier output impedance and the RC charge bucket circuit (R_{filt} and C_{filt}). The bandwidth of the RC circuit is shown in the following equation to be 1.56kHz. The simulated bandwidth of 2kHz includes effects from the output impedance interacting with the impedance of the load. See [TI Precision Labs - Op Amps: Bandwidth 1](#) for more details on this subject.

$$f_c = \frac{1}{2 \times \pi \times R_{\text{filt}} \times C_{\text{filt}}} = \frac{1}{2 \times \pi \times (200\text{k}\Omega) \times (510\text{pF})} = 1.56\text{kHz}$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of an LSB (402µV). Refer to [Introduction to SAR ADC Front-End Component Selection](#) for detailed theory on this subject.



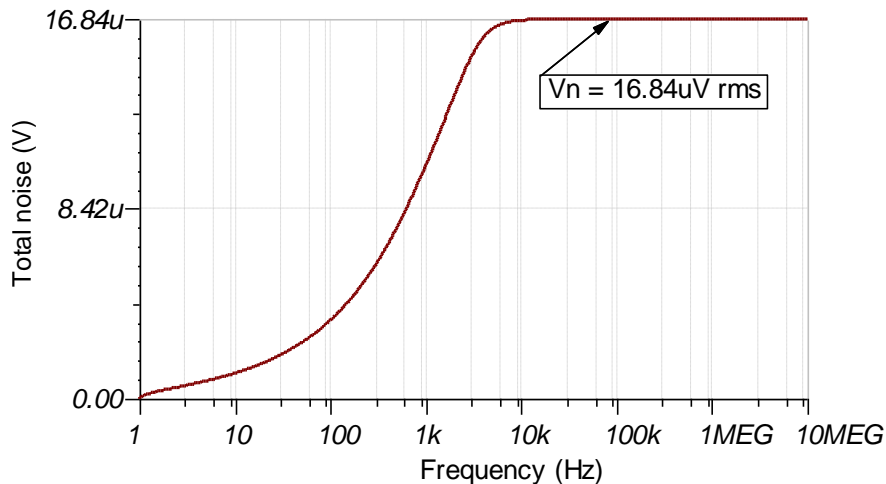
Noise Simulation

This section walks through a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \times \pi \times R_{fit} \times C_{fit}} = \frac{1}{2 \times \pi \times 200k\Omega \times 510pF} = 1560Hz$$

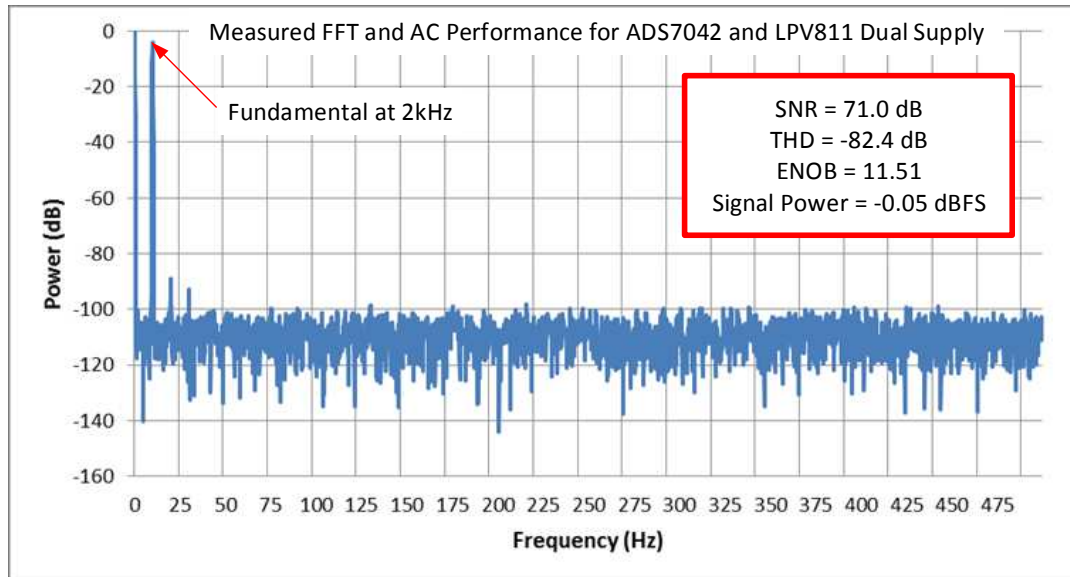
$$E_n = e_{n811} \times \sqrt{K_n \times f_c} = \frac{340nV}{\sqrt{Hz}} \times \sqrt{1.57 \times 1560Hz} = 16.8\mu V$$

Note that the calculated and simulated values match well. Refer to [Calculating the Total Noise for ADC Systems](#) for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM with a 10-Hz input sine wave. The AC performance indicates SNR = 71.0dB, THD = -82.4dB, and ENOB (effective number of bits) = 11.51, which matches well with the specified performance of the ADC, SNR = 70dB and THD = -80dB. This test was performed at room temperature. See [Introduction to Frequency Domain](#) for more details on this subject.



Design Featured Devices

| Device | Key Features | Link | Similar Devices |
|------------------------|--|--|--|
| ADS7042 ⁽¹⁾ | 12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD reference input range 1.6 V to 3.6 V. | www.ti.com/product/ADS7042 | www.ti.com/adcs |
| LPV811 ⁽²⁾ | 8-kHz bandwidth, rail-to-rail output, 450-nA supply current, unity gain stable | www.ti.com/product/LPV811 | www.ti.com/opamp |

⁽¹⁾ The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

⁽²⁾ The LPV811 is also commonly used in low-speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across the entire ADC input range.

Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

Link to Key Files (TINA)

Design files for this circuit – <http://www.ti.com/lit/zip/sbam342>.

Revision History

| Revision | Date | Change |
|----------|------------|--|
| A | March 2019 | Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page. |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated