LM321LV, LM358LV, LM324LV Industry Standard, Low Voltage Operational Amplifiers

1 Features

- Industry standard amplifier for cost-sensitive systems
- Low input offset voltage: ±1 mV
- Common-mode voltage range includes ground
- Unity-gain bandwidth: 1 MHz
- Low broadband noise: 40 nV/√Hz
- Low quiescent current: 90 μA/Ch
- Unity-gain stable
- Operational at supply voltages from 2.7 V to 5.5 V
- Offered in single, dual, and quad channel variants
- Robust ESD specification: 2-kV HBM
- Extended temperature range: –40°C to 125°C

2 Applications

- Cordless appliances
- Uninterruptible power supply
- Battery pack, charger, and test equipment
- Power supply modules
- Environmental sensors signal conditioning
- Field transmitter: temperature sensors
- Oscilloscopes, digital multimeters, test equipment
- Rack mount server
- HVAC: heating, ventilating, and air conditioning
- DC motor control
- Low-side current sensing

3 Description

The LM3xxLV family includes the single LM321LV, dual LM358LV, and quad LM324LV operational amplifiers, or op amps. The devices operate from a low voltage of 2.7 V to 5.5 V.

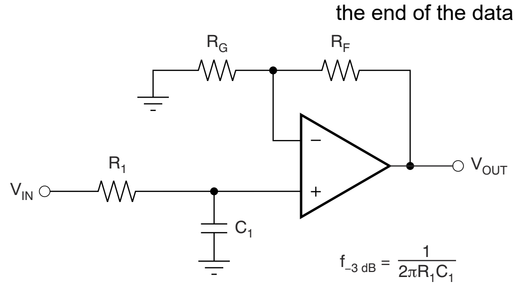
These op amps supply an alternative to the LM321, LM358, and LM324 in low-voltage applications that are sensitive to cost. Some applications are large appliances, smoke detectors, and personal electronics. The LM3xxLV devices supply better performance than the LM3xx devices at low voltage, and have lower power consumption. The op amps are stable at unity gain, and do not have reverse phase in overdrive conditions. The design for ESD gives the LM3xxLV family an HBM specification for a minimum of 2 kV.

The LM3xxLV family is available in packages that have industry standards. The packages include SOT-23, SOIC, VSSOP, and TSSOP packages.

Device Information

PART NUMBER[1]	PACKAGE	BODY SIZE (NOM)
LM321LV	SOT-23 (5)	1.60 mm × 2.90 mm
	SC70 (5)	1.25 mm × 2.00 mm
LM358LV	SOIC (8)	3.91 mm × 4.90 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LM324LV	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	SOT-23 (14)	4.20 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2019) to Revision E (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added SOT-23 (DYY) package to *Device Information* table	1
• Added DYY (SOT-23) information to *Pin Configuration and Functions* section	3
• Added DYY (SOT-23) to *Thermal Information: LM324LV* table	7

Changes from Revision C (May 2019) to Revision D (September 2019)	Page
• Deleted all preview notations in data sheet for SOT-23 (DDF) package	1

Changes from Revision B (February 2019) to Revision C (May 2019)	Page
• Added SOT-23 (DDF) package to *Device Information* table	1
• Added DDF (SOT-23) information to *Pin Configuration and Functions* section	3
• Added DDF (SOT-23) to *Thermal Information: LM358LV* table	7

Changes from Revision A (January 2019) to Revision B (February 2019)	Page
• Changed LM321LVIDBV (SOT-23) pinout diagram to match the LM321LVIDCK (SC70) pinout	3

Changes from Revision * (September 2018) to Revision A (January 2019)	Page
• Changed data sheet title from *LM3xxLV...* to *LM321LV, LM358LV, LM324LV...*	1

5 Pin Configuration and Functions

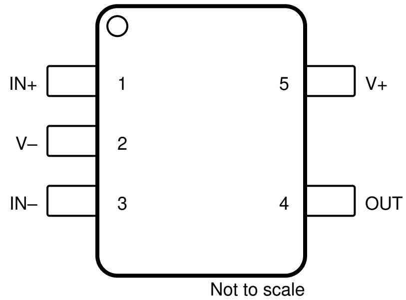


**Figure 5-1. LM321LV DBV and DCK Package
5-Pin SOT-23 and SC70
(Top View)**

Table 5-1. Pin Functions: LM321LV

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	3	I	Inverting input
IN+	1	I	Noninverting input
OUT	4	O	Output
V–	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	I	Positive (high) supply

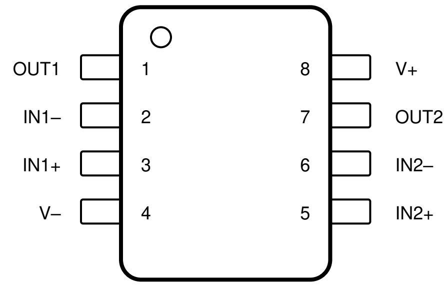


Figure 5-2. LM358LV D, DGK, PW, and DDF Package 8-Pin SOIC, VSSOP, TSSOP, and SOT-23 (Top View)

Table 5-2. Pin Functions: LM358LV

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I or —	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

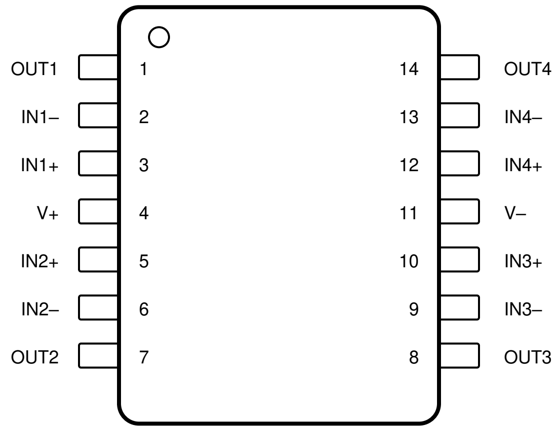


Figure 5-3. LM324LV D, PW, and DYY Package 14-Pin SOIC, TSSOP, and SOT-23 (Top View)

Table 5-3. Pin Functions: LM324LV

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
Supply voltage, ([V+] – [V–])			0	6	V
Signal input pins	Voltage[(2)]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current[(2)]		–10	10	mA
Output short-circuit[(3)]			Continuous		
Operating, T_A			–55	150	°C
Operating junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage [(V+) – (V–)]	2.7	5.5	V
V_{IN}	Input pin voltage range	(V–) – 0.1	(V+) – 1	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information: LM321LV

THERMAL METRIC[(1)]		LM321LV		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.9	239.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.8	148.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.9	82.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	77.2	54.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	100.4	81.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Thermal Information: LM358LV

THERMAL METRIC[(1)]		LM358LV				UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.9	201.2	200.7	183.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.8	85.7	95.4	112.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	129.7	122.9	128.6	98.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26	21.2	27.2	18.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	127.9	121.4	127.2	97.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.6 Thermal Information: LM324LV

THERMAL METRIC[(1)]		LM324LV			UNIT
		D (SOIC)	PW (TSSOP)	DYY (SOT-23)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.1	148.3	154.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.8	68.1	86.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	92.7	67.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.5	16.9	9.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.1	91.8	67.1	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 5.5 V (±1.35 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±1	±3	mV
		V_S = 5 V, T_A = –40°C to 125°C			±5	
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to 125°C		±4		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{CM} = (V–)	80	100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal	(V–) – 0.1		(V+) – 1	V
CMRR	Common-mode rejection ratio	V_S = 2.7 V, (V–) – 0.1 V < V_{CM} < (V+) – 1 V, T_A = –40°C to 125°C		84		dB
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1 V, T_A = –40°C to 125°C	63	92		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±15		pA
I_{OS}	Input offset current			±5		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		5.1		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		40		$nV/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			5.5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 2.7 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		110		dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		125		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V		1		MHz
$φ_m$	Phase margin	V_S = 5.5 V, G = 1		75		°
SR	Slew rate	V_S = 5 V		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = 1, C_L = 100 pF		4		µs
		To 0.01%, V_S = 5 V, 2-V step, G = 1, C_L = 100 pF		5		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		1		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = 1, f = 1 kHz, 80-kHz measurement BW		0.005%		
OUTPUT						
V_{OH}	Voltage output swing from positive supply	R_L ≥ 2 kΩ, T_A = –40°C to 125°C	1			V
V_{OL}	Voltage output swing from negative supply	R_L ≤ 10 kΩ, T_A = –40°C to 125°C		40	75	mV
I_{SC}	Short-circuit current	V_S = 5.5 V		±40		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 1 MHz		1200		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7 (±1.35)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		90	150	µA
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to 125°C			160	

6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

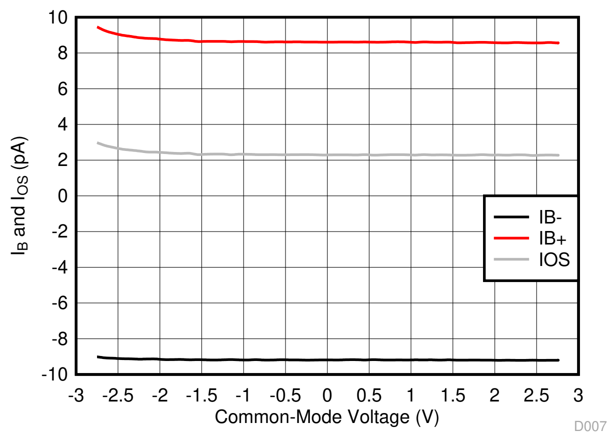


Figure 6-1. I_B and I_{OS} vs Common-Mode Voltage

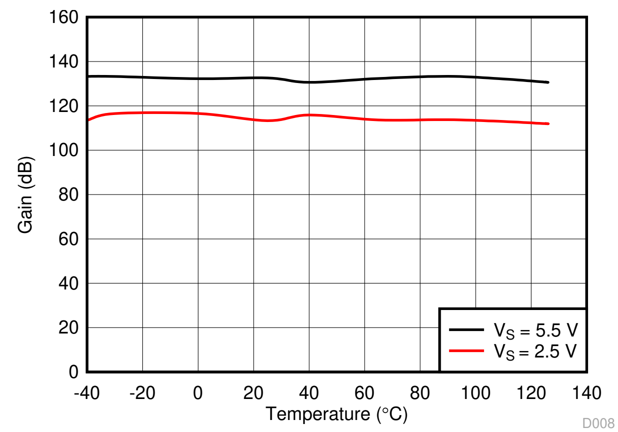
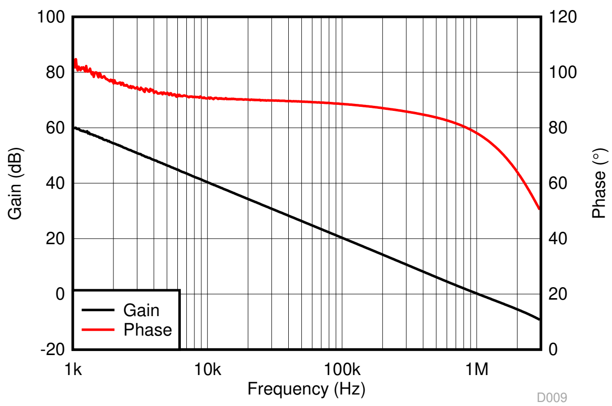


Figure 6-2. Open-Loop Gain vs Temperature



C_L = 10 pF

Figure 6-3. Open-Loop Gain and Phase vs Frequency

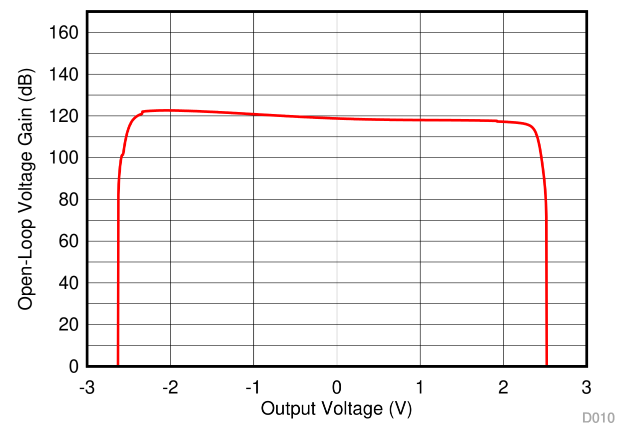
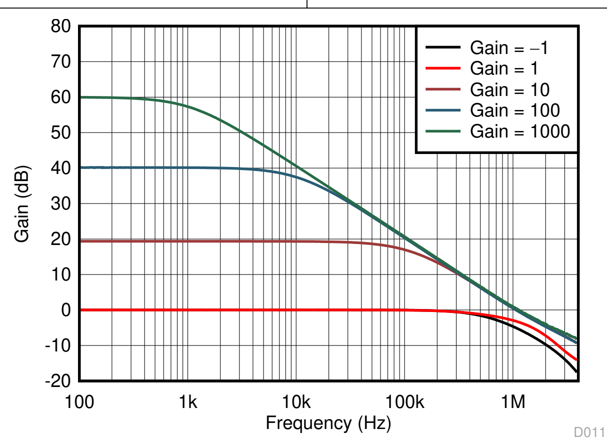


Figure 6-4. Open-Loop Voltage Gain vs Output Voltage



C_L = 10 pF

Figure 6-5. Closed-Loop Gain vs Frequency

6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

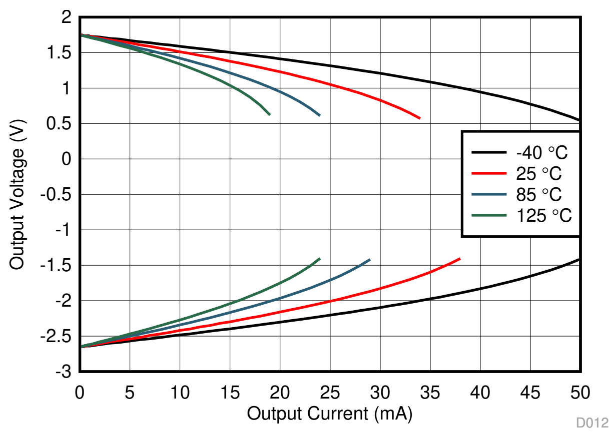


Figure 6-6. Output Voltage vs Output Current (Claw)

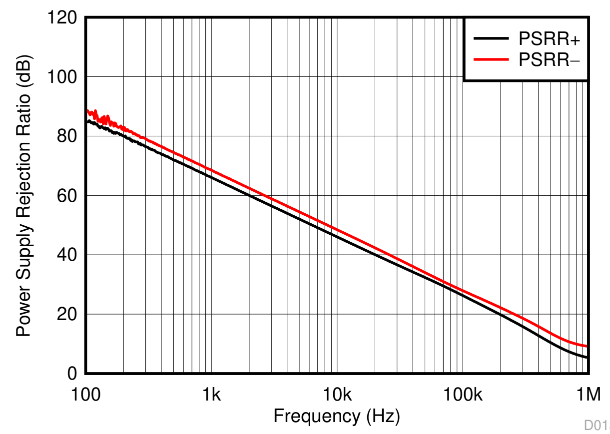
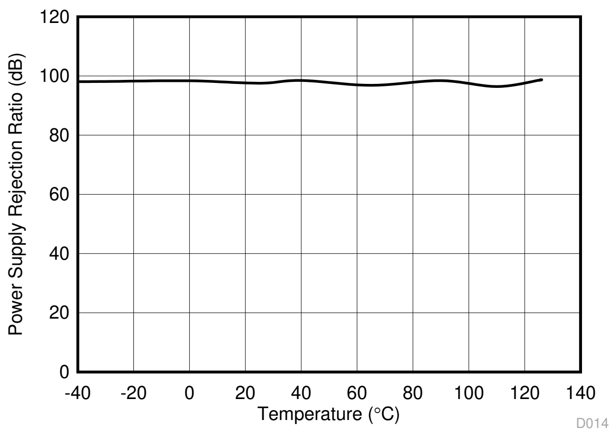


Figure 6-7. PSRR vs Frequency



V_S = 2.7 V to 5.5 V

Figure 6-8. DC PSRR vs Temperature

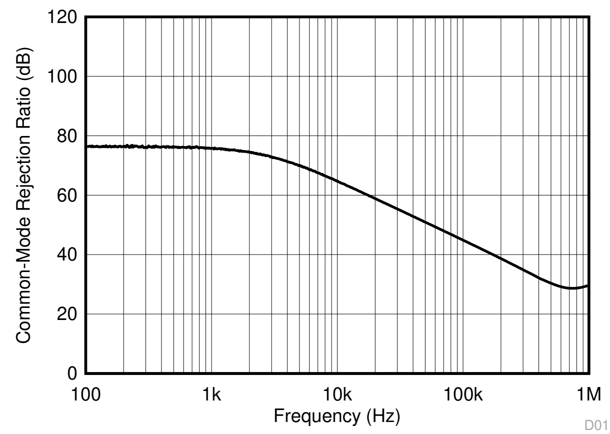
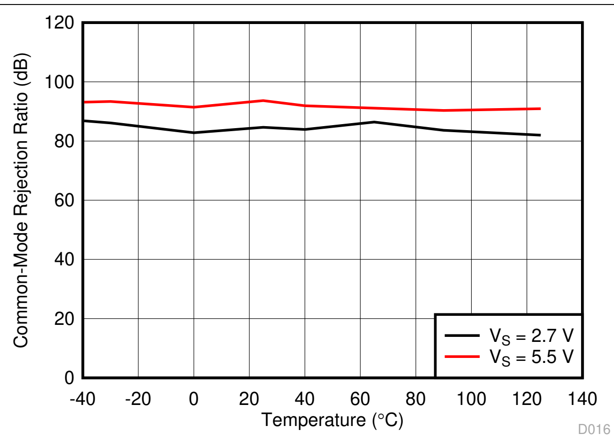


Figure 6-9. CMRR vs Frequency



V_{CM} = (V–) – 0.1 V to (V+) – 1.5 V

Figure 6-10. DC CMRR vs Temperature

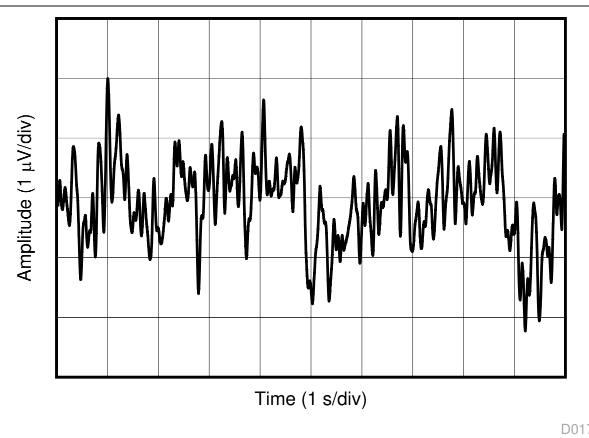


Figure 6-11. 0.1-Hz to 10-Hz Integrated Voltage Noise

6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

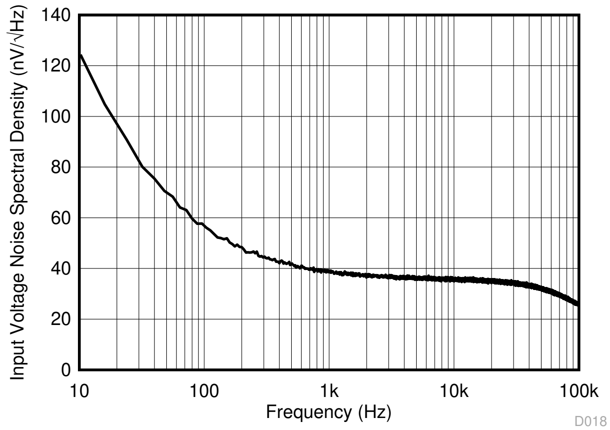
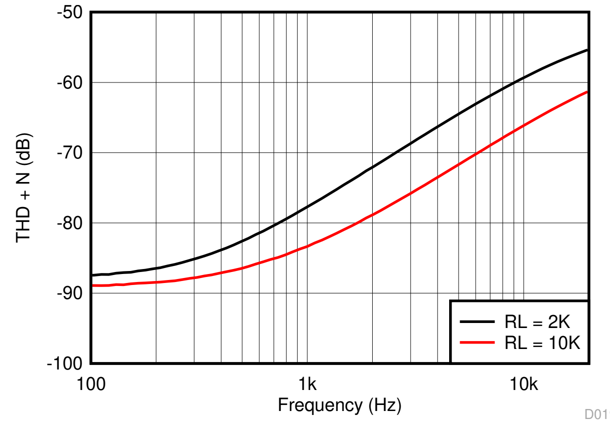
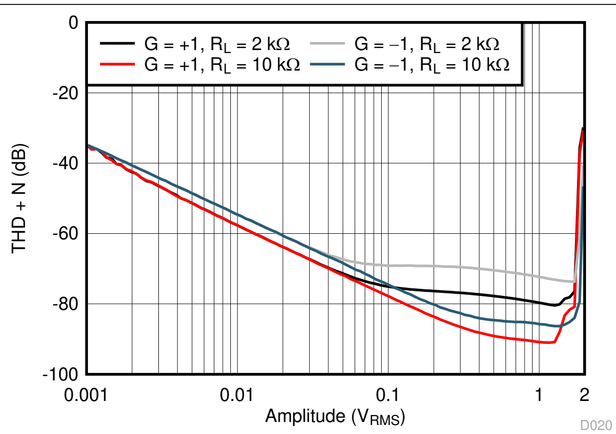


Figure 6-12. Input Voltage Noise Spectral Density



V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

Figure 6-13. THD + N vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz f = 1 kHz

Figure 6-14. THD + N vs Amplitude

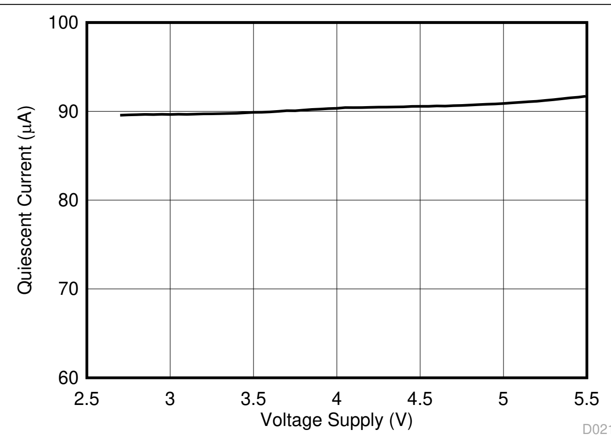


Figure 6-15. Quiescent Current vs Supply Voltage

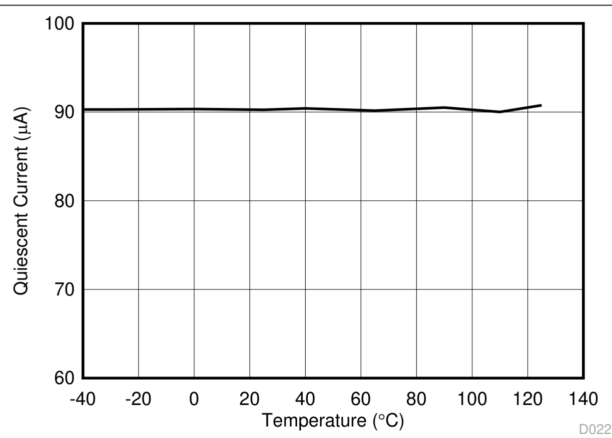


Figure 6-16. Quiescent Current vs Temperature

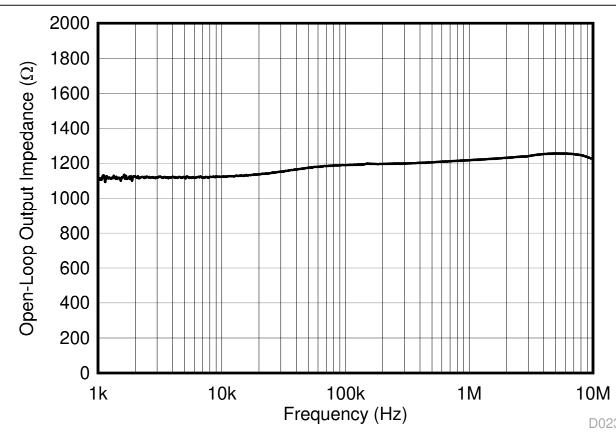
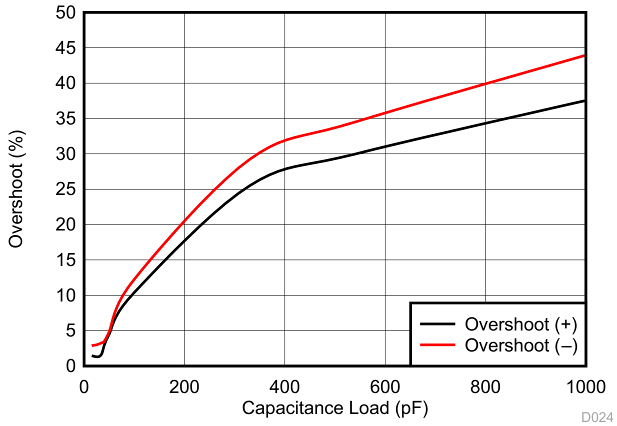


Figure 6-17. Open-Loop Output Impedance vs Frequency

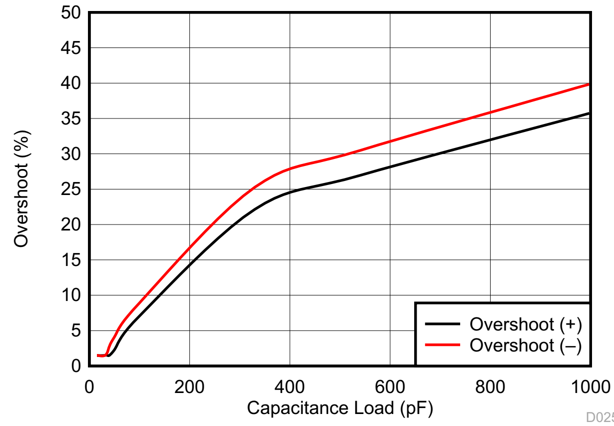
6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1 V_{IN} = 100 mVpp

Figure 6-18. Small Signal Overshoot vs Capacitive Load



G = –1 V_{IN} = 100 mVpp

Figure 6-19. Small Signal Overshoot vs Capacitive Load

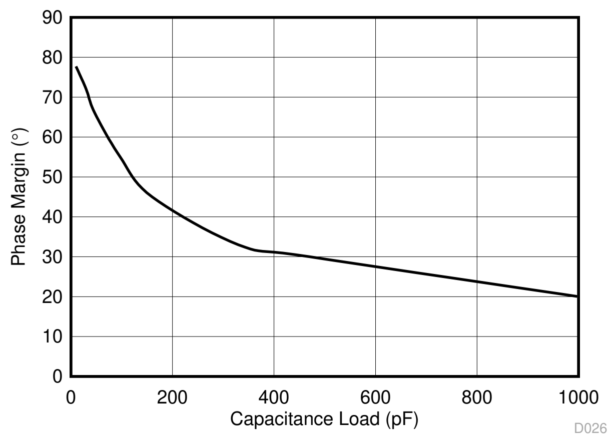
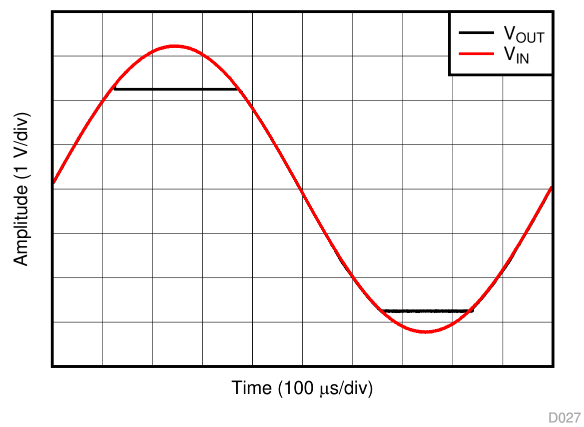
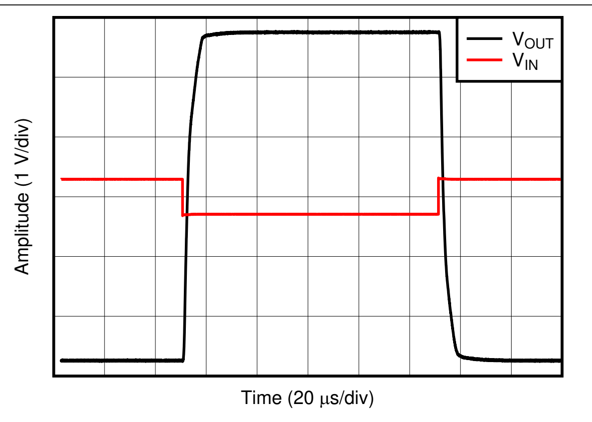


Figure 6-20. Phase Margin vs Capacitive Load



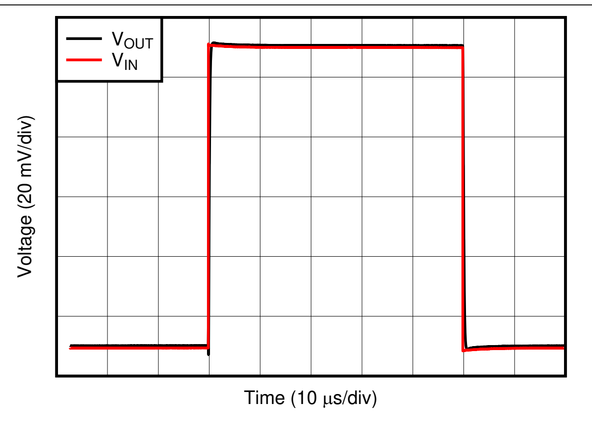
G = 1 V_{IN} = 6.5 V_{PP}

Figure 6-21. No Phase Reversal



G = –10 V_{IN} = 600 mV_{PP}

Figure 6-22. Overload Recovery

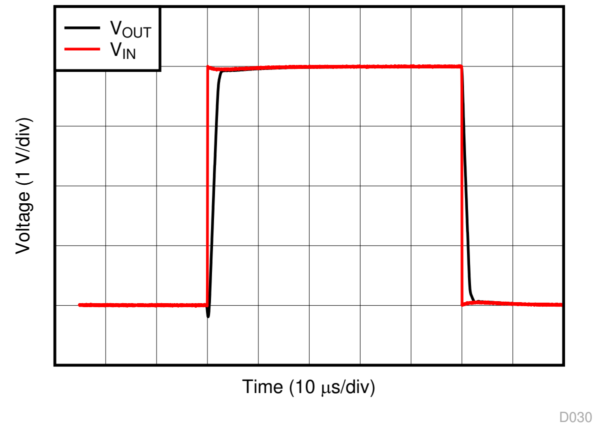


G = 1 V_{IN} = 100 mV_{PP} C_L = 10 pF

Figure 6-23. Small-Signal Step Response

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

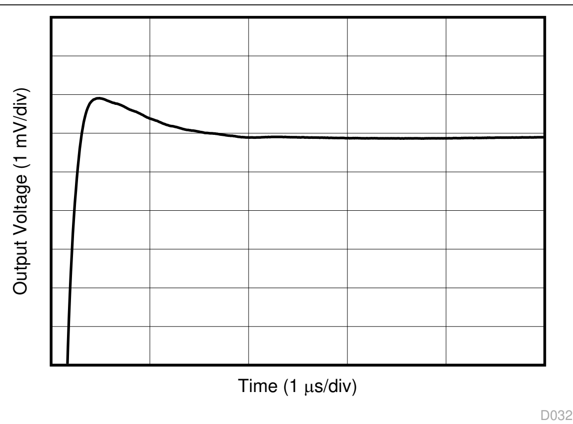


G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

Figure 6-24. Large-Signal Step Response

G = 1 C_L = 100 pF   2-V step

Figure 6-25. Large-Signal Settling Time (Negative)



G = 1 C_L = 100 pF   2-V step

Figure 6-26. Large-Signal Settling Time (Positive)

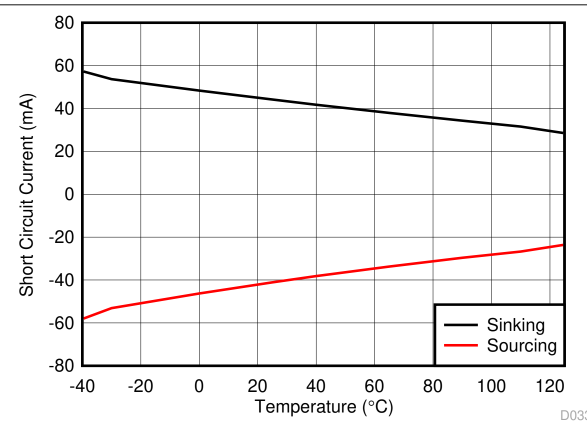


Figure 6-27. Short-Circuit Current vs Temperature

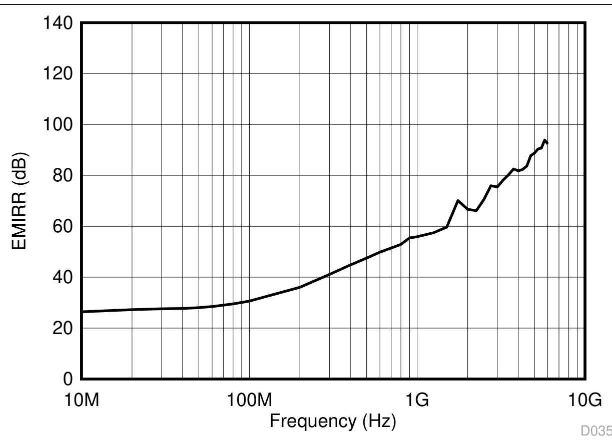


Figure 6-28. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

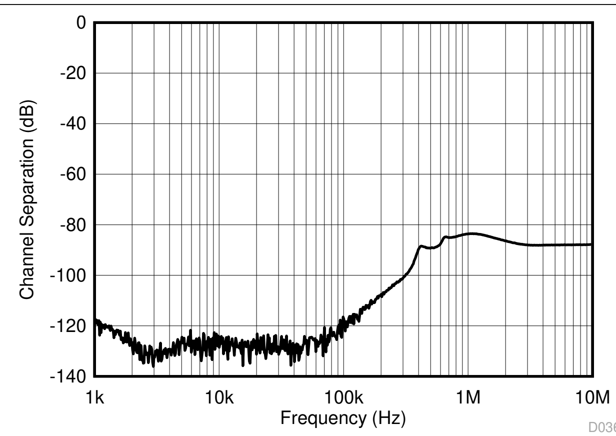


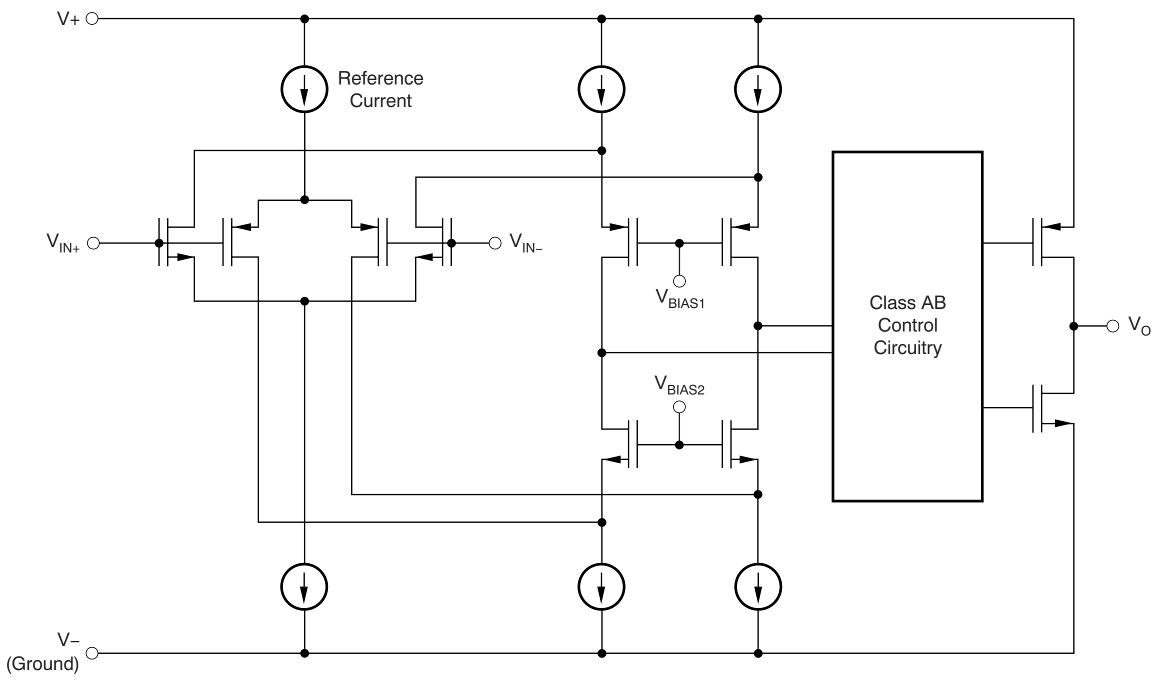
Figure 6-29. Channel Separation

7 Detailed Description

7.1 Overview

The LM3xxLV family of low-power op amps is intended for cost-optimized systems. These devices operate from 2.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the LM3xxLV family to be used in many single-supply applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The LM3xxLV family of op amps is specified for operation from 2.7 V to 5.5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Electrical Characteristics* section.

7.3.2 Common-Mode Input Range Includes Ground

The input common-mode voltage range of the LM3xxLV family extends to the negative supply rail and within 1 V below the positive rail for the full supply voltage range of 2.7 V to 5.5 V. This performance is achieved with a P-channel differential pair, as shown in the *Functional Block Diagram*. Additionally, a complementary N-channel differential pair has been included in parallel to eliminate issues with phase reversal that are common with previous generations of op amps. However, the N-channel pair is not optimized for operation, and significant performance degradation occurs while this pair is operational. TI recommends limiting any voltage applied at the inputs to at least 1 V below the positive supply rail (V+) to ensure that the op amp conforms to the specifications detailed in the *Electrical Characteristics* section.

7.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the specified output voltage swing, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate.

Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the LM3xxLV family is typically 1 µs.

7.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can also involve the supply voltage pins. Each of these different pin functions has electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 7-1 shows the ESD circuits contained in the LM3xxLV. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

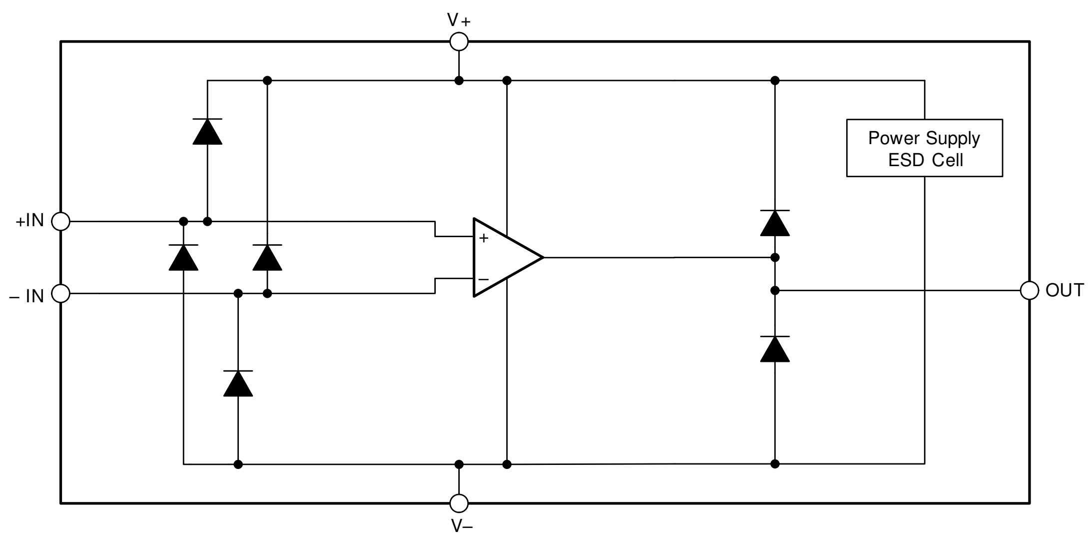


Figure 7-1. Equivalent Internal ESD Circuitry

7.3.5 EMI Susceptibility and Input Filtering

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The Figure 6-28 plot illustrates the performance of the LM3xxLV family's EMI filters across a wide range of frequencies. For more detailed information, see *EMI Rejection Ratio of Operational Amplifiers* available for download from www.ti.com.

7.4 Device Functional Modes

The LM3xxLV family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 2.7 V (±1.35 V) and 5.5 V (±2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM3xxLV devices are a family of low-power, cost-optimized operational amplifiers. The devices operate from 2.7 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail, and allows the LM3xxLV to be used in any single-supply applications.

8.2 Typical Application

Figure 8-1 shows the LM3xxLV device configured in a low-side current sensing application.

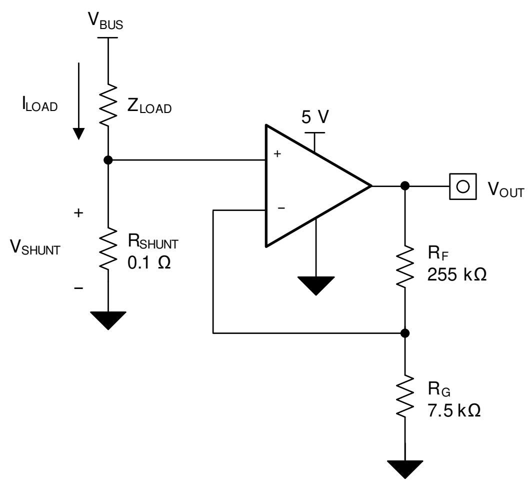


Figure 8-1. LM3xxLV Device in a Low-Side, Current-Sensing Application

8.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 3.5 V
- Maximum shunt voltage: 100 mV

8.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 8-1 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest allowable shunt resistor is shown using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the LM3xxLV device to produce an output voltage of approximately 0 V to 3.5 V. The gain needed by the LM3xxLV to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using Equation 3, the required gain is calculated to be 35 V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the LM3xxLV device to 35 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

8.2.3 Application Curve

Selecting R_F as 255 kΩ and R_G as 7.5 kΩ provides a combination that equals 35 V/V. Figure 8-2 shows the measured transfer function of the circuit shown in Figure 8-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

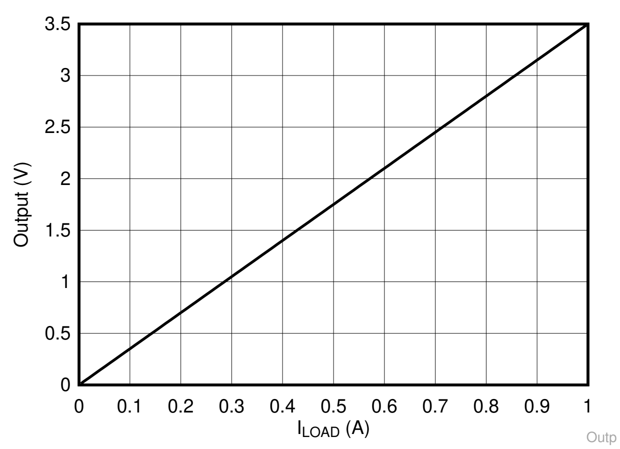


Figure 8-2. Low-Side, Current-Sense Transfer Function

9 Power Supply Recommendations

The LM3xxLV family is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Electrical Characteristics* section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

9.1 Input and ESD Protection

The LM3xxLV family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the *Section 6.1* table. Figure 9-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

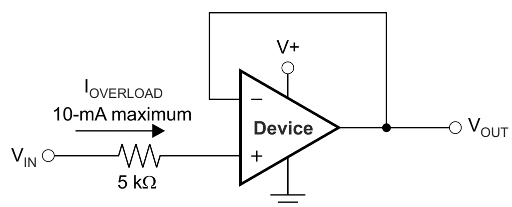


Figure 9-1. Input Current Protection

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds. Use thermal signatures or EMI measurement techniques to determine where the majority of the ground current is flowing and be sure to route this path away from sensitive analog circuitry. For more detailed information, see *Circuit Board Layout Techniques* application note.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in Figure 10-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

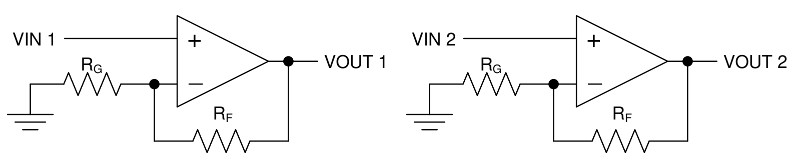


Figure 10-1. Schematic Representation for

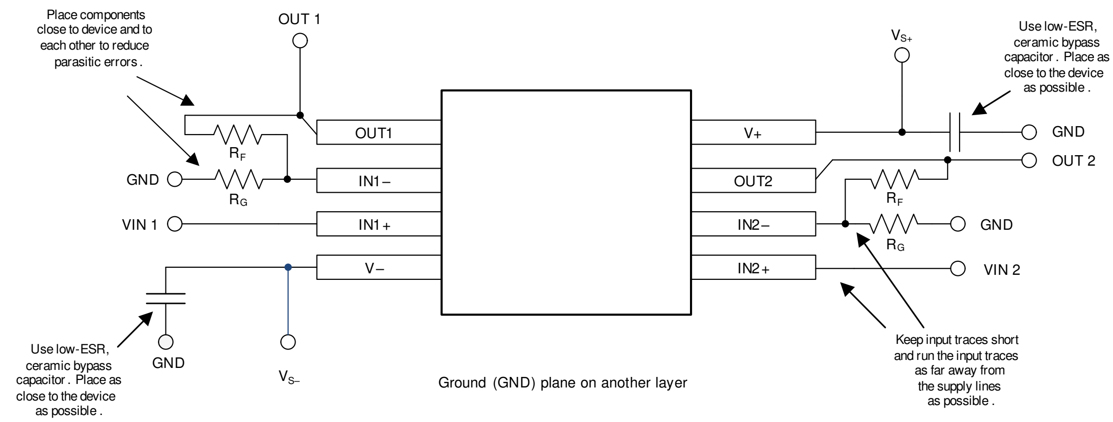


Figure 10-2. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Circuit Board Layout Techniques* application note

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM321LVIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1SPF
LM321LVIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SPF
LM321LVIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1DH
LM321LVIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1DH
LM324LVIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM324LV
LM324LVIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM324LV
LM324LVIDYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM324L
LM324LVIDYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM324L
LM324LVIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LM324LV
LM324LVIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LM324LV
LM358LVIDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L58L
LM358LVIDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L58L
LM358LVIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1PKX
LM358LVIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1PKX
LM358LVIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	L358LV
LM358LVIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	L358LV
LM358LVIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L358LV
LM358LVIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L358LV
LM358LVIPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	358LV
LM358LVIPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	358LV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

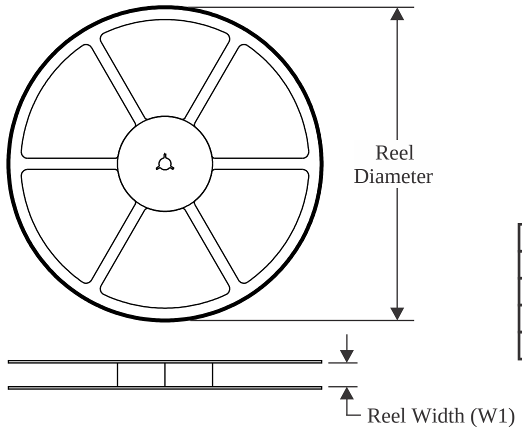
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

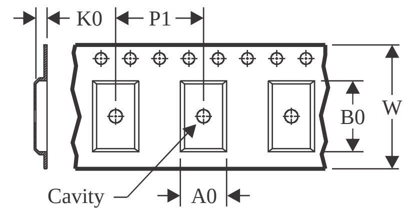
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

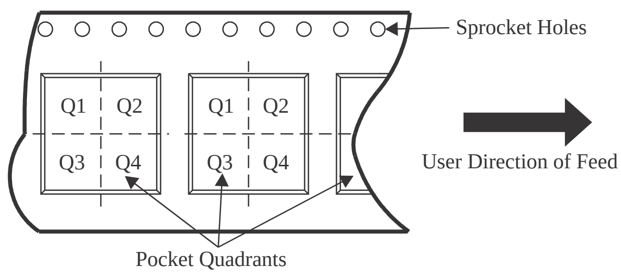
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





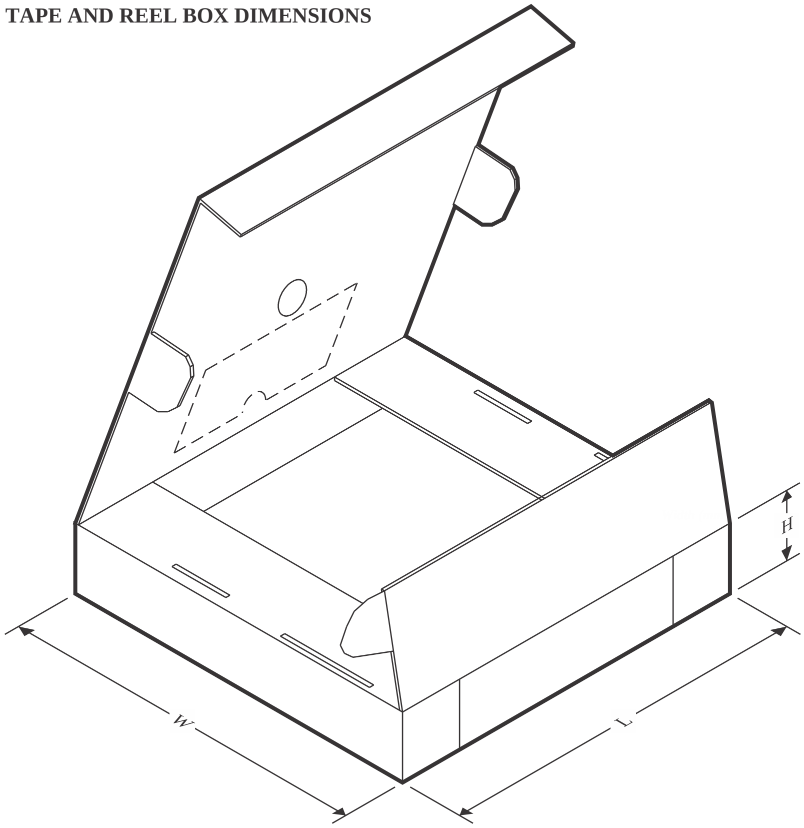
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

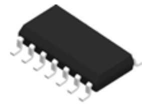
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM321LVIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321LVIDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
LM324LVIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324LVIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
LM324LVIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324LVIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM358LVIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM358LVIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358LVIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358LVIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358LVIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM321LVIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM321LVIDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
LM324LVIDR	SOIC	D	14	2500	356.0	356.0	35.0
LM324LVIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
LM324LVIPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
LM324LVIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LM358LVIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM358LVIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
LM358LVIDR	SOIC	D	8	2500	356.0	356.0	35.0
LM358LVIDRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM358LVIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

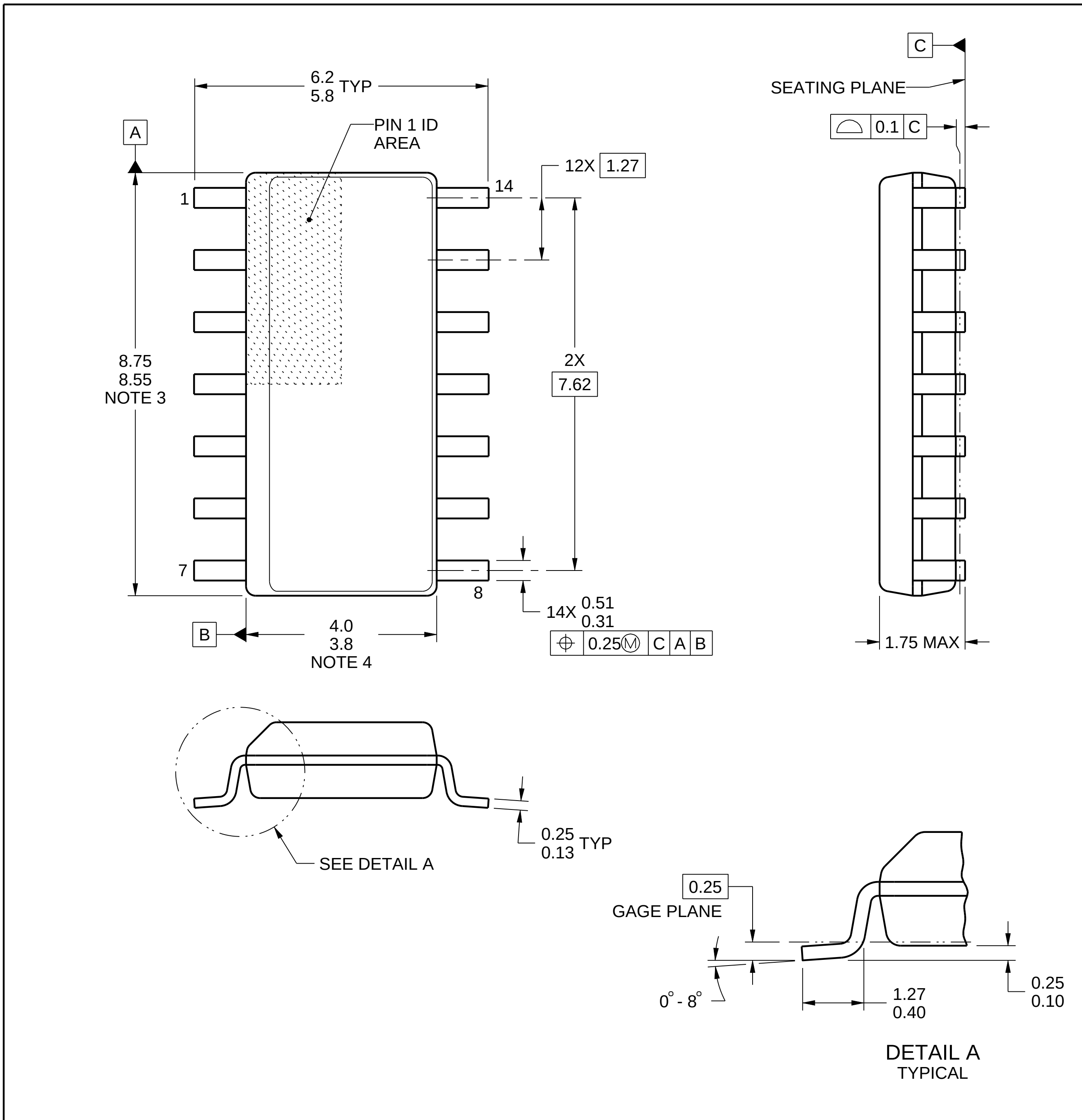


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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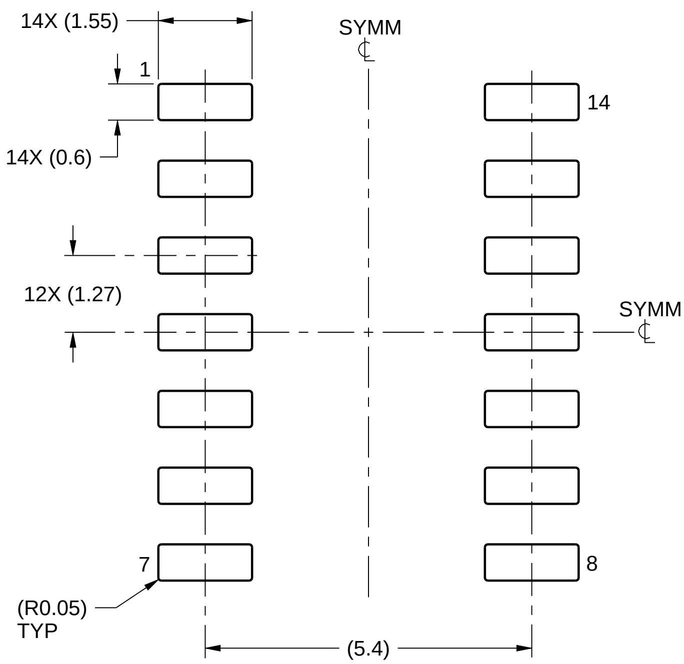
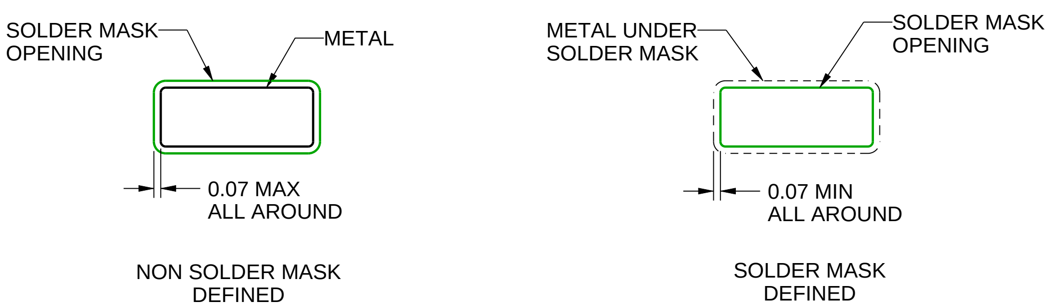
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

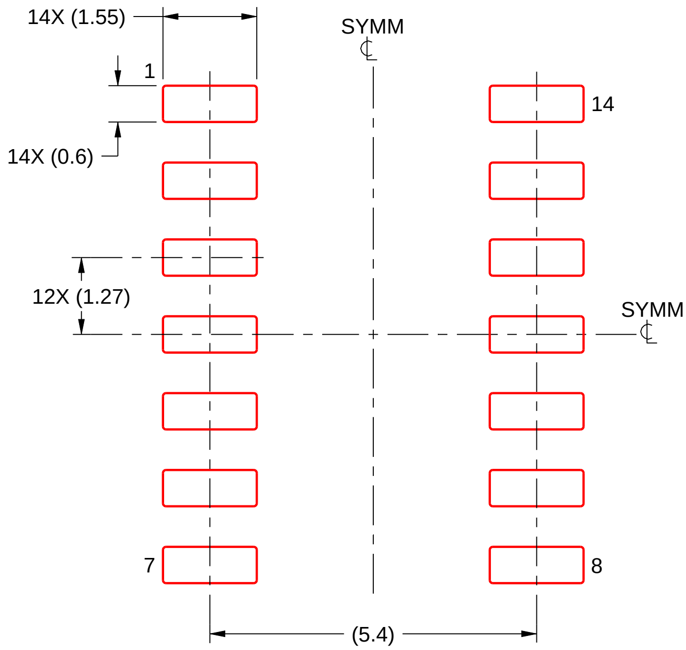


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

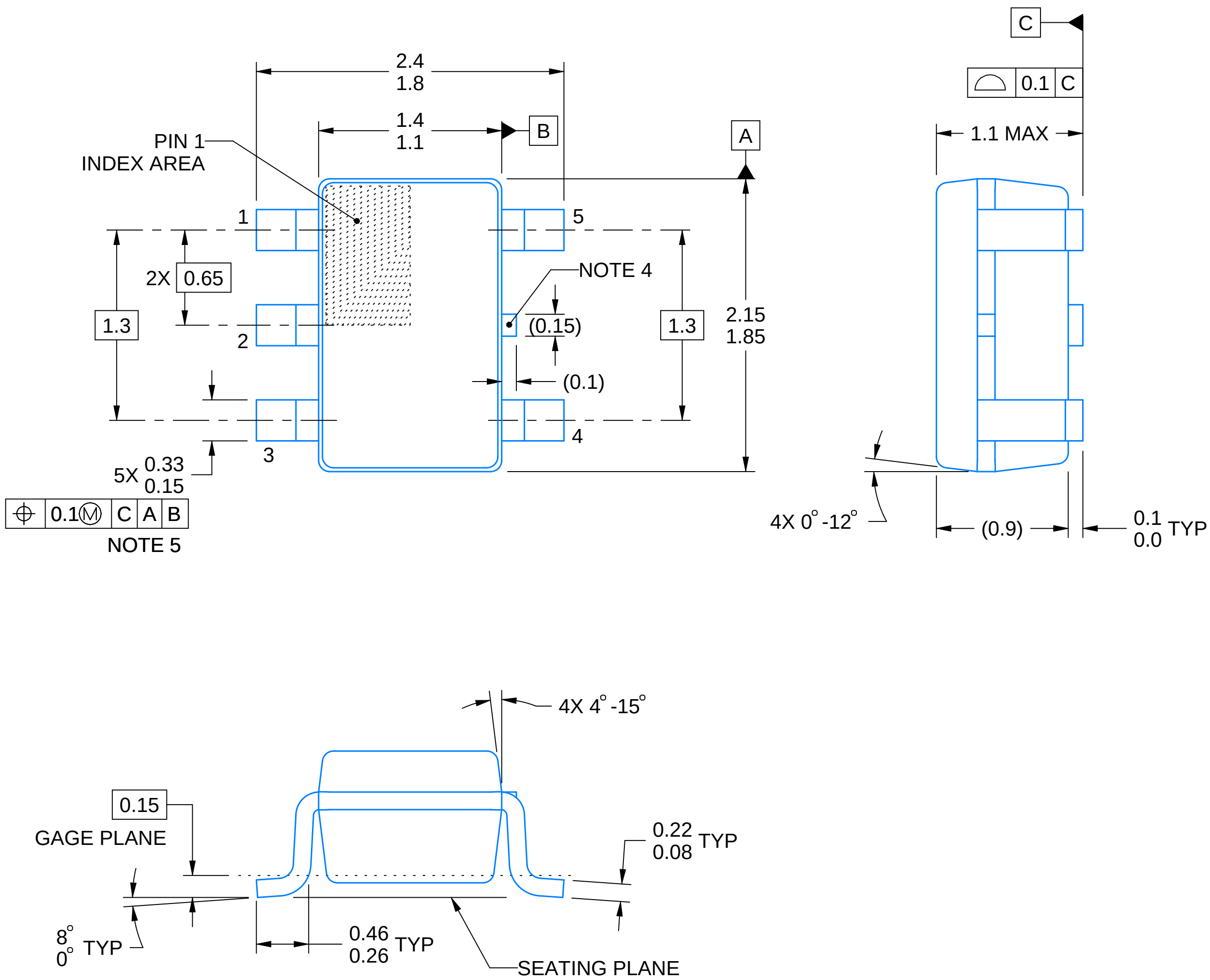


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

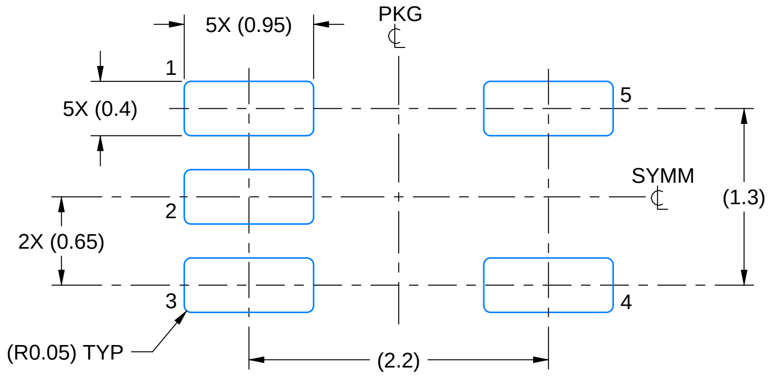
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



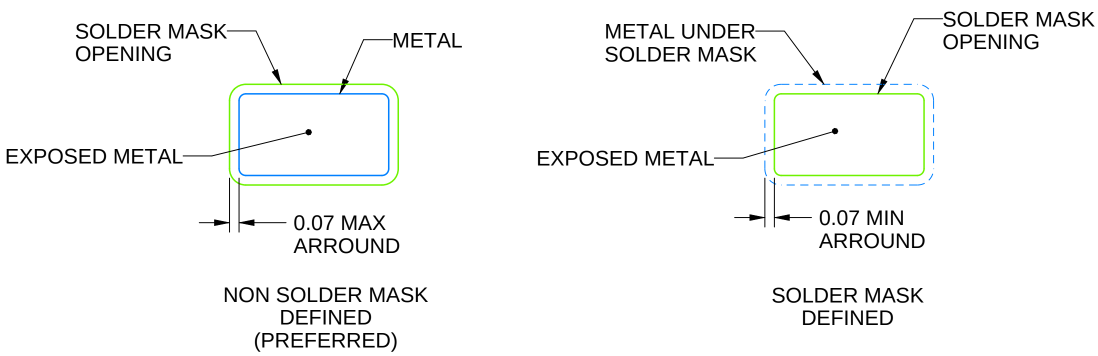
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

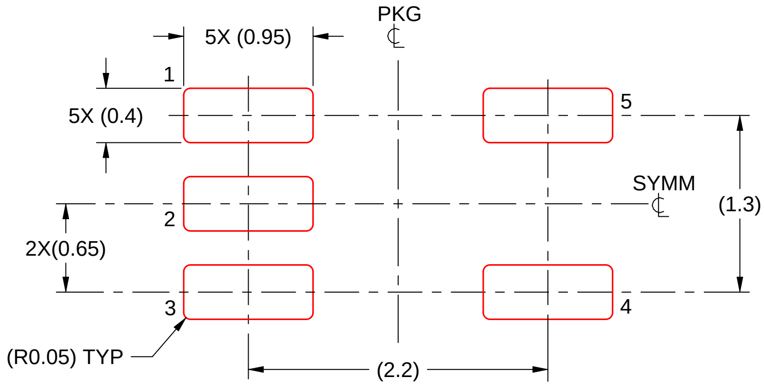


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

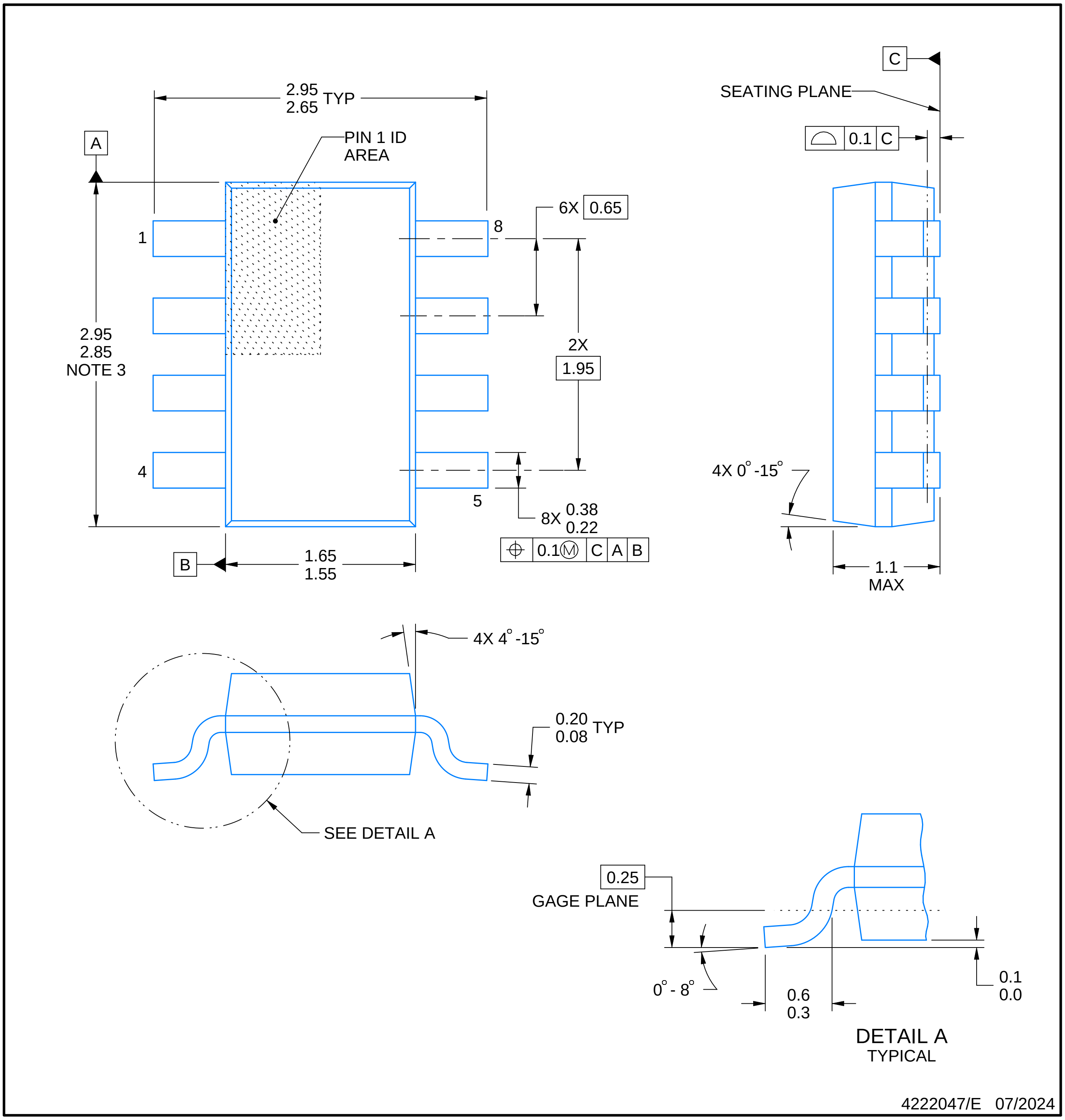


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

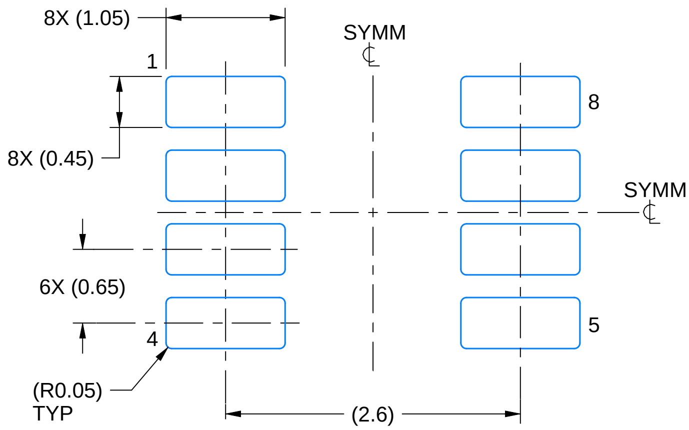
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



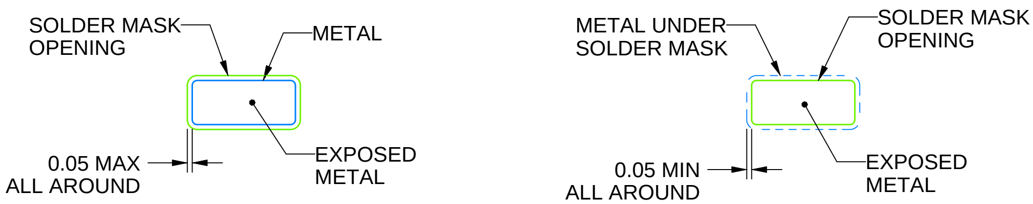
4222047/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

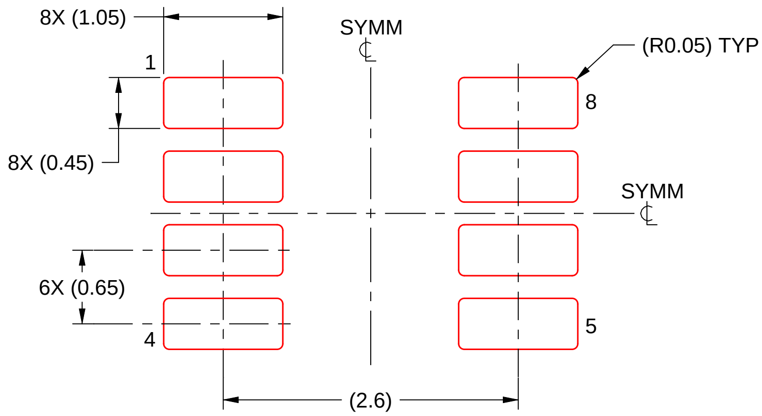
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

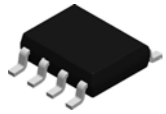


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

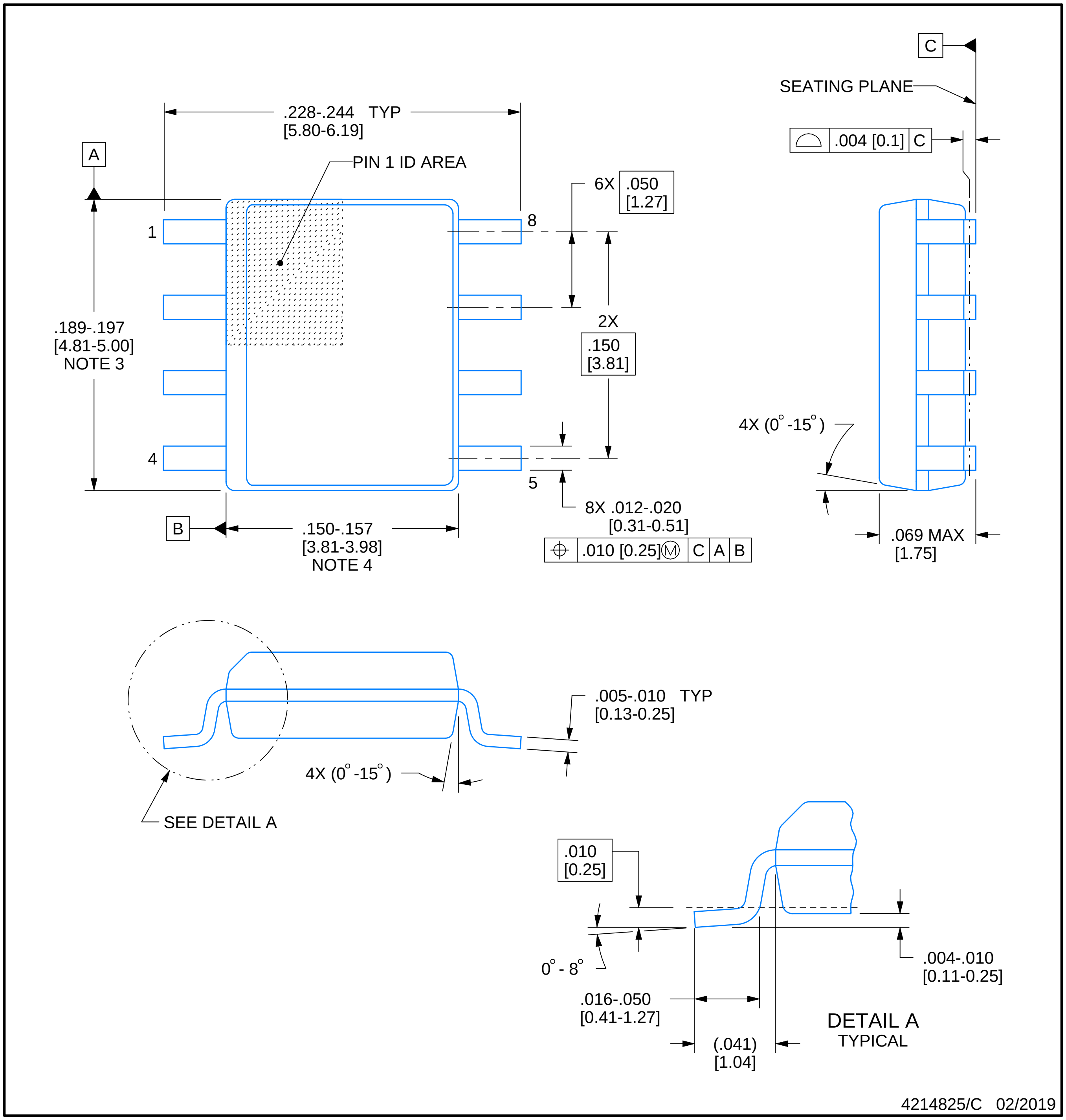


PACKAGE OUTLINE

D0008A

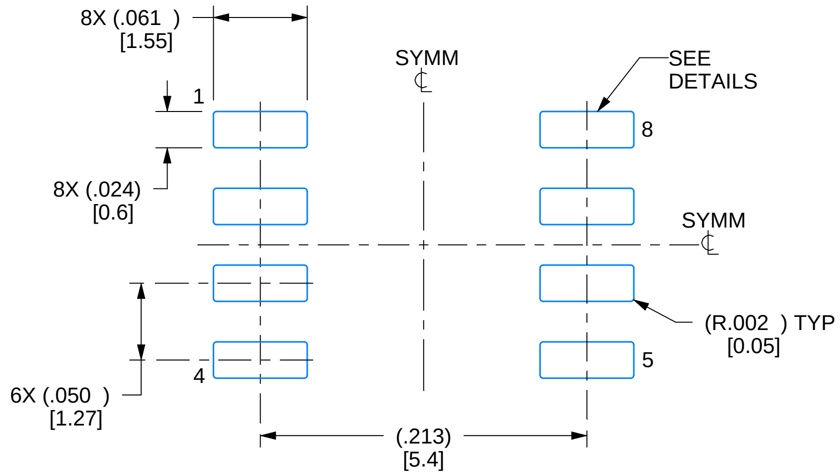
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

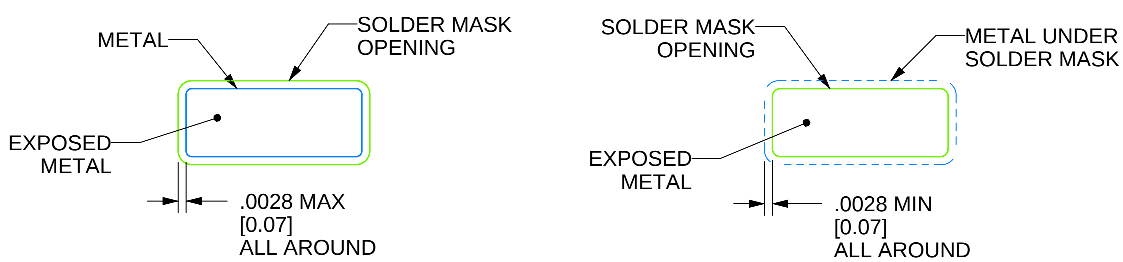


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

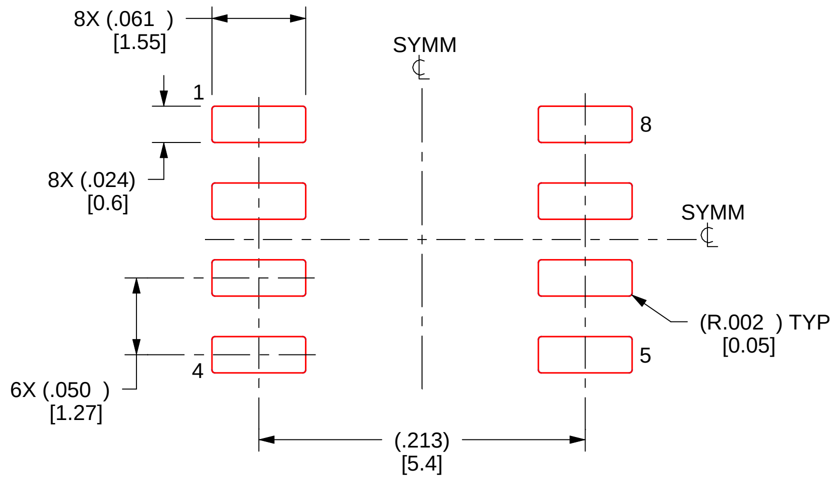
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

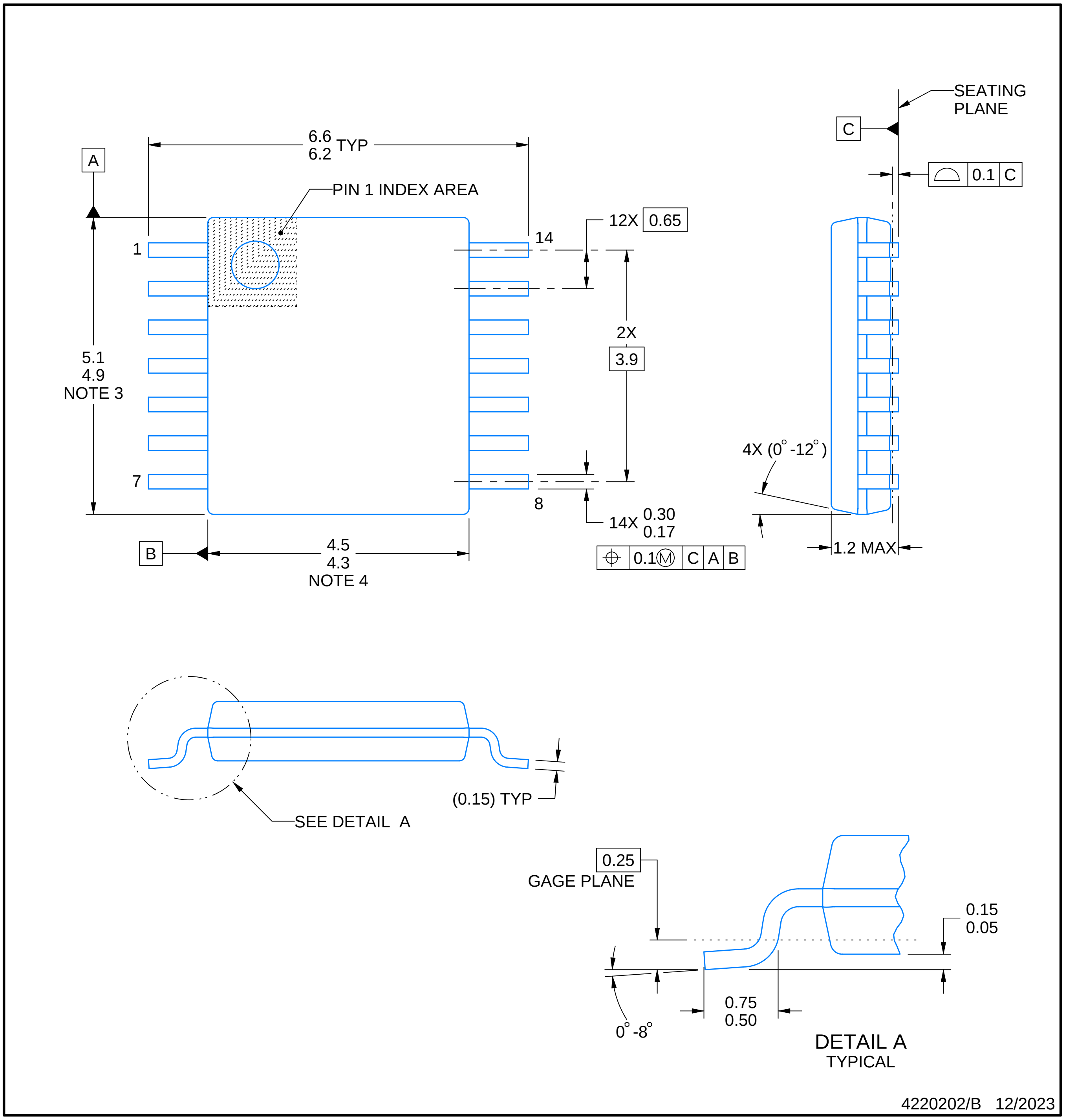


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

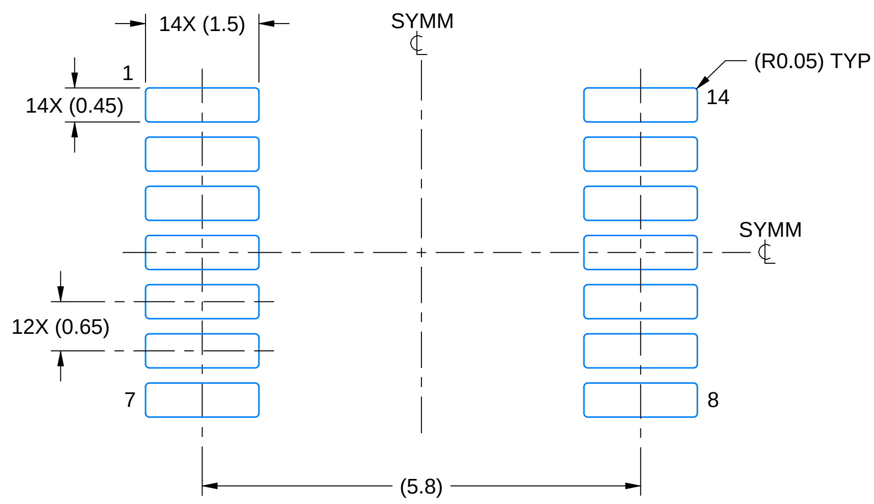
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

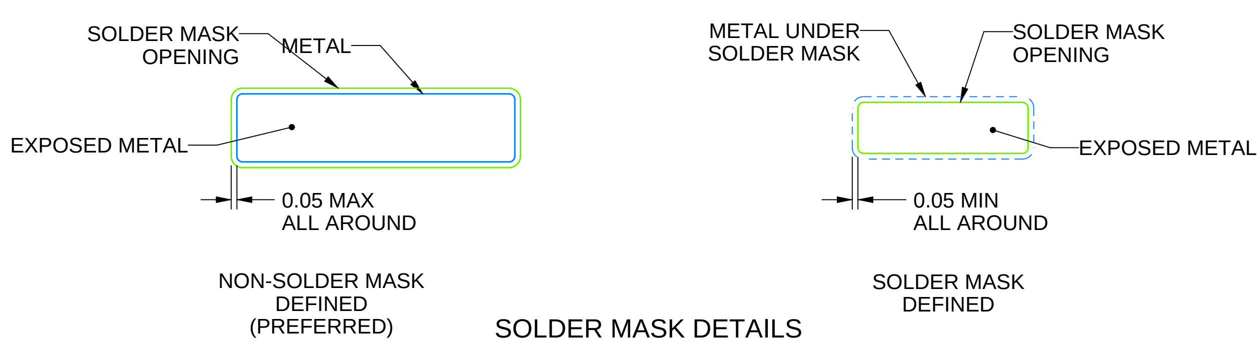


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

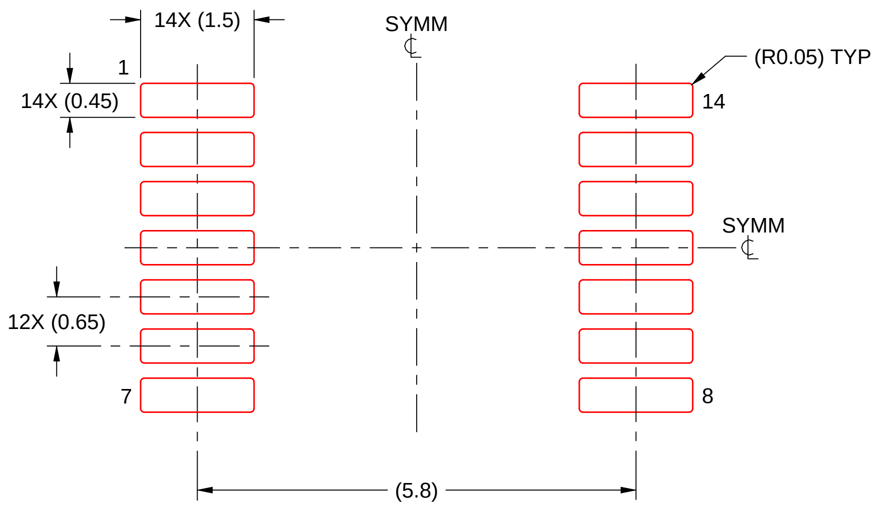


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

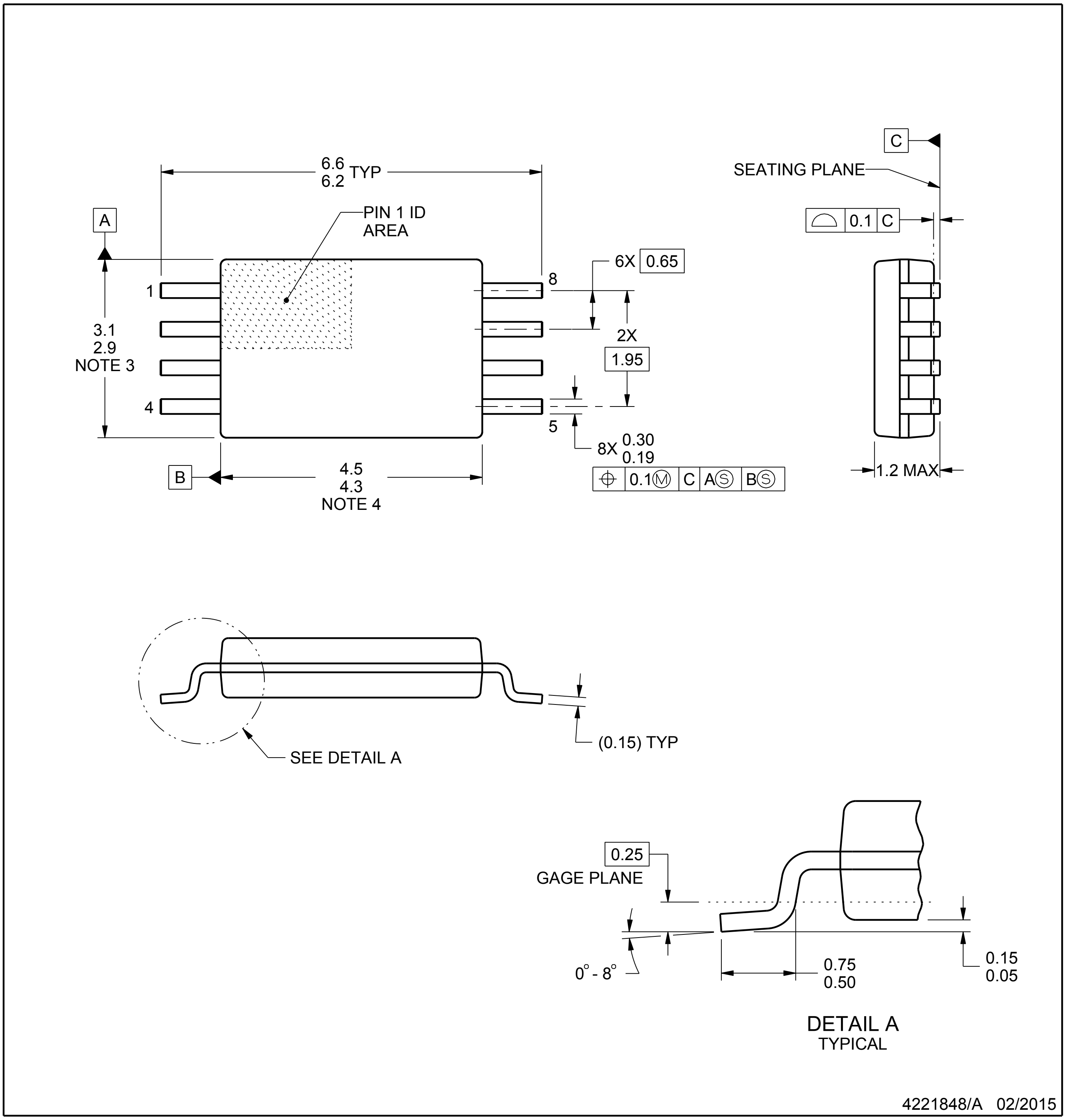


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

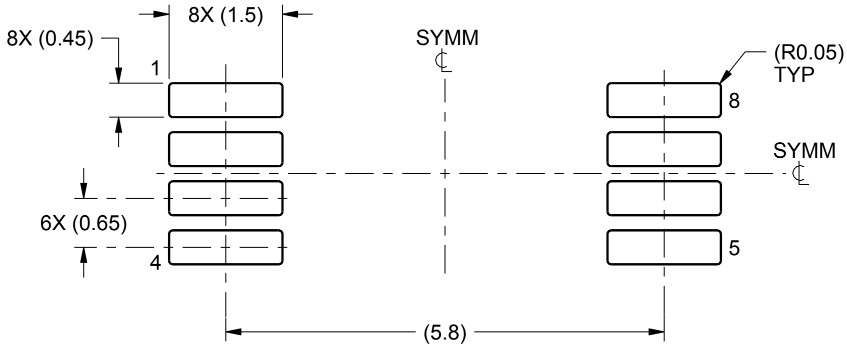
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

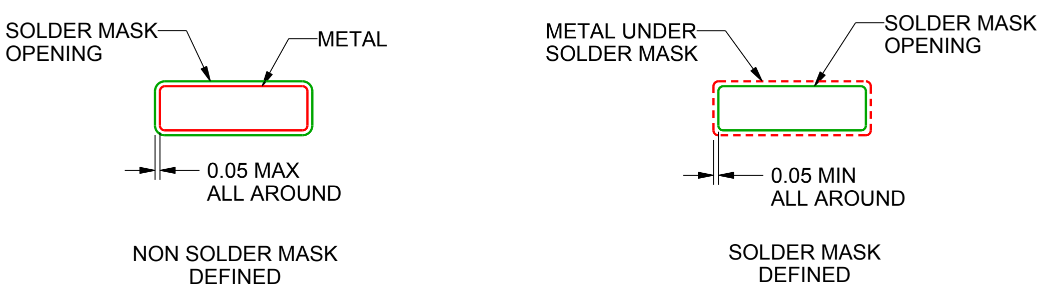


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

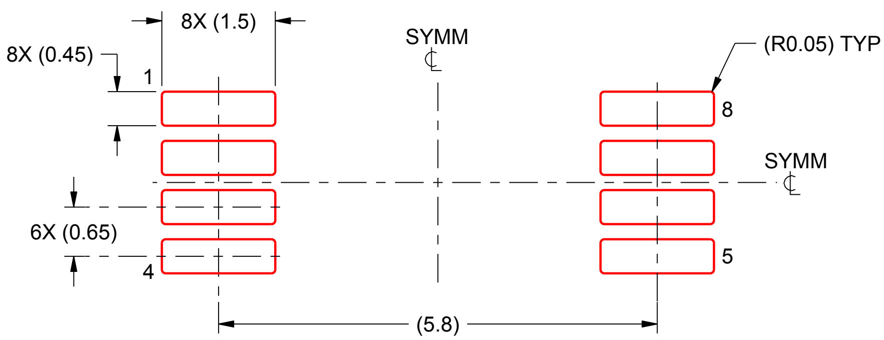


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

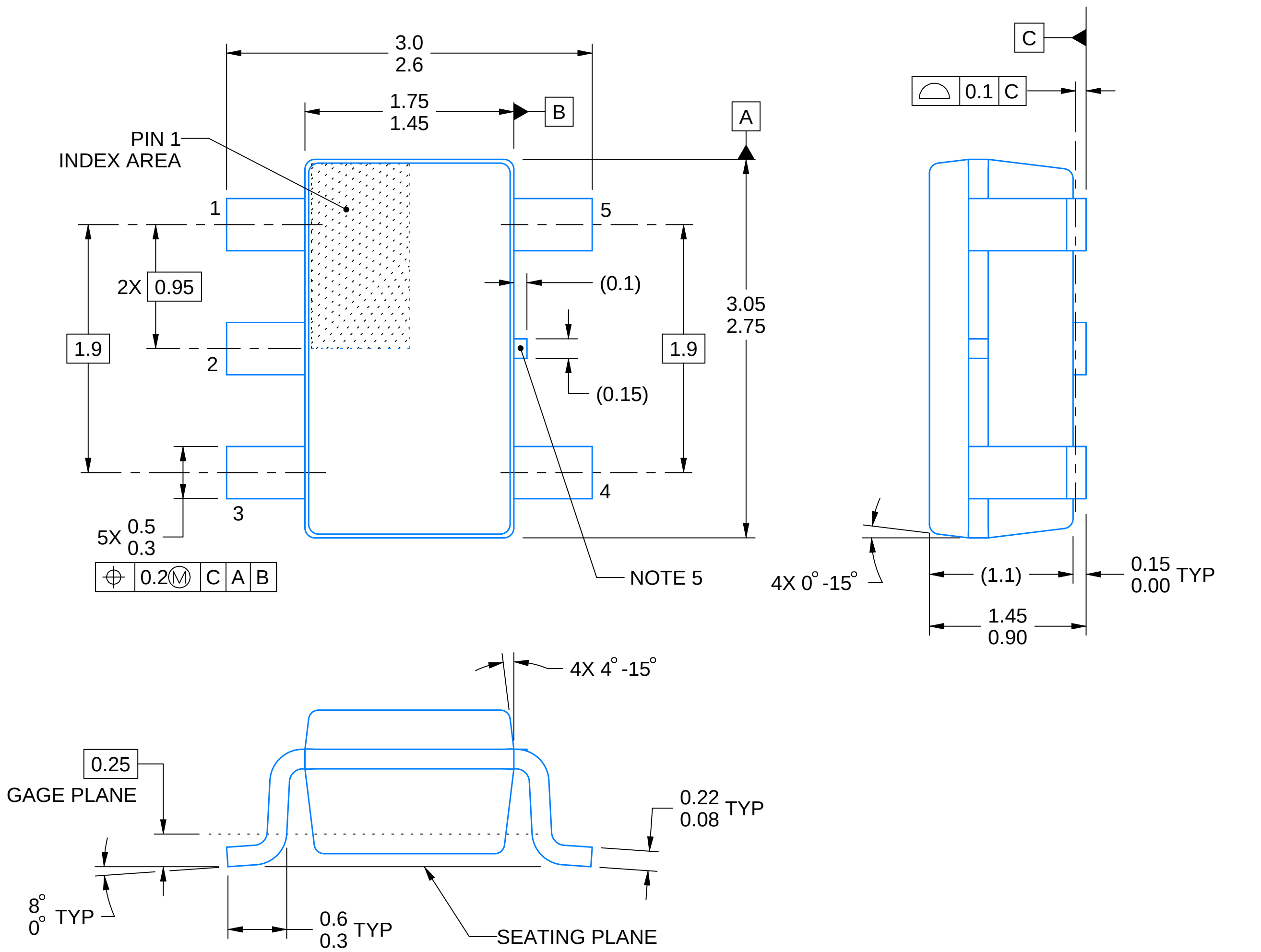


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

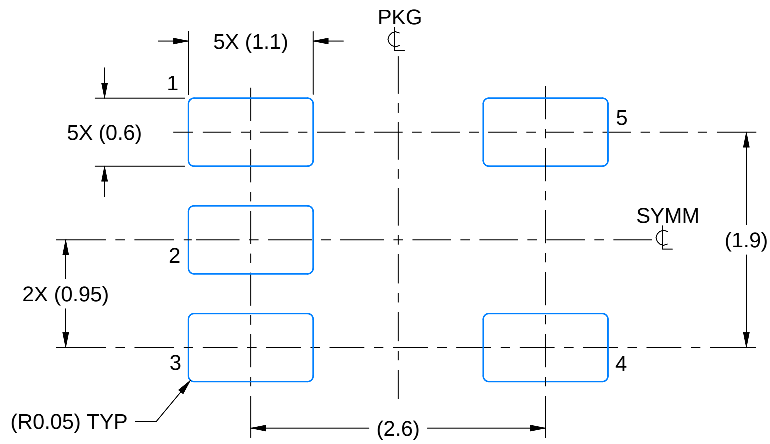
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



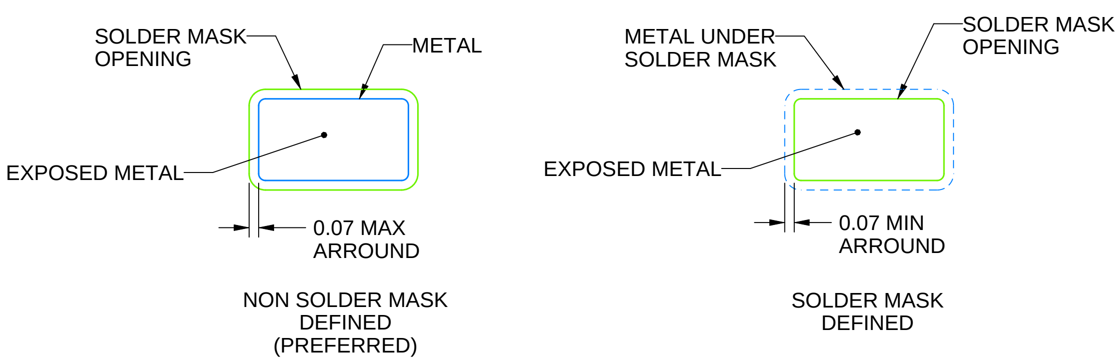
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

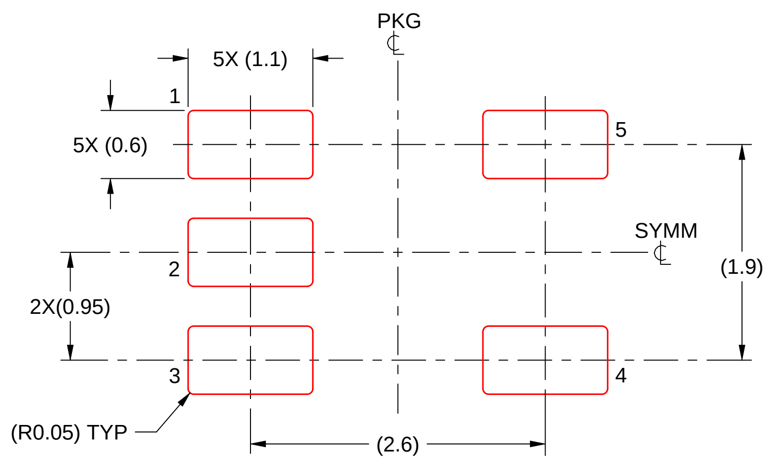


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

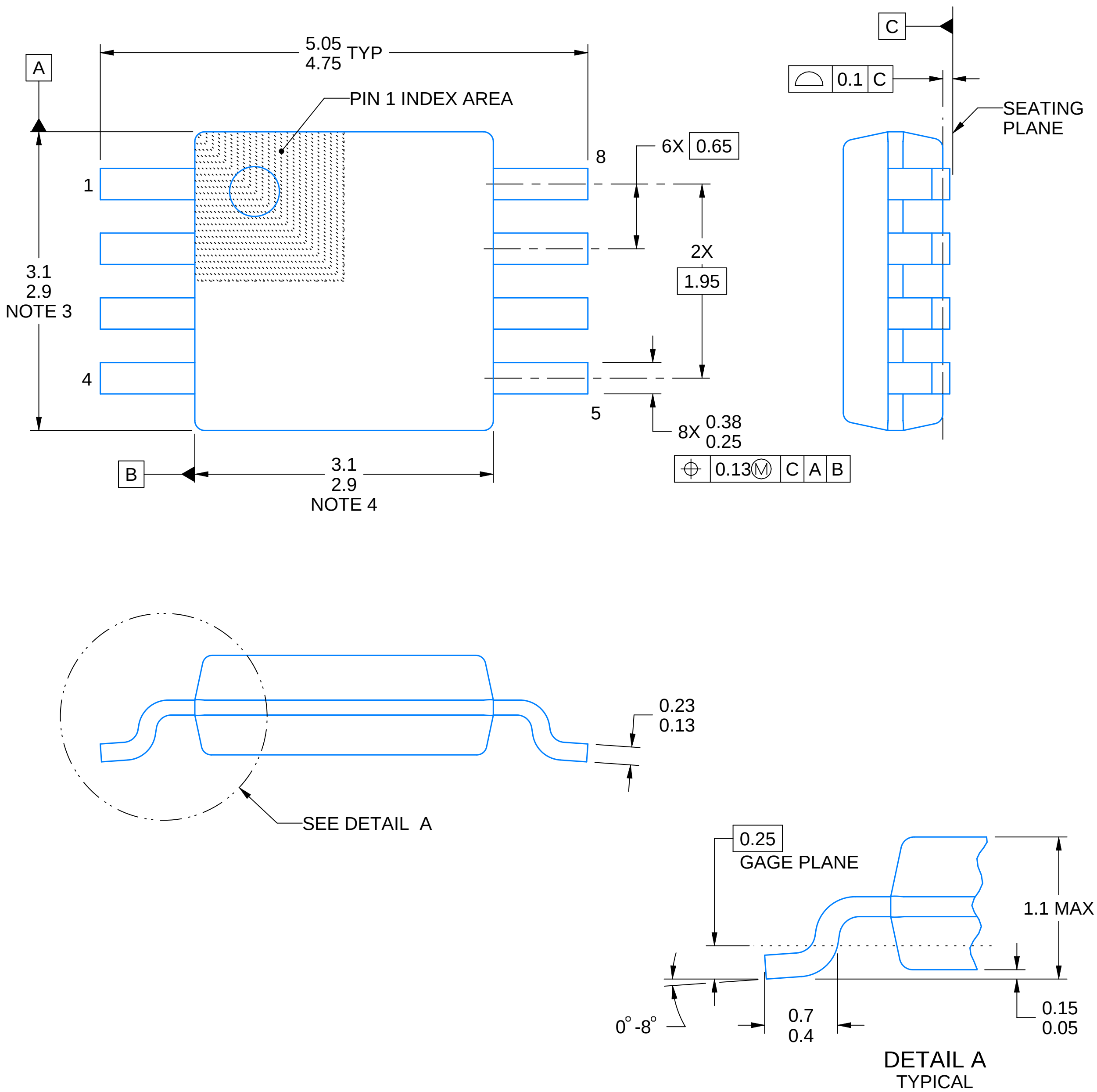


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

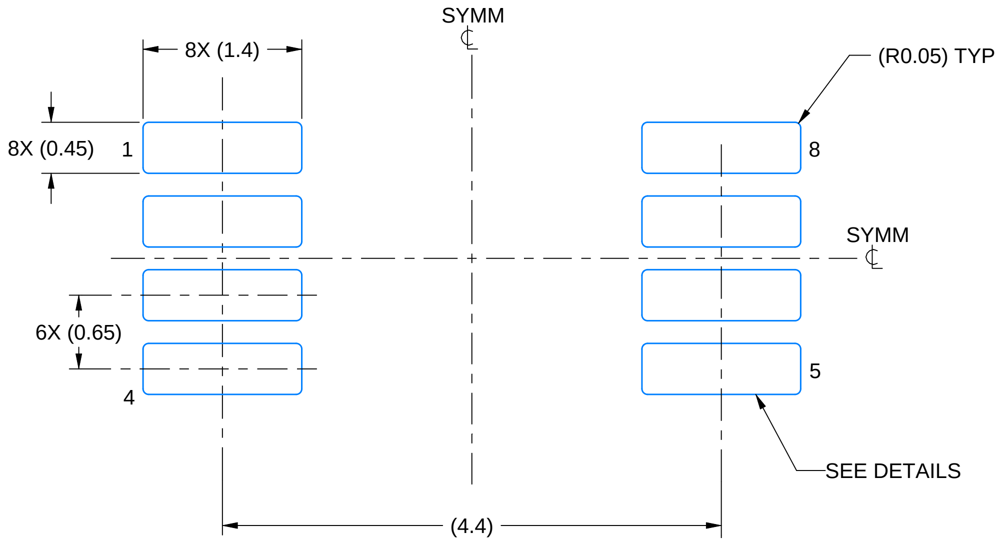


4214862/A 04/2023

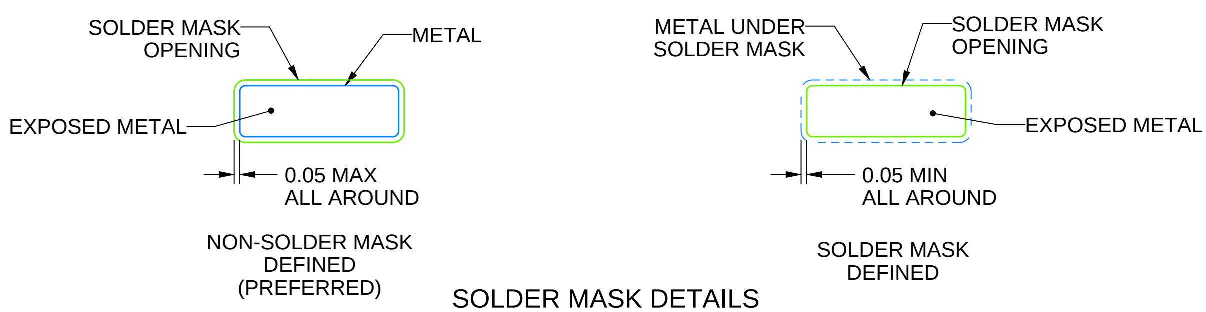
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

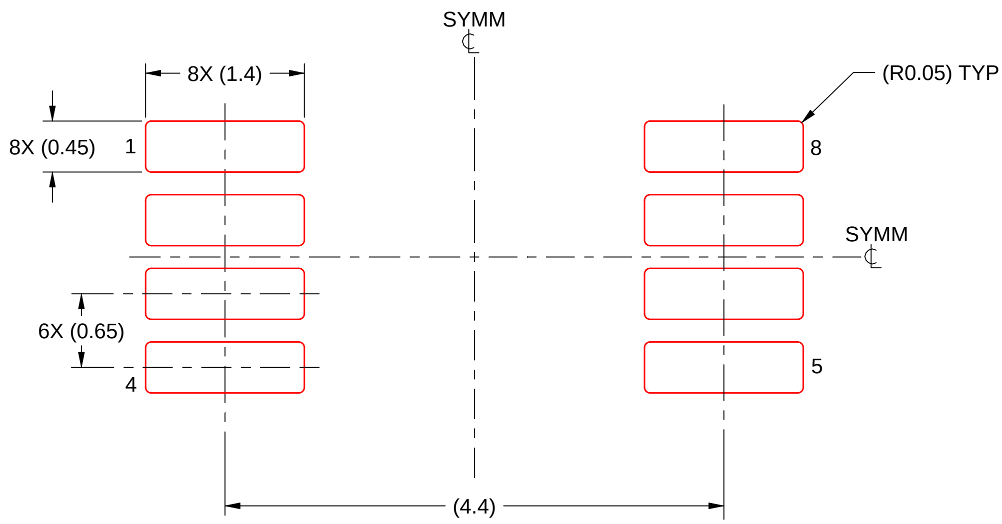


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

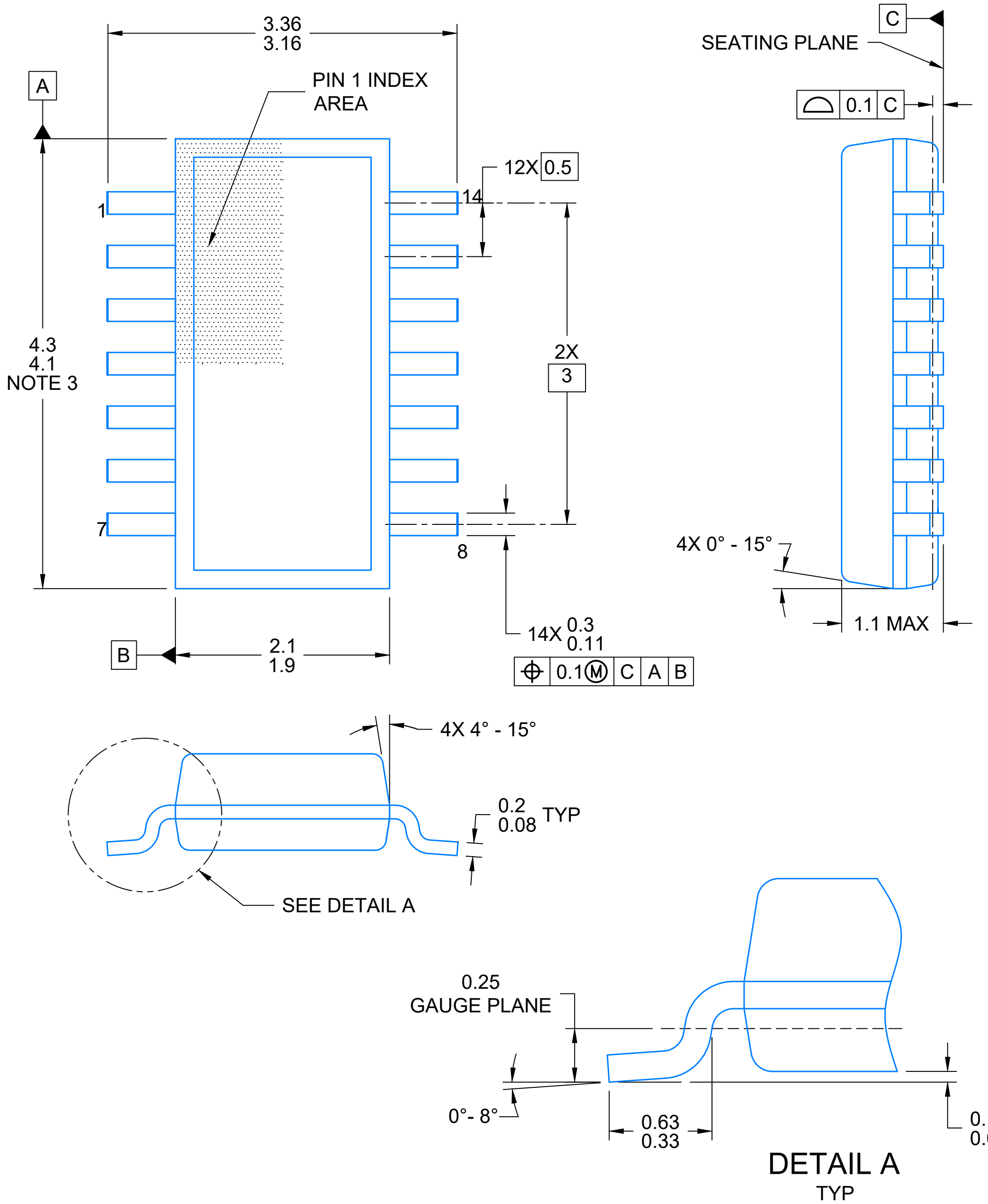


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

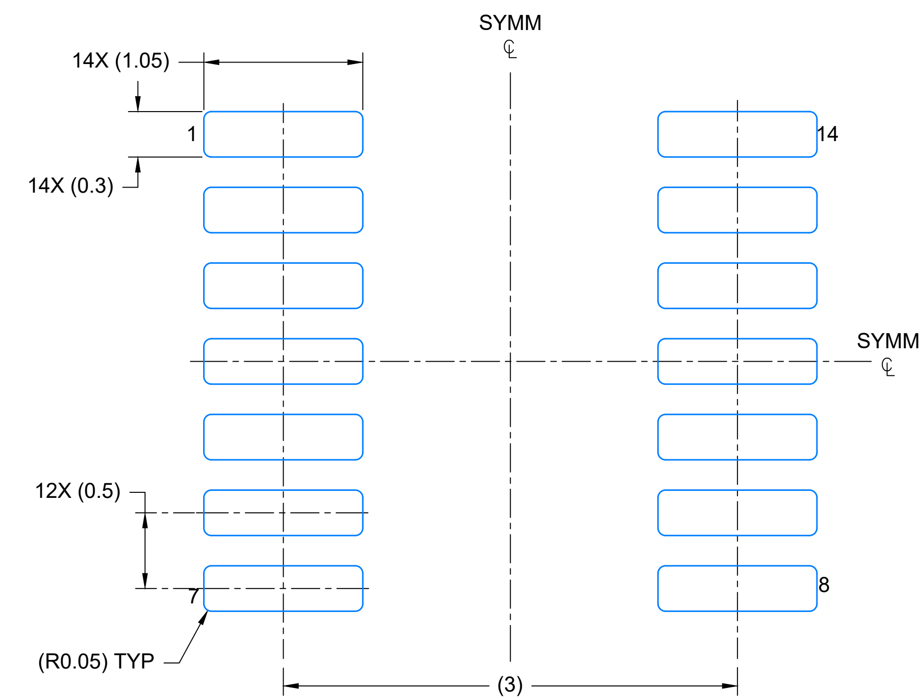
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



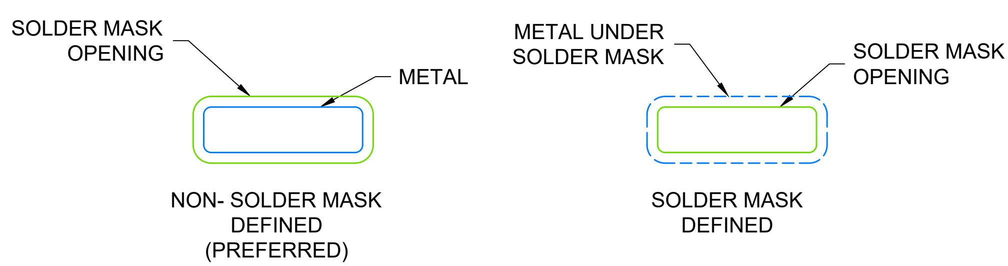
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

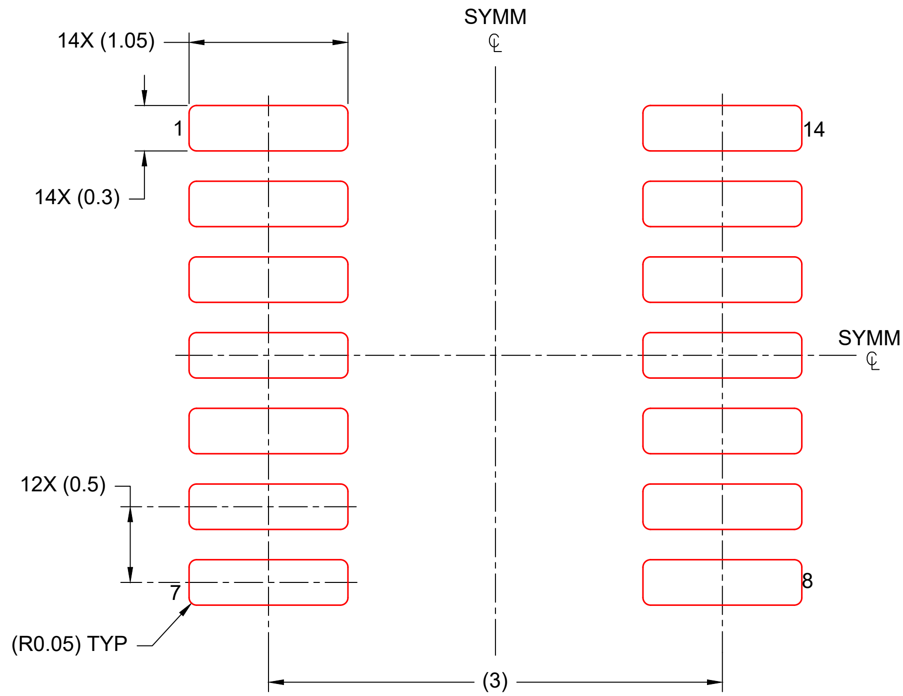


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER