# TS3A5017 Dual SP4T Analog Switch / Multiplexer / Demultiplexer

## 1 Features

- Isolation in the Powered-Down Mode, $V_+$ = 0
- Low ON-State Resistance
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 2.3-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 1500-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

## 3 Description

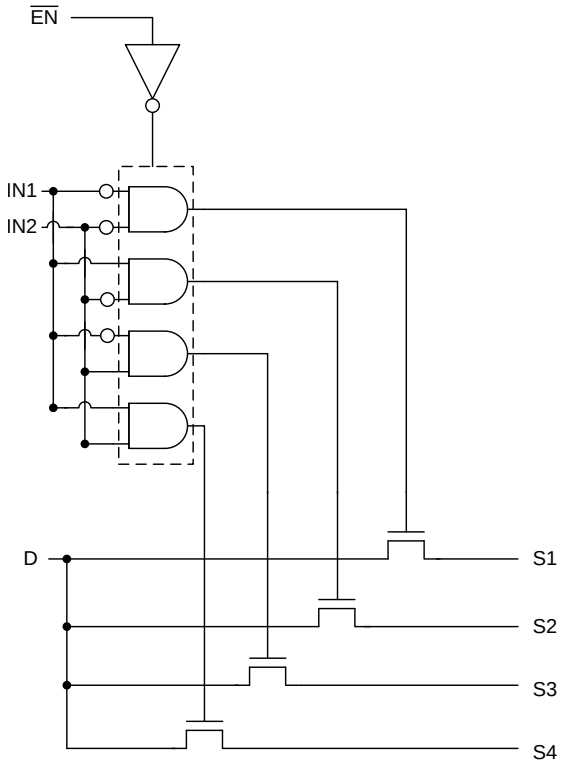
The TS3A5017 device is a dual single-pole quadruple-throw (4:1) analog switch that is designed to operate from 2.3 V to 3.6 V. This device can handle both digital and analog signals, and signals up to $V_+$ can be transmitted in either direction.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TS3A5017 | SOIC (16) | 9.90 mm × 3.90 mm |
| | SSOP (16) | 4.90 mm × 3.90 mm |
| | TSSOP (16) | 5.00 mm × 4.40 mm |
| | TVSOP (16) | 4.40 mm × 3.60 mm |
| | UQFN (16) | 2.50 mm × 1.80 mm |
| | VQFN (16) | 4.00 mm × 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Block Diagram**



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## 4 Revision History

**Changes from Revision F (October 2018) to Revision G** **Page**

- Changed *Feature* From: 2000-V Human-Body Model To: 1500-V Human-Body Model ... 1
- Changed the HBM value From: ±2000 V To: ±1500 V in the *ESD Ratings* ... 4

**Changes from Revision E (April 2015) to Revision F** **Page**

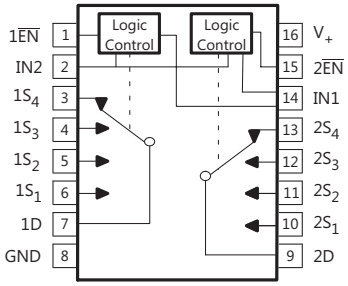
- Changed the $X_{TALK}$ MAX value From:–49 dB To – 69 dB in the *Electrical Characteristics for 3.3-V Supply* ... 6

**Changes from Revision D (December 2008) to Revision E** **Page**

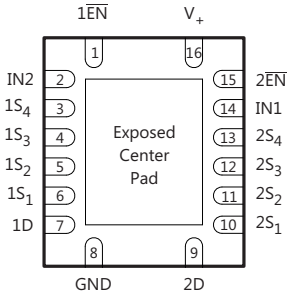
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

# 5 Pin Configuration and Functions

**D, DBQ, DGV, and PW Package**
**16-Pin SOIC, SSOP, TVSOP and TSSOP**
**(Top View)**

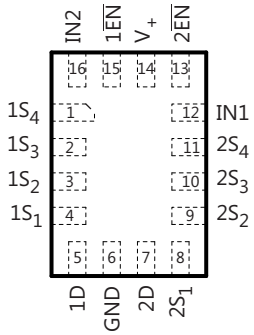



**RGY Package**
**16-Pin VQFN**
**(Top View)**




If exposed center pad is used, it must be connected as a secondary ground or left electrically open.

**RSV Package**
**16-Pin UQFN**
**(Top View)**




**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, SSOP, TVSOP, TSSOP, VQFN NO. | UQFN NO. | | |
| 1D | 7 | 5 | I/O | Common path for switch 1 |
| 1$\overline{EN}$ | 1 | 15 | I | Active-low enable for switch 1 |
| 1S1 | 6 | 4 | I/O | Switch 1 channel 1 |
| 1S2 | 5 | 3 | I/O | Switch 1 channel 2 |
| 1S3 | 4 | 2 | I/O | Switch 1 channel 3 |
| 1S4 | 3 | 1 | I/O | Switch 1 channel 4 |
| 2D | 9 | 7 | I/O | Common path for switch 2 |
| 2$\overline{EN}$ | 15 | 13 | I | Active-low enable for switch 2 |
| 2S1 | 10 | 8 | I/O | Switch 2 channel 1 |
| 2S2 | 11 | 9 | I/O | Switch 2 channel 2 |
| 2S3 | 12 | 10 | I/O | Switch 2 channel 3 |
| 2S4 | 13 | 11 | I/O | Switch 2 channel 4 |
| GND | 8 | 6 | – | Ground |
| IN1 | 14 | 12 | I | Switch 1 input select |
| IN2 | 2 | 16 | I | Switch 2 input select |
| V+ | 16 | 14 | – | Supply voltage |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_+$ | Supply voltage(3) | | –0.5 | 4.6 | V |
| $V_S$, $V_D$ | Analog voltage(3)(4) | | –0.5 | 4.6 | V |
| $I_{SK}$, $I_{DK}$ | Analog port clamp current | $V_S$, $V_D$ < 0 | –50 | | mA |
| $I_S$, $I_D$ | ON-state switch current | $V_S$, $V_D$ = 0 to 7 V | –128 | 128 | mA |
| $V_I$ | Digital input voltage | | –0.5 | 4.6 | V |
| $I_{IK}$ | Digital input clamp current(3)(4) | $V_I$ < 0 | –50 | | mA |
| $I_+$ | Continuous current through $V_+$ | | | 100 | mA |
| $I_{GND}$ | Continuous current through GND | | –100 | | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{I/O}$ | Switch input/output voltage range | 0 | 3.6 | V |
| V+ | Supply voltage range | 2.3 | 3.6 | V |
| $V_I$ | Control input voltage range | 0 | 3.6 | V |
| $T_A$ | Operating Temperature Range | –40 | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TS3A5018 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DBQ (SSOP) | DGV (TVSOP) | PW (TSSOP) | RGY (VQFN) | RSV (UQFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73 | 82 | 120 | 108 | 91.6 | 184 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics for 3.3-V Supply

$V_+$ = 2.7 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| $V_D$, $V_S$ | Analog signal range | | | | | 0 | | $V_+$ | V |
| $r_{on}$ | ON-state resistance | 0 ≤ $V_S$ ≤ $V_+$, $I_D$ = –32 mA, | Switch ON, see Figure 12 | 25°C | 3 V | | 11 | 12 | Ω |
| | | | | Full | | | | 14 | |
| $\Delta r_{on}$ | ON-state resistance match between channels | $V_S$ = 2.1 V, $I_D$ = –32 mA, | Switch ON, see Figure 12 | 25°C | 3 V | | 1 | 2 | Ω |
| | | | | Full | | | | 3 | |
| $r_{on(flat)}$ | ON-state resistance flatness | 0 ≤ $V_S$ ≤ $V_+$, $I_D$ = –32 mA, | Switch ON, see Figure 12 | 25°C | 3 V | | 7 | 9 | Ω |
| | | | | Full | | | | 10 | |
| $I_{S(OFF)}$ | S OFF leakage current | $V_S$ = 1 V, $V_D$ = 3 V, or $V_S$ = 3 V, $V_D$ = 1 V, | Switch OFF, see Figure 13 | 25°C | 3.6 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| $I_{SPWR(OFF)}$ | | $V_S$ = 0 to 3.6 V, $V_D$ = 3.6 V to 0, | | 25°C | 0 V | –1 | 0.5 | 1 | |
| | | | | Full | | –5 | | 5 | |
| $I_{D(OFF)}$ | D OFF leakage current | $V_S$ = 1 V, $V_D$ = 3 V, or $V_S$ = 3 V, $V_D$ = 1 V, | Switch OFF, see Figure 13 | 25°C | 3.6 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| $I_{DPWR(OFF)}$ | | $V_D$ = 0 to 3.6 V, $V_S$ = 3.6 V to 0, | | 25°C | 0 V | –1 | 0.5 | 1 | |
| | | | | Full | | –5 | | 5 | |
| $I_{S(ON)}$ | S ON leakage current | $V_S$ = 1 V, $V_D$ = Open, or $V_S$ = 3 V, $V_D$ = Open, | Switch ON, see Figure 14 | 25°C | 3.6 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| $I_{D(ON)}$ | D ON leakage current | $V_D$ = 1 V, $V_S$ = Open, or $V_D$ = 3 V, $V_S$ = Open, | Switch ON, see Figure 14 | 25°C | 3.6 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| **Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)** | | | | | | | | | |
| $V_{IH}$ | Input logic high | | | Full | | 2 | | $V_+$ | V |
| $V_{IL}$ | Input logic low | | | Full | | 0 | | 0.8 | V |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_I$ = $V_+$ or 0 | | 25°C | 3.6 V | –1 | 0.05 | 1 | µA |
| | | | | Full | | –1 | | 1 | |
| $Q_C$ | Charge injection | $V_{GEN}$ = 0, $R_{GEN}$ = 0, $C_L$ = 0.1 nF, | See Figure 21 | 25°C | 3.3 V | | 5 | | pC |
| $C_{S(OFF)}$ | S OFF capacitance | $V_S$ = $V_+$ or GND, Switch OFF, | See Figure 15 | 25°C | 3.3 V | | 4.5 | | pF |
| $C_{D(OFF)}$ | D OFF capacitance | $V_D$ = $V_+$ or GND, Switch OFF, | See Figure 15 | 25°C | 3.3 V | | 19 | | pF |
| $C_{S(ON)}$ | S ON capacitance | $V_S$ = $V_+$ or GND, Switch ON, | See Figure 15 | 25°C | 3.3 V | | 25 | | pF |
| $C_{D(ON)}$ | D ON capacitance | $V_D$ = $V_+$ or GND, Switch ON, | See Figure 15 | 25°C | 3.3 V | | 25 | | pF |
| $C_I$ | Digital input capacitance | $V_I$ = $V_+$ or GND, | See Figure 15 | 25°C | 3.3 V | | 2 | | pF |
| BW | Bandwidth | $R_L$ = 50 Ω, Switch ON, | See Figure 17 | 25°C | 3.3 V | | 165 | | MHz |
| $O_{ISO}$ | OFF isolation | $R_L$ = 50 Ω, f = 1 MHz, | See Figure 18 | 25°C | 3.3 V | | –69 | | dB |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at $V_+$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics for 3.3-V Supply (continued)

$V_+$ = 2.7 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, f = 1 MHz, | See Figure 19 | 25°C | 3.3 V | | –69 | | dB |
| $X_{TALK(ADJ)}$ | Crosstalk adjacent | $R_L$ = 50 Ω, f = 1 MHz, | See Figure 20 | 25°C | 3.3 V | | –74 | | dB |
| THD | Total harmonic distortion | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, see Figure 22 | 25°C | 3.3 V | | 0.21% | | |
| **Supply** | | | | | | | | | |
| $I_+$ | Positive supply current | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 3.6 V | | 2.5 | 7 | µA |
| | | | | Full | | | | 10 | |

## 6.6 Electrical Characteristics for 2.5-V Supply

$V_+$ = 2.3 V to 2.7 V, $T_A$ = –40°C to 85°C (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| $V_D$, $V_S$ | Analog signal range | | | | | 0 | | $V_+$ | V |
| $r_{on}$ | ON-state resistance | 0 ≤ $V_S$ ≤ $V_+$, $I_D$ = –24 mA, | Switch ON, see Figure 12 | 25°C | 2.3 V | | 20.5 | 22 | Ω |
| | | | | Full | | | | 24 | |
| $\Delta r_{on}$ | ON-state resistance match between channels | $V_S$ = 1.6 V, $I_D$ = –24 mA, | Switch ON, see Figure 12 | 25°C | 2.3 V | | 1 | 2 | Ω |
| | | | | Full | | | | 3 | |
| $r_{on(flat)}$ | ON-state resistance flatness | 0 ≤ $V_S$ ≤ $V_+$, $I_D$ = –24 mA, | Switch ON, see Figure 12 | 25°C | 2.3 V | | 16 | 18 | Ω |
| | | | | Full | | | | 20 | |
| $I_{S(OFF)}$ | S OFF leakage current | $V_S$ = 0.5 V, $V_D$ = 2.2 V, or $V_S$ = 2.2 V, $V_D$ = 0.5 V, | Switch OFF, see Figure 13 | 25°C | 2.7 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| $I_{SPWR(OFF)}$ | | $V_S$ = 0 to 2.7 V, $V_D$ = 2.7 V to 0, | | 25°C | 0 V | –1 | 0.5 | 1 | |
| | | | | Full | | –5 | | 5 | |
| $I_{D(OFF)}$ | D OFF leakage current | $V_S$ = 0.5 V, $V_D$ = 2.2 V, or $V_S$ = 2.2 V, $V_D$ = 0.5V, | Switch OFF, see Figure 13 | 25°C | 2.7 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| $I_{DPWR(OFF)}$ | | $V_D$ = 0 to 2.7 V, $V_S$ = 2.7 V to 0, | | 25°C | 0 V | –1 | 0.5 | 1 | |
| | | | | Full | | –5 | | 5 | |
| $I_{S(ON)}$ | S ON leakage current | $V_S$ = 0.5 V, $V_D$ = Open, or $V_S$ = 2.2 V, $V_D$ = Open, | Switch ON, see Figure 14 | 25°C | 2.7 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| $I_{D(ON)}$ | D ON leakage current | $V_D$ = 0.5 V, $V_S$ = Open, or $V_D$ = 2.2 V, $V_S$ = Open, | Switch ON, see Figure 14 | 25°C | 2.7 V | –0.1 | 0.05 | 0.1 | µA |
| | | | | Full | | –0.2 | | 0.2 | |
| **Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)** | | | | | | | | | |
| $V_{IH}$ | Input logic high | | | Full | | 1.7 | | $V_+$ | V |
| $V_{IL}$ | Input logic low | | | Full | | 0 | | 0.7 | V |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_I$ = $V_+$ or 0 | | 25°C | 2.7 V | –1 | 0.05 | 1 | µA |
| | | | | Full | | –1 | | 1 | |
| $Q_C$ | Charge injection | $V_{GEN}$ = 0, $R_{GEN}$ = 0, $C_L$ = 0.1 nF, | See Figure 21 | 25°C | 2.5 V | | | | pC |
| $C_{S(OFF)}$ | S OFF capacitance | $V_S$ = $V_+$ or GND, Switch OFF, | See Figure 15 | 25°C | 2.5 V | | 4.5 | | pF |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at $V_+$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics for 2.5-V Supply (continued)

$V_+$ = 2.3 V to 2.7 V, $T_A$ = –40°C to 85°C (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $C_{D(OFF)}$ | D OFF capacitance | $V_D$ = $V_+$ or GND, Switch OFF, | See Figure 15 | 25°C | 2.5 V | | 18.5 | | pF |
| $C_{S(ON)}$ | S ON capacitance | $V_S$ = $V_+$ or GND, Switch ON, | See Figure 15 | 25°C | 2.5 V | | 24 | | pF |
| $C_{D(ON)}$ | D ON capacitance | $V_D$ = $V_+$ or GND, Switch ON, | See Figure 15 | 25°C | 2.5 V | | 24 | | pF |
| $C_I$ | Digital input capacitance | $V_I$ = $V_+$ or GND, | See Figure 15 | 25°C | 2.5 V | | 2 | | pF |
| BW | Bandwidth | $R_L$ = 50 Ω, Switch ON, | See Figure 17 | 25°C | 2.5 V | | 165 | | MHz |
| $O_{ISO}$ | OFF isolation | $R_L$ = 50 Ω, f = 1 MHz, | See Figure 18 | 25°C | 2.5 V | | –69 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, f = 1 MHz, | See Figure 19 | 25°C | 2.5 V | | –69 | | dB |
| $X_{TALK(ADJ)}$ | Crosstalk adjacent | $R_L$ = 50 Ω, f = 1 MHz, | See Figure 20 | 25°C | 2.5 V | | –74 | | dB |
| THD | Total harmonic distortion | $R_L$ = 600 Ω, $C_L$ = 50 pF, | f = 20 Hz to 20 kHz, see Figure 22 | 25°C | 2.5 V | | 0.29% | | |
| **Supply** | | | | | | | | | |
| $I_+$ | Positive supply current | $V_I$ = $V_+$ or GND, | Switch ON or OFF | 25°C | 2.7 V | | 2.5 | 7 | μA |
| | | | | Full | | | | 10 | |

## 6.7 Switching Characteristics for 3.3-V supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{ON}$ | Turnon time | $V_D$ = 2 V, $R_L$ = 300 Ω, | $C_L$ = 35 pF, see Figure 16 | 25°C | 3.3 V | 1 | 5 | 9.5 | ns |
| | | | | Full | 3 V to 3.6 V | 1 | | 10.5 | |
| $t_{OFF}$ | Turnoff time | $V_D$ =2 V, $R_L$ = 300 Ω, | $C_L$ = 35 pF, see Figure 16 | 25°C | 3.3 V | 0.5 | 1.5 | 3.5 | ns |
| | | | | Full | 3 V to 3.6 V | 0.5 | | 4.5 | |

## 6.8 Switching Characteristics for 2.5-V supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | $V_+$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{ON}$ | Turnon time | $V_{COM}$ = 2 V, $R_L$ = 300 Ω, | $C_L$ = 35 pF, see Figure 16 | 25°C | 2.5 V | 1.5 | 5 | 8 | ns |
| | | | | Full | 2.3 V to 2.7 V | 1 | | 10 | |
| $t_{OFF}$ | Turnoff time | $V_{COM}$ =2 V, $R_L$ = 300 Ω, | $C_L$ = 35 pF, see Figure 16 | 25°C | 2.5 V | 0.3 | 2 | 4.5 | ns |
| | | | | Full | 2.3 V to 2.7 V | 0.3 | | 6 | |

## 6.9 Typical Characteristics

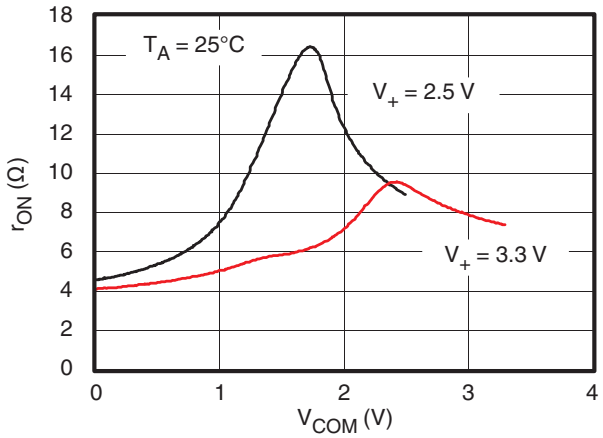



**Figure 1. $r_{on}$ vs $V_{COM}$**

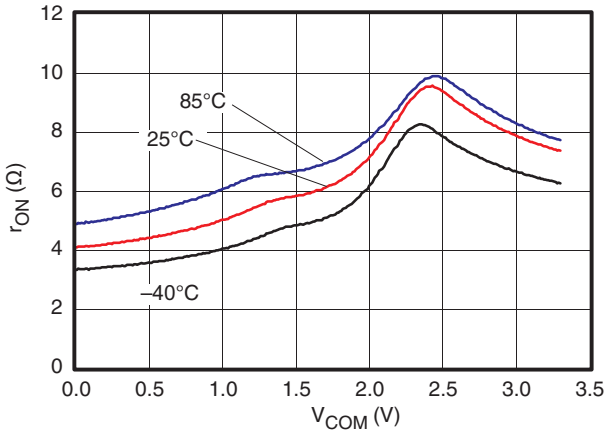



**Figure 2. $r_{on}$ vs $V_{COM}$ ($V_+$ = 3.3 V)**

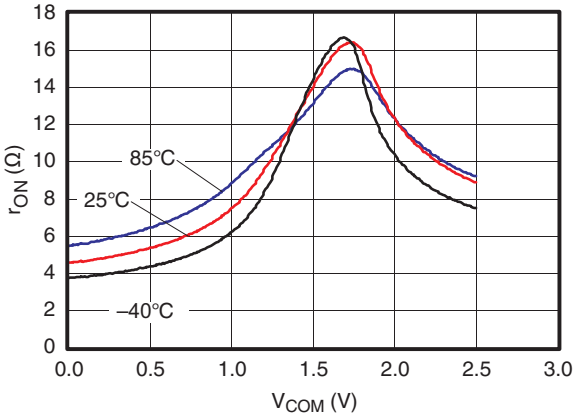



**Figure 3. $r_{on}$ vs $V_{COM}$ ($V_+$ = 2.5 V)**

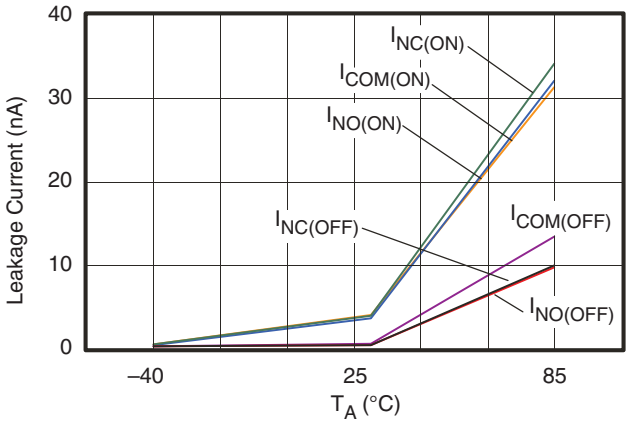



**Figure 4. Leakage Current vs Temperature ($V_+$ = 3.6 V)**

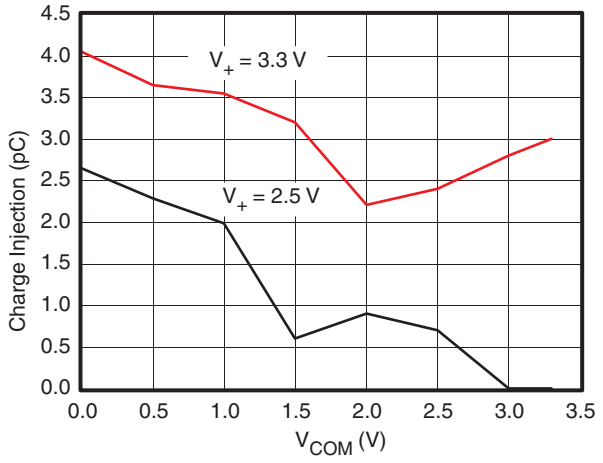



**Figure 5. Charge Injection ($Q_C$) vs $V_{COM}$**

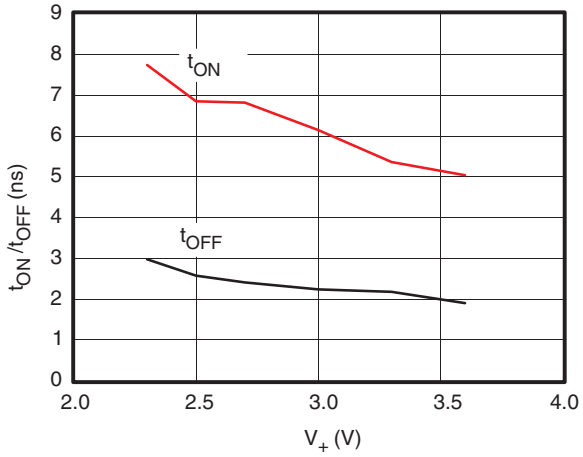



**Figure 6. $t_{ON}$ and $t_{OFF}$ vs Supply Voltage**

## Typical Characteristics (continued)

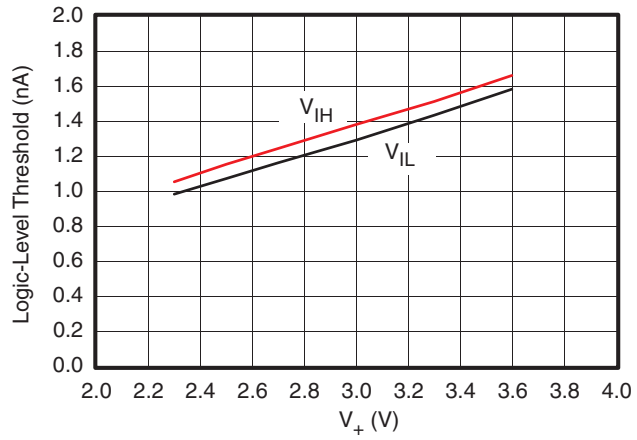



**Figure 7. Logic-Level Threshold vs $V_+$**

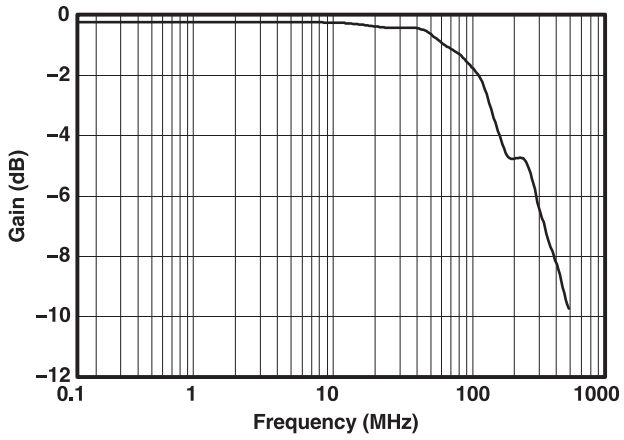



**Figure 8. Bandwidth (Gain vs Frequency) ($V_+$ = 3.3 V)**

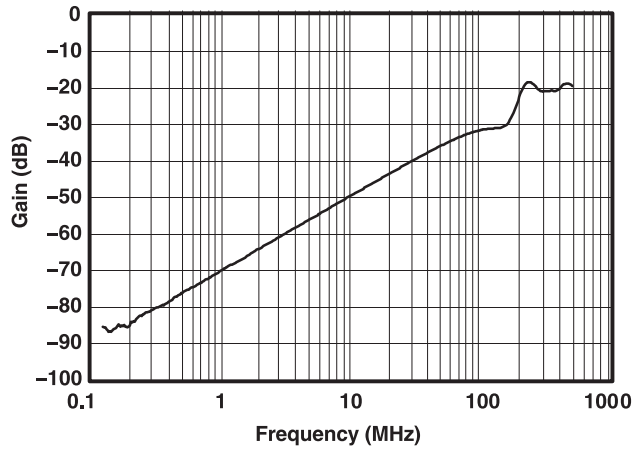



**Figure 9. OFF Isolation and Crosstalk vs Frequency ($V_+$ = 3.3 V)**

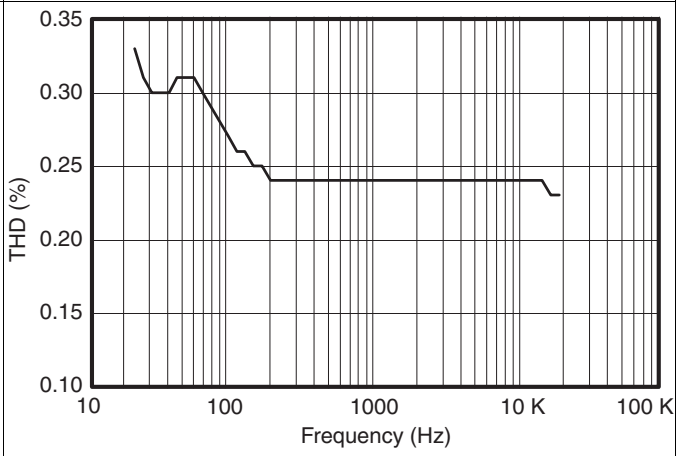



**Figure 10. Total Harmonic Distortion vs Frequency**

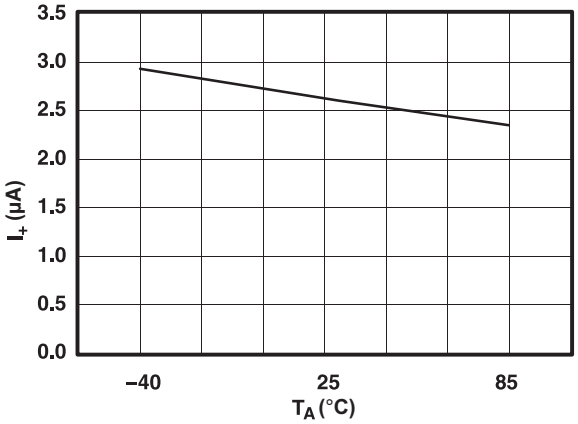



**Figure 11. Power-Supply Current vs Temperature ($V_+$ = 3.6 V)**

# 7 Parameter Measurement Information

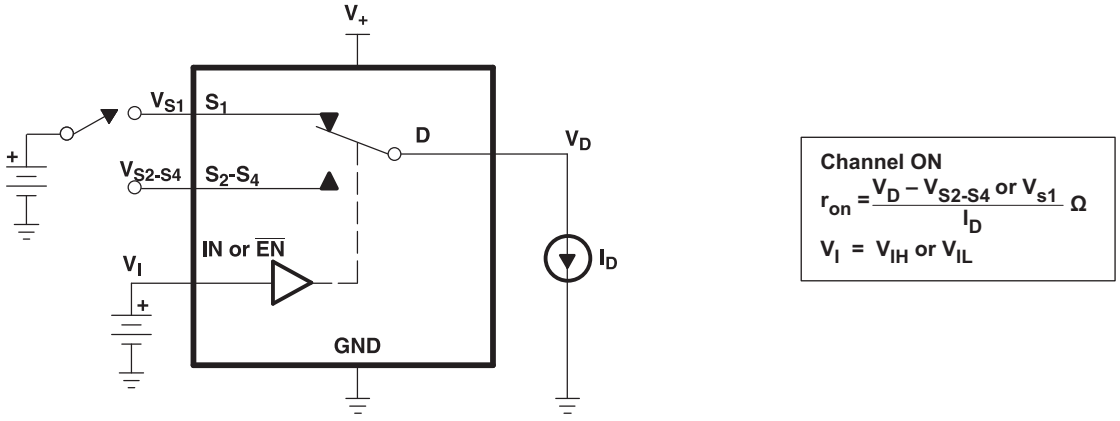



**Figure 12. ON-State Resistance ($r_{on}$)**

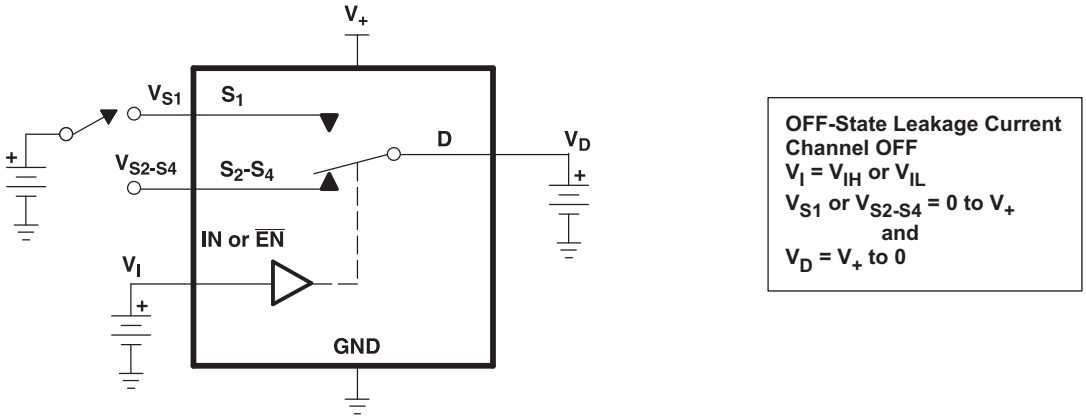



**Figure 13. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$)**

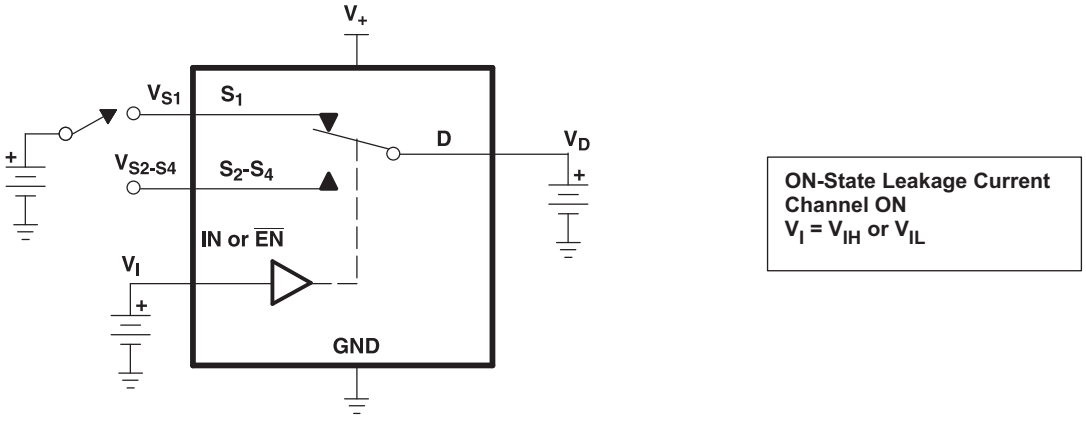



**Figure 14. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)**

## Parameter Measurement Information (continued)

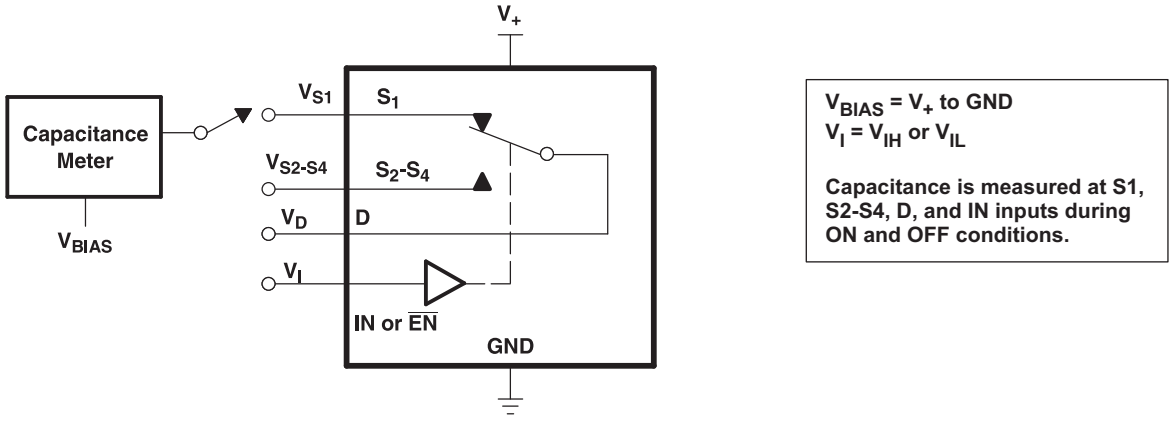
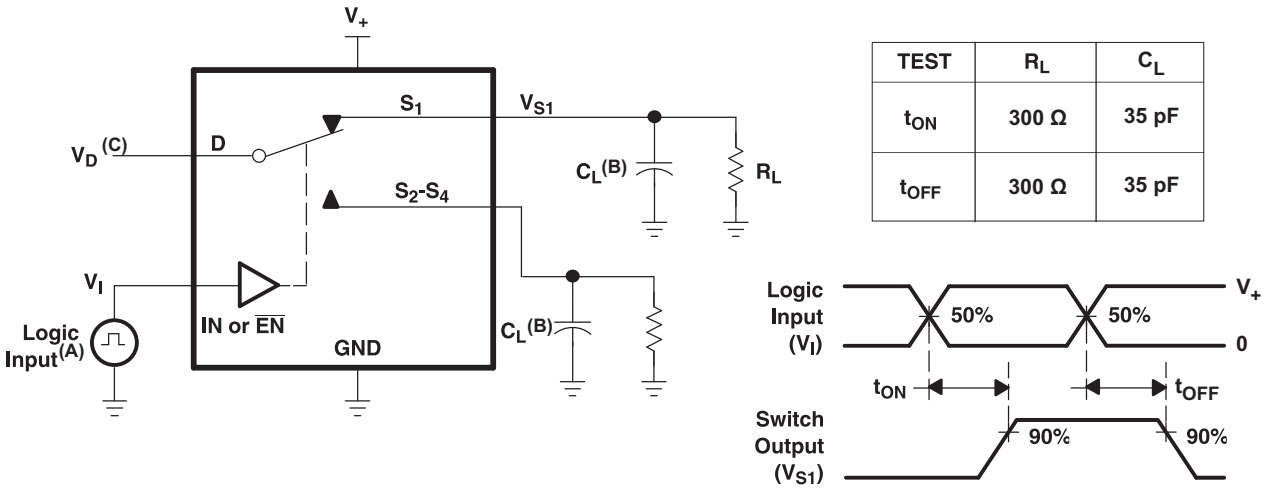



**Figure 15. Capacitance ($C_I$, $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)**




| TEST | $R_L$ | $C_L$ |
|---|---|---|
| $t_{ON}$ | 300 Ω | 35 pF |
| $t_{OFF}$ | 300 Ω | 35 pF |

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

C. See Electrical Characteristics for $V_D$.

**Figure 16. Turnon ($t_{ON}$) and Turnoff Time ($t_{OFF}$)**

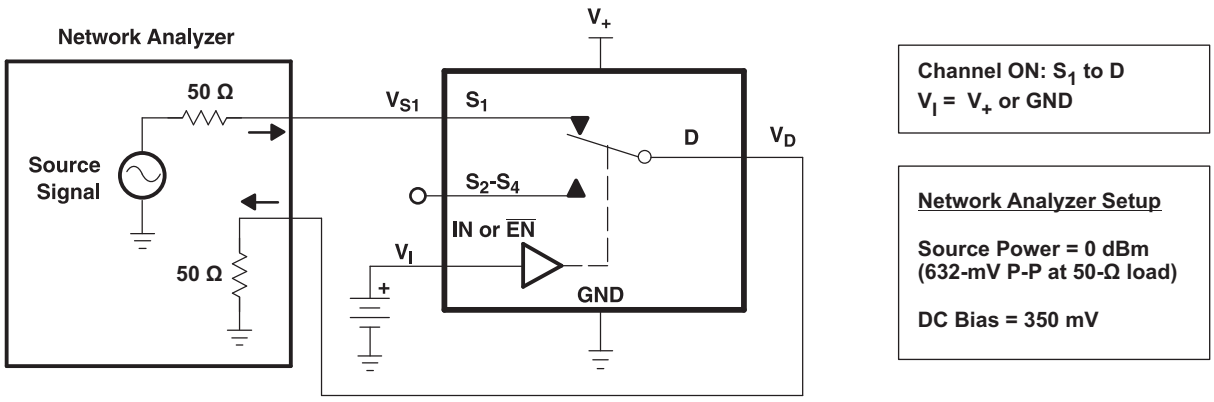



**Figure 17. Bandwidth (BW)**

## Parameter Measurement Information (continued)

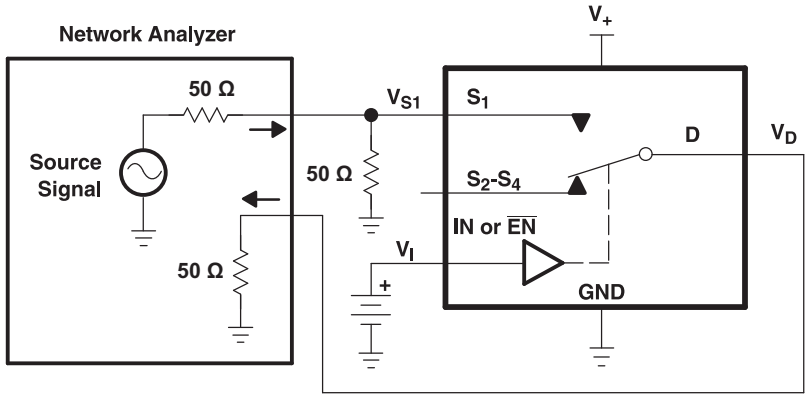



**Figure 18. OFF Isolation ($O_{ISO}$)**

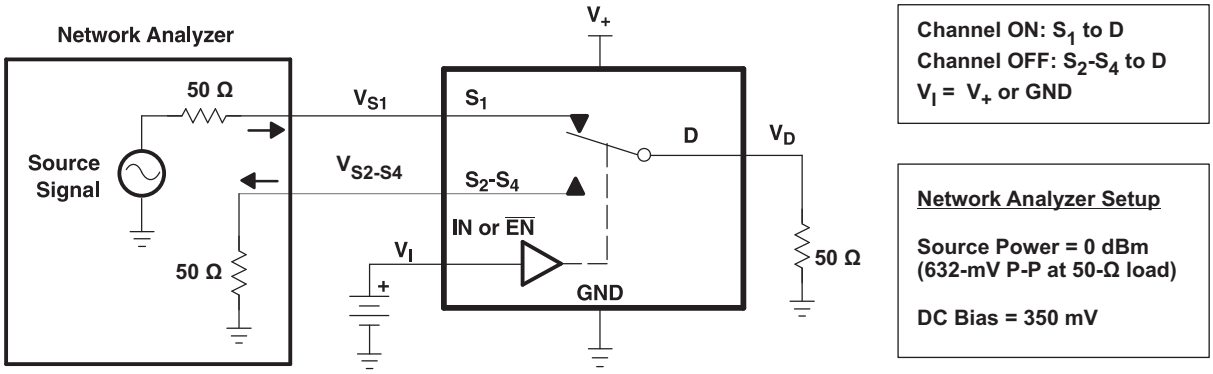



**Figure 19. Crosstalk ($X_{TALK}$)**

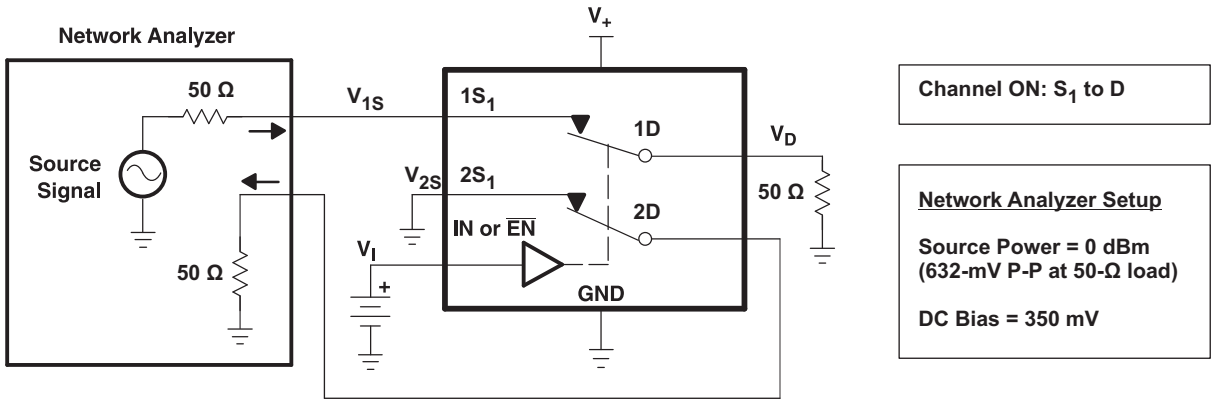
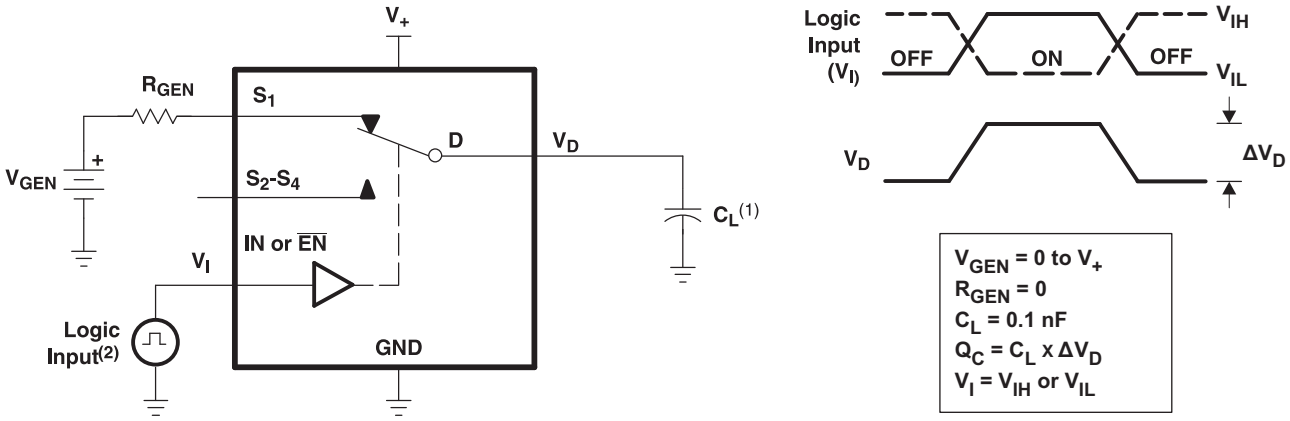



**Figure 20. Adjacent Crosstalk ($X_{TALK}$)**

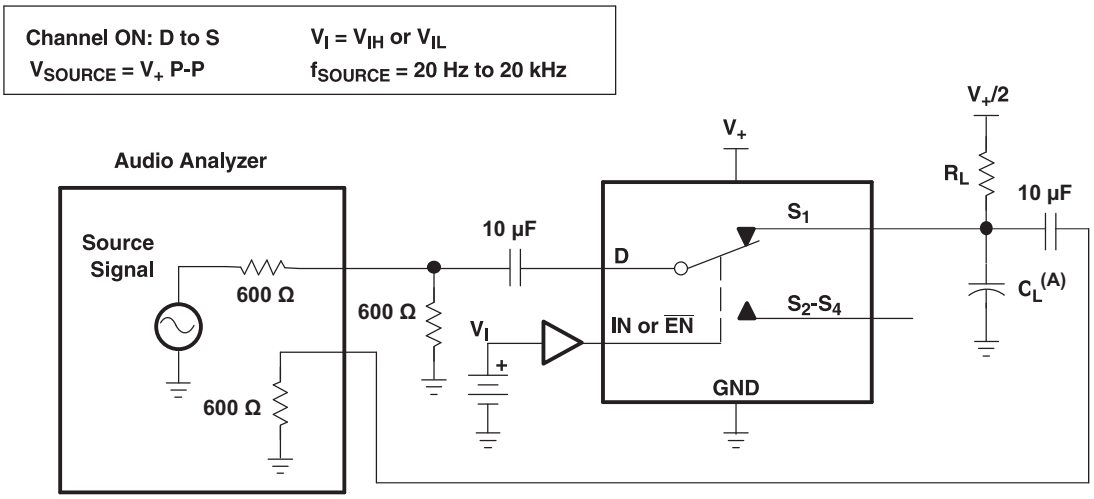
## Parameter Measurement Information (continued)




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

B. $C_L$ includes probe and jig capacitance.

**Figure 21. Charge Injection ($Q_C$)**




A. $C_L$ includes probe and jig capacitance.

**Figure 22. Total Harmonic Distortion (THD)**

# 8 Detailed Description

## 8.1 Overview

The TS3A5017 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of $\overline{EN}$, IN2, and IN1. See Table 1 for the switch configuration truth table.

## 8.2 Functional Block Diagram

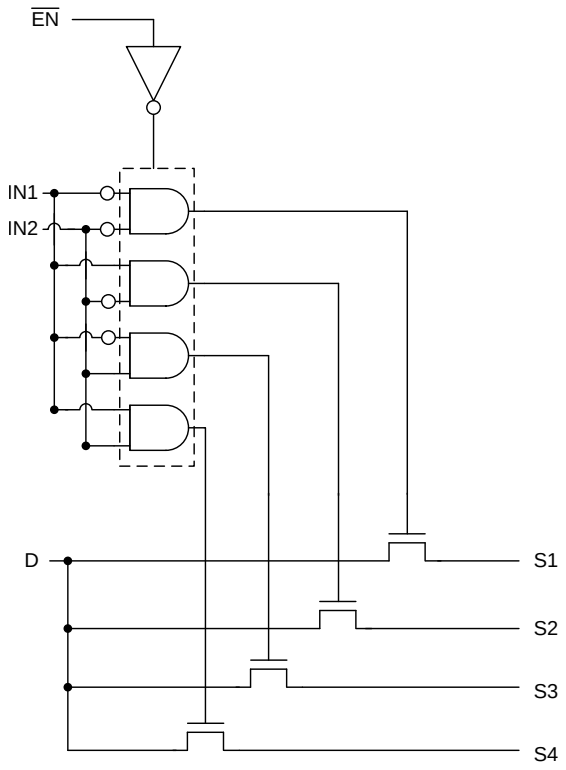



**Figure 23. Functional Block Diagram (Each Switch)**

## 8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017 better performance at higher speeds.

## 8.4 Device Functional Modes

**Table 1. Function Table**

| $\overline{EN}$ | IN2 | IN1 | D TO S, S TO D |
|---|---|---|---|
| L | L | L | D = $S_1$ |
| L | L | H | D = $S_2$ |
| L | H | L | D = $S_3$ |
| L | H | H | D = $S_4$ |
| H | X | X | OFF |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TS3A5018 can be used in a variety of customer systems. The TS3A5018 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

## 9.2 Typical Application

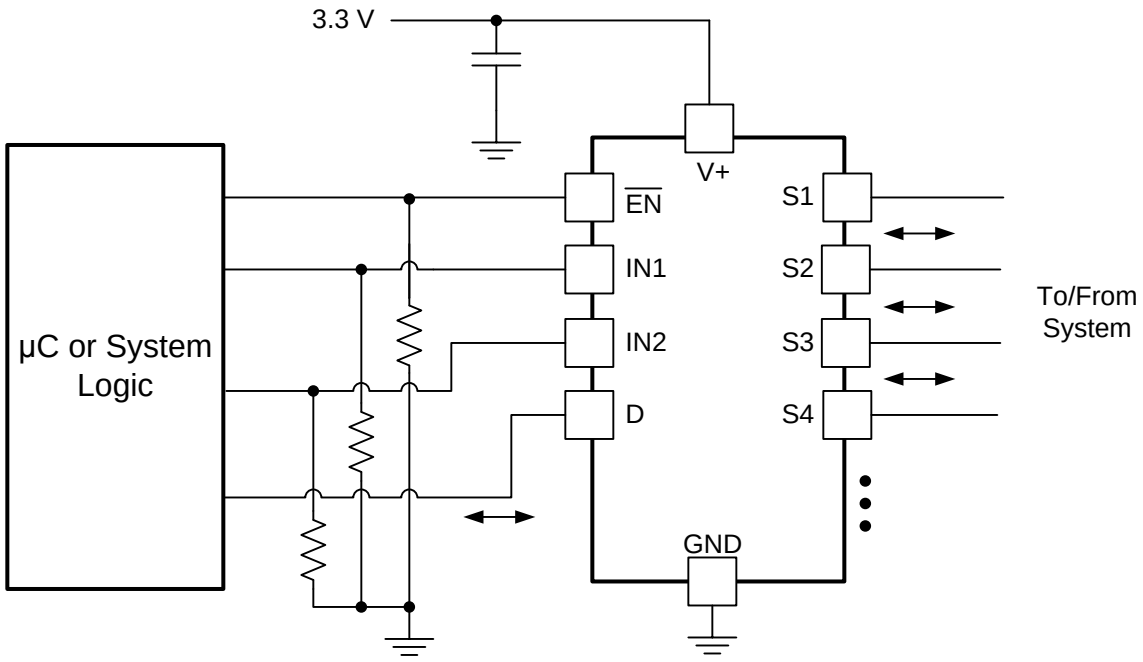



**Figure 24. System Schematic for TS3A5017**

### 9.2.1 Design Requirements

In this particular application, V+ was 3.3 V, although V+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

### 9.2.2 Detailed Design Procedure

In this application, $\overline{EN}$, IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

## Typical Application (continued)

### 9.2.3 Application Curve

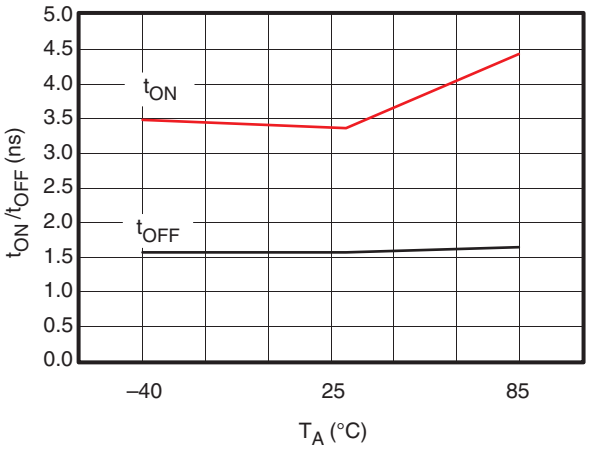



**Figure 25. $t_{ON}$ and $t_{OFF}$ vs Temperature ($V_+$ = 3.3 V)**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled $V_{CC}$, then a 0.01-µF or 0.022-µF capacitor is recommended for each $V_{CC}$ because the $V_{CC}$ pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example $V_{CC}$ and $V_{DD}$, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and $\overline{EN}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased $I_{CC}$ or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs,* SCBA004 for more details.

## 11.2 Layout Example

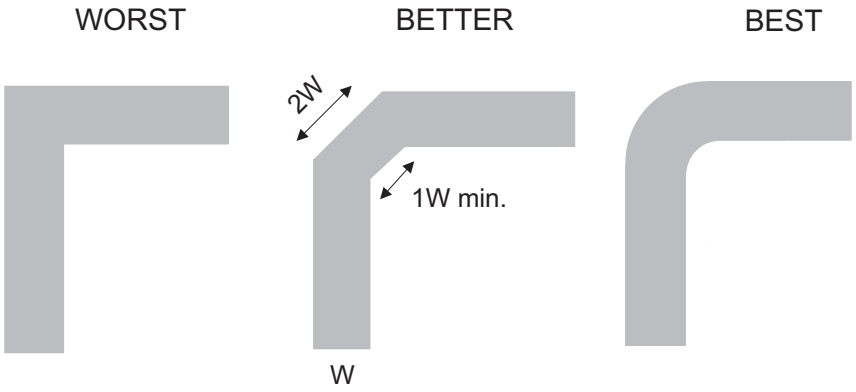



**Figure 26. Trace Example**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Device Nomenclature

**Table 2. Parameter Description**

| SYMBOL | DESCRIPTION |
|---|---|
| $V_{COM}$ | Voltage at COM |
| $V_{NC}$ | Voltage at NC |
| $V_{NO}$ | Voltage at NO |
| $r_{on}$ | Resistance between COM and NC or NO ports when the channel is ON |
| $\Delta r_{on}$ | Difference of $r_{on}$ between channels in a specific device |
| $r_{on(flat)}$ | Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions |
| $I_{NC(OFF)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state |
| $I_{NC(ON)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open |
| $I_{NO(OFF)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state |
| $I_{NO(ON)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open |
| $I_{COM(OFF)}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state |
| $I_{COM(ON)}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open |
| $V_{IH}$ | Minimum input voltage for logic high for the control input (IN, $\overline{EN}$) |
| $V_{IL}$ | Maximum input voltage for logic low for the control input (IN, $\overline{EN}$) |
| $V_I$ | Voltage at the control input (IN, $\overline{EN}$) |
| $I_{IH}$, $I_{IL}$ | Leakage current measured at the control input (IN, $\overline{EN}$) |
| $t_{ON}$ | Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output NC or NO) signal when the switch is turning ON. |
| $t_{OFF}$ | Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF. |
| $Q_C$ | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage. |
| $C_{NC(OFF)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF |
| $C_{NC(ON)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON |
| $C_{NO(OFF)}$ | Capacitance at the NC port when the corresponding channel (NO to COM) is OFF |
| $C_{NO(ON)}$ | Capacitance at the NC port when the corresponding channel (NO to COM) is ON |
| $C_{COM(OFF)}$ | Capacitance at the COM port when the corresponding channel (COM to NC) is OFF |
| $C_{COM(ON)}$ | Capacitance at the COM port when the corresponding channel (COM to NC) is ON |
| $C_I$ | Capacitance of control input (IN, $\overline{EN}$) |
| $O_{ISO}$ | OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state. |
| $X_{TALK}$ | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2) .This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain. |
| THD | Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic. |
| $I_+$ | Static power-supply current with the control (IN) pin at $V_+$ or GND |

## 12.2 Documentation Support

### 12.2.1 Related Documentation

- *Implications of Slow or Floating CMOS Inputs,* SCBA004

## 12.3 Trademarks

All trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TS3A5017D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -40 to 85 | TS3A5017 |
| TS3A5017DBQR | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YA017 |
| TS3A5017DBQR.B | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YA017 |
| TS3A5017DBQRG4 | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YA017 |
| TS3A5017DBQRG4.B | Active | Production | SSOP (DBQ) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YA017 |
| TS3A5017DGVR | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YA017 |
| TS3A5017DGVR.B | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YA017 |
| TS3A5017DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS3A5017 |
| TS3A5017DR.B | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS3A5017 |
| TS3A5017PW | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 85 | YA017 |
| TS3A5017PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YA017 |
| TS3A5017PWR.B | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YA017 |
| TS3A5017RGYR | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YA017 |
| TS3A5017RGYR.B | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YA017 |
| TS3A5017RSVR | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZVL |
| TS3A5017RSVR.B | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZVL |
| TS3A5017RSVRG4 | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZVL |
| TS3A5017RSVRG4.B | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZVL |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TS3A5017 :**

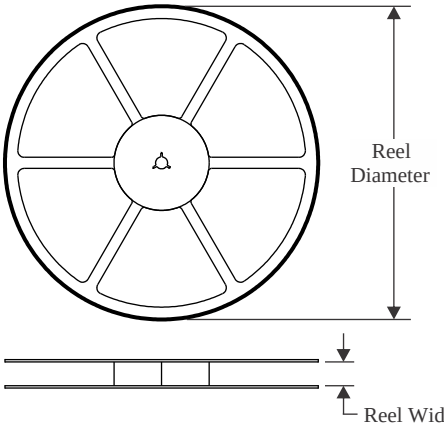
- Automotive : TS3A5017-Q1

NOTE: Qualified Version Definitions:

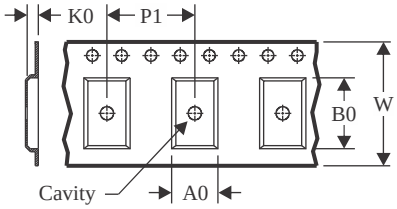
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

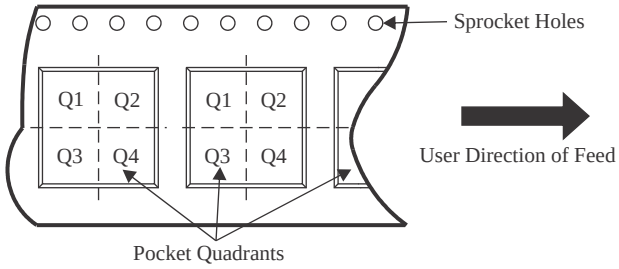



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

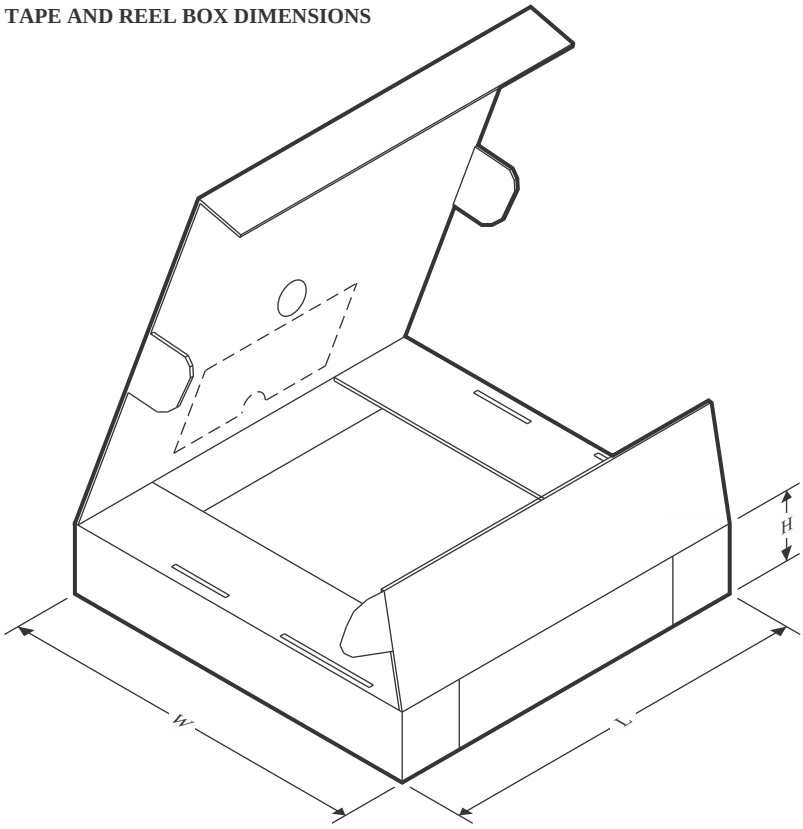
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS3A5017DBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TS3A5017DBQRG4 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TS3A5017DGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| TS3A5017DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TS3A5017PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TS3A5017RGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| TS3A5017RSVR | UQFN | RSV | 16 | 3000 | 180.0 | 12.4 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |
| TS3A5017RSVRG4 | UQFN | RSV | 16 | 3000 | 180.0 | 12.4 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

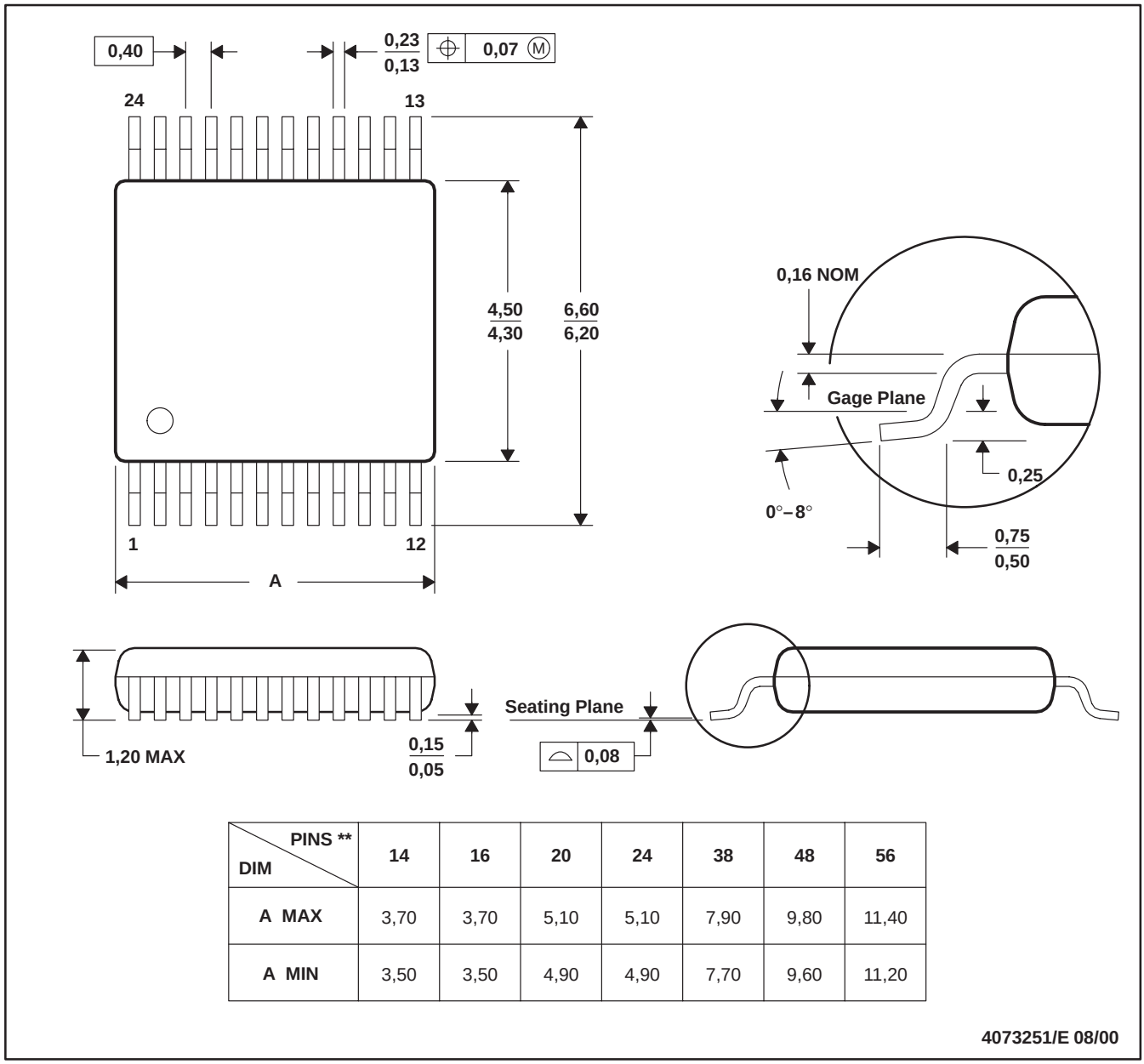



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS3A5017DBQR | SSOP | DBQ | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| TS3A5017DBQRG4 | SSOP | DBQ | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| TS3A5017DGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TS3A5017DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| TS3A5017PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TS3A5017RGYR | VQFN | RGY | 16 | 3000 | 356.0 | 356.0 | 35.0 |
| TS3A5017RSVR | UQFN | RSV | 16 | 3000 | 200.0 | 183.0 | 25.0 |
| TS3A5017RSVRG4 | UQFN | RSV | 16 | 3000 | 200.0 | 183.0 | 25.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

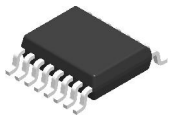
**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

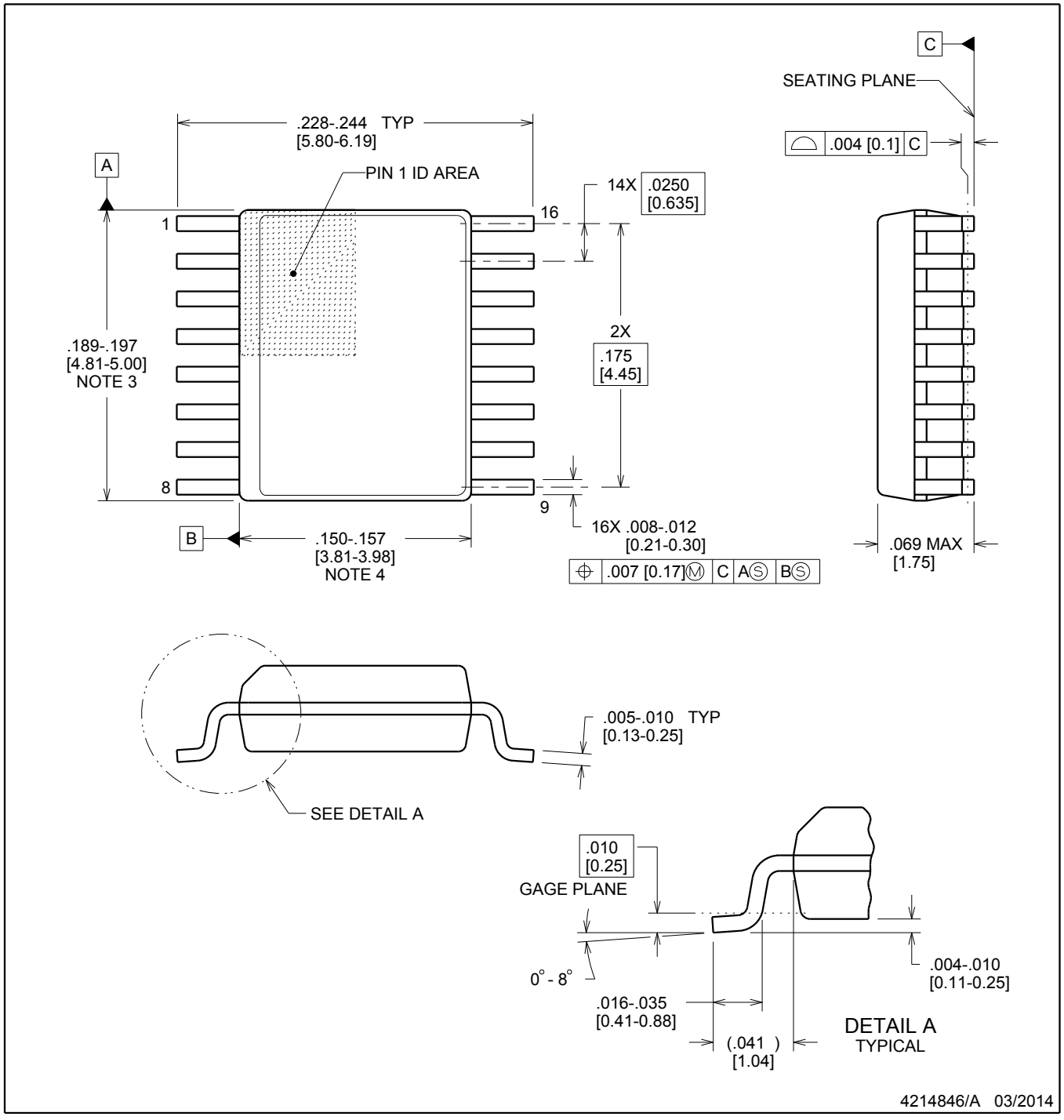


# PACKAGE OUTLINE

## DBQ0016A

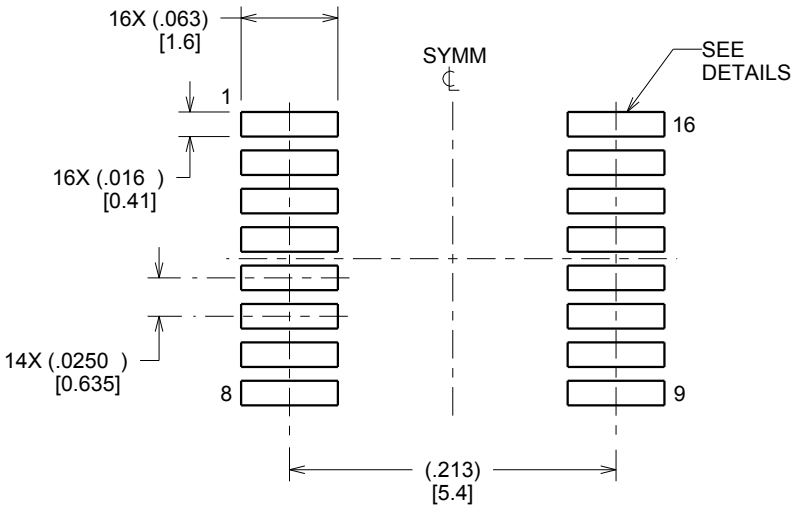
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

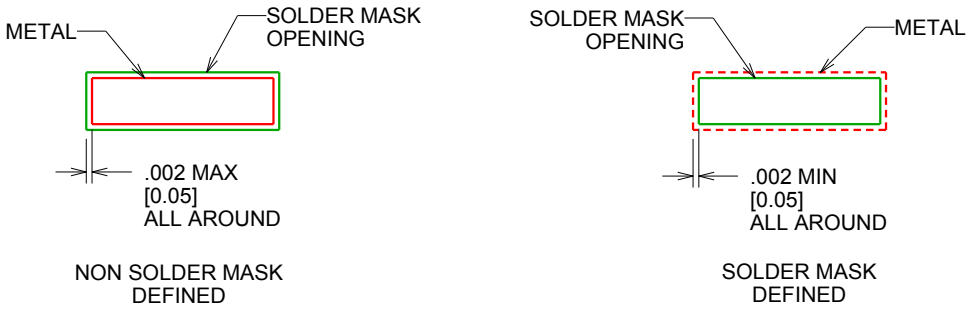



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

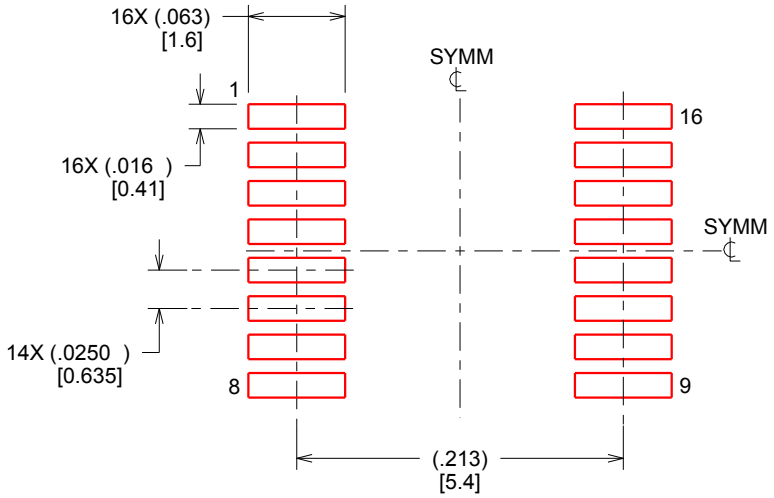
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



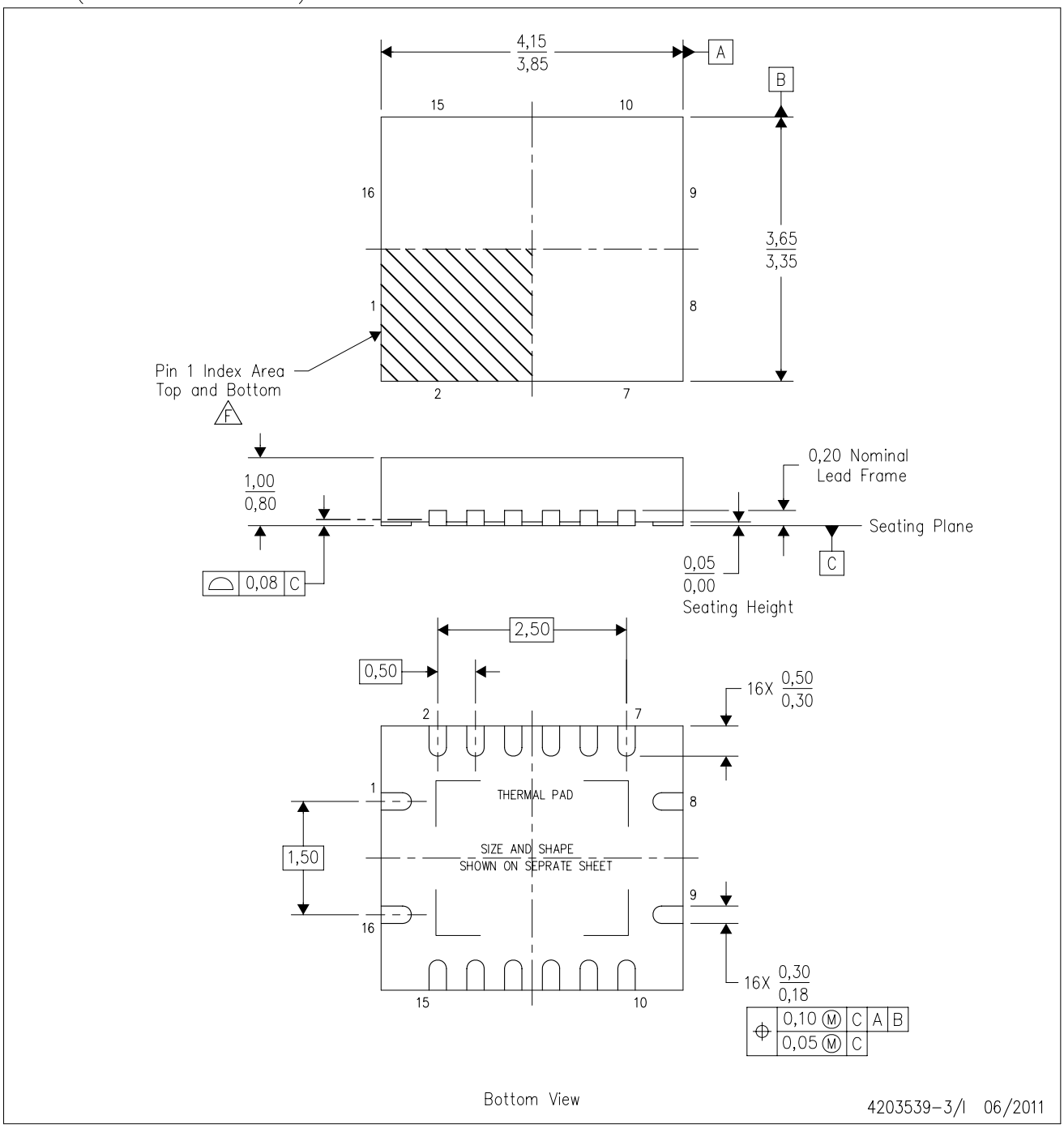

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

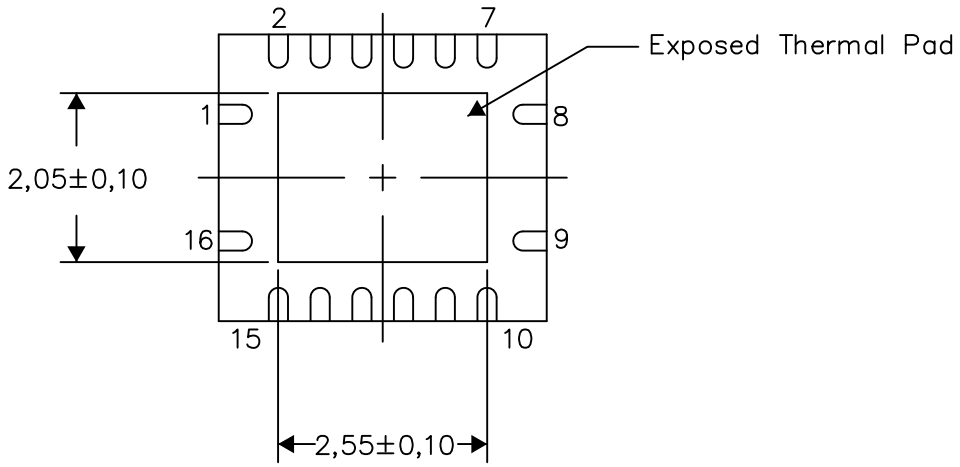
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



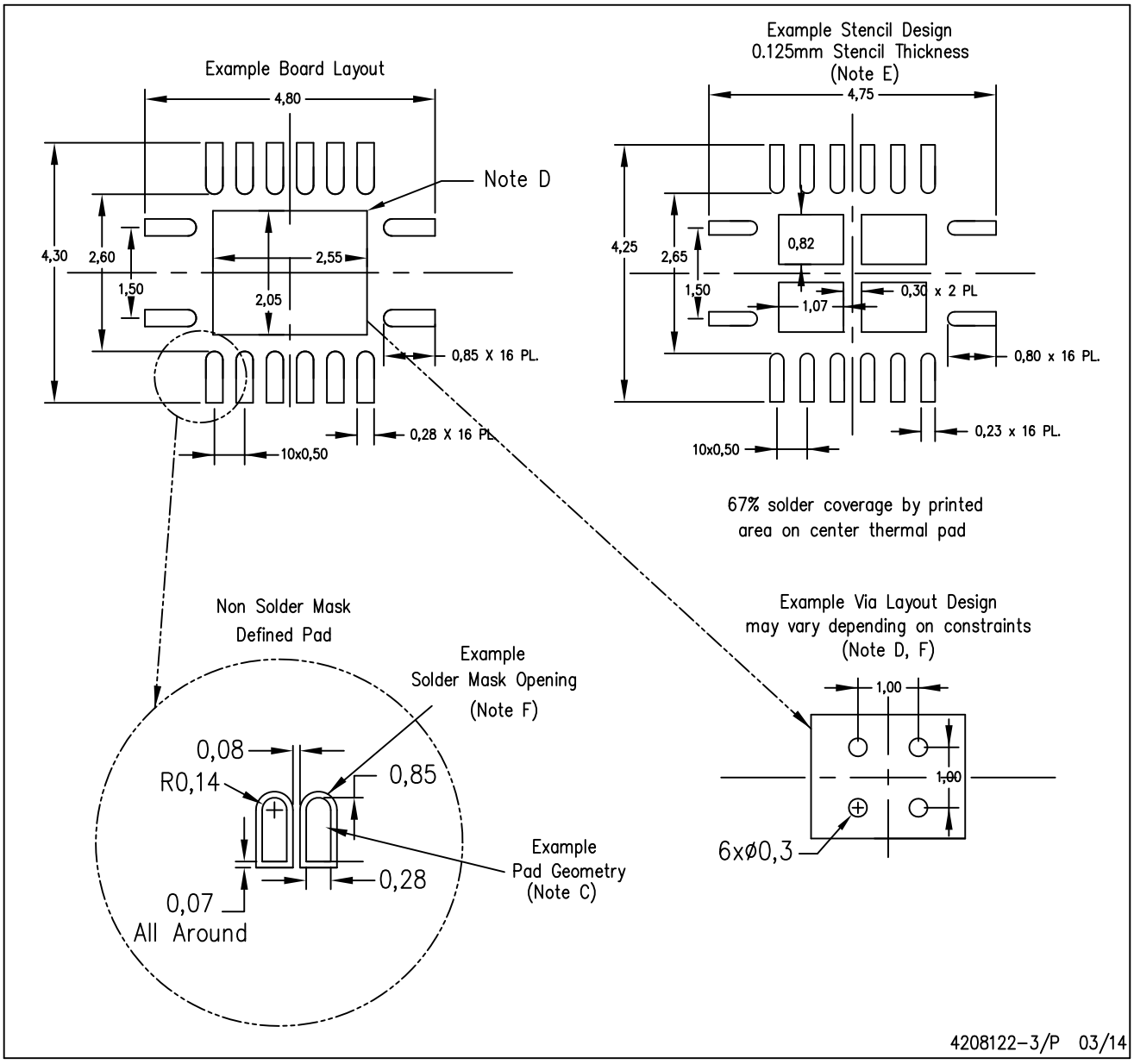

Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

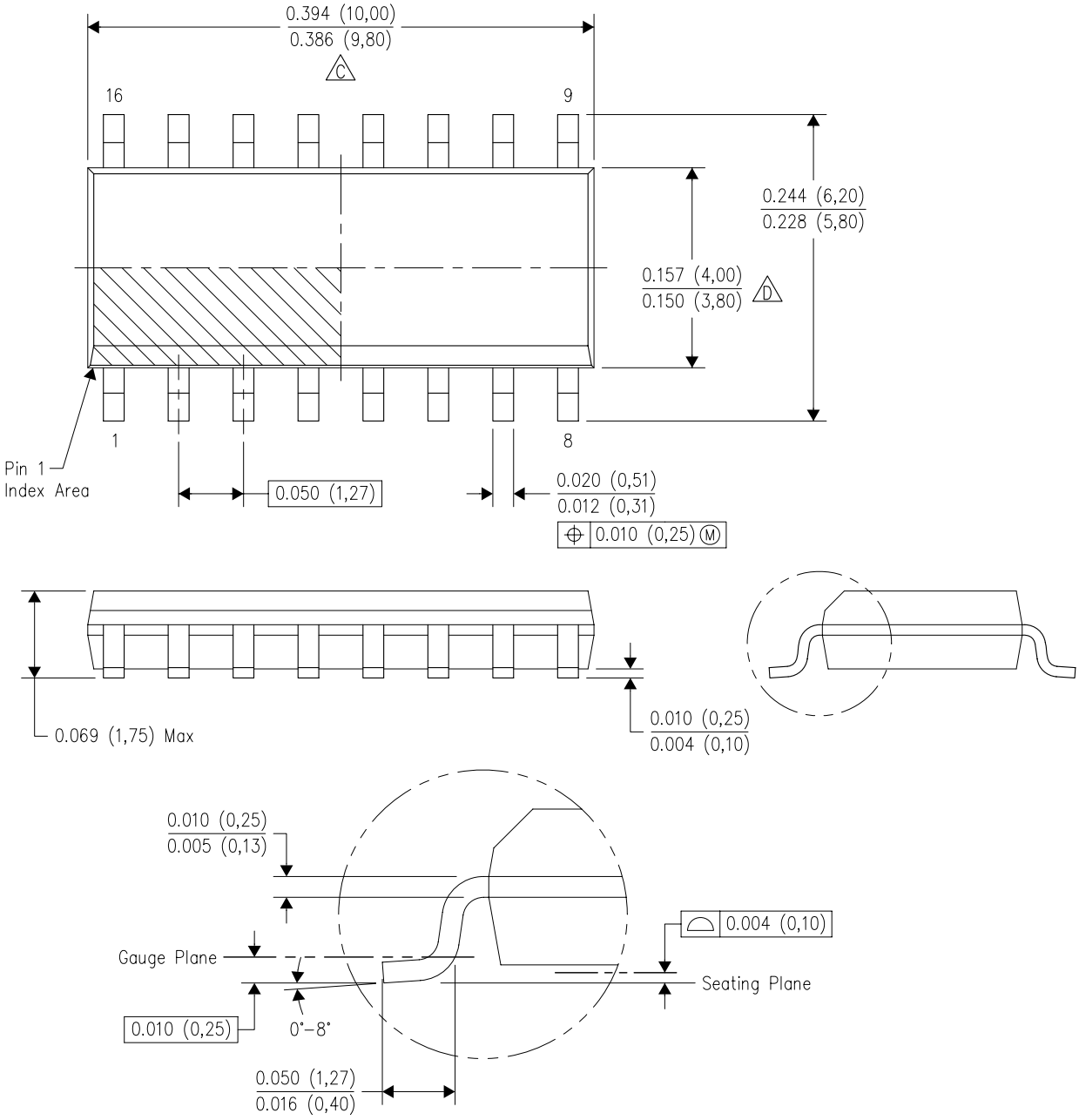
NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



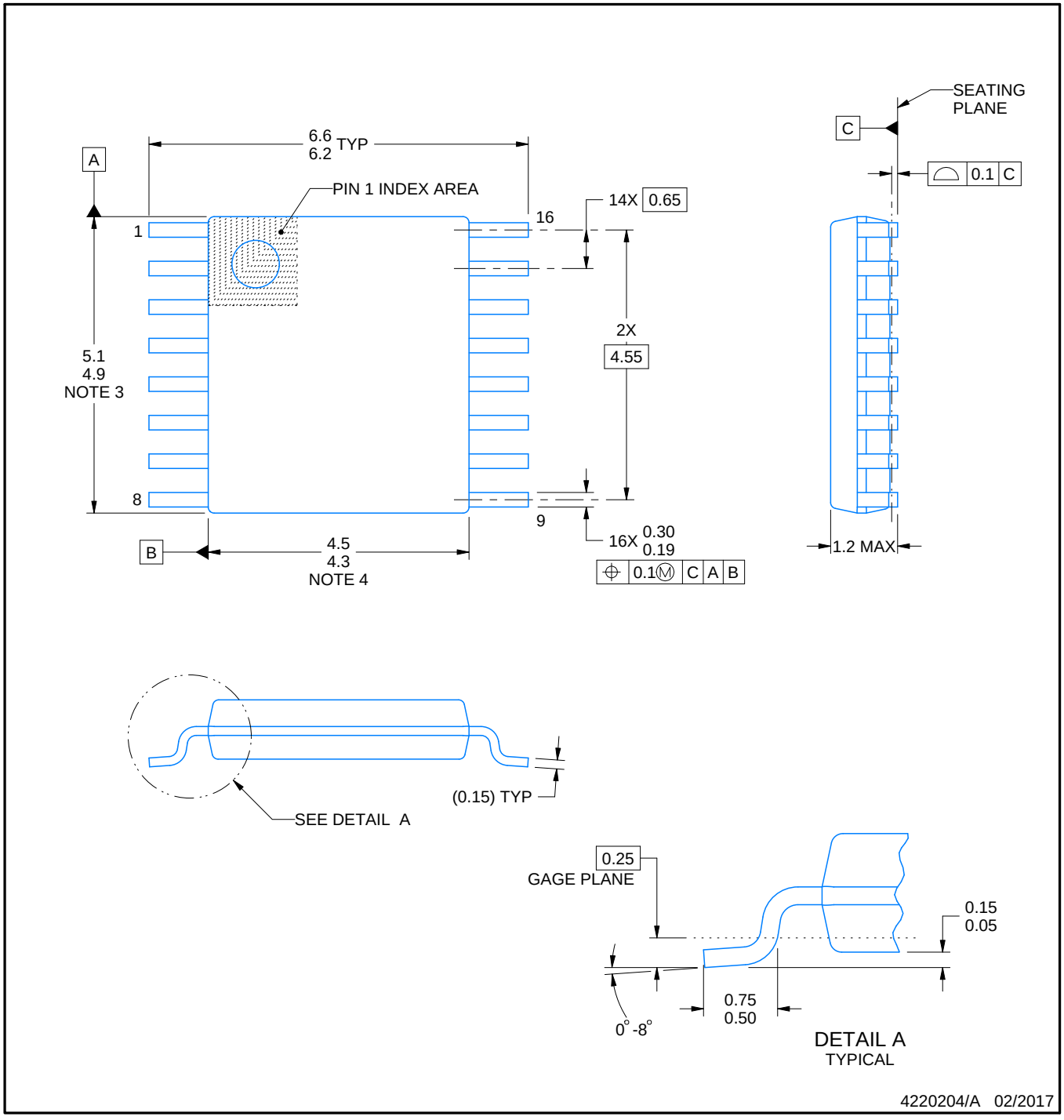

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## PW0016A

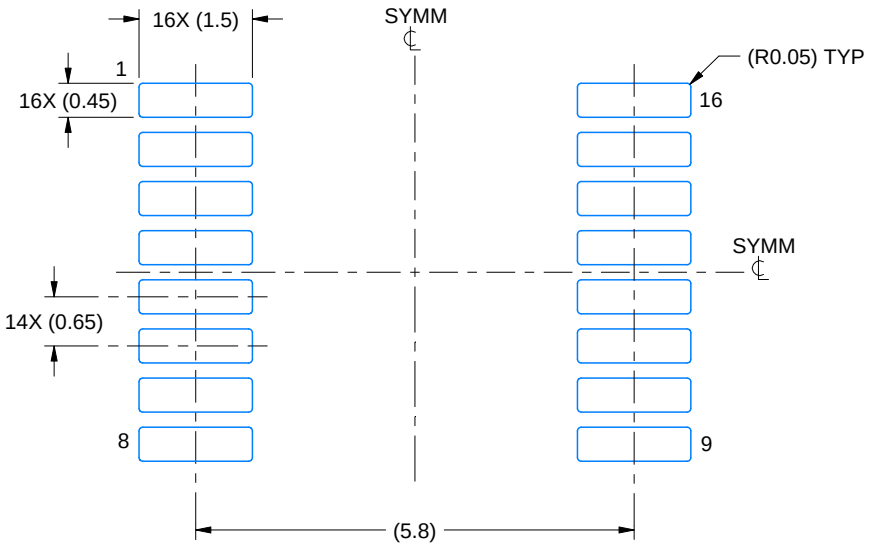
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

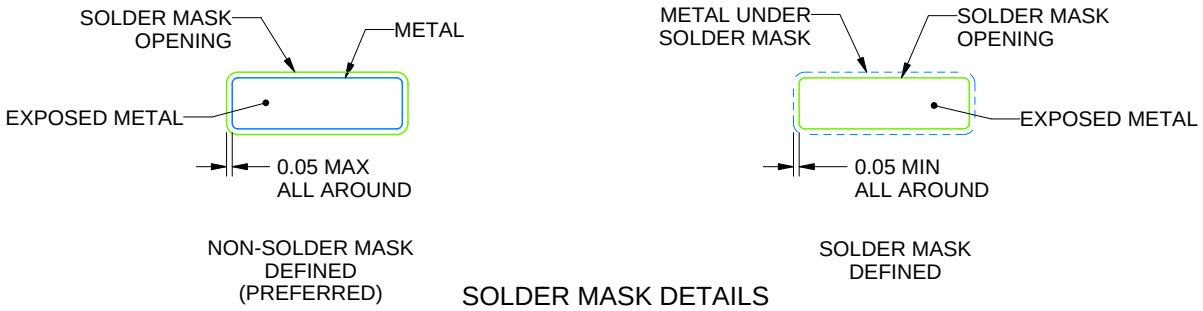



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

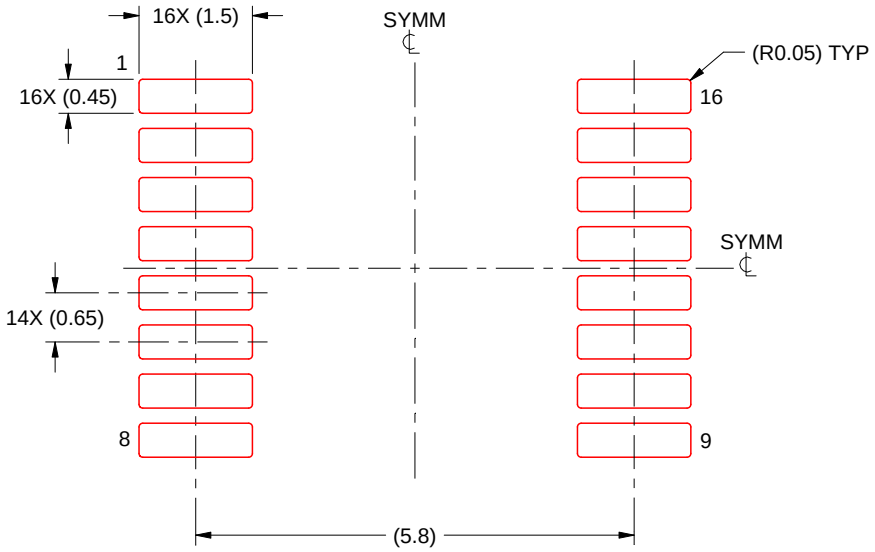



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

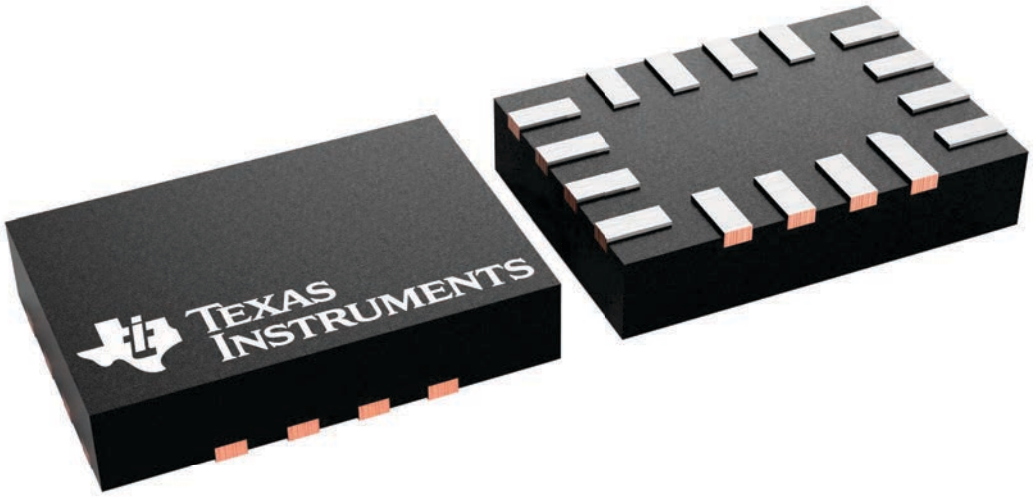
## RSV 16

## UQFN - 0.55 mm max height

**1.8 x 2.6, 0.4 mm pitch**

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



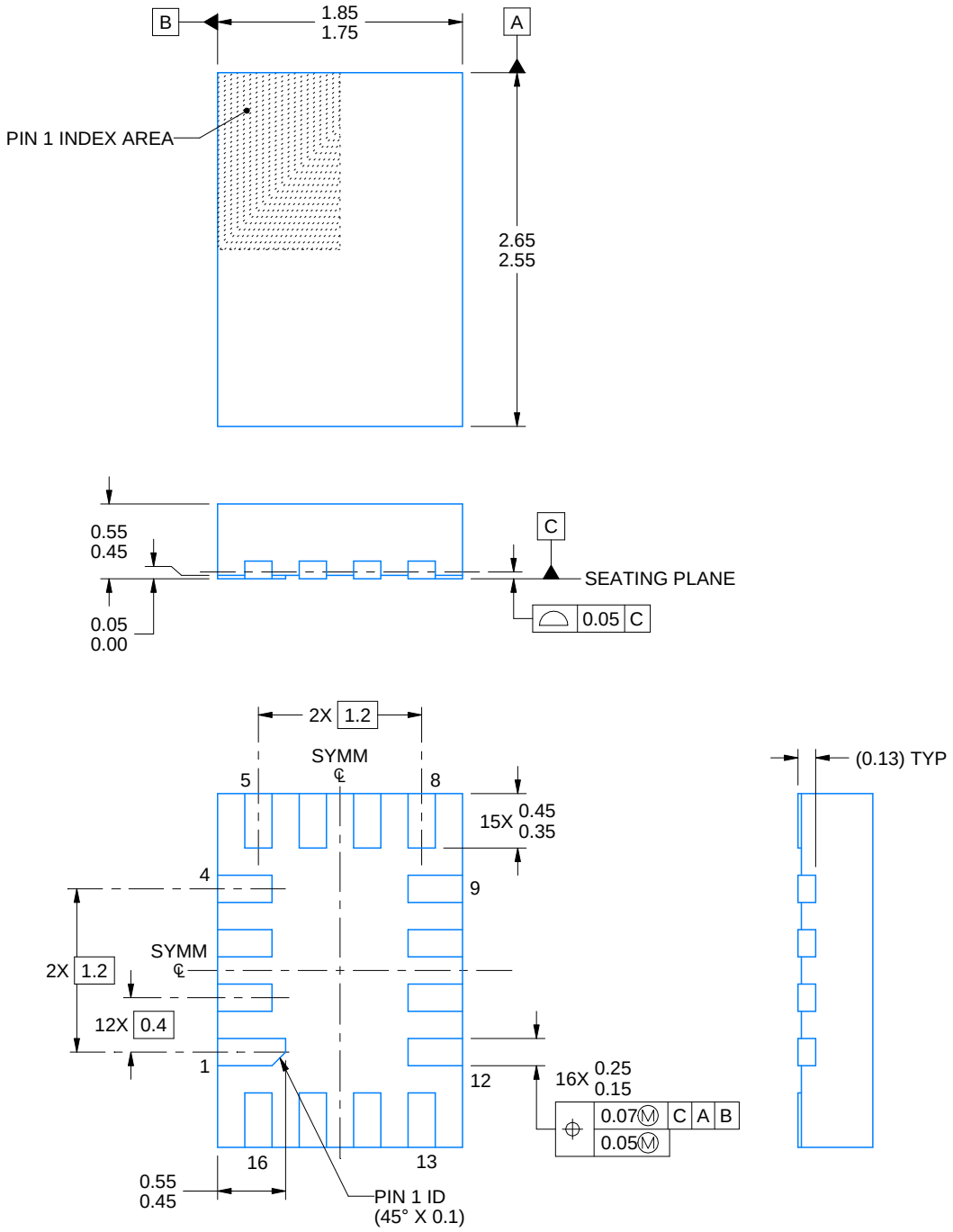

4231225/A

# RSV0016A

# PACKAGE OUTLINE

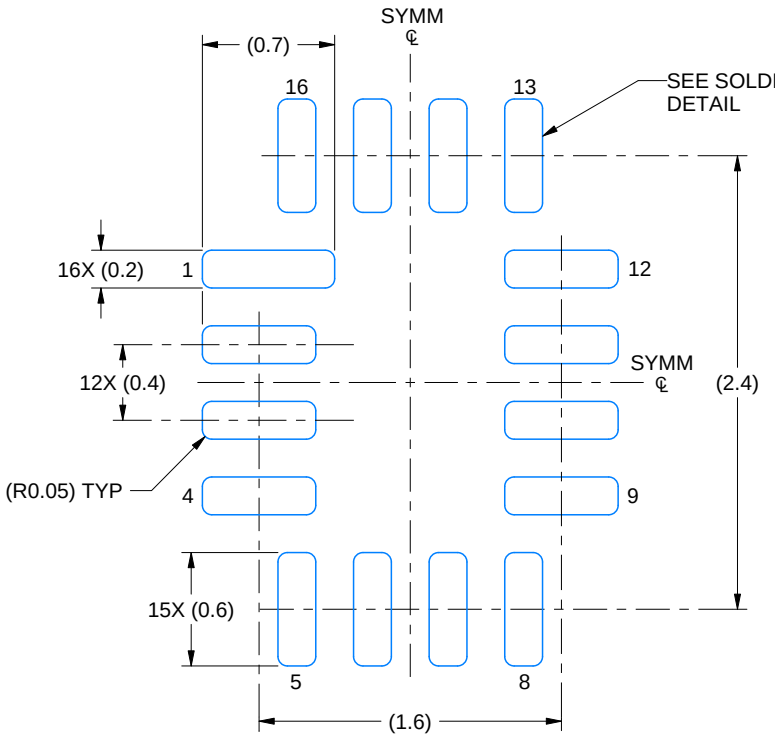
## UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

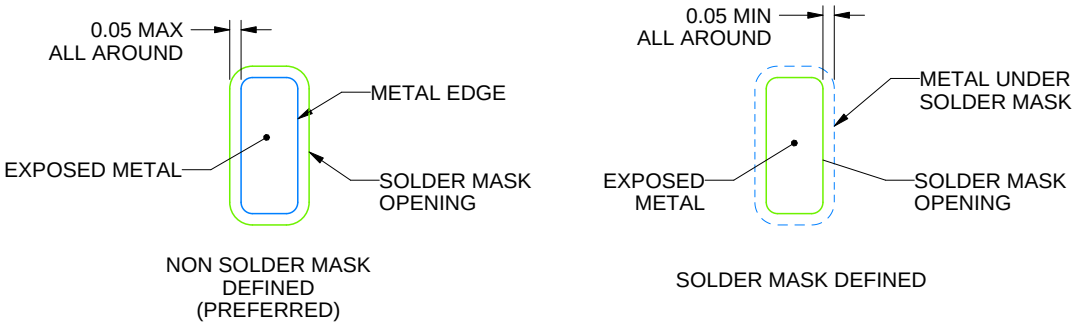



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

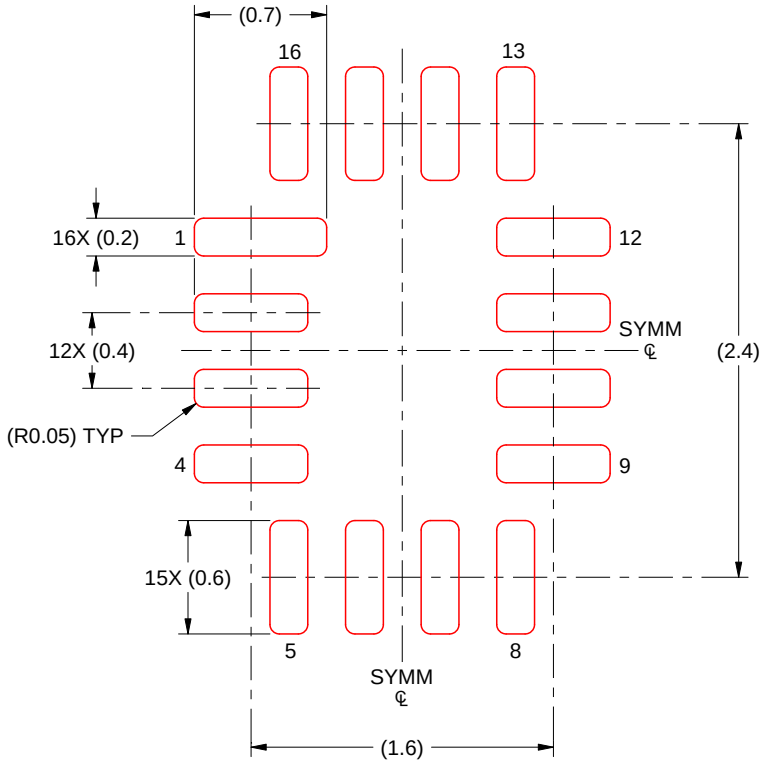



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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