

SLLS871-NOVEMBER 2007

FEATURES

- Controlled Baseline
 - One Assembly
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Meets or Exceeds the Requirements of TIA/EIA-422-B and ITU Recommendation V.11
- Low Power, $I_{CC} = 100 \ \mu A Typ$
- Operates From a Single 5 V Supply
- High Speed, t_{PLH} = t_{PHL} = 7 ns Typ
- Low Pulse Distortion, t_{sk(p)} = 0.5 ns Typ
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION/ORDERING INFORMATION

The AM26C31 is a differential line driver with complementary outputs, designed to meet the requirements of TIA/EIA -422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines, such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable functions are common to all four drivers and offer the choice of an active-high (G) or active-low (\overline{G}) enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

The AM26C31 is characterized for operation over extended temperature range of –55°C to 125°C.

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Reel of 2500	AM26C31MDREP	26C31EP

ORDERING INFORMATION⁽¹⁾

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Improved Replacement for AM26LS31

AM26C3	81.	D PACKAGE
1A [1Y [1Z [2Z [2Y [2A [GND [1 2 3 4 5 6 7 8	16 V _{CC} 15 4A 14 4Y 13 4Z 12 G 11 3Z 10 3Y 9 3A

AM26C31-EP QUADRUPLE DIFFERENTIAL LINE DRIVER

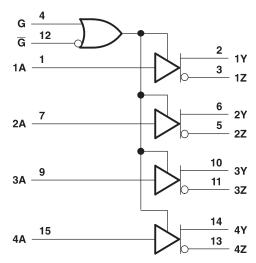
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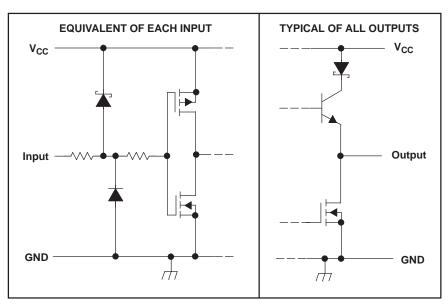
FUNCTION TABLE (each driver)

INPUT	ENA	BLES	OUT	PUT
Α	G	G	Y	Z
Н	Н	Х	Н	L
L	н	Х	L	Н
Н	Х	L	Н	L
L	Х	L	L	Н
Х	L	н	Z	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS OF INPUTS AND OUTPUTS





ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.5	7	V
VI	Input voltage range	-0.5	V _{CC} + 0.5	V
V _{ID}	Differential input voltage range	-14	14	V
Vo	Output voltage range	-0.5	7	V
I _{IK} or I _{OK}	Input or output clamp current		±20	mA
lo	Output current		±150	mA
	V _{CC} current		200	mA
	GND current		-200	mA
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾		73	°C/W
TJ	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)

All voltage values, except differential output voltage (V_{OD}), are with respect to the network ground terminal. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. (3)

The package thermal impedance is calculated in accordance with JESD 51-7. (4)

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V_{ID}	Differential input voltage		±7		V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			-20	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature	-55		125	°C

AM26C31-EP QUADRUPLE DIFFERENTIAL LINE DRIVER

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ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TES	CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	$I_0 = -20 \text{ mA}$		2.2	3.4		V
V _{OL}	Low-level output voltage	l _O = 20 mA			0.2	0.4	V
V _{OD}	Differential output voltage magnitude	$R_L = 100 \ \Omega,$	See Figure 1	2	3.1		V
$\Delta V_{OD} $	Change in magnitude of differential output voltage ⁽²⁾	$R_L = 100 \ \Omega,$	See Figure 1			±0.4	V
V _{OC}	Common-mode output voltage	$R_L = 100 \ \Omega,$	See Figure 1			3	V
Δ V _{OC}	Change in magnitude of common-mode output voltage ⁽²⁾	$R_L = 100 \Omega$,	See Figure 1			±0.4	V
I _I	Input current	$V_{I} = V_{CC}$ or C	ND			±1	μA
	Driver extent extremt with newer off	V 0	V _O = 6 V			100	۸
I _{O(off)}	Driver output current with power off	$V_{CC} = 0$	V _O = -0.25 V			-100	μA
I _{OS}	Driver output short-circuit current	$V_0 = 0$				-170	mA
	Link impedance off state entropy entropy	V _O = 2.5 V				20	A
I _{OZ}	High-impedance off-state output current	$V_{0} = 0.5 V$				-20	μA
	Ouissesst sussels sussent	I _O = 0	$V_{I} = 0 V \text{ or } 5 V$			100	μA
I _{CC}	Quiescent supply current	I _O = 0	$V_{I} = 2.4 \text{ V or } 0.5 \text{ V}^{(3)}$			3.2	mA
CI	Input capacitance		·		6		pF

All typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}C$. (1)

 $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level (2)to a low level.

This parameter is measured per input. All other inputs are at 0 V or 5 V. (3)

SWITCHING CHARACTERISTICS

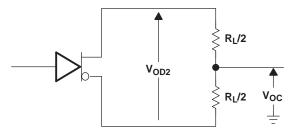
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST C	CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	S1 is open,	See Figure 2		7	12	ns
t _{PHL}	Propagation delay time, high- to low-level output	S1 is open,	See Figure 2		6.5	12	ns
t _{sk(p)}	Pulse skew time (t _{PLH} – t _{PHL})	S1 is open,	See Figure 2		0.5	4	ns
t _{r(OD)} , t _{f(OD)}	Differential output rise and fall times	S1 is open,	See Figure 3		5	12	ns
t _{PZH}	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
t _{PZL}	Output enable time to low level	S1 is closed,	See Figure 4		10	19	ns
t _{PHZ}	Output disable time from high level	S1 is closed,	See Figure 4		7	16	ns
t _{PLZ}	Output disable time from low level	S1 is closed,	See Figure 4		7	16	ns
C _{pd}	Power dissipation capacitance (each driver) ⁽²⁾	S1 is open,	See Figure 2		100		pF

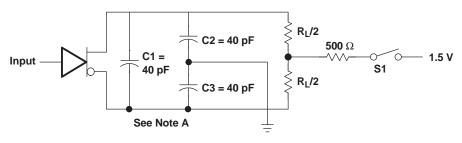
(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}^2 \times f$, where f is the switching frequency.



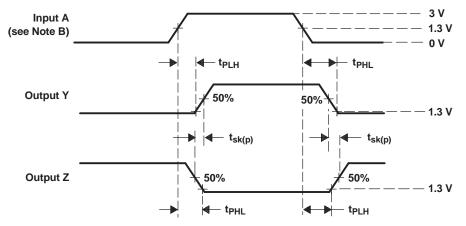
PARAMETER MEASUREMENT INFORMATION











- A. C1, C2, and C3 include probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, and t_r, t_f \leq 6 ns.

Figure 2. Propagation Delay Time and Skew Waveforms and Test Circuit

R_L/2 C2 = 40 pF **500** Ω C1 = - 1.5 V $\sim \sim$ 0 Input **S**1 40 pF ≶ R_L/2 C3 = 40 pFSee Note A **TEST CIRCUIT** 3 V Input A (see Note B) 0 V 90% 90% Differential 10% 10% Output – t_{f(OD)} tr(OD) **VOLTAGE WAVEFORMS**

PARAMETER MEASUREMENT INFORMATION (continued)

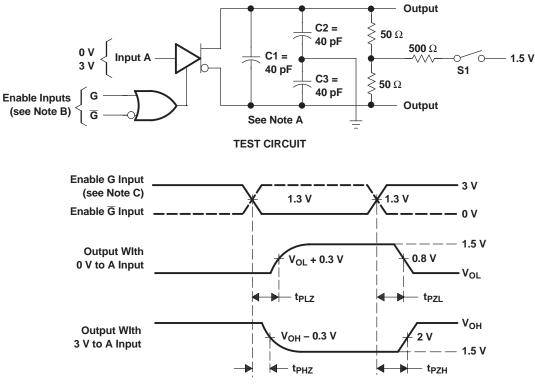
- A. C1, C2, and C3 include probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, and t_r, t_f \leq 6 ns.

Figure 3. Differential Output Rise and Fall Time Waveforms and Test Circuit



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PARAMETER MEASUREMENT INFORMATION (continued)



VOLTAGE WAVEFORMS

- A. C1, C2, and C3 include probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, t_r < 6 ns, and t_f < 6 ns.
- C. Each enable is tested separately.

Figure 4. Output Enable and Disable Time Waveforms and Test Circuit



TYPICAL CHARACTERISTICS

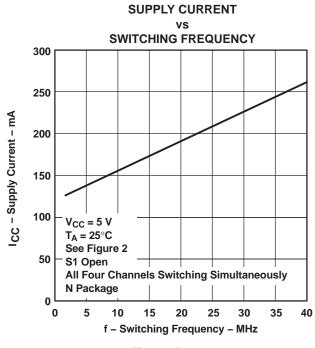


Figure 5.



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
AM26C31MDREP	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP
AM26C31MDREP.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP
V62/07647-01XE	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF AM26C31-EP :

Catalog : AM26C31



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23-May-2025

Military : AM26C31M

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

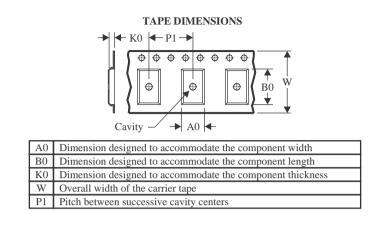
• Military - QML certified for Military and Defense Applications



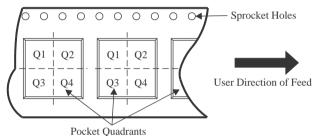
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*	All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	AM26C31MDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



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PACKAGE MATERIALS INFORMATION

10-Jan-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C31MDREP	SOIC	D	16	2500	340.5	336.1	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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