

## DAC0800/DAC0802 8-Bit Digital-to-Analog Converters

Check for Samples: [DAC0800](#), [DAC0802](#)

### FEATURES

- **Fast Settling Output Current:** 100 ns
- **Full Scale Error:**  $\pm 1$  LSB
- **Nonlinearity Over Temperature:**  $\pm 0.1\%$
- **Full Scale Current Drift:**  $\pm 10$  ppm/ $^{\circ}\text{C}$
- **High Output Compliance:**  $-10\text{V}$  to  $+18\text{V}$
- **Complementary Current Outputs**
- **Interface Directly with TTL, CMOS, PMOS and Others**
- **2 Quadrant Wide Range Multiplying Capability**
- **Wide Power Supply Range:**  $\pm 4.5\text{V}$  to  $\pm 18\text{V}$
- **Low Power Consumption:** 33 mW at  $\pm 5\text{V}$
- **Low Cost**

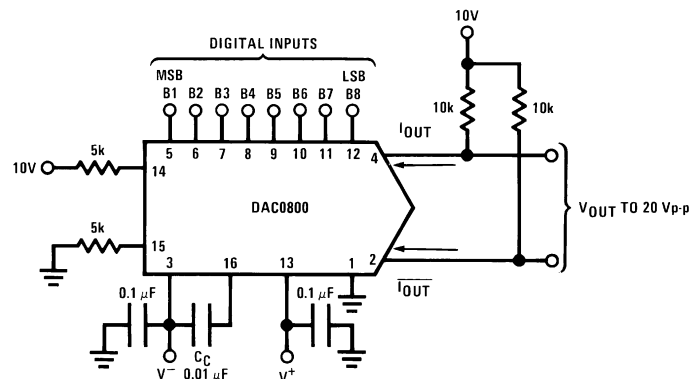
### DESCRIPTION

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 V<sub>p-p</sub> with simple resistor loads. The reference-to-full-scale current matching of better than  $\pm 1$  LSB eliminates the need for full-scale trims in most applications, while the nonlinearities of better than  $\pm 0.1\%$  over temperature minimizes system error accumulations.

The noise immune inputs will accept a variety of logic levels. The performance and characteristics of the device are essentially unchanged over the  $\pm 4.5\text{V}$  to  $\pm 18\text{V}$  power supply range and power consumption at only 33 mW with  $\pm 5\text{V}$  supplies is independent of logic input levels.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively. For single supply operation, refer to AN-1525.

### Typical Application



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 1.  $\pm 20$  V<sub>p-p</sub> Output Digital-to-Analog Converter**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

**Absolute Maximum Ratings** <sup>(1)</sup>

Supply Voltage ( $V^+ - V^-$ )	$\pm 18V$ or $36V$
Power Dissipation <sup>(2)</sup>	500 mW
Reference Input Differential Voltage (V14 to V15)	$V^-$ to $V^+$
Reference Input Common-Mode Range (V14, V15)	$V^-$ to $V^+$
Reference Input Current	5 mA
Logic Inputs	$V^-$ to $V^-$ plus $36V$
Analog Current Outputs ( $V_{S-} = -15V$ )	4.25 mA
ESD Susceptibility <sup>(3)</sup>	TBD V
Storage Temperature	$-65^\circ C$ to $+150^\circ C$
Lead Temp. (Soldering, 10 seconds)	
PDIP Package (plastic)	$260^\circ C$
CDIP Package (ceramic)	$300^\circ C$
Surface Mount Package	
Vapor Phase (60 seconds)	$215^\circ C$
Infrared (15 seconds)	$220^\circ C$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
- (2) The maximum junction temperature of the DAC0800 and DAC0802 is  $125^\circ C$ . For operating at elevated temperatures, devices in the CDIP package must be derated based on a thermal resistance of  $100^\circ C/W$ , junction-to-ambient,  $175^\circ C/W$  for the molded PDIP package and  $100^\circ C/W$  for the SOIC package.
- (3) Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

**Operating Conditions** <sup>(1)</sup>

	Min	Max	Units
Temperature ( $T_A$ )			
DAC0800L	$-55$	$+125$	$^\circ C$
DAC0800LC	0	$+70$	$^\circ C$
DAC0802LC	0	$+70$	$^\circ C$
$V^+$	$(V^-) + 10$	$(V^-) + 30$	V
$V^-$	$-15$	$-5$	V
$I_{REF}$ ( $V^- = -5V$ )	1	2	mA
$I_{REF}$ ( $V^- = -15V$ )	1	4	mA

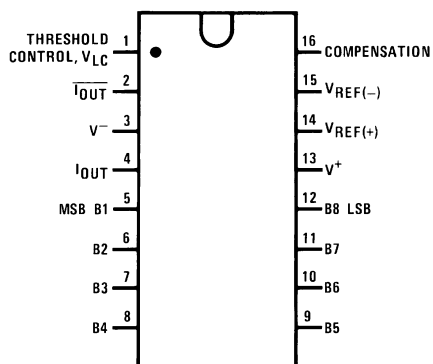
- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

## Electrical Characteristics

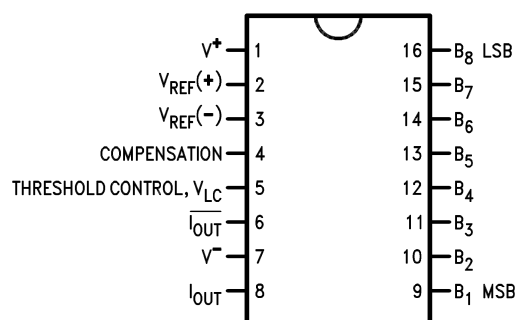
The following specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2\text{ mA}$  and  $T_{MIN} \leq T_A \leq T_{MAX}$  unless otherwise specified. Output characteristics refer to both  $I_{OUT}$  and  $\bar{I}_{OUT}$ .

Parameter		Test Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				$\pm 0.1$			$\pm 0.19$	%FS
$t_s$	Settling Time	To $\pm \frac{1}{2}$ LSB, All Bits Switched "ON" or "OFF", $T_A = 25^\circ\text{C}$		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Each Bit All Bits Switched	$T_A = 25^\circ\text{C}$		35	60		35	60	ns
				35	60		35	60	ns
$TC_{IFS}$	Full Scale Tempco			$\pm 10$	$\pm 50$		$\pm 10$	$\pm 50$	ppm/ $^\circ\text{C}$
$V_{OC}$	Output Voltage Compliance	Full Scale Current Change $< \frac{1}{2}$ LSB, $R_{OUT} > 20\text{ M}\Omega$ , Typical	-10		18	-10		18	V
$I_{FS4}$	Full Scale Current	$V_{REF} = 10.000V$ , $R_{14} = R_{15} = 5.000\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	1.984	1.992	2.00	1.94	1.99	2.04	mA
$I_{FSS}$	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		$\pm 0.5$	$\pm 4.0$		$\pm 1$	$\pm 8.0$	$\mu\text{A}$
$I_{ZS}$	Zero Scale Current			0.1	1.0		0.2	2.0	$\mu\text{A}$
$I_{FSR}$	Output Current Range	$V^- = -5V$	0	2.0	2.1	0	2.0	2.1	mA
		$V^- = -8V$ to $-18V$	0	2.0	4.2	0	2.0	4.2	
$V_{IL}$ $V_{IH}$	Logic Input Levels Logic "0" Logic "1"	$V_{LC} = 0V$			0.8			0.8	V
			2.0			2.0			V
$I_{IL}$ $I_{IH}$	Logic Input Current Logic "0" Logic "1"	$V_{LC} = 0V$		-2.0	-10		-2.0	-10	$\mu\text{A}$
		$-10V \leq V_{IN} \leq +0.8V$							
		$2V \leq V_{IN} \leq +18V$		0.002	10		0.002	10	$\mu\text{A}$
$V_{IS}$	Logic Input Swing	$V^- = -15V$	-10		18	-10		18	V
$V_{THR}$	Logic Threshold Range	$V_S = \pm 15V$	-10		13.5	-10		13.5	V
$I_{15}$	Reference Bias Current			-1.0	-3.0		-1.0	-3.0	$\mu\text{A}$
$dI/dt$	Reference Input Slew Rate	(Figure 26)	4.0	8.0		4.0	8.0		mA/ $\mu\text{s}$
$PSSI_{FS+}$	Positive Power Supply Sensitivity	$4.5V \leq V^+ \leq 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$	Negative Power Supply Sensitivity	$-4.5V \leq V^- \leq 18V$ , $I_{REF} = 1\text{ mA}$		0.0001	0.01		0.0001	0.01	%/%
$I^+$ $I^-$	Power Supply Current	$V_S = \pm 5V$ , $I_{REF} = 1\text{ mA}$		2.3	3.8		2.3	3.8	mA
				-4.3	-5.8		-4.3	-5.8	mA
$I^+$ $I^-$	Power Supply Current	$V_S = +5V$ , $-15V$ , $I_{REF} = 2\text{ mA}$		2.4	3.8		2.4	3.8	mA
				-6.4	-7.8		-6.4	-7.8	mA
$I^+$ $I^-$	Power Supply Current	$V_S = \pm 15V$ , $I_{REF} = 2\text{ mA}$		2.5	3.8		2.5	3.8	mA
				-6.5	-7.8		-6.5	-7.8	mA
$P_D$	Power Consumption	$\pm 5V$ , $I_{REF} = 1\text{ mA}$		33	48		33	48	mW
		$+5V$ , $-15V$ , $I_{REF} = 2\text{ mA}$		108	136		108	136	mW
		$\pm 15V$ , $I_{REF} = 2\text{ mA}$		135	174		135	174	mW

## Connection Diagrams

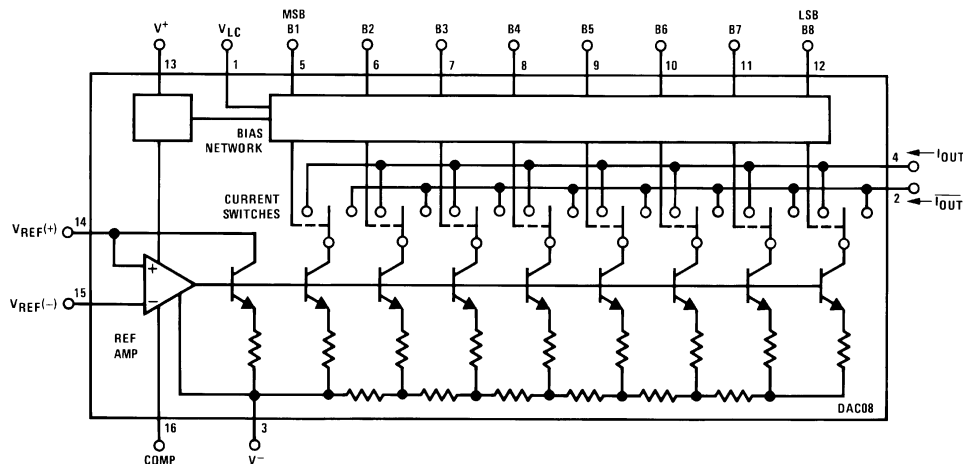


**Figure 2. PDIP, CDIP Packages - Top View**  
(See Package Number NFG0016E or NFE0016A)



**Figure 3. SOIC Package - Top View**  
(See Package Number D0016A)

## Block Diagram



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 4.**

## Typical Performance Characteristics

Full Scale Current  
vs.  
Reference Current

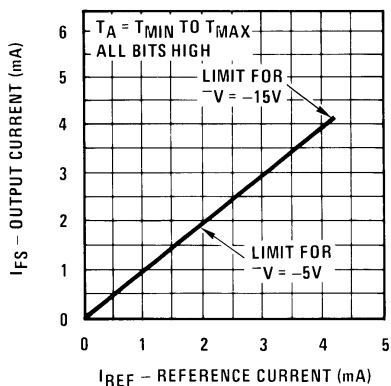


Figure 5.

LSB Propagation Delay  
vs.  
 $I_{FS}$

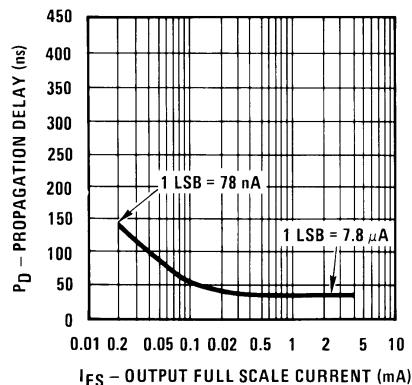
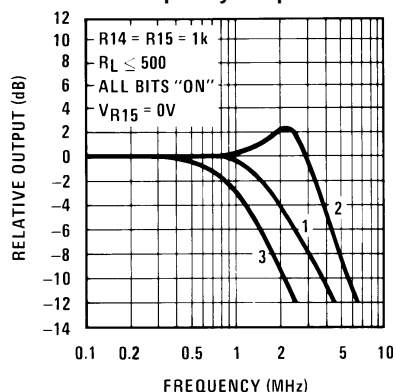


Figure 6.

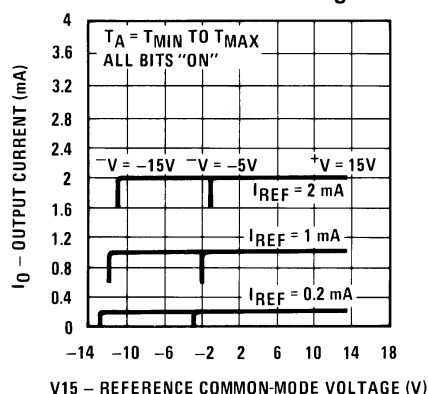
Reference Input  
Frequency Response



Curve 1:  $C_C = 15 \text{ pF}$ ,  $V_{IN} = 2 \text{ Vp-p}$  centered at 1V.  
Curve 2:  $C_C = 15 \text{ pF}$ ,  $V_{IN} = 50 \text{ mVp-p}$  centered at 200 mV.  
Curve 3:  $C_C = 0 \text{ pF}$ ,  $V_{IN} = 100 \text{ mVp-p}$  centered at 0V and applied through  $50\Omega$  connected to pin 14.2V applied to  $R_{14}$ .

Figure 7.

Reference Amp  
Common-Mode Range



Note. Positive common-mode range is always  $(V_+) - 1.5V$ .

Figure 8.

Logic Input Current vs.  
Input Voltage

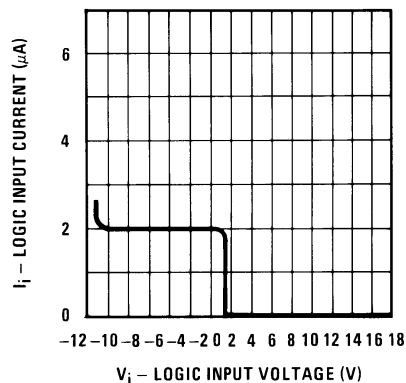


Figure 9.

$V_{TH} - V_{LC}$   
vs.  
Temperature

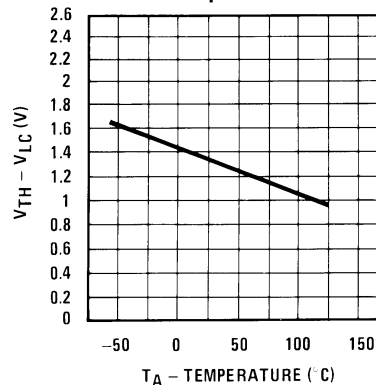


Figure 10.

## Typical Performance Characteristics (continued)

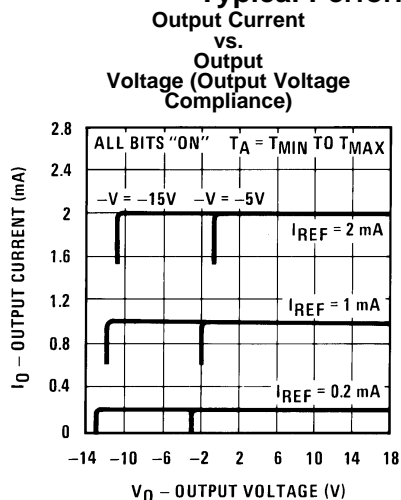


Figure 11.

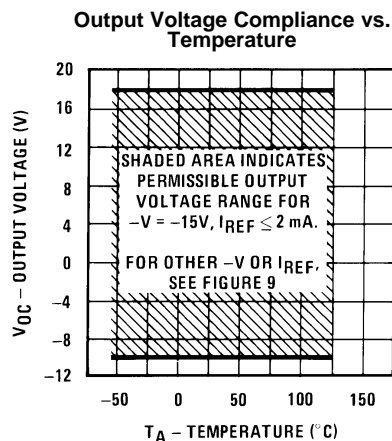
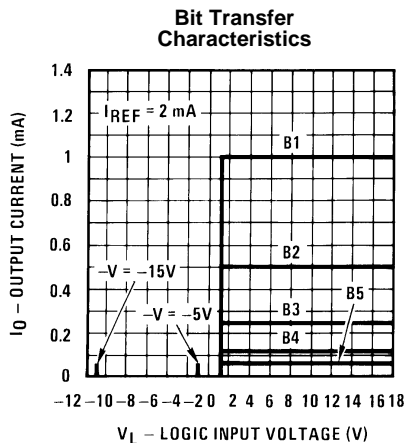


Figure 12.



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range ( $V_{LC} = 0V$ ).

Figure 13.

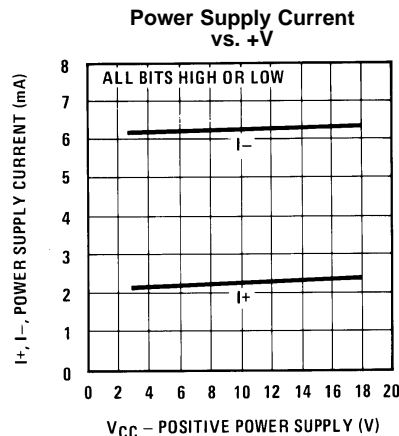


Figure 14.

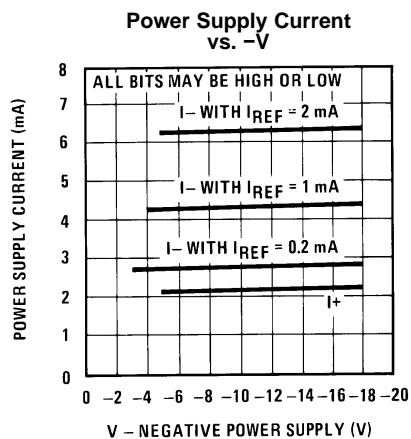


Figure 15.

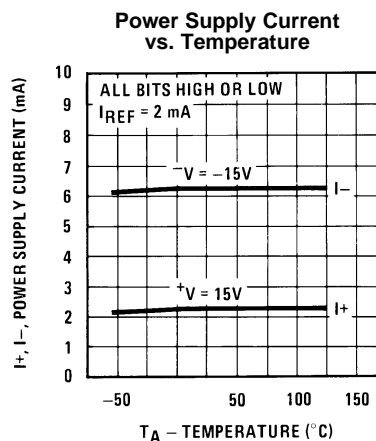
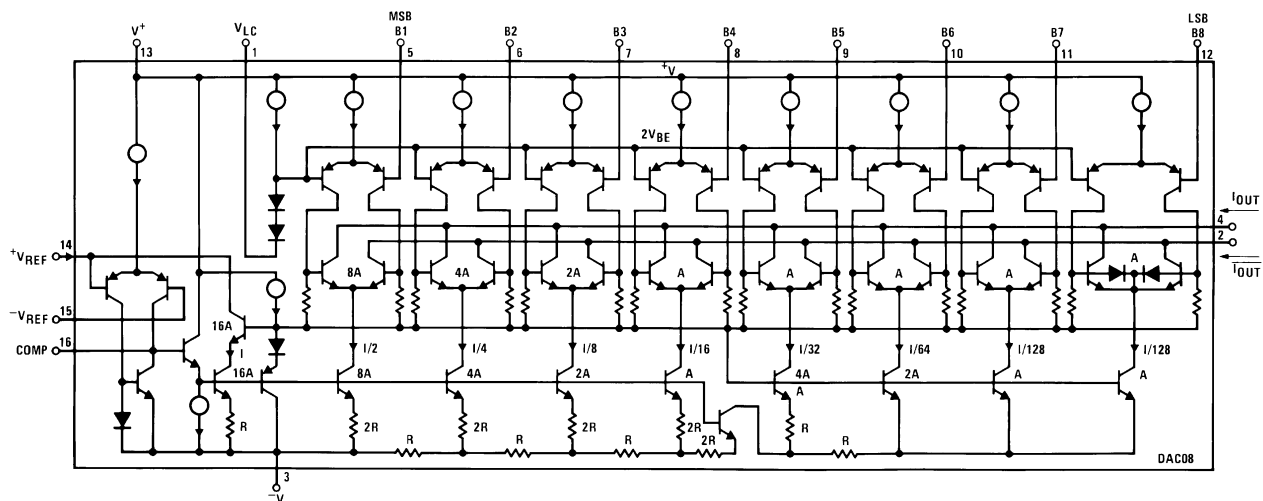


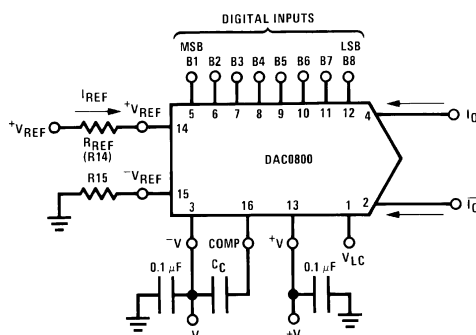
Figure 16.

## EQUIVALENT CIRCUIT



**Figure 17. Equivalent Circuit**

## TYPICAL APPLICATIONS



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \bar{I}_O = I_{FS}$  for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$

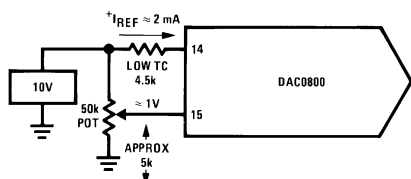
$R_{REF} = 5.000k$

$R15 \approx R_{REF}$

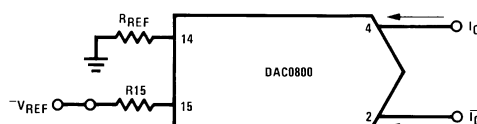
$C_C = 0.01 \mu F$

$V_{LC} = 0V$  (Ground)

**Figure 18. Basic Positive Reference Operation**



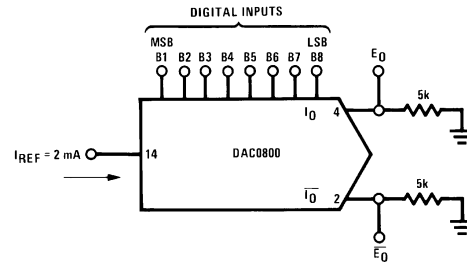
**Figure 19. Recommended Full Scale Adjustment Circuit**



**Figure 20. Basic Negative Reference Operation**

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.



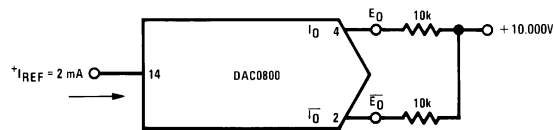


Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 21. Basic Unipolar Negative Operation**

**Table 1. Basic Unipolar Negative Operation**

	B1	B2	B3	B4	B5	B6	B7	B8	$I_O$ mA	$\bar{I}_O$ mA	$E_O$	$\bar{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
Full Scale-LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale-LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

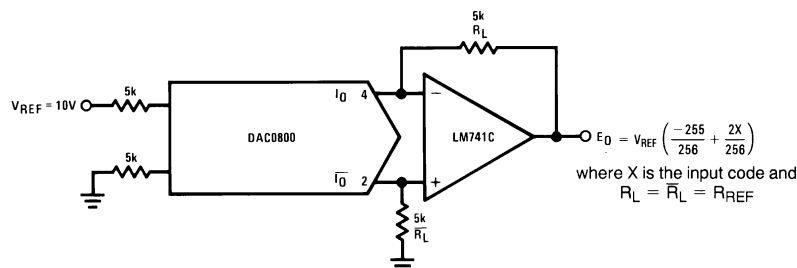


Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 22. Basic Bipolar Output Operation**

**Table 2. Basic Bipolar Output Operation**

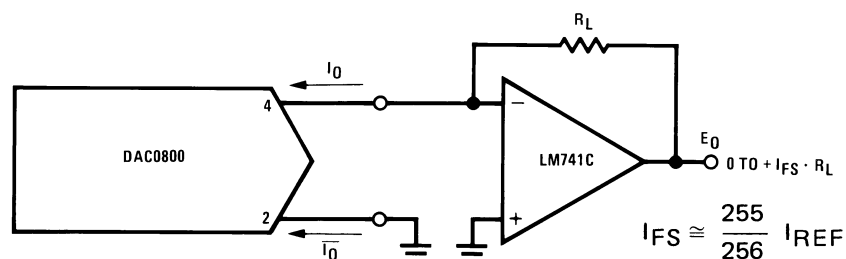
	B1	B2	B3	B4	B5	B6	B7	B8	$E_O$	$\bar{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale-LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920



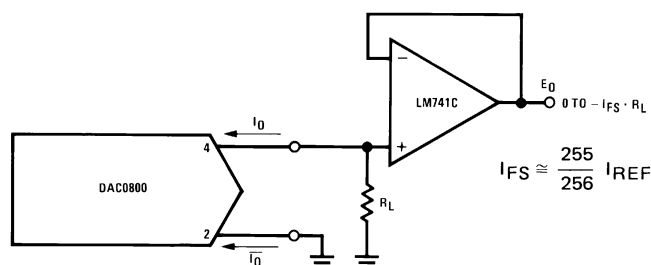
- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) If  $R_L = \bar{R}_L$  within  $\pm 0.05\%$ , output is symmetrical about ground.

**Figure 23. Symmetrical Offset Binary Operation****Table 3. Symmetrical Offset Binary Operation**

	B1	B2	B3	B4	B5	B6	B7	B8	EO
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(-)Zero Scale	0	1	1	1	1	1	1	1	-0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	-9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	-9.960

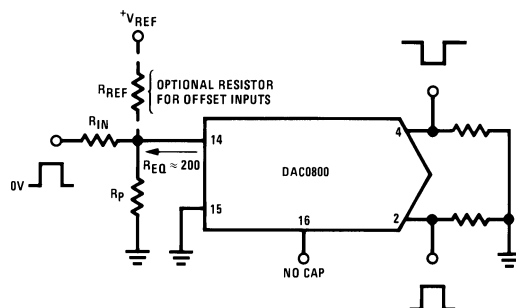


- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) For complementary output (operation as negative logic DAC), connect inverting input of op amp to  $\bar{I}_O$  (pin 2), connect  $I_O$  (pin 4) to ground.

**Figure 24. Positive Low Impedance Output Operation**

- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to  $\bar{I}_O$  (pin 2); connect  $I_O$  (pin 4) to ground.

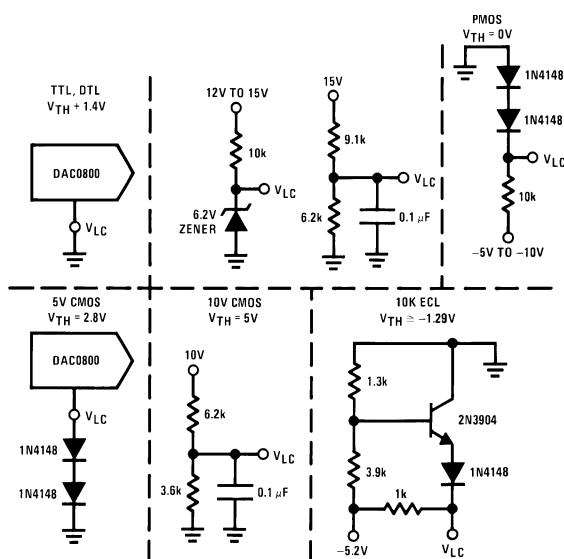
**Figure 25. Negative Low Impedance Output Operation**



Typical values:  $R_{IN}=5k, +V_{IN}=10V$

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

### Figure 26. Pulsed Reference Operation



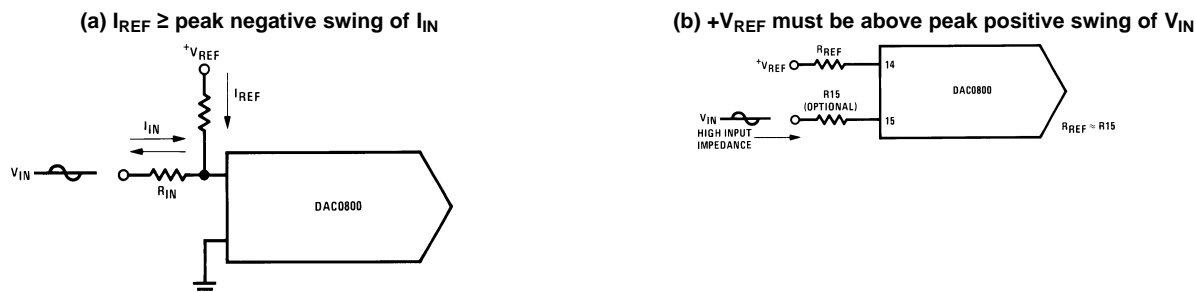
$$V_{TH} = V_{IC} + 1.4V$$

15V CMOS, HTL, HNIL

$$V_{TH} = 7.6V$$

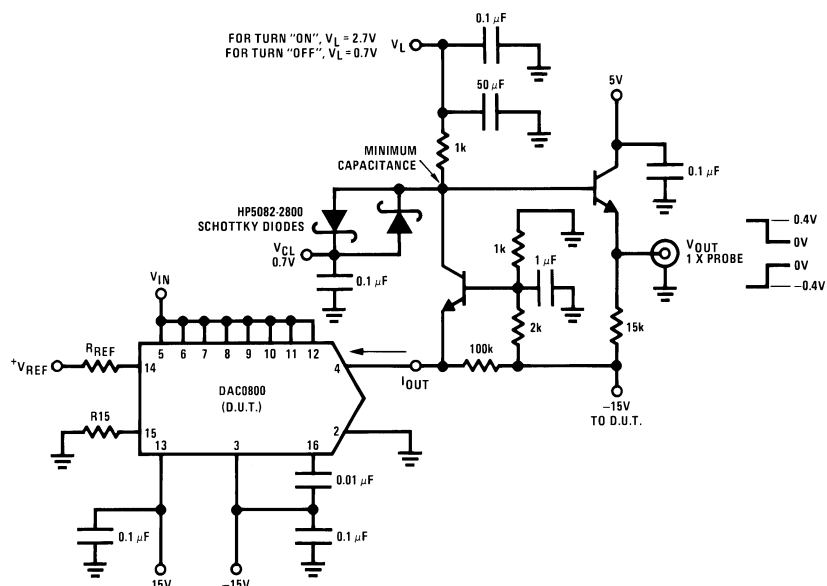
Note. Do not exceed negative logic input range of DAC.

### Figure 27. Interfacing with Various Logic Families



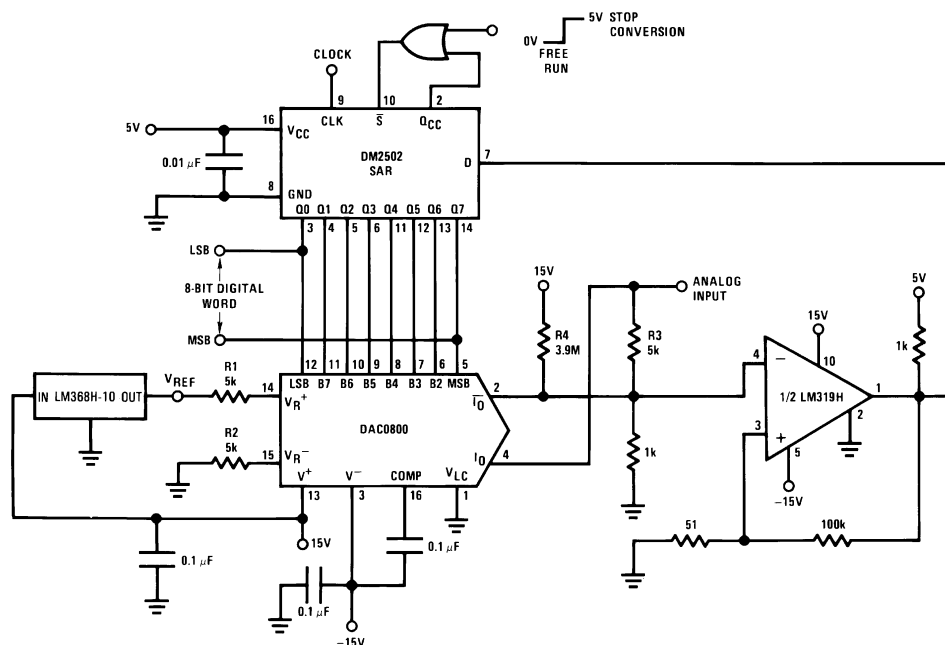
Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

### Figure 28. Accommodating Bipolar References



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 29. Settling Time Measurement**



- (1) For 1  $\mu s$  conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 k $\Omega$  and R4 to 2 M $\Omega$ .
- (2) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 30. A Complete 2  $\mu s$  Conversion Time, 8-Bit A/D Converter**

## REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
<ul style="list-style-type: none"><li>Changed layout of National Data Sheet to TI format .....</li></ul>	<a href="#">12</a>

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DAC0800LCM/NOPB</a>	Active	Production	SOIC (D)   16	48   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM
DAC0800LCM/NOPB.B	Active	Production	SOIC (D)   16	48   TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM
<a href="#">DAC0800LCMX/NOPB</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM
DAC0800LCMX/NOPB.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM
<a href="#">DAC0800LCN/NOPB</a>	Active	Production	PDIP (NFG)   16	25   TUBE	Yes	SN	Level-1-NA-UNLIM	0 to 70	DAC0800LCN DAC-08EP
DAC0800LCN/NOPB.B	Active	Production	PDIP (NFG)   16	25   TUBE	Yes	SN	Level-1-NA-UNLIM	0 to 70	DAC0800LCN DAC-08EP
<a href="#">DAC0802LCMX/NOPB</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0802LCM
DAC0802LCMX/NOPB.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	DAC0802LCM

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC0800LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0802LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC0800LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
DAC0802LCMX/NOPB	SOIC	D	16	2500	356.0	356.0	35.0

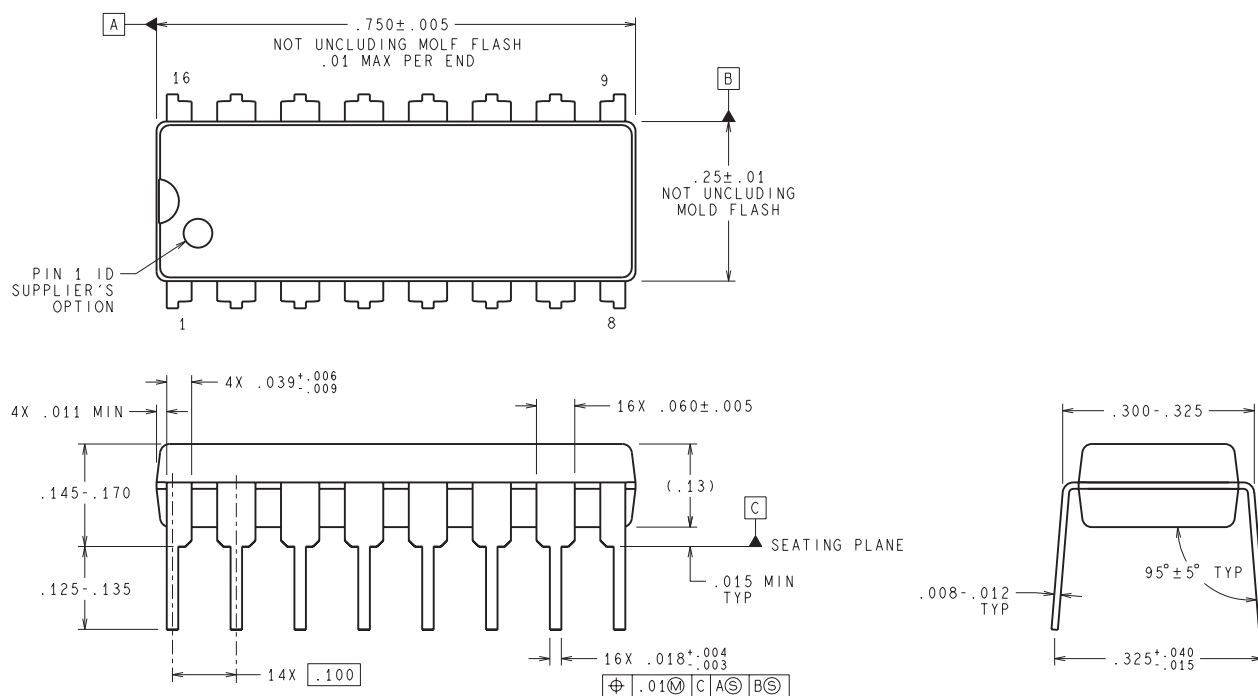
## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC0800LCM/NOPB	D	SOIC	16	48	495	8	4064	3.05
DAC0800LCM/NOPB.B	D	SOIC	16	48	495	8	4064	3.05
DAC0800LCN/NOPB	NFG	PDIP	16	25	502	14	11938	4.32
DAC0800LCN/NOPB.B	NFG	PDIP	16	25	502	14	11938	4.32

NFG0016E



**DIMENSIONS ARE IN INCHES**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated