DRV8802-Q1 Automotive DC Motor-Driver IC

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Dual H-Bridge Current-Control Motor Driver
  - Drives Two DC Motors
  - Brake Mode
  - Two-Bit Winding Current Control Allows Up to 4 Current Levels
  - Low MOSFET On-Resistance
- 1.6-A Maximum Drive Current at 24 V, 25°C
- Built-In 3.3-V Reference Output
- Industry Standard Parallel Digital Control Interface
- 8-V to 45-V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package

2 Applications

- Automotive HVAC
- Automotive Valves
- Automotive Infotainment

3 Description

The DRV8802-Q1 device provides an integrated motor driver solution for automotive applications. The device has two H-bridge drivers, and is intended to drive DC motors. The output driver block for each consists of N-channel power MOSFET's configured as H-bridges to drive the motor windings. The DRV8802-Q1 device can supply up to 1.6-A peak or 1.1-A RMS output current (with proper heatsinking at 24 V and 25°C) per H-bridge.

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable to allow braking or coasting of the motor when disabled.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

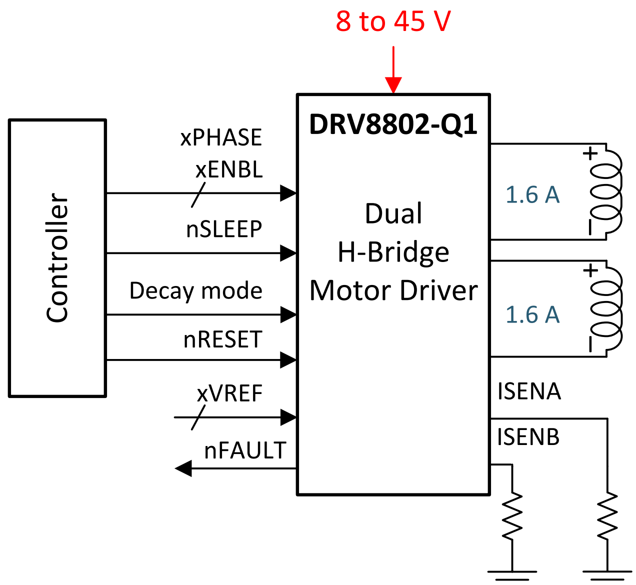
The DRV8802-Q1 device is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8802-Q1	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Diagram



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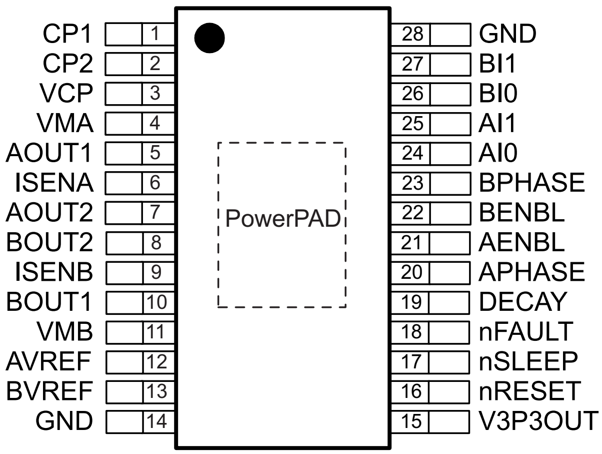
4 Revision History

DATE	REVISION	NOTES
June 2014	A	Initial release.

5 Pin Configuration and Functions

28-Pin HTSSOP With PowerPAD
PWP Package
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-μF 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
GND	14	—	Device ground	
	28			
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-μF 6.3-V ceramic capacitor. Can be used to supply VREF.
VMA	4	—	Bridge A power supply	Connect to motor supply (8 to 45 V). Both pins must be connected to same supply.
VMB	11	—	Bridge B power supply	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-μF 16-V ceramic capacitor and a 1-MΩ resistor to VMx.
CONTROL				
AI0	24	I	Bridge A current set	Sets bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0
AI1	25	I		
AENBL	21	I	Bridge A enable	Logic high to enable bridge A
APHASE	20	I	Bridge A phase (direction)	Logic high sets AOUT1 high, AOUT2 low
AVREF	12	I	Bridge A current set reference input	Reference voltage for winding current set. Can be driven individually with an external DAC for microstepping, or tied to a reference (for example, V3P3OUT).
BVREF	13	I	Bridge B current set reference input	
BI0	26	I	Bridge B current set	Sets bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0
BI1	27	I		
BENBL	22	I	Bridge B enable	Logic high to enable bridge B
BPHASE	23	I	Bridge B phase (direction)	Logic high sets BOUT1 high, BOUT2 low
DECAY	19	I	Decay (brake) mode	Low = brake (slow decay), high = coast (fast decay)
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode

(1) I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT				
AOUT1	5	O	Bridge A output 1	Connect to motor winding A
AOUT2	7	O	Bridge A output 2	
BOUT1	10	O	Bridge B output 1	Connect to motor winding B
BOUT2	8	O	Bridge B output 2	
ISENA	6	IO	Bridge A ground and current sense	Connect to current sense resistor for bridge A
ISENB	9	IO	Bridge B ground and current sense	Connect to current sense resistor for bridge B

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Power supply voltage	$V_{(VMx)}$		–0.3	47	V
Charge pump voltage	VCP, CP1, CP2		–0.3	$V_{(VMx)}$+7	V
Digital pin voltage	xPHASE, xENBL, nSLEEP, nFAULT, nRESET, xI0, xI1, DECAY		–0.5	7	V
Reference input voltage	$V_{(xVREF)}$		–0.3	4	V
Sense pin voltage	$V_{(ISENx)}$		–0.3	0.8	V
H-bridge output Current	xOUT1, xOUT2, ISENx	Peak motor drive, t < 1 μS	Internally limited		A
		Continuous motor drive(3)		1.6	A
Continuous total power dissipation			See the *Power Dissipation* section		
Operating virtual junction temperature, T_J			–40	150	°C
Operating ambient temperature, T_A			–40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–60	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 14, 15, and 28)	–750	750	
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{(VMx)}$	Power supply voltage(1)	8.2	45	V
$V_{(xVREF)}$	VREF input voltage(2)	1	3.5	V
$I_{(OUT1x, OUT2x)}$	H-Bridge Output Current		1.6	A
$I_{L(V3P3OUT)}$	V3P3OUT load current		1	mA

(1) All VMx pins must be connected to the same supply voltage.
(2) Operational at $V_{(xVREF)}$ between 0 V and 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC(1)		PWP 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	20.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temp range of -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
$I_{(VMx)}$	VMx operating supply current	$V_{(VMx)}$ = 24 V, $f_{(PWM)}$ < 50 kHz		5	8	mA
$I_{(VMx\_Q)}$	VMx sleep mode supply current	$V_{(VMx)}$ = 24 V		10	20	μA
$V_{(UVLO)}$	VMx undervoltage lockout voltage	$V_{(VMx)}$ rising		7.8	8.2	V
V3P3OUT REGULATOR						
$V_{(V3P3OUT)}$	V3P3OUT voltage	I_O = 0 to 1 mA	3.1	3.3	3.5	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.7	V
V_{IH}	Input high voltage		2.1			V
V_{hys}	Input hysteresis			0.45		V
I_{IL}	Input low current	V_I = 0	–20		20	μA
I_{IH}	Input high current	V_I = 3.3 V			100	μA
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	μA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay mode	0		0.8	V
V_{IH}	Input high threshold voltage	For fast decay mode	2			V
I_I	Input current				±40	μA
H-BRIDGE FETS						
$r_{DS(on)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.63		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.76	0.9	
		V_M = 24 V, I_O = 1 A, T_J = 125°C		0.85	1	
$r_{DS(on)}$	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.65		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.78	0.9	
		V_M = 24 V, I_O = 1 A, T_J = 125°C		0.85	1	
$I_{lkg(OFF)}$	Off-state leakage current		–20		20	μA
MOTOR DRIVER						
$f_{(PWM)}$	Internal PWM frequency			50		kHz
$t_{(blank)}$	Current-sense blanking time			3.75		μs
t_r	Rise time	V_M = 24 V	100		360	ns
t_f	Fall time	V_M = 24 V	80		250	ns
$t_{(dead)}$	Dead time			400		ns
PROTECTION CIRCUITS						
$I_{(OCP)}$	Overcurrent protection trip level		1.8		5	A
$T_{(SD)}$	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
$I_{(xVREF)}$	xVREF input current	$V_{(xVREF)}$ = 3.3 V	–3		3	μA
$V_{(TRIP)}$	xISENSE trip voltage	$V_{(xVREF)}$ = 3.3 V, 100% current setting	635	660	685	mV
		$V_{(xVREF)}$ = 3.3 V, 71% current setting	445	469	492	
		$V_{(xVREF)}$ = 3.3 V, 38% current setting	225	251	276	
$G_{(ISENx)}$	Current sense amplifier gain	Reference only		5		V/V

6.6 Typical Characteristics

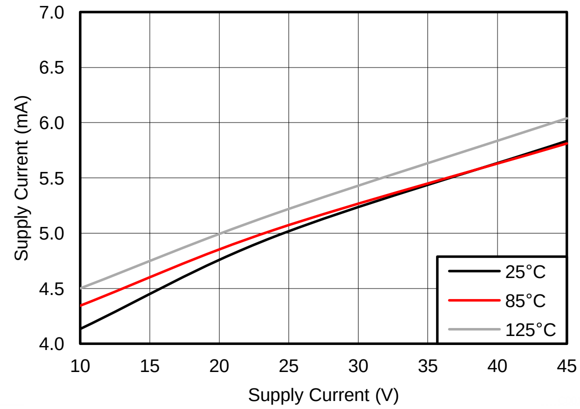


Figure 1. $I_{(VMx)}$ vs $V_{(VMx)}$

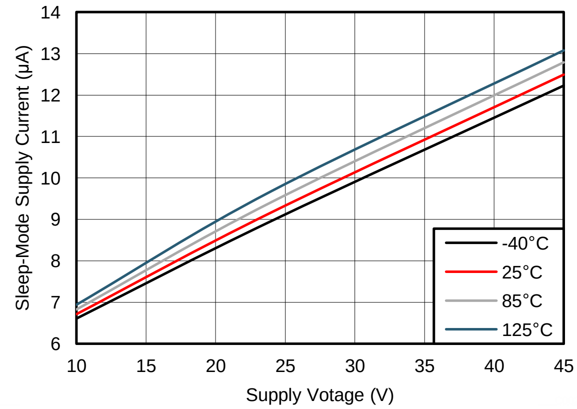


Figure 2. $I_{(VMx\_Q)}$ vs $V_{(VMx)}$

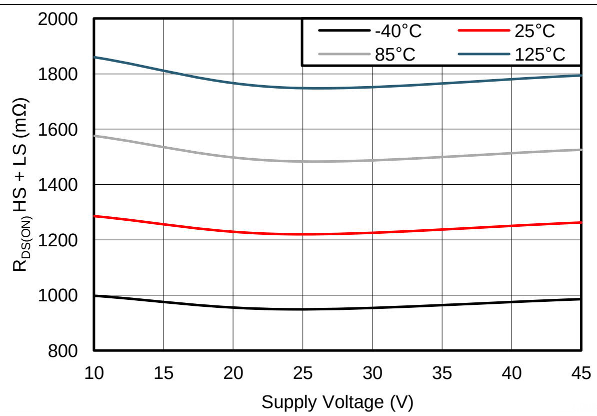


Figure 3. $r_{DS(on)}$ vs $V_{(VMx)}$

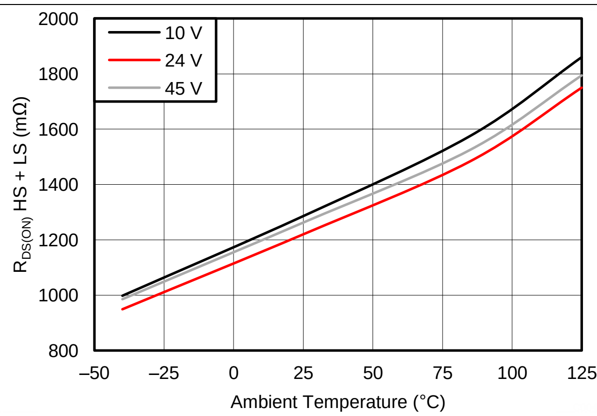


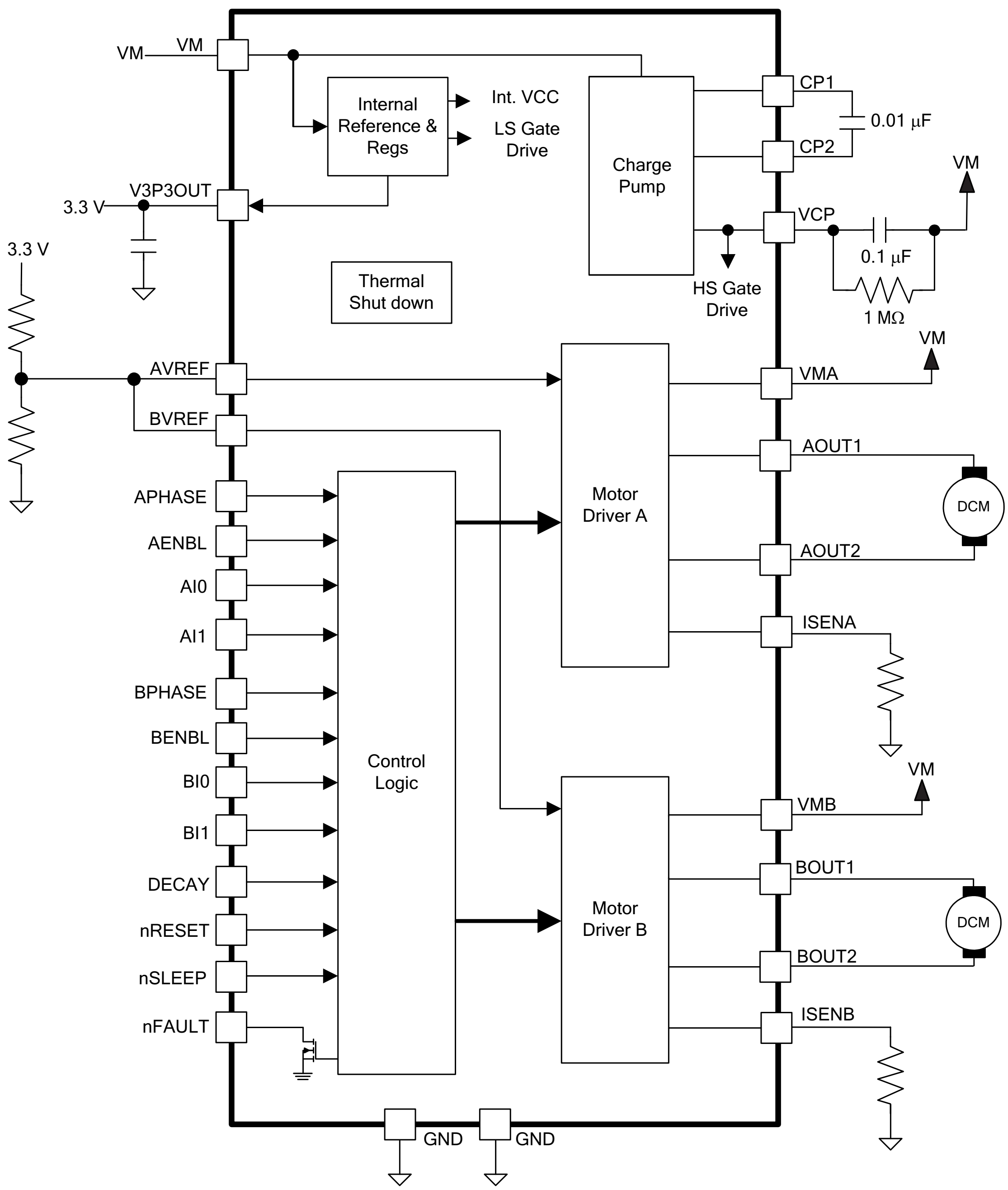
Figure 4. $r_{DS(on)}$ vs Temperature

7 Detailed Description

7.1 Overview

The DRV8802-Q1 device provides an integrated motor driver solution for automotive applications. The device has two H-bridge drivers, and is intended to drive DC motors. The output driver block for each consists of N-channel power MOSFET's configured as H-bridges to drive the motor windings. The DRV8802-Q1 device can supply up to 1.6-A peak or 1.1-A RMS output current (with proper heatsinking at 24 V and 25°C) per H-bridge. A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable to allow braking or coasting of the motor when disabled. Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8802-Q1 device contains two H-bridge motor drivers with current-control PWM circuitry. Figure 5 shows a block diagram of the motor control circuitry.

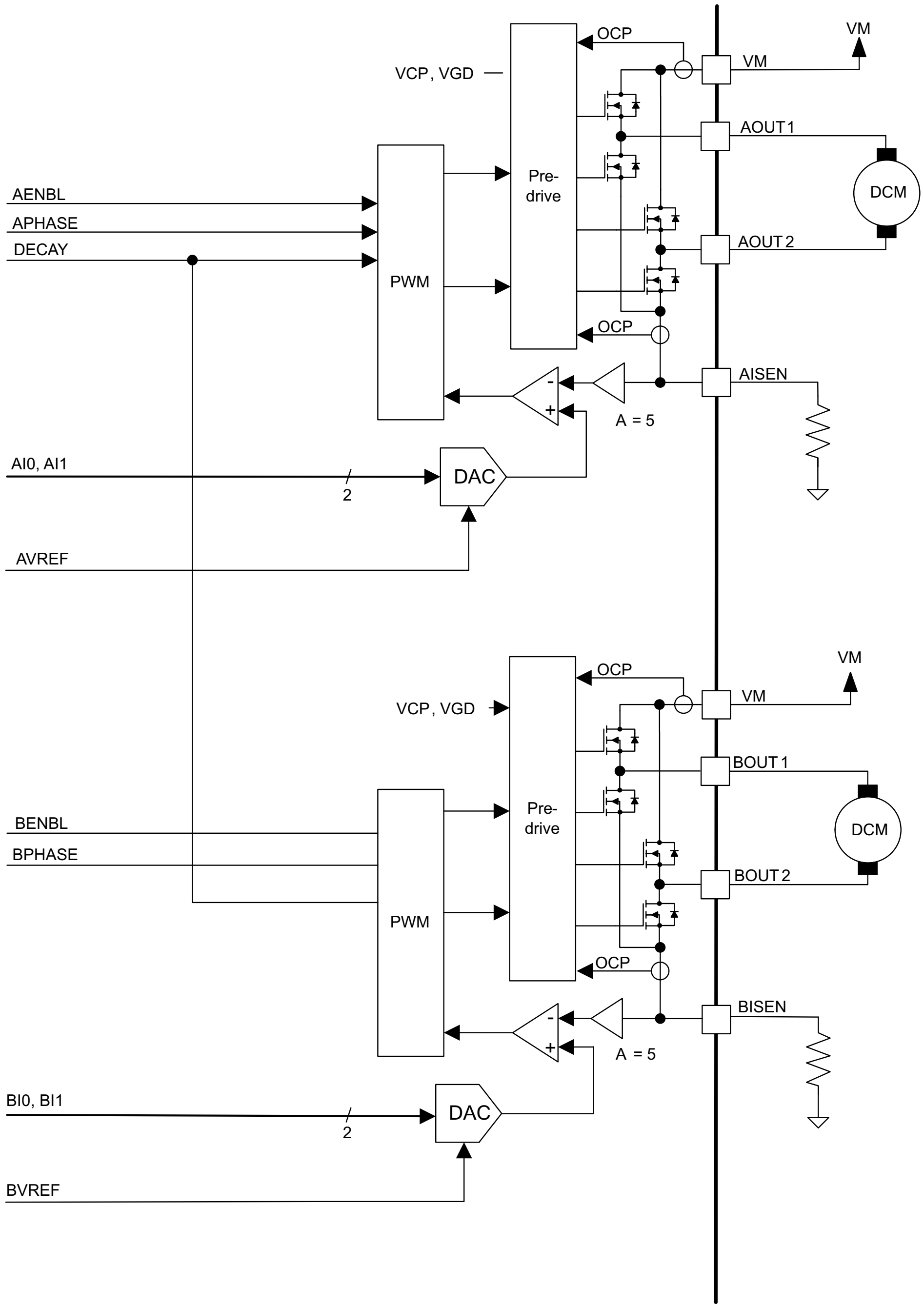


Figure 5. Motor Control Circuitry

Note that there are multiple VM pins (VMx). All VMx pins must be connected together to the motor supply voltage.

Feature Description (continued)

7.3.2 Bridge Control

The xPHASE input pins control the direction of current flow through each H-bridge, and therefore control the direction of rotation of a DC motor. The xENBL input pins enable the H-bridge outputs when active high, and can also be used for PWM speed control of the motor. Table 1 lists the H-bridge logic.

Table 1. H-Bridge Logic

xENBL	xPHASE	xOUT1	xOUT2
0	X	see (1)	see (1)
1	1	H	L
1	0	L	H

(1) Depends on state of the DECAY pin. See the *Decay Mode and Braking* section.

7.3.3 Current Regulation

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. When the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and can change the current that is used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

The PWM chopping current is set by a comparator that compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 2-bit DAC that allows current settings of 38%, 71%, and 100% of full-scale, plus zero.

Use Equation 1 to calculate the full-scale (100%) chopping current.

$$I_{(CHOP)} = \frac{V_{(xVREF)}}{5 \times R_{(ISENx)}} \tag{1}$$

For example:

If a 0.5-Ω sense resistor is used and the voltage on the xVREF pin is 3.3 V, the full-scale (100%) chopping current is 3.3 V / (5 × 0.5 Ω) = 1.32 A.

Two input pins per H-bridge (xI1 and xI0) are used to scale the current in each bridge as a percentage of the full-scale current set by the xVREF input pin and sense resistance. Table 2 lists the function of the pins.

Table 2. H-Bridge Pin Functions

xI1	xI0	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
1	1	0% (Bridge disabled)
1	0	38%
0	1	71%
0	0	100%

Note that when both xI bits are 1, the H-bridge is disabled and no current flows.

For example:

If a 0.5-Ω sense resistor is used and the voltage on the xVREF pin is 3.3 V, the chopping current is 1.32 A at the 100% setting (xI1, xI0 = 00). At the 71% setting (xI1, xI0 = 01) the current is 1.32 A × 0.71 = 0.937 A. At the 38% setting (xI1, xI0 = 10) the current is 1.32 A × 0.38 = 0.502 A. If (xI1, xI0 = 11) the bridge is disabled and no current will flow.

7.3.4 Decay Mode and Braking

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. See case 1 in Figure 6. The current-flow direction shown indicates the state when the xENBL pin is high.

When the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, when the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. See case 2 in Figure 6 for fast decay mode.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. See case 3 in Figure 6.

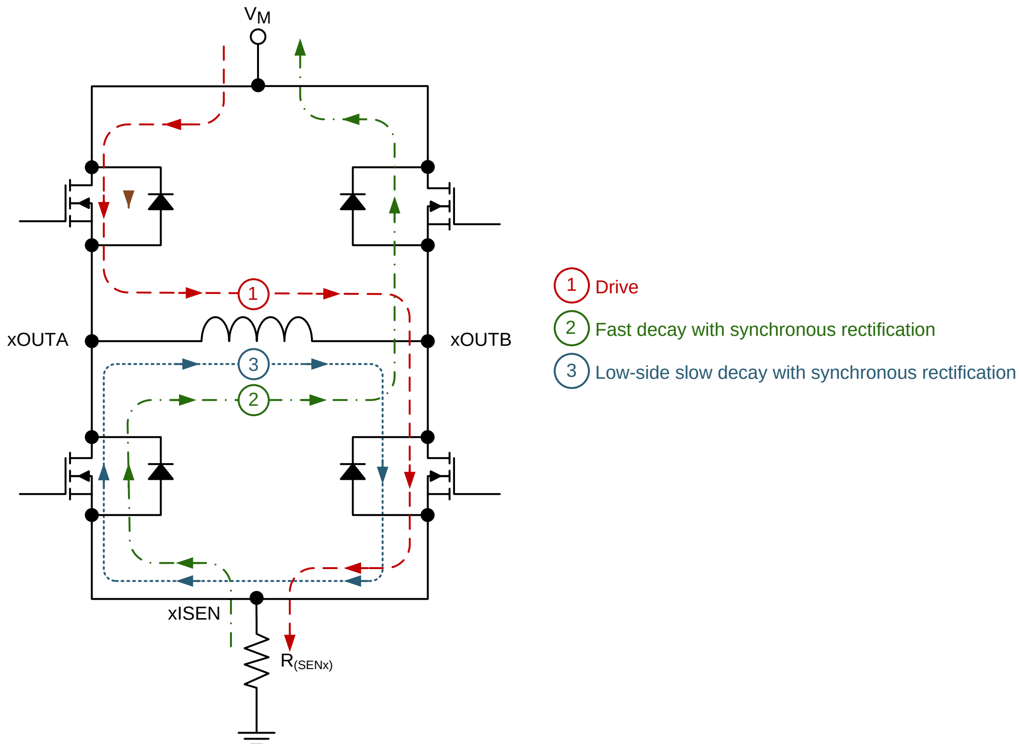


Figure 6. Decay Mode

The DRV8802-Q1 device supports fast decay and slow decay mode. Slow or fast decay mode is selected by the state of the DECAY pin. A logic low selects slow decay, and logic high sets fast decay mode. Note that the DECAY pin sets the decay mode for both H-bridges.

The DECAY mode also affects the operation of the bridge when it is disabled (by taking the ENBL pin inactive). This effect applies if the ENABLE input is being used for PWM speed control of the motor, or if it is simply being used to start and stop motor rotation.

If the DECAY pin is high (fast decay), when the bridge is disabled, all FETs are turned off and decay current flows through the body diodes, allowing the motor to coast to a stop.

If the DECAY pin is low (slow decay), both low-side FETs are turned on when the xENBL pin is made inactive. When the xENBL pin is made inactive, the inactivation essentially shorts out the back EMF of the motor, causing the motor to brake, and stop quickly. The low-side FETs stays in the ON state even after the current reaches zero.

7.3.5 Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on time of the PWM.

7.3.6 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. This pin also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low puts the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) must pass before the motor driver becomes fully operational.

7.3.7 Protection Circuits

The DRV8802-Q1 device is fully protected against undervoltage, overcurrent, and overtemperature events.

FAULT	ERROR REPORT	H-BRIDGE	CHARGE PUMP	RECOVERY
$V_{(VMx)}$ undervoltage (UVLO)	No error report – nFAULT is hi-Z	Disabled	Shut Down	$V_{(VMx)}$ > VUVLO RISING
Overcurrent (OCP)	nFAULT pulled low	Disabled	Operating	Retry time, $t_{(OCP)}$
Overtemperature Shutdown (OTS)	nFAULT remains pulled low (set during OTW)	Disabled	Shut Down	$T_J < T_{(OTS)} – T_{hys(OTS)}$

7.3.7.1 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current-limit persists for longer than the OCP time, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until either nRESET pin is applied, or $V_{(VMx)}$ is removed and re-applied.

Overcurrent conditions on both high-side and low-side devices (such as a short to ground, supply, or across the motor winding) result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control and is independent of the $R_{(ISENx)}$ resistor value or xVREF voltage.

7.3.7.2 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown temperature limit, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. When the die temperature has fallen below the temperature hsyteresis level, operation resumes automatically.

7.3.7.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VMx pins falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic resets. Operation resumes when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

The DRV8802-Q1 device is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the V3P3OUT regulator is disabled, and the H-bridge FETs are disabled hi-Z. The DRV8802-Q1 is brought out of sleep mode when nSLEEP is brought logic high.

8 Application and Implementation

8.1 Application Information

The DRV8802-Q1 device is used in medium voltage brushed-DC motor control applications.

8.2 Typical Application

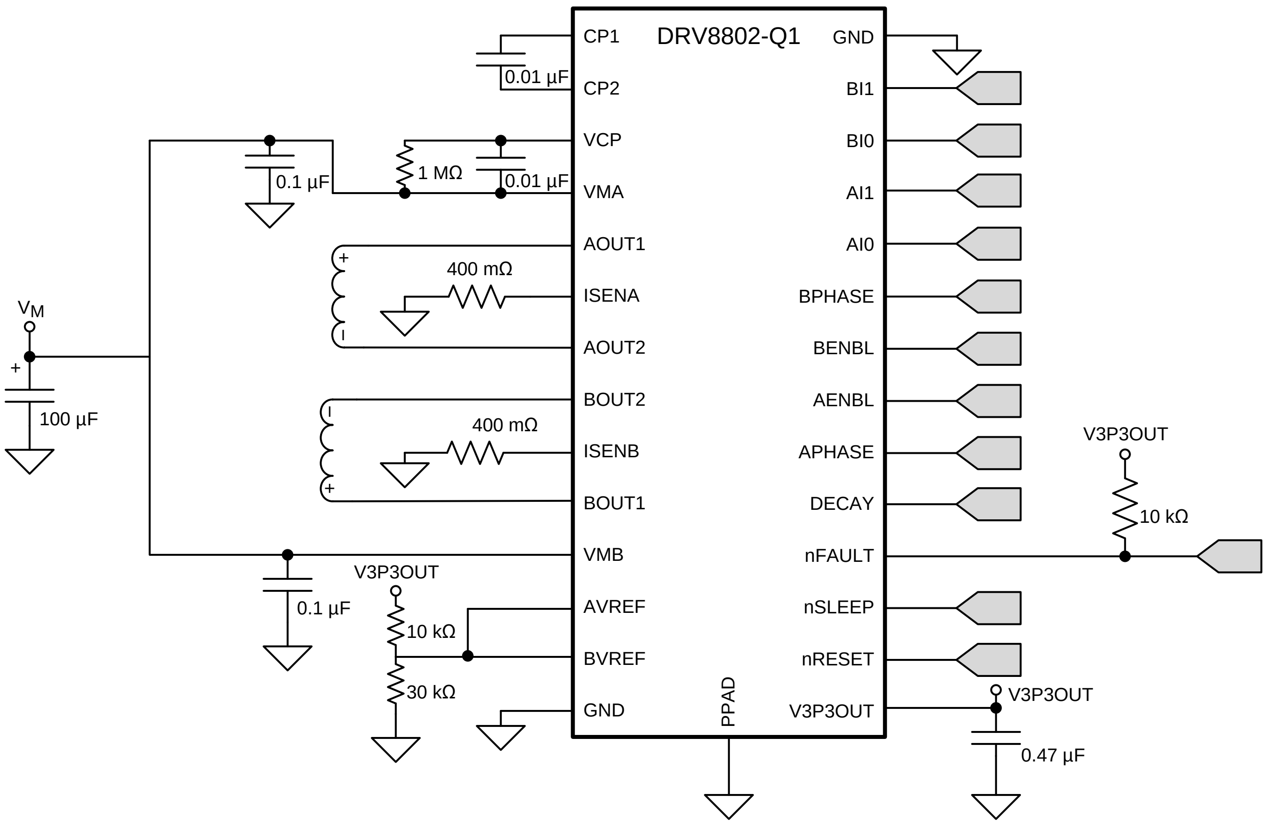


Figure 7. Typical Application Diagram

8.2.1 Design Requirements

The example supply for this design is $V_{(VMx)}$ = 18 V.

8.2.2 Detailed Design Procedure

8.2.2.1 Drive Current

The current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS power driver. Power dissipation I^2R losses in one source and sink DMOS driver are shown in Equation 2.

$$P_D = I^2(r_{DS(on)Source} + r_{DS(on)Sink}) \tag{2}$$

8.2.2.2 Slow-Decay SR (Brake Mode)

In slow-decay mode, both low-side sinking drivers turn on, allowing the current to circulate through the low side of the H-bridge (two sink drivers) and the load. Power dissipation I^2R loses in the two sink DMOS drivers as shown in Equation 3.

$$P_D = I^2(2 \times r_{DS(on)Sink}) \tag{3}$$

Typical Application (continued)

8.2.3 Application Curves

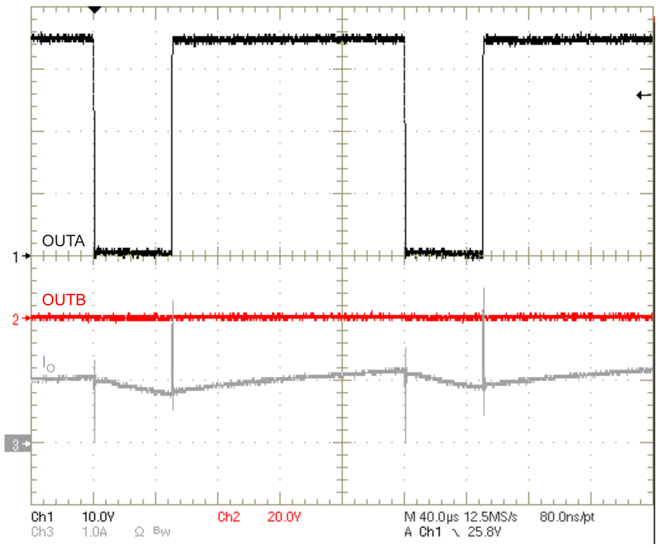


Figure 8. 75% Drive, 25% Slow Decay; $f_{(PWM)}$ = 5 kHz

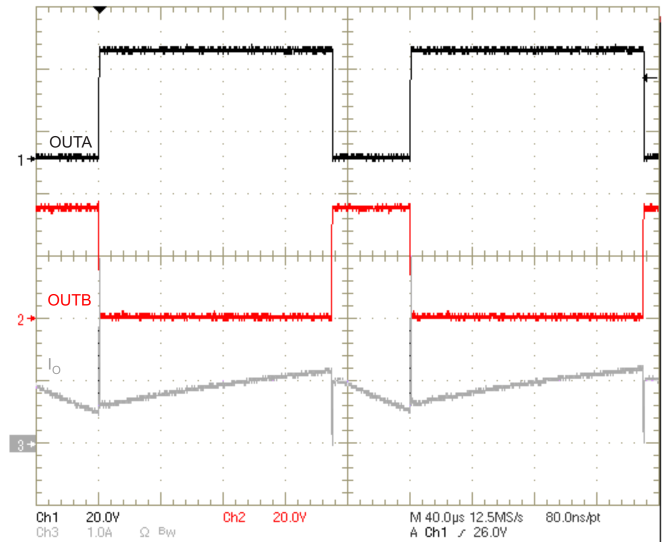


Figure 9. 75% Drive, 25% Fast Decay; $f_{(PWM)}$ = 5 kHz

9 Power Supply Recommendations

The DRV8802-Q1 is designed to operate from an input voltage supply $V_{(VMx)}$ range between 8.2 and 45 V. Two 0.1-µF ceramic capacitors rated for $V_{(VMx)}$ must be placed as close as possible to the VMA and VMB pins respectively (one on each pin). In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (Brushed DC, Brushless DC, Stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. You should size the bulk capacitance to meet acceptable voltage ripple levels. The datasheet generally provides a recommended value but system level testing is required to determine the appropriate sized bulk capacitor.

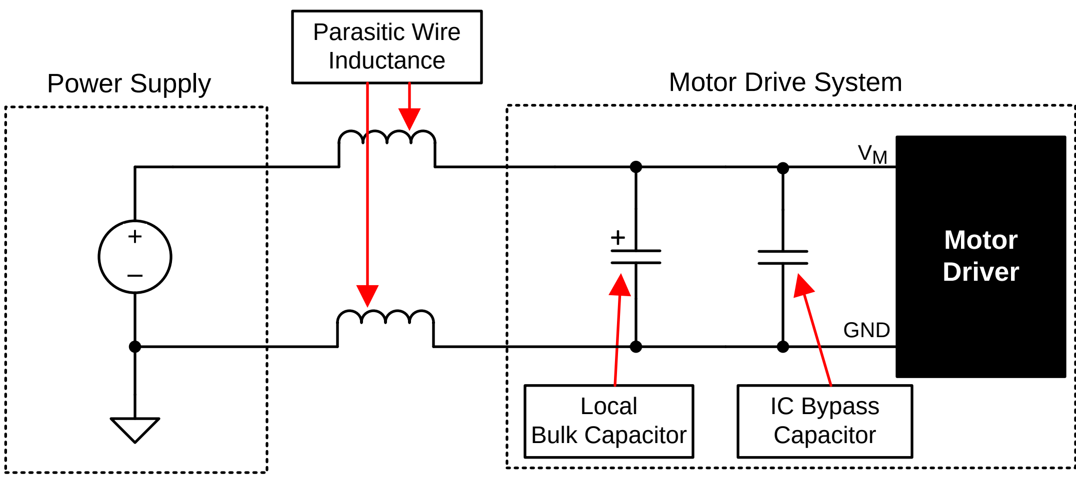


Figure 10. Example Setup of Motor Drive System WIth External Power Supply

9.2 Power Supply and Logic Sequencing

No specific sequence exists for powering-up the DRV8802-Q1 device. Digital input signals can be present before $V_{(VMx)}$ is applied. After $V_{(VMx)}$ is applied to the DRV8802-Q1 device, it begins operation based on the status of the control pins.

10 Layout

10.1 Layout Guidelines

The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VM. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin. The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8802-Q1. A low-ESR ceramic capacitor must be placed in between the CPL and

Layout Guidelines (continued)

CPH pins. TI recommends a value of 0.01-µF rated for VM. Place this component as close to the pins as possible. A low-ESR ceramic capacitor must be placed in between the VMA and VCP pins. TI recommends a value of 0.1-µF rated for 16 V. Place this component as close to the pins as possible. Also, place a 1-MΩ resistor between VCP and VMA. Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible.

10.2 Layout Example

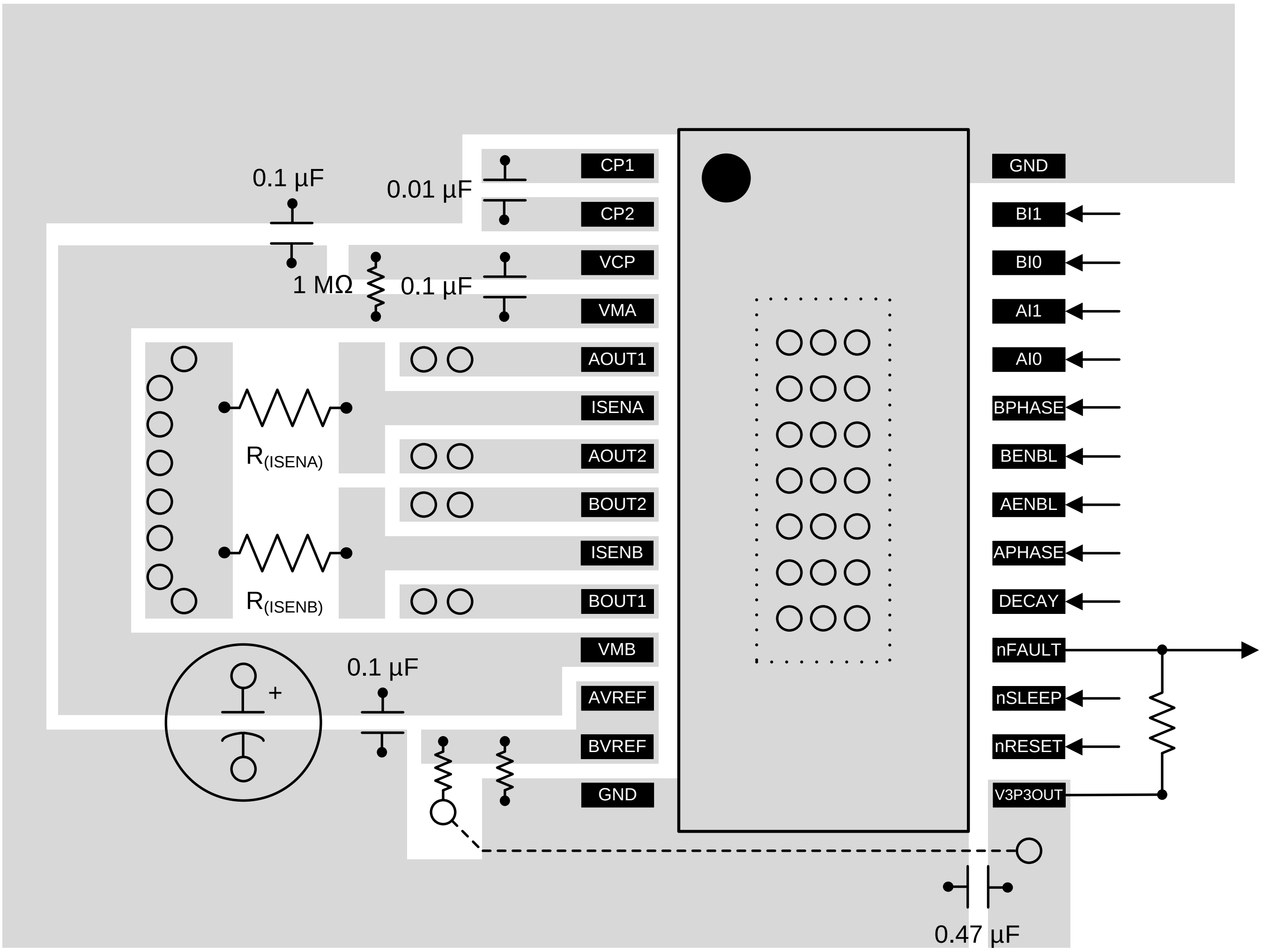


Figure 11. DRV8802-Q1 Layout Example

10.3 Thermal Information

10.3.1 Thermal Protection

The DRV8802-Q1 device has thermal shutdown (TSD) as described in the *Thermal Shutdown (TSD)* section. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops below the hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Thermal Information (continued)

10.3.2 Power Dissipation

Power dissipation in the DRV8802-Q1 device is dominated by the power dissipated in the output FET resistance, or $r_{DS(on)}$. Use Equation 4 to calculate the estimated average power dissipation of each H-bridge when running a DC motor.

$$P_D = 2 \times r_{DS(on)} \times I_O^2$$

where

- P_D is the power dissipation of one H-bridge
- $r_{DS(on)}$ is the resistance of each FET
- I_O is the RMS output current being applied to each winding (4)

I_O is equal to the average current drawn by the DC motor. Note that at startup and fault conditions this current is much higher than normal running current; these peak currents and the current duration must also be considered. The factor of 2 exists because at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation is the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

$r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

10.3.3 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to the TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002), "" and the TI application brief, *PowerPAD Made Easy™* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

11 Device and Documentation Support

11.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8802QPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8802Q1
DRV8802QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8802Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

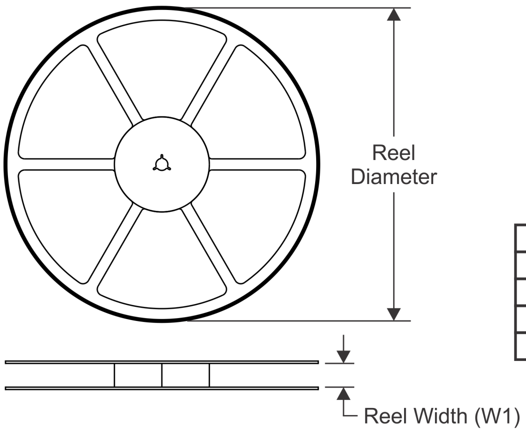
OTHER QUALIFIED VERSIONS OF DRV8802-Q1 :

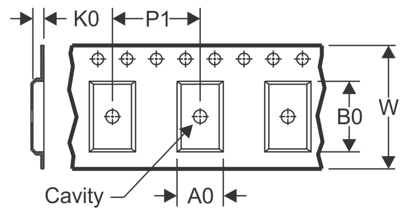
- Catalog : DRV8802

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

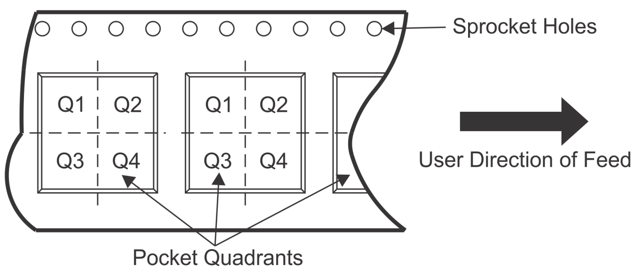
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

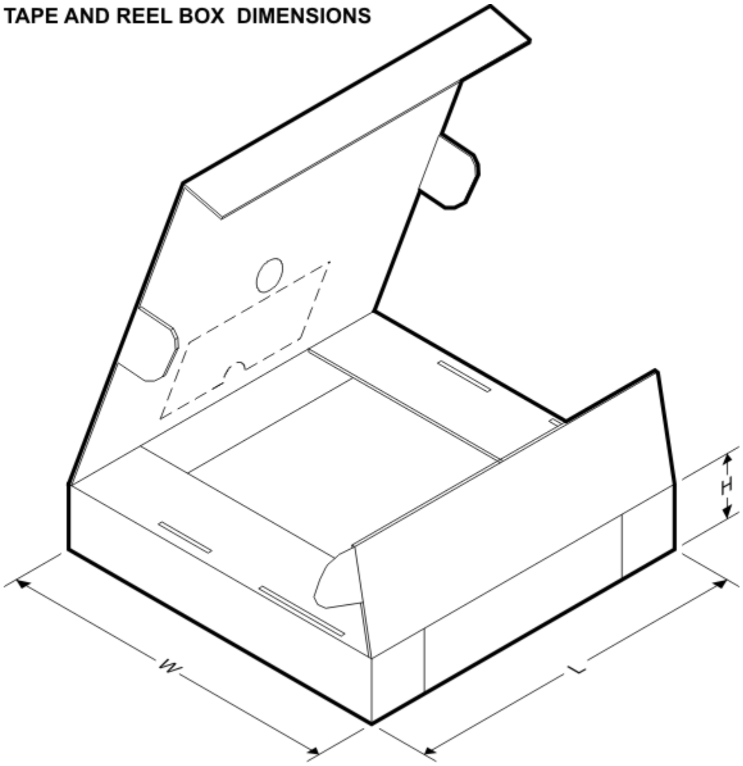
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8802QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

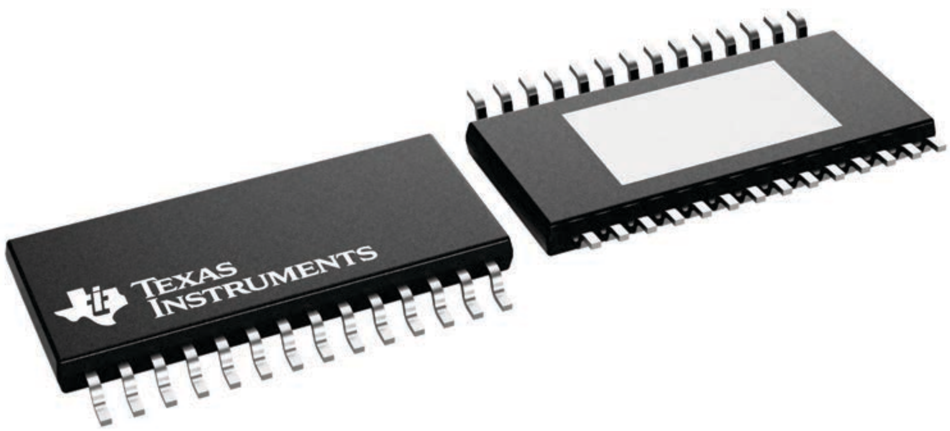
TAPE AND REEL BOX DIMENSIONS

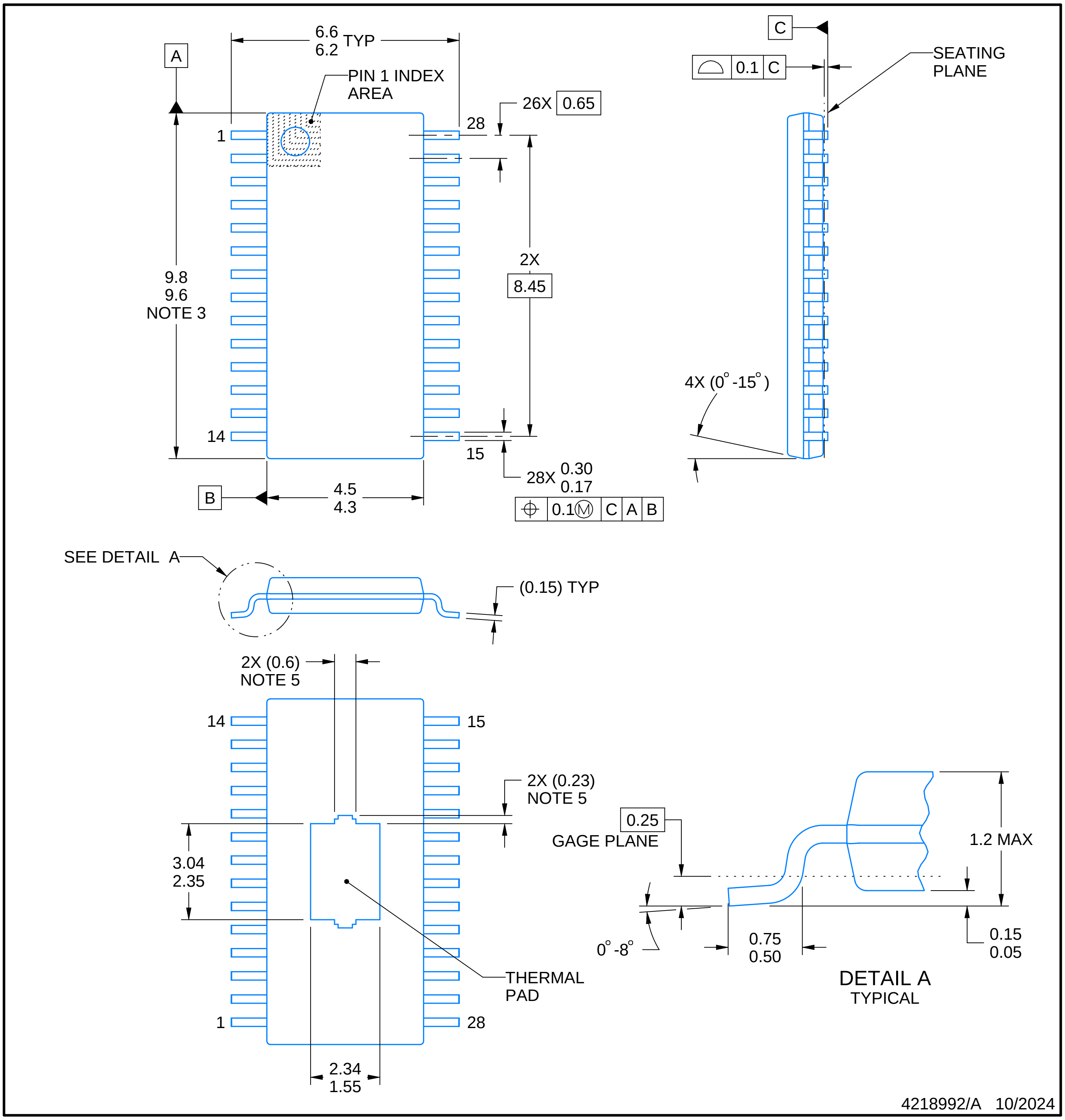


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8802QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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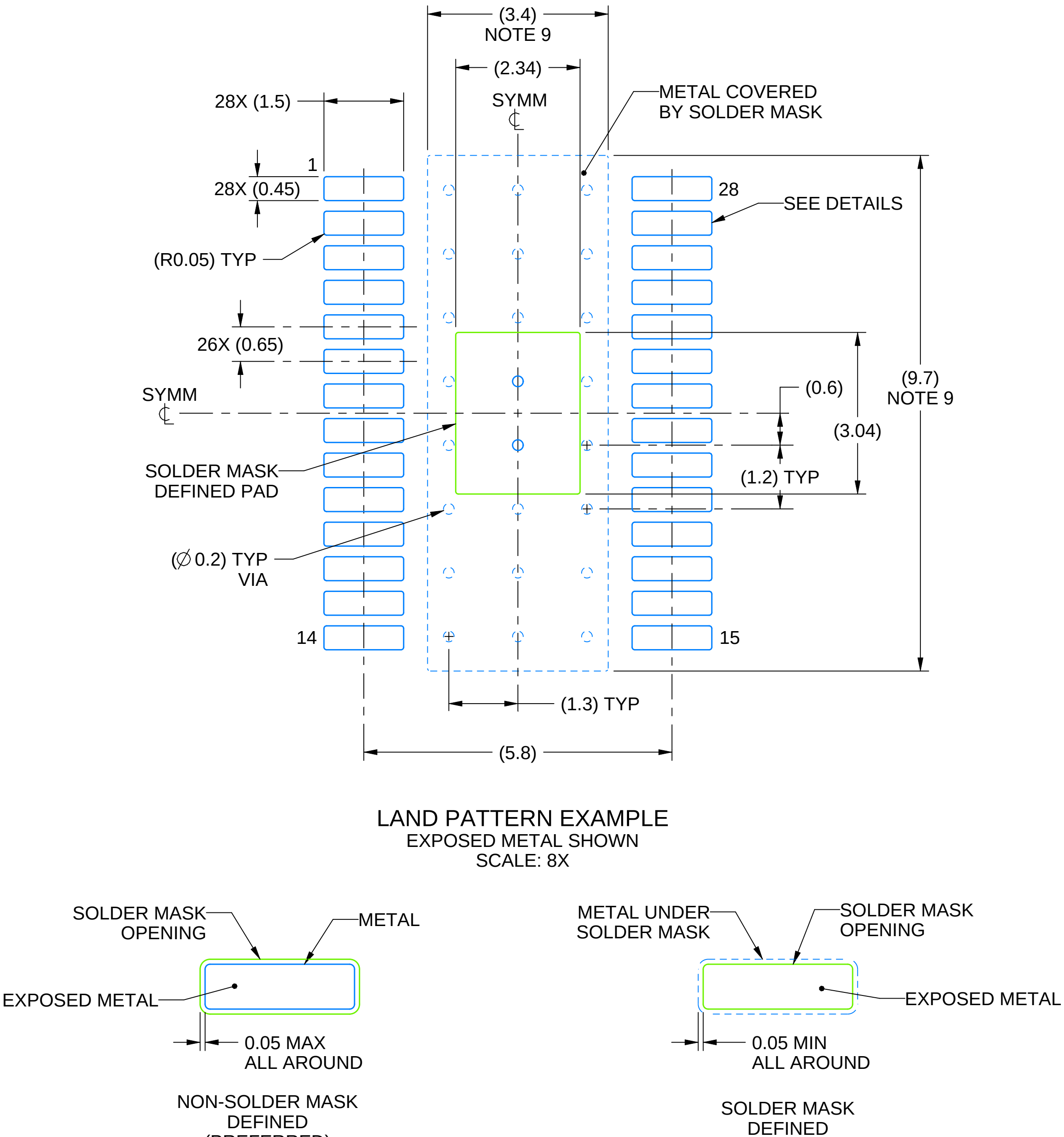
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

SOLDER MASK DETAILS

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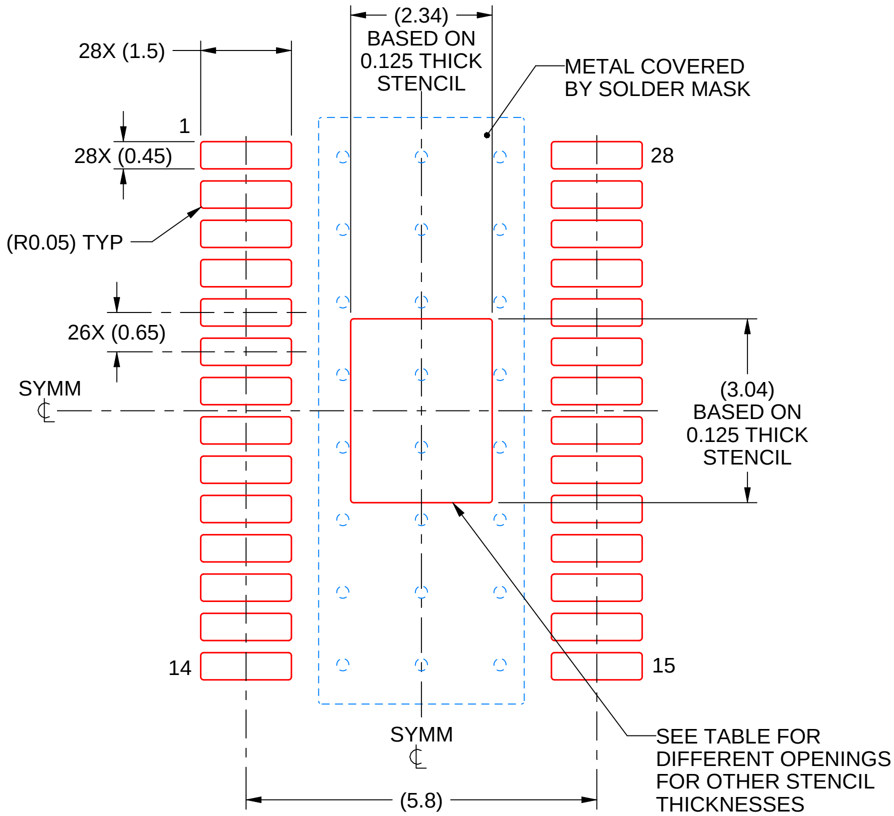
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.