RC4580 Dual Audio Operational Amplifier

1 Features

- Operating voltage: ±2V to ±18V
- Low noise voltage: 0.8μVrms
- Gain bandwidth product: 12MHz
- Total harmonic distortion: 0.0005%
- Slew rate: 5V/μs
- Drop-in replacement for NJM4580
- Pin and function compatible with LM833, NE5532, NJM4558/9, and NJM4560/2/5 devices

2 Applications

- Audio Preamplifiers
- Active Filters
- Headphone Amplifiers
- Industrial Measurement Equipment

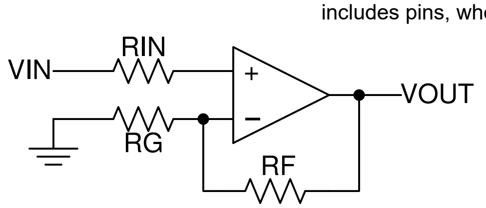
3 Description

The RC4580 device is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. The device offers low noise, high gain bandwidth, low harmonic distortion, and high output current designed for audio electronics, such as preamplifiers, active filters, and industrial measurement equipment. When high output current is required, the RC4580 device can be used as a headphone amplifier. Due to the wide operating supply voltage of the device, the RC4580 device can also be used in low-voltage applications.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE(2)
RC4580	D (SOIC, 8)	3.9mm × 4.9mm
	P (PDIP, 8)	9.81mm × 9.43mm
	PW (TSSOP, 8)	3.0mm × 4.4mm
	DGK (VSSOP, 8)	3.0mm × 3.0mm
	DDF (SOT-23, 8)	1.6mm × 2.9mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Noninverting Amplifier Schematic

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4 Pin Configuration and Functions

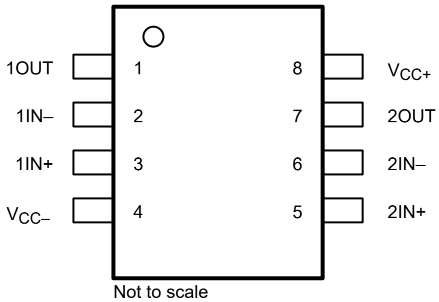


Figure 4-1. D, PW, and DGK Packages 8-Pin SOIC, TSSOP, and VSSOP (Top View)

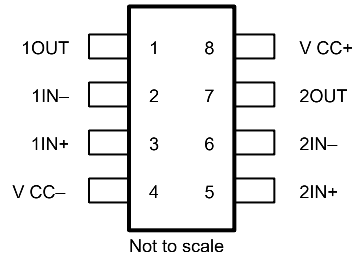


Figure 4-2. DDF Package 8-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN–	2	I	Inverting input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN–	6	I	Inverting input
2OUT	7	O	Output
V_{CC+}	8	—	Positive supply
$V_{CC–}$	4	—	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage		±18	V
V_I	Input voltage (any input)		±15	V
V_{ID}	Differential input voltage		±30	V
I_O	Output current		±50	mA
T_A	Ambient temperature range	–40	125	°C
T_{stg}	Storage temperature range	–60	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	0	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	0	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
V_{CC-}		–2	–16	
V_{ICR}	Input common-mode voltage range	–13.5	13.5	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		RC4580					UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109	99.2	163	160.5	177.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.7	78.8	38	70.2	96.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	49	61.9	90.6	95.6	95.2	
Ψ_{JT}	Junction-to-top characterization parameter	10.6	44.8	1.3	8.8	9.5	
Ψ_{JB}	Junction-to-board characterization parameter	48.6	61.2	88.9	94.0	95.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

$V_{CC\pm}$ = ±15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = < 10kΩ		0.5	3	mV
I_{IO}	Input offset current			5	200	nA
I_{IB}	Input bias current			100	500	nA
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ, V_O = ±10V	90	110		dB
V_{CM}	Output voltage swing	R_L ≥ 2kΩ	±12	±13.5		V
V_{ICR}	Common-mode input voltage		±12	±13.5		V
CMRR	Common-mode rejection ratio	R_S ≤ 10kΩ	80	110		dB
k_{SVR}	Supply-voltage rejection ratio[(1)]	R_S ≤ 10kΩ	80	110		dB
I_{CC}	Total supply current (all amplifiers)			6	9	mA

(1) Measured with $V_{CC\pm}$ varied simultaneously

5.6 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	R_L ≥ 2kΩ	5	V/µs
GBW	Gain-bandwidth product	f = 10kHz	12	MHz
THD	Total harmonic distortion	V_O = 5V, R_L = 2kΩ, f = 1kHz, A_{VD} = 20dB	0.0005%	
V_n	Equivalent input noise voltage	RIAA, R_S ≤ 2.2kΩ, 30kHz LPF	0.8	µVrms

5.7 Typical Characteristics

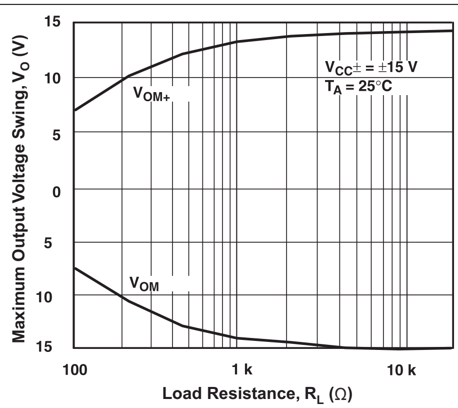


Figure 5-1. Maximum Output Voltage Swing vs Load Resistance

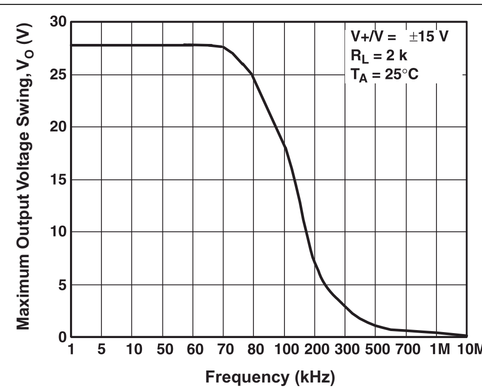


Figure 5-2. Maximum Ouput Voltage Swing vs Frequency

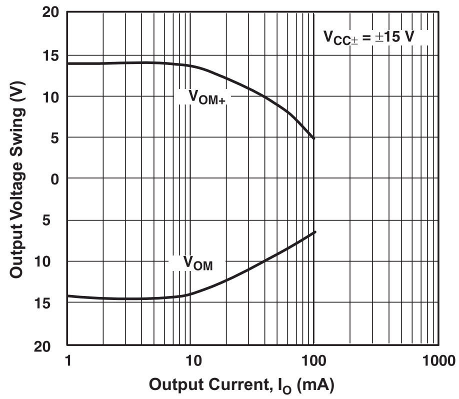


Figure 5-3. Output Voltage Swing vs Output Current

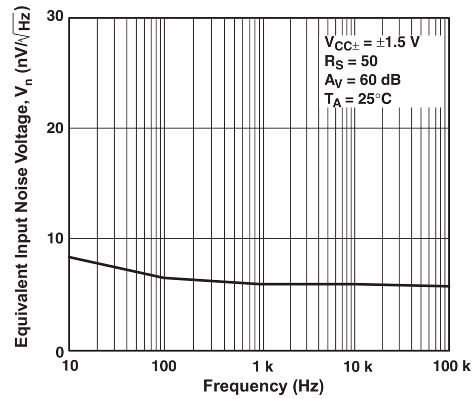


Figure 5-4. Equivalent Input Noise Voltage vs Frequency

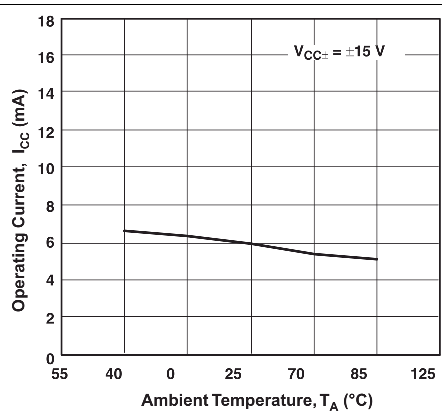


Figure 5-5. Operating Current vs Temperature

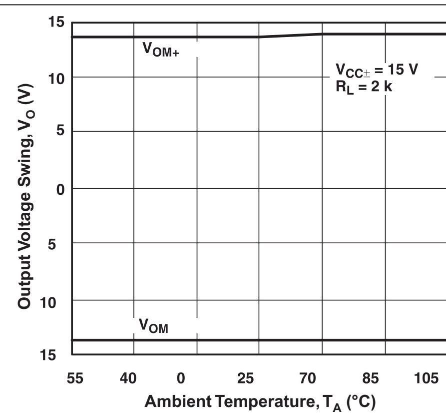


Figure 5-6. Output Voltage Swing vs Temperature

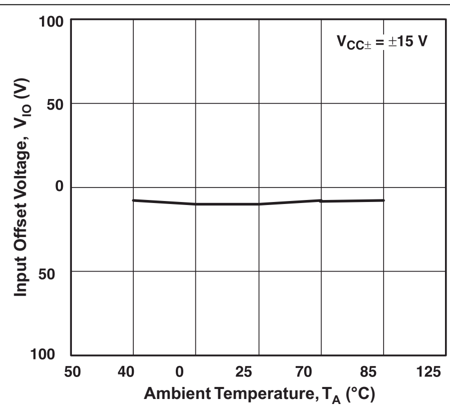


Figure 5-7. Input Offset Voltage vs Temperature

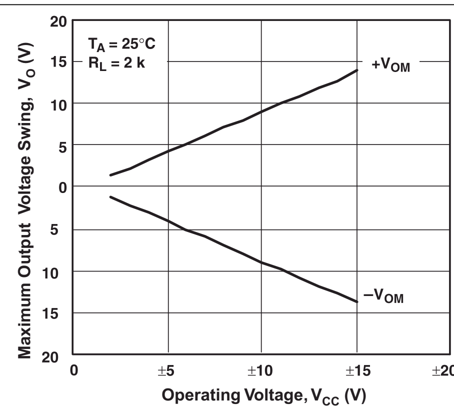


Figure 5-8. Input Bias Current vs Temperature

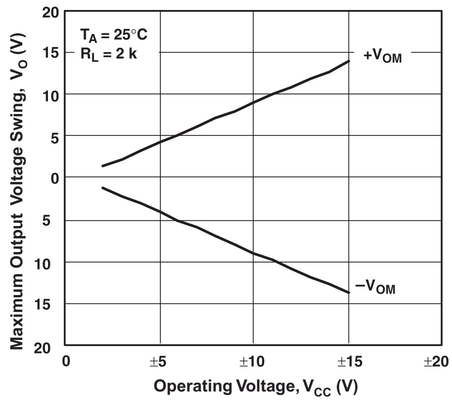


Figure 5-9. Maximum Output Voltage Swing vs Operating Voltage

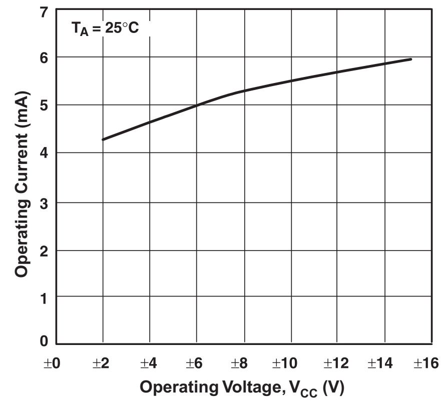


Figure 5-10. Operating Current vs Operating Voltage

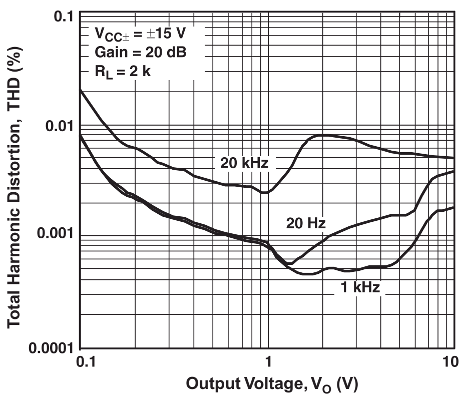


Figure 5-11. Total Harmonic Distortion vs Output Voltage

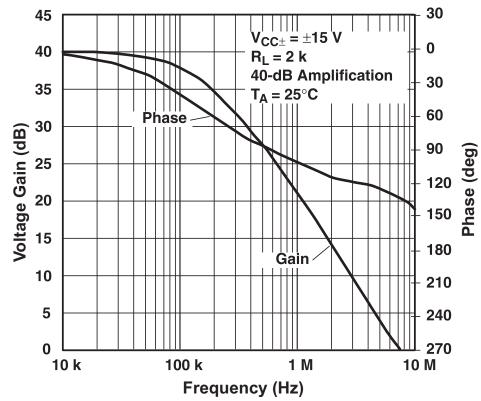


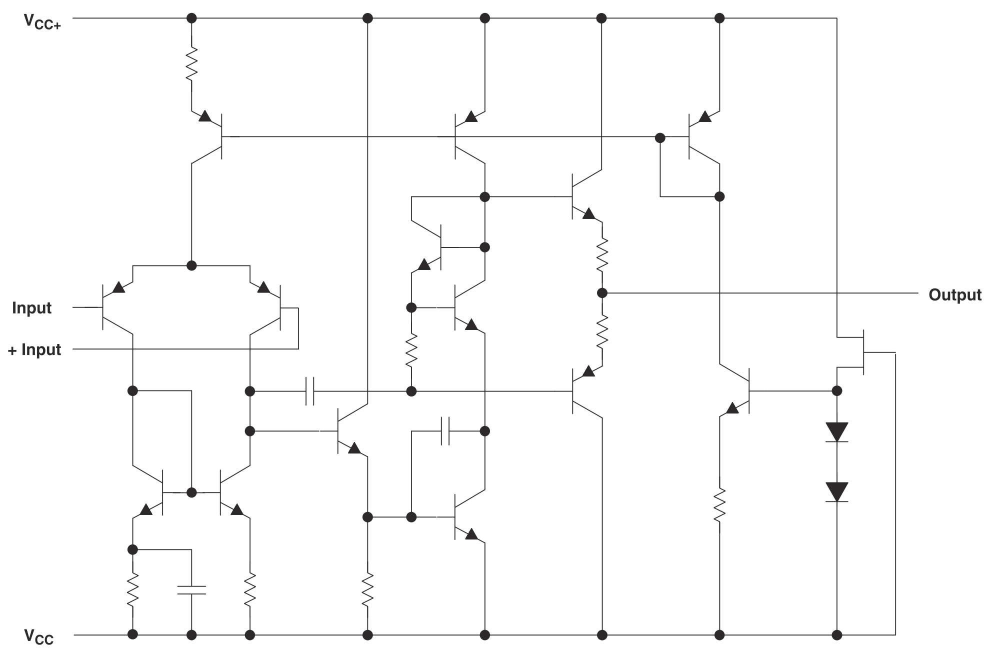
Figure 5-12. Voltage Gain, Phase vs Frequency

6 Detailed Description

6.1 Overview

The RC4580 device is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. The device offers low noise, high gain bandwidth, low harmonic distortion, and high output current. When high output current is required, the RC4580 device can be used as a headphone amplifier. Due to the wide operating supply voltage of the device, the RC4580 device can also be used in low-voltage applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The RC4580 device has a 12MHz unity-gain bandwidth.

6.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. The CMRR is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have the CMRR as high as possible. The CMRR of the RC4580 device is 110dB.

6.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change the op amp output when there is a change on the input. The RC4580 device has a 5V/µs slew rate.

6.4 Device Functional Mode

The RC4580 device is powered on when the supply is connected. Each device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

Some applications require differential signals. Figure 7-1 shows a simple circuit to convert a single-ended input of 2V to 10V into differential output of ±8V on a single 15V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-}. Both V_{OUT+} and V_{OUT-} range from 2V to 10V. The difference, V_{DIFF}, is the difference between V_{OUT+} and V_{OUT-}.

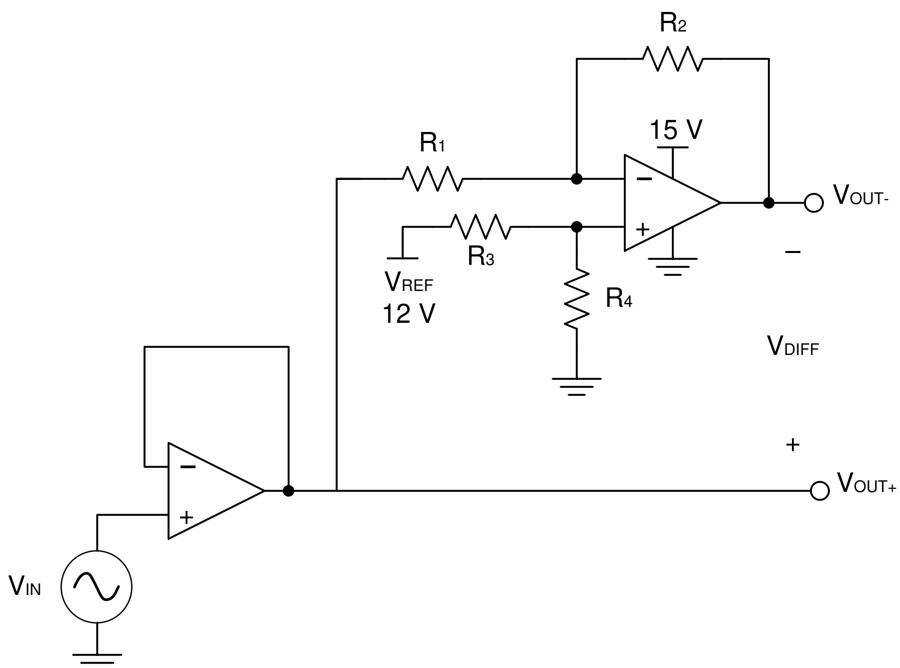


Figure 7-1. Schematic for Single-Ended Input to Differential Output Conversion

7.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15V
- Reference voltage: 12V
- Input: 2V to 10V
- Output differential: ±8V

7.1.2 Detailed Design Procedure

The circuit in Figure 7-1 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see Equation 1). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2{\times}V_{REF}$. Furthermore, the common-mode voltage is one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

7.1.2.1 Amplifier Selection

Linearity over the input range is key for good DC accuracy. The common-mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. The RC4580 device has a bandwidth of 12MHz, therefore this circuit is only be able to process signals with frequencies of less than 12MHz.

7.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

7.1.3 Application Curves

The measured transfer functions in Figure 7-2, Figure 7-3, and Figure 7-4 were generated by sweeping the input voltage from 0V to 12V. However, this design should only be used between 2V and 10V for optimum linearity.

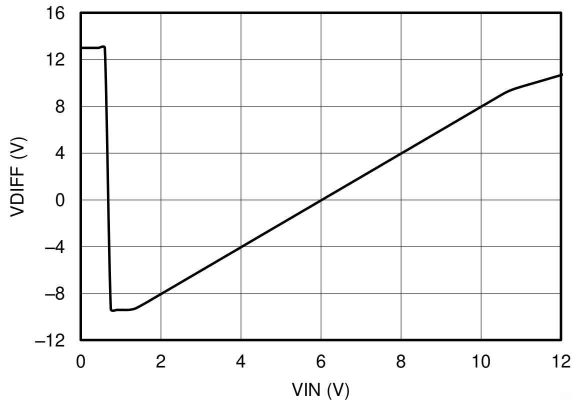


Figure 7-2. Differential Output Voltage vs Input Voltage

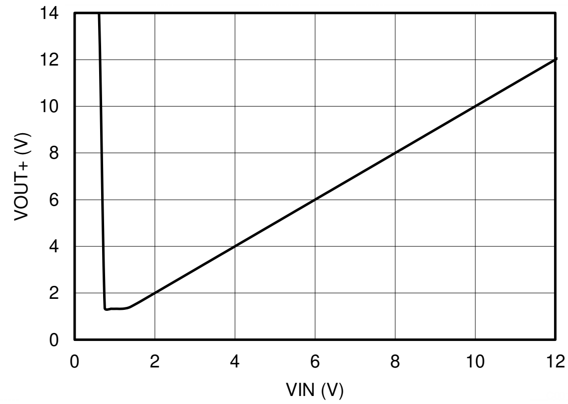


Figure 7-3. Positive Output Voltage vs Input Voltage

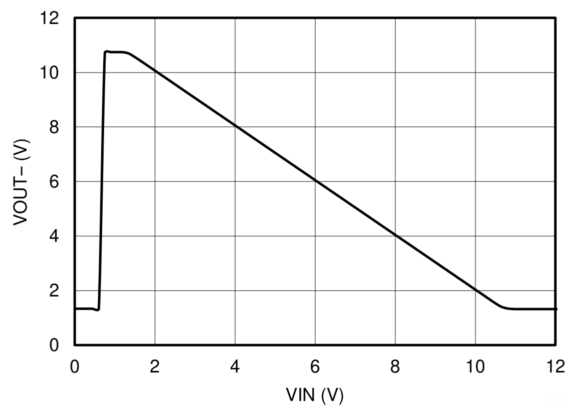


Figure 7-4. Positive Output Voltage vs Input Voltage

7.2 Power Supply Recommendations

The RC4580 device is specified for operation over the range of ±2V to ±16V; many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages outside of the ±18V range can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

7.3 Layout

7.3.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.3.2 Layout Example

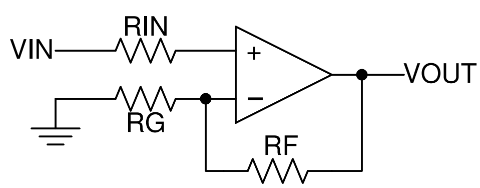


Figure 7-5. Operational Amplifier Schematic for Noninverting Configuration

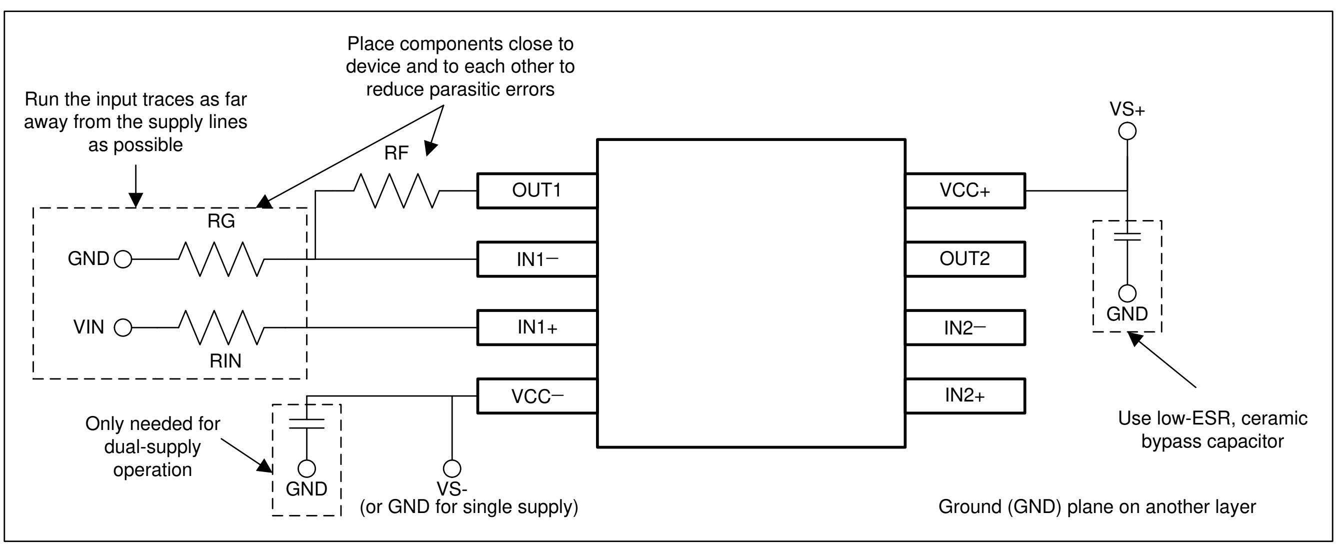


Figure 7-6. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision D (November 2014) to Revision E (November 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added the P (PDIP, 8), DGK (VSSOP, 8), and DDF (SOT-23, 8) packages to the data sheet..........................1
- Changed the slew rate value listed in the *Slew Rate* section from: 5V/ms to: 5V/μs to match the slew rate values listed in the *Features* section and *Electrical Characteristics* table.. 8
- Deleted references to the *Circuit Board Layout Techniques* application note... 11

Changes from Revision C (March 2004) to Revision D (November 2014) **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.. 1
- Removed *Ordering Information* table.. 1
- Changed T_A = 25°C to T_A = –40°C to 125°C in condition statement for *Electrical Characteristics* table and *Operational Characteristics* table...5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RC4580ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	R4580I
RC4580IDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580F
RC4580IDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580F
RC4580IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580
RC4580IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580
RC4580IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I
RC4580IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I
RC4580IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	RC4580IP
RC4580IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	RC4580IP
RC4580IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 125	R4580I
RC4580IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I
RC4580IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF RC4580 :

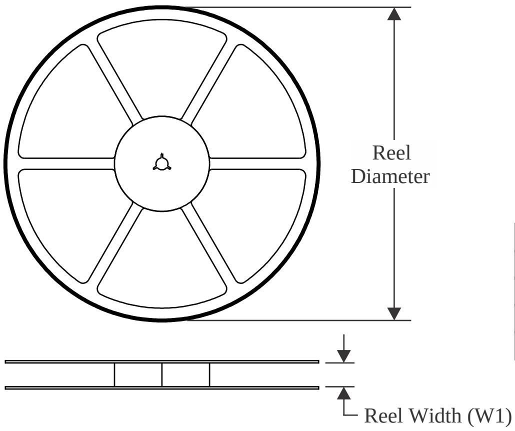
- Automotive : RC4580-Q1

NOTE: Qualified Version Definitions:

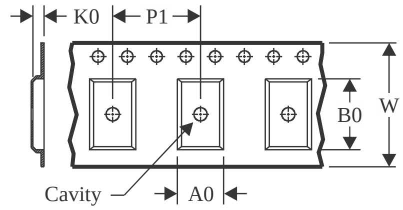
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

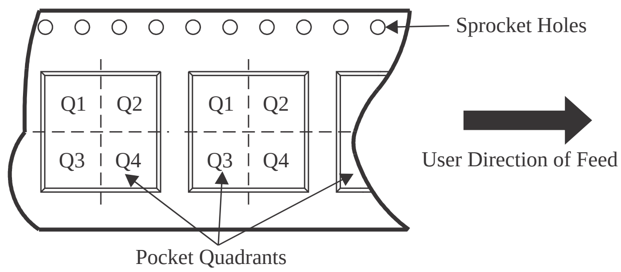


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

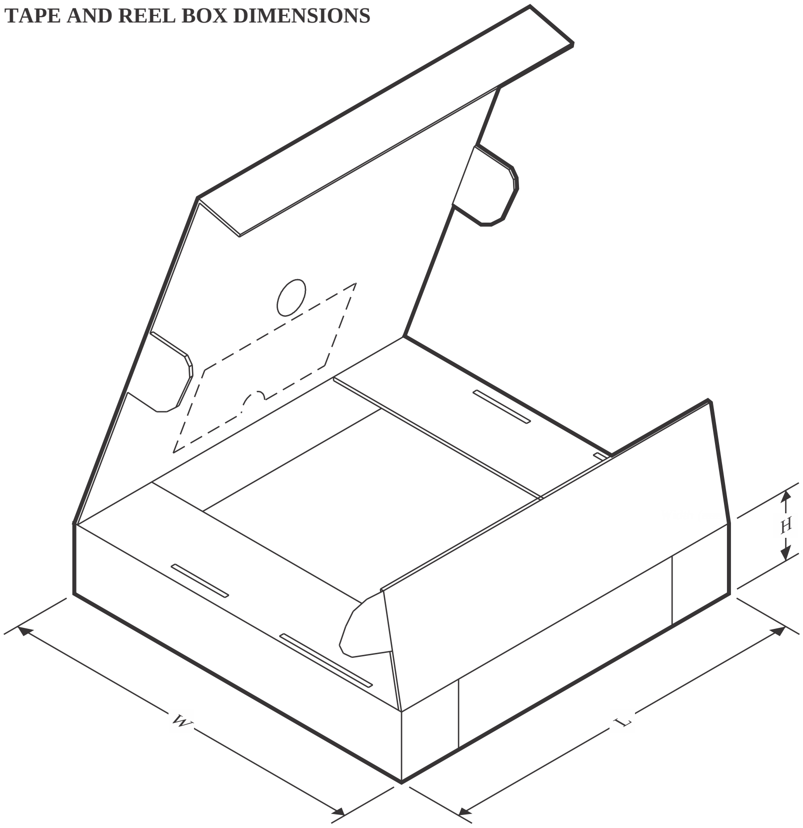
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4580IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
RC4580IDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

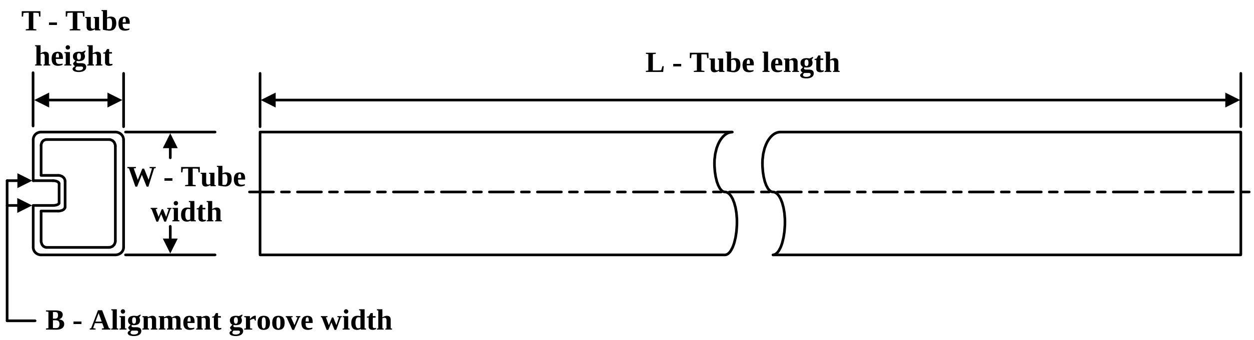
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

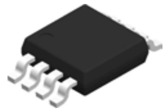
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4580IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
RC4580IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
RC4580IDR	SOIC	D	8	2500	353.0	353.0	32.0
RC4580IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

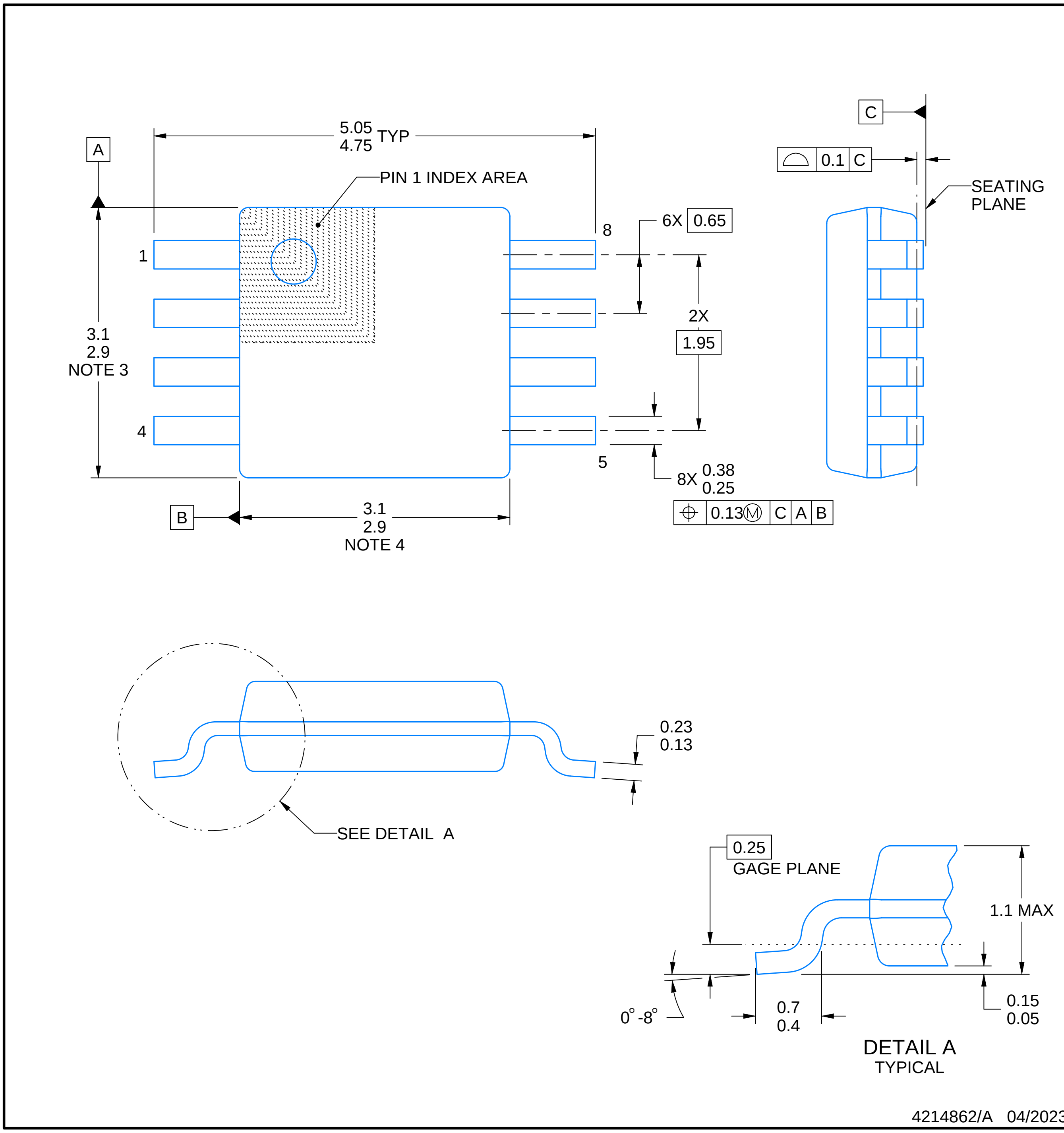
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
RC4580IP	P	PDIP	8	50	506	13.97	11230	4.32
RC4580IP.A	P	PDIP	8	50	506	13.97	11230	4.32



DGK0008A

VSSOP - 1.1 mm max height

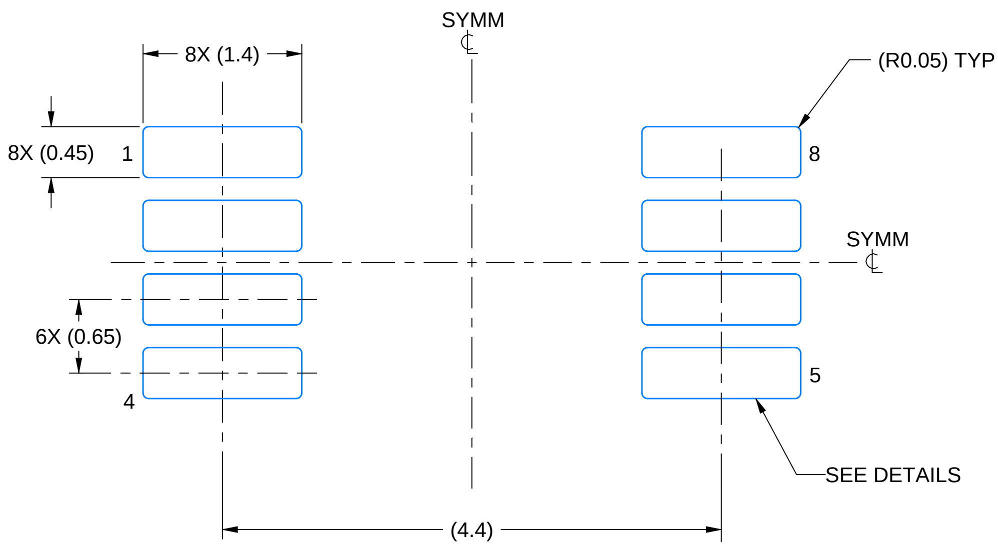
SMALL OUTLINE PACKAGE



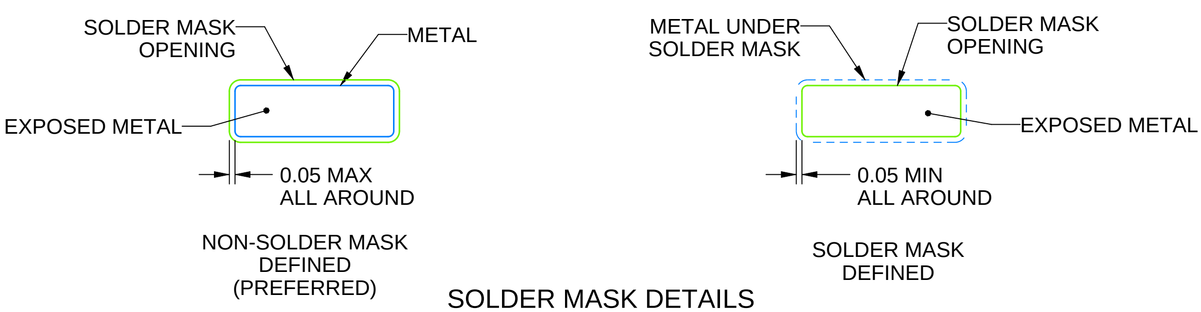
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

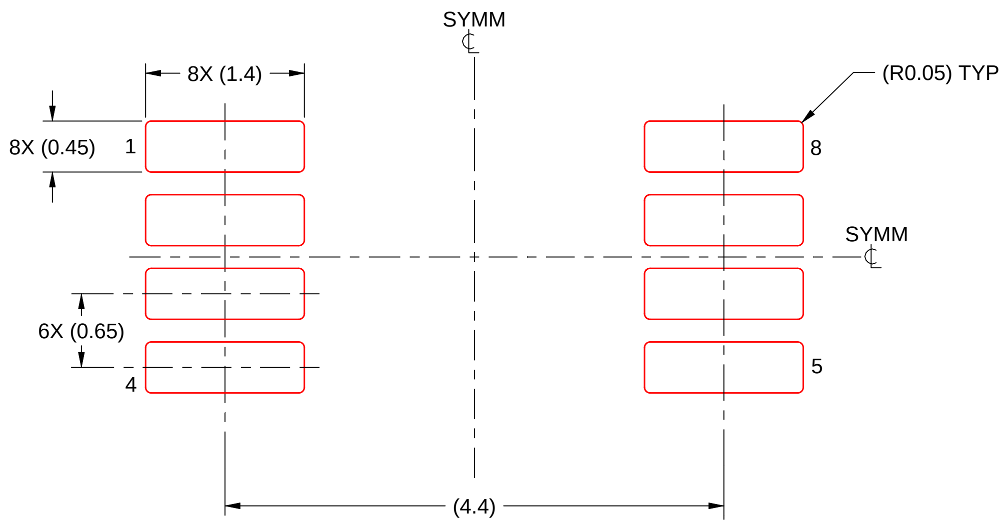


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

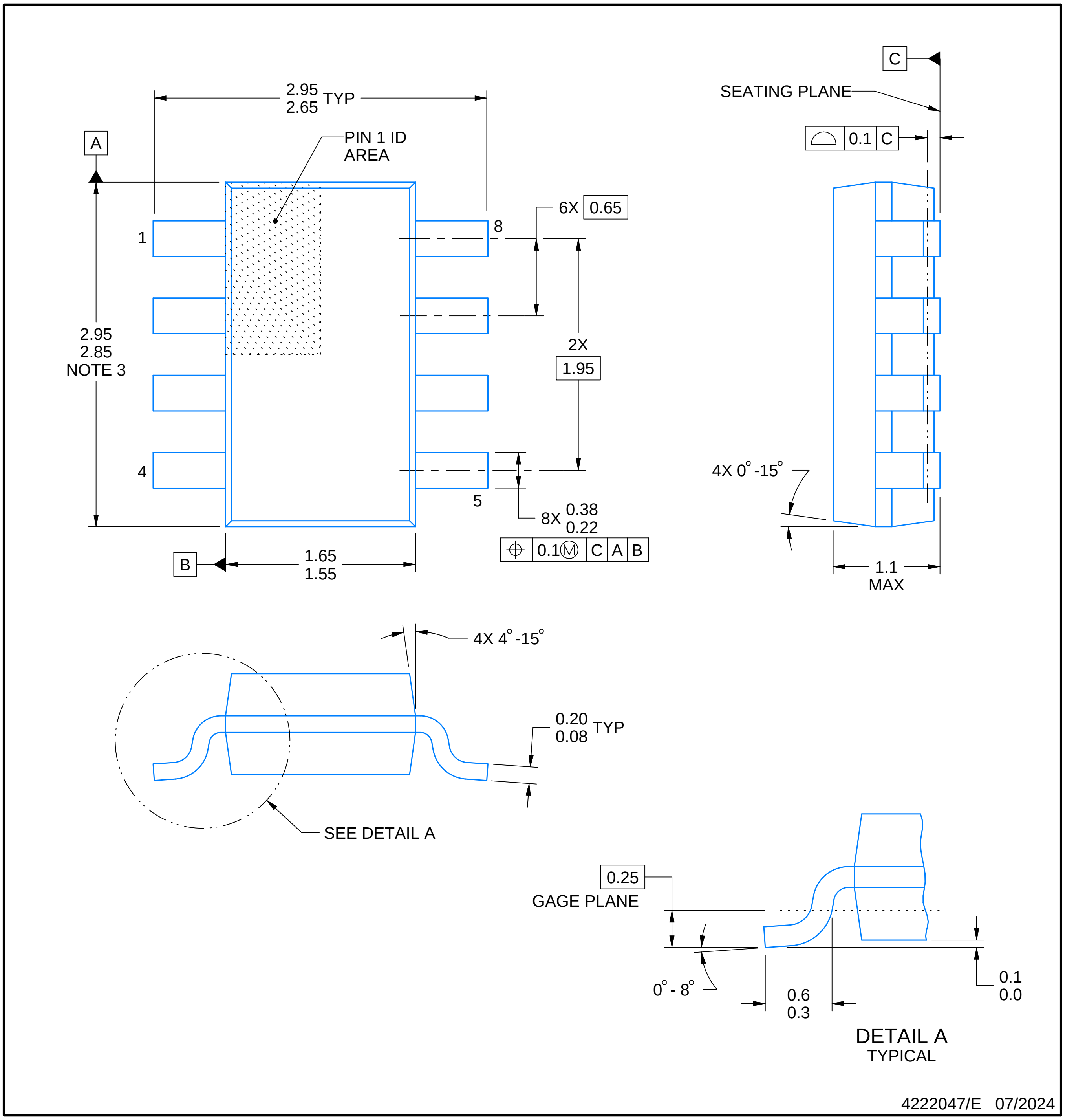


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

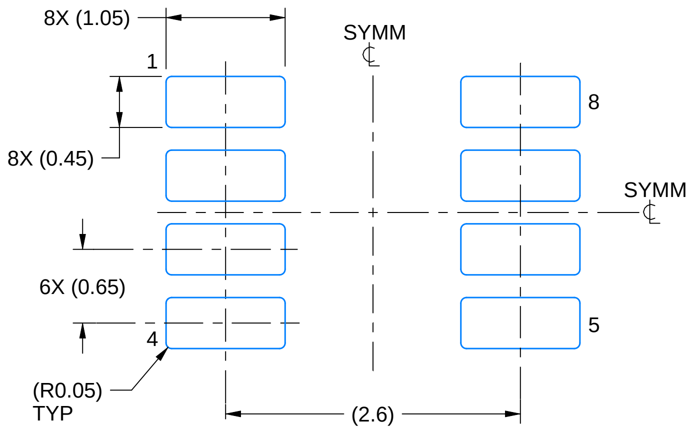
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



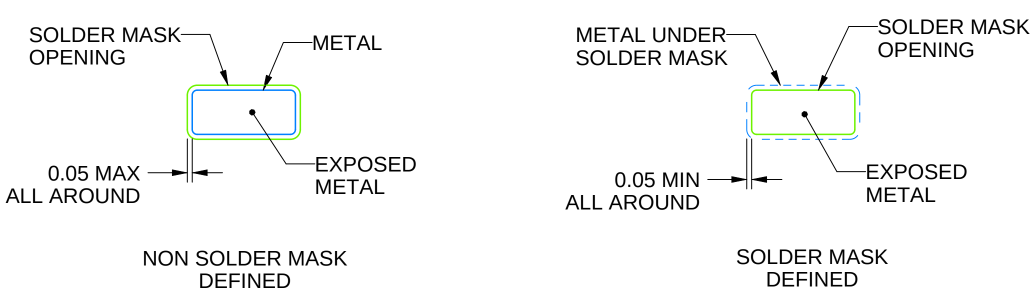
4222047/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

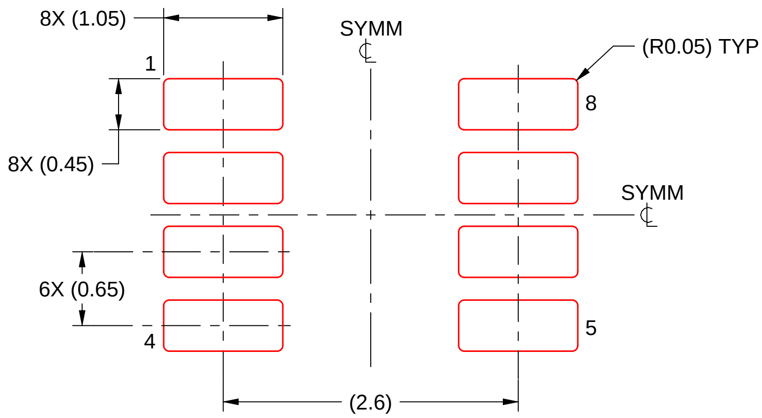


SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

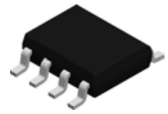


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

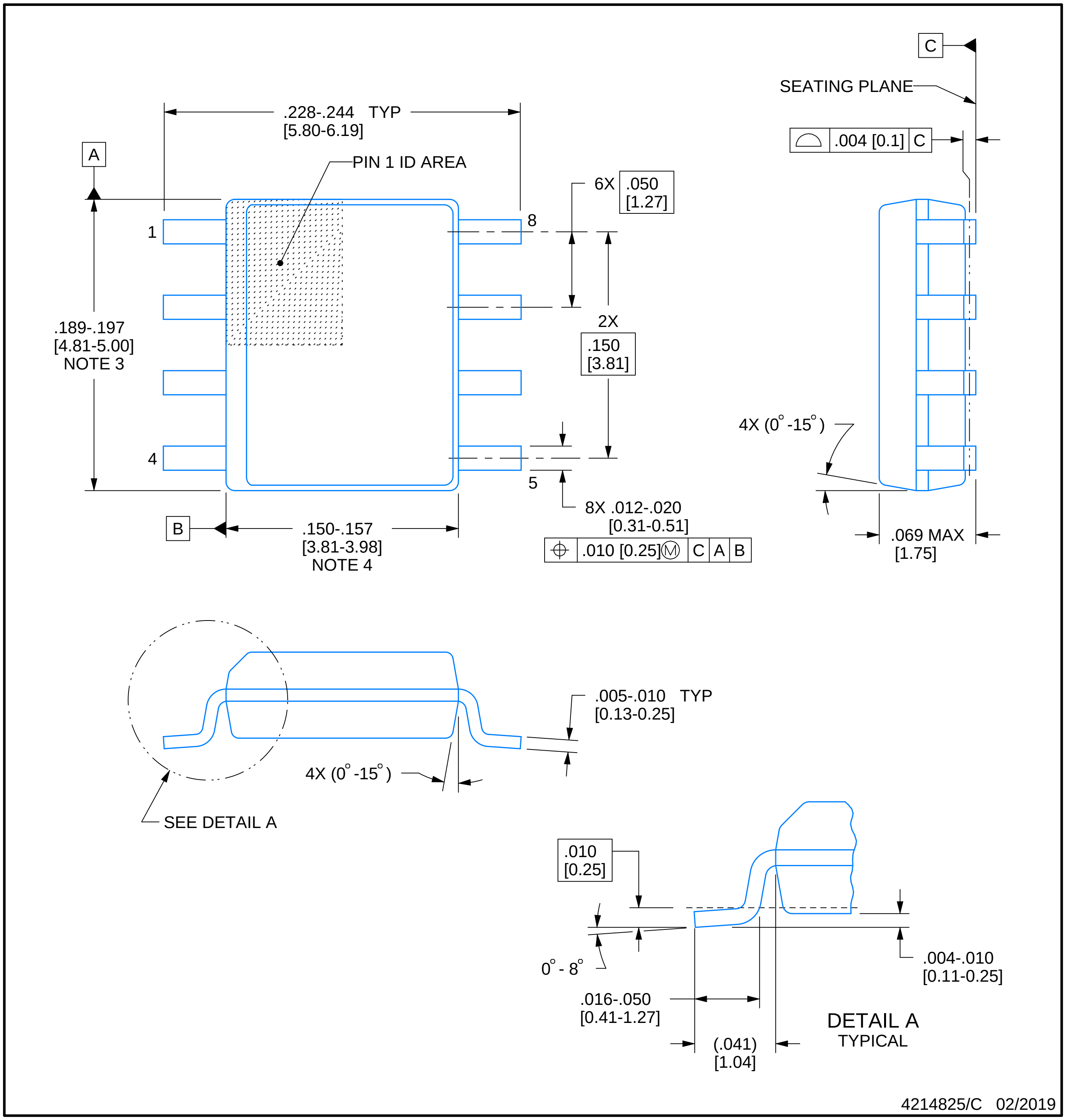


PACKAGE OUTLINE

D0008A

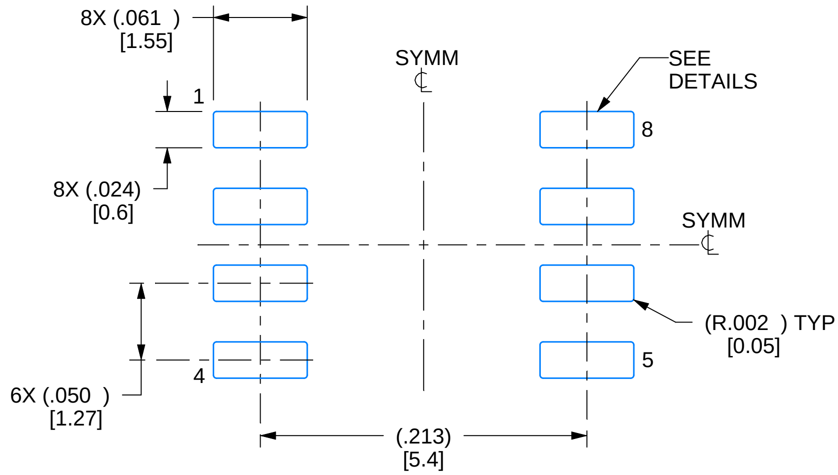
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

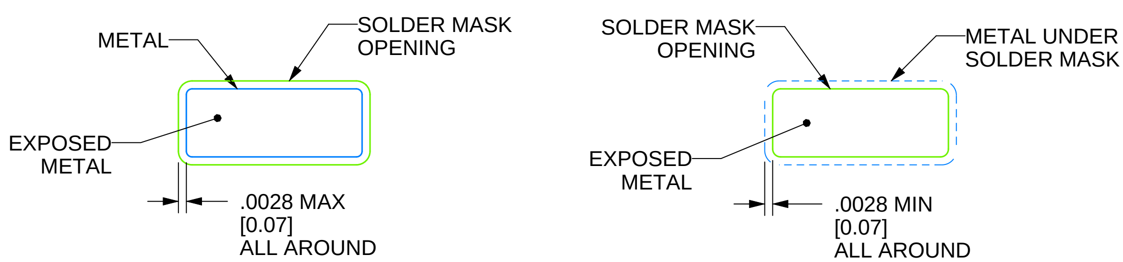


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

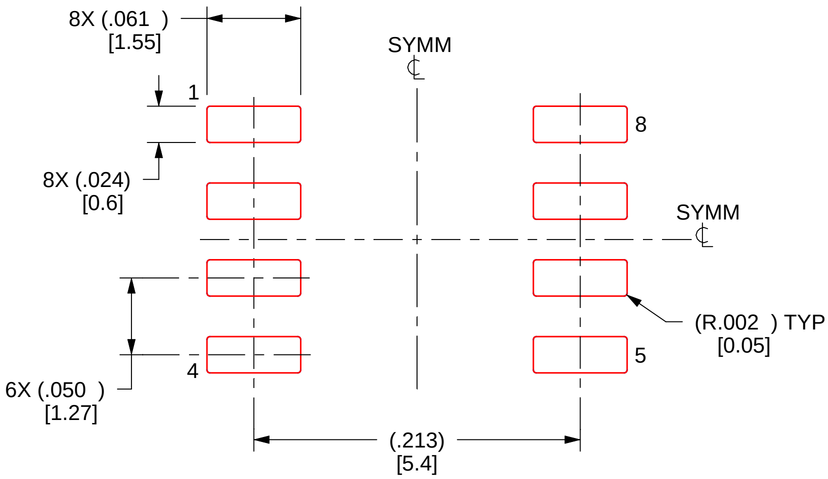
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



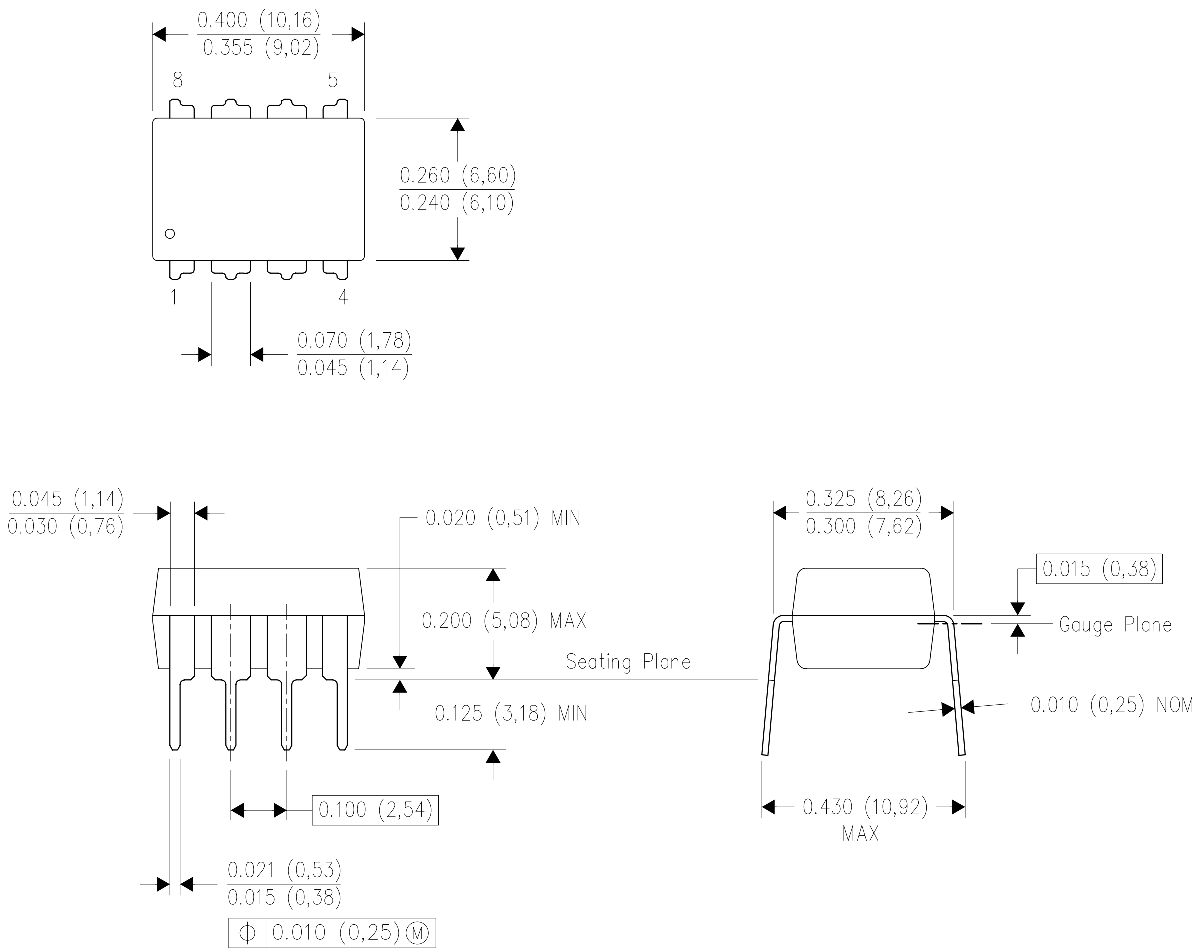
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

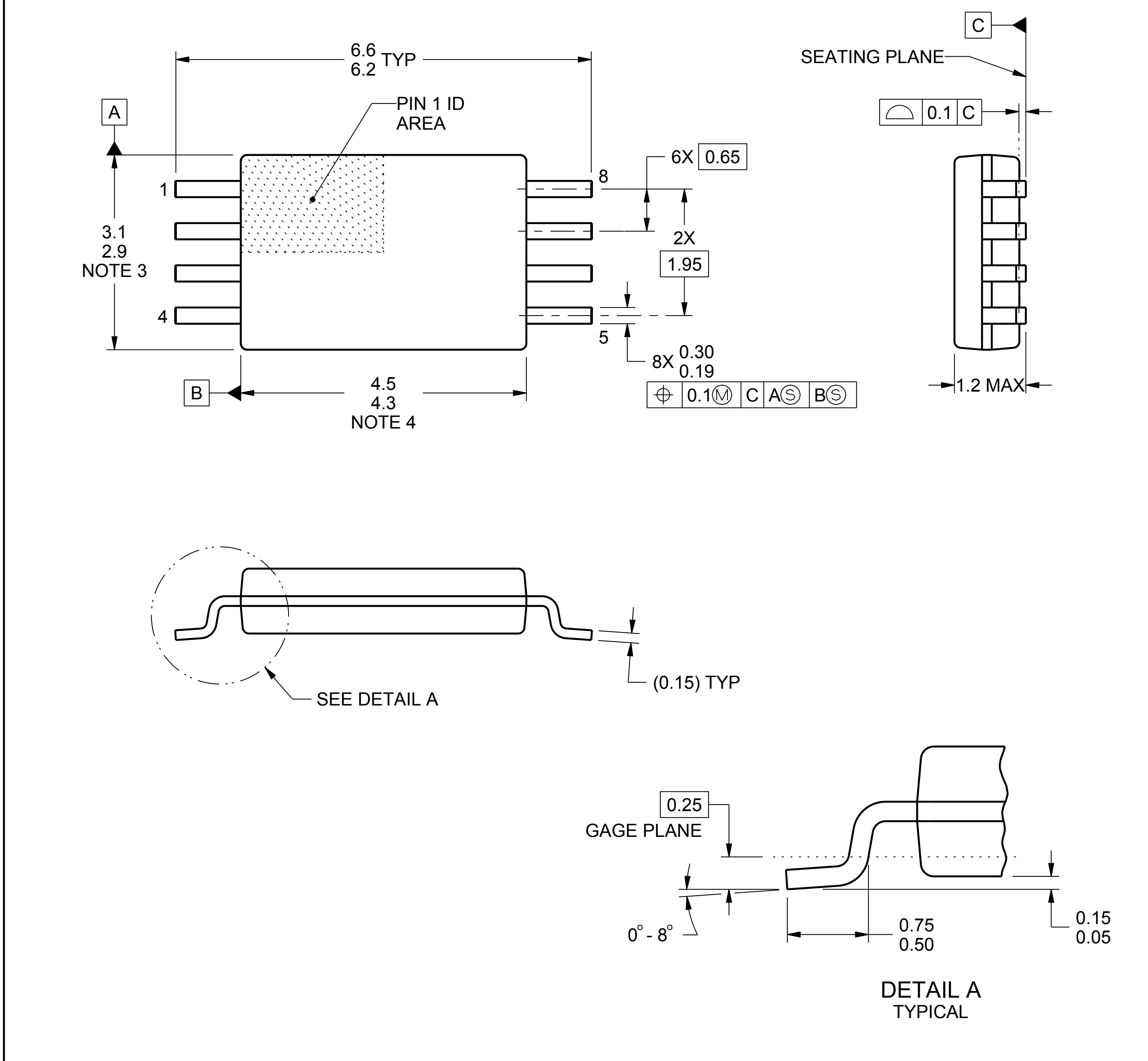
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



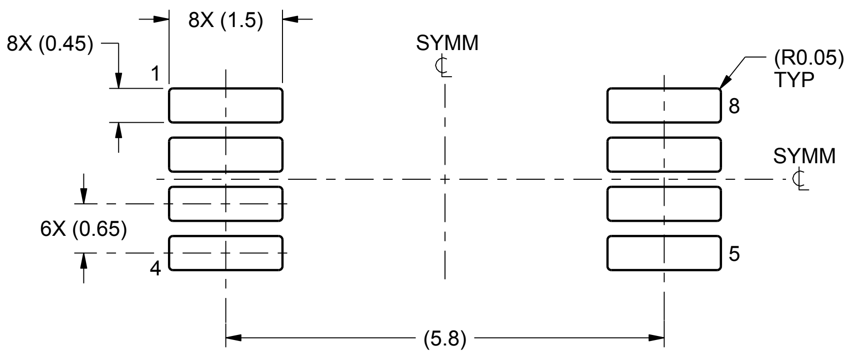
4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

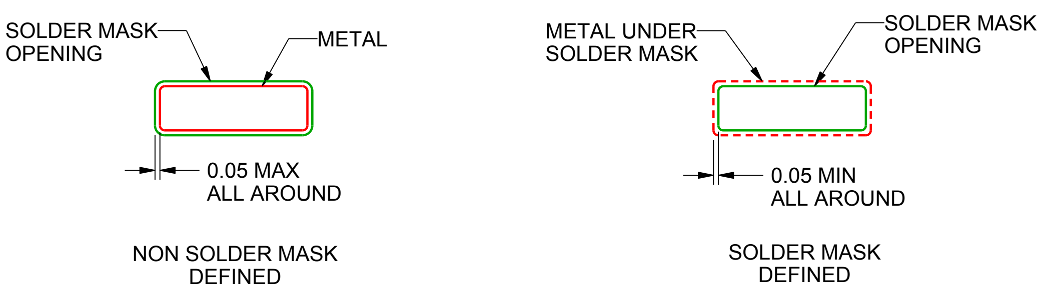


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

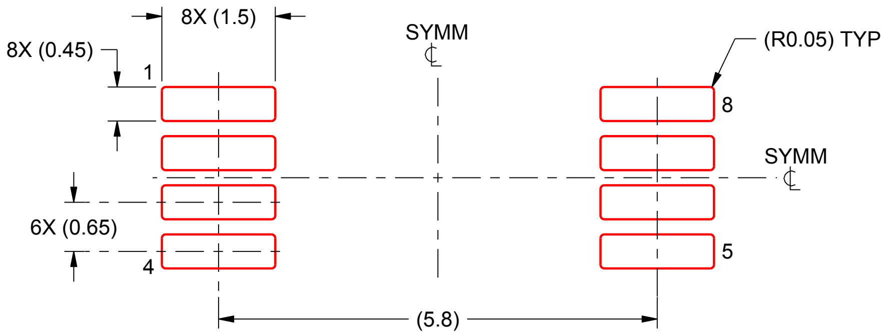


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.