20-W Stereo Digital Audio Power Amplifier With Feedback

Check for Samples: TAS5704

FEATURES

- **Audio Input/Output**
  - **20-W into an 8-Ω Load From an 18-V Supply**
  - **Two Serial Audio Inputs (Four Audio Channels)**
  - **Supports Multiple Output Configurations:**
    - **2-Ch Bridged Outputs (20 W × 2)**
    - **4-Ch Single-Ended Outputs (10 W × 4)**
    - **2-Ch Single-Ended + 1-Ch Bridged (2.1) (10 W × 2 + 20 W)**
- **Closed Loop Power Stage Architecture**
  - **Improved PSRR Reduces Power Supply Performance Requirements**
  - **Higher Damping Factor Provides for Tighter, More Accurate Sound With Improved Bass Response**
  - **Lower EMC Emissions**
  - **Output Power is Independent of Supply Voltage Variation**
- **Wide PVCC Range From (10 V to 26 V)**
- **Supports 32-kHz–192-kHz (DVD-Audio) Sample Rates (LJ/RJ/I^{2}S)**
- **Line-Level Subwoofer PWM Outputs**
- **Audio/PWM Processing (Hardware Controlled)**
  - **4-Step Gain Control (-3dB, 3dB, 9dB, 12dB)**
  - **Soft Mute Control (50% Output Duty Cycle)**
- **Factory-Trimmed Internal Oscillator Enables Automatic Detection of Incoming Sample Rates**
- **Thermal and Short-Circuit Protection**

DESCRIPTION

The TAS5704 is a 20-W, efficient, digital audio power amplifier for driving stereo bridge-tied speakers. Two serial data inputs allow processing of up to four discrete audio channels and seamless integration to most digital audio processors accepting a wide range of input data and clock rates. A hardware configurable data path allows these channels to be routed to the internal speaker drivers or output via the subwoofer PWM outputs.

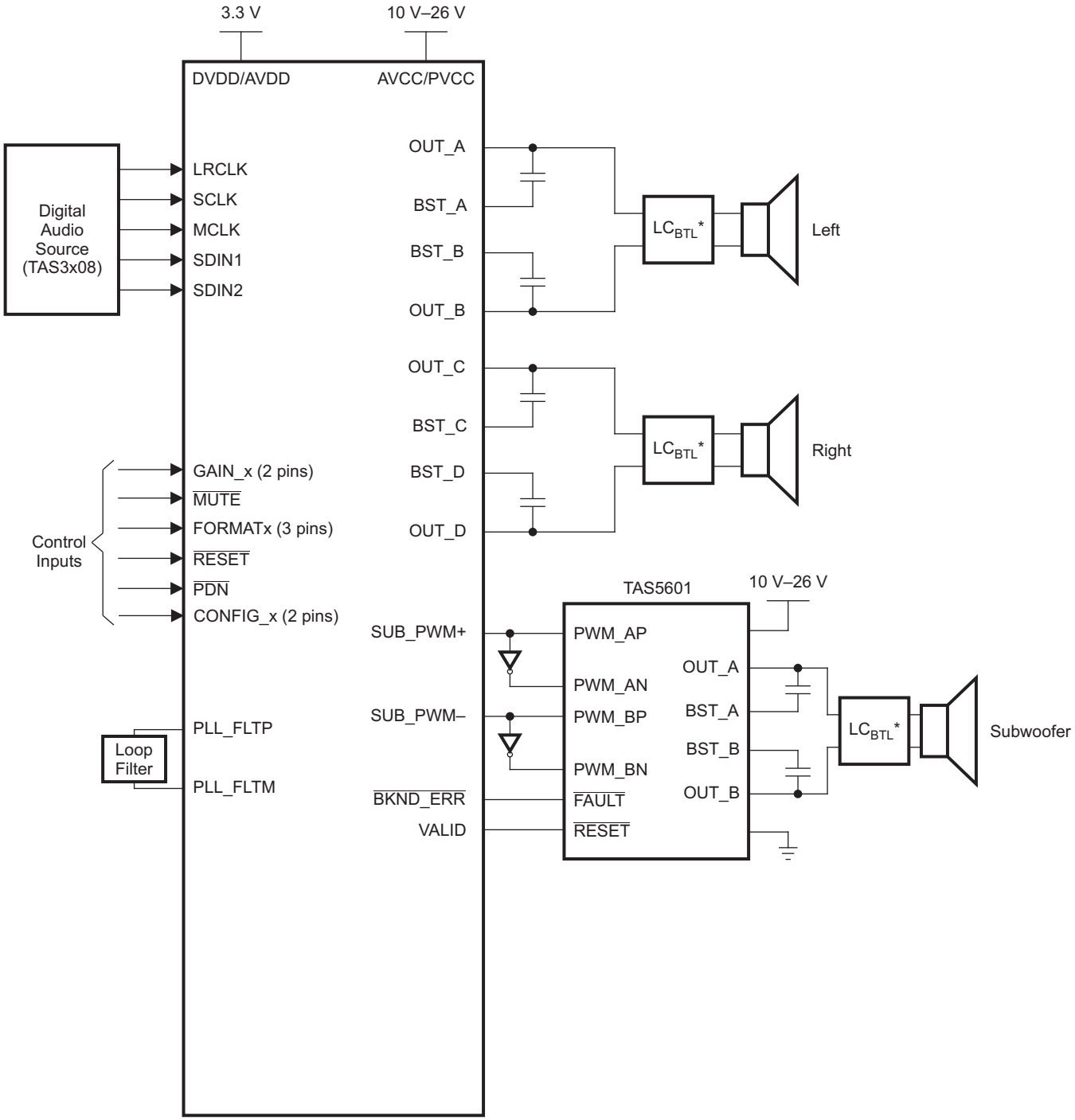
The TAS5704 is a slave-only device receiving all clocks from external sources. The TAS5704 operates at a 384-kHz switching rate for 32-, 48-, 96-, and 192-kHz data, and at a 352.8 kHz switching rate for 44.1-, 88.2-, and 176.4-kHz data. The 8× oversampling combined with the fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

The closed-loop architecture of the TAS5704 provides several benefits. The high power supply rejection enables superior audio performance from a noisy, low cost supply. The high damping factor allows tighter control over speaker movement resulting in an improved bass response. Finally, switching edge rate control lowers EMC emissions without sacrificing audio performance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED APPLICATION DIAGRAMS

Bridge-Tied Load (BTL) Mode



* Refer to TI Application Note (SLOA119) on LC filter design for BTL (AD/BD mode) configuration.

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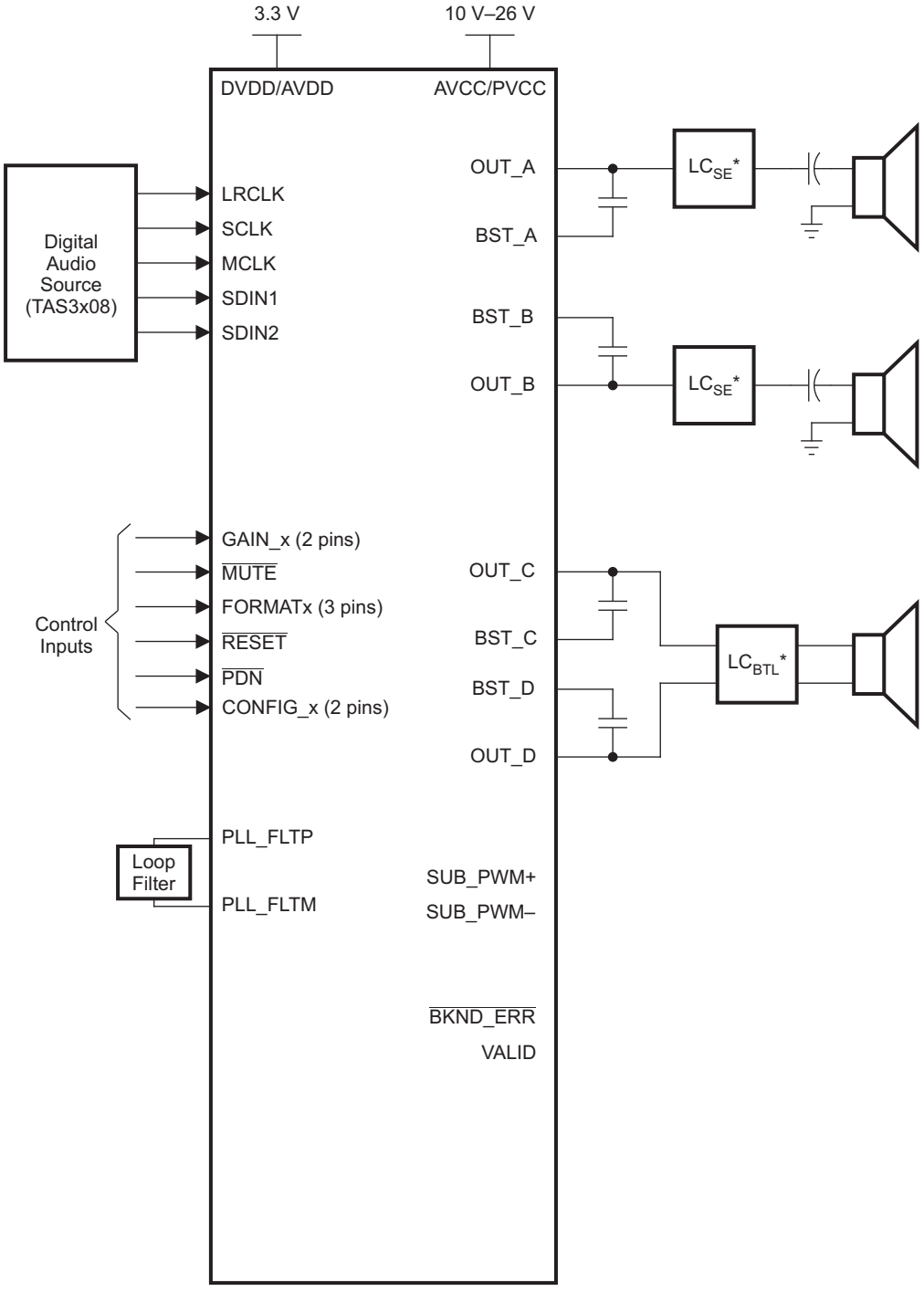
Single-Ended (SE) 2.1 Mode



* Refer to TI Application Note (SLOA119) on LC filter design for SE or BTL configuration.

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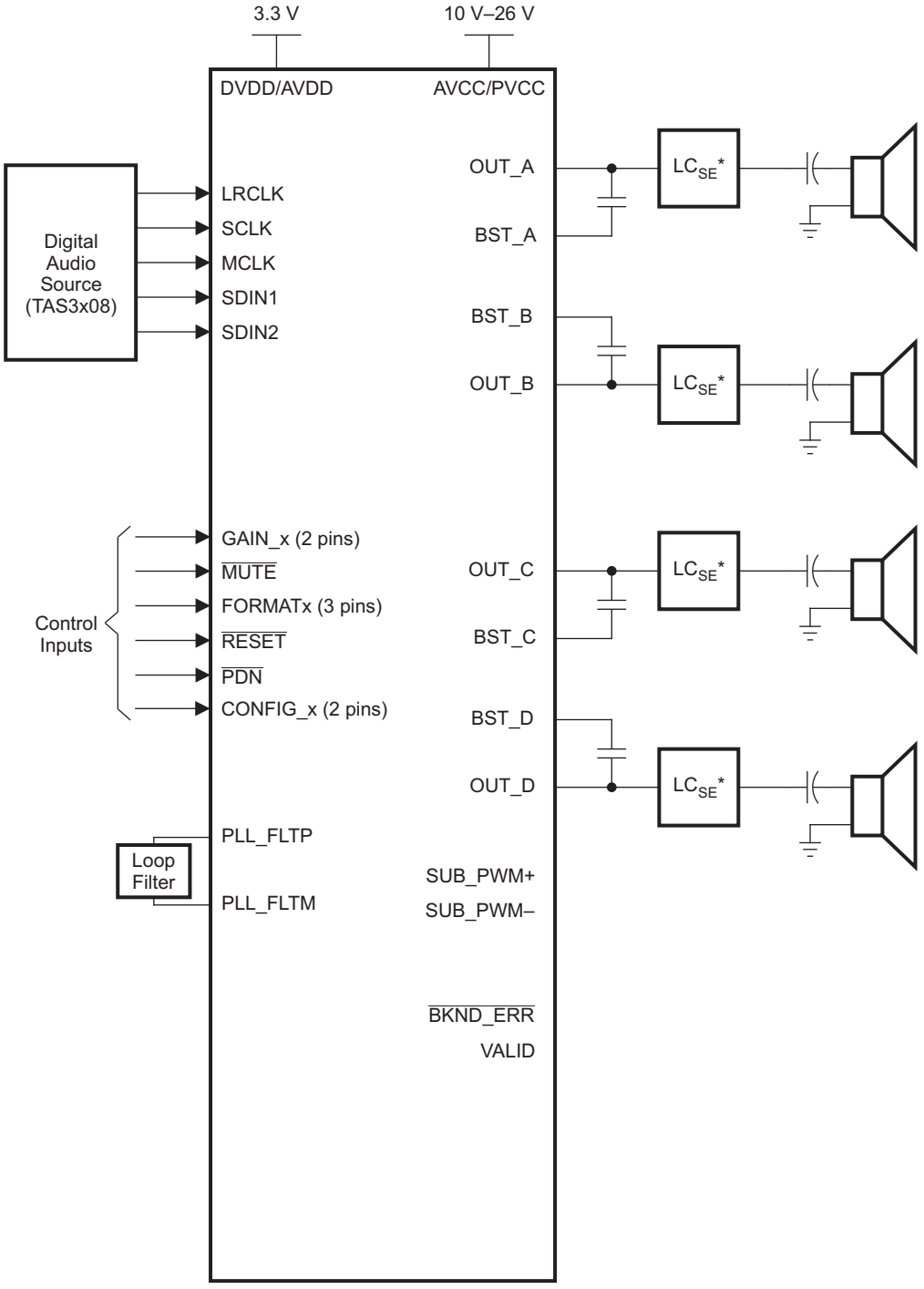
Single-Ended (SE) 4.0 Mode



* Refer to TI Application Note (SLOA119) on LC filter design for SE configuration.

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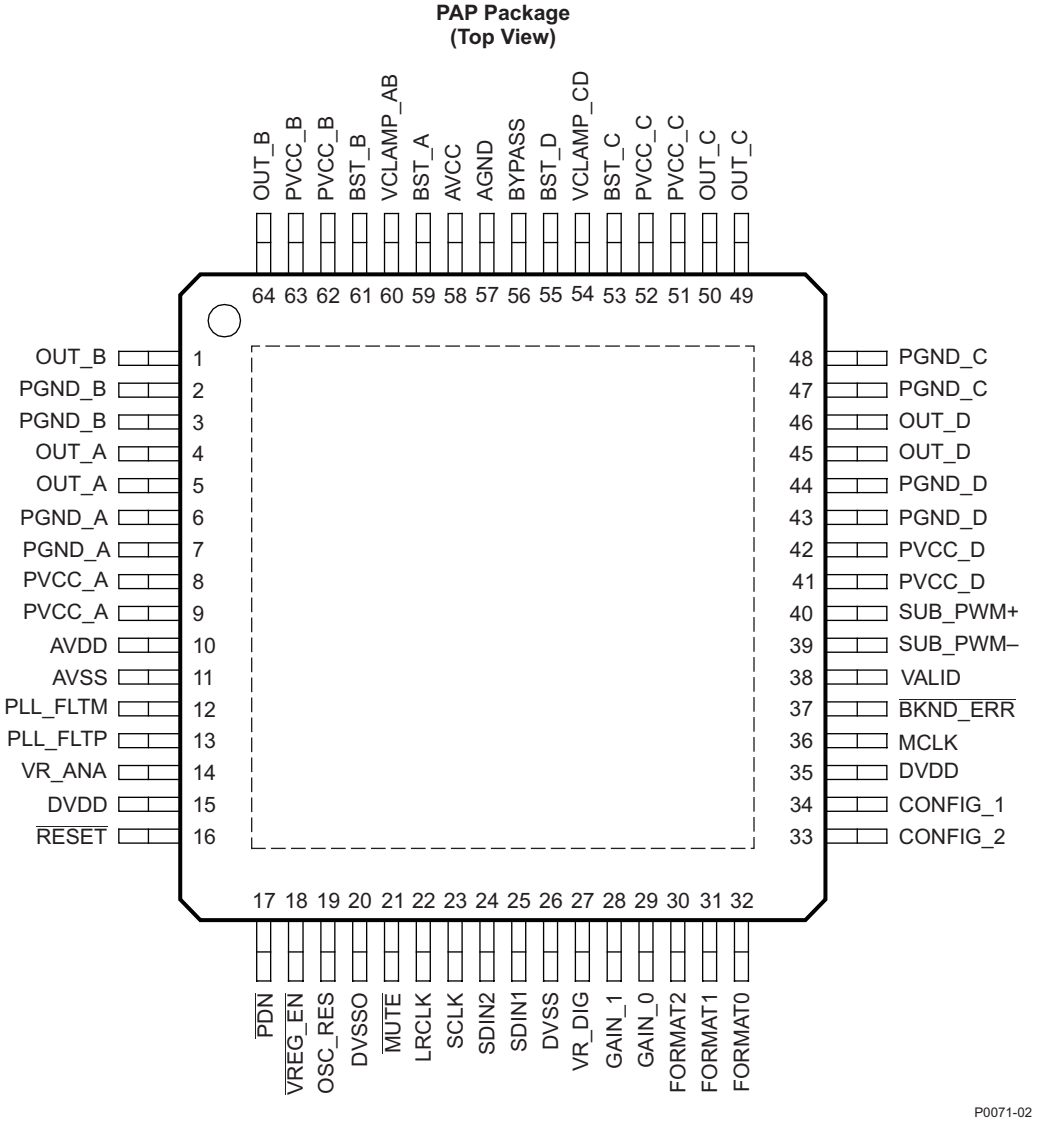
64-PIN, HTQFP PACKAGE



PIN FUNCTIONS

PIN		TYPE (1)	5-V TOLERANT	TERMINATION (2)	DESCRIPTION
NAME	NO.				
AGND	57	P			Analog ground for power stage
AVCC	58	P			Analog power supply for power stage. Connect externally to same potential as PVCC.
AVDD	10	P			3.3-V analog power supply
AVSS	11	P			3.3-V analog supply ground
BKND_ERR	37	DI		Pullup	Active low. A back-end error sequence is initiated by applying a logic low to this pin. Connect to an external power stage. If no external power stage is used, connect directly to DVDD.
BST_A	59	P			High-side bootstrap supply for half-bridge A

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2) All pullups are 20-μA weak pullups and all pulldowns are 20-μA weak pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input). Devices that drive inputs with pullups must be able to sink 50 μA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 50 μA while maintaining a logic-1 drive level.

PIN FUNCTIONS (continued)

PIN		TYPE (1)	5-V TOLERANT	TERMINATION (2)	DESCRIPTION
NAME	NO.				
BST_B	61	P			High-side bootstrap supply for half-bridge B
BST_C	53	P			High-side bootstrap supply for half-bridge C
BST_D	55	P			High-side bootstrap supply for half-bridge D
BYPASS	56	O			Nominally equal to V_{CC}/8. Internal reference voltage for analog cells
CONFIG_1	34	P		Pulldown	Input/output configuration.
CONFIG_2	33	P		Pulldown	Input/output configuration.
DVDD	15, 35	P			3.3-V digital power supply
DVSS	26	P			Digital ground
DVSSO	20	P			Oscillator ground
FORMAT0	32	DI		Pulldown	Digital data format select.
FORMAT1	31	DI		Pulldown	Digital data format select.
FORMAT2	30	DI			Digital data format select.
GAIN_0	29	DI			LSB of gain select. GAIN_0 and GAIN_1 allow 4 possible gain selections.
GAIN_1	28	DI			MSB of gain select. GAIN_0 and GAIN_1 allow 4 possible gain selections.
LRCLK	22	DI	5-V		Input serial audio data left/right clock (sampling rate clock)
MCLK	36	DI	5-V		Master clock input. The input frequency of this clock can range from 4.9 MHz to 49.2 MHz.
$\overline{\text{MUTE}}$	21	DI	5-V	Pullup	Performs a soft mute of outputs, active-low. A logic low on this terminal sets the outputs equal to 50% duty cycle. A logic high on this terminal allows normal operation. The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
OSC_RES	19	AO			Oscillator trim resistor. Connect an 18.2-kΩ resistor to DVSSO.
OUT_A	4, 5	O			Output, half-bridge A
OUT_B	1, 64	O			Output, half-bridge B
OUT_C	49, 50	O			Output, half-bridge C
OUT_D	45, 46	O			Output, half-bridge D
$\overline{\text{PDN}}$	17	DI	5-V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ stops all clocks and outputs stop switching. When $\overline{\text{PDN}}$ is released, the device powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration. Changes to CONFIG_x, FORMATx, and GAIN_x pins are ignored on $\overline{\text{PDN}}$ cycling.
PGND_A	6, 7	P			Power ground for half-bridge A
PGND_B	2, 3	P			Power ground for half-bridge B
PGND_C	47, 48	P			Power ground for half-bridge C
PGND_D	43, 44	P			Power ground for half-bridge D
PLL_FLTM	12	AO			PLL negative loop filter terminal
PLL_FLTP	13	AO			PLL positive loop filter terminal
PVCC_A	8, 9	P			Power supply input for half-bridge output A
PVCC_B	62, 63	P			Power supply input for half-bridge output B
PVCC_C	51, 52	P			Power supply input for half-bridge output C
PVCC_D	41, 42	P			Power supply input for half-bridge output D

PIN FUNCTIONS (continued)

PIN		TYPE (1)	5-V TOLERANT	TERMINATION (2)	DESCRIPTION
NAME	NO.				
$\overline{\text{RESET}}$	16	DI	5-V	Pullup	Reset, active-low. A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that sets the VALID outputs low, and places the PWM in the hard-mute state (stops switching). Gain is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4- to 5-ms device initialization and sets the gain, output configuration, and format to the settings determined by the hardware pins.
SCLK	23	DI	5-V		Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
SDIN1	25	DI	5-V		Serial audio data-1 input is one of the serial data input ports. SDIN1 supports three discrete (stereo) data formats.
SDIN2	24	DI	5-V		Serial audio data-2 input is one of the serial data input ports. SDIN2 supports three discrete (stereo) data formats.
SUB_PWM–	39	DO			Subwoofer negative PWM output
SUB_PWM+	40	DO			Subwoofer positive PWM output
VALID	38	DO			Output indicating validity of all PWM channels, active high. Connect this pin to an external power stage or leave floating.
VCLAMP_AB	60	P			Internally generated voltage supply for channels A and B gate drive. Not to be used as a supply or connected to any component other than the decoupling capacitor
VCLAMP_CD	54	P			Internally generated voltage supply for channels C and D gate drive. Not to be used as a supply or connected to any component other than the decoupling capacitor
VR_ANA	14	P			Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices.
VR_DIG	27	P			Internally regulated 1.8-V digital supply voltage. This terminal must not be used to power external devices.
$\overline{\text{VREG\_EN}}$	18	DI		Pulldown	Voltage regulator enable. Connect directly to GND.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage	DVDD, AVDD	–0.3 to 3.6	V
	PVCC_X	-0.3 to 30	V
Input voltage	3.3-V digital input	–0.5 to DVDD + 0.5	V
	5-V tolerant(2) digital input	–0.5 to 6	V
Input clamp current, I_{IK} (V_I < 0 or V_I > 1.8 V		±20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > 1.8 V		±20	mA
Operating free-air temperature		0 to 85	°C
Operating junction temperature range		0 to 150	°C
Storage temperature range, T_{stg}		–40 to 125	°C

(1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDIN1, and SDIN2.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TAS5704 PAP (64 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	27	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	15.6	
θ_{JB}	Junction-to-board thermal resistance	12.6	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	7.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Digital/analog supply voltage	DVDD	3	3.3	3.6	V
	Half-bridge supply voltage	PVCC_xx	10		26	V
V_{IH}	High-level input voltage	3.3-V TTL, 5-V tolerant	2			V
V_{IL}	Low-level input voltage	3.3-V TTL, 5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J	Operating junction temperature range		0		150	°C
R_L (BTL)	Load impedance	Output filter: L = 22 μH, C = 680 nF.	6.0	8		Ω
R_L (SE)			3.2	4		
R_L (PBTL)			3.2	4		
L_O (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition		10		μH
L_O (SE)				10		
L_O (PBTL)				10		

PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MODE	VALUE	UNITS
Output sample rate 2×–1× oversampled	32–kHz data rate ±2%	12× sample rate	384	kHz
	44.1-, 88.2-, 176.4-kHz data rate ±2%	8×, 4×, and 2× sample rates	352.8	kHz
	48-, 96-, 192-kHz data rate ±2%	8×, 4×, and 2× sample rates	384	kHz

PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLKI}	Frequency, MCLK (1 / t_{cyc2})		4.9		49.2	MHz
	MCLK duty cycle		40%	50%	60%	
	MCLK minimum high time	≥2-V MCLK = 49.152 MHz, within the min and max duty cycle constraints	8			ns
	MCLK minimum low time	≤0.8-V MCLK = 49.152 MHz, within the min and max duty cycle constraints	8			ns
	LRCLK allowable drift before LRCLK reset				4	MCLKs
	External PLL filter capacitor C1	SMD 0603 Y5V		47		nF
	External PLL filter capacitor C2	SMD 0603 Y5V		4.7		nF
	External PLL filter resistor R	SMD 0603, metal film		470		Ω

ELECTRICAL CHARACTERISTICS

DC Characteristics, T_A = 25°C, PVCC_X, AVCC = 18 V, DVDD = AVDD = 3.3 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL and 5-V tolerant (1)	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	3.3-V TTL and 5-V tolerant (1)	I_{OL} = 4 mA			0.5	V
| VOS |	Class-D output offset voltage				±26		mV
V_{BYPASS}	PVCC/8 reference for analog section		No load	2.2	2.26	2.3	V
I_{IL}	Low-level input current	LRCLK, SCLK, SDINx, MCLK, GAIN_x, $\overline{\text{VREG\_EN}}$, FORMATx, CONFIG_x	V_I = 0 V, DVDD = 3.6 V			±2	μA
		$\overline{\text{BKND\_ERR}}$, $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$	V_I = 0 V, DVDD = 3.6 V			±50	
I_{IH}	High-level input current	$\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, GAIN_x, $\overline{\text{BKND\_ERR}}$	V_I = 3.6 V, DVDD = 3.6 V			±2	μA
		$\overline{\text{VREG\_EN}}$, FORMAT_x, CONFIGx, LRCLK, SCLK, SDINx, MCLK	V_I = 3.6 V, DVDD = 3.6 V			±50	
		$\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, LRCLK, SCLK, SDINx, MCLK, GAIN_x	V_I = 5.5 V, DVDD = 3.6 V			±50	
I_{DD}	Digital supply current	Supply voltage (DVDD, AVDD)	Normal mode		65	80	mA
			Power down ($\overline{\text{PDNZ}}$ = LOW)		8	16	
			Reset ($\overline{\text{RESET}}$ = LOW)		23	33	
I_{CC}	Quiescent supply current		No load	14	33	57	mA
$I_{CC(\overline{\text{RESET}})}$	Quiescent supply current in reset mode		No load		58	176	μA
$I_{CC(\overline{\text{PDNZ}})}$	Quiescent supply current in power down mode		No load		58	176	μA
PSRR	DC power-supply rejection ratio		PVCC = 17.5 V to 18.5 V		60		dB
$R_{DS(on)}$	Drain-source on-state resistance, high-side		V_{CC} = 18 V , I_O = 500 mA, T_J = 25°C		240		mΩ
	Low-side				240		
	Total				480	850	
t_{ON}	Turnon time (SE mode) (CONFIG_2 = 0)		$C_{(BYPASS)}$ = 1 μF, Time required for the BYPASS pin to reach its final value		500		ms
	Turnon time (BTL mode) (CONFIG_2 = 1)				30		
t_{OFF}	Turnoff time (SE mode) (CONFIG_2 = 0) (2)				500		ms
	Turnoff time (BTL mode) (CONFIG_2 = 0) (2)				30		

(1) 5-V tolerant pins are $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDIN1, and SDIN2.
(2) For *pop-free* power-off (PVDD = 0 V), it is recommended that $\overline{\text{PDN}}$ be cycled low for at least this period of time before PVDD drops below 10 V and DVDD drops below 3 V.

AC Characteristics, T_A = 25°C, PVCC_X, AVCC = 18 V, AVDD, DVDD = 3.3 V, R_L = 8 Ω (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Supply ripple rejection	100-mV_{PP} ripple at 20 Hz–20 kHz, BTL, 50% duty cycle PWM		–60		dB
P_O	Continuous output power	BTL (R_L = 8 Ω, THD+N = 10%, f = 1 kHz, PVCC = 18 V)		20.6		W
		BTL (R_L = 8 Ω, THD+N = 7%, f = 1 kHz, PVCC = 18 V)		19.3		W
		SE (R_L = 4 Ω, THD+N = 10%, f = 1 kHz, PVCC = 24 V)		18.1		W
		SE (R_L = 4 Ω, THD+N = 7%, f = 1 kHz, PVCC = 24 V)		17.3		W
THD+N	Total harmonic distortion + noise (SE)	V_{CC} = 24 V, R_L = 4 Ω, f = 1 kHz, P_O = 10 W (half-power)		0.08%		
	Total harmonic distortion + noise (BTL)	V_{CC} = 18 V, R_L = 8 Ω, f = 1 kHz, P_O = 10 W (half-power)		0.05%		
V_n	Output integrated noise	20 Hz to 22 kHz (BD mode)		89		μV
		A-weighted filter; $\overline{MUTE}$ = LOW		–81		dBV
Crosstalk		P_O = 1 W, f = 1 kHz		–69		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, A-weighted		100		dB
	Thermal trip point (output shutdown, unlatched fault)			150		°C
	Thermal hysteresis			15		°C

(1) All measurement in AD mode (unless otherwise noted).

AC Characteristics, T_A = 25°C, PVCC_X, AVCC = 12 V, AVDD, DVDD = 3.3 V, R_L = 8 Ω (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Supply ripple rejection	100-mVpp ripple at 20 Hz–20 kHz, BTL, 50% duty cycle PWM		–60		dB
P_O	Continuous output power	BTL (R_L = 8 Ω, THD+N = 10%, f = 1 kHz)		9.2		W
		BTL (R_L = 8 Ω, THD+N = 7%, f = 1 kHz)		8.7		W
		SE (R_L = 4 Ω, THD+N = 10%, f = 1 kHz)		4.5		W
		SE (R_L = 4 Ω, THD+N = 7%, f = 1 kHz)		4.2		W
THD+N	Total harmonic distortion + noise (BTL)	V_{CC} = 12 V, R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half-power)		0.07%		
V_n	Output integrated noise	20 Hz to 22 kHz (BD mode)		89		μV
		A-weighted filter		–81		dBV
Crosstalk		P_O = 1 W, f = 1 kHz		–75		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, A-weighted		96		dB
	Thermal trip point (output shutdown, unlatched fault)			150		°C
	Thermal hysteresis			15		°C

(1) All measurement in AD mode (unless otherwise noted).

SERIAL AUDIO PORTS SLAVE MODE

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, SCLK 32 × f_S, 48 × f_S, 64 × f_S	C_L = 30 pF	1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		32		64	SCLK edges
$t_{(edge)}$	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period

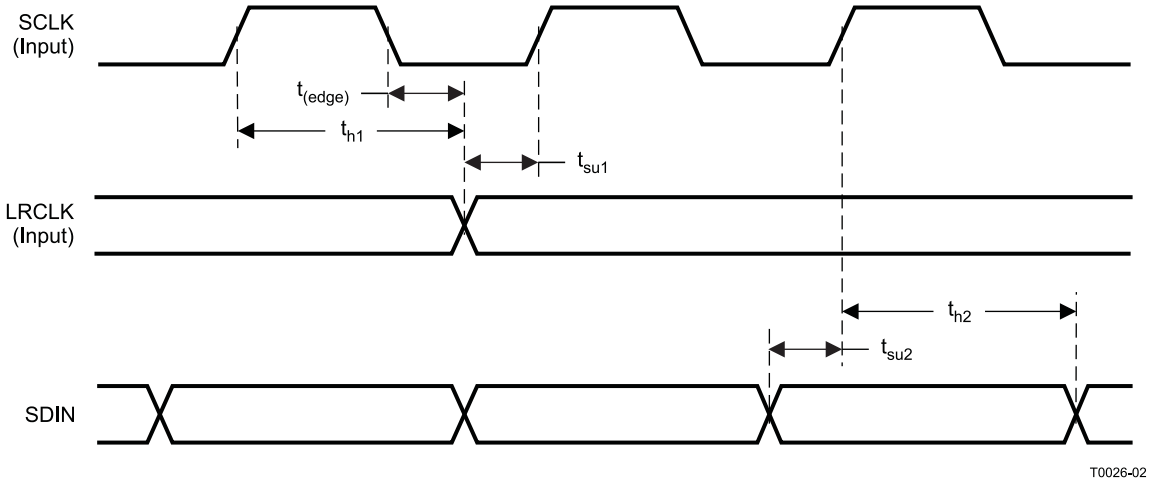


Figure 1. Slave Mode Serial Data Interface Timing

HARDWARE SELECT PINS

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{su}	Setup time, FORMATx, CONFIG_x, GAIN_x to $\overline{\text{RESET}}$ rising edge	100			µs

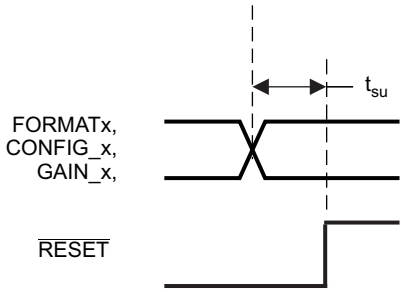


Figure 2. Mode Pins Setup Time

RESET TIMING ($\overline{\text{RESET}}$) AND POWER-ON RESET

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VALID\_LOW)}$	Time to assert VALID (reset to power stage) low		300		ns
$t_{w(RESET)}$	Pulse duration, $\overline{\text{RESET}}$ active		1		ms
$t_{d(START)}$	Time to start-up		13.5		ms

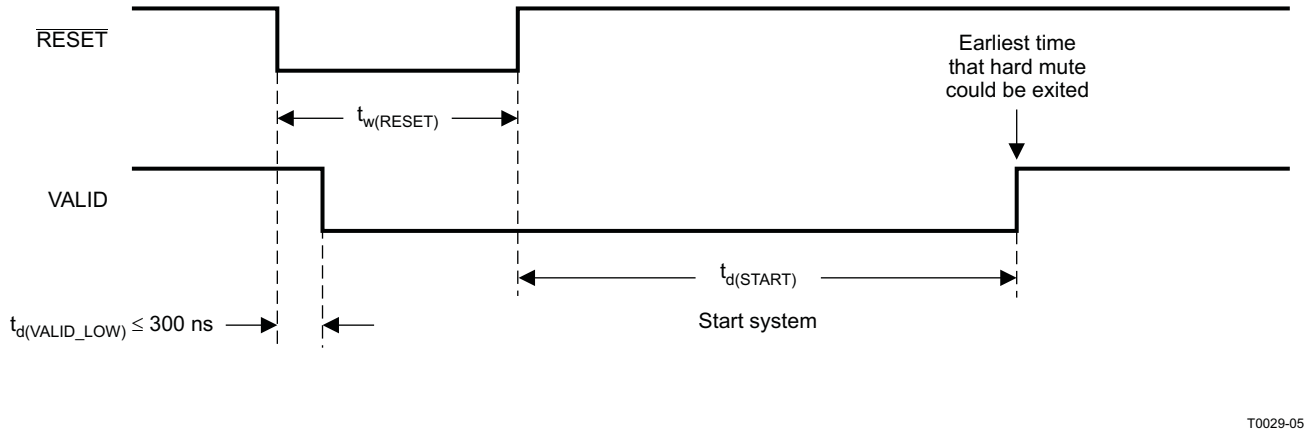


Figure 3. Reset Timing

When power is applied to DVDD, must be held low for at least 100 μs after DVDD reaches 3.0 V.

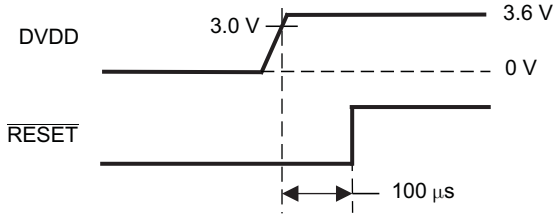


Figure 4. Power-On Reset Timing

POWER-DOWN ($\overline{\text{PDN}}$) TIMING

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VALID\_LOW)}$	Time to assert VALID (reset to power stage) low		725		μs
$t_{d(STARTUP)}$	Device startup time		120		ms
t_w	Minimum pulse duration required		800		ns

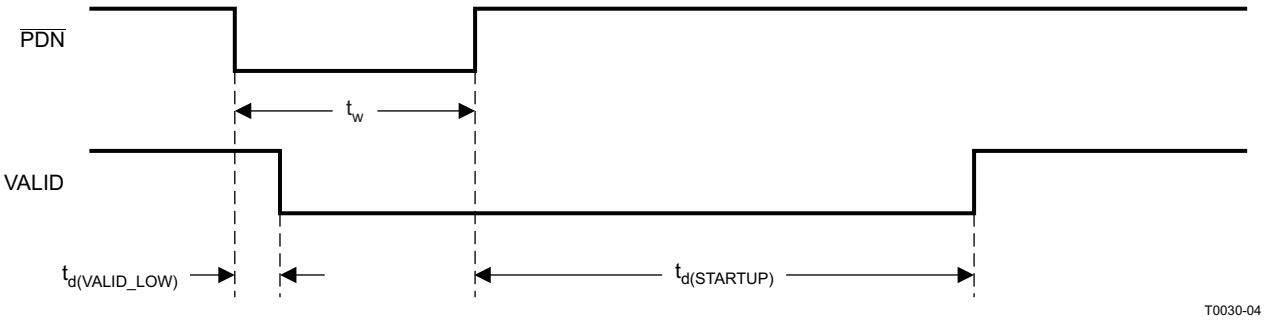


Figure 5. Power-Down Timing

BACK-END ERROR ($\overline{\text{BKND\_ERR}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(ER)}$	Pulse duration, $\overline{\text{BKND\_ERR}}$ active (active-low)	350			ns
$t_{p(valid\_high)}$	Time to stay in the OUT_x low state. After $t_{p(valid\_high)}$, the TAS5704 attempts to bring the system out of the OUT_x low state if $\overline{\text{BKND\_ERR}}$ is high.		300		ms
$t_{p(valid\_low)}$	Time TAS5704 takes to bring OUT_x low after $\overline{\text{BKND\_ERR}}$ assertion.		350		ns

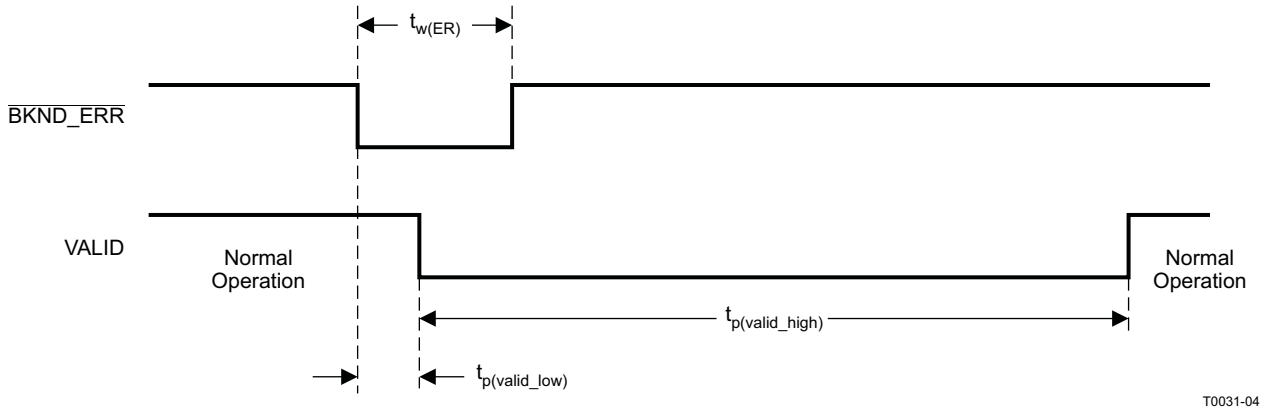


Figure 6. Error Recovery Timing

MUTE TIMING ($\overline{\text{MUTE}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VOL)}$	Volume ramp time. Ramp Time = Number of Steps × Stepsize(1)		1024		steps

(1) Stepsize = 4 LRCLKs (for 32–48 kHz sample rate); 8 LRCLKs (for 88.2–96 kHz sample rate); 16 LRCLKs (for 176.4–192 kHz sample rate)

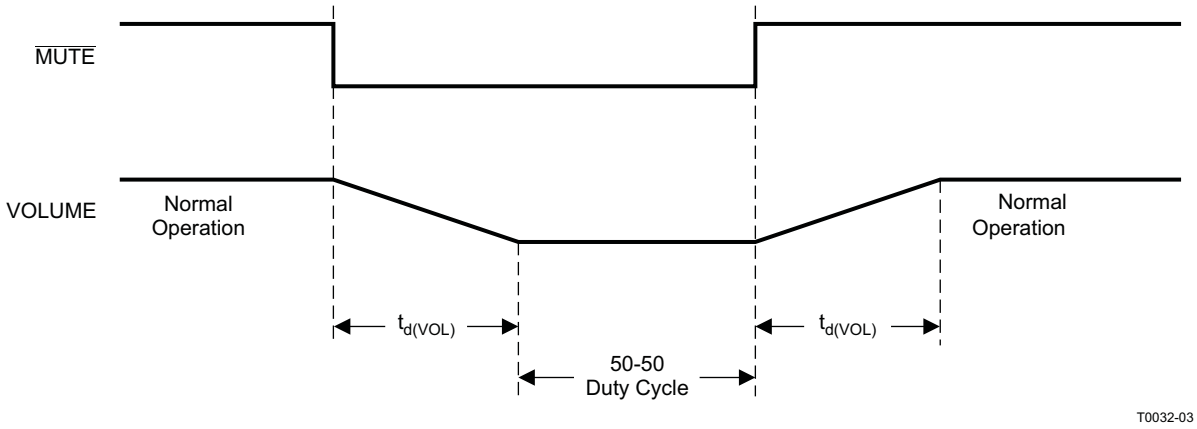


Figure 7. Mute Timing

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

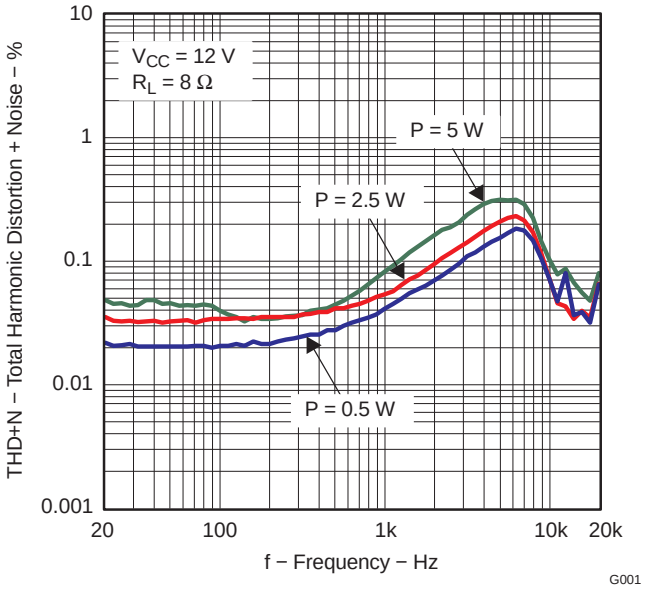


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

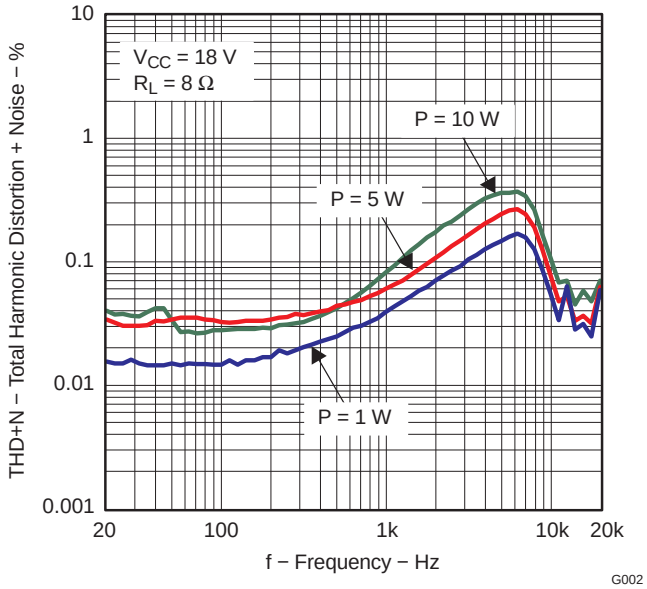


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

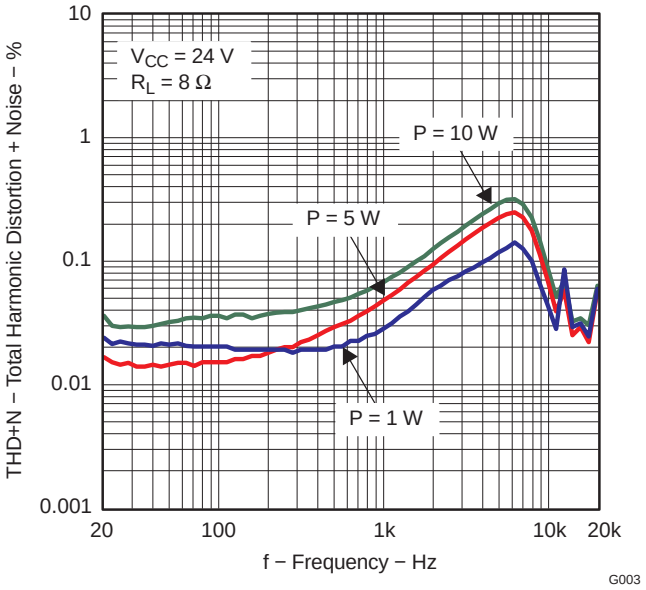


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

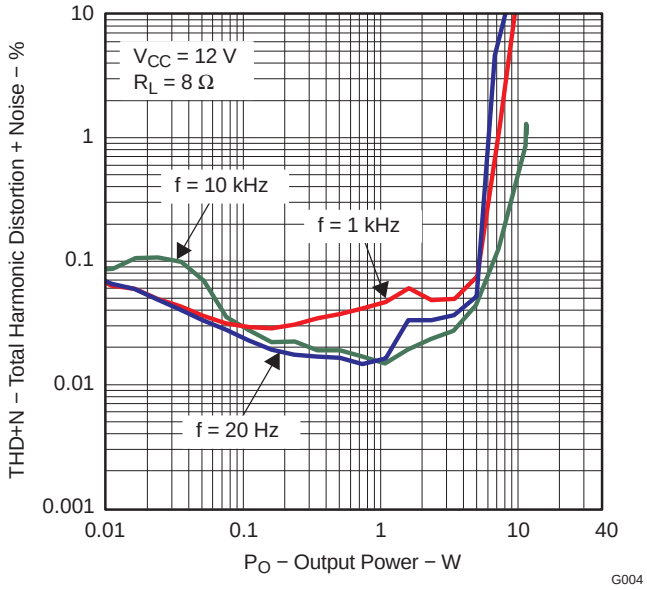


Figure 11.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

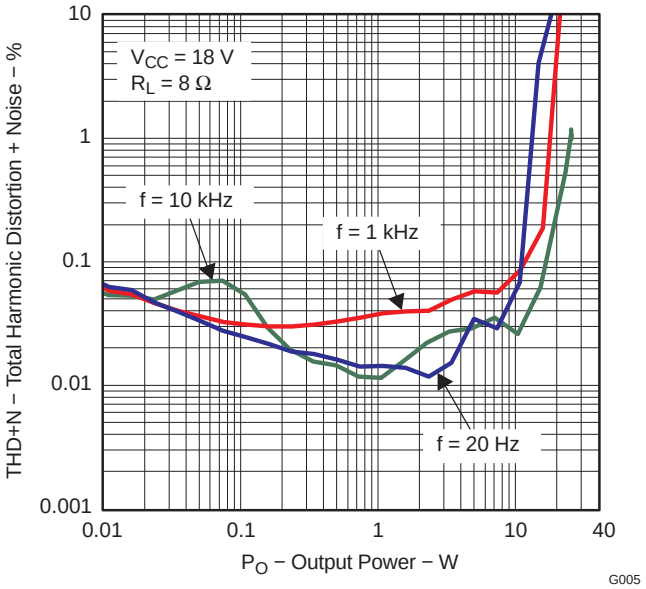


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

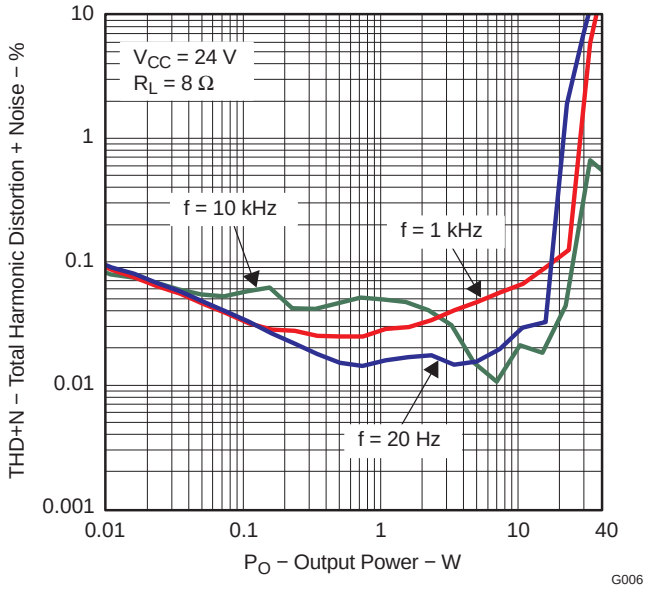


Figure 13.

EFFICIENCY vs OUTPUT POWER

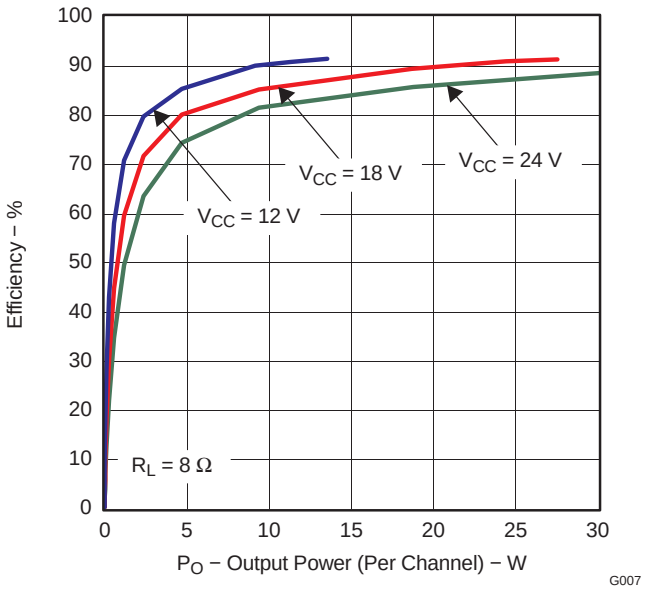


Figure 14.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

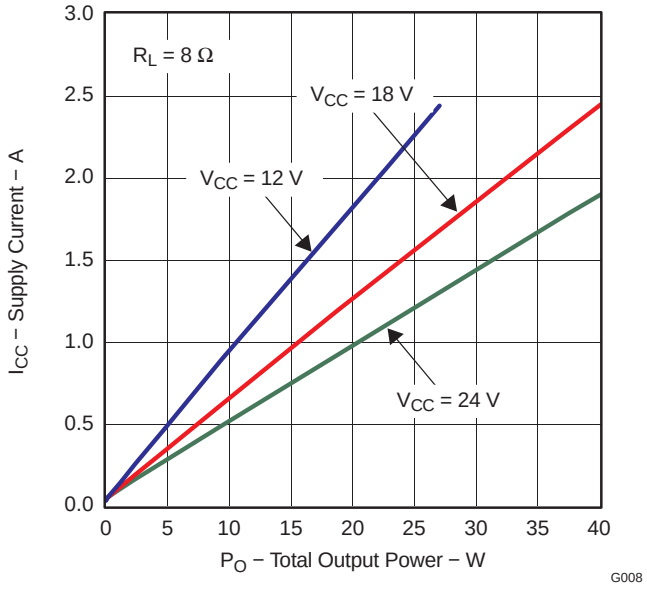


Figure 15.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

OUTPUT POWER vs SUPPLY VOLTAGE

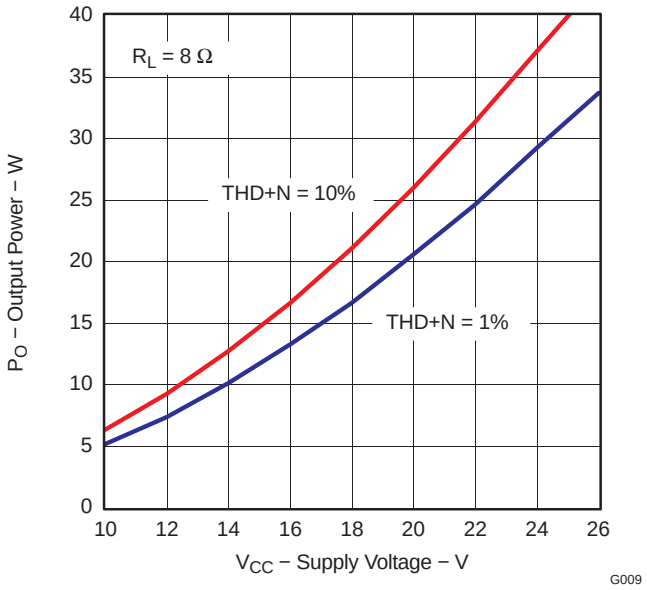


Figure 16.

CROSSTALK vs FREQUENCY

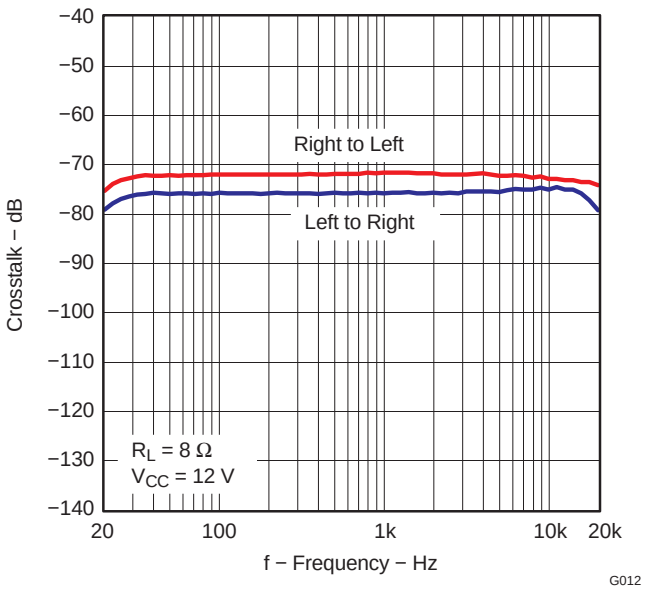


Figure 17.

CROSSTALK vs FREQUENCY

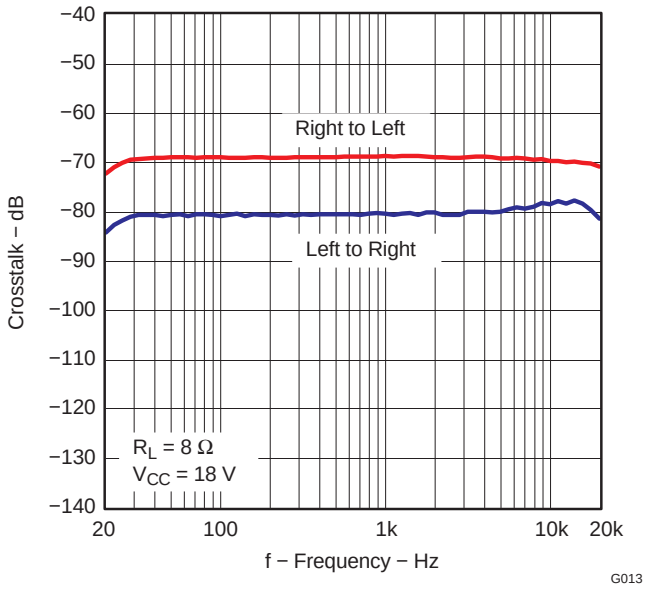


Figure 18.

CROSSTALK vs FREQUENCY

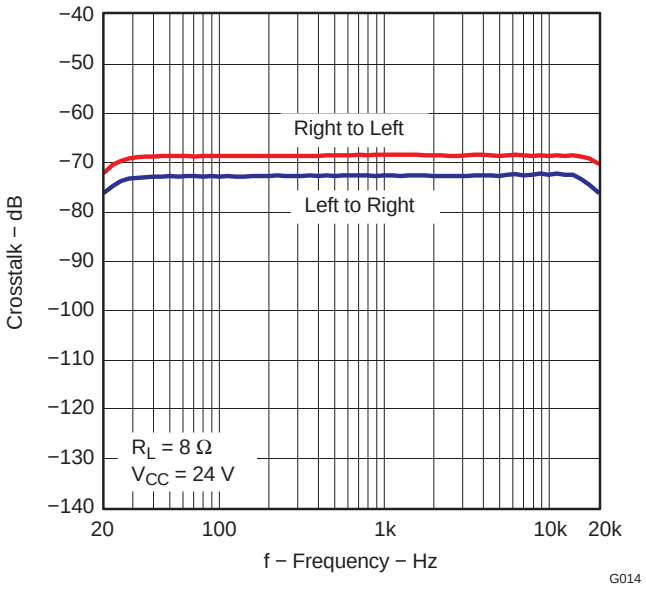


Figure 19.

TYPICAL CHARACTERISTICS, SE CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE (SE) vs FREQUENCY

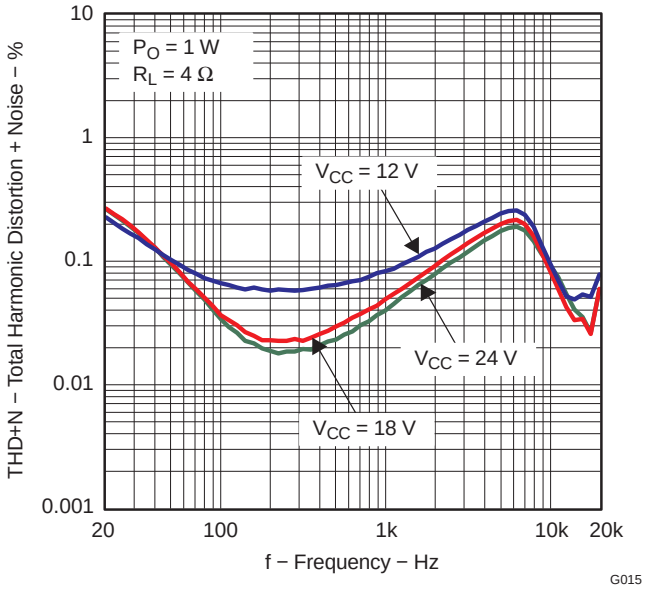


Figure 20.

TOTAL HARMONIC DISTORTION + NOISE (SE) vs OUTPUT POWER

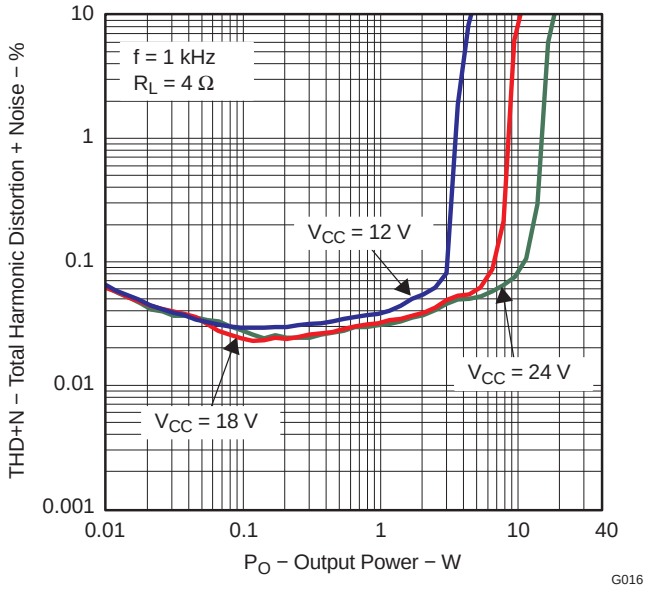


Figure 21.

EFFICIENCY vs OUTPUT POWER

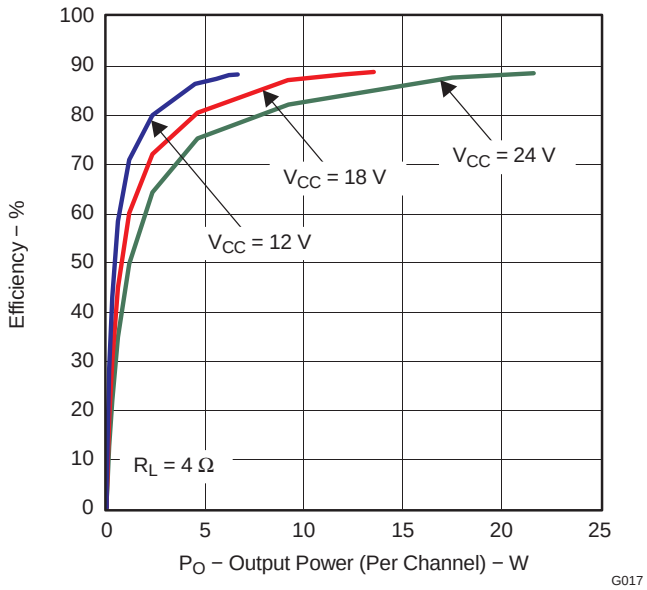


Figure 22.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

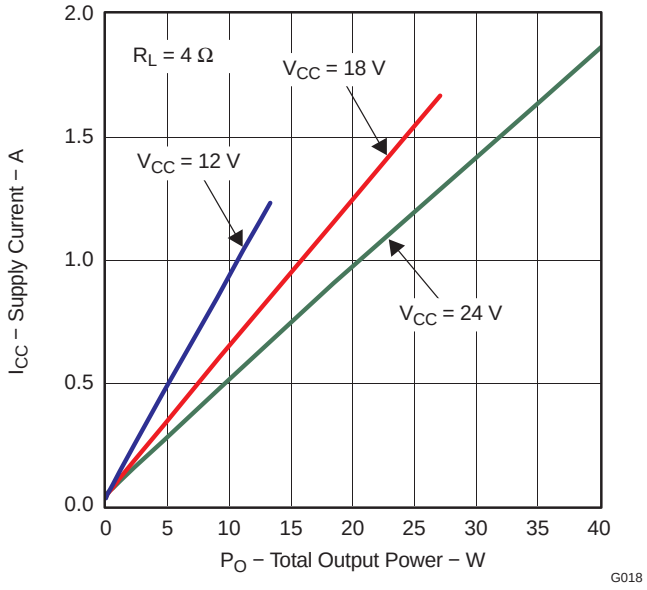


Figure 23.

TYPICAL CHARACTERISTICS, SE CONFIGURATION (continued)

OUTPUT POWER vs SUPPLY VOLTAGE

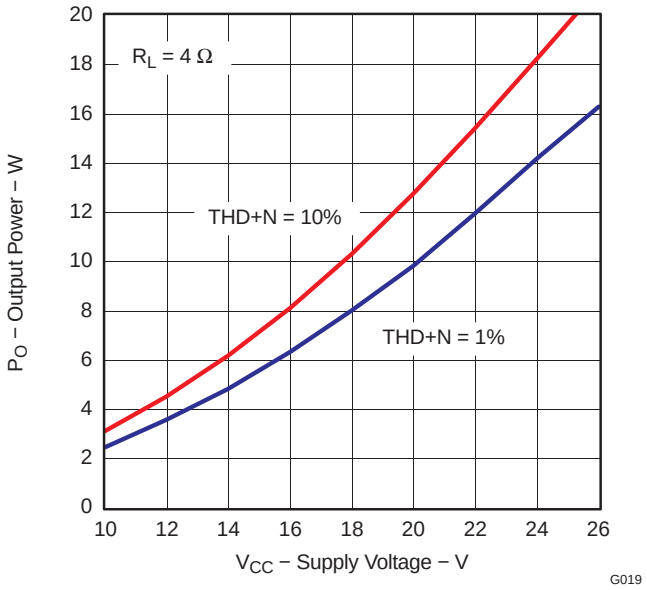


Figure 24.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

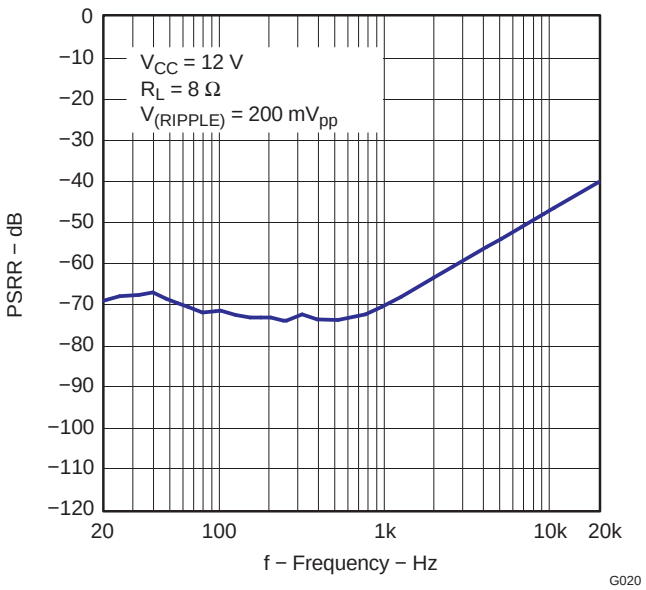


Figure 25.

DETAILED DESCRIPTION

POWER SUPPLY

The digital portion of the chip requires 3.3 V, and the power section operates from a variable range from 10 V to 26 V.

Clock, Auto Detection, and PLL

The TAS5704 DAP is a clock slave device. It accepts MCLK, SCLK, and LRCLK.

The TAS5704 checks to verify that SCLK is a specific value of 32-f_s, 48- f_s, or 64-f_s. The DAP only supports a 1 × f_s LRCLK. The timing relationship of these clocks to SDIN1 and SDIN2 is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to produce the internal clock.

The DAP can auto-detect and set the internal clock control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz or 192 kHz).

PWM SECTION

The DAP (digital audio processor) has four channels of high-performance digital PWM modulators that are designed to drive bridge-tied output H-bridge configurations with AD or BD modulation and single-ended output configurations with AD modulation.

The DAP uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction.

The PWM section accepts 24-bit PCM data from the DAP and outputs up to 4 PWM audio output channels.

The PWM section has individual channel dc blocking filters that are ALWAYS enabled. The filter cutoff frequency is less than 1 Hz.

SERIAL DATA INTERFACE

Serial data is input on SDIN1 and SDIN2. The PWM outputs are derived from SDIN1 and SDIN2. The TAS5704 DAP accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 18-, 20-, or 24-bit data in left-justified, right-justified, and I^2S serial data formats. See Table 1 for format control settings.

SERIAL INTERFACE CONTROL AND TIMING

I^2S Timing

I^2S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A system clock (SCLK) running at 32, 48, or 64 × f_s is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

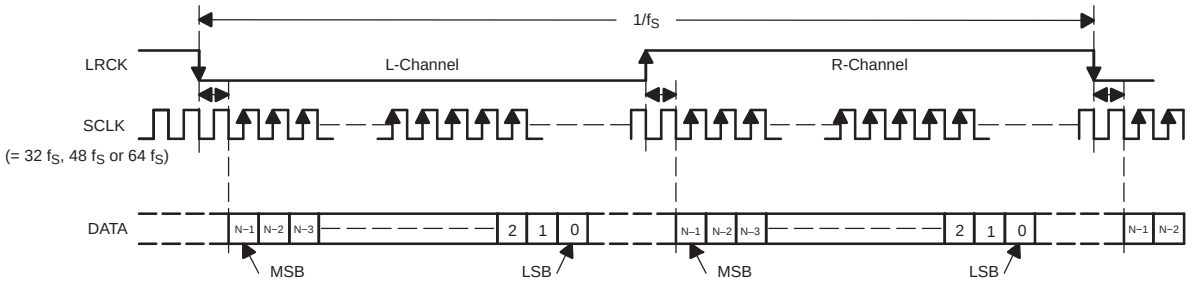


Figure 26. I^2S Format

Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_s is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

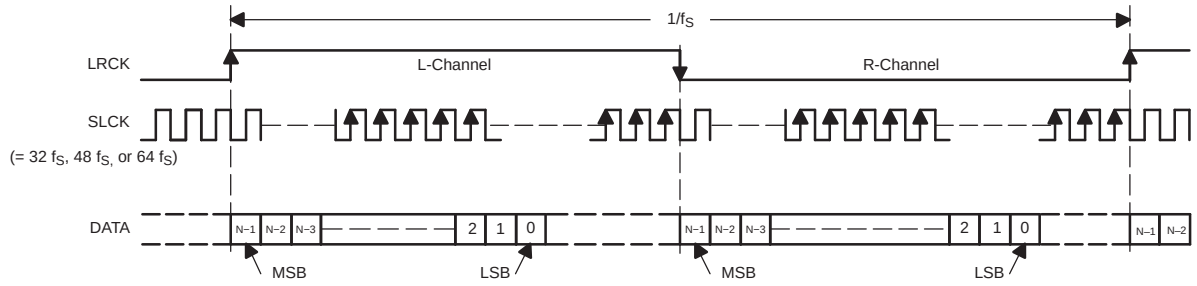


Figure 27. Left-Justified Format

Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_s is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused leading data bit positions.

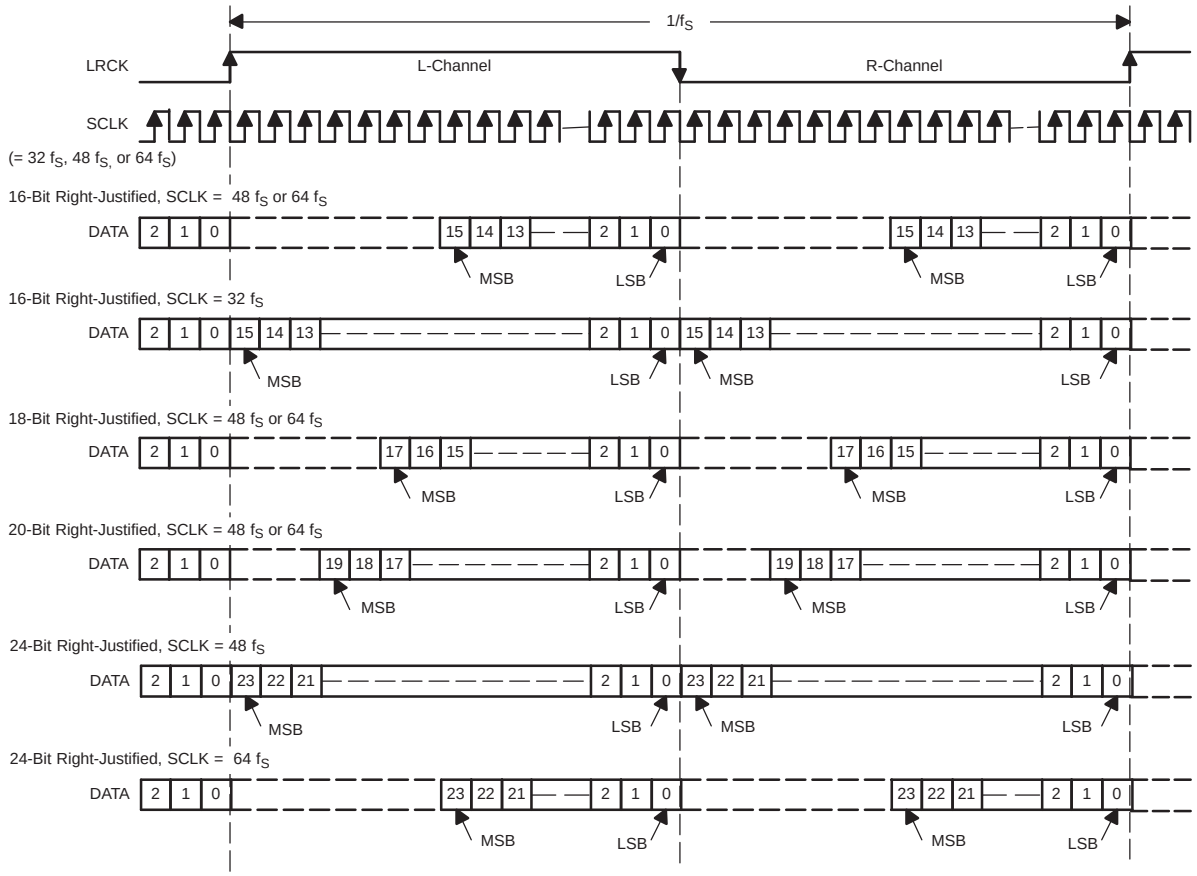


Figure 28. Right-Justified Format

Format Control

The digital data input format is selected via three external terminals (FORMAT0, FORMAT1, and FORMAT2). Table 1 lists the corresponding data format for SDIN1 and SDIN2. LRCLK and SCLK are shared clocks for SDIN1 and SDIN2. Changes to the FORMATx terminals are latched in immediately on a rising edge of RESET. Changes to the FORMATx terminals while RESET is high are not allowed.

Table 1. Format Control

FORMAT2	FORMAT1	FORMAT0	SERIAL DIGITAL DATA FORMAT
0	0	0	16-Bit right-justifed
0	0	1	18-Bit right-justified
0	1	0	20-Bit right-justified
0	1	1	24-Bit right-justified
1	0	0	16-, 24-Bit I^2S
1	0	1	16-, 24-Bit left-justified
1	1	0	Reserved. Setting is not allowed.
1	1	1	Reserved. Setting is not allowed.

Gain Control

The gain of the DAP is selected via two external gain pins (GAIN_0 and GAIN_1). Table 2 lists the corresponding channel gain (for ALL channels) for GAIN_0 and GAIN_1 settings. Individual channel gain is not possible. Changes to the GAIN_x terminals are latched in immediately on a rising edge of RESET. Changes to the GAIN_x terminals while RESET is high are not allowed.

Table 2. Gain Control

GAIN_1	GAIN_0	CHANNEL GAIN (dB)	OUTPUT VOLTAGE WITH FULL SCALE INPUT (V_{rms}) — BTL
0	0	-3	17.56
0	1	3	35.04 (1)
1	0	9	70.08 (1)
1	1	12	99.00 (1)

(1) Output clipped. See the calculation example in the Application section.

Output Configuration Control

The PWM outputs can be remapped to allow 2-ch, 2.1-ch, and 4-ch operation. Two terminals are used for this mapping, CONFIG_1 and CONFIG_2. Table 3 lists the output configurations that are supported. Changes to the CONFIG_x terminals are latched in immediately on a rising edge of RESET. Changes to the CONFIG_x terminals while RESET is high are not allowed.

Table 3. Output Configurations

CONFIG_2	CONFIG_1	OUTPUT CONFIGURATION
0	0	2-Ch Mode, BTL, AD modulation. SUB+/- is derived from the SDIN2 input (left channel). SUB+/- is AD modulation with SUB- equal to the compliment of SUB+.
0	1	2-Ch Mode, BTL, BD modulation. SUB+/- is derived from the SDIN2 input (left channel), and SUB+/- is BD PWM.
1	0	2.1-Ch Mode (2xSE outputs, 1xBTL output). AD modulation. No SUB+/- PWM output.
1	1	4-Ch Mode (4xSE outputs). AD modulation. No SUB+/- PWM output.

APPLICATION INFORMATION

CLOSED-LOOP POWER STAGE CHARACTERISTICS

The TAS5704 is PWM input power stage with a closed loop architecture. A feedback loop varies the PWM output duty cycle with changes in the supply voltage. This ensures that the output voltage (and output power) remain the same over transitions in the power supply.

Open-loop power stages have an output duty cycle that is equal to the input duty cycle. Since the duty cycle does NOT change to compensate for changes in the supply voltage, the output voltage (and power) change with supply voltage changes. This is undesirable effect that closed-loop architecture of the TAS5704 solves.

The single-ended (SE) gain of the TAS5704 is fixed, and specified below:

TAS5704 Gain = 0.13 / Modulation Level (Vrms/%)

Modulation level = fraction of full-scale modulation of the PWM signal at the input of the power stage.

TAS5704 (SE) Voltage Level (in Vrms) = 0.13 x Modulation Level

The bridge-tied (BTL) gain of the TAS5704 is equal to 2x the SE gain:

TAS5704 (BTL) Voltage Level (in Vrms) = 0.26 x Modulation Level

For a digital modulator like the TAS5704, the default maximum modulation limit is 97.7%. For a full scale input, the PWM output switches between 2.3% and 97.7%. This equates to a modulation level of 95.4% for a full scale input (0 dBFS).

For example, calculate the output voltage in RMS volts given a –20 dBFS signal to a digital modulator with a maximum modulation limit of 97.7% in a BTL output configuration:

TAS5704 Output Voltage = 0.1 (–20dB) x 0.26 (Gain) x 95.4 (Modulation Level)

= 2.48 Vrms

For shutdown and power-down, the $\overline{\text{PDN}}$ terminal should be cycled low for the “turn-off” time specified in the DC Electrical Characteristics table before PVCC falls below 10 V and DVDD/AVDD falls below 3 V. For SE mode, this is approximately 500ms. For BTL mode, the time is much faster, at 30ms. This ensures the best “pop” performance in the system.

POWER SUPPLIES

To allow simplified system design, the TAS5704 requires only a single supply (PVCC) for the the power blocks and a 3.3 V (DVDD/AVDD) supply for PWM input blocks. In addition, the high-side gate drive is provided by built-in bootstrap circuits requiring only an external capacitor for each half-bridge.

DVDD/AVDD must be applied at the same time or before PVCC is applied on power-up. For power-down, PVCC and DVDD/AVDD should remain active while the $\overline{\text{PDN}}$ terminal is cycled low and held low for at least the time specified for t_{OFF} in the Electrical Characteristics table.

In order for the bootstrap circuit to function properly, it is necessary to connect a small ceramic capacitor from each bootstrap pin (BS_) to the corresponding output pin (OUT_). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate drive.

DEVICE PROTECTION SYSTEM

The TAS5704 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overtemperature, overvoltage, and undervoltage.

PROTECTION MECHANISMS IN THE TAS5704

- SCP (short-circuit protection) protects against shorts across the load, to GND, and to PVCC.
- OTP turns off the device if $T_{junction}$ (typical) > 150°C.
- UVP turns off the device if PVCC (typical) < 8.4 V
- OVP turns off the device if PVCC (typical) > 27.5 V

A short-circuit condition can be detected also by an external controller. The VALID pin goes low in the event of a short circuit. The VALID pin can be monitored by an external μC. The TAS5704 initiates a back-end error sequence by itself to recover from the error, which involves settling VALID low for 300 ms and then retrying to check whether the short-circuit condition still exists.

RECOVERY FROM ERROR

- OTP turns on the device back when T_{die}(typical) < 135°C.
- UVP turns on the device if PVCC (typical) is > 8.5 V.
- OVP turns on the device if PVCC (typical) is < 27.2 V.
- SCP (short-circuit protection) turns on the device if the short-circuit is removed. See the Back-End Error section for the sequence.

SINGLE-ENDED OUTPUT CAPACITOR, C_O

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls of with decreasing frequency at a rate of 20 dB/decade. The cutoff frequency is determined by

$$f_c = 1/2\pi C_O Z_L \quad (1)$$

Table 4 shows some common component values and the associated cutoff frequencies:

Table 4. Common Filter Responses

SPEAKER IMPEDANCE (Ω)	C_{SE} – DC BLOCKING CAPACITOR (μF)		
	f_c = 60 Hz (–3 dB)	f_c = 40 Hz (–3 dB)	f_c = 20 Hz (–3 dB)
4	680	1000	2200
8	330	470	1000

OUTPUT FILTER AND FREQUENCY RESPONSE

For the best frequency response, a flat-passband output filter (second-order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the output pins. There are several possible configurations, depending on the speaker impedance and whether the output configuration is single-ended (SE) or bridge-tied load (BTL). Table 5 lists the recommended values for the filter components. It is important to use a high-quality capacitor in this application. A rating of at least X7R is required.

Table 5. Recommended Filter Output Components

OUTPUT CONFIGURATION	SPEAKER IMPEDANCE (Ω)	FILTER INDUCTOR (μH)	FILTER CAPACITOR (nF)
Single Ended (SE)	4	22	680
	8	47	390
Bridge Tied Load (BTL)	4	10	1500
	8	22	680

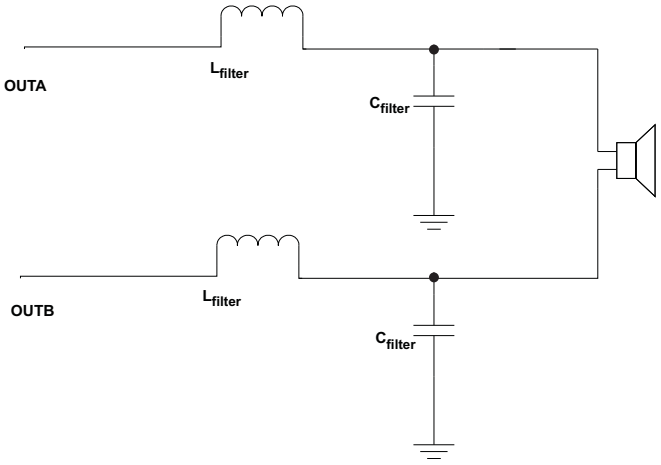


Figure 29. BTL Filter Configuration

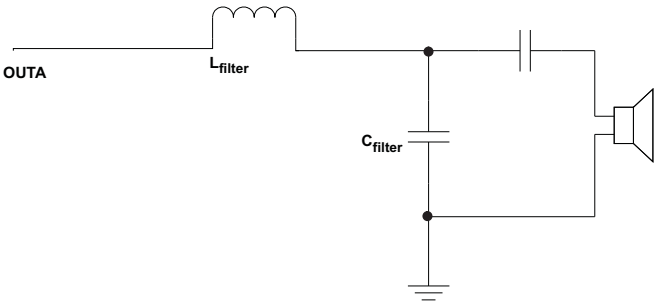


Figure 30. SE Filter Configuration

POWER-SUPPLY DECOUPLING, C_S

The TAS5704 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF to 1 μF, placed as close as possible to the device V_{CC} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220-μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220-μF or larger capacitor should be placed on each PVCC terminal. A 10-μF capacitor on the AVCC terminal is adequate. These capacitors must be properly derated for voltage and ripple-current rating to ensure reliability.

BOOTSTRAP CAPACITORS

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input.

The bootstrap capacitors connected between the BSx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP CAPACITOR

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, one internal regulator clamps the gate voltage. One 1-μF capacitor must be connected from each VCLAMP (terminal) to ground and must be rated for at least 16 V. The voltages at the VCLAMP terminal may vary with V_{CC} and may not be used for powering any other circuitry.

VBYP CAPACITOR SELECTION

The scaled supply reference (BYPASS) nominally provides an AVCC/8 internal bias for the preamplifier stages. The external capacitor for this reference (C_{BYP}) is a critical component and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts. The start up time is proportional to 0.5 s per microfarad in single-ended mode (SE/$\overline{\text{BTL}}$ = DVDD). Thus, the recommended 1-μF capacitor results in a start-up time of approximately 500 ms (SE/$\overline{\text{BTL}}$ = DVDD). The second function is to reduce noise produced by the power supply caused by coupling with the output drive signal. This noise could result in degraded power-supply rejection and THD+N.

The circuit is designed for a C_{BYP} value of 1 μF for best pop performance. The input capacitors should have the same value. A ceramic or tantalum low-ESR capacitor is recommended.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TAS5704 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 0.1-μF decoupling capacitors should be placed as close to the PVCC, VR_DIG, and AVCC terminals as possible. The BYPASS capacitor and VCLAMP_XX capacitors should also be placed as close to the device as possible. Large (220-μF or greater) bulk power-supply decoupling capacitors should be placed near the TAS5704 on the PVCCx terminals. For single-ended operation, a 220 μF capacitor should be placed on each PVCC pin. For Bridge-tied operation, a single 220 μF, capacitor can be shared between A and B or C and D.
- Grounding—The AVCC decoupling capacitor and BYPASS capacitor should each be grounded to analog ground (AGND). The PVCCx decoupling capacitors and VCLAMP_xx capacitors should each be grounded to power ground (PGND). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TAS5704.
- Output filter—The reconstruction LC filter should be placed as close to the output terminals as possible for the best EMI performance. The capacitors should be grounded to power ground.
- Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance, audio performance, and optimal reliability. The dimensions of the thermal pad and thermal land are described in the mechanical section at the back of the data sheet. See TI Technical Briefs SLMA002 and SLOA120 for more information about using the thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TAS5704 Evaluation Module (TAS5704EVM) User Manual, (SLOU189). Both the EVM user manual and the thermal pad application note are available on the TI Web site at http://www.ti.com.

BASIC MEASUREMENT SYSTEM

This section focuses on methods that use the basic equipment listed below:

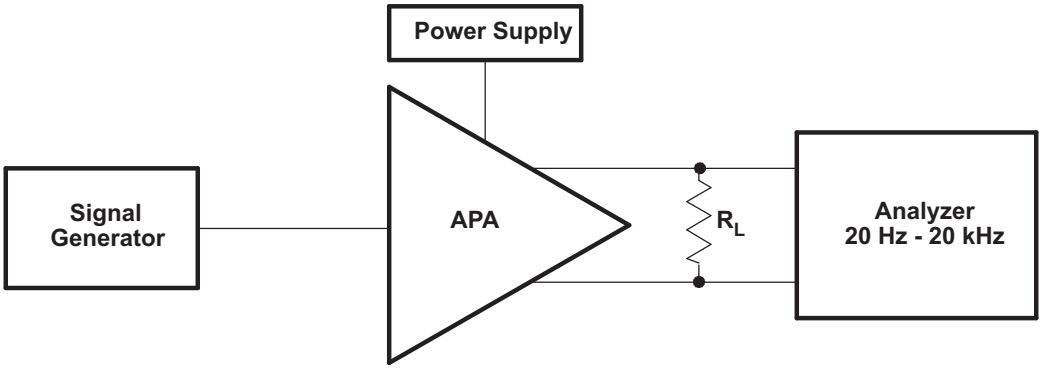
- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

Figure 31 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the audio power amplifier (APA) output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two™ audio measurement system (AP-II) by Audio Precision™ includes the signal generator and analyzer in one package.

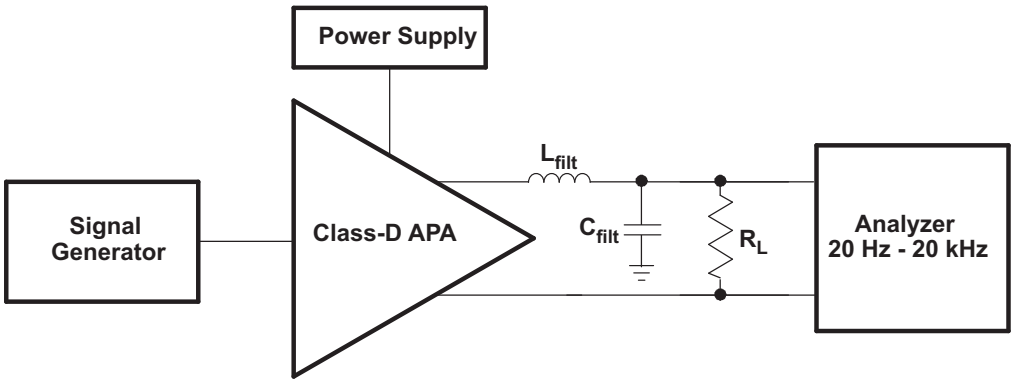
The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer input impedance should be high. The output resistance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 31(a) shows a class-AB amplifier system. It takes an analog signal input and produces an analog signal output. This amplifier circuit can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 31(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.



(a) Basic Class-AB



(b) Traditional Class-D

Figure 31. Audio Measurement Systems

SE INPUT AND SE OUTPUT (TAS5704 Stereo Configuration)

The SE input and output configuration is used with class-AB amplifiers. A block diagram of a fully SE measurement circuit is shown in Figure 32. SE inputs normally have one input pin per channel. In some cases, two pins are present; one is the signal and the other is ground. SE outputs have one pin driving a load through an output ac-coupling capacitor and the other end of the load is tied to ground. SE inputs and outputs are considered to be unbalanced, meaning one end is tied to ground and the other to an amplifier input/output.

The generator should have unbalanced outputs, and the signal should be referenced to the generator ground for best results. Unbalanced or balanced outputs can be used when floating, but they may create a ground loop that affects the measurement accuracy. The analyzer should have balanced inputs to cancel out any common-mode noise in the measurement.

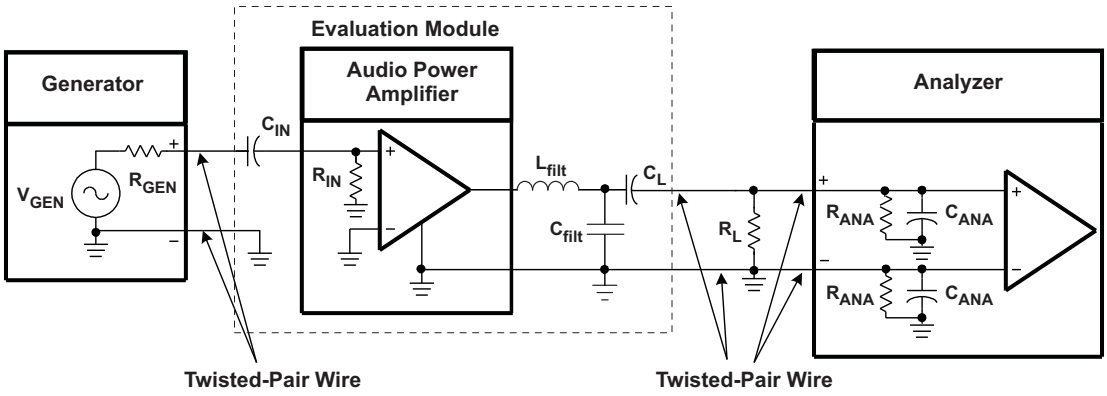


Figure 32. SE Input—SE Output Measurement Circuit

The following general rules should be followed when connecting to APAs with SE inputs and outputs:

- Use an unbalanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 6).

DIFFERENTIAL INPUT AND BTL OUTPUT (TAS5704 Mono Configuration)

Many of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied-load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180° out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc-blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 33. The differential input is a balanced input, meaning the positive (+) and negative (–) pins have the same impedance to ground. Similarly, the SE output equates to a balanced output.

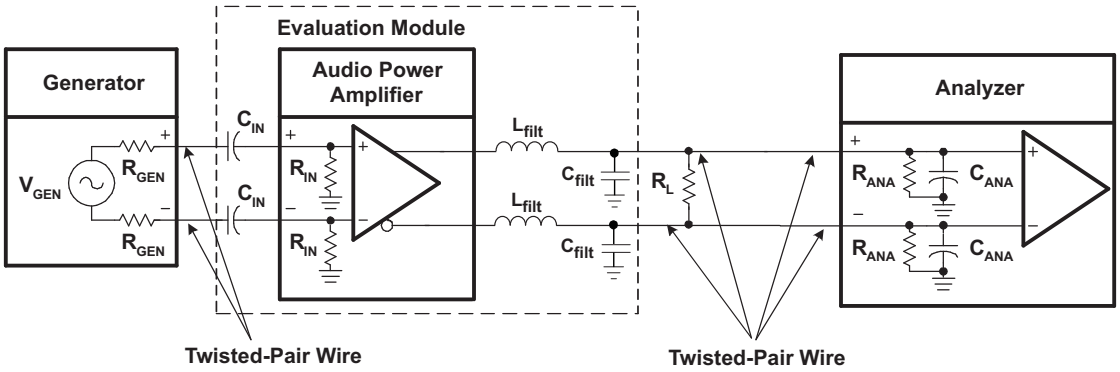


Figure 33. Differential Input, BTL Output Measurement Circuit

The generator should have balanced outputs, and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common-mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure that the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 6).

Table 6 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch (30.5-cm)-long wire with a 20-kHz sine-wave signal at 25°C.

Table 6. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L(Ω)	AWG Size		DC POWER LOSS (mW)		AC POWER LOSS (mW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8	3.7	8.5
1	8	22	28	2	8	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

REVISION HISTORY

Changes from Original (March 2008) to Revision A	Page
• Replaced the Dissipation Ratings table with the Thermal Information table	8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5704PAP	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5704
TAS5704PAP.A	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5704
TAS5704PAP.B	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5704
TAS5704PAPR	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5704
TAS5704PAPR.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5704
TAS5704PAPR.B	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5704

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

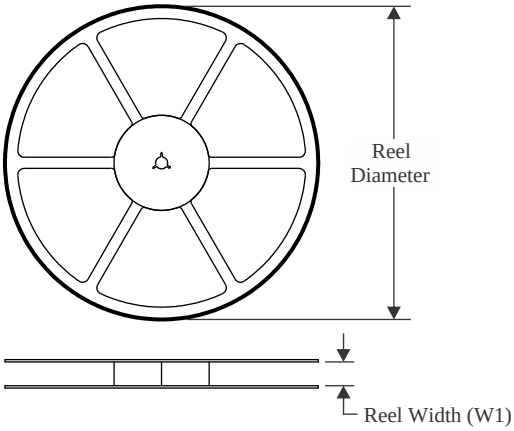
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

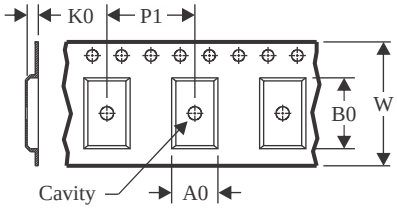
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

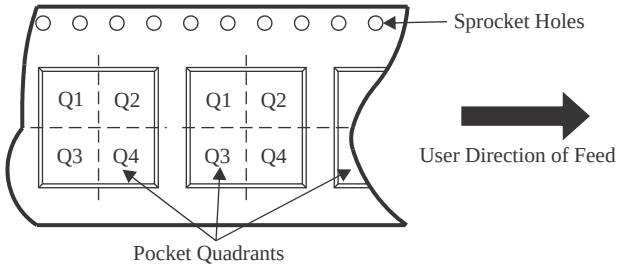


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

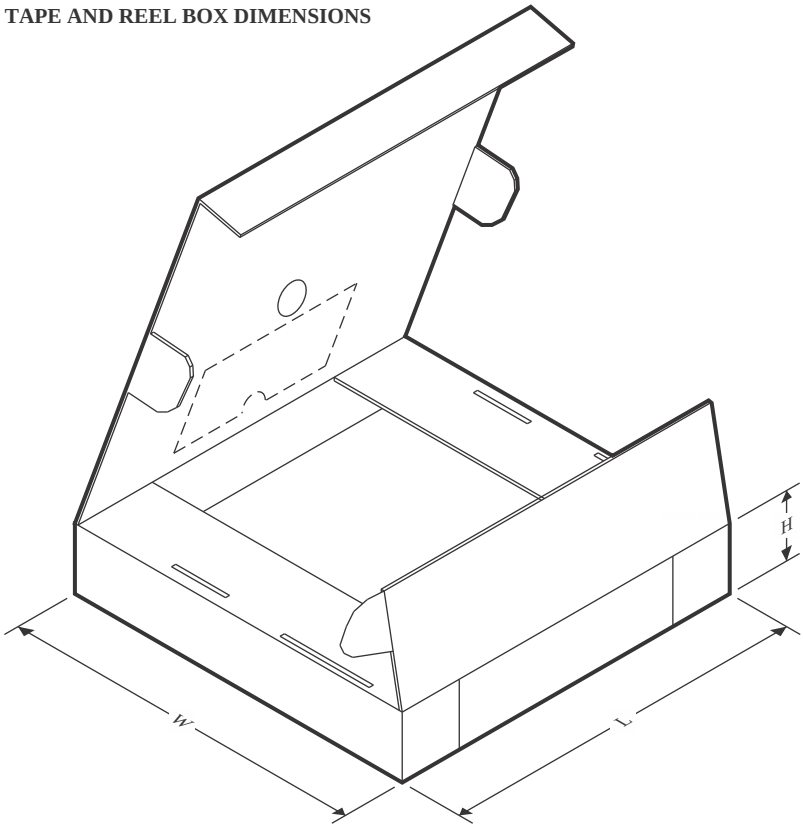
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5704PAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

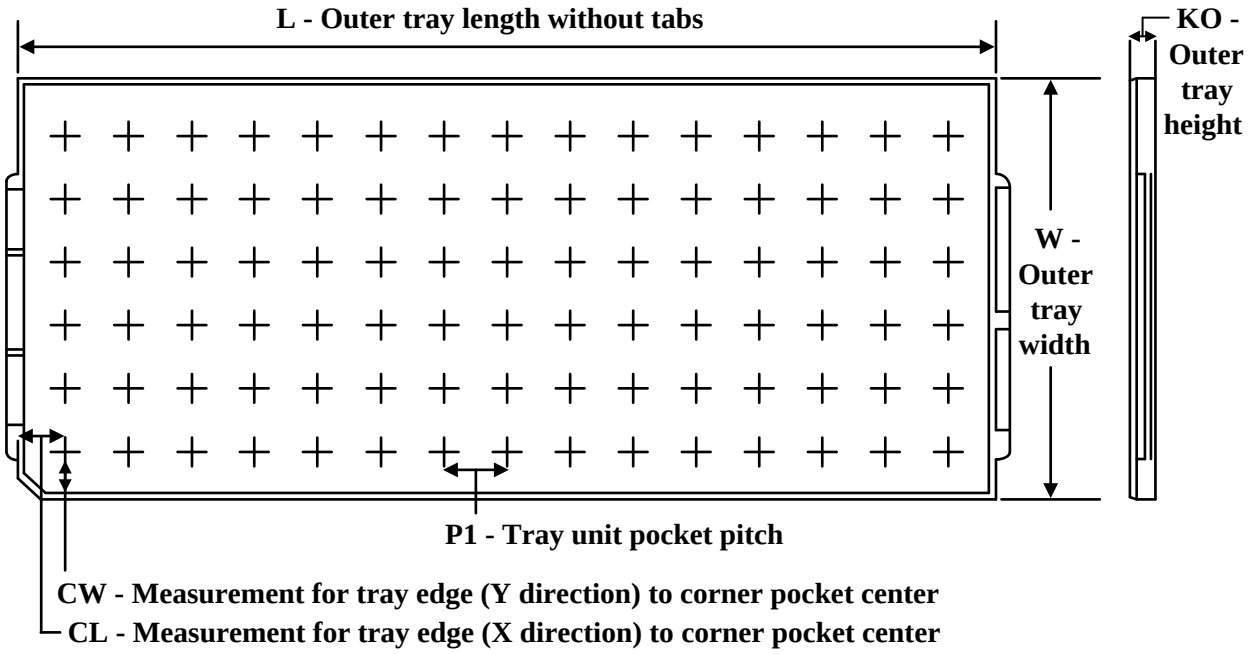
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5704PAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TAS5704PAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TAS5704PAP.A	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TAS5704PAP.B	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

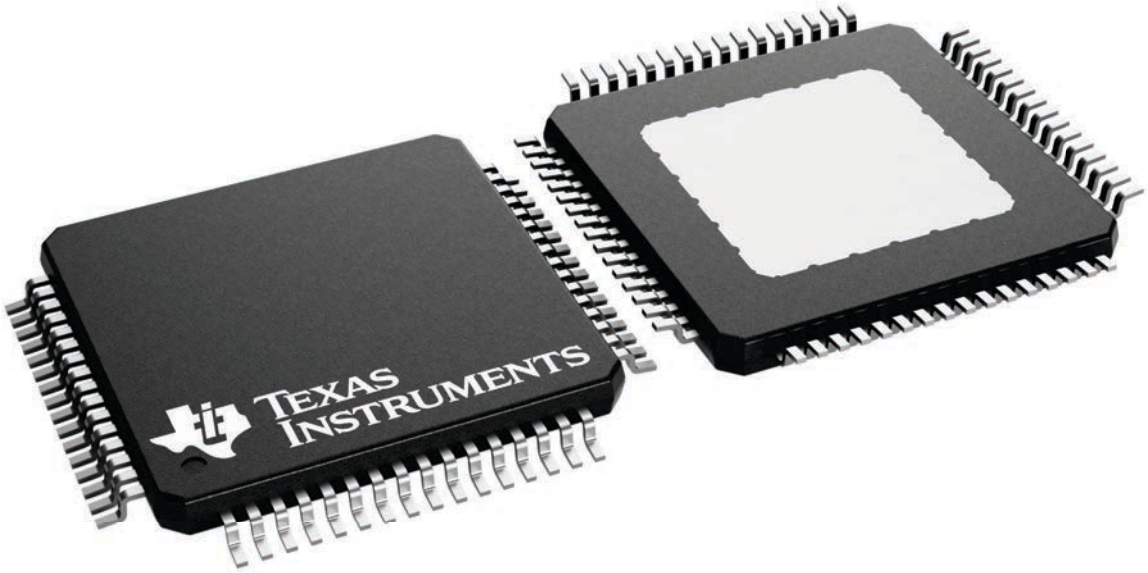
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



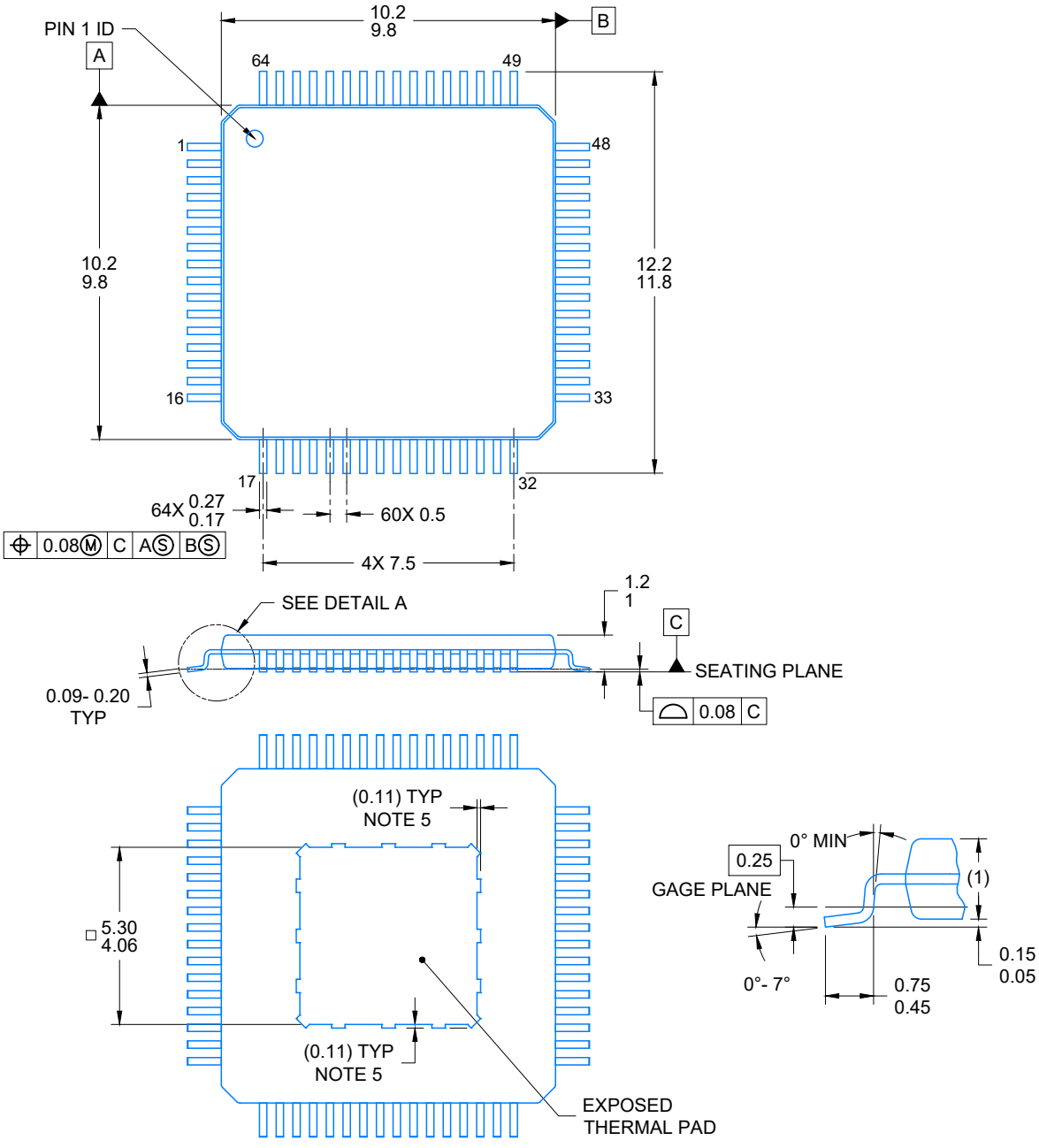
4226442/A

PACKAGE OUTLINE

PAP0064N

HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

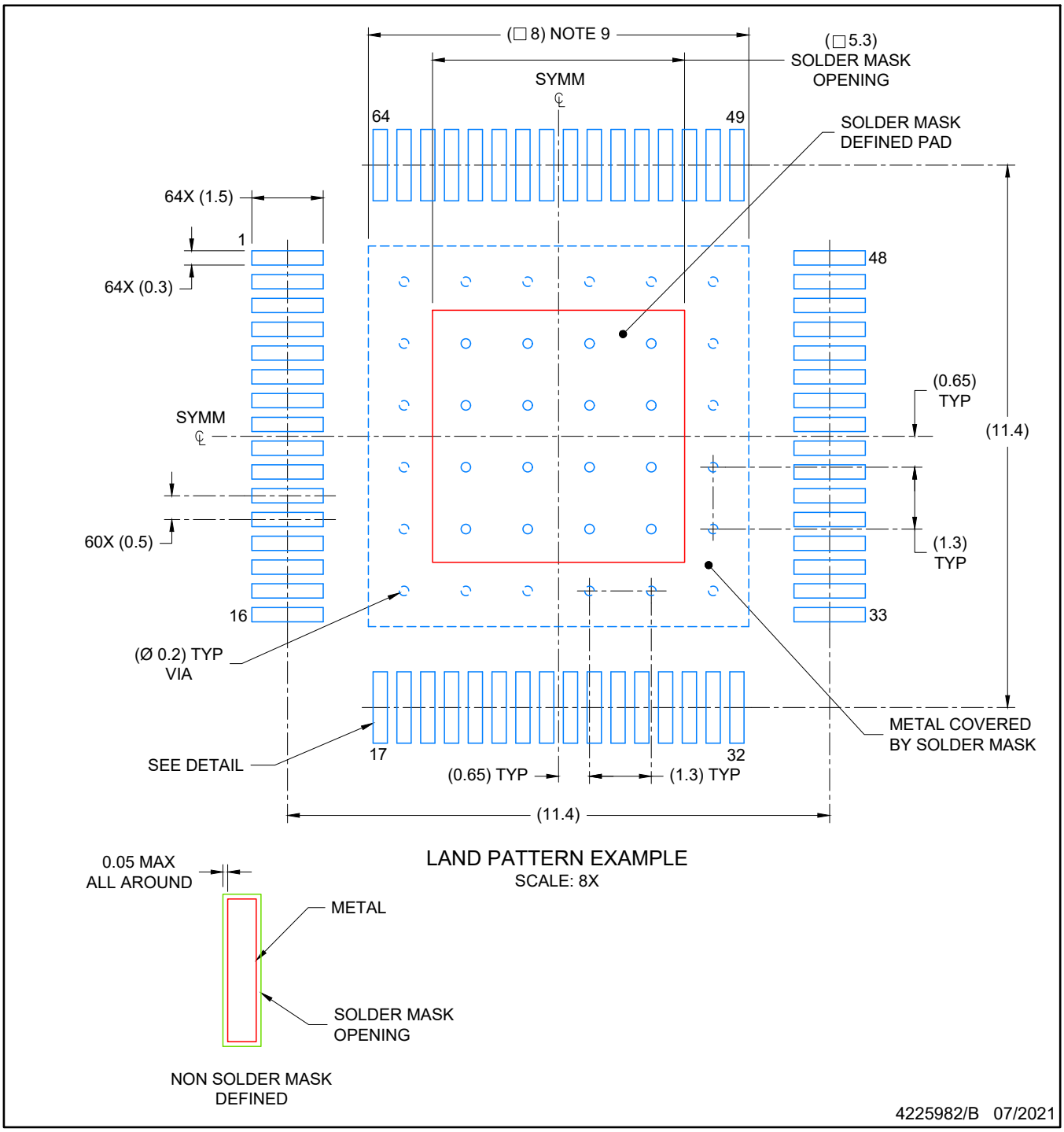


4225982/B 07/2021

NOTES:

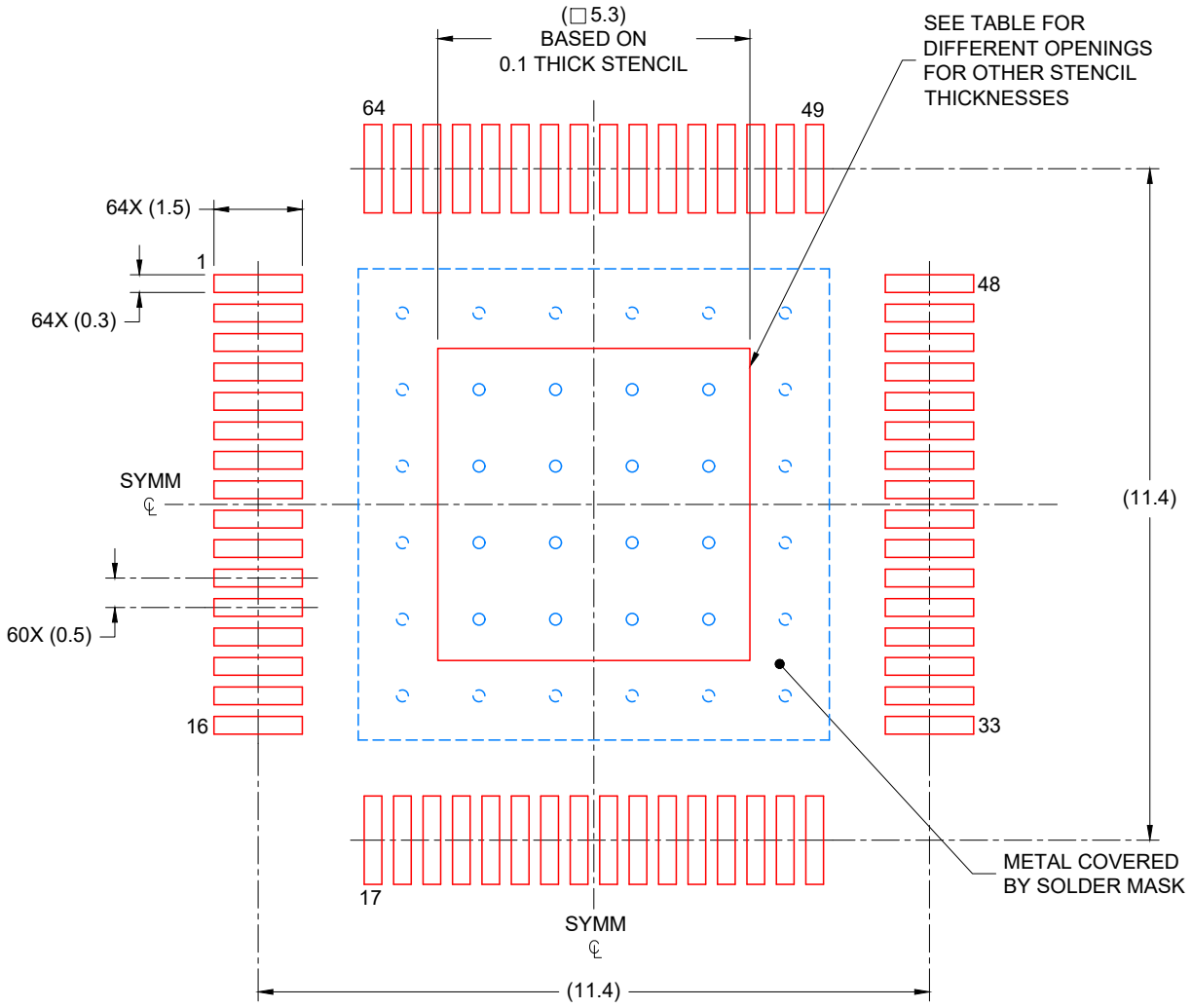
PowerPAD is a trademark of Texas Instruments

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Strap features may not be present.
6. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED COVERAGE BY AREA
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.3X5.3 (SHOWN)
0.127	4.44 X 4.44
0.152	4.06 X 4.06
0.178	3.75 X 3.75

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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