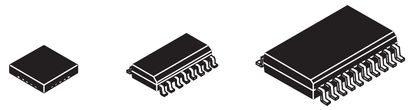


LOW-POWER DISSIPATION ADSL LINE DRIVER

FEATURES

- **Low-Power Dissipation Increases ADSL Line Card Density**
- **Low THD of -88 dBc (100 Ω, 1 MHz)**
- **Low MTPR Driving +20 dBm on the Line**
  - **-76 dBc With High Bias Setting**
  - **-74 dBc With Low Bias Setting**
- **Wide Output Swing of 44 V_{PP} Differential Into a 200-Ω Differential Load (V_{CC} = ±12 V)**
- **High Output Current of 600 mA (Typ)**
- **Wide Supply Voltage Range of ±5 V to ±15 V**
- **Pin Compatible with EL1503C and EL1508C**
  - **Multiple Package Options**
- **Multiple Power Control Modes**
  - **11 mA/ch Full Bias Mode**
  - **7.5 mA/ch Mid Bias Mode**
  - **4 mA/ch Low Bias Mode**
  - **0.25 mA/ch Shutdown Mode**
  - **I_{ADJ} Pin for User Controlled Bias Current**
  - **Stable Operation Down to 1.8 mA/ch**
- **Low Noise for Increased Receiver Sensitivity**
  - **3.2 nV/$\sqrt{Hz}$ Voltage Noise**
  - **1.5 pA/$\sqrt{Hz}$ Noninverting Current Noise**
  - **10 pA/$\sqrt{Hz}$ Inverting Current Noise**

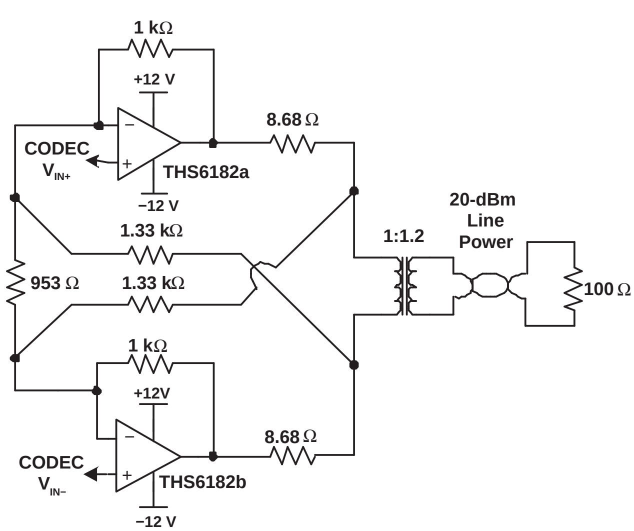
APPLICATIONS

- **Ideal for Full Rate ADSL Applications**

DESCRIPTION

The THS6182 is a current feedback differential line driver ideal for full rate ADSL systems. Its extremely low-power dissipation is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique architecture of the THS6182 allows the quiescent current to be much lower than existing line drivers while still achieving high linearity without the need for excess open loop gain. Fixed multiple bias settings of the amplifiers allow for enhanced power savings for line lengths where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, an I_{ADJ} pin is available to further lower the bias currents while maintaining stable operation with as little as 1.8 mA per channel. The wide output swing of 44 V_{PP} differentially with ±12-V power supplies allows for more dynamic headroom, keeping distortion at a minimum. With a low 3.2 nV/$\sqrt{Hz}$ voltage noise coupled with a low 10 pA/$\sqrt{Hz}$ inverting current noise, the THS6182 increases the sensitivity of the receive signals, allowing for better margins and reach.

TYPICAL ADSL CO-LINE DRIVER CIRCUIT USING ACTIVE IMPEDANCE



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PRODUCT	PACKAGE(1)	PACKAGE CODE	SYMBOL	ORDER NUMBER	TRANSPORT MEDIA
THS6182RHF	Leadless 24-pin 4, mm x 5, mm PowerPAD™	RHF-24	6182	THS6182RHFR	Tape and reel (3000 devices)
				THS6182RHFT	Tape and reel (250 devices)
THS6182D	SOIC-16	D-16	THS6182	THS6182D	Tube (40 devices)
				THS6832DR	Tape and reel (2500 devices)
THS6182DW	SOIC-20	DW-20	THS6182	THS6182DW	Tube (25 devices)
				THS6182DWR	Tape and reel (2000 devices)
THS6182DWP	SOIC-20 PowerPAD	DWP-20	THS6182	THS6182DWP	Tube (25 devices)
				THS6182DWPR	Tape and reel (2000 devices)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	PowerPAD SOLDERED(2) θ_{JA}	PowerPAD NOT SOLDERED(3) θ_{JC}	θ_{JC}
RHF-24(2)	32°C/W	74°C/W	1.7°C/W
D-16	--	62.9°C/W	25.7°C/W
DW-20	--	45.4°C/W	16.4°C/W
DWP-20(2)	21.5°C/W	43.9°C/W	0.37°C/W

(1) θ_{JA} values shown are typical for standard test PCBs only.
(2) For high-power dissipation applications, use of the PowerPAD package with the PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage and/or reduce the lifetime the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.
(3) Use of packages without the PowerPAD or not soldering the PowerPAD to the PCB, should be limited to low-power dissipation applications.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
$V_{CC+}$to V_{CC-}	Supply voltage	Dual supply	±5	±12	±15	V
		Single supply	10	24	30	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

ELECTRICAL		THS6132
V_{CC}	Supply voltage	±16.5 V
V_I	Input voltage	$\pm V_{CC}$
I_O	Output current	1000 mA
V_{IO}	Differential input voltage	±2 V
THERMAL		
T_J	Maximum junction temperature, any condition	150°C
	Maximum junction temperature, continuous operation, long term reliability [2]	125°C
T_{stg}	Storage temperature	65°C to 150°C
ESD		
ESD ratings	HBM	2000 V
	CDM	1500 V
	MM	200 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those ispecified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 kΩ, Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE/DISTORTION PERFORMANCE								
MTPR	Multitone power ratio		Gain = +9.5, 163 kHz to 1.1 MHz DMT, +20 dBm Line Power, See Figure 1 for circuit			-76		dBc
	Receive band spill-over		Gain =+5, 25 kHz to 138 kHz with MTPR signal applied, See Figure 1 for circuit			-95		dBc
HD	Harmonic distortion, $V_{O(PP)}$ = 2 V f = 1 MHz		2nd harmonic	Differential load = 200 Ω		-88		dBc
				Differential load = 50 Ω		-70		
			3rd harmonic	Differential load = 200 Ω		-107		dBc
				Differential load = 50 Ω		-84		
V_n	Input voltage noise		V_{CC} = ±5 V, ±12 V, ±15 V, f = 100 kHz			3.2		$nV/\sqrt{Hz}$
I_n	Input current noise	+Input	V_{CC} = ±5 V, ±12 V, ±15 V, f = 100 kHz			1.5		$pA/\sqrt{Hz}$
		-Input				10		
	Crosstalk		f = 1 MHz, $V_{O(PP)}$ = 2 V, V_{CC} = ±5 V, ±12 V, ±15 V	R_L = 100 Ω		-65		dBc
				R_L = 25 Ω		-60		dBc

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 kΩ, Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS							
V_O	Single-ended output voltage swing	V_{CC} = ±5 V	R_L = 100 Ω	±3.9	±4.1		V
			R_L = 25 Ω	±3.7	±3.9		
		V_{CC} = ±12 V	R_L = 100 Ω	±10.7	±11		V
			R_L = 25 Ω	±10	±10.6		
		V_{CC} = ±15 V	R_L = 100 Ω	±13.5	±13.9		V
			R_L = 25 Ω	±12.7	±13.4		
I_O	Output current (1)	R_L = 5 Ω	V_{CC} = ±5 V	±350	±400		mA
		R_L = 10 Ω	V_{CC} = ±12 V	±450	±600		
			V_{CC} = ±15 V	±450	±600		
$I_{(SC)}$	Short-circuit current(1)	R_L = 1 Ω	V_{CC} = ±12 V		1000		mA
	Output resistance	Open-loop			6		Ω
	Output resistance—terminate mode	f = 1 MHz,	Gain = +10		0.05		Ω
	Output resistance—shutdown mode	f = 1 MHz,	Open-loop		8.5		kΩ
POWER SUPPLY							
V_{CC}	Operating range	Dual supply		±4	±12	±16.5	V
		Single supply		8	24	33	
I_{CC}	Quiescent current (each driver)(2) Full-bias mode (Bias-1 = 0, Bias-2 = 0) (Trimmed with V_{CC} = ±12 V at 25°C)	V_{CC} = ± 5 V	T_A = 25°C		9.7	10.7	mA
			T_A = full range			11.7	
		V_{CC} = ± 12 V	T_A = 25°C		11	12	mA
			T_A = full range			12.5	
		V_{CC} = ±15 V	T_A = 25°C		11.5	12.5	mA
			T_A = full range			13	
	Quiescent current (each driver) Variable bias modes, V_{CC} = ±12 V	Mid; Bias-1 - 1, Bias-2 = 0			7.5	8.5	mA
		Low; Bias-1 = 0, Bias-2 = 1			4	5	
		Shutdown; Bias-1 = 1, Bias-2 = 1			0.25	0.9	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V, ΔV_{CC} = ±0.5 V	T_A = 25°C	-50	-56		dB
			T_A = full range	-47			
		V_{CC} = ±12 V, ±15 V, ΔV_{CC} = ±1 V	T_A = 25°C	-56	-60		
			T_A = full range	-53			
DYNAMIC PERFORMANCE							
BW	Single-ended small-signal bandwidth (-3 dB), V_O = 0.1 Vrms	R_L = 100 Ω	Gain = +1, RF = 1.2 kΩ		100		MHz
			Gain = +2, RF = 1 kΩ		80		
			Gain = +5, RF = 1 kΩ		35		
			Gain = +10, RF = 1 kΩ		20		
		R_L = 25 Ω	Gain = +1, RF = 1.5 kΩ		65		MHz
			Gain = +2, RF = 1 kΩ		60		
			Gain = +5, RF = 1 kΩ		40		
			Gain = +10, RF = 1 kΩ		22		
SR	Single-ended slew rate (3)	V_O = 10 V_{PP},	Gain = +5		450		V/µs

(1) A heatsink is required to keep the junction temperature below absolute maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.
(2) Approximately 0.5 mA (total) flows from V_{CC+} to GND for internal logic control bias.
(3) Slew rate is defined from the 25% to the 75% output levels.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, R_F = 2 kΩ, Gain = +5, I_{ADJ} = Bias1 = Bias2 = 0 V, R_L = 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
V_{OS}	Input offset voltage	V_{CC} = ±5 V, ±12 V, ±15 V	T_A = 25°C		1	20	mV
			T_A = full range			25	
	Differential offset voltage		T_A = 25°C		0.5	10	
			T_A = full range			15	
	Offset drift		T_A = full range		50		µV/°C
I_{IB}	-Input bias current	V_{CC} = ±5 V, ±12 V, ±15 V	T_A = 25°C		8	15	µA
			T_A = full range			20	
	+Input bias current		T_A = 25°C		8	15	
			T_A = full range			20	
Z_{OL}	Open loop transimpedance	R_L = 1 kΩ, V_{CC} = ±12 V, ±15 V			900		kΩ
INPUT CHARACTERISTICS							
V_{ICR}	Input common-mode voltage range	V_{CC} = ±5 V	T_A = 25°C	±2.7	±3		V
			T_A = full range	±2.6			
		V_{CC} = ±12 V	T_A = 25°C	±9.5	±9.8		V
			T_A = full range	±±9.3			
		V_{CC} = ±15 V	T_A = 25°C	±12.4	±12.7		V
			T_A = full range	±12.1			
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V, ±12 V, ±15 V	T_A = 25°C	48	54		dB
			T_A = full range	44			
R_I	Input resistance	+Input			800		kΩ
		-Input			30		Ω
C_i	Input capacitance				1.7		pF
LOGIC CONTROL CHARACTERISTICS							
V_{IH}	Bias pin voltage for logic 1	Relative to GND pin voltage		2			V
V_{IL}	Bias pin voltage for logic 0					0.8	
I_{IH}	Bias pin current for logic 1	V_{IH} = 3.3 V, GND = 0 V			4	30	µA
I_{IL}	Bias pin current for logic 0	V_{IL} = 0.5 V, GND = 0 V			1	10	µA
	Transition time, logic 0 to logic 1 (4)				1		µs
	Transition time, logic 1 to logic 0 (4)				1		µs

(4) Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final value.

LOGIC TABLE (1) (2)

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers ON with lowest distortion possible (default state)
1	0	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
0	1	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance
1	1	Shutdown mode	Amplifiers OFF and output has high impedance

(1) The default state for all logic pins is a logic zero (0).
(2) The GND pin useable range is from V_{CC-} to (V_{CC+} - 4 V).

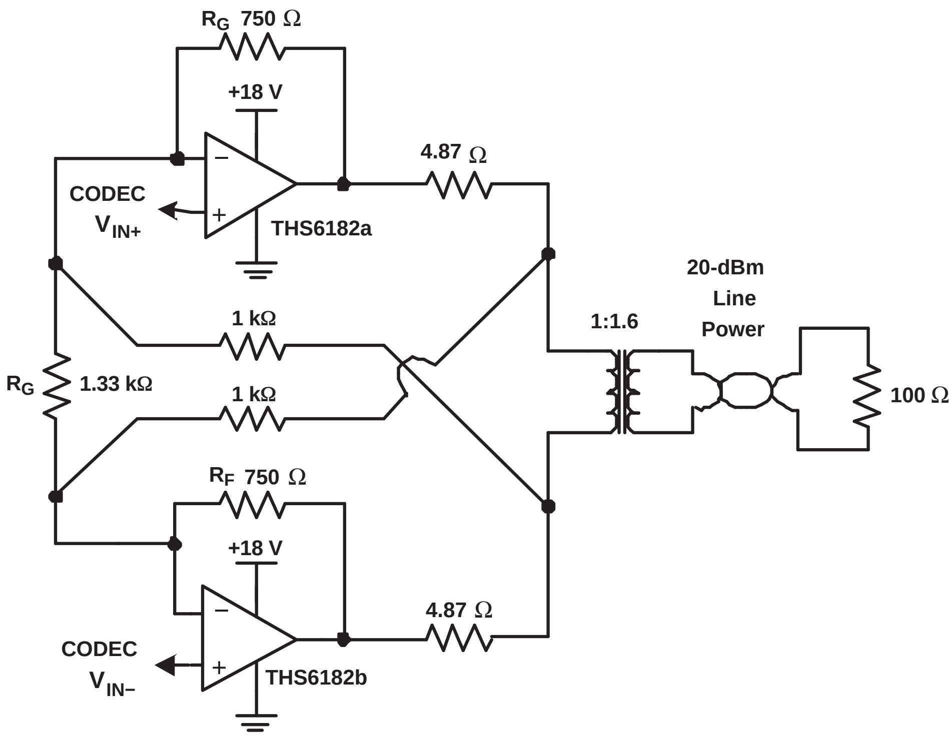
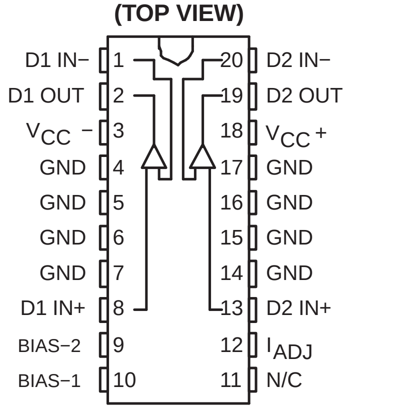


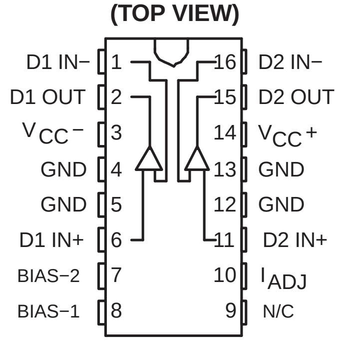
Figure 1. Single-Supply ADSL CO Line Driver Circuit Utilizing Active Impedance (SF = 4)

PIN ASSIGNMENTS

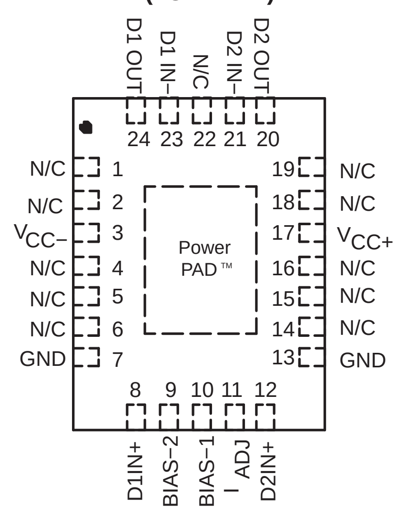
THS6182
SOIC−20 (DW) AND
SOIC−20 PowerPAD™ (DWP) PACKAGES
(TOP VIEW)



THS6182
SOIC−16 (D) PACKAGE
(TOP VIEW)



THS6182
Leadless 24−pin PowerPAD™
4 mm X 5 mm (RHF) PACKAGE
(TOP VIEW)



A. The PowerPAD is electrically isolated from all active circuitry and pins. Connection of the PowerPAD to the PCB ground plane is highly recommended, although not required, as this plane is typically the largest copper plane on a PCB. The thermal performance will be better with a large copper plane than a small one.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage headroom	vs Output current	2
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Total quiescent current		5
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Overdrive recovery		10
Power supply rejection ratio	vs Frequency	11
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Slew rate	vs Output voltage	38
Closed-loop output impedance	vs Frequency	39
Quiescent current	vs Supply voltage	40
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2nd Harmonic distribution	vs Frequency	45-52
3rd Harmonic distribution	vs Frequency	53-60
2nd Harmonic distribution	vs Output voltage	61-64
3rd Harmonic distribution	vs Output voltage	65-68

OUTPUT VOLTAGE HEADROOM
vs
OUTPUT CURRENT

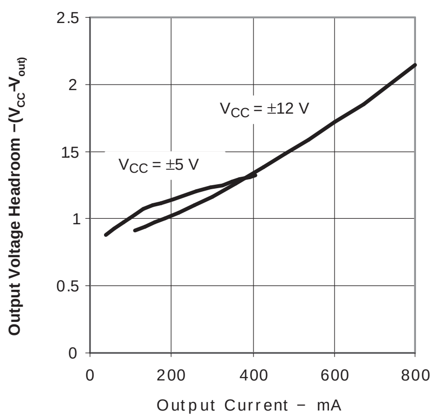


Figure 2.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

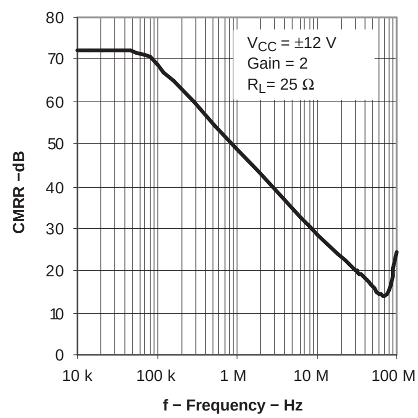


Figure 3.

CROSSTALK
vs
FREQUENCY

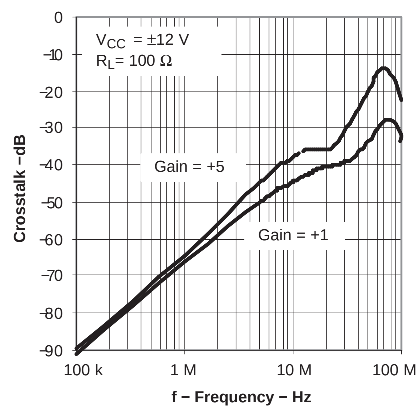


Figure 4.

TOTAL QUIESCENT CURRENT

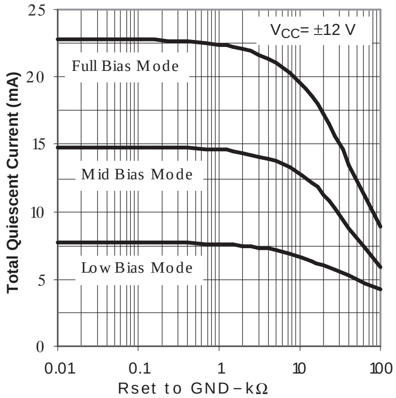


Figure 5.

LARGE SIGNAL OUTPUT AMPLITUDE vs FREQUENCY

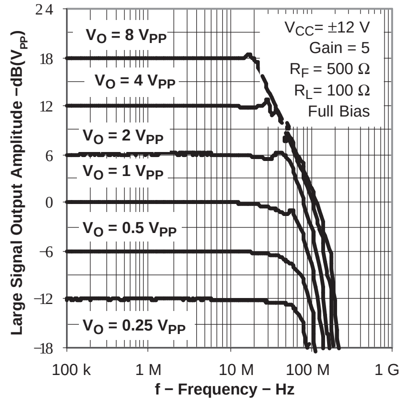


Figure 6.

LARGE SIGNAL OUTPUT AMPLITUDE vs FREQUENCY

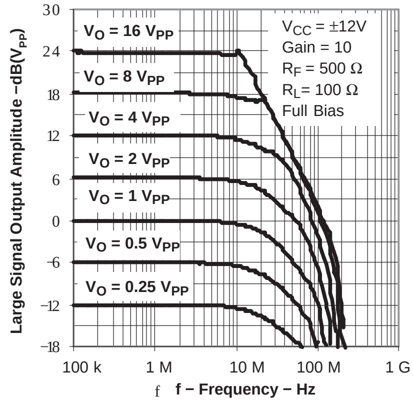


Figure 7.

LARGE SIGNAL OUTPUT AMPLITUDE vs FREQUENCY

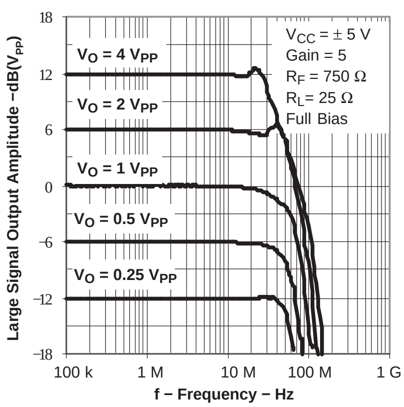


Figure 8.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

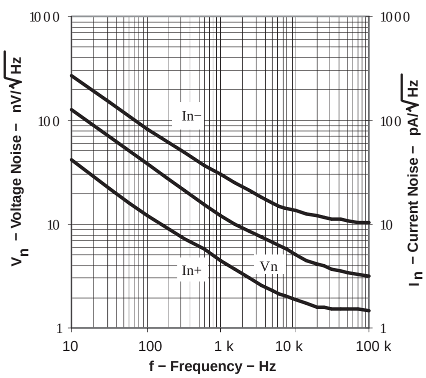


Figure 9.

OVERDRIVE RECOVERY

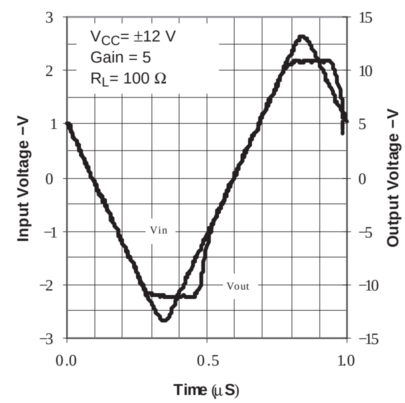


Figure 10.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

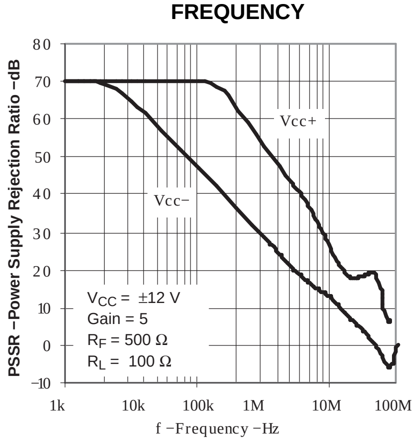


Figure 11.

OUTPUT AMPLITUDE vs FREQUENCY

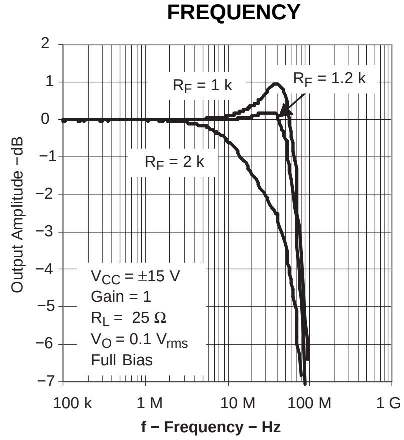


Figure 12.

OUTPUT AMPLITUDE vs FREQUENCY

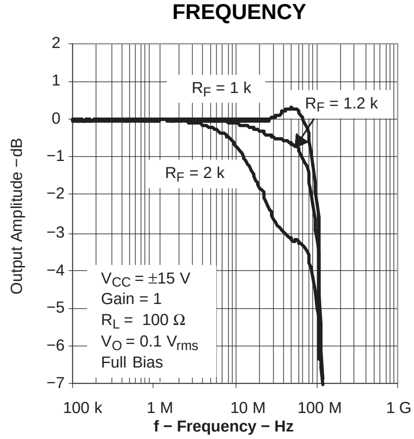


Figure 13.

OUTPUT AMPLITUDE vs FRQUENCY

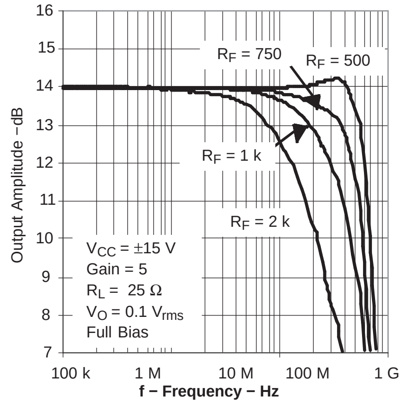


Figure 14.

OUTPUT AMPLITUDE vs FREQUENCY

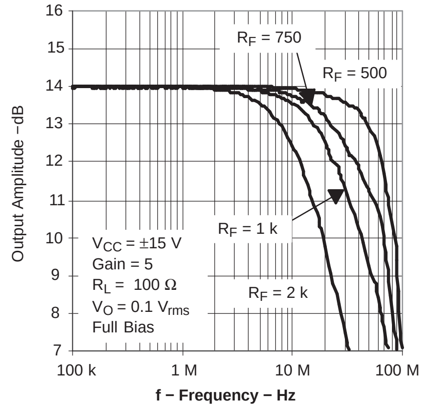


Figure 15.

OUTPUT AMPLITUDE vs FREQUENCY

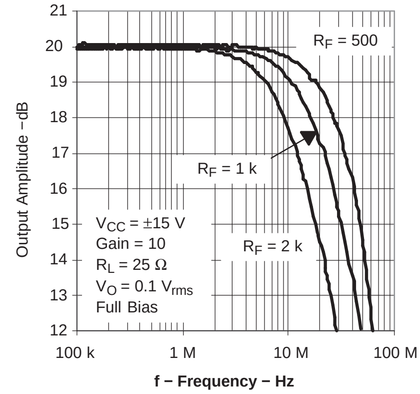


Figure 16.

OUTPUT AMPLITUDE vs FREQUENCY

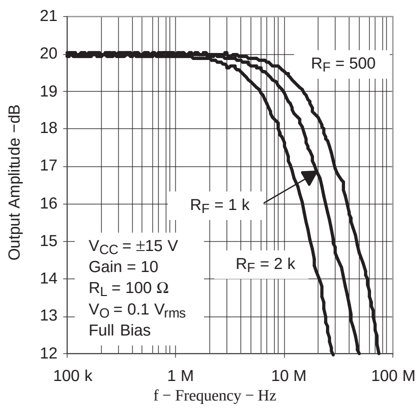


Figure 17.

OUTPUT AMPLITUDE vs FREQUENCY

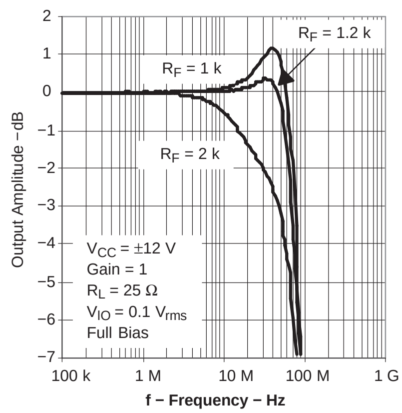


Figure 18.

OUTPUT AMPLITUDE vs FREQUENCY

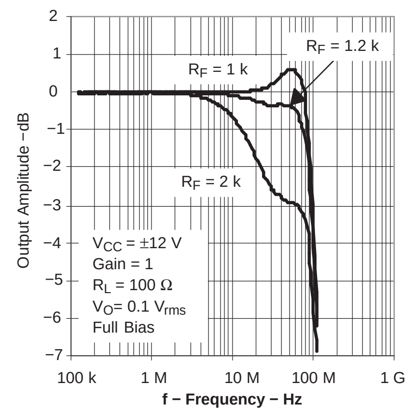


Figure 19.

OUTPUT AMPLITUDE vs FREQUENCY

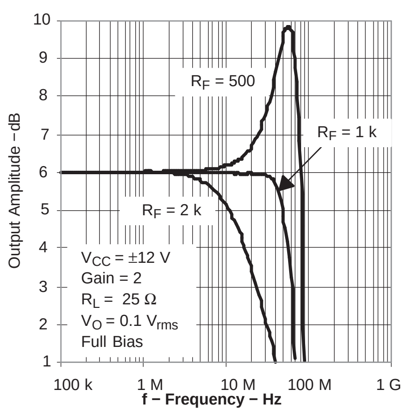


Figure 20.

OUTPUT AMPLITUDE vs FREQUENCY

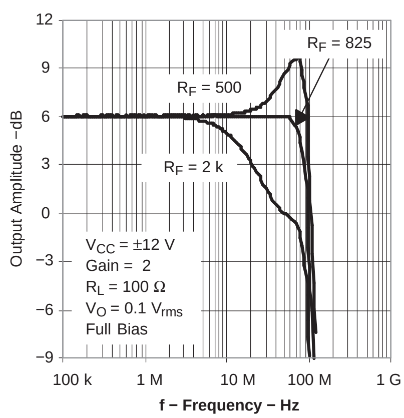


Figure 21.

OUTPUT AMPLITUDE vs FREQUENCY

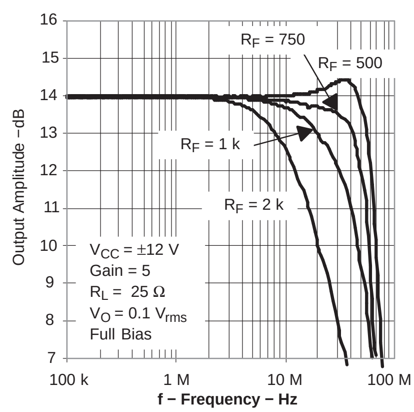


Figure 22.

OUTPUT AMPLITUDE vs FREQUENCY

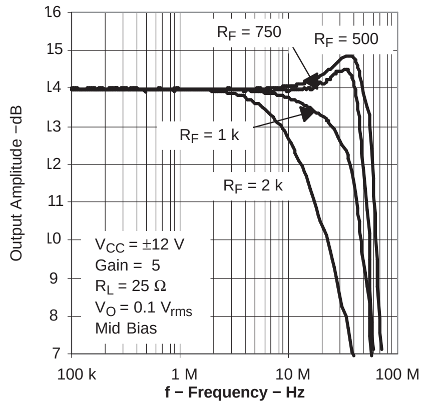


Figure 23.

OUTPUT AMPLITUDE vs FREQUENCY

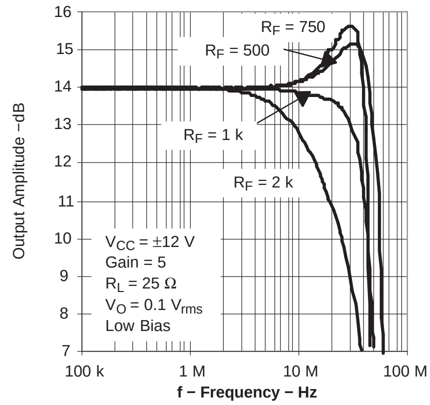


Figure 24.

OUTPUT AMPLITUDE vs FREQUENCY

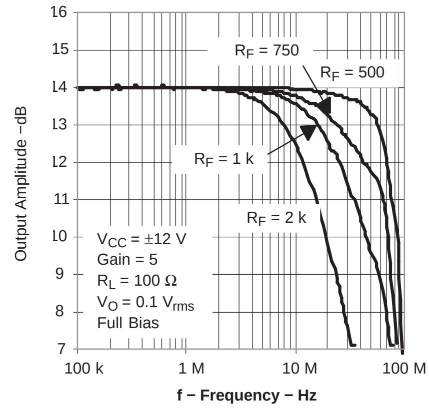


Figure 25.

OUTPUT AMPLITUDE vs FREQUENCY

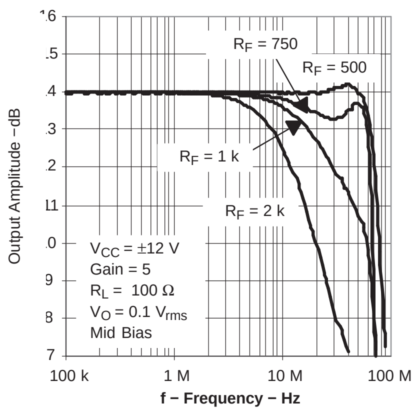


Figure 26.

OUTPUT AMPLITUDE vs FREQUENCY

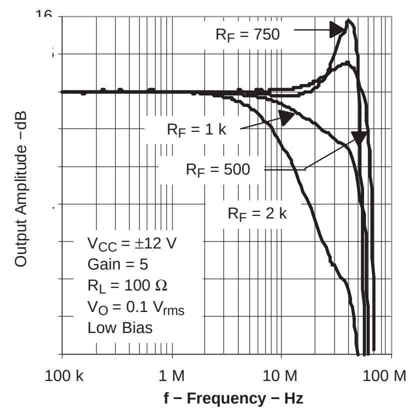


Figure 27.

OUTPUT AMPLITUDE vs FREQUENCY

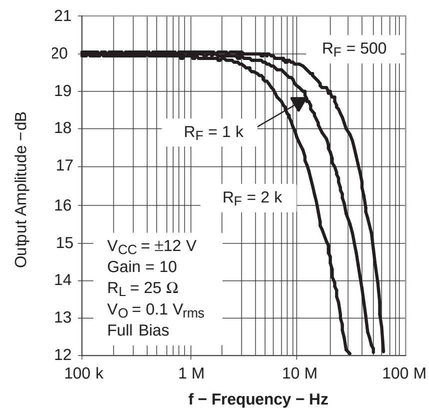


Figure 28.

OUTPUT AMPLITUDE vs FREQUENCY

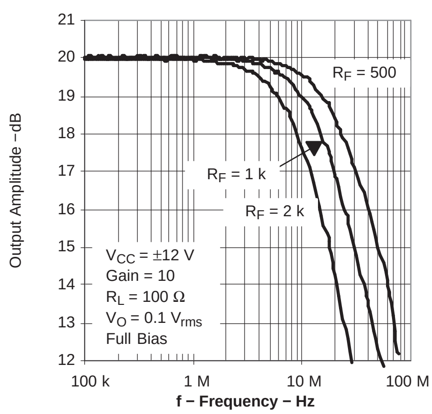


Figure 29.

OUTPUT AMPLITUDE vs FREQUENCY

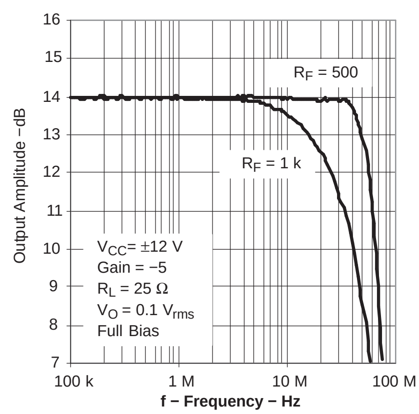


Figure 30.

OUTPUT AMPLITUDE vs FREQUENCY

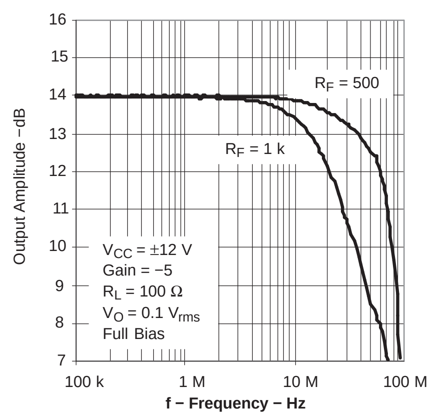


Figure 31.

OUTPUT AMPLITUDE vs FREQUENCY

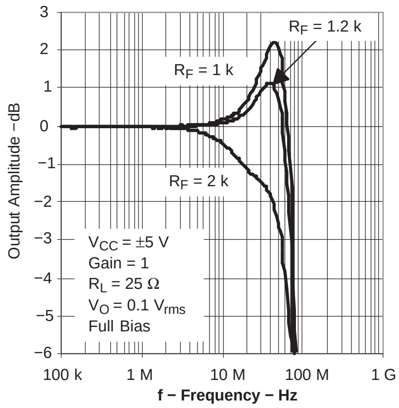


Figure 32.

OUTPUT AMPLITUDE vs FREQUENCY

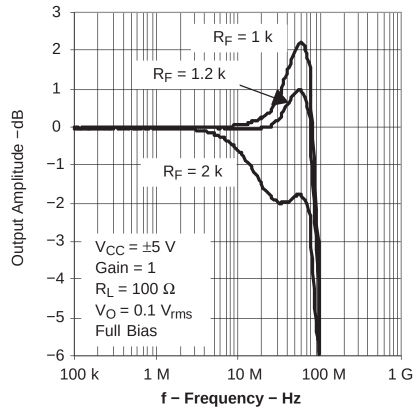


Figure 33.

OUTPUT AMPLITUDE vs FREQUENCY

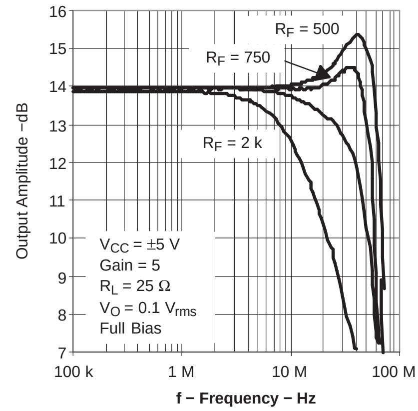


Figure 34.

OUTPUT AMPLITUDE vs FREQUENCY

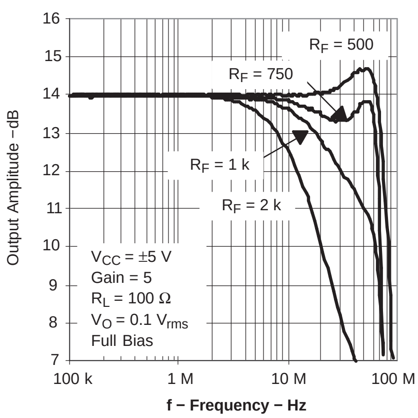


Figure 35.

OUTPUT AMPLITUDE vs FREQUENCY

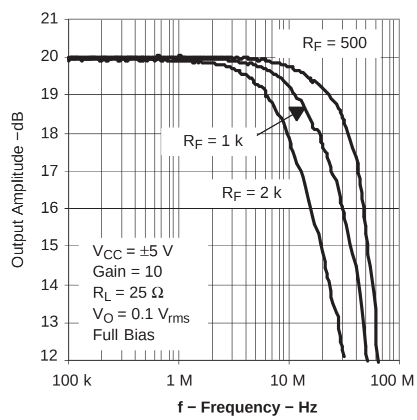


Figure 36.

OUTPUT AMPLITUDE vs FREQUENCY

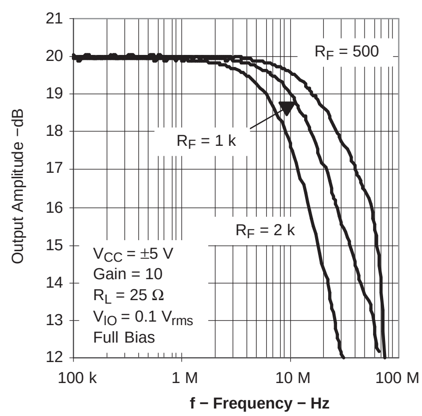


Figure 37.

SLEW RATE vs OUTPUT VOLTAGE

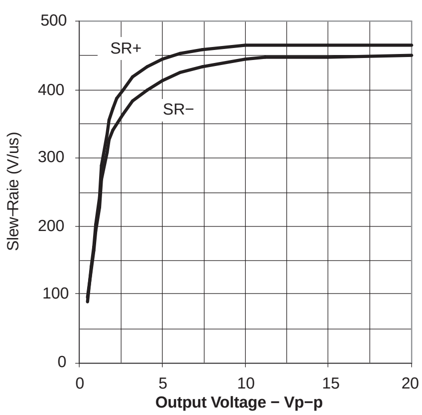


Figure 38.

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

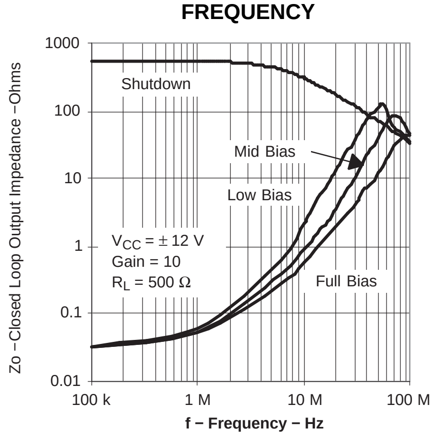


Figure 39.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

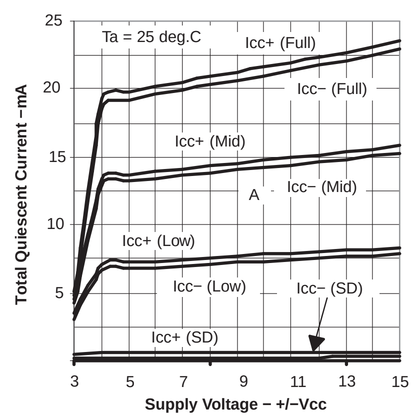


Figure 40.

QUIESCENT CURRENT vs TEMPERATURE

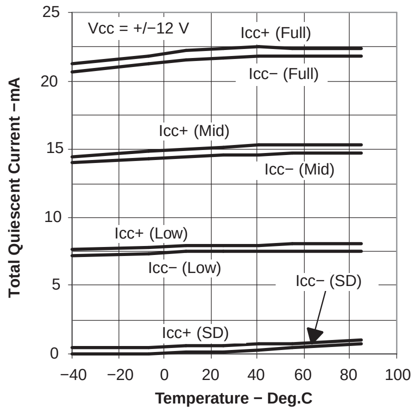


Figure 41.

COMMON-MODE REJECTION RATIO vs COMMON-MODE VOLTAGE

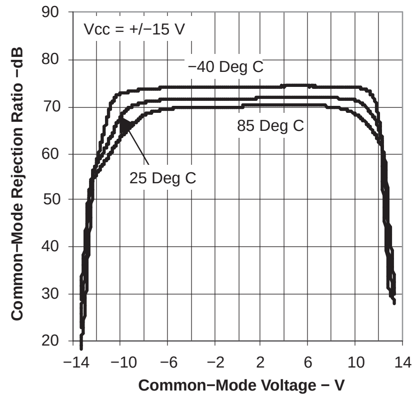


Figure 42.

INPUT BIAS CURRENT vs TEMPERATURE

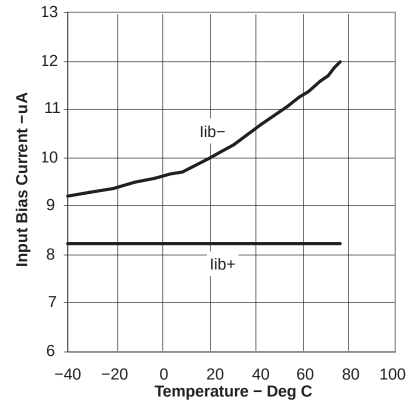


Figure 43.

INPUT OFFSET VOLTAGE vs TEMPERATURE

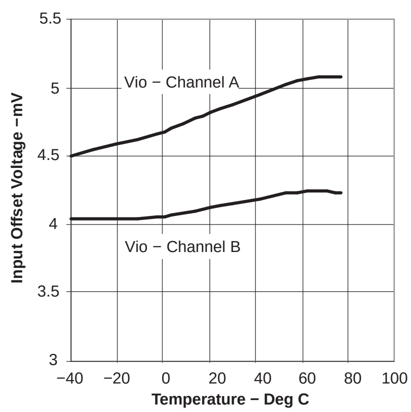


Figure 44.

2ND HARMONIC DISTORTION vs FREQUENCY

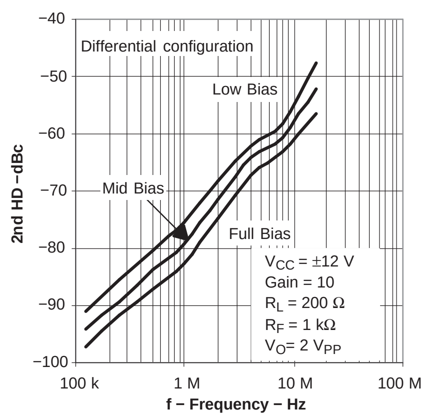


Figure 45.

2ND HARMONIC DISTORTION vs FREQUENCY

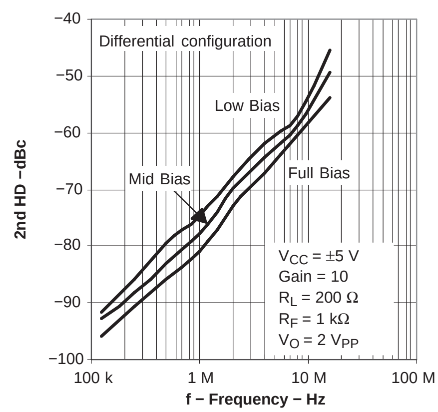


Figure 46.

2ND HARMONIC DISTORTION vs FREQUENCY

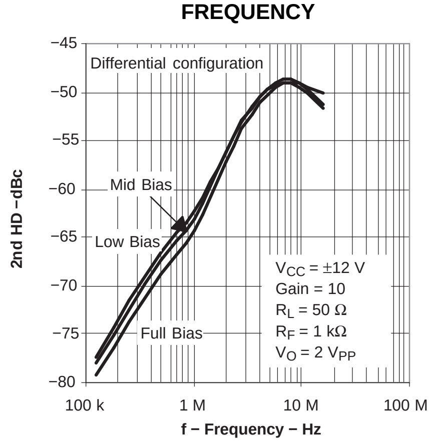


Figure 47.

2ND HARMONIC DISTORTION vs FREQUENCY

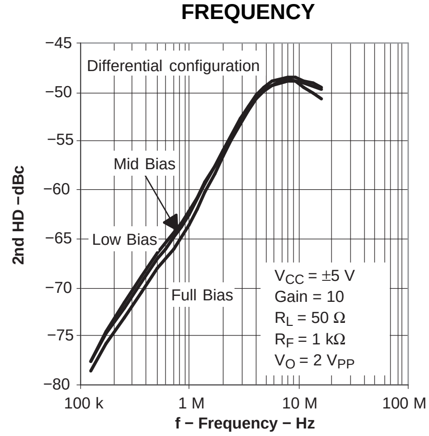


Figure 48.

2ND HARMONIC DISTORTION vs FREQUENCY

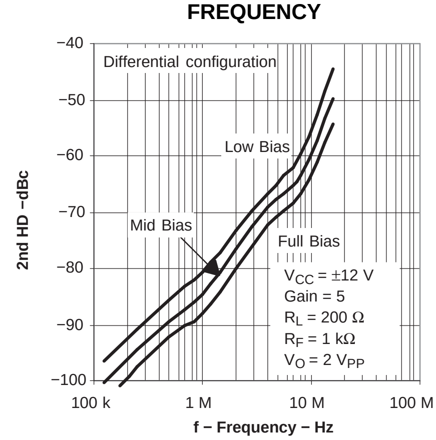


Figure 49.

2ND HARMONIC DISTORTION vs FREQUENCY

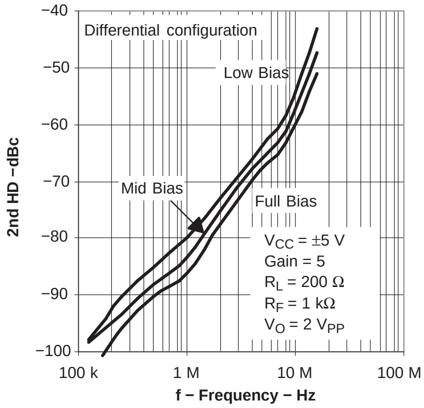


Figure 50.

2ND HARMONIC DISTORTION vs FREQUENCY

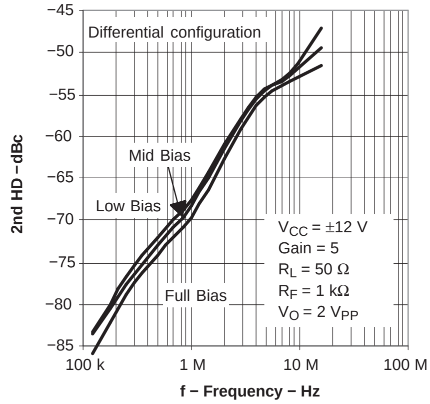


Figure 51.

2ND HARMONIC DISTORTION vs FREQUENCY

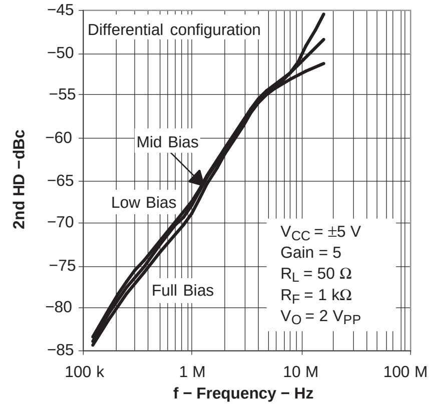


Figure 52.

3RD HARMONIC DISTORTION vs FREQUENCY

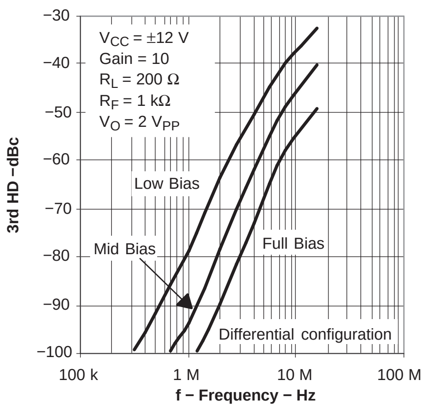


Figure 53.

3RD HARMONIC DISTORTION vs FREQUENCY

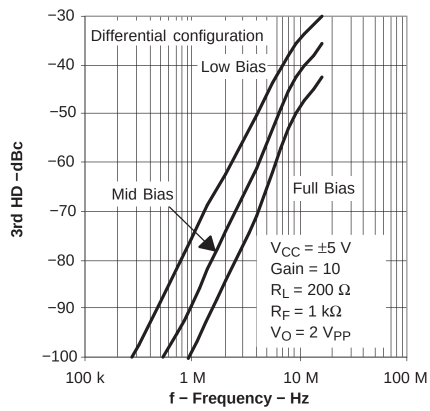


Figure 54.

3RD HARMONIC DISTORTION vs FREQUENCY

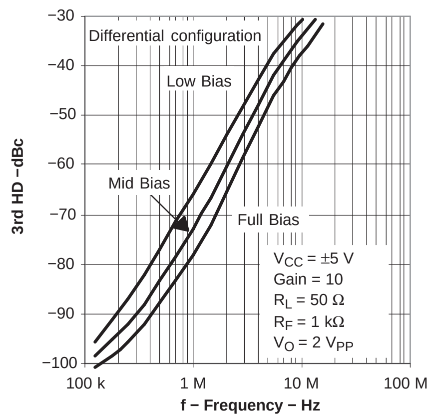


Figure 55.

3RD HARMONIC DISTORTION vs FREQUENCY

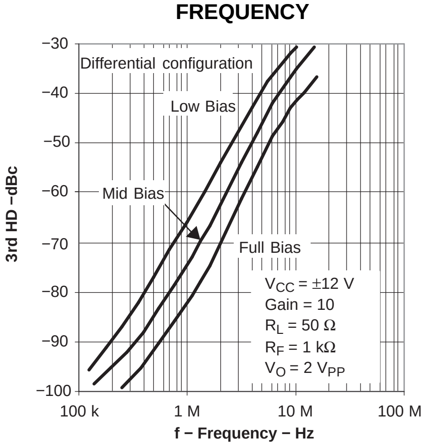


Figure 56.

3RD HARMONIC DISTORTION vs FREQUENCY

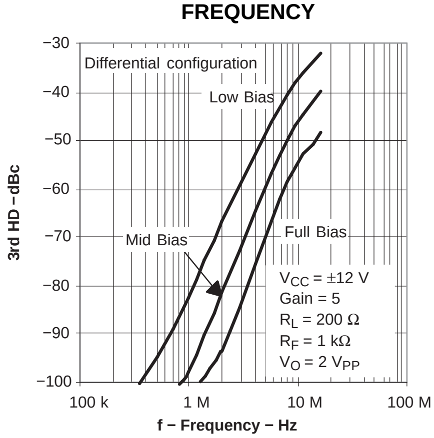


Figure 57.

3RD HARMONIC DISTORTION vs FREQUENCY

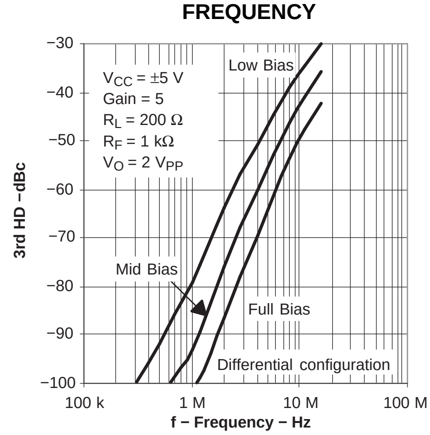


Figure 58.

3RD HARMONIC DISTORTION vs FREQUENCY

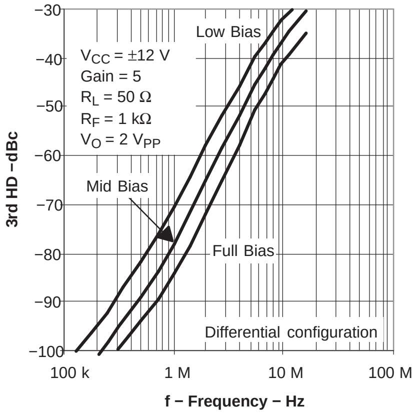


Figure 59.

3RD HARMONIC DISTORTION vs FREQUENCY

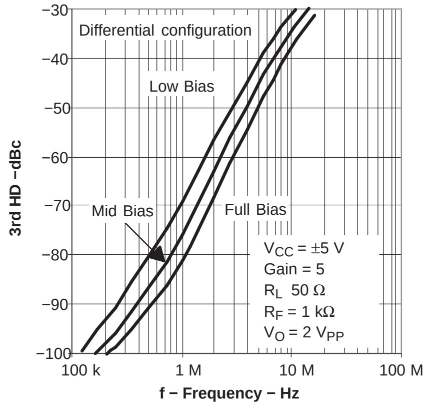


Figure 60.

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

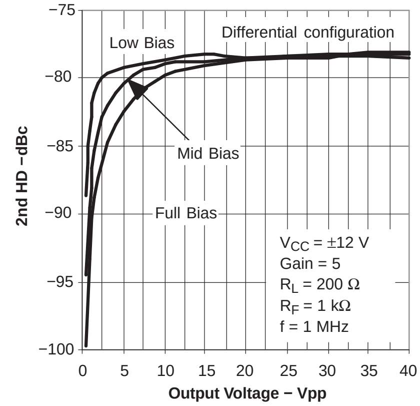


Figure 61.

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

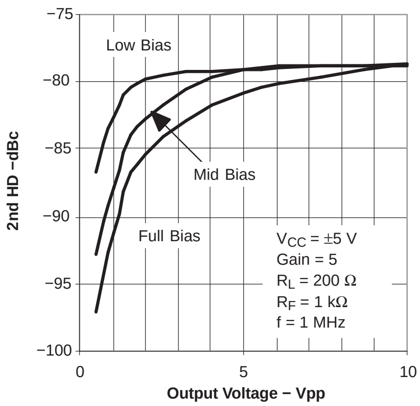


Figure 62.

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

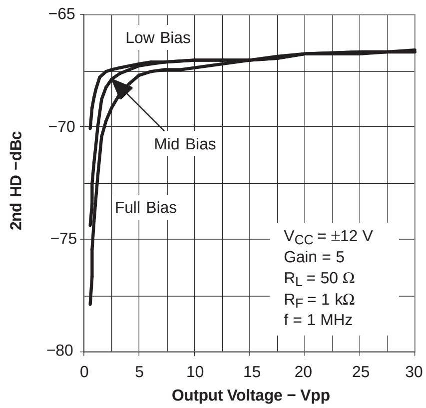


Figure 63.

2ND HARMONIC DISTORTION vs OUTPUT VOLTAGE

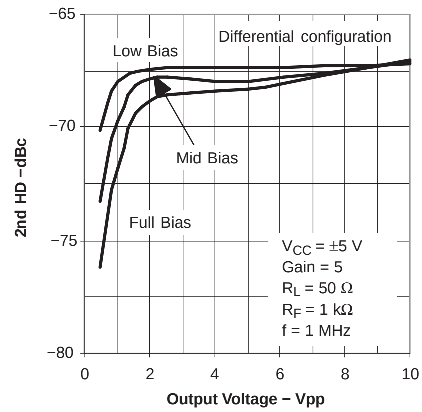


Figure 64.

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

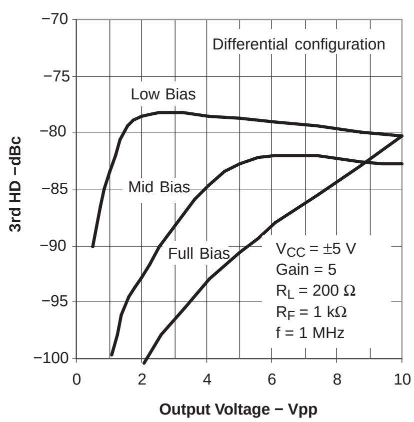


Figure 65.

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

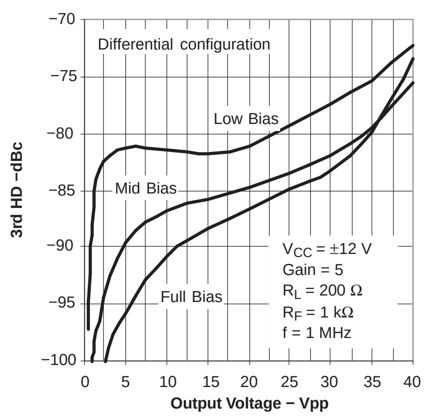


Figure 66.

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

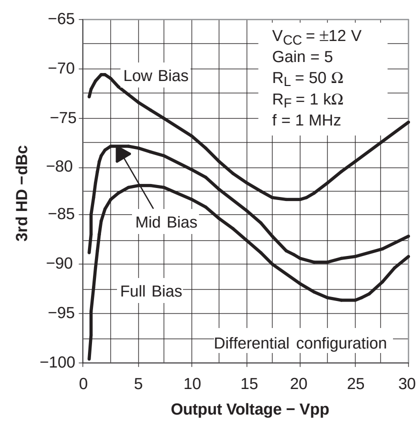


Figure 67.

3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE

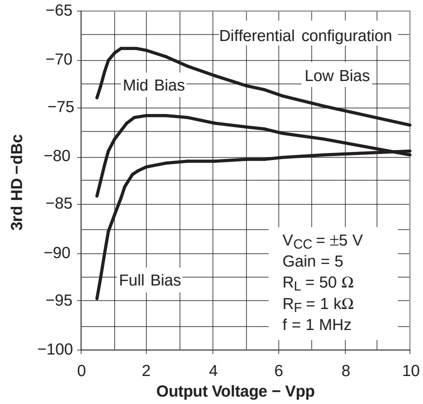


Figure 68.

APPLICATION INFORMATION

The THS6182 contains two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6182 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

DEVICE PROTECTION FEATURE

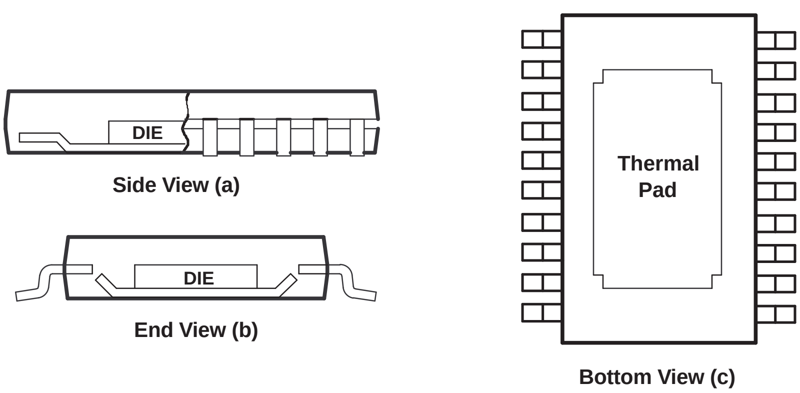
The THS6182 has a built-in thermal protection feature. Should the internal junction temperature rise above approximately 160°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on. This occurs at approximately 145°C, junction temperature. Note that the THS6182 does not have short-circuit protection and care should be taken to minimize the output current below the absolute maximum ratings.

THERMAL INFORMATION

The THS6182 is available in a thermally-enhanced DWP and RHF package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 69(a) and Figure 69(b), for the DWP package example]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 69(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that the PowerPAD is electronically isolated from the active circuitry and any pins. Thus, the PowerPAD can be connected to any potential voltage within the absolute maximum voltage range. Ideally, connection of the PAD to the ground plane is preferred as the plane typically is the largest copper plane on a PCB.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 69. Views of Thermally Enhanced DWP Package

APPLICATION INFORMATION (continued)

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current feedback amplifiers, the bandwidth of the THS6182 is an inversely proportional function of the value of the feedback resistor. The recommended resistors with a ±12-V power supply for the optimum frequency response with a 25-Ω load system is 1 kΩ for a gain of 5. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics.

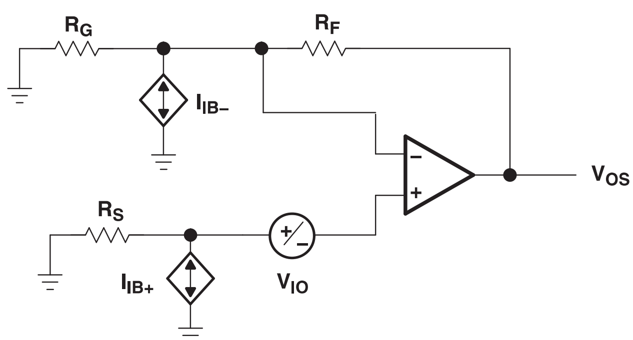
Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers.

It is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

Finally, in a differential configuration as shown in Figure 1, it is important to note that there is a differential gain and a common-mode gain which are different from each other. Differentially, the gain is at 1 + R_F/R_G. While common-mode gain = 1 due to R_G being connected directly between each amplifier and not to ground. This can lead to potential problems as the stability of the amplifier is determined by R_F. Thus, R_F must be large enough to ensure the common-mode stability, even though a large differential gain may be required.

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 70. Output Offset Voltage Model

NOISE CALCULATIONS

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 71. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN- = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{RX} = Thermal voltage noise associated with each resistor (e_{RX} = 4 kTR_x)

APPLICATION INFORMATION (continued)

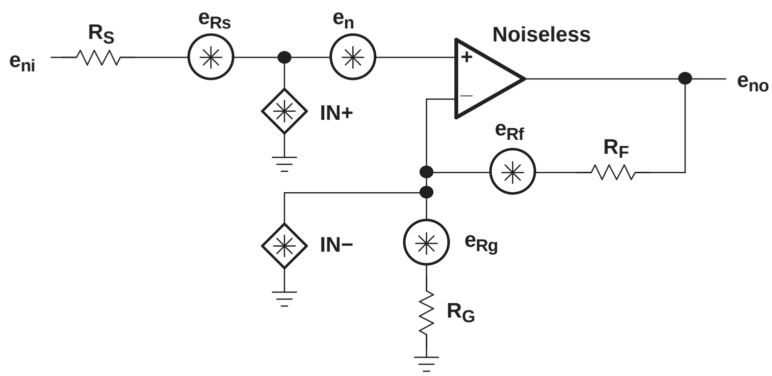


Figure 71. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
R_F || R_G = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{(Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6182 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 72. A minimum value of 2 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

APPLICATION INFORMATION (continued)

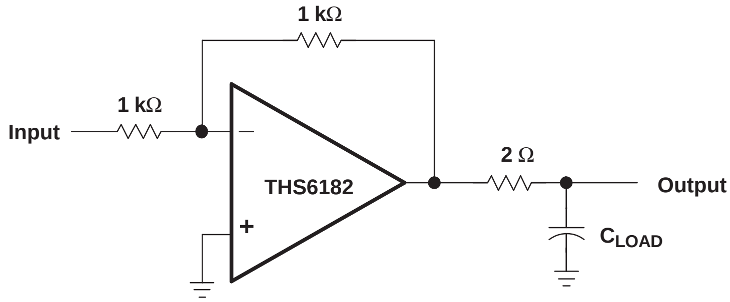


Figure 72. Driving a Capacitive Load

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to assure proper operation of the THS6182. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6182 is a high-speed part, the following guidelines are recommended.

- Ground plane - It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6012 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal. Note that the BiCom process is a SOI process and thus, the substrate is isolated from the active circuitry.
- Input stray capacitance - To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane should be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration.
- Proper power supply decoupling - Use a minimum of a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.
- For a differential configuration as shown in Figure 1, it is recommended that a 0.1-µF or 1-µF capacitor be added across the power supplies (from V_{CC+} to V_{CC-}) as close as possible to the THS6182. This allows for differential currents to flow properly, signficantly reducing even-order harmonic distortion. The 0.1-µF capacitors to ground should also be used as previously stipulated.

Because of its power dissipation, proper thermal management of the THS6182 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane utilizing the 20 pin DWP PowerPAD package.

1. Prepare the PCB with a top side etch pattern as shown in Figure 73. There should be etch for the leads as well as etch for the thermal pad.
2. Place 18 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. It is recommended, but not required, to place six more holes under the package, but outside the thermal pad area. These holes are 25 mils in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.
4. Connect all 24 holes, the 18 within the thermal pad area and the 6 outside the pad area, to the internal ground plane.
5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the

APPLICATION INFORMATION (continued)

heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6182 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.

6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
8. With these preparatory steps in place, the THS6182 DWP is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

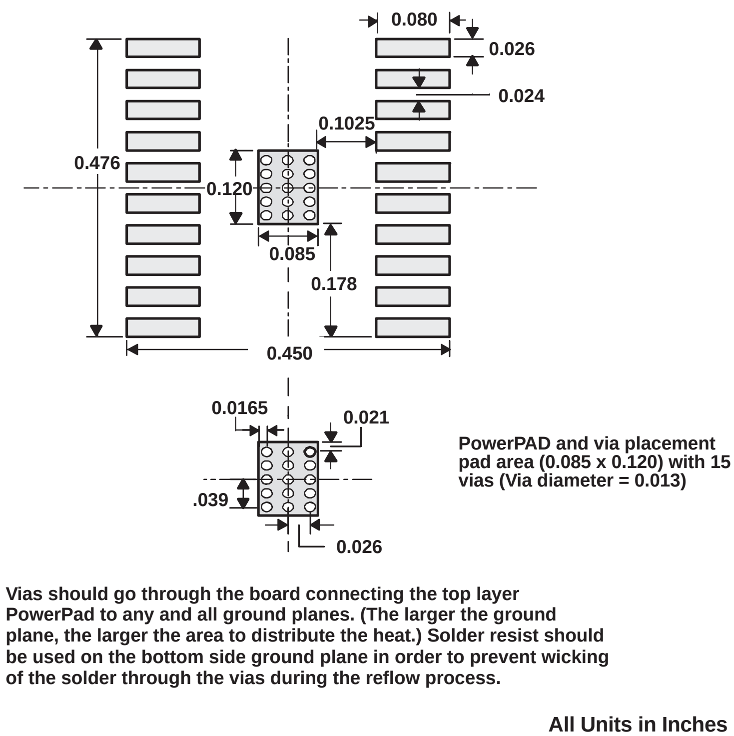
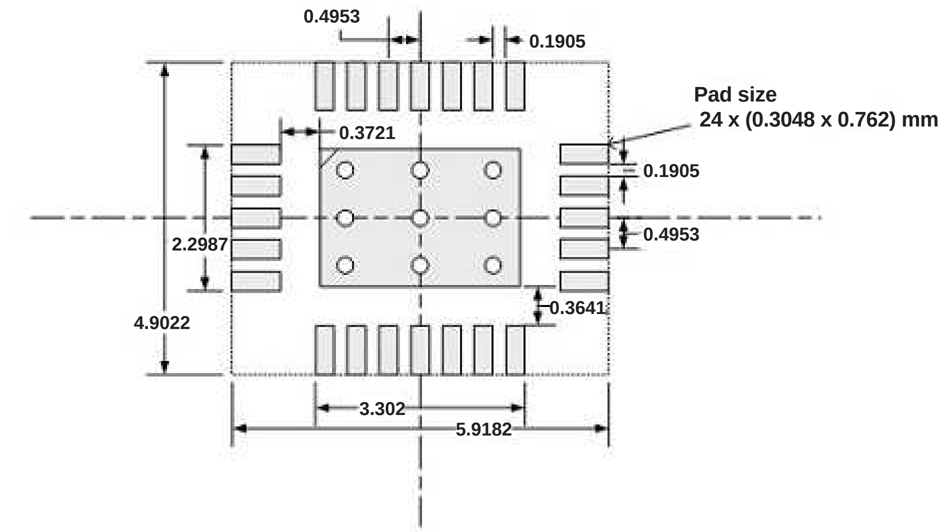


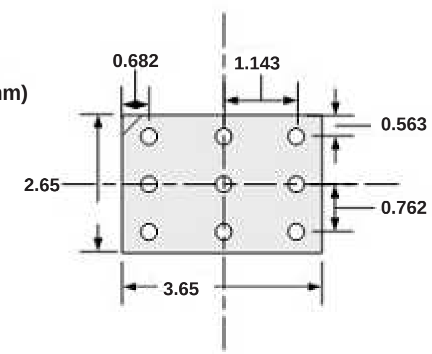
Figure 73. 20-Pin DWP PowerPAD PCB Etch and Via Pattern

The RHF package is similar to the DWP package with respect to PCB mounting procedures. The recommended PCB layout is as shown in Figure 74.

APPLICATION INFORMATION (continued)



PowerPAD and Via layout
(Pad size 3.65 mm x 2.65 mm ,
9 Vias with diameter = 0.254 mm)



Vias should go through the board connecting the top layer PowerPAD to any and all ground planes. The larger the ground plane, the more area to distribute the heat.

Solder resist should be used on the bottom side ground plane to prevent wicking of the solder through the vias during the reflow process.

Figure 74. Suggested PCB Layout

The actual thermal performance achieved with the THS6182 in the 20-pin DWP PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, Θ_{JA}, is about 21.5°C/W. (See the Package Dissipation Ratings Table for all other package metrics.) For a given Θ_{JA}, the maximum power dissipation is calculated by the following formula:

APPLICATION INFORMATION (continued)

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

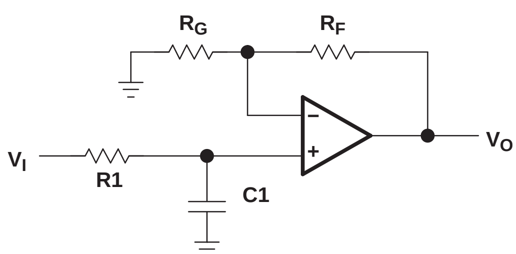
P_D = Maximum power dissipation of THS6182 (watts)
T_{MAX} = Absolute maximum operating junction temperature (125°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case. See the Package Dissipation Ratings table.
θ_{CA} = Thermal coefficient from case to ambient determined by PCB layout and construction.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is **not** recommended. The THS6182, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 75).



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 75. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 76.

APPLICATION INFORMATION (continued)

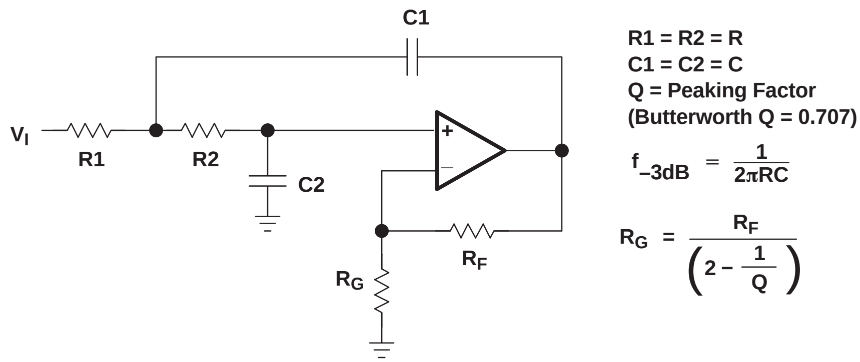


Figure 76. 2-Pole Low-Pass Sallen-Key Filter

EVALUATION BOARD

An evaluation board is available for the THS6182. This board has been configured for proper thermal management of the THS6182. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, refer to the *THS6182EVM User's Guide* (literature number SLOU152). To order the evaluation board contact your local TI sales office or distributor.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS6182D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS6182
THS6182D.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS6182
THS6182DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS6182
THS6182DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS6182
THS6182DWP	Active	Production	SO PowerPAD (DWP) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6182
THS6182DWP.A	Active	Production	SO PowerPAD (DWP) | 20	25 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6182
THS6182DWPR	Active	Production	SO PowerPAD (DWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6182
THS6182DWPR.A	Active	Production	SO PowerPAD (DWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6182
THS6182RHFR	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6182
THS6182RHFR.A	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6182
THS6182RHFT	Active	Production	VQFN (RHF) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6182
THS6182RHFT.A	Active	Production	VQFN (RHF) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6182

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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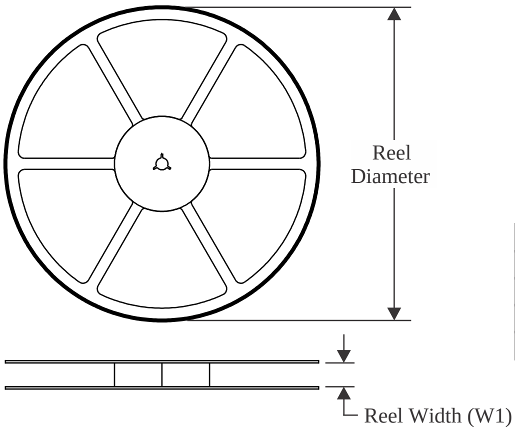
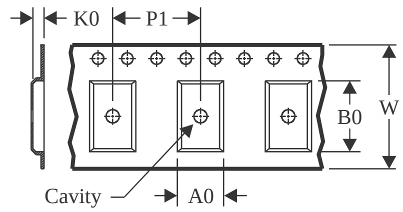
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

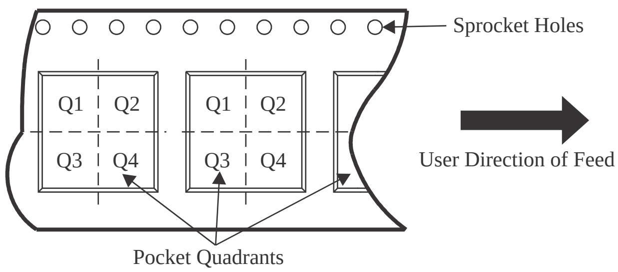


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

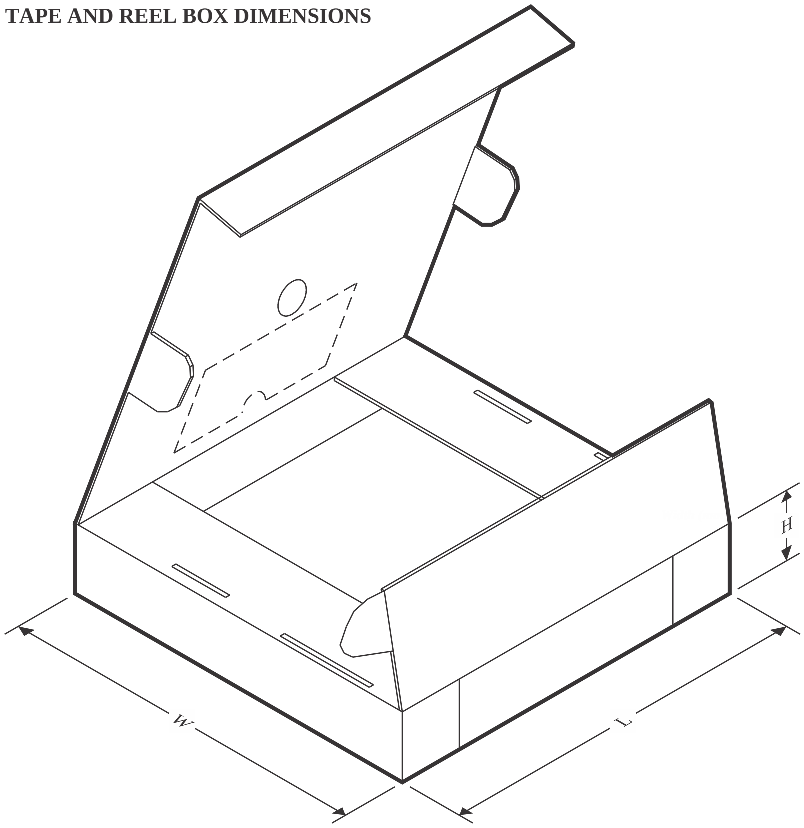
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6182DWPR	SO PowerPAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

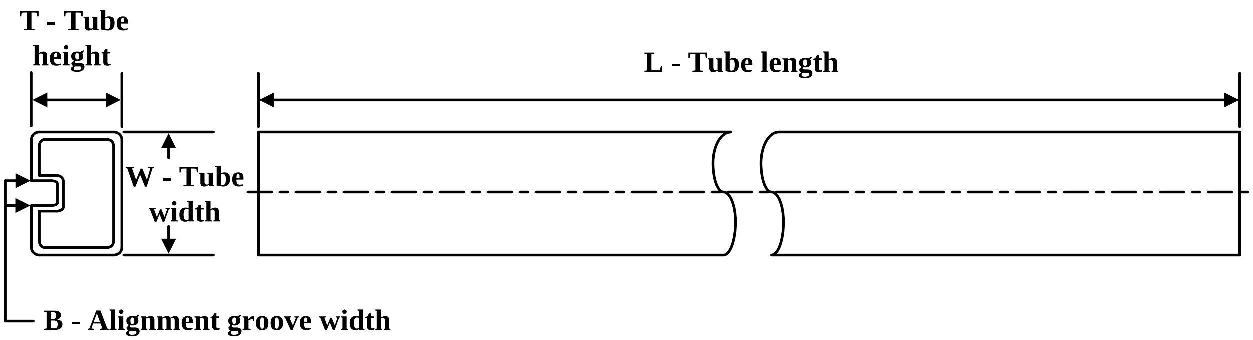
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6182DWPR	SO PowerPAD	DWP	20	2000	350.0	350.0	43.0

TUBE

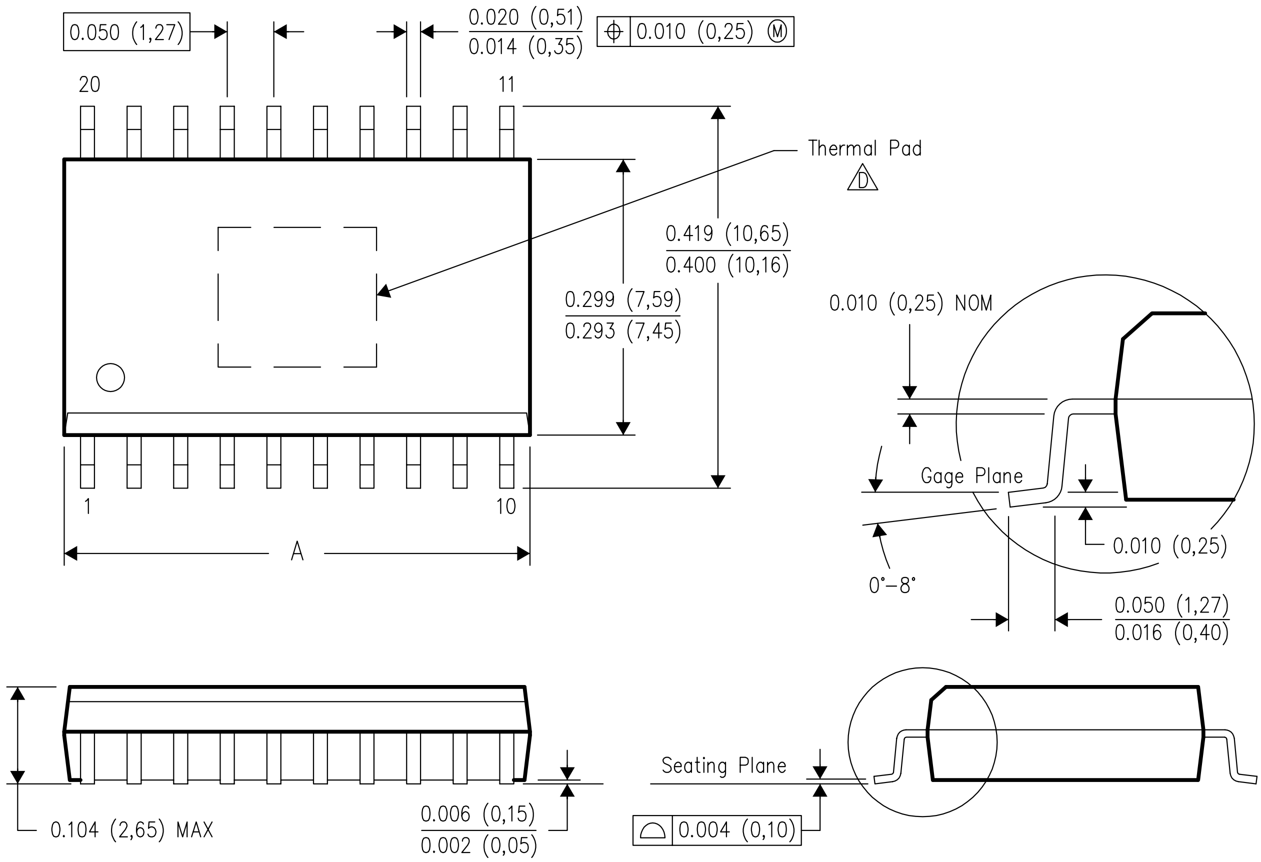


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS6182D	D	SOIC	16	40	505.46	6.76	3810	4
THS6182D.A	D	SOIC	16	40	505.46	6.76	3810	4
THS6182DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
THS6182DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
THS6182DWP	DWP	HSOIC	20	25	506.98	12.7	4826	6.6
THS6182DWP.A	DWP	HSOIC	20	25	506.98	12.7	4826	6.6

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



PINS ** / DIM	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

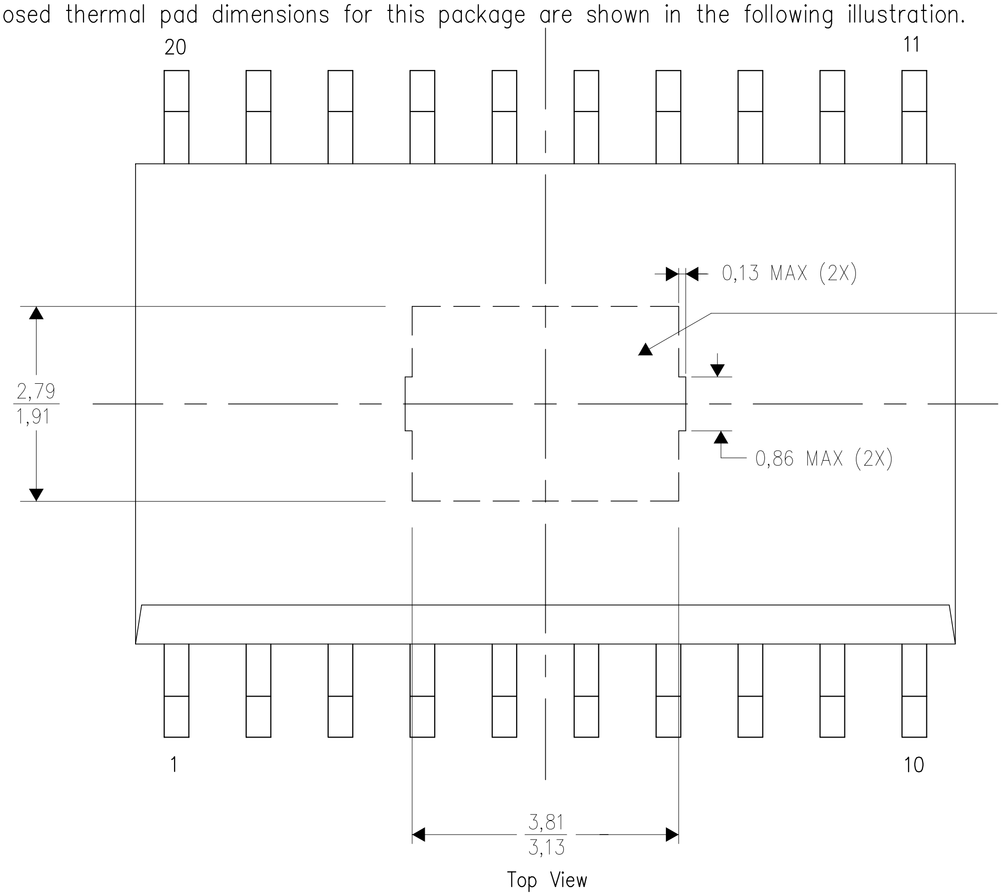
DWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

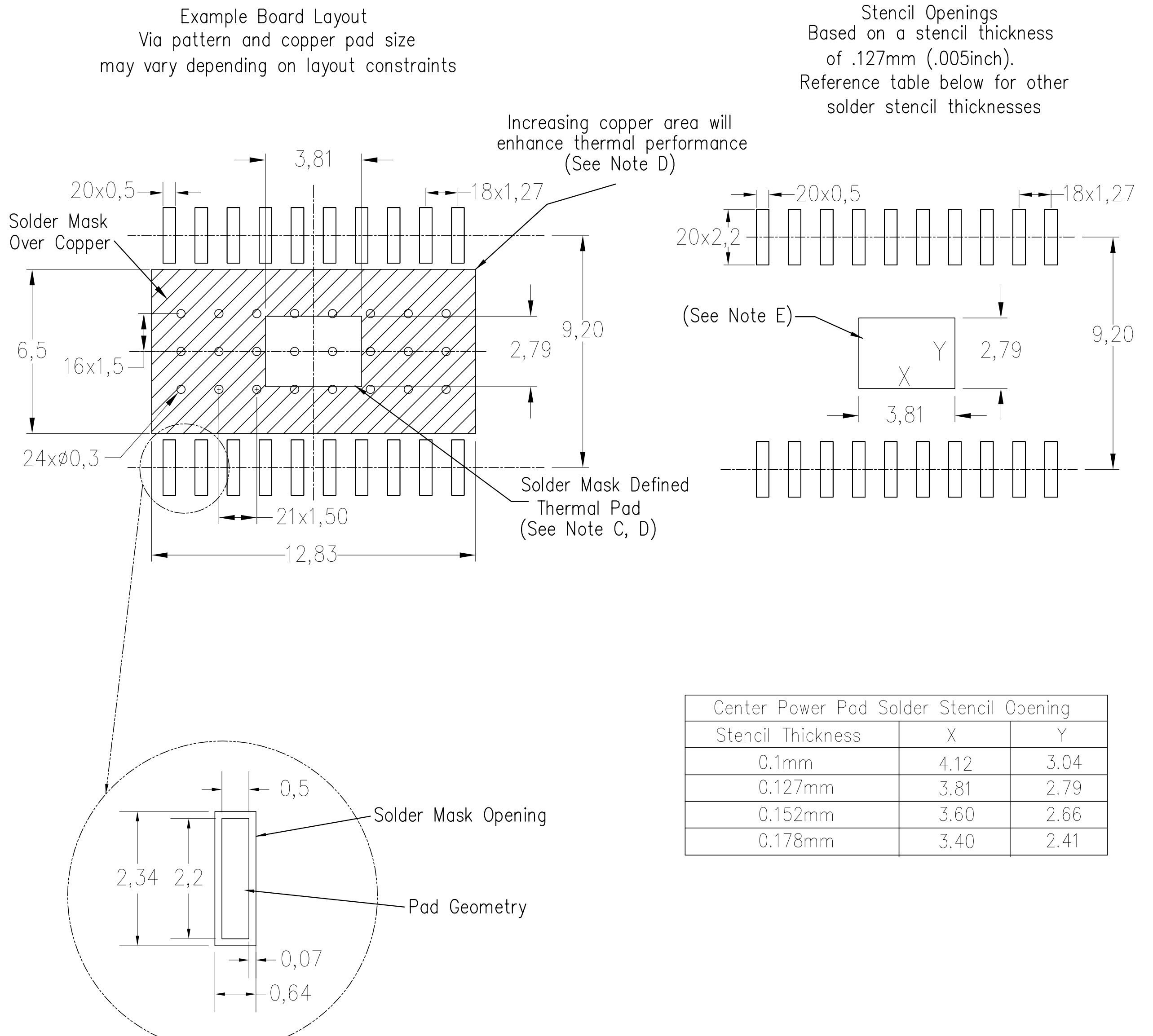


Exposed Thermal Pad Dimensions

4206325-4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

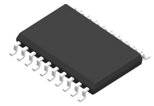


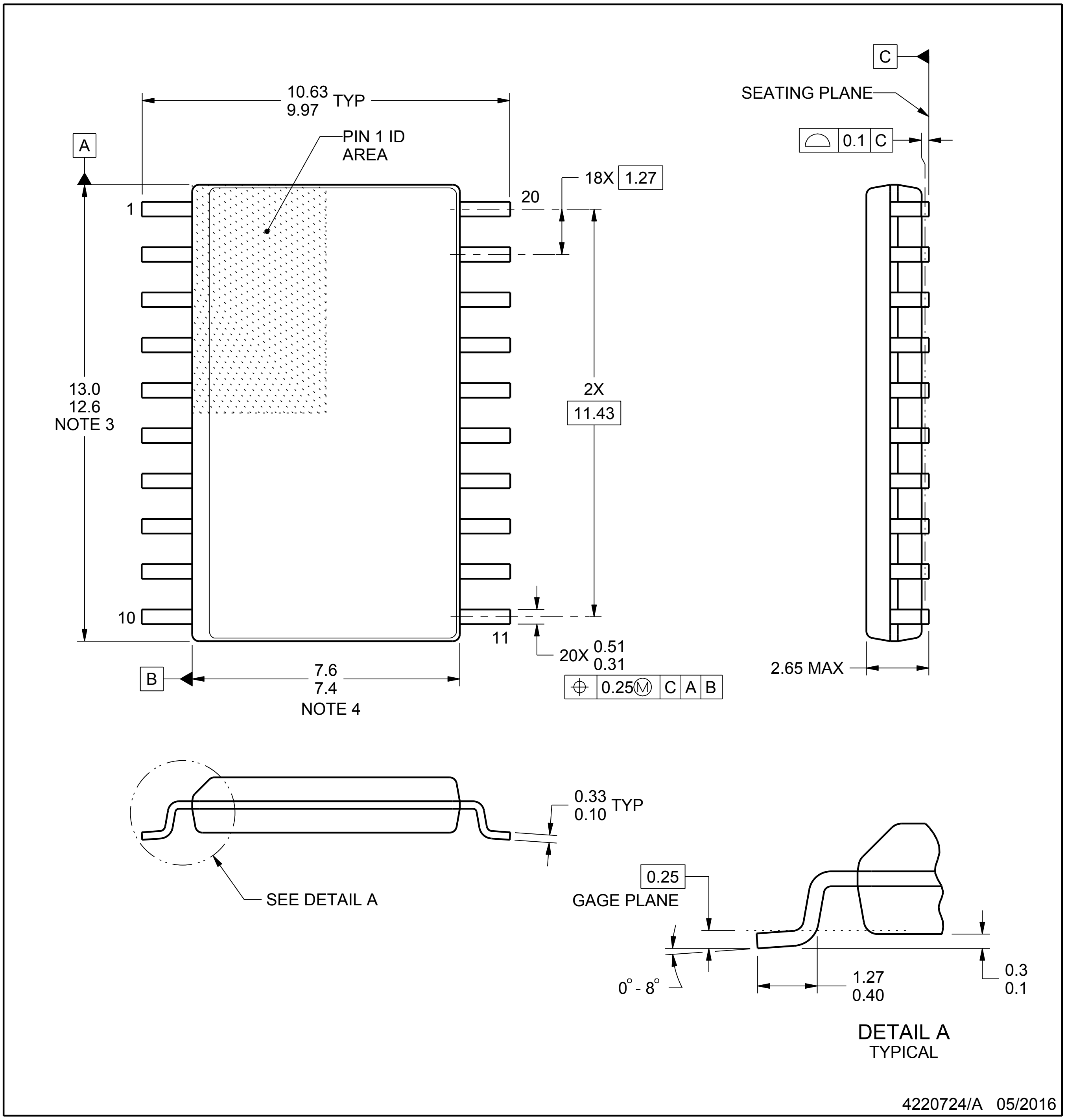
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.12	3.04
0.127mm	3.81	2.79
0.152mm	3.60	2.66
0.178mm	3.40	2.41

4208286–3/B 12/10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

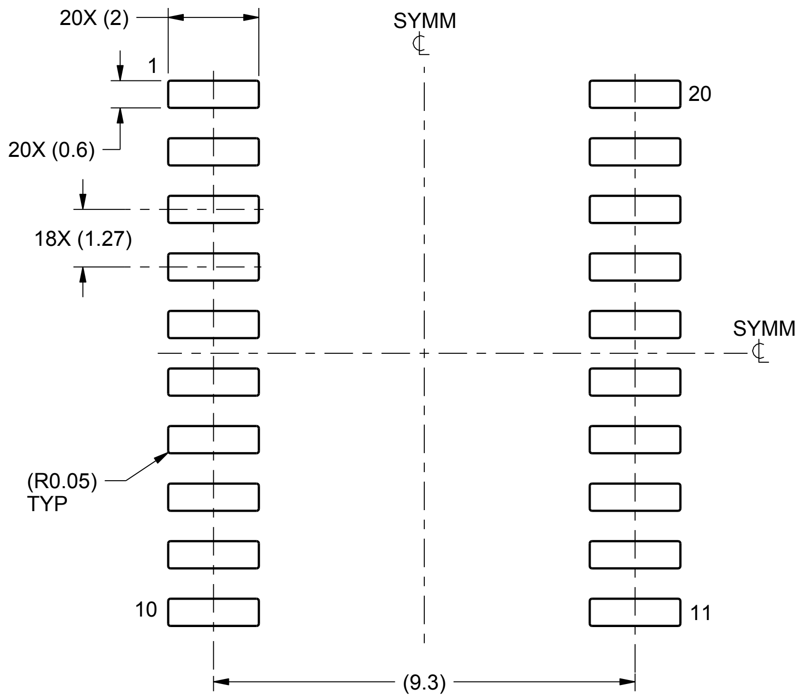
PowerPAD is a trademark of Texas Instruments.



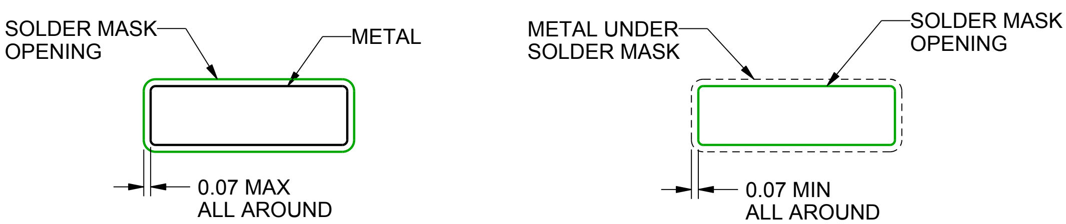


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

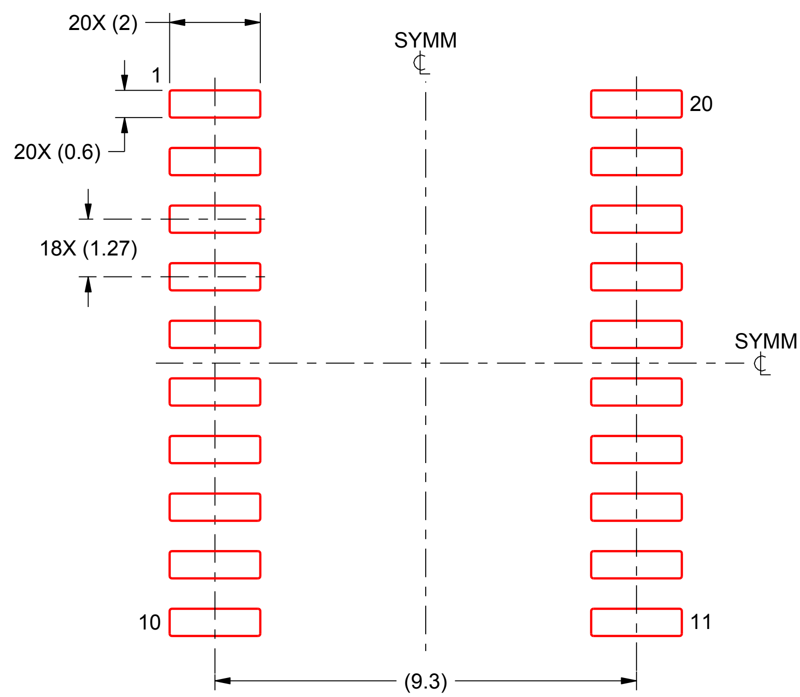
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



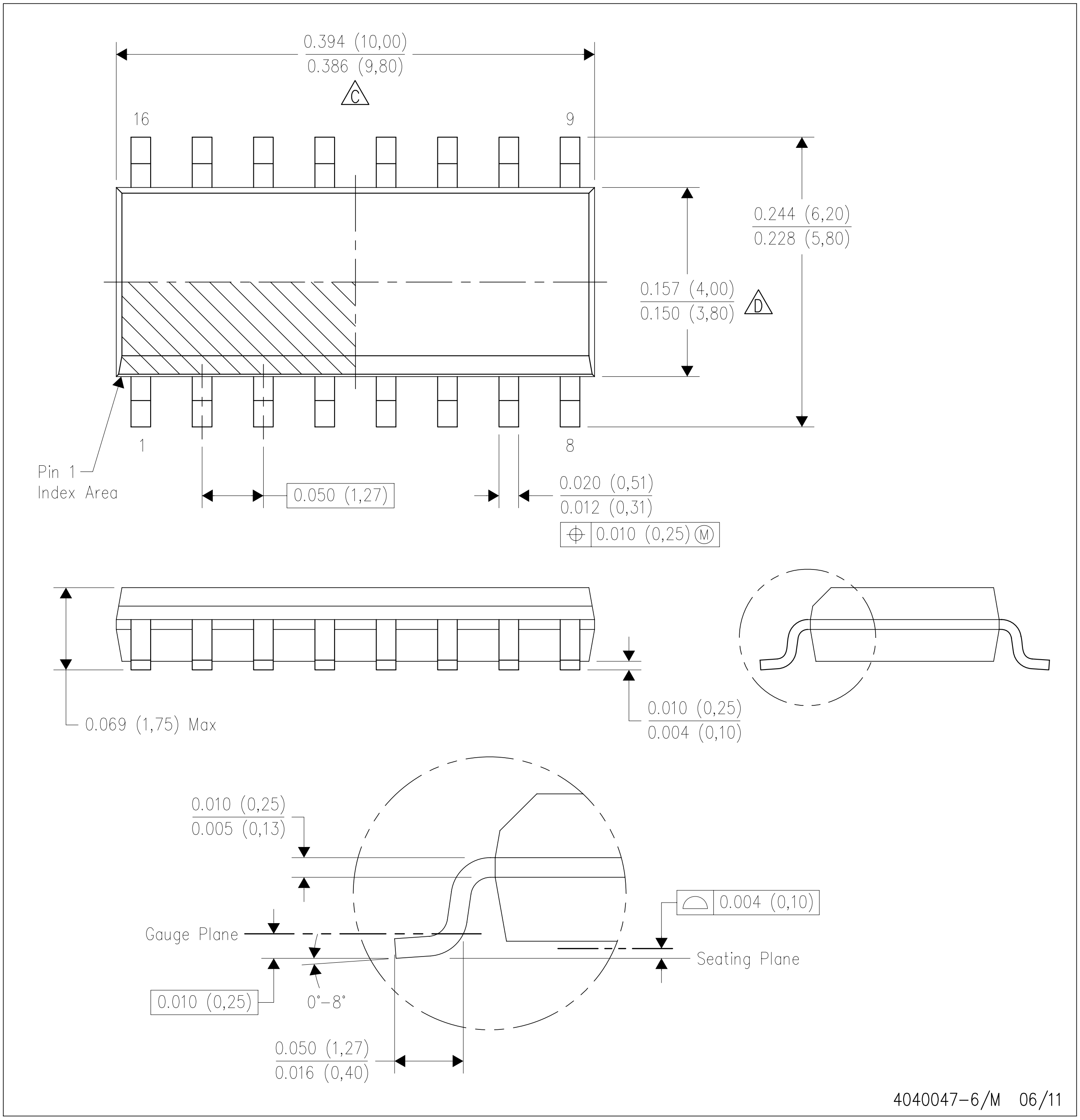
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

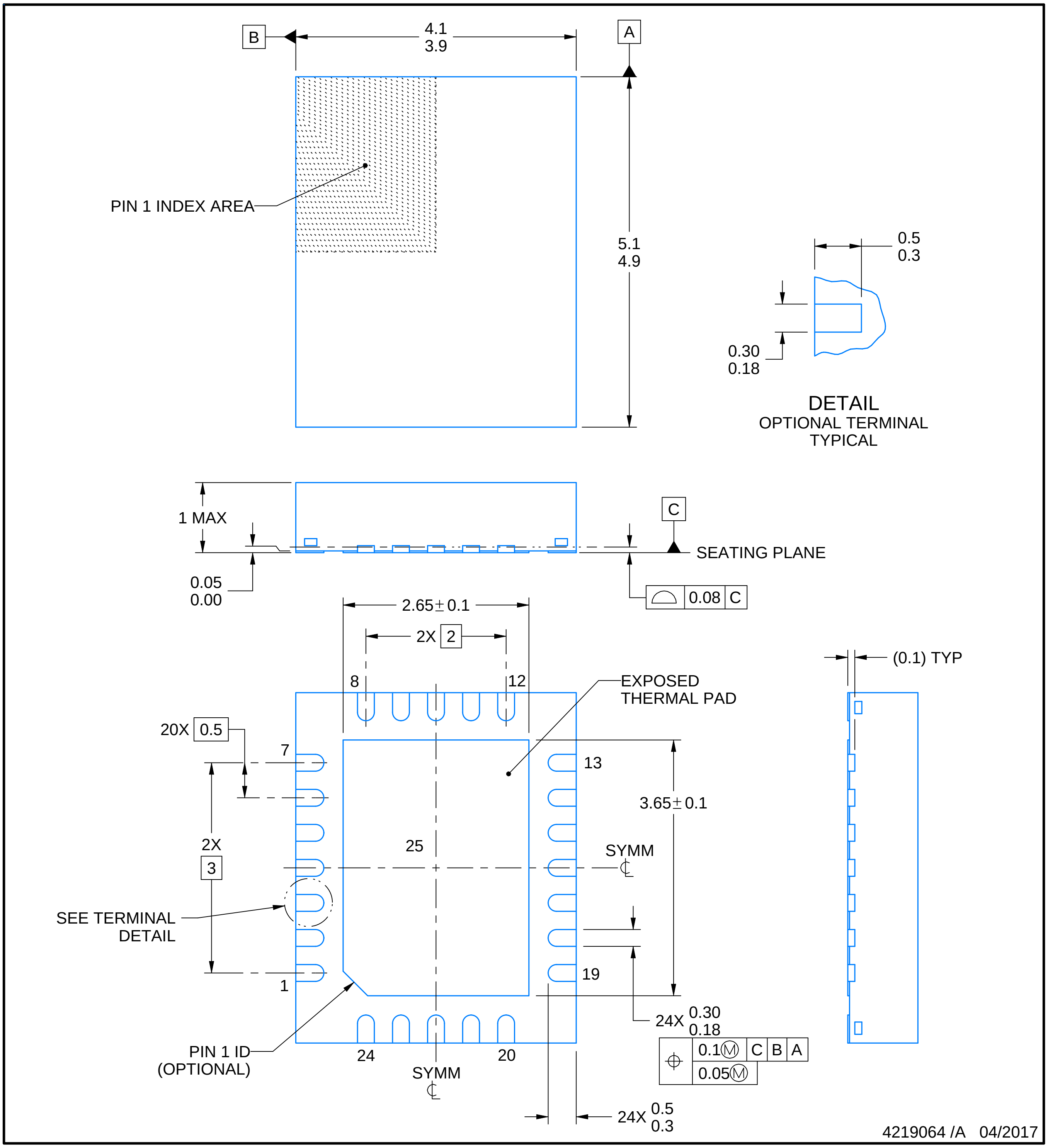
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE

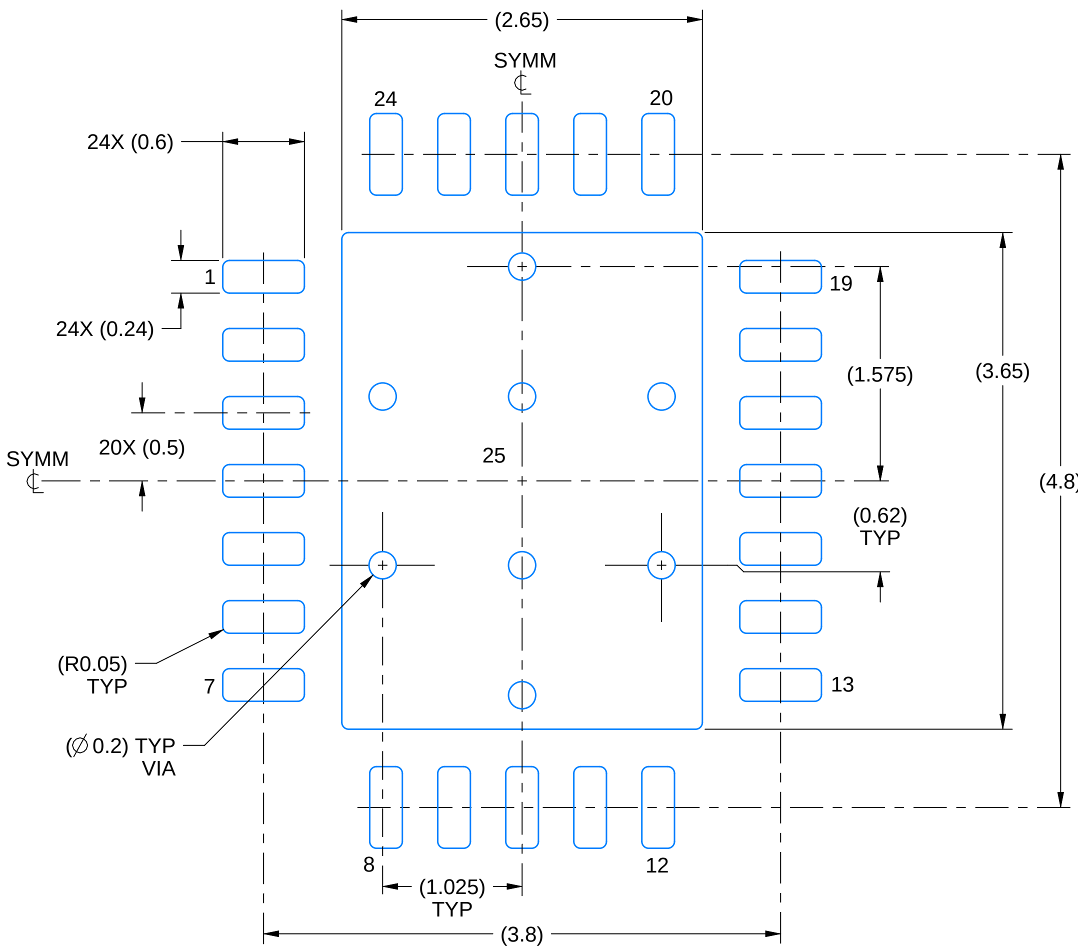


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

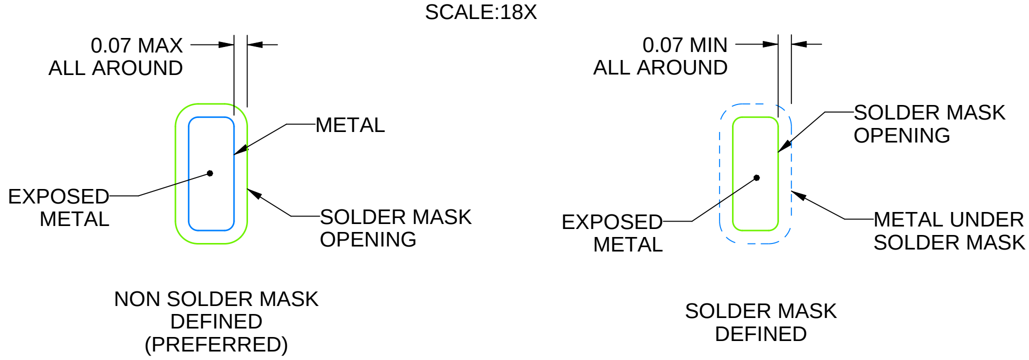


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

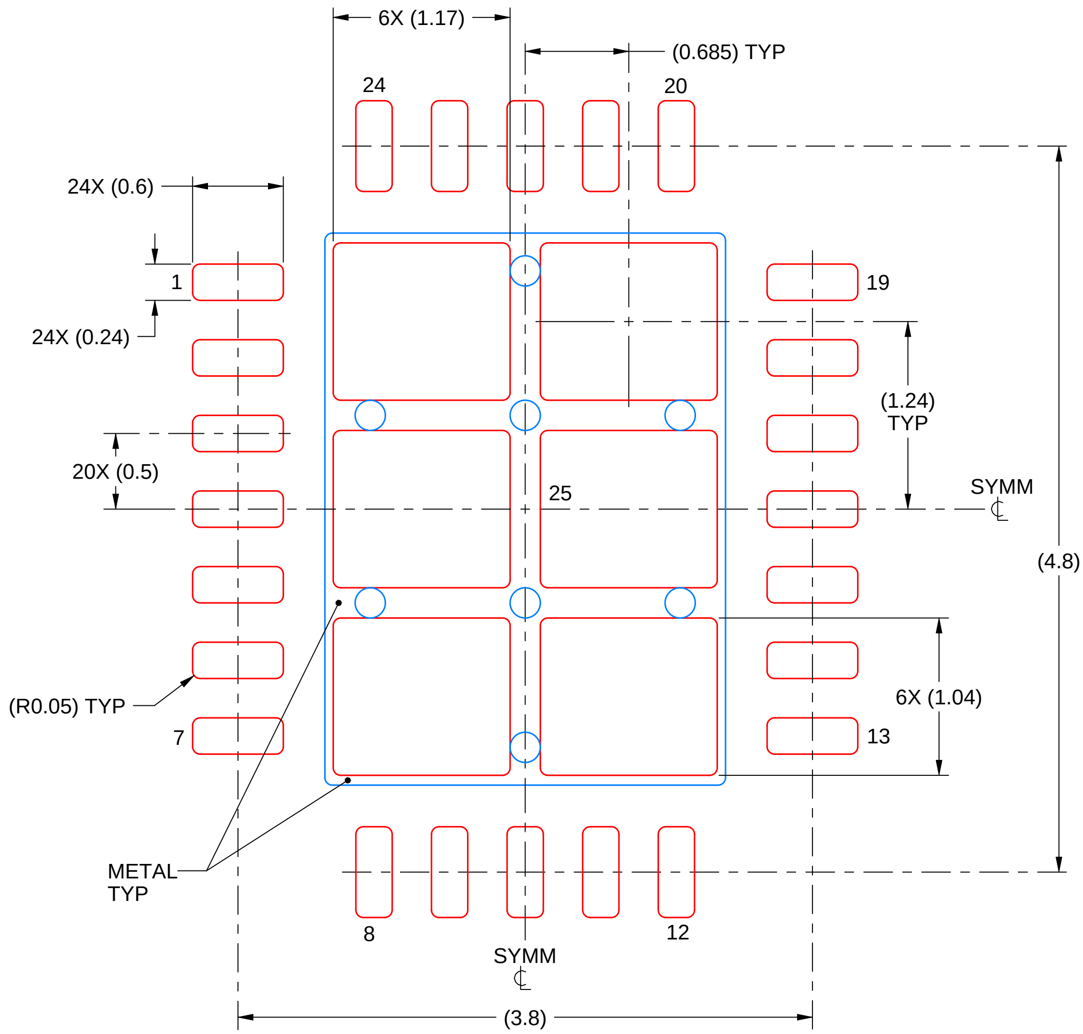


SOLDER MASK DETAILS

4219064 /A 04/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219064 /A 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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