TPD4S214 USB OTG Companion Device with V_{BUS} Over Voltage Protection, Over Current Protection, and Four Channel ESD Protection

1 Features

- Input Voltage Protection at V_{BUS} from –7 V to 30 V
- IEC61000-4-2 Level 4 ESD Protection
  - ±15-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-5 Surge Protection
  - 7.8 A (8/20 µs)
- Low $R_{DS(ON)}$ N-CH FET Switch for High Efficiency
- Compliant with USB2.0 and USB3.0 OTG spec
- User Adjustable Current Limit From 250 mA to Beyond 1.2 A
- Built-in Soft-start
- Reverse Current Blocking
- Over Voltage Lock Out for V_{BUS}
- Under Voltage Lock Out for V_{OTG_IN}
- Thermal Shutdown and Short Circuit Protection
- Auto Retry on any Fault; No Latching Off States
- Integrated V_{BUS} Detection Circuit
- Low Capacitance TVS ESD Clamp for USB2.0 High Speed Data Rate
- Internal 16ms Startup Delay
- Space Saving WCSP (12-YFF) Package
- UL Listed and CB File No. E169910

2 Applications

- Cell Phones
- Tablet, eBook
- Portable Media Players
- Digital Camera

3 Description

The TPD4S214 is a single-chip protection solution for USB On-the-Go (OTG) and other current limited USB applications. This device includes an integrated low $R_{DS(ON)}$ N-channel current limited switch for the OTG current supply to peripheral devices. TPD4S214 offers low capacitance transient voltage suppression (TVS) electrostatic discharge (ESD) clamping diodes for the D+, D–, and ID pins for both USB2.0 and USB3.0 applications. The V_{BUS} pin can handle continuous voltage ranging from –7 V to 30 V. The over voltage lock-out (OVLO) at the V_{BUS} pin ensures that if there is a fault condition at the V_{BUS} line, TPD4S214 is able to isolate it and protect the internal circuitry from damage. Similarly, the under voltage lock out (UVLO) at the V_{OTG_IN} pin ensures that there is no power drain from the internal OTG supply to external V_{BUS} if V_{OTG_IN} droops below a safe operating level. When EN is high, the OTG switch is activated and the $\overline{FLT}$ pin indicates whether there is a fault condition. The soft start feature waits 16 ms to turn on the OTG switch after all operating conditions are met.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (MAX)
TPD4S214	WCSP (12)	1.39 mm × 1.69 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

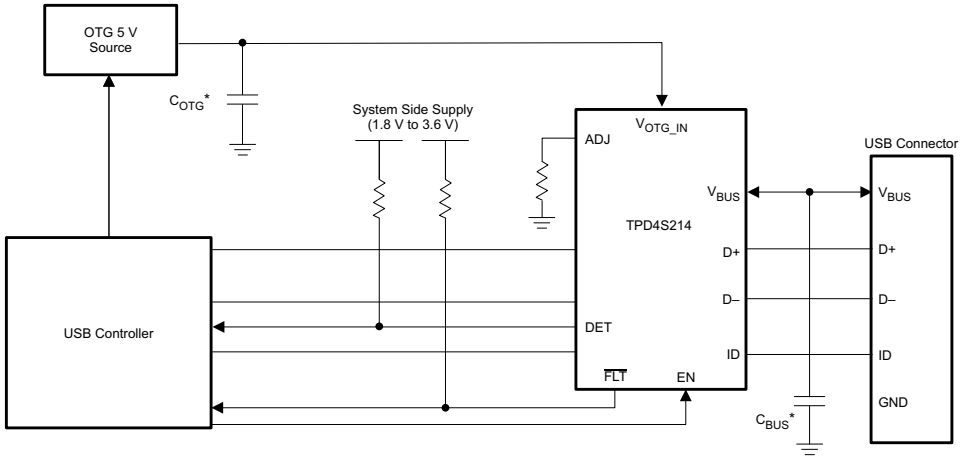


Table of Contents

5 Revision History

Changes from Revision E (January 2015) to Revision F — **Page**

- Added UL and CB certifications. ... 1

Changes from Revision D (October 2014) to Revision E — **Page**

- Added R_{LOAD} TEST CONDITIONS to I_{OCP} in the Electrical Characteristics for Current Limit and Short Circuit Protection table. ... 7

Changes from Revision C (August 2013) to Revision D — **Page**

- Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

Changes from Original (January 2013) to Revision A — **Page**

- Changed the Product Preview data sheet ... 1

Changes from Revision A (February 2013) to Revision B — **Page**

- Changed the device From: Product Preview To: Production data ... 1

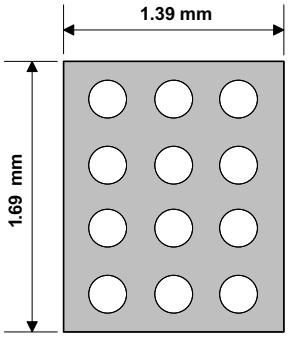
Changes from Revision B (February 2013) to Revision C — **Page**

- YFF PACKAGE Changed the YFF package dimensions ... 3

6 Pin Configuration and Functions

TPD4S214 WCSP (YFF) PIN MAPPING (TOP SIDE/SEE-THROUGH VIEW)

	1	2	3
A	V_{OTG_N}	DET	V_{BUS}
B	V_{OTG_IN}	$\overline{FLT}$	V_{BUS}
C	EN	GND	ID
D	ADJ	D-	D+



Pin Functions

NAME	PIN	TYPE	DESCRIPTION
D–	D2	I/O	USB data–
D+	D3	I/O	USB data+
ID	C3	I/O	USB ID signal
$\overline{FLT}$	B2	O	Open-Drain Output. Connect a pull-up resistor from $\overline{FLT}$ to the supply voltage of the host system.
ADJ	D1	I	Attach external resistor to adjust the current limit
EN	C1	I	Enable Input. Drive EN high to enable the OTG switch.
V_{BUS}	A3, B3	O	USB Power Output
V_{OTG_IN}	A1, B1	I	USB OTG Supply Input
DET	A2	O	Open-Drain Output. Connect a pull-up resistor from DET to the supply voltage of the host system.
GND	C2	Ground	Connect to PCB ground plane

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–40	85	°C
V_{OTG_IN}, ADJ, EN	Input voltage		–0.5	7	V
V_{BUS}	Output voltage to USB connector		–7	30	V
$\overline{FLT}$, DET	Output voltage		–0.5	7	V
	Input clamp current	$V_I < 0$		–50	mA
	I_{OUT} Continuous current through $\overline{FLT}$ and DET output			10	mA
	I_{GND} Continuous current through GND			100	mA
	$T_{J(max)}$ maximum junction temperature		–65	150	°C
D+, D-, ID, V_{BUS} pins	IEC 61000-4-2 Contact Discharge at 25°C			±15	kV
D+, D-, ID, V_{BUS} pins	IEC 61000-4-2 Air-gap Discharge at 25°C			±15	kV
D+, D-, ID pins	Peak Pulse Current (tp = 8/20 µs) at 25°C			7.8	A
D+, D-, ID pins	Peak Pulse Power (tp = 8/20 µs) at 25°C			84	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±500	
		IEC 61000-4-2 Contact Discharge	D+, D-, ID, V_{BUS} Pins	±15000	V
		IEC 61000-4-2 Air-gap Discharge			

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
T_A	Operating free-air temperature		-40		85	°C
V_{IH}	High-level input voltage EN		1.2			V
V_{IL}	Low-level input voltage EN				0.4	V
t_{EN}	EN ramp rate for proper turn on	Valid ramp rate is between 10 µs and 100 ms, rising and falling	0.01		100	ms
t_{UVLO_SLEW}	V_{OTG_IN} ramp rate for proper UVLO operation	Valid ramp rate is between 10 µs and 100 ms, rising and falling	0.01		100	ms
t_{OVLO_SLEW}	V_{BUS} ramp rate for proper OVLO operation	Valid ramp rate is between 10 µs and 100 ms, rising and falling	0.01		100	ms
$T_{A\_VBUS\_ATT}$	Time to detect V_{BUS} device attachment and turn on DET				200	ms

7.4 Thermal Information

THERMAL METRIC(1)		TPD4S214 YFF 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	40.0	
ψ_{JT}	Junction-to-top characterization parameter	3.0	
ψ_{JB}	Junction-to-board characterization parameter	39.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Shutdown

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
T_{SHDN+}	Shutdown temp rising		141		ºC
T_{SHDN-}	Shutdown temp falling		125		ºC
T_{HYST}	Thermal-shutdown Hysteresis		16		ºC
P_{MAX}	Maximum power dissipation	V_{OTG_IN} = 5 V, R_{load} = 5 Ω, EN = 5 V, R_{ADJ} = 75 KΩ		0.16	W
T_{JMAX}	Junction Temp at max power dissipation			150	ºC

7.6 Electrical Characteristics for EN, $\overline{FLT}$, DET, D+, D–, V_{BUS}, ID Pins

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL_EN}	EN pin input leakage current	EN = 3.3 V			1	µA
I_{OL}	$\overline{FLT}$, DET pin output leakage current	$\overline{FLT}$, DET = 3.6 V			1	µA
$V_{OL\_\overline{FLT}}$	Low-level output voltage $\overline{FLT}$	V_{BUS} or V_{OTG_IN} = 5 V or 0 V I_{OL} = 100 µA			100	mV
V_{OL_DET}	Low-level output voltage DET	V_{BUS} and V_{OTG_IN} = 5 V or 0 V I_{OL} = 100 µA			100	mV
C_{EN}	Enable capacitance	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V_{OTG_IN} = 5 V		4.5		pF
V_D	Diode forward voltage D+, D–, ID pins; lower clamp diode	I_O = 8 mA			0.95	V
I_{L_D}	Leakage current on D+, D–, ID Pins	D+, D–, ID = 3.3 V			100	nA
ΔC_{IO}	Differential capacitance between the D+, D– lines	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V_{OTG_IN} = 5 V			0.04	pF
C_{IO}	Capacitance to GND for the D+, D– lines	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V_{OTG_IN} = 5 V		1.9		pF
	Capacitance to GND for the ID lines			1.9		
V_{BR}	Breakdown voltage D+, D–, ID pins	I_{br} = 1 mA	6			V
	Breakdown voltage on V_{BUS}	I_{br} = 1 mA	33			V
R_{DYN}	Dynamic on resistance D+, D–, ID clamps			1		Ω

7.7 Electrical characteristics for UVLO / OVLO

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UNDER-VOLTAGE LOCKOUT						
V_{UVLO+}	Under-voltage lock-out, input power detected threshold rising	V_{OTG_IN} increasing from 0 V to 5 V, No load on V_{BUS} pin	3.4	3.6	3.8	V
$V_{UVLO–}$	Under-voltage lock-out, input power detected threshold falling	V_{OTG_IN} decreasing from 5 V to 0 V, No load on V_{BUS} pin	3.0	3.2	3.5	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	Δ of V_{UVLO+} and $V_{UVLO–}$		260		mV
T_{RUVLO}	Recovery time from UVLO	V_{OTG_IN} increasing from 0V to 5V, No load on V_{BUS} pin; time from V_{OTG_IN} = V_{UVLO+} to $\overline{FLT}$ toggles high		18		ms
T_{RESP_UVLO}	Response time for UVLO	V_{OTG_IN} decreasing from 5V to 0V, No load on V_{BUS} pin; time from V_{OTG_IN} = $V_{UVLO–}$ to $\overline{FLT}$ toggles low		0.18		µs
OUTPUT OVERVOLTAGE LOCKOUT						
V_{OVP+}	OVLO rising threshold	Both V_{OTG_IN} and V_{BUS} increasing from 5 V to 7 V	5.55	6.15	6.45	V
$V_{OVP–}$	OVLO falling threshold	Both V_{OTG_IN} and V_{BUS} decreasing from 7 V to 5 V	5.4	6	6.3	V
$V_{HYS-OVP}$	Hysteresis on OVLO	Δ of V_{UVLO+} and $V_{UVLO–}$		100		mV
T_{ROVLO}	Recovery time from OVLO	Both V_{OTG_IN} and V_{BUS} decreasing from 7 V to 5 V, V_{OTG_IN} = 5 V; time from V_{BUS} = $V_{OVP–}$ to $\overline{FLT}$ toggles high		9		ms
T_{RESP_OVLO}	Response time for OVLO	Both V_{OTG_IN} and V_{BUS} increasing from 5 V to 7 V, V_{OTG_IN} = 5 V; time from V_{BUS} = V_{OVP+} to $\overline{FLT}$ toggles low		17		µs

7.8 Electrical Characteristics for DET Circuits

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BUS\_VALID–}$	Valid V_{BUS} voltage detect	V_{BUS} = 7 V to 0 V	2.7	2.9	3	V
V_{BUS_VALID+}	Valid V_{BUS} voltage detect	V_{BUS} = 0 V to 7 V	5.3	5.4	5.6	V
$T_{DET\_DELAY–}$	V_{BUS} detect propagation delay–	V_{BUS} 0 V to 4 V, 200 ns ramp; V_{BUS} = $V_{BUS\_VALID–\ MIN}$ to DET toggles high		4.9		µs
T_{DET_DELAY+}	V_{BUS} detect propagation delay+	V_{BUS} 6 V to 4 V, 200 ns ramp; V_{BUS} = $V_{BUS\_VALID+\ MAX}$ to DET toggles low		1.8		µs

7.9 Electrical Characteristics for OTG Switch

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{DS_ON}	OTG switch resistance	TA = 25 °C, V_{BUS} = 5 V, IOUT = 100 mA, R_{ADJ} = 75 kΩ (1)			263	290	mΩ
V_{DROP}	OTG switch voltage drop	V_{BUS} = 5 V, IOUT = 100 mA, R_{ADJ} = 75 kΩ			12.6	29	mV
$I_{OTG\_OFF\_30V}$	Leakage current at 30V	Measured at V_{OTG_IN}	V_{BUS} = 30 V, EN = 5 V, V_{OTG_IN} = 5 V		6		µA
			V_{BUS} = 30 V, EN = 5 V, V_{OTG_IN} = 0 V		11		nA
$I_{OTG\_OFF\_2V}$	Leakage current at–2V		V_{BUS} = -2 V, EN = 5 V, V_{OTG_IN} = 5 V		30		µA
I_{OTG_OFF}	Standby Leakage current		V_{BUS} = 0 V, EN = 0 V, V_{OTG_IN} = 5 V		32		µA
			V_{BUS} = 5 V, EN = 0 V, V_{OTG_IN} = 0 V		10		nA
I_{BUS_REV}	Reverse Leakage current		V_{BUS} = 5 V, EN = 5 V, V_{OTG_IN} = 0V		1		nA
			V_{BUS} = 5.5 V, EN = 5 V, V_{OTG_IN} = 5 V		6		µA
T_{ON}	Turn-ON time	R_L = 100 Ω, C_L = 1 µF, R_{ADJ} = 75 kΩ			16		ms
T_{OFF_EN}	Turn-OFF time	R_L = 100 Ω, C_L = 1 µF, R_{ADJ} = 75 kΩ, toggle EN			80		µs
T_{OFF_OTG}	Turn-OFF time	R_L = 100 Ω, C_L = 1 µF, R_{ADJ} = 75 kΩ, toggle V_{OTG_IN}			0.5		µs
T_{RISE}	Output rise time	R_L = 100 Ω, C_L = 1 µF, R_{ADJ} = 75 kΩ			137		µs
T_{FALL}	Output fall time	R_L = 100 Ω, C_L = 1 µF, R_{ADJ} = 75 kΩ			1.6		µs

(1) $R_{DS(ON)}$ is measured at 25°C

7.10 Electrical Characteristics for Current Limit and Short Circuit Protection

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OCP}	Current−limit threshold (maximum DC output current IOUT delivered to load)	V_{OTG_IN} = 5 V, R_{LOAD} = 2.0 Ω	R_{ADJ} = 226 kΩ (1)	235	245	281	mA
			R_{ADJ} = 75 kΩ (1)	735	792	830	
			R_{ADJ} = 62 kΩ (1)	885	959	1005	
			R_{ADJ} = 45 kΩ (1)	1128	1200	1363	
T_{BLANK}	Blanking time after enable	V_{OTG_IN} = 5 V	RL = 1 Ω, CL = 1 µF, RADJ = 75 kΩ		4		ms
T_{DEGL}	Deglitch time while enabled	V_{OTG_IN} = 5 V, RL = 100 Ω, CL = 1 µF, RADJ = 75 kΩ, apply short to ground			9.4		ms
T_{DET_SC}	Response time to short circuit				10		µs
T_{REG}	Short circuit regulation time		Hiccup pulse width; auto-retry time		13		ms
T_{OCP}	Short circuit over current protection time		Hiccup pulse period		153		ms
V_{SHORT}	Short circuit threshold				4		V
I_{INRUSH}	Inrush current during a startup	See Figure 23 under test configuration	RL = 100 Ω, CL = 22 µF, RADJ = 75 kΩ		726		mA

(1) External resistor tolerance is ±1%

7.11 Supply Current Consumption

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
$I_{VOTG\_IN}ON$	High-level V_{OTG_IN} operating current consumption	V_{OTG_IN} = 5 V, No load on V_{BUS}, EN = 5 V	RADJ = 75 kΩ	162	200	µA
			RADJ = 226 kΩ	150	200	µA

7.12 Typical Characteristics

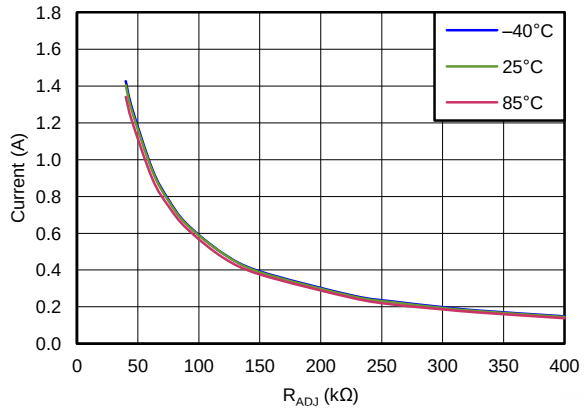


Figure 1. I_{OCP} vs. R_{ADJ}

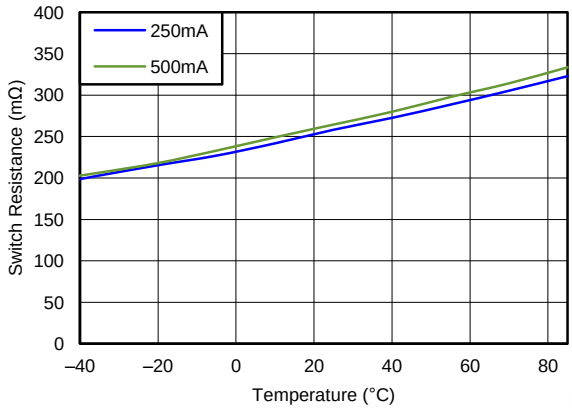


Figure 2. R_{DSON} vs. Temperature

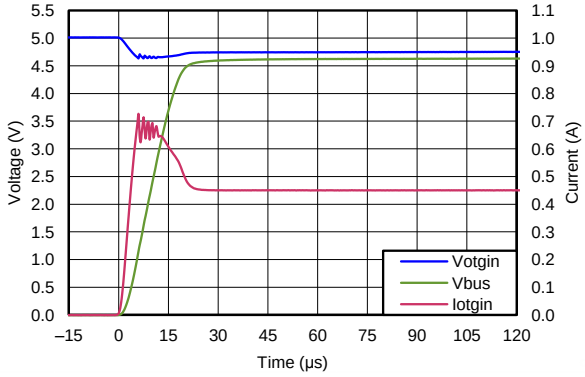


Figure 3. Inrush, R_{ADJ} = 75 kΩ

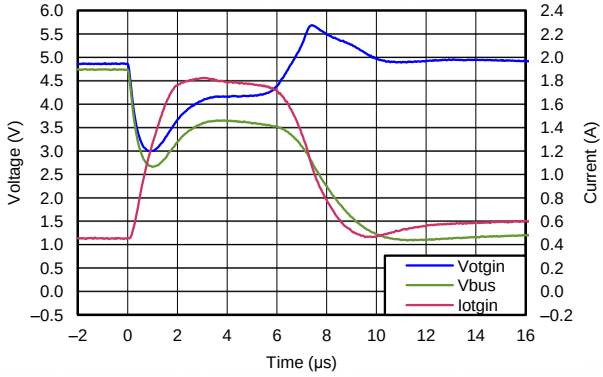


Figure 4. 10 Ω Load to Short, 2 µs

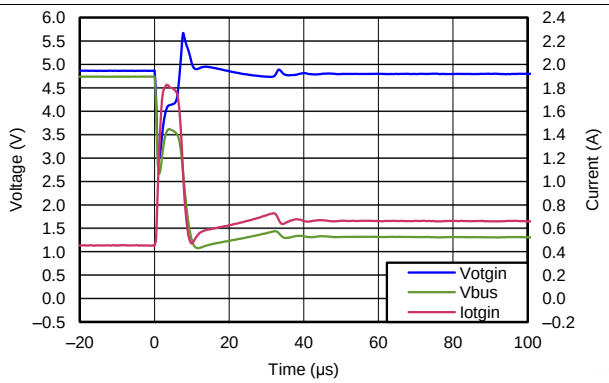


Figure 5. 10 Ω Load to Short, 20 µs

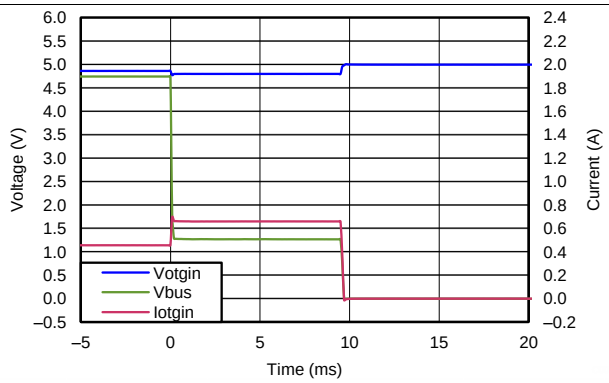


Figure 6. 10 Ω Load to Short, 5 ms

Typical Characteristics (continued)

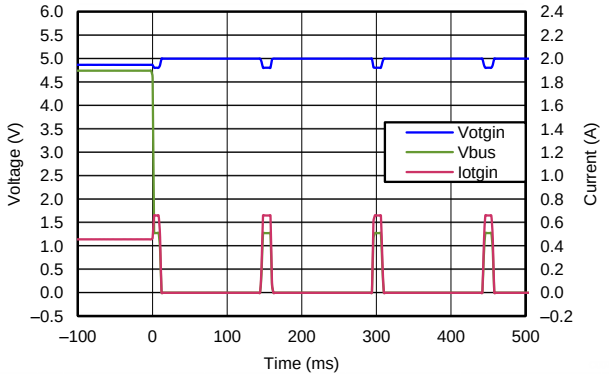


Figure 7. 10 Ω Load to Short, 100 ms

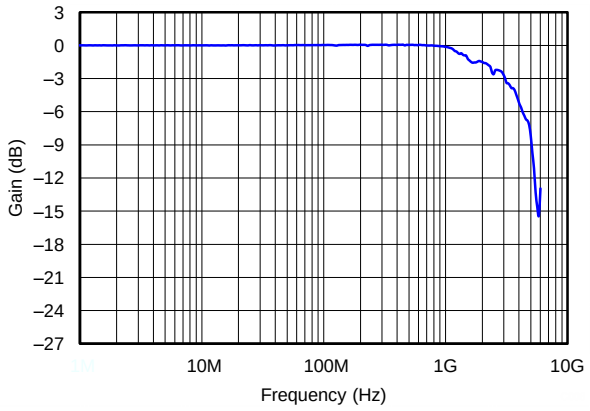


Figure 8. Data Line Insertion Loss

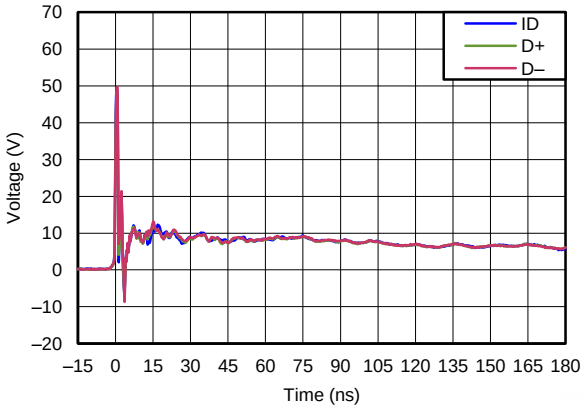


Figure 9. +8 kV Contact, 1 GHz

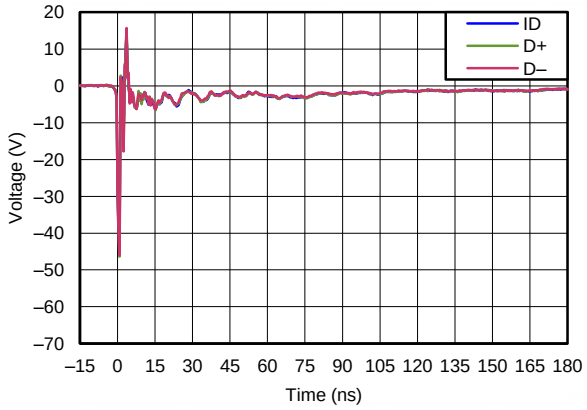


Figure 10. -8 kV Contact, 1 GHz

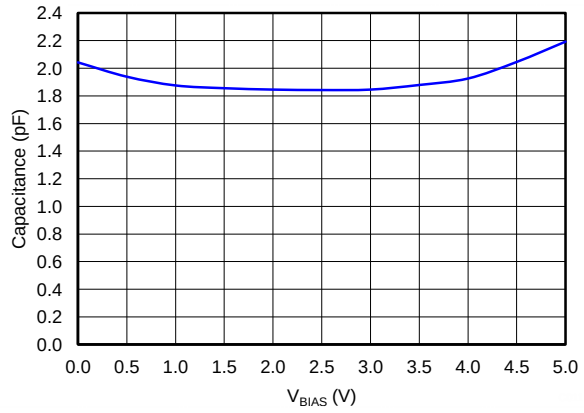


Figure 11. C_{IO} vs. V_{BIAS}, f = 1 MHz

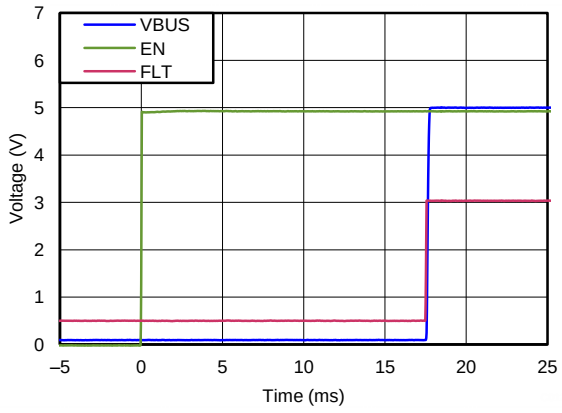


Figure 12. TPD4S214 Turn On Characteristics

Typical Characteristics (continued)

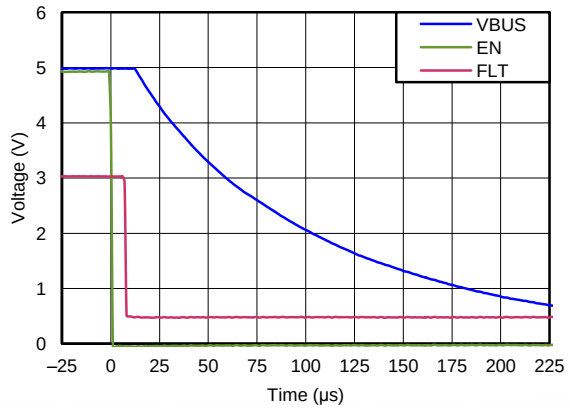


Figure 13. TPD4S214 Turn Off Characteristics

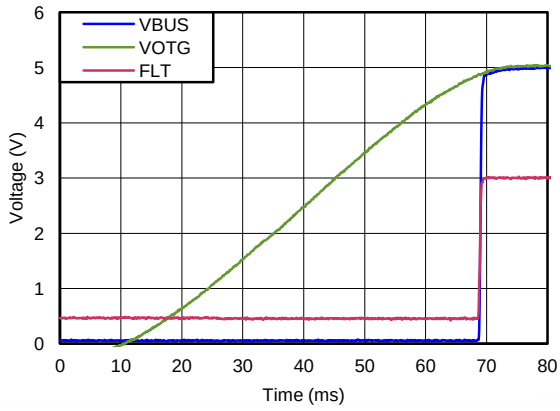


Figure 14. UVLO

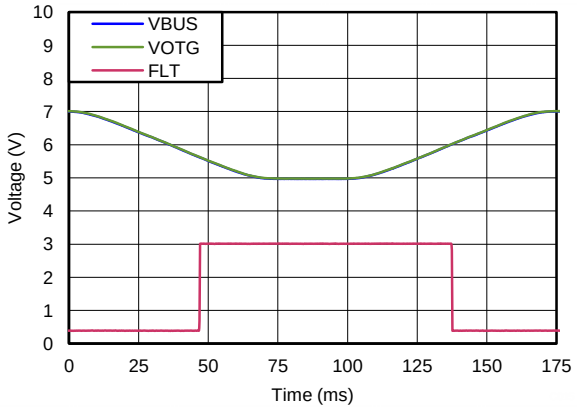


Figure 15. OVLO

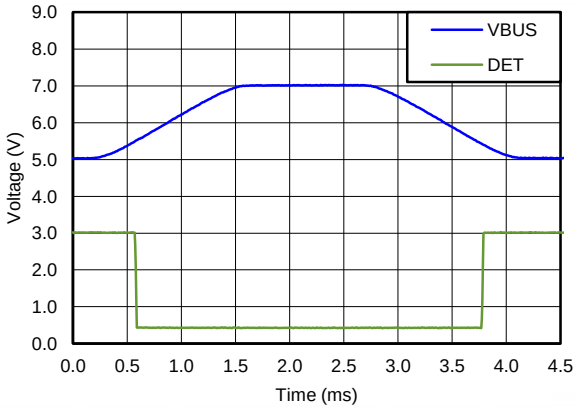


Figure 16. V_{BUS} Valid Detect Upper

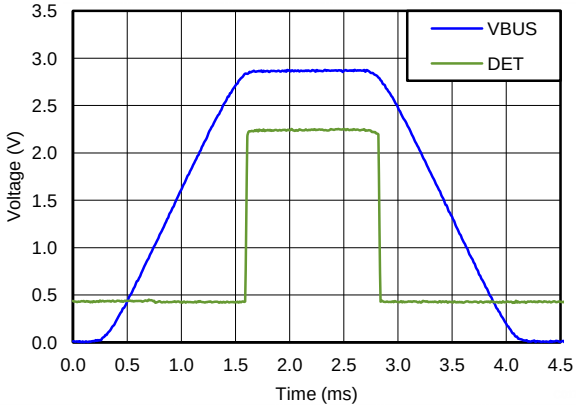


Figure 17. V_{BUS} Valid Detect Lower

8 Detailed Description

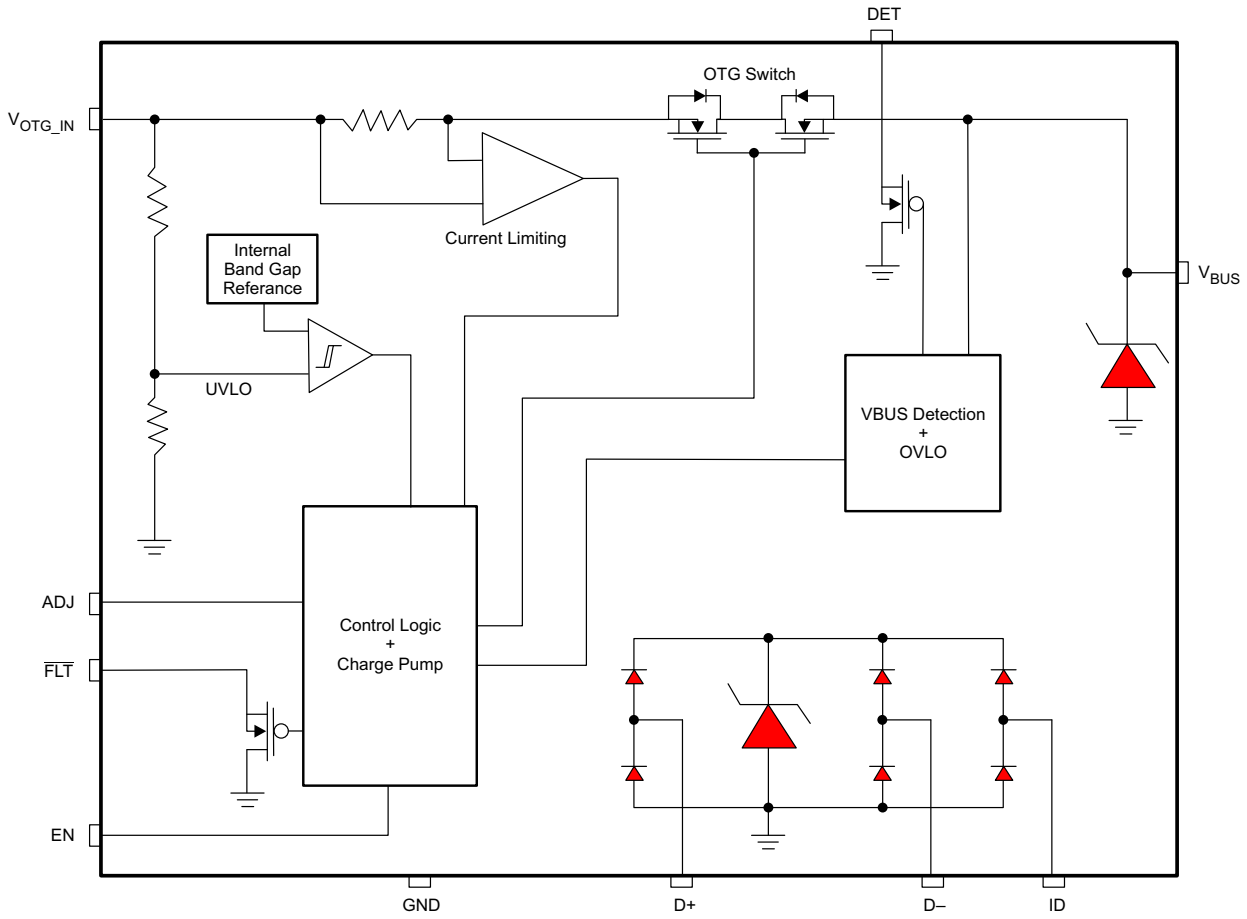
8.1 Overview

The TPD4S214 is a single-chip protection solution for USB On-the-Go and other current limited USB applications. This device includes an integrated low $R_{DS(ON)}$ N-channel current limited switch for OTG current supply to peripheral devices. TPD4S214 offers low capacitance TVS ESD clamps for the D+, D–, and ID pins for both USB2.0 and USB3.0 applications. The V_{BUS} pin can handle continuous voltage ranging from –7 V to 30 V. The OVLO at the V_{BUS} pin ensures that if there is a fault condition at the V_{BUS} line, TPD4S214 is able to isolate it and protect the internal circuitry from damage. Similarly, the UVLO at the V_{OTG_IN} pin ensures that there is no power drain from the internal OTG supply to external V_{BUS} if V_{OTG_IN} droops below a safe operating level.

When EN is high, the OTG switch is activated and the $\overline{FLT}$ pin indicates whether there is a fault condition. The soft start feature waits 16 ms to turn on the OTG switch after all operating conditions are met. The $\overline{FLT}$ pin asserts low during any one of the following fault conditions: OVLO ($V_{BUS} > V_{OVLO}$), UVLO condition ($V_{OTG\_IN} < V_{UVLO}$) over temperature, over current, short circuit condition, or reverse-current-condition ($V_{BUS} > V_{OTG\_IN}$). The OTG switch is turned off during any fault condition. Once the switch is turned off, the IC periodically rechecks the faults internally. If the IC returns to normal operating conditions, the switch turns back on and $\overline{FLT}$ is reset to high.

There is also a V_{BUS} detection feature for facilitating USB communication between USB host and peripheral device. If this is not used, the DET pin can be either floating or connected to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Protection at V_{BUS} from –7 V to 30 V

The V_{BUS} pin can handle continuous voltage ranging from –7 V to 30 V. The OVLO at the V_{BUS} pin ensures that if there is a fault condition at the V_{BUS} line, TPD4S214 is able to isolate the fault and protect the internal circuitry from damage.

8.3.2 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and air gap. An ESD clamp diverts the current to ground.

8.3.3 Low $R_{DS(ON)}$ N-CH FET Switch for High Efficiency

A Low $R_{DS(ON)}$ ensures there is minimal voltage loss when supplying high current to OTG devices.

8.3.4 Compliant with USB2.0 and USB3.0 OTG spec

The capability of TPD4S214 to supply greater than 1.2 A of current on V_{BUS} meets or exceeds the USB2.0 and USB3.0 OTG specification.

8.3.5 User Adjustable Current Limit From 250 mA to Beyond 1.2 A

The designer can select the over current protection level by selecting the proper R_{ADJ}.

8.3.6 Built-in Soft-start

The soft start feature waits 16 ms to turn on the OTG switch after all operating conditions are met.

8.3.7 Reverse Current Blocking

If V_{BUS} is greater than V_{OTG_IN} by 50 mV, the OTG switch is disabled in 17.5 ms.

8.3.8 Over Voltage Lock Out for V_{BUS}

OVLO ensures that an over voltage condition on V_{BUS} disables the OTG switch to protect the system.

8.3.9 Under Voltage Lock Out for V_{OTG_IN}

UVLO ensures that an under voltage condition on V_{BUS} disables the OTG switch to protect the system.

8.3.10 Thermal Shutdown and Short Circuit Protection

TPD4S214 has an over-temperature protection circuit to protect against system faults or improper use. The basic function of the thermal shutdown (TSD) circuit is to sense when the junction temperature has exceeded the absolute maximum rating and shut down the device until the junction temperature has cooled to a safe level. Short circuit protection prevents any damaging current demand from the system.

8.3.11 Auto Retry on any Fault; no Latching off States

In any fault condition, TPD4S214 will reassess V_{BUS}, V_{OTG_IN}, and thermal conditions until a safe state is reached and then enable the OTG switch, eliminating any latched off states.

8.3.12 Integrated V_{BUS} Detection Circuit

TPD4S214 has a V_{BUS} detection feature facilitating communication between the USB host and peripheral device. The use of this feature is optional.

8.3.13 Low Capacitance TVS ESD Clamp for USB2.0 High Speed Data Rate

The High Speed data lines have a capacitance less than 2 pF, supporting a bandwidth greater than 3 GHz. This easily accommodates the 480-Mbps data rate defined in the USB2.0 specification.

Feature Description (continued)

8.3.14 Internal 16ms Startup Delay

The built-in start up delay allows for voltages on V_{BUS} to reach a steady state after which a 1-µA trickle charge slowly turns on the main switch. During the inrush period, the peak inrush current will be limited to no more than the current limit set by the external resistor R_{ADJ}.

8.3.15 Space Saving WCSP (12-YFF) Package

The 1.69 mm × 1.39 mm (Max) WCSP package is valuable in space constrained designs.

8.3.16 Inrush Current Protection

As soon as TPD4S214 is enabled, its logic block detects the presence of any fault conditions highlighted in Table 2. In the absence of any fault condition, a counter waits for 16 ms, after which a 1-µA trickle charge slowly turns on the main switch. During the inrush period, the peak inrush current will be limited to no more than the current limit set by the external resistor R_{ADJ}.

8.3.17 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{OTG_IN} and GND. A 10-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

8.3.18 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_{LOAD} is highly recommended. A C_{LOAD} greater than C_{IN} can cause V_{BUS} to exceed V_{OTG_IN} when the system supply is removed. A C_{IN} to C_{LOAD} ratio of 10 to 1 is recommended for minimizing V_{OTG_IN} dip caused by inrush currents during startup.

8.3.19 Current Limit

The TPD4S214 provides current limiting protection, which is set by an external resistor connected from the ADJ pin to ground shown in Figure 18. The current limiting threshold I_{OCP} is set by the external resistor R_{ADJ}. Figure 19 shows the typical current limit for a corresponding R_{ADJ} value with ±1% tolerance across the operating temperature range.

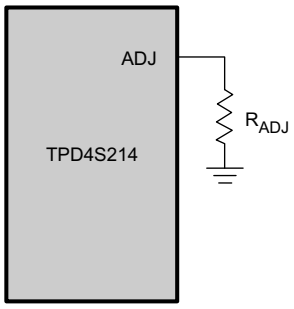


Figure 18. Current Limit Diagram

$$R_{ADJ} = \frac{55.358}{I_{OCP}} \quad (1)$$

Where:

R_{ADJ} = external resistor used to set the current limit (kΩ)
I_{OCP} = current limit set by the external R_{ADJ} resistor (A)

R_{ADJ} is placed between the ADJ pin and ground, shown in Figure 18, providing a maximum current limit between 250 mA and 1.2 A.

Feature Description (continued)

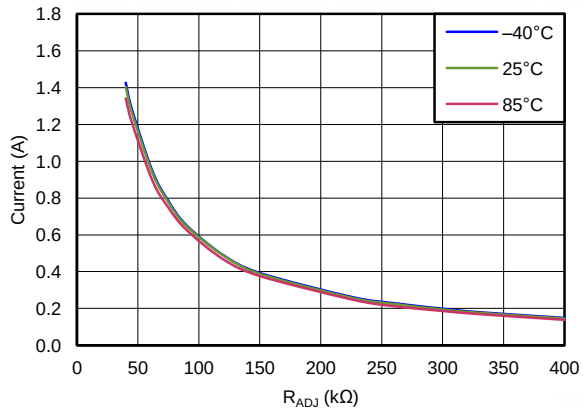


Figure 19. I_{OCP} versus R_{ADJ}

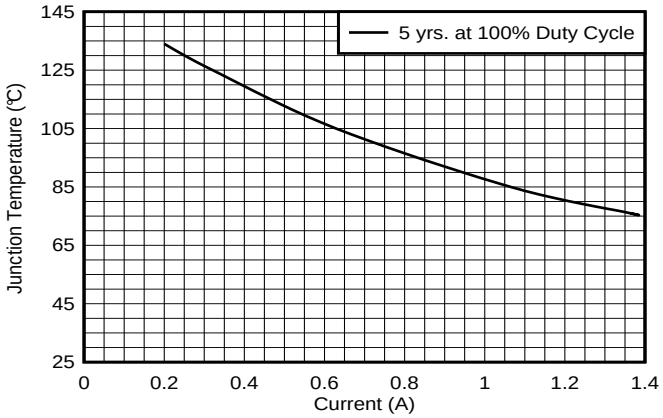


Figure 20. I_{BUS} Temperature Derating Curve

The temperature derating curve shown in Figure 20 graphs the line where TPD4S214 will have a Mean Time Before Failure (MTBF) of 5 years at a 100% duty cycle for a given junction temperature, T_j, and current on V_{BUS}, or I_{BUS}. MTBF of 5 years at a 100% duty cycle is equivalent to 7.5 years at a 75% duty cycle, or 10 years at a 50% duty cycle. See Equation 2 to calculate the junction temperature. If a current and junction temperature point lie below the curve on the graph then the MTBF will exceed 5 years at a 100% duty cycle, or its equivalent. If above the curve, the MTBF will be decreased.

8.3.20 Thermal Shutdown

When the device is ON, current flowing through the device will cause the device to heat up. Overheating can lead to permanent damage to the device. To prevent this, an over temperature protection has been designed into the device. Whenever the junction temperature exceeds 141ºC, the switch will turn off, thereby limiting the temperature. Once the device cools down to below 125ºC the switch will turn on if the EN is active and the V_{BUS} voltage is within the UVLO and OVP thresholds. While the over temperature protection in the device will not kick-in unless the die temperature reaches 141ºC, it is generally recommended that care is taken to keep the junction temperature below 125ºC. Operation of the device above 125ºC for extended periods of time can affect the long-term reliability of the part.

The junction temperature of the device can be calculated using the below formula:

$$T_j = T_A + P_D R_{\theta JA} \quad (2)$$

Where:

T_j = Junction temperature

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance

P_D = Power Dissipated in device

$$P_D = I^2 R_{DS(ON)} \quad (3)$$

I = Current through device

$R_{DS(ON)}$ = Max on resistance of device

Example

At 0.5 A, the continuous current power dissipation is given by:

$$P_D = 0.5^2 \times 0.3 = 0.075\ W \quad (4)$$

If the ambient temperature is about 85 °C the junction temperature will be:

$$T_j = 85 + (0.075 \times 89.1) = 91.7°C \quad (5)$$

Feature Description (continued)

This implies that, at an ambient temperature of 85ºC, TPD4S214 can pass a continuous 0.5 A without sustaining damage. Conversely, the above calculation can also be used to calculate the total continuous current the TPD4S214 can handle at any given temperature.

The MTBF can be estimated by examining Figure 20. Locating 0.5 A and 91.7 °C, the point is below the curve. This implies that the MTBF for this calculation is longer than 5 years at a 100% duty cycle. If the duty cycle is 50% then MTBF exceeds 10 years.

8.3.21 V_{BUS} Detection

There are several important protocols defined in [OTG and EH Supplement] that governs communication between Targeted Hosts (A-device) and USB peripherals (B-device). Communication between host and peripheral is usually done on the ID pin only. In the case when two OTG devices that could both act as either host or peripheral are connected, measuring voltage level on V_{BUS} will aid in the handshaking process. If an embedded host instead of a USB peripheral is connected to the OTG device, OTG charging would not be required and the system's OTG source should remain off to conserve power. The TPD4S214 V_{BUS} detection block aids power conservation and is powered from V_{BUS}. See Functional Block Diagram. The DET pin is an open drain PMOS output with default state low.

In the event when an A-plug is attached, the system detects ID pin as FALSE, in which case ID pin resistance to ground is less than 10 Ω. For a B-plug, the system detects ID pin as TRUE and ID pin resistance to ground is greater than 100 kΩ. For the system to power a USB device through OTG switch once it is connected, voltage on V_{BUS} should remain below $V_{BUS\_VALID\ MIN}$ within $T_{A\_VBUS\_ATT}$ of the ID pin becoming FALSE. After this event, the system confirms that the USB device requires power and enables both TPD4S214 and OTG source. However, if V_{BUS_VALID} is detected on V_{BUS} within $T_{A\_VBUS\_ATT}$ of the ID pin becoming FALSE, there is either a system error or the device connected does not require charging. OTG source remains switched off and the entire sequence would restart when the system detects another FALSE on the ID pin.

Table 1. V_{BUS} Detection scheme

EN	V_{OTG_IN} (V_{BUS} Detect Power)	V_{BUS}	DET	Condition
X	X	$V_{BUS\_VALID}^{-} < V_{BUS} < V_{BUS\_VALID}^{+}$	H	V_{BUS} within V_{BUS_VALID}
X	X	$V_{BUS\_VALID}^{-} > V_{BUS}$ or $V_{BUS} > V_{BUS\_VALID}^{+}$	L	V_{BUS} outside of V_{BUS_VALID}

X = Don't Care, H = Signal High, and L = Signal Low

Figure 21 and Figure 22 shows suggested system level timing diagrams for detecting V_{BUS} according to [OTG and EH Supplement]. Figure 28 shows the application diagram. In Figure 21, DET pin remains low after ID pin becomes FALSE, indicating there is not an active voltage source on V_{BUS}. The USB controller proceeds to turn on OTG 5-V source and the TPD4S214 respectively; this sequence is recommended because TPD4S214 is powered through the OTG source. After a period of t_{ON}, current starts to flow through the OTG switch and V_{BUS} is ramped to the voltage level of V_{OTG_IN}.

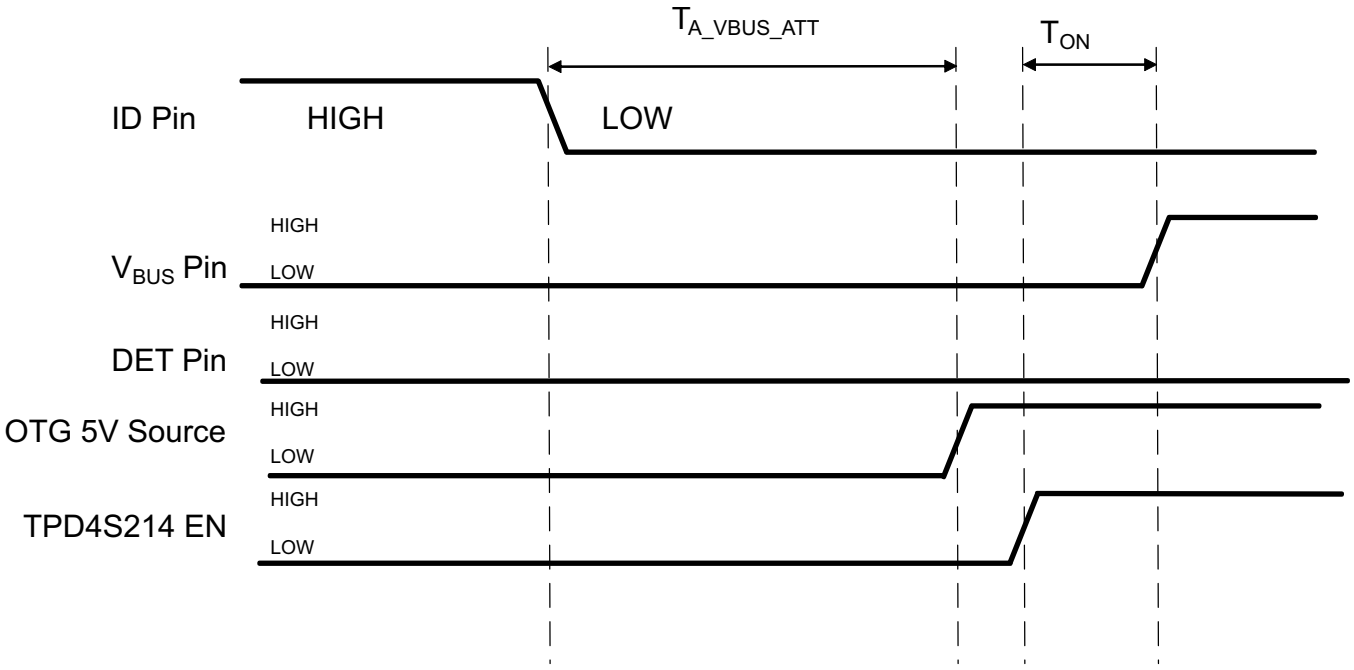


Figure 21. Timing Diagram for Valid USB Device

In Figure 22, DET pin toggles high after an active voltage is detected on V_{BUS} within $T_{A\_VBUS\_ATT}$. This indicates that the USB device attached is not suitable for OTG charging and both OTG 5-V source and TPD4S214 remain off.

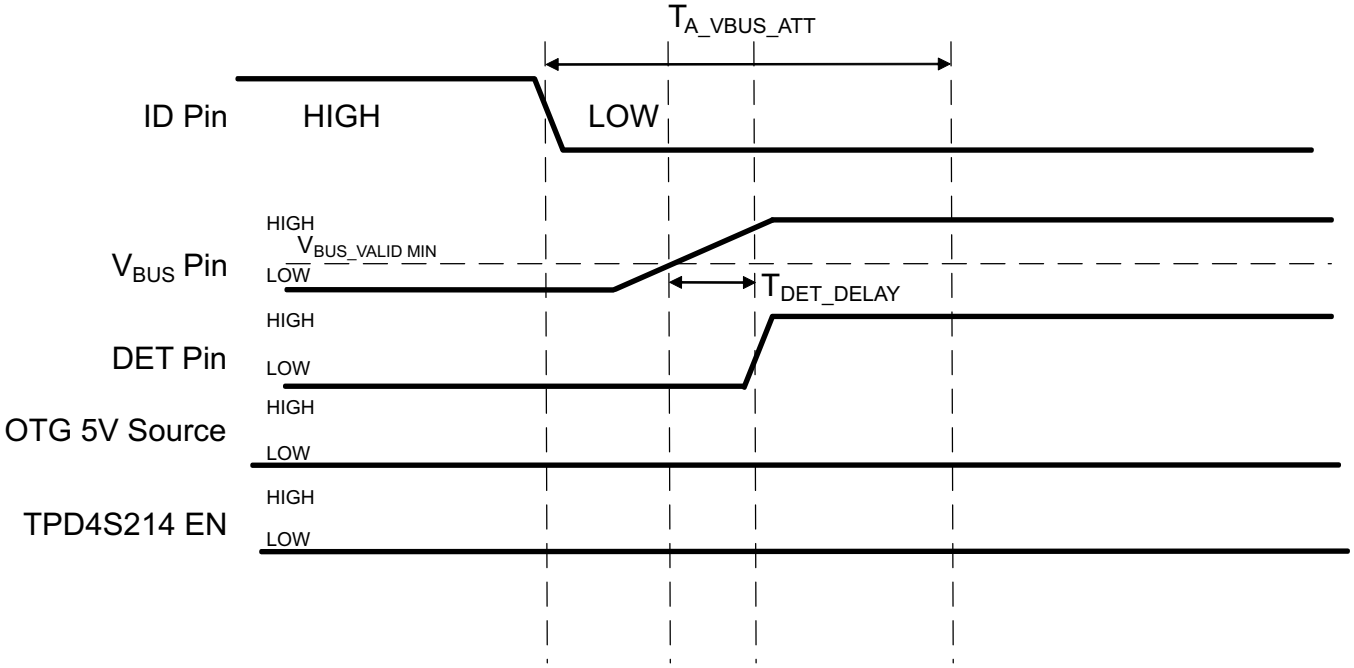


Figure 22. System Level Timing Diagram for invalid USB Device

8.3.22 Test Configuration

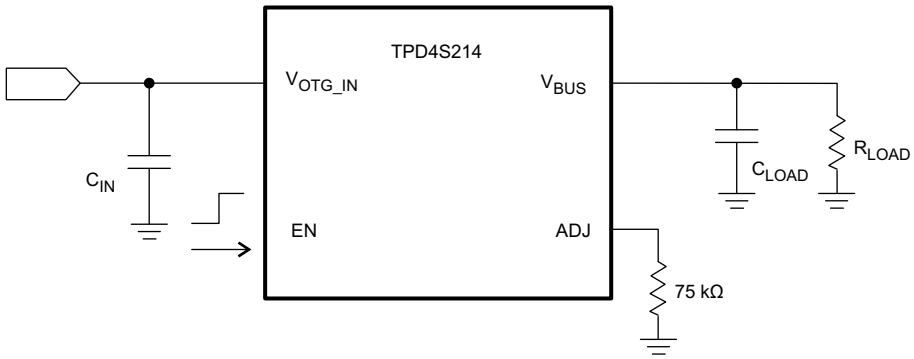


Figure 23. Inrush Current Test Configuration.

Enable is toggled from low to high. See the *Application Information* section for C_{IN} and C_{LOAD} value recommendations.

8.4 Device Functional Modes

Table 2. Device Operation

EN	V_{OTG_IN}	V_{BUS}	OCP	OTP	OTG SW	$\overline{FLT}$	FAULT CONDITION
X	0	0	F	F	OFF	L	SW Disabled
X	X	X	X	T	OFF	L	Over Temperature
H	X	X	T	X	OFF	L	Over Current
H	$V_{OTG\_IN} > V_{UVLO}$	$V_{BUS} > V_{OTG\_IN}$	F	F	OFF	L	Reverse-current
H	X	$V_{BUS} > V_{OVLO}$	F	F	OFF	L	V_{BUS} over-voltage
H	$V_{OTG\_IN} < V_{UVLO}$	X	F	F	OFF	L	V_{OTG_IN} under-voltage
H	$V_{OTG\_IN} > V_{BUS}$ and $V_{OTG\_IN} > V_{UVLO}$	$V_{SHORT} < V_{BUS} < V_{OTG\_IN}$ and $V_{SHORT} < V_{BUS} < V_{OVLO}$	F	F	ON	H	Normal (SW Enabled)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A USB OTG device's one and only connector is the AB receptacle, which accepts either an A or B plug. When an A-plug is inserted, the OTG device is called the A-device and when a B-plug is inserted it is called the B-device. A-device is often times referred to as "Targeted Host" and B-device as "USB peripheral". TPD4S214 supports an OTG device when TPD4S214's system is acting as an A-device and powering the USB interface. The TPD4S214 may also be used in non-OTG applications where it resides on the current source side.

9.2 Typical Application

The TPD4S214 is placed next to the USB connector to provide over voltage, over current, and ESD protection for the OTG 5-V source and USB Controller.

9.2.1 USB 2.0 Without Using On-chip V_{BUS} Detect

An example using TPD4S214 to protect an OTG 5-V source and USB 2.0 Controller is shown below. This USB Controller does not utilize V_{BUS} detection with the DET pin, so DET is tied to GND. TPD4S214 is placed in the transmitter channel immediately adjacent to the USB connector. The D+, D-, ID pins on TPD4S214 are interchangeable so that each can protect either of the D+, D-, ID pins on the USB connector, the naming convention is just a suggestion.

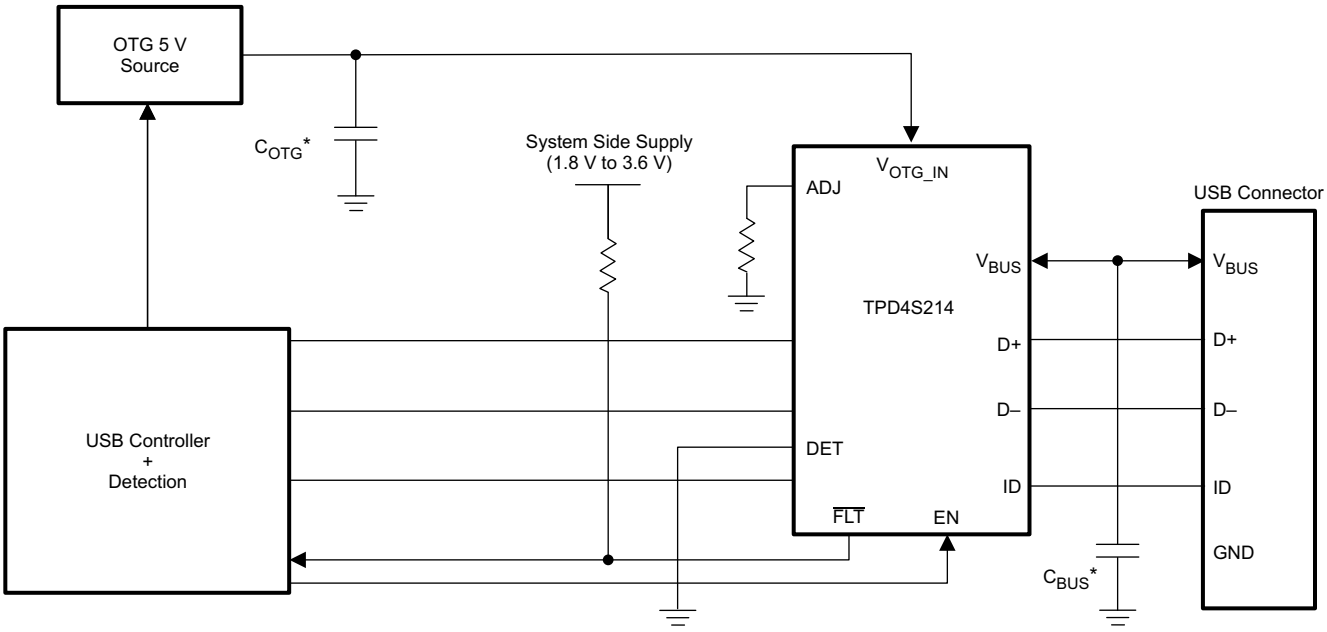


Figure 24. USB2.0 Application Diagram Without Using On-chip V_{BUS} Detect

*C_{OTG} and C_{BUS} have minimum recommended values of 1 µF each

Typical Application (continued)

9.2.1.1 Design Requirements

For this example, use the following table as input parameters:

Design Parameters	Example Value
Signal range on V_{OTG_IN}	3.8 V – 5.5 V
Signal range on V_{BUS}	0 V – 5.3 V nominal, withstand -7 V to 30 V
I_{BUS_MAX}	500 mA
R_{ADJ}	100 kΩ
Drive EN low (disabled)	0 V – 0.4 V
Drive EN high (enabled)	1.2 V – 5.5 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the maximum current expected under normal usage. In this example, the maximum expected current is 500 mA so an R_{ADJ} of 100 kΩ was selected to begin current limiting at around 550 mA and protect the OTG system. Fault conditions are monitored by the USB controller by using the $\overline{FLT}$ Pin. DET is not used and is grounded and can optionally be left floating instead.

9.2.1.3 Application Curves

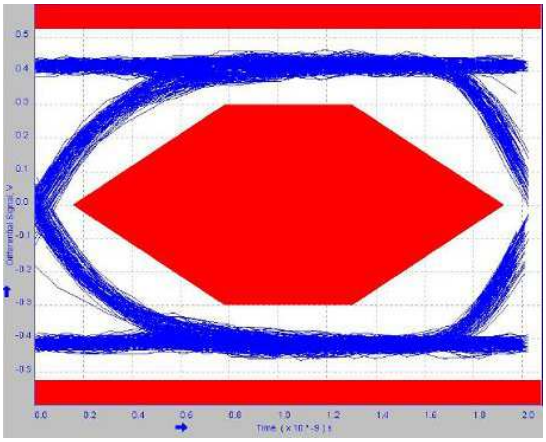


Figure 25. Eye Diagram with no EVM and no IC, Full USB2.0 Speed at 480 Mbps

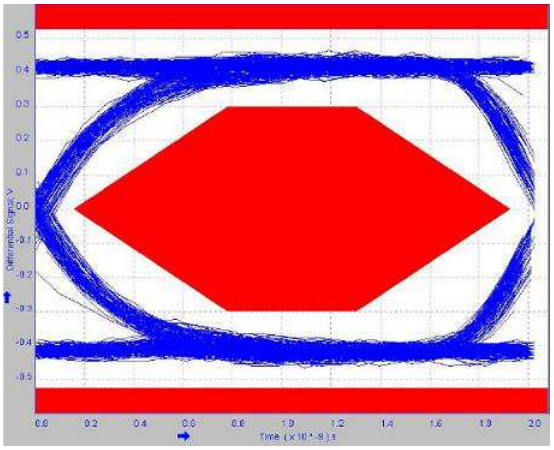


Figure 26. Eye Diagram with TPD4S214EVM but no IC, Full USB2.0 Speed at 480 Mbps

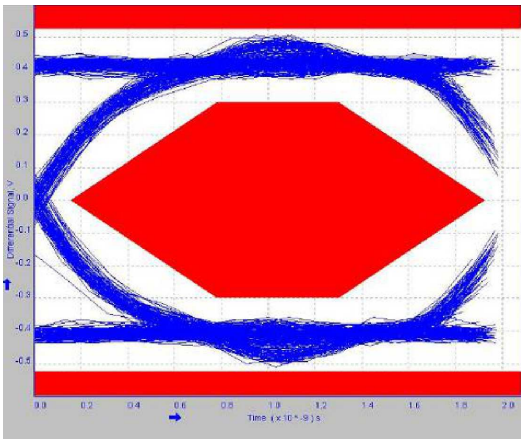


Figure 27. Eye Diagram with TPD4S214EVM and IC, Full USB2.0 Speed at 480 Mbps

9.2.2 USB 2.0 Using On-chip V_{BUS} Detect

An example using TPD4S214 to protect an OTG 5-V source and USB 2.0 Controller is shown below. This USB Controller monitors V_{BUS} detection with the DET pin. This can be advantageous when a peripheral with an Embedded Host is attached. In this case, if there is a valid voltage present on V_{BUS} there is no need to provide OTG power, so the USB Controller can be programmed to disable the OTG 5-V source, resulting in a power savings. The D+, D-, ID pins on TPD4S214 are interchangeable so that each can protect either of the D+, D-, ID pins on the USB connector, the naming convention is just a suggestion.

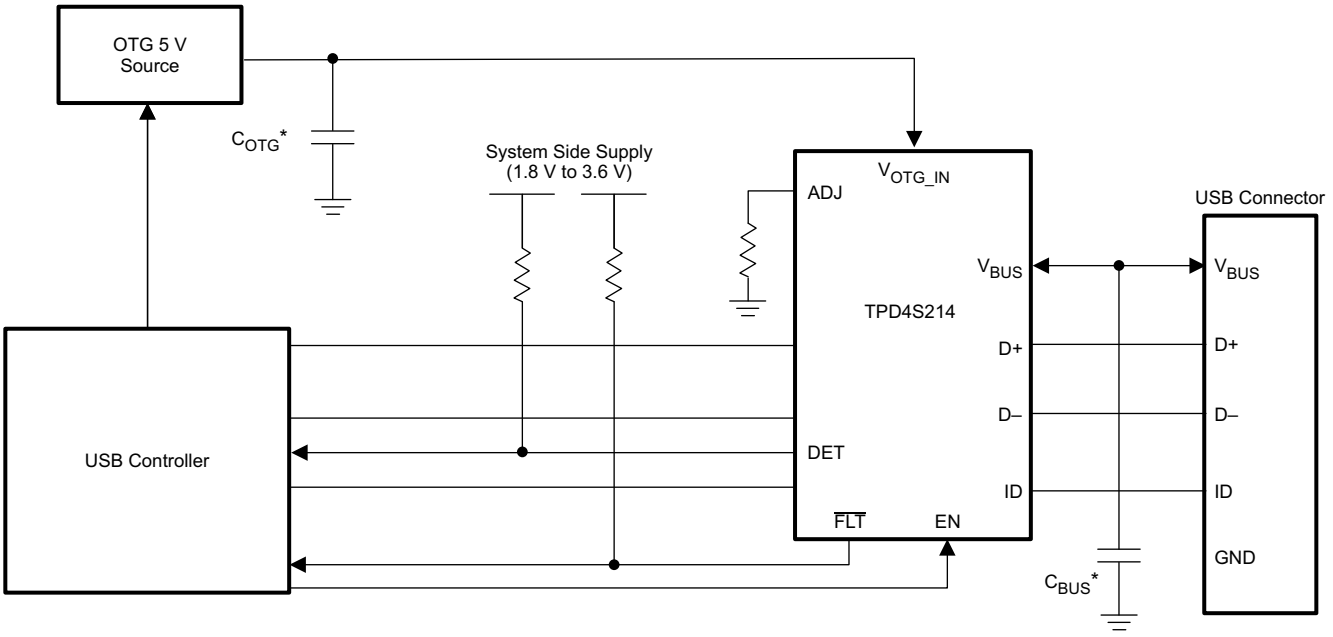


Figure 28. USB 2.0 Application Diagram Using On-chip V_{BUS} Detect

*C_{OTG} and C_{BUS} each have minimum recommended values of 1 µF

9.2.2.1 Design Requirements

For this example, use the following table as input parameters:

Design Parameters	Example Value
Signal range on V_{OTG_IN}	3.8 V – 5.5 V
Signal range on V_{BUS}	0 V – 5.3 V nominal, withstand –7 V to 30 V
I_{BUS_MAX}	500 mA
R_{ADJ}	100 kΩ
Drive EN low (disabled)	0 V – 0.4 V
Drive EN high (enabled)	1.2 V – 5.5 V

9.2.2.2 Detailed Design Procedure

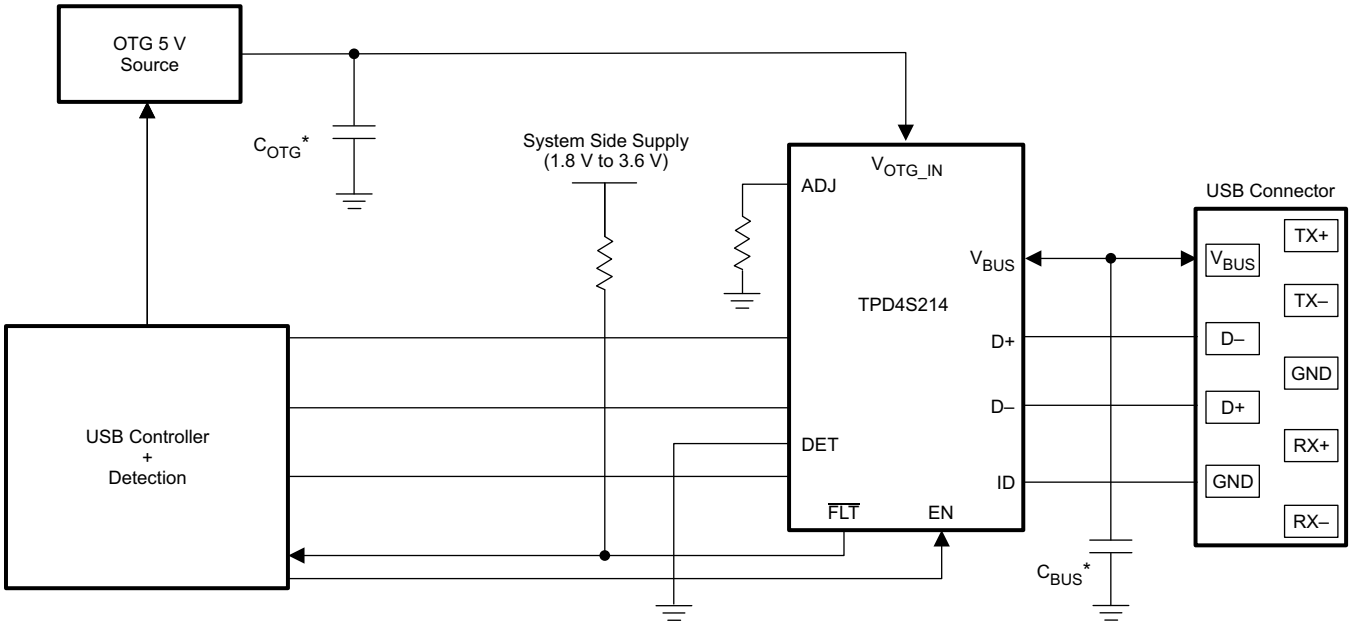
To begin the design process, determine the maximum current expected under normal usage. In this example, the maximum expected current is 500 mA so an R_{ADJ} of 100 kΩ was selected to begin current limiting at around 550 mA and protect the OTG system. Fault conditions are monitored by the USB controller by using the $\overline{FLT}$ Pin. DET Pin is used to facilitate detecting between a USB host and peripheral device on V_{BUS}.

9.2.2.3 Application Curves

Refer to *Application Curves* for related application curves.

9.2.3 USB 3.0 Without Using On-chip V_{BUS} Detect

An example using TPD4S214 to protect an OTG 5-V source and USB 3.0 Controller is shown below. This USB Controller does not utilize V_{BUS} detection with the DET pin, so it is tied to GND. The D+, D-, ID pins on TPD4S214 are interchangeable so that each can protect either of the D+, D-, ID pins on the USB connector, the naming convention is just a suggestion.



*C_{BUS} and C_{OTG} each have minimum recommended values of 1 µF

Figure 29. USB 3.0 Application Diagram Without Using On-chip V_{BUS} Detect

9.2.3.1 Design Requirements

For this example, use the following table as input parameters:

Design Parameters	Example Value
Signal range on V_{OTG_IN}	3.8 V – 5.5 V
Signal range on V_{BUS}	0 V – 5.3 V nominal, withstand –7 V to 30 V
I_{BUS_MAX}	900 mA
R_{ADJ}	56 kΩ
Drive EN low (disabled)	0 V – 0.4 V
Drive EN high (enabled)	1.2 V – 5.5 V

9.2.3.2 Detailed Design Procedure

To begin the design process, determine the maximum current expected under normal usage. In this example, the maximum expected current is 900 mA so an R_{ADJ} of 56 kΩ was selected to begin current limiting at around 1 A and protect the OTG system. Fault conditions are monitored by the USB controller by the $\overline{FLT}$ Pin. DET is not used and is grounded and can optionally be left floating instead.

9.2.3.3 Application Curves

Refer to *Application Curves* for related application curves.

10 Power Supply Recommendations

TPD4S214 Is designed to receive power from an OTG 5-V power source. It can operate normally (nFET ON) between 3.8 V and 5.55 V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for TPD4S214 to be able to switch the nFET ON is between 3.8 V + V_{RIPPLE} and 5.55 V – V_{RIPPLE}.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Avoid using VIAs between the connecter and an I/O protection pin on TPD4S214.
- Avoid 90º turns in traces.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Minimize impedance on the path to GND for maximum ESD dissipation.
- The capacitors on V_{BUS} and V_{OTG_IN} should be placed close to their respective pins on TDP4S214.

11.2 Layout Example

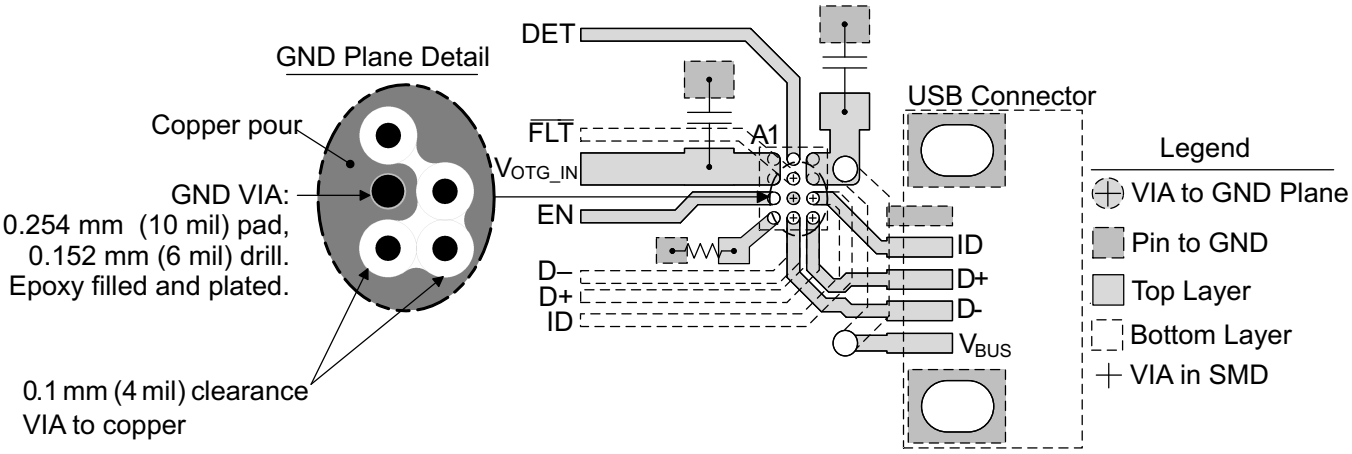


Figure 30. TPD4S214 Layout Example

Successful dissipation of an ESD event is largely dependent on minimizing the impedance along the designated electrical path to ground. For this reason any TVS, including TPD4S214, needs to have the lowest possible impedance to GND. The BGA footprint of this device constrains the path to ground through a VIA in the GND pad of TPD4S214. Due to the "skin effect," maximizing the surface area of the VIA minimizes the impedance of the path to GND. For this reason make both the VIA pad diameter and the VIA drill diameter as large as possible, thus maximizing the surface area of the outside of the VIA surface and the inside of the VIA surface. The GND plane should not be broken in the vicinity of the GND VIA. If possible, attaching the GND VIA to a GND plane on multiple layers minimizes the impedance. The GND VIA should be filled with a non-conductive filler (like epoxy) as opposed to a conductive filler, in order to keep the surface area of the inside of the VIA created by the drill. The GND VIA should be plated over at the SMD pad.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

OTG and EH Supplement: *On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification*, July 14th, 2011. www.usb.org

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4S214YFFR	Active	Production	DSBGA (YFF) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B3214
TPD4S214YFFR.A	Active	Production	DSBGA (YFF) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B3214

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

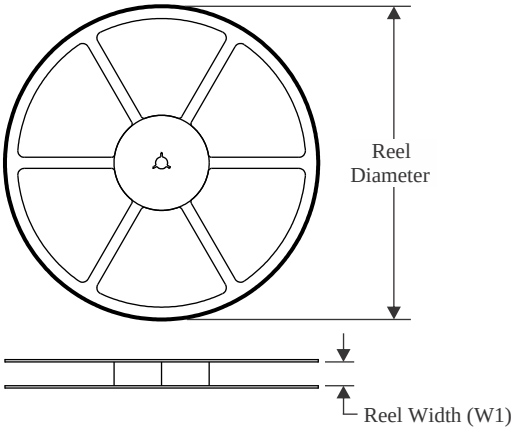
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

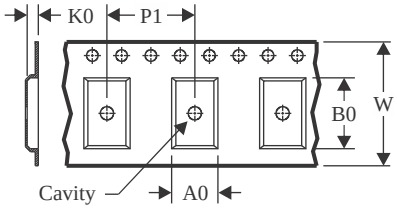
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

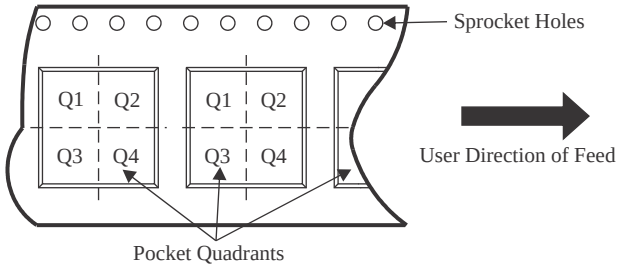


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

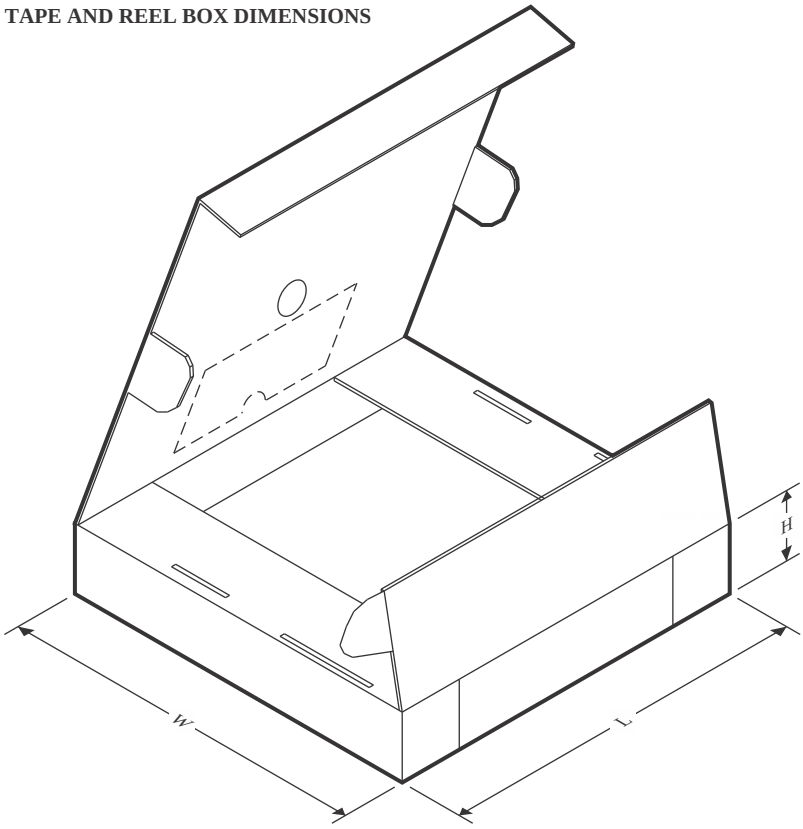
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S214YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.48	1.78	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

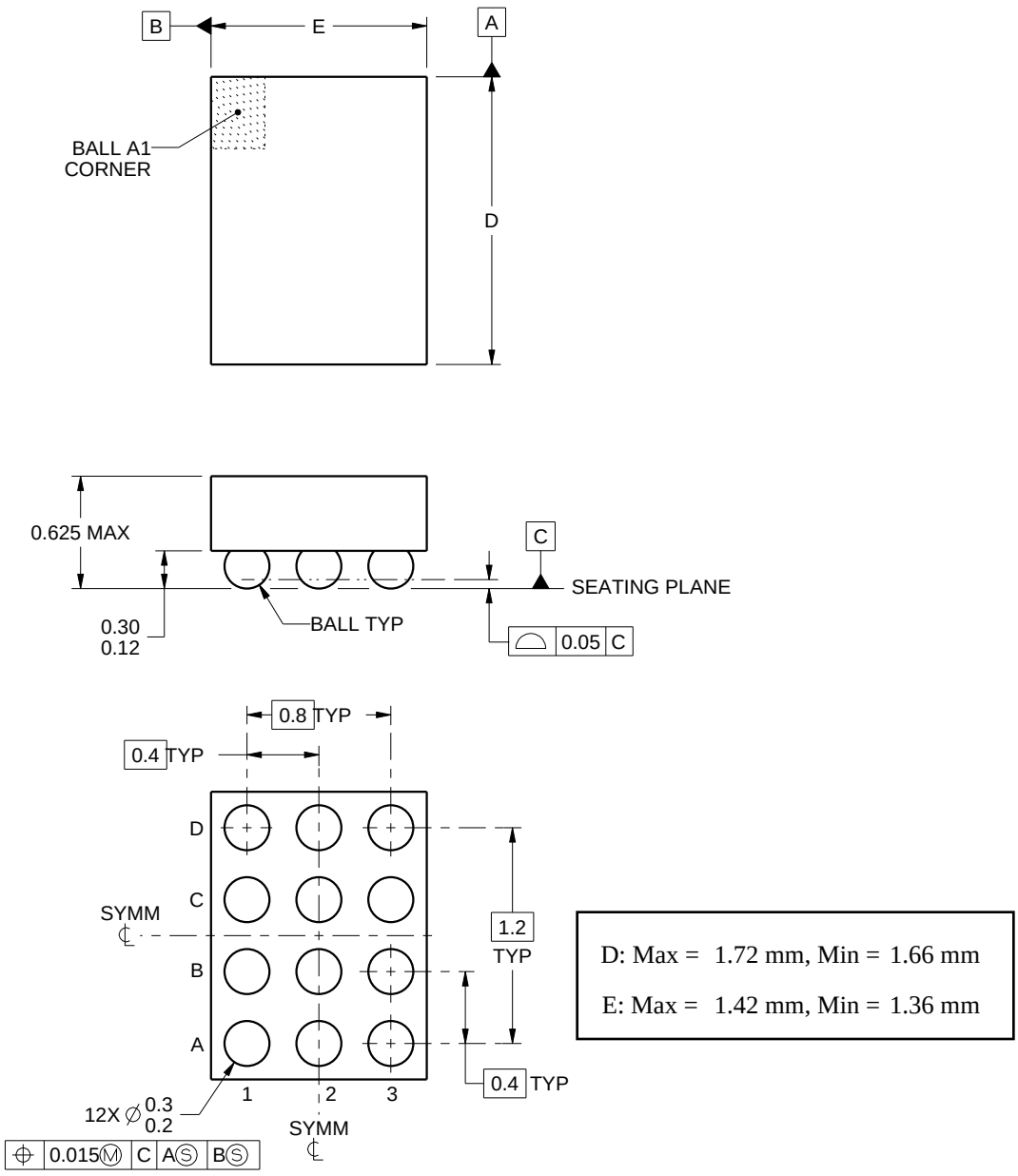
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S214YFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0012

DSBGA - 0.625 mm max height

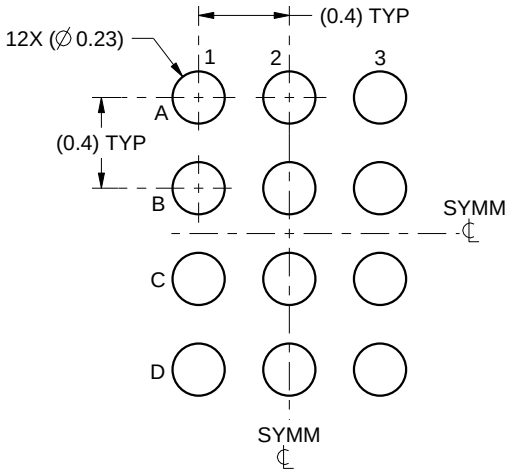
DIE SIZE BALL GRID ARRAY



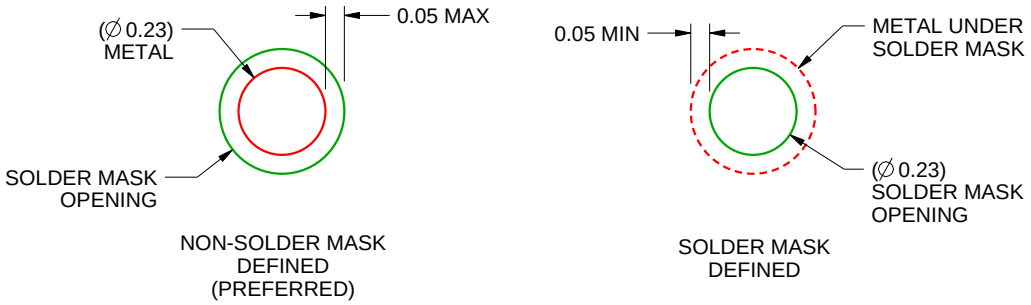
4222191/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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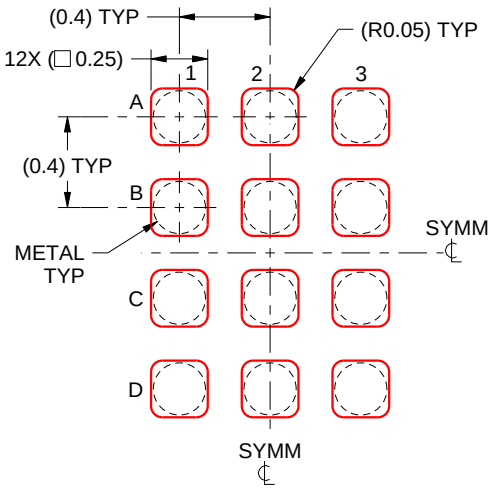
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222191/A 07/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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