AM263Px Sitara™ Microcontrollers

1 Features

Processor Cores:

- Single, dual, and quad-core Arm® Cortex®-R5F MCU with each core running up to 400MHz
  - 16KB I-cache with 64-bit ECC per CPU core
  - 16KB D-cache with 32-bit ECC per CPU core
  - 256KB Tightly-Coupled Memory (TCM) with 32-bit ECC per CPU core cluster
  - Lockstep or Dual-core capable clusters
- Trigonometric Math Unit (TMU) for accelerating trigonometric functions
  - Up to 4x, one per R5F MCU core

Memory Subsystem:

- 3MB of On-Chip RAM (OCSRAM)
  - 6 Banks x 512KB
  - ECC error protection
  - Internal DMA engine support
  - Remote L2 Cache for external memory, software programmable up to 128KB per CPU core

System on Chip (SoC) Services and Architecture:

- 1x EDMA to support data movement functions
- Device Boot supported from the following interfaces:
  - UART (Primary/Backup)
  - QSPI NOR Flash (4S/1S) (Primary)
  - OSPI NOR Flash (8S 50MHz SDR Mode0, 8S 25MHz DDR XSPI) (Primary)
- Interprocessor communication modules
  - SPINLOCK module for synchronizing processes running on multiple cores
  - MAILBOX functionality implemented through CTRLMMR registers
- Central Platform Time Sync (CPTS) support with time-sync and compare-event interrupt routers

Flash Memory Interfaces:

- 1x Flash Subsystem with OptiFlash memory technology and eXecute In Place (XIP) support
  - 1x Octal Serial Peripheral Interface (OSPI), up to 133MHz SDR and DDR
- 1x 4-bit Multi-Media Card/Secure Digital (MMC/SD) interface

General Connectivity:

- 6x Universal Asynchronous RX-TX (UART)
- 8x Serial Peripheral Interface (SPI) controllers
- 5x Local Interconnect Network (LIN) ports
- 4x Inter-Integrated Circuit (I2C) ports
- 8x Modular Controller Area Network (MCAN) modules with CAN-FD support
- 4x Fast Serial Interface Transmitters (FSITX)
- 4x Fast Serial Interface Receivers (FSIRX)
- Up to 139 General-Purpose I/O (GPIO) pins

Sensing & Actuation:

- Real-time Control Subsystem (CONTROLSS)
- Flexible Input/Output Crossbars (XBAR)
- 5x 12-bit Analog-to-Digital Converters (ADC)
  - 6-input SAR ADC up to 4MSPS
    - 6x Single-ended channels **OR**
    - 3x Differential channels
  - Highly Configurable ADC Digital Logic
    - XBAR Start of Conversion Triggers (SOC)
    - User-defined Sample and Hold (S+H)
    - Flexible Post-Processing Blocks (PPB)
- 1x Resolver with up to 2x resolver to digital converters and dedicated ADCs
  - 2x 12-bit ADCs can also be used for general purpose
    - 4-input SAR ADC up to 3MSPS
      - 4x Single-ended channels **OR**
      - 2x Differential channels
- 10x Analog Comparators with Type-A programmable DAC reference (CMPSSA)
- 10x Analog Comparators with Type-B programmable DAC reference (CMPSSB)
- 1x 12-bit Digital-to-Analog Converter (DAC)
- 32x Pulse Width Modulation (EPWM) modules
  - Single or Dual PWM channels
  - Advanced PWM Configurations
  - Extended HRPWM time resolution
- 16x Enhanced Capture (ECAP) modules
- 3x Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2x 4-Ch Sigma-Delta Filter Modules (SDFM)
- Additional Signal-multiplex Crossbars (XBAR)

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Industrial Connectivity:

- Programmable Real-Time Unit (PRU-SS) and PRU-Industrial Communication Subsystem (PRU-ICSS)
  - Dual core Programmable Realtime Unit Subsystem (PRU0 / PRU1)
    - Deterministic Hardware
    - Dynamic Firmware
  - 20-channel enhanced input (eGPI) per PRU
  - 20-channel enhanced output (eGPO) per PRU
  - Embedded Peripherals and Memory
    - 1x UART, 1x ECAP
    - 1x MDIO, 1x IEP,
    - 1x 32KB Shared General Purpose RAM
    - 2x 8KB Shared Data RAM
    - 1x 16KB IRAM per PRU
    - ScratchPad (SPAD), MAC/CRC
  - Digital encoder and sigma-delta control loops
  - The PRU-ICSS enables advanced industrial protocols including:
    - EtherCAT®, Ethernet/IP™,
    - PROFINET®, IO-Link® for order
  - Dedicated Interrupt Controller (INTC)
  - Dynamic CONTROLSS XBAR Integration

High-Speed Interfaces:

- Integrated Ethernet switch supporting up to two external ports
  - MII (10/100), RMII (10/100), or RGMII (10/100/1000)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - 512x ALE engine-based Packet Classifiers
  - Priority flow control with up to 2KB packet size
  - Four CPU hardware interrupt pacing
  - IP/UDP/TCP checksum offload in hardware

Security:

- Hardware Security Module (HSM) with support for Auto SHE 1.1/EVITA
- Secure boot support
  - Device Take Over Protection
  - Hardware-enforced root-of-trust
  - Authenticated boot
  - SW Anti-rollback protection
- Debug security
  - Secure device debug only after proper authentication
  - Ability to disable device debug functionality
- Device ID and Key Management
  - Support for OTP Memory (FUSEROM)
    - Store root keys & other security fields
  - Separate EFUSE controllers and FUSE ROMs
  - Unique Public Device Identifiers (UIDs)
- Memory Protection Units (MPU)
  - Dedicated Arm® MPU per Cortex®-R5F core
  - System MPU - present at various interfaces in the SoC (MPU or Firewall)
  - 8-16 Programmable Regions
    - Enable/Privilege ID
    - Start/End Address
    - Read/Write/Cachable
    - Secure/Non-Secure
- Cryptographic Acceleration
  - Cryptographic cores with DMA Support
  - AES - 128/192/256-bit key sizes
  - SHA2 - 256/384/512-bit support
  - DRBG with pseudo and true random number generator
  - PKA (public key accelerator) to assist in RSA/ECC processing

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Functional Safety:

- Enables design of systems with functional safety requirements
  - Error Signaling Module (ESM) with designated SAFETY_ERRORn pin
  - ECC or parity on calculation-critical memories
  - Built-In Self-Test (BIST) and fault-injection for CPU and on-chip RAM
  - Runtime internal diagnostic modules including voltage, temperature, and clock monitoring, windowed watchdog timers, CRC engines for memory integrity checks
- Functional Safety-Compliant targeted [Industrial]
  - Developed for functional safety applications
  - Documentation to be made available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL-3 targeted
  - Hardware integrity up to SIL-3 targeted
  - Safety-related certification
    - IEC 61508 planned
- Functional Safety-Compliant targeted [Automotive]
  - Developed for functional safety applications
  - Documentation to be made available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL-D targeted
  - Hardware integrity up to ASIL-D targeted
  - Safety-related certification
    - ISO 26262 planned

Optimal Power Management Solution

- Recommended **TPS653860-Q1** Power Management ICs (PMIC)
  - Companion PMIC specially designed to meet device power supply requirements
  - Flexible mapping and factory programmed configurations to support different use cases

Technology / Package:

- AEC-Q100 qualified for automotive applications
- 45nm technology
- ZCZ Package
  - AM263x Compatible (ZCZ-C)
    - Pin-to-Pin compatible option with AM263x
  - AM263Px Resolver (Sensor) (ZCZ-S)
  - AM263Px SIP Resolver (Sensor) (ZCZ-S)
    - Includes 1x internally connected 64Mb ISSI IS25LX064-LWLA3 OSPI Flash device in package; up to 133MHz SDR and DDR
  - 324-pin NFBGA
  - 15.0mm x 15.0mm
  - 0.8mm pitch

2 Applications

- AC Inverter & VF Drives
- Battery Management Systems
- Combo box Architectures
- DC-DC Converters
- Domain Controllers
- EV Charging
- IO Aggregators
- Onboard Chargers
- Renewable Energy Storage
- Single & Multi Axis Servo Drives
- Solar Energy
- Telematics
- Traction Inverters

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3 Description

The AM263Px Sitara™ Arm® Microcontrollers are built to meet the complex real-time processing needs of next generation industrial and automotive embedded products. The AM263Px MCU family consists of multiple pin-to-pin compatible devices with up to four 400MHz Arm® Cortex®-R5F cores. As an option, the Arm® R5F subsystem can be programmed to run in lockstep or dual-core mode for multiple functional safety configurations. The industrial communications subsystem (PRU-ICSS) enables integrated industrial Ethernet communication protocols such as PROFINET®, Ethernet/IP®, EtherCAT® (among many others), standard Ethernet connectivity, and even custom I/O interfaces. The family is designed for the future of motor control and digital power applications with advanced analog sensing and digital actuation modules.

The multiple R5F cores are arranged in cluster subsystems with 256KB of shared tightly coupled memory (TCM) along with 3MB of shared SRAM, greatly reducing the need for external memory. Extensive ECC is included for on-chip memories, peripherals, and interconnects for enhanced reliability. Granular firewalls managed by the Hardware Security Manager (HSM) enable developers to implement stringent security-minded system design requirements. Cryptographic acceleration and secure boot are also available on AM263Px devices.

TI provides a complete set of microcontroller software and development tools for the AM263Px family of microcontrollers.

Package Information

PART NUMBER(1) (2)	PACKAGE	PACKAGE SIZE(3)
AM263P4...ZCZ	ZCZ (nFBGA, 324)	15.0mm × 15.0mm
AM263P2...ZCZ	ZCZ (nFBGA, 324)	15.0mm × 15.0mm
AM263P1...ZCZ	ZCZ (nFBGA, 324)	15.0mm × 15.0mm
AM263P4...ZCZQ1	ZCZQ1 (nFBGA, 324)	15.0mm × 15.0mm
AM263P2...ZCZQ1	ZCZQ1 (nFBGA, 324)	15.0mm × 15.0mm
AM263P1...ZCZQ1	ZCZQ1 (nFBGA, 324)	15.0mm × 15.0mm

(1) For more information, see Section 11.
(2) All devices are available in both tray or tape and reel packaging.
(3) The package size (length x width) is a nominal value and includes pins, where applicable.

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3.1 Functional Block Diagram

Figure 3-1 is the functional block diagram for the device.

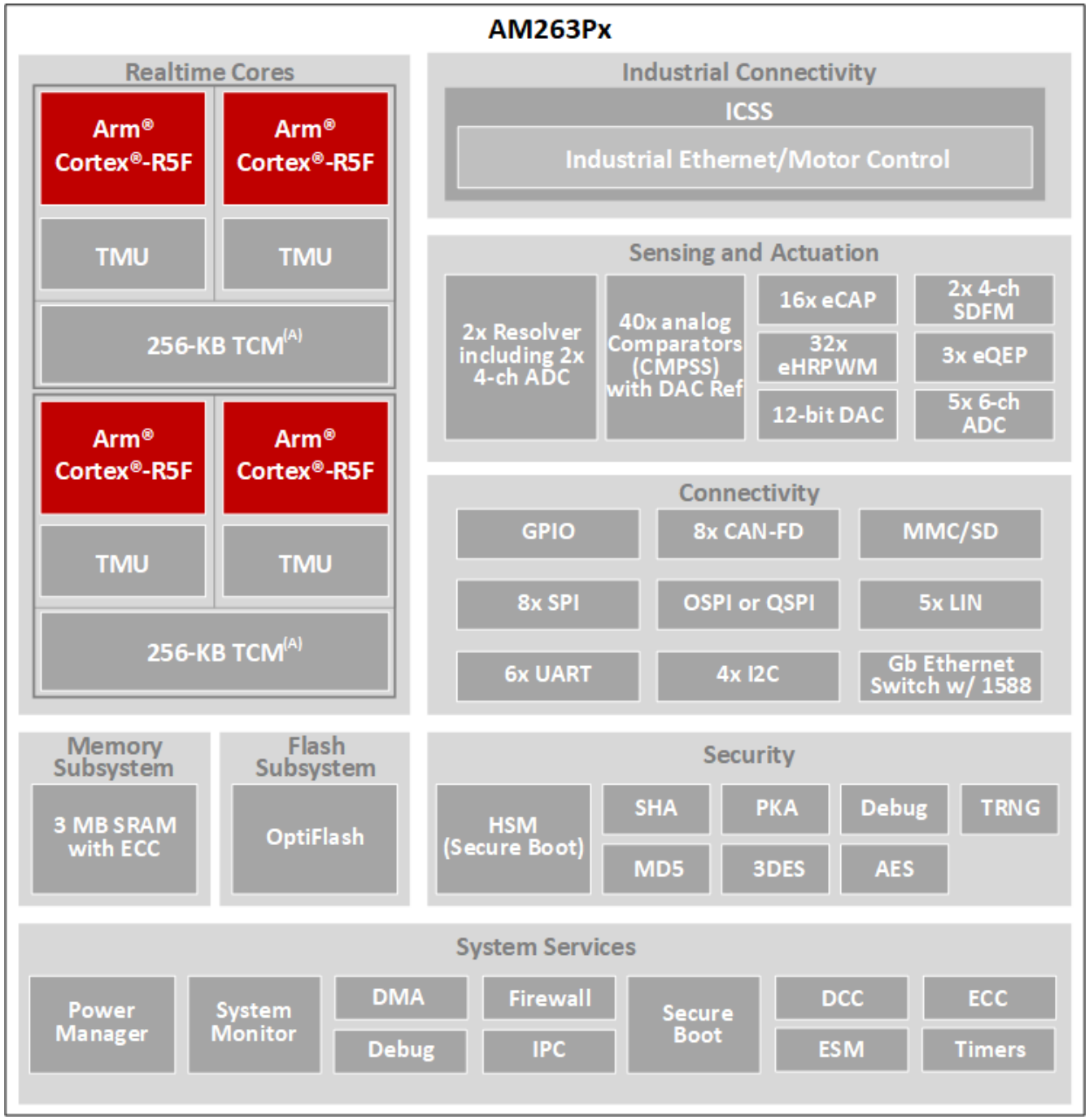

Figure 3-1. Functional Block Diagram

A. All 256KB TCM is available for R5FSSn_0 while operating in Single-Core or Lockstep Modes.

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4 Device Comparison

Table 4-1 shows a comparison between devices, highlighting the differences.

Table 4-1. Device Comparison

FEATURES	REFERENCE NAME	AM263P4	AM263P2	AM263P1
JTAG DEVICE ID COMPARISON (FEATURES)				
JTAG Device ID(1)	Industrial:	M: 0x6111BBE9 L: 0x61119BE9 K: 0x61117BE9 E: 0x6110B3E9 D: 0x611093E9	M: 0x6109B3E9 L: 0x6109B3E9 K: 0x61097BE9 E: 0x6108BBA9 D: 0x61089BA9	- - - E: 0x6104B3A9 -
	Extended Automotive:(13)	K: 0x61117BF9 (ZCZ_C) K: 0x61117BFD (ZCZ_S) K: 0x61117BFA (ZCZ_F) D: 0x611093F9 (ZCZ_C, G = O) D: 0x61109439 (ZCZ_C, G = P) D: 0x61109BFD (ZCZ_S, G = O) D: 0x61109C3D (ZCZ_S, G = P)	K: 0x61097BF9 (ZCZ_C) K: 0x610973FD (ZCZ_S) - D: 0x61089BF9 (ZCZ_C, G = O) D: 0x61089C39 (ZCZ_C, G = P) D: 0x610893FD (ZCZ_S, G = O) D: 0x61089C3D (ZCZ_S, G = P)	- - - D: 0x610493B9 - - -
PROCESSORS AND ACCELERATORS				
Speed Grade		See Section 6.6, *Operating Performance Points*		
Arm® Cortex-R5F	R5FSS	4	2	1
Trigonometric Math Unit	TMU	Yes		
Hardware Security Module	HSM	Yes		
Crypto Accelerators	Security	Yes		
PROGRAM AND DATA STORAGE				
On-Chip Shared Memory (RAM)	OCSRAM	See Section 6.6, *Operating Performance Points*		
R5F Tightly Coupled Memory (TCM)	TCM	Up to 512KB(10)		
PERIPHERALS				
Modular Controller Area Network Interface	MCAN	8		
Full CAN-FD Support	MCAN	8		
General-Purpose I/O	GPIO	Up to 139		
Serial Peripheral Interface	SPI	8		
Universal Asynchronous Receiver and Transmitter	UART	6		
Local Interconnect Network	LIN	5		
Inter-Integrated Circuit Interface	I2C	4		
Analog-to-Digital Converter	ADC	3(2) or 5(3)	3(2) or 5(3)	3
Resolver (ADC12B3M)(4)	RDC	0(8) or 2(9)	0(8) or 2(9)	0
	ADC	0(8) or 2(9)	0(8) or 2(9)	0
Comparator Modules	CMPSS	12(2) or 20(3)	12(2) or 20(3)	12
Digital-to-Analog Converter	DAC	1		
Programmable Real-Time Unit Subsystem(5)	PRU-ICSS	0 or 1		
Industrial Communication Subsystem Support(6)	PRU-ICSS	Optional		
Gigabit Ethernet Interface	CPSW	Yes (2(8) or 1(9))		
Multi-Media Card/Secure Digital Interface	MMCSD	1		
Enhanced High-Resolution Pulse-Width Modulator Module	EHRPWM	16(2) or 32(3)	16(2) or 32(3)	16
Enhanced Capture Module	ECAP	8(2) or 16(3)	8(2) or 16(3)	8
Enhanced Quadrature Encoder Pulse Module	EQEP	2(2) or 3(3)	2(2) or 3(3)	2
Sigma Delta Filter Module	SDFM	1(2) or 2(3)	1(2) or 2(3)	1
Fast Serial Interface	FSI	4x FSI_RX + 4x FSI_TX		
Octal SPI Flash Interface	OSPI	1 or 0(11)		
Miscellaneous				
Junction Temperature		Industrial: –40°C to 105°C		
		Extended Automotive: –40°C to 150°C(12)		
Automotive Qualification		AEC-Q100(7) Option		

(1) "X:" letter refers to feature parameter and (Grade "X") refers to Grade in the Section 6.6, *Operating Performance Points* table.
(2) Standard Analog configuration contains 3x ADC, 16x EHRPWM, 8x eCAP, 2x EQEP, 1x SDFM, 12x CMPSS
(3) Enhanced Analog configuration contains 5x ADC, 32x EHRPWM, 16x eCAP, 3x EQEP, 2x SDFM, 20x CMPSS
(4) The 2x Resolver ADC12B3M modules can be used as either Resolver ADCs or general-purpose ADCs

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(5) Programmable Real-Time Unit Subsystem is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, M, or N. Refer to the Nomenclature Description table for definition of feature codes.
(6) Industrial Communication Subsystem Support is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, M, or N. Refer to the Nomenclature Description table for definition of feature codes.
(7) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Nomenclature Description table.
(8) Applies to devices in the ZCZ-C Package only and have a Special Features code of C. Refer to the Nomenclature Description table for definition of Special Features codes.
(9) Applies to devices in the ZCZ-S Package only and have a Special Features code of F or S. Refer to the Nomenclature Description table for definition of Special Features codes.
(10) Each R5FSS cluster supports 256KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 256KB of TCM memory, while in Dual-Core mode, each core may only utilize its designated half (128KB TCM).
(11) The SIP Flash-in-Package variant connects the OSPI interface to an OSPI Flash device included in the package, disabling the external OSPI interface for application use.
(12) The SIP Flash-in-Package variant is limited by the OSPI Flash device in the package to 125°C.
(13) "G =" refers to the values listed in Section 6.6, *Operating Performance Points*.

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4.1 Related Products

Sitara™ Microcontrollers Family of Arm® Cortex®-R based high performance microcontrollers with advanced networking, real-time control, and signal processing accelerators to meet emerging MCU requirements for industrial and automotive applications.

Sitara™ Processors Family of broad, scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity and unified software support – an excellent choice for sensors to servers. Sitara™ processors have the features and reliability necessary for the latest industrial and automotive application-level requirements.

Sitara™ Microcontrollers - Evaluation Modules TI provides device-specific Evaluation Module (EVM) designs to help kick-start product development. See the **AM263Px ControlCard** for more information.

MCU-PLUS-SDK-AM263PX The AM263Px microcontroller (MCU) plus software development kit (SDK) is a unified software platform for embedded processors providing easy setup and fast out-of-the-box access to examples, benchmarks and demonstrations.

Products to complete your design The following list of products are frequently purchased or used in conjunction with the AM263Px device to meet your system design requirements.

- **TPS653860-Q1** - Functional safety-compliant multi-rail power supply for safety MCUs for Q100 grade-0 applications.
- **TPS3704-Q1** - Automotive multichannel window supervisor with very-high accuracy and compact form factor.
- **DP83TG720S-Q1** - 1000BASE-T1 automotive Ethernet PHY with RGMII.
- **DP83826E** - Low latency 10/100Mbps Ethernet PHY with MII interface and enhanced mode.
- **TCAN1042H-Q1** - Automotive 70V bus-fault-protected CAN transceiver with flexible data-rate.

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5 Terminal Configuration and Functions

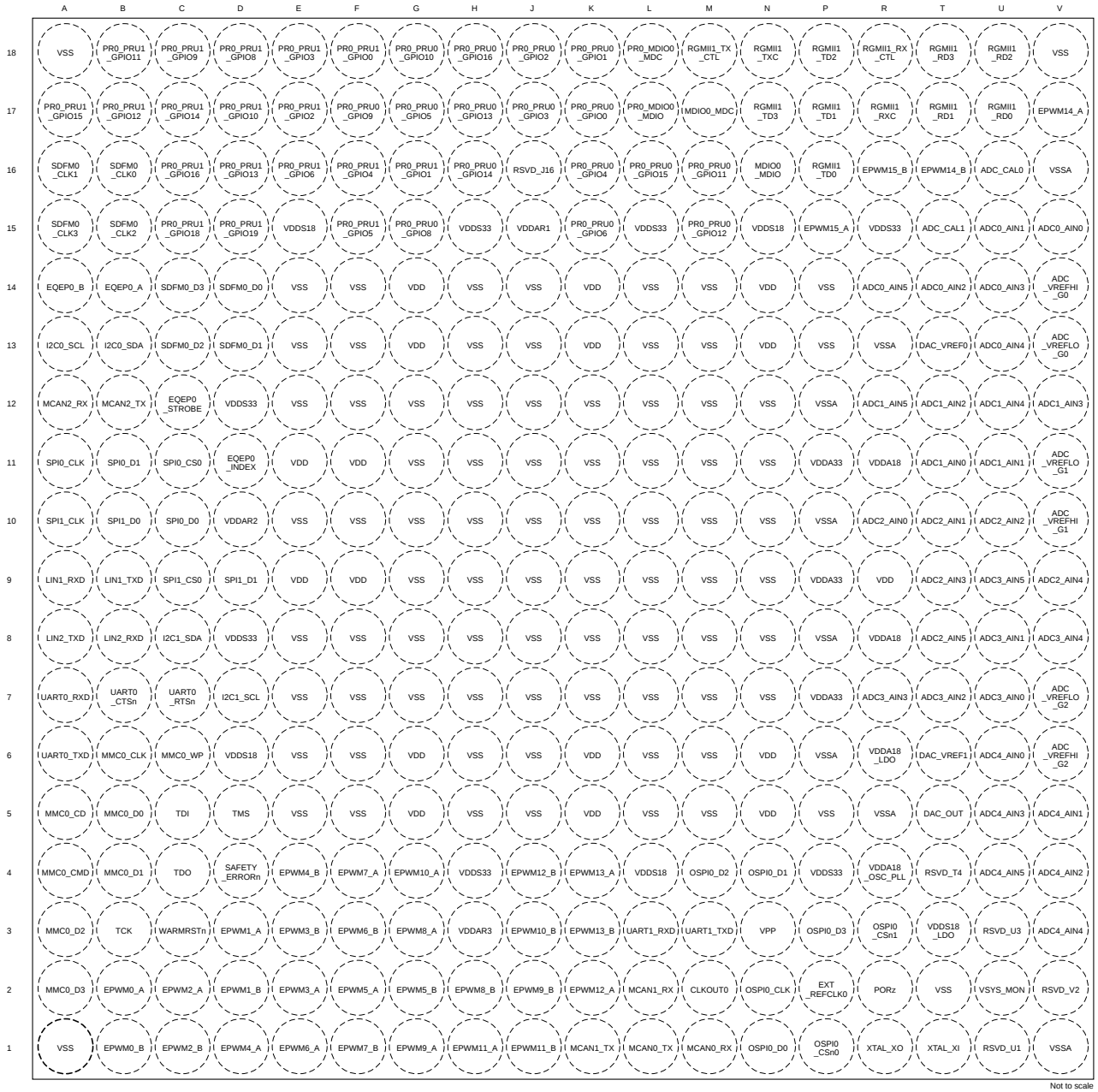
5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers.

5.1.1 ZCZ_C Pin Diagram



Not to scale

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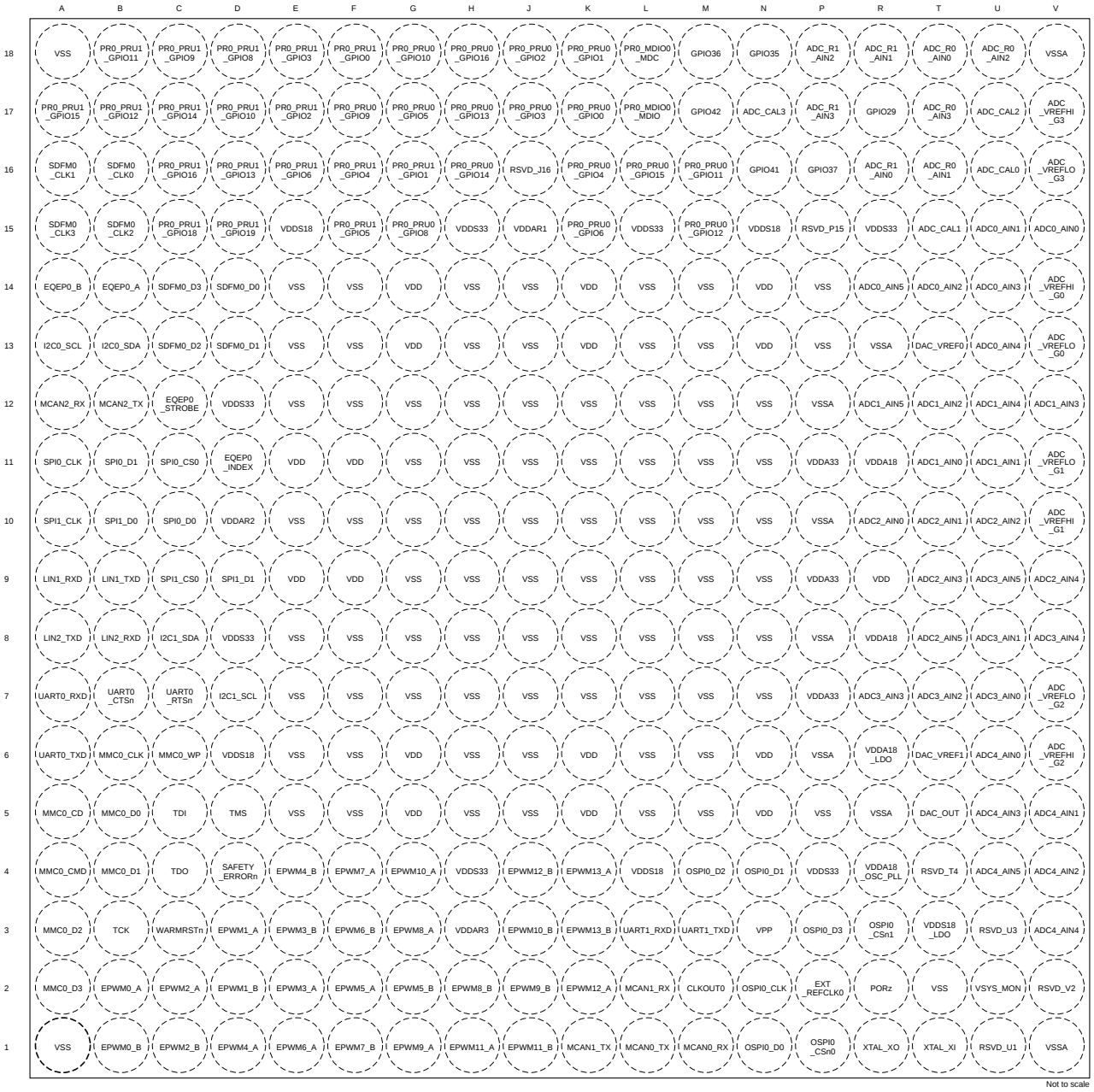
5.1.2 ZCZ_S Pin Diagram



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V
18	VSS	PR0_PRU1_GPIO11	PR0_PRU1_GPIO9	PR0_PRU1_GPIO8	PR0_PRU1_GPIO3	PR0_PRU1_GPIO0	PR0_PRU0_GPIO10	PR0_PRU0_GPIO16	PR0_PRU0_GPIO2	PR0_PRU0_GPIO1	PR0_MDIO0_MDC	GPIO36	GPIO35	ADC_R1_AIN2	ADC_R1_AIN1	ADC_R0_AIN0	ADC_R0_AIN2	VSSA
17	PR0_PRU1_GPIO15	PR0_PRU1_GPIO12	PR0_PRU1_GPIO14	PR0_PRU1_GPIO10	PR0_PRU1_GPIO2	PR0_PRU0_GPIO9	PR0_PRU0_GPIO5	PR0_PRU0_GPIO13	PR0_PRU0_GPIO3	PR0_PRU0_GPIO0	PR0_MDIO0_MDIO	GPIO42	ADC_CAL3	ADC_R1_AIN3	GPIO29	ADC_R0_AIN3	ADC_CAL2	ADC_VREFHI_G3
16	SDFM0_CLK1	SDFM0_CLK0	PR0_PRU1_GPIO16	PR0_PRU1_GPIO13	PR0_PRU1_GPIO6	PR0_PRU1_GPIO4	PR0_PRU1_GPIO1	PR0_PRU0_GPIO14	RSVD_J16	PR0_PRU0_GPIO4	PR0_PRU0_GPIO15	PR0_PRU0_GPIO11	GPIO41	GPIO37	ADC_R1_AIN0	ADC_R0_AIN1	ADC_CAL0	ADC_VREFLO_G3
15	SDFM0_CLK3	SDFM0_CLK2	PR0_PRU1_GPIO18	PR0_PRU1_GPIO19	VDDS18	PR0_PRU1_GPIO5	PR0_PRU0_GPIO8	VDDS33	VDDAR1	PR0_PRU0_GPIO6	VDDS33	PR0_PRU0_GPIO12	VDDS18	RSVD_P15	VDDS33	ADC_CAL1	ADC0_AIN1	ADC0_AIN0
14	EQEP0_B	EQEP0_A	SDFM0_D3	SDFM0_D0	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VSS	VDD	VSS	ADC0_AIN5	ADC0_AIN2	ADC0_AIN3	ADC_VREFHI_G0
13	I2C0_SCL	I2C0_SDA	SDFM0_D2	SDFM0_D1	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VSSA	DAC_VREF0	ADC0_AIN4	ADC_VREFLO_G0
12	MCAN2_RX	MCAN2_TX	EQEP0_STROBE	VDDS33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSSA	ADC1_AIN5	ADC1_AIN2	ADC1_AIN4	ADC1_AIN3
11	SPI0_CLK	SPI0_D1	SPI0_CS0	EQEP0_INDEX	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDA33	VDDA18	ADC1_AIN0	ADC1_AIN1	ADC_VREFLO_G1
10	SPI1_CLK	SPI1_D0	SPI0_D0	VDDAR2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSSA	ADC2_AIN0	ADC2_AIN1	ADC2_AIN2	ADC_VREFHI_G1
9	LIN1_RXD	LIN1_TXD	SPI1_CS0	SPI1_D1	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDA33	VDD	ADC2_AIN3	ADC3_AIN5	ADC2_AIN4
8	LIN2_TXD	LIN2_RXD	I2C1_SDA	VDDS33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSSA	VDDA18	ADC2_AIN5	ADC3_AIN1	ADC3_AIN4
7	UART0_RXD	UART0_CTSn	UART0_RTSn	I2C1_SCL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDA33	ADC3_AIN3	ADC3_AIN2	ADC3_AIN0	ADC_VREFLO_G2
6	UART0_TXD	MMC0_CLK	MMC0_WP	VDDS18	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VSS	VDD	VSSA	VDDA18_LDO	DAC_VREF1	ADC4_AIN0	ADC_VREFHI_G2
5	MMC0_CD	MMC0_D0	TDI	TMS	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VSSA	DAC_OUT	ADC4_AIN3	ADC4_AIN1
4	MMC0_CMD	MMC0_D1	TDO	SAFETY_ERRORn	EPWM4_B	EPWM7_A	EPWM10_A	VDDS33	EPWM12_B	EPWM13_A	VDDS18	OSPI0_D2	OSPI0_D1	VDDS33	VDDA18_OSC_PLL	RSVD_T4	ADC4_AIN5	ADC4_AIN2
3	MMC0_D2	TCK	WARMRSTn	EPWM1_A	EPWM3_B	EPWM6_B	EPWM8_A	VDDAR3	EPWM10_B	EPWM13_B	UART1_RXD	UART1_TXD	VPP	OSPI0_D3	OSPI0_CSn1	VDDS18_LDO	RSVD_U3	ADC4_AIN4
2	MMC0_D3	EPWM0_A	EPWM2_A	EPWM1_B	EPWM3_A	EPWM5_A	EPWM5_B	EPWM8_B	EPWM9_B	EPWM12_A	MCAN1_RX	CLKOUT0	OSPI0_CLK	EXT_REFCLK0	PORz	VSS	VSYS_MON	RSVD_V2
1	VSS	EPWM0_B	EPWM2_B	EPWM4_A	EPWM6_A	EPWM7_B	EPWM9_A	EPWM11_A	EPWM11_B	MCAN1_TX	MCAN0_TX	MCAN0_RX	OSPI0_D0	OSPI0_CSn0	XTAL_XO	XTAL_XI	RSVD_U1	VSSA

Not to scale

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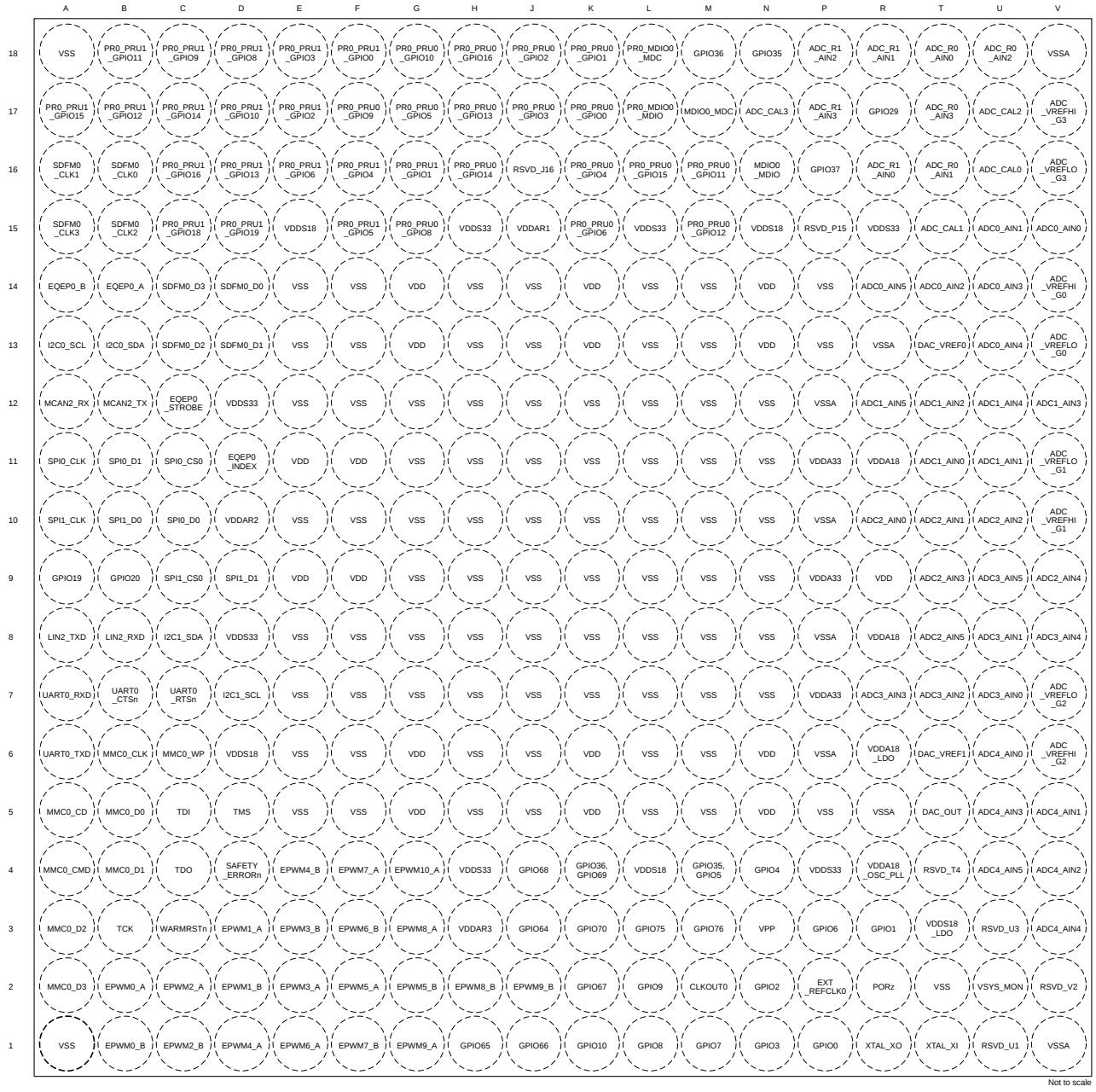
5.1.3 ZCZ_F Pin Diagram



Not to scale

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5.2 Pin Attributes

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
   - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
   - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
   - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   - An empty box or "-" means Not Applicable.

Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Type:** Signal type and direction:
   - I = Input
   - O = Output
   - ID = Input, with open-drain output function
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
6. **Ball State During Reset (RX/TX/PULL):** State of the terminal while PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)

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  - Off: The input buffer is **disabled**.
  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - Low: The output buffer is **enabled** and drives V_{OL}.
- PULL (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up** resistor is turned on.
  - Down: Internal **pull-down** resistor is turned on.
  - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

7. **Ball State After Reset (RX/TX/PULL):** State of the terminal after PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.
     - On: The input buffer is **enabled**.
   - TX (Output buffer)
     - Off: The output buffer is **disabled**.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned **off.**
     - Up: Internal **pull-up resistor** is turned on.
     - Down: Internal **pull-down resistor** is turned on.
     - NA: No internal pull resistor.
   - An empty box, NA, or "-" means Not Applicable.
8. **Mux Mode After Reset:** The value found in this column defines the **default** pin multiplexed signal function after PORz is deasserted.
   - An empty box, NA, or "-" means Not Applicable.
9. **I/O Voltage**: This column describes I/O **operating voltage** options of the respective power supply, when applicable.
   - An empty box, NA, or "-" means Not Applicable.

   For more information, see valid operating voltage range defined for each power supply in *Recommended Operating Conditions*.
10. **Power:** The power supply of the associated I/O, when applicable.
    - An empty box, NA, or "-" means Not Applicable.
11. **Hys:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: Hysteresis Support
    - No: **No** Hysteresis Support
    - An empty box, NA, or "-" means Not Applicable.

    For more information, see the hysteresis values in *Electrical Characteristics*.
12. **Pull Type:** Indicates the presence of an internal pull-up or pull-down resistor. Internal resistors can be enabled or disabled via software.
    - PU: Internal pull-up Only
    - PD: Internal pull-down Only
    - PU/PD: Internal pull-up and pull-down
    - An empty box, NA, or "-" means No internal pull.

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Note

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

13. **Buffer Type:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.
    - An empty box, NA, or "-" means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.
14. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
15. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
16. **Pad Configuration Register Default Value**: This is the default value of the register device pad/pin configuration register after PORz is deasserted.

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
V15	V15	V15	ADC0_AIN0	ADC0_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
U15	U15	U15	ADC0_AIN1	ADC0_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
T14	T14	T14	ADC0_AIN2	ADC0_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	
U14	U14	U14	ADC0_AIN3	ADC0_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
U13	U13	U13	ADC0_AIN4	ADC0_AIN4		I				3.3V	VDDA_CIO		AnalogCIO	
R14	R14	R14	ADC0_AIN5	ADC0_AIN5		I				3.3V	VDDA_CIO		AnalogCIO	
T11	T11	T11	ADC1_AIN0	ADC1_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
U11	U11	U11	ADC1_AIN1	ADC1_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
T12	T12	T12	ADC1_AIN2	ADC1_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	
V12	V12	V12	ADC1_AIN3	ADC1_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
U12	U12	U12	ADC1_AIN4	ADC1_AIN4		I				3.3V	VDDA_CIO		AnalogCIO	
R12	R12	R12	ADC1_AIN5	ADC1_AIN5		I				3.3V	VDDA_CIO		AnalogCIO	
R10	R10	R10	ADC2_AIN0	ADC2_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
T10	T10	T10	ADC2_AIN1	ADC2_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
U10	U10	U10	ADC2_AIN2	ADC2_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	
T9	T9	T9	ADC2_AIN3	ADC2_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
V9	V9	V9	ADC2_AIN4	ADC2_AIN4		I				3.3V	VDDA_CIO		AnalogCIO	
T8	T8	T8	ADC2_AIN5	ADC2_AIN5		I				3.3V	VDDA_CIO		AnalogCIO	
U7	U7	U7	ADC3_AIN0	ADC3_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
U8	U8	U8	ADC3_AIN1	ADC3_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
T7	T7	T7	ADC3_AIN2	ADC3_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	
R7	R7	R7	ADC3_AIN3	ADC3_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
V8	V8	V8	ADC3_AIN4	ADC3_AIN4		I				3.3V	VDDA_CIO		AnalogCIO	
U9	U9	U9	ADC3_AIN5	ADC3_AIN5		I				3.3V	VDDA_CIO		AnalogCIO	
U6	U6	U6	ADC4_AIN0	ADC4_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
V5	V5	V5	ADC4_AIN1	ADC4_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
V4	V4	V4	ADC4_AIN2	ADC4_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	
U5	U5	U5	ADC4_AIN3	ADC4_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
V3	V3	V3	ADC4_AIN4	ADC4_AIN4		I				3.3V	VDDA_CIO		AnalogCIO	
U4	U4	U4	ADC4_AIN5	ADC4_AIN5		I				3.3V	VDDA_CIO		AnalogCIO	
U16	U16	U16	ADC_CAL0	ADC_CAL0		I				3.3V	VDDA_CIO		AnalogCIO	
T15	T15	T15	ADC_CAL1	ADC_CAL1		I				3.3V	VDDA_CIO		AnalogCIO	
	U17	U17	ADC_CAL2	ADC_CAL2		A				3.3V	VDDA_CIO		AnalogCIO	
	N17	N17	ADC_CAL3	ADC_CAL3		A				3.3V	VDDA_CIO		AnalogCIO	
	T18	T18	ADC_R0_AIN0	ADC_R0_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
	T16	T16	ADC_R0_AIN1	ADC_R0_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
	U18	U18	ADC_R0_AIN2	ADC_R0_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
	T17	T17	ADC_R0_AIN3	ADC_R0_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
	R16	R16	ADC_R1_AIN0	ADC_R1_AIN0		I				3.3V	VDDA_CIO		AnalogCIO	
	R18	R18	ADC_R1_AIN1	ADC_R1_AIN1		I				3.3V	VDDA_CIO		AnalogCIO	
	P18	P18	ADC_R1_AIN2	ADC_R1_AIN2		I				3.3V	VDDA_CIO		AnalogCIO	
	P17	P17	ADC_R1_AIN3	ADC_R1_AIN3		I				3.3V	VDDA_CIO		AnalogCIO	
V14	V14	V14	ADC_VREFHI_G0	ADC_VREFHI_G0		A				3.3V	VDDA_CIO		AnalogCIO	
V10	V10	V10	ADC_VREFHI_G1	ADC_VREFHI_G1		A				3.3V	VDDA_CIO		AnalogCIO	
V6	V6	V6	ADC_VREFHI_G2	ADC_VREFHI_G2		A				3.3V	VDDA_CIO		AnalogCIO	
	V17	V17	ADC_VREFHI_G3	ADC_VREFHI_G3		A				3.3V	VDDA_CIO		AnalogCIO	
V13	V13	V13	ADC_VREFLO_G0	ADC_VREFLO_G0		A				3.3V	VDDA_CIO		AnalogCIO	
V11	V11	V11	ADC_VREFLO_G1	ADC_VREFLO_G1		A				3.3V	VDDA_CIO		AnalogCIO	
V7	V7	V7	ADC_VREFLO_G2	ADC_VREFLO_G2		A				3.3V	VDDA_CIO		AnalogCIO	
	V16	V16	ADC_VREFLO_G3	ADC_VREFLO_G3		A				3.3V	VDDA_CIO		AnalogCIO	
M2	M2	M2	CLKOUT0	CLKOUT0	0	O	Off / Off / Off	Off / SS / Off	0	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
			CLKOUT0_CFG_REG 0x5310 0228 0x0000 0570	GPIO138	7	IO								
T5	T5	T5	DAC_OUT	DAC_OUT		O				3.3V	VDDA_CIO		AnalogCIO	
T13	T13	T13	DAC_VREF0	DAC_VREF0		A				3.3V	VDDA_CIO		AnalogCIO	
T6	T6	T6	DAC_VREF1	DAC_VREF1		A				3.3V	VDDA_CIO		AnalogCIO	
B2	B2	B2	EPWM0_A	EPWM0_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
			EPWM0_A_CFG_REG 0x5310 00AC 0x0000 05F7	GPIO43	7	IO								
				EPWM0_A	10	O								
B1	B1	B1	EPWM0_B	EPWM0_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
			EPWM0_B_CFG_REG 0x5310 00B0 0x0000 05F7	GPIO44	7	IO								
				EPWM0_B	10	O								
D3	D3	D3	EPWM1_A	EPWM1_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
			EPWM1_A_CFG_REG 0x5310 00B4 0x0000 05F7	GPIO45	7	IO								
				EPWM1_A	10	O								
D2	D2	D2	EPWM1_B	EPWM1_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
			EPWM1_B_CFG_REG 0x5310 00B8 0x0000 05F7	GPIO46	7	IO								
				EPWM4_B	10	O								
C2	C2	C2	EPWM2_A	EPWM2_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
			EPWM2_A_CFG_REG 0x5310 00BC 0x0000 05F7	GPIO47	7	IO								
				EPWM2_A	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
C1	C1	C1	EPWM2_B EPWM2_B_CFG_REG 0x5310 00C0 0x0000 05F7	EPWM2_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO48	7	IO								
				EPWM2_B	10	O								
E2	E2	E2	EPWM3_A EPWM3_A_CFG_REG 0x5310 00C4 0x0000 05F7	EPWM3_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO49	7	IO								
				EPWM3_A	10	O								
E3	E3	E3	EPWM3_B EPWM3_B_CFG_REG 0x5310 00C8 0x0000 05F7	EPWM3_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO50	7	IO								
				EPWM6_A	10	O								
D1	D1	D1	EPWM4_A EPWM4_A_CFG_REG 0x5310 00CC 0x0000 05F7	EPWM4_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO51	7	IO								
				EPWM4_A	10	O								
E4	E4	E4	EPWM4_B EPWM4_B_CFG_REG 0x5310 00D0 0x0000 05F7	EPWM4_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				FSITX1_CLK	6	O								
				GPIO52	7	IO								
				EPWM1_B	10	O								
F2	F2	F2	EPWM5_A EPWM5_A_CFG_REG 0x5310 00D4 0x0000 05F7	EPWM5_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_CS0	3	IO								
				FSITX1_DATA0	6	O								
				GPIO53	7	IO								
				EPWM5_A	10	O								
G2	G2	G2	EPWM5_B EPWM5_B_CFG_REG 0x5310 00D8 0x0000 05F7	EPWM5_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_CLK	3	IO								
				FSITX1_DATA1	6	O								
				GPIO54	7	IO								
				EPWM8_B	10	O								
E1	E1	E1	EPWM6_A EPWM6_A_CFG_REG 0x5310 00DC 0x0000 05F7	EPWM6_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_D0	3	IO								
				FSIRX1_CLK	6	I								
				GPIO55	7	IO								
				EPWM3_B	10	O								
F3	F3	F3	EPWM6_B EPWM6_B_CFG_REG 0x5310 00E0 0x0000 05F7	EPWM6_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_D1	3	IO								
				FSIRX1_DATA0	6	I								
				GPIO56	7	IO								
				EPWM6_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
F4	F4	F4	EPWM7_A EPWM7_A_CFG_REG 0x5310 00E4 0x0000 05F7	EPWM7_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI6_CS0	3	IO								
				FSIRX1_DATA1	6	I								
				GPIO57	7	IO								
				EPWM7_A	10	O								
F1	F1	F1	EPWM7_B EPWM7_B_CFG_REG 0x5310 00E8 0x0000 05F7	EPWM7_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI6_CLK	3	IO								
				GPIO58	7	IO								
				EPWM5_B	10	O								
G3	G3	G3	EPWM8_A EPWM8_A_CFG_REG 0x5310 00EC 0x0000 05F7	EPWM8_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART4_TXD	1	O								
				I2C3_SDA	2	IO								
				SPI6_D0	3	IO								
				FSITX2_CLK	6	O								
				GPIO59	7	IO								
				EPWM8_A	10	O								
H2	H2	H2	EPWM8_B EPWM8_B_CFG_REG 0x5310 00F0 0x0000 05F7	EPWM8_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART4_RXD	1	I								
				I2C3_SCL	2	IO								
				SPI6_D1	3	IO								
				FSITX2_DATA0	6	O								
				GPIO60	7	IO								
				EPWM9_B	10	O								
G1	G1	G1	EPWM9_A EPWM9_A_CFG_REG 0x5310 00F4 0x0000 05F7	EPWM9_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI7_CS0	3	IO								
				MCAN4_RX	4	I								
				FSITX2_DATA1	6	O								
				GPIO61	7	IO								
				EPWM9_A	10	O								
J2	J2	J2	EPWM9_B EPWM9_B_CFG_REG 0x5310 00F8 0x0000 05F7	EPWM9_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_RTSn	1	O								
				SPI7_CLK	3	IO								
				MCAN4_TX	4	O								
				FSIRX2_CLK	6	I								
				GPIO62	7	IO								
				EPWM11_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
G4	G4	G4	EPWM10_A EPWM10_A_CFG_REG 0x5310 00FC 0x0000 05F7	EPWM10_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_CTSn	1	I								
				SPI7_D0	3	IO								
				MCAN5_RX	4	I								
				FSIRX2_DATA0	6	I								
				GPIO63	7	IO								
				EPWM7_B	10	O								
J3	J3		EPWM10_B EPWM10_B_CFG_REG 0x5310 0100 0x0000 05F7	EPWM10_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_RTSn	1	O								
				SPI7_D1	3	IO								
				MCAN5_TX	4	O								
				OSPI0_RESET_OUT0	5	O								
				FSIRX2_DATA1	6	I								
				GPIO64	7	IO								
				EPWM10_B	10	O								
H1	H1		EPWM11_A EPWM11_A_CFG_REG 0x5310 0104 0x0000 05F7	EPWM11_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_CTSn	1	I								
				OSPI0_ECC_FAIL	2	I								
				MCAN6_RX	4	I								
				OSPI0_RESET_OUT1	5	O								
				OSPI0_CSn0	6	O								
				GPIO65	7	IO								
				EPWM11_A	10	O								
J1	J1		EPWM11_B EPWM11_B_CFG_REG 0x5310 0108 0x0000 05F7	EPWM11_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_RTSn	1	O								
				OSPI0_RESET_OUT0	2	O								
				MCAN6_TX	4	O								
				OSPI0_D1	6	IO								
				GPIO66	7	IO								
				EPWM12_B	10	O								
K2	K2		EPWM12_A EPWM12_A_CFG_REG 0x5310 010C 0x0000 05F7	EPWM12_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_CTSn	1	I								
				SPI4_CS1	2	IO								
				MCAN7_RX	4	I								
				OSPI0_D5	6	IO								
				GPIO67	7	IO								
				EPWM12_A	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
J4	J4		EPWM12_B EPWM12_B_CFG_REG 0x5310 0110 0x0000 05F7	EPWM12_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_DCDn	1	I								
				SPI7_CS0	2	IO								
				MCAN7_TX	4	O								
				OSPI0_D7	6	IO								
				GPIO68	7	IO								
				EPWM10_A	10	O								
K4	K4		EPWM13_A EPWM13_A_CFG_REG 0x5310 0114 0x0000 05F7	EPWM13_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_RIn	1	I								
				SPI7_CLK	2	IO								
				OSPI0_D3	6	IO								
				GPIO69	7	IO								
				EPWM13_A	10	O								
K3	K3		EPWM13_B EPWM13_B_CFG_REG 0x5310 0118 0x0000 05F7	EPWM13_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_DTRn	1	O								
				SPI7_D0	2	IO								
				OSPI0_ECC_FAIL	6	I								
				GPIO70	7	IO								
				EPWM13_B	10	O								
V17			EPWM14_A EPWM14_A_CFG_REG 0x5310 011C 0x0000 05F7	EPWM14_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_DSRn	1	I								
				SPI7_D1	2	IO								
				MCAN6_RX	3	I								
				GPIO71	7	IO								
				EPWM14_A	10	O								
T16			EPWM14_B EPWM14_B_CFG_REG 0x5310 0120 0x0000 05F7	EPWM14_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MII1_RX_ER	2	I								
				MCAN6_TX	3	O								
				GPIO72	7	IO								
				EPWM14_B	10	O								
P15			EPWM15_A EPWM15_A_CFG_REG 0x5310 0124 0x0000 05F7	EPWM15_A	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART5_TXD	1	O								
				MII1_COL	2	I								
				MCAN7_RX	3	I								
				GPIO73	7	IO								
				ADC_EXTCH_XBAROUT4	9	O								
				EPWM15_A	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
R16			EPWM15_B EPWM15_B_CFG_REG 0x5310 0128 0x0000 05F7	EPWM15_B	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART5_RXD	1	I								
				MII1_CRS	2	I								
				MCAN7_TX	3	O								
				GPIO74	7	IO								
				ADC_EXTCH_XBAROUT5	9	O								
				EPWM15_B	10	O								
B14	B14	B14	EQEP0_A EQEP0_A_CFG_REG 0x5310 0208 0x0000 05F7	UART4_RTSn	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_CLK	3	IO								
				GPIO130	7	IO								
				EQEP0_A	8	I								
				SDFM1_CLK0	9	I								
A14	A14	A14	EQEP0_B EQEP0_B_CFG_REG 0x5310 020C 0x0000 05F7	UART4_CTSn	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_CS0	3	IO								
				GPIO131	7	IO								
				EQEP0_B	8	I								
				SDFM1_D0	9	I								
D11	D11	D11	EQEP0_INDEX EQEP0_INDEX_CFG_REG 0x5310 0214 0x0000 05F7	UART4_RXD	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN4_RXD	1	IO								
				SPI4_D1	3	IO								
				GPIO133	7	IO								
				EQEP0_INDEX	8	IO								
				SDFM1_D1	9	I								
				ADC_EXTCH_XBAROUT3	10	O								
C12	C12	C12	EQEP0_STROBE EQEP0_STROBE_CFG_REG 0x5310 0210 0x0000 05F7	UART4_TXD	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN4_TXD	1	IO								
				SPI4_D0	3	IO								
				GPIO132	7	IO								
				EQEP0_STROBE	8	IO								
				SDFM1_CLK1	9	I								
				ADC_EXTCH_XBAROUT2	10	O								
P2	P2	P2	EXT_REFCLK0 EXT_REFCLK0_CFG_REG 0x5310 01E4 0x0000 05F7	EXT_REFCLK0	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				XBAROUT15	5	O								
				GPIO121	7	IO								
				EQEP1_INDEX	9	IO								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
		P1	GPIO0 OSPI0_CSn0_CFG_REG 0x5310 0000 0x0000 05F7	OSPI0_D0	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO0	7	IO								
		R3	GPIO1 OSPI0_CSn1_CFG_REG 0x5310 0004 0x0000 05F7	MCAN5_TX	2	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_CS1	4	IO								
				XBAROUT0	5	O								
				UART2_RTSn	6	O								
				GPIO1	7	IO								
				FSIRX2_DATA1	8	I								
				EPWM10_B	10	O								
		N2	GPIO2 OSPI0_CLK_CFG_REG 0x5310 0008 0x0000 05F7	MCAN7_RX	2	I	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI7_CS0	4	IO								
				UART3_CTSn	6	I								
				GPIO2	7	IO								
				EPWM12_A	10	O								
		N1	GPIO3 OSPI0_D0_CFG_REG 0x5310 000C 0x0000 05D7	MCAN7_TX	2	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI7_CLK	4	IO								
				UART1_DCDn	6	I								
				GPIO3	7	IO								
				EPWM12_B	10	O								
				SOP0	Bootstrap									
		N4	GPIO4 OSPI0_D1_CFG_REG 0x5310 0010 0x0000 05D7	SPI7_D0	4	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_RIn	6	I								
				GPIO4	7	IO								
				EPWM13_A	10	O								
				SOP1	Bootstrap									
		M4	GPIO5 OSPI0_D2_CFG_REG 0x5310 0014 0x0000 05F7	OSPI0_D6	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO5	7	IO								
		P3	GPIO6 OSPI0_D3_CFG_REG 0x5310 0018 0x0000 05F7	OSPI0_D4	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO6	7	IO								
		M1	GPIO7 MCAN0_RX_CFG_REG 0x5310 001C 0x0000 05F7	OSPI0_DQS	6	I	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO7	7	IO								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
		L1	GPIO8 MCAN0_TX_CFG_REG 0x5310 0020 0x0000 05F7	OSPI0_D2	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO8	7	IO								
		L2	GPIO9 MCAN1_RX_CFG_REG 0x5310 0024 0x0000 05F7	OSPI0_CLK	6	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO9	7	IO								
		K1	GPIO10 MCAN1_TX_CFG_REG 0x5310 0028 0x0000 05F7	MCAN1_TX	0	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_D1	1	IO								
				SPI7_D1	4	IO								
				UART1_DTRn	6	O								
				GPIO10	7	IO								
				EPWM13_B	10	O								
		A9	GPIO19 LIN1_RXD_CFG_REG 0x5310 004C 0x0000 05F7	LIN1_RXD	0	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_RXD	1	I								
				SPI2_CS0	2	IO								
				XBAROUT5	5	O								
				GPIO19	7	IO								
		B9	GPIO20 LIN1_TXD_CFG_REG 0x5310 0050 0x0000 05F7	LIN1_TXD	0	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_TXD	1	O								
				SPI2_CLK	2	IO								
				XBAROUT6	5	O								
				GPIO20	7	IO								
	R17	R17	GPIO29 RGMII1_RXC_CFG_REG 0x5310 0074 0x0000 05F7	RGMII1_RXC	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_REF_CLK	1	IO								
				MII1_RXCLK	2	I								
				FSITX0_CLK	6	O								
				GPIO29	7	IO								
				EQEP2_A	8	I								
				EPWM14_A	10	O								
	N18	M4, N18	GPIO35 RGMII1_TXC_CFG_REG 0x5310 008C 0x0000 05F7	RGMII1_TXC	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MII1_TXCLK	2	I								
				FSITX1_CLK	6	O								
				GPIO35	7	IO								
				EQEP0_INDEX	8	IO								
				EPWM14_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
	M18	K4, M18	GPIO36 RGMII1_TX_CTL_CFG_REG 0x5310 0090 0x0000 05F7	RGMII1_TX_CTL	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_TX_EN	1	O								
				MII1_TX_EN	2	O								
				FSITX1_DATA0	6	O								
				GPIO36	7	IO								
				EQEP0_STROBE	8	IO								
				EPWM15_B	10	O								
	P16	P16	GPIO37 RGMII1_TD0_CFG_REG 0x5310 0094 0x0000 05F7	RGMII1_TD0	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_TXD0	1	O								
				MII1_TXD0	2	O								
				FSITX1_DATA1	6	O								
				GPIO37	7	IO								
				EQEP1_A	8	I								
				EPWM15_A	9	O								
				EPWM15_B	10	O								
		J3	GPIO64 EPWM10_B_CFG_REG 0x5310 0100 0x0000 05F7	OSPI0_RESET_OUT0	5	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO64	7	IO								
		H1	GPIO65 EPWM11_A_CFG_REG 0x5310 0104 0x0000 05F7	OSPI0_CSn0	6	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO65	7	IO								
		J1	GPIO66 EPWM11_B_CFG_REG 0x5310 0108 0x0000 05F7	OSPI0_D1	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO66	7	IO								
		K2	GPIO67 EPWM12_A_CFG_REG 0x5310 010C 0x0000 05F7	OSPI0_D5	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO67	7	IO								
		J4	GPIO68 EPWM12_B_CFG_REG 0x5310 0110 0x0000 05F7	OSPI0_D7	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO68	7	IO								
		K4	GPIO69 EPWM13_A_CFG_REG 0x5310 0114 0x0000 05F7	OSPI0_D3	6	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO69	7	IO								
		K3	GPIO70 EPWM13_B_CFG_REG 0x5310 0118 0x0000 05F7	OSPI0_ECC_FAIL	6	I	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO70	7	IO								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
		L3	GPIO75 UART1_RXD_CFG_REG 0x5310 012C 0x0000 05F7	UART1_RXD	0	I	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN1_RXD	1	IO								
				EPWM16_A	5	O								
				GPIO75	7	IO								
				EPWM16_A	10	O								
				EPWM10_A	11	O								
		M3	GPIO76 UART1_TXD_CFG_REG 0x5310 0130 0x0000 05F7	UART1_TXD	0	O	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN1_TXD	1	IO								
				EPWM16_B	5	O								
				GPIO76	7	IO								
				EPWM16_B	10	O								
A13	A13	A13	I2C0_SCL I2C0_SCL_CFG_REG 0x5310 021C 0x0000 05F7	I2C0_SCL	0	IOD	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	I2C OD	
				GPIO135	7	IOD								
				EQEP2_B	8	ID								
				SDFM1_CLK3	9	ID								
B13	B13	B13	I2C0_SDA I2C0_SDA_CFG_REG 0x5310 0218 0x0000 05F7	I2C0_SDA	0	IOD	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	I2C OD	
				GPIO134	7	IOD								
				EQEP2_A	8	ID								
				SDFM1_CLK2	9	ID								
D7	D7	D7	I2C1_SCL I2C1_SCL_CFG_REG 0x5310 005C 0x0000 05F7	I2C1_SCL	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI3_CS0	2	IO								
				XBAROUT7	5	O								
				GPIO23	7	IO								
C8	C8	C8	I2C1_SDA I2C1_SDA_CFG_REG 0x5310 0060 0x0000 05F7	I2C1_SDA	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI3_CLK	2	IO								
				XBAROUT8	5	O								
				GPIO24	7	IO								
A9	A9		LIN1_RXD LIN1_RXD_CFG_REG 0x5310 004C 0x0000 05F7	LIN1_RXD	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_RXD	1	I								
				SPI2_CS0	2	IO								
				OSPI0_ECC_FAIL	3	I								
				XBAROUT5	5	O								
				GPIO19	7	IO								
				OSPI0_RESET_OUT1	8	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
B9	B9		LIN1_TXD LIN1_TXD_CFG_REG 0x5310 0050 0x0000 05F7	LIN1_TXD	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_TXD	1	O								
				SPI2_CLK	2	IO								
				OSPI0_RESET_OUT0	3	O								
				XBAROUT6	5	O								
				GPIO20	7	IO								
B8	B8	B8	LIN2_RXD LIN2_RXD_CFG_REG 0x5310 0054 0x0000 05F7	LIN2_RXD	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_RXD	1	I								
				SPI2_D0	2	IO								
				GPIO21	7	IO								
A8	A8	A8	LIN2_TXD LIN2_TXD_CFG_REG 0x5310 0058 0x0000 05F7	LIN2_TXD	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_TXD	1	O								
				SPI2_D1	2	IO								
				GPIO22	7	IO								
M1	M1		MCAN0_RX MCAN0_RX_CFG_REG 0x5310 001C 0x0000 05F7	MCAN0_RX	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_CS0	1	IO								
				OSPI0_D4	2	IO								
				OSPI0_DQS	6	I								
				GPIO7	7	IO								
L1	L1		MCAN0_TX MCAN0_TX_CFG_REG 0x5310 0020 0x0000 05F7	MCAN0_TX	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_CLK	1	IO								
				OSPI0_D5	2	IO								
				OSPI0_D2	6	IO								
				GPIO8	7	IO								
L2	L2		MCAN1_RX MCAN1_RX_CFG_REG 0x5310 0024 0x0000 05F7	MCAN1_RX	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_D0	1	IO								
				OSPI0_D6	2	IO								
				OSPI0_CLK	6	O								
				GPIO9	7	IO								
K1	K1		MCAN1_TX MCAN1_TX_CFG_REG 0x5310 0028 0x0000 05F7	MCAN1_TX	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI4_D1	1	IO								
				OSPI0_D7	2	IO								
				SPI7_D1	4	IO								
				UART1_DTRn	6	O								
				GPIO10	7	IO								
				EPWM13_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
A12	A12	A12	MCAN2_RX MCAN2_RX_CFG_REG 0x5310 0224 0x0000 05F7	MCAN2_RX	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_RTSn	1	O								
				GPIO137	7	IO								
				EQEP2_INDEX	8	IO								
				SDFM1_D3	9	I								
B12	B12	B12	MCAN2_TX MCAN2_TX_CFG_REG 0x5310 0220 0x0000 05F7	MCAN2_TX	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART1_RTSn	1	O								
				GPIO136	7	IO								
				EQEP2_STROBE	8	IO								
				SDFM1_D2	9	I								
M17	M17	M17	MDIO0_MDC MDIO0_MDC_CFG_REG 0x5310 00A8 0x0000 05F7	MDIO0_MDC	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO42	7	IO								
N16	N16	N16	MDIO0_MDIO MDIO0_MDIO_CFG_REG 0x5310 00A4 0x0000 05F7	MDIO0_MDIO	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO41	7	IO								
A5	A5	A5	MMC0_CD MMC0_CD_CFG_REG 0x5310 0150 0x0000 05F7	MMC0_CD	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART0_CTSn	1	I								
				I2C2_SDA	2	IO								
				MCAN5_TX	3	O								
				EPWM20_B	5	O								
				GPIO84	7	IO								
				SDFM1_D3	8	I								
				EPWM20_B	10	O								
B6	B6	B6	MMC0_CLK MMC0_CLK_CFG_REG 0x5310 0134 0x0000 05F7	MMC0_CLK	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART0_RXD	1	I								
				LIN0_RXD	2	IO								
				MCAN0_RX	3	I								
				EPWM17_A	5	O								
				GPIO77	7	IO								
				SDFM1_CLK0	8	I								
				EPWM17_A	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
A4	A4	A4	MMC0_CMD MMC0_CMD_CFG_REG 0x5310 0138 0x0000 05F7	MMC0_CMD	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART0_TXD	1	O								
				LIN0_TXD	2	IO								
				MCAN0_TX	3	O								
				EPWM17_B	5	O								
				GPIO78	7	IO								
				SDFM1_D0	8	I								
				EPWM17_B	10	O								
C6	C6	C6	MMC0_WP MMC0_WP_CFG_REG 0x5310 014C 0x0000 05F7	MMC0_WP	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART0_RTSn	1	O								
				I2C2_SCL	2	IO								
				MCAN5_RX	3	I								
				EPWM20_A	5	O								
				GPIO83	7	IO								
				SDFM1_CLK3	8	I								
				EPWM20_A	10	O								
B5	B5	B5	MMC0_D0 MMC0_D0_CFG_REG 0x5310 013C 0x0000 05F7	MMC0_D0	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_RXD	1	I								
				I2C1_SCL	2	IO								
				MCAN1_RX	3	I								
				EPWM18_A	5	O								
				GPIO79	7	IO								
				SDFM1_CLK1	8	I								
				EPWM18_A	10	O								
B4	B4	B4	MMC0_D1 MMC0_D1_CFG_REG 0x5310 0140 0x0000 05F7	MMC0_D1	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN1_TX	3	O								
				EPWM18_B	5	O								
				GPIO80	7	IO								
				SDFM1_D1	8	I								
				EPWM18_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
A3	A3	A3	MMC0_D2 MMC0_D2_CFG_REG 0x5310 0144 0x0000 05F7	MMC0_D2	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART2_TXD	1	O								
				I2C1_SDA	2	IO								
				MCAN4_RX	3	I								
				EPWM19_A	5	O								
				GPIO81	7	IO								
				SDFM1_CLK2	8	I								
				EPWM19_A	10	O								
A2	A2	A2	MMC0_D3 MMC0_D3_CFG_REG 0x5310 0148 0x0000 05F7	MMC0_D3	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_RTSn	1	O								
				MCAN4_TX	3	O								
				EPWM19_B	5	O								
				GPIO82	7	IO								
				SDFM1_D2	8	I								
				EPWM19_B	10	O								
N2	N2		OSPI0_CLK OSPI0_CLK_CFG_REG 0x5310 0008 0x0000 05F7	OSPI0_CLK	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN7_RX	2	I								
				SPI7_CS0	4	IO								
				UART3_CTSn	6	I								
				GPIO2	7	IO								
				EPWM12_A	10	O								
LB	LB	LB	OSPI0_CLKLB OSPI0_CLKLB_CFG_REG 0x5310 0244 0x5F0	OSPI0_CLKLB	0	IO	Off / Off / Off	Off / Off / Off	0	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
P1	P1		OSPI0_CSn0 OSPI0_CSn0_CFG_REG 0x5310 0000 0x0000 05F7	OSPI0_CSn0	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				OSPI0_D0	6	IO								
				GPIO0	7	IO								
R3	R3		OSPI0_CSn1 OSPI0_CSn1_CFG_REG 0x5310 0004 0x0000 05F7	OSPI0_CSn1	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN5_TX	2	O								
				SPI4_CS1	4	IO								
				XBAROUT0	5	O								
				UART2_RTSn	6	O								
				GPIO1	7	IO								
				FSIRX2_DATA1	8	I								
				EPWM10_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
N1	N1		OSPI0_D0 OSPI0_D0_CFG_REG 0x5310 000C 0x0000 05D7	OSPI0_D0	0	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN7_TX	2	O								
				SPI7_CLK	4	IO								
				UART1_DCDn	6	I								
				GPIO3	7	IO								
				EPWM12_B	10	O								
				SOP0	Bootstrap	IO								
N4	N4		OSPI0_D1 OSPI0_D1_CFG_REG 0x5310 0010 0x0000 05D7	OSPI0_D1	0	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI7_D0	4	IO								
				UART1_RIn	6	I								
				GPIO4	7	IO								
				EPWM13_A	10	O								
				SOP1	Bootstrap	IO								
M4	M4		OSPI0_D2 OSPI0_D2_CFG_REG 0x5310 0014 0x0000 05F7	OSPI0_D2	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				OSPI0_D6	6	IO								
				GPIO5	7	IO								
P3	P3		OSPI0_D3 OSPI0_D3_CFG_REG 0x5310 0018 0x0000 05F7	OSPI0_D3	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				OSPI0_D4	6	IO								
				GPIO6	7	IO								
R2	R2	R2	PORz	PORz		I				3.3V	VDDSHV0	Yes	RESET	
L18	L18	L18	PR0_MDIO0_MDC PR0_MDIO0_MDC_CFG_REG 0x5310 0158 0x0000 05F7	PR0_MDIO0_MDC	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				EPWM21_B	5	O								
				GPIO86	7	IO								
				EPWM21_B	10	O								
L17	L17	L17	PR0_MDIO0_MDIO PR0_MDIO0_MDIO_CFG_REG 0x5310 0154 0x0000 05F7	PR0_MDIO0_MDIO	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				EPWM21_A	5	O								
				GPIO85	7	IO								
				EPWM21_A	10	O								
K17	K17	K17	PR0_PRU0_GPIO0 PR0_PRU0_GPIO0_CFG_REG 0x5310 0174 0x0000 05F7	PR0_PRU0_GPIO0	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_RXD0	2	I								
				RGMII2_RD0	3	I								
				MII2_RXD0	4	I								
				EPWM25_A	5	O								
				GPIO93	7	IO								
				EPWM25_A	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
K18	K18	K18	PR0_PRU0_GPIO1 PR0_PRU0_GPIO1_CFG_REG 0x5310 0178 0x0000 05F7	PR0_PRU0_GPIO1	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_RXD1	2	I								
				RGMII2_RD1	3	I								
				MII2_RXD1	4	I								
				EPWM25_B	5	O								
				GPIO94	7	IO								
				EPWM25_B	10	O								
J18	J18	J18	PR0_PRU0_GPIO2 PR0_PRU0_GPIO2_CFG_REG 0x5310 017C 0x0000 05F7	PR0_PRU0_GPIO2	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RGMII2_RD2	3	I								
				MII2_RXD2	4	I								
				EPWM26_A	5	O								
				GPIO95	7	IO								
				EPWM26_A	10	O								
J17	J17	J17	PR0_PRU0_GPIO3 PR0_PRU0_GPIO3_CFG_REG 0x5310 0180 0x0000 05F7	PR0_PRU0_GPIO3	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RGMII2_RD3	3	I								
				MII2_RXD3	4	I								
				EPWM26_B	5	O								
				GPIO96	7	IO								
				EPWM26_B	10	O								
K16	K16	K16	PR0_PRU0_GPIO4 PR0_PRU0_GPIO4_CFG_REG 0x5310 0170 0x0000 05F7	PR0_PRU0_GPIO4	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RGMII2_RX_CTL	3	I								
				MII2_RXDV	4	I								
				EPWM24_B	5	O								
				GPIO92	7	IO								
				EPWM24_B	10	O								
G17	G17	G17	PR0_PRU0_GPIO5 PR0_PRU0_GPIO5_CFG_REG 0x5310 015C 0x0000 05F7	PR0_PRU0_GPIO5	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_RX_ER	2	I								
				MII2_RX_ER	4	I								
				EPWM22_A	5	O								
				GPIO87	7	IO								
				EPWM22_A	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
K15	K15	K15	PR0_PRU0_GPIO6 PR0_PRU0_GPIO6_CFG_REG 0x5310 016C 0x0000 05F7	PR0_PRU0_GPIO6	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_REF_CLK	2	IO								
				RGMII2_RXC	3	I								
				MII2_RXCLK	4	I								
				EPWM24_A	5	O								
				GPIO91	7	IO								
				EPWM24_A	10	O								
G15	G15	G15	PR0_PRU0_GPIO8 PR0_PRU0_GPIO8_CFG_REG 0x5310 0168 0x0000 05F7	PR0_PRU0_GPIO8	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				EPWM23_B	5	O								
				GPIO90	7	IO								
				EPWM29_A	10	O								
F17	F17	F17	PR0_PRU0_GPIO9 PR0_PRU0_GPIO9_CFG_REG 0x5310 0160 0x0000 05F7	PR0_PRU0_GPIO9	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				PR0_UART0_CTSn	3	I								
				MII2_COL	4	I								
				EPWM22_B	5	O								
				GPIO88	7	IO								
G18	G18	G18	PR0_PRU0_GPIO10 PR0_PRU0_GPIO10_CFG_REG 0x5310 0164 0x0000 05F7	PR0_PRU0_GPIO10	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_CRS_DV	2	I								
				PR0_UART0_RTSn	3	O								
				MII2_CRS	4	I								
				EPWM23_A	5	O								
				GPIO89	7	IO								
				EPWM22_B	10	O								
M16	M16	M16	PR0_PRU0_GPIO11 PR0_PRU0_GPIO11_CFG_REG 0x5310 018C 0x0000 05F7	PR0_PRU0_GPIO11	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_TXD0	2	O								
				RGMII2_TD0	3	O								
				MII2_TXD0	4	O								
				EPWM28_A	5	O								
				GPIO99	7	IO								
				EPWM28_A	10	O								
M15	M15	M15	PR0_PRU0_GPIO12 PR0_PRU0_GPIO12_CFG_REG 0x5310 0190 0x0000 05F7	PR0_PRU0_GPIO12	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_TXD1	2	O								
				RGMII2_TD1	3	O								
				MII2_TXD1	4	O								
				EPWM28_B	5	O								
				GPIO100	7	IO								
				EPWM28_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
H17	H17	H17	PR0_PRU0_GPIO13 PR0_PRU0_GPIO13_CFG_REG 0x5310 0194 0x0000 05F7	PR0_PRU0_GPIO13	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RGMII2_TD2	3	O								
				MII2_TXD2	4	O								
				EPWM29_A	5	O								
				GPIO101	7	IO								
				EPWM27_B	10	O								
H16	H16	H16	PR0_PRU0_GPIO14 PR0_PRU0_GPIO14_CFG_REG 0x5310 0198 0x0000 05F7	PR0_PRU0_GPIO14	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RGMII2_TD3	3	O								
				MII2_TXD3	4	O								
				EPWM29_B	5	O								
				GPIO102	7	IO								
				EPWM29_B	10	O								
L16	L16	L16	PR0_PRU0_GPIO15 PR0_PRU0_GPIO15_CFG_REG 0x5310 0188 0x0000 05F7	PR0_PRU0_GPIO15	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII2_TX_EN	2	O								
				RGMII2_TX_CTL	3	O								
				MII2_TX_EN	4	O								
				EPWM27_B	5	O								
				GPIO98	7	IO								
H18	H18	H18	PR0_PRU0_GPIO16 PR0_PRU0_GPIO16_CFG_REG 0x5310 0184 0x0000 05F7	PR0_PRU0_GPIO16	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RGMII2_TXC	3	O								
				MII2_TXCLK	4	I								
				EPWM27_A	5	O								
				GPIO97	7	IO								
				EPWM27_A	10	O								
F18	F18	F18	PR0_PRU1_GPIO0 PR0_PRU1_GPIO0_CFG_REG 0x5310 01B4 0x0000 05F7	PR0_PRU1_GPIO0	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN1_RX	1	I								
				FSITX2_DATA1	3	O								
				TRC_DATA6	4	O								
				GPIO109	7	IO								
				EPWM23_A	10	O								
G16	G16	G16	PR0_PRU1_GPIO1 PR0_PRU1_GPIO1_CFG_REG 0x5310 01B8 0x0000 05F7	PR0_PRU1_GPIO1	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN1_TX	1	O								
				FSIRX2_CLK	3	I								
				TRC_DATA7	4	O								
				GPIO110	7	IO								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
E17	E17	E17	PR0_PRU1_GPIO2 PR0_PRU1_GPIO2_CFG_REG 0x5310 01BC 0x0000 05F7	PR0_PRU1_GPIO2	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN4_RX	1	I								
				FSIRX2_DATA0	3	I								
				TRC_DATA8	4	O								
				GPIO111	7	IO								
E18	E18	E18	PR0_PRU1_GPIO3 PR0_PRU1_GPIO3_CFG_REG 0x5310 01C0 0x0000 05F7	PR0_PRU1_GPIO3	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN4_TX	1	O								
				FSIRX2_DATA1	3	I								
				TRC_DATA9	4	O								
				GPIO112	7	IO								
				EPWM23_B	10	O								
F16	F16	F16	PR0_PRU1_GPIO4 PR0_PRU1_GPIO4_CFG_REG 0x5310 01B0 0x0000 05F7	PR0_PRU1_GPIO4	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN0_TX	1	O								
				FSITX2_DATA0	3	O								
				TRC_DATA5	4	O								
				GPIO108	7	IO								
F15	F15	F15	PR0_PRU1_GPIO5 PR0_PRU1_GPIO5_CFG_REG 0x5310 019C 0x0000 05F7	PR0_PRU1_GPIO5	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_CS0	2	IO								
				TRC_DATA0	4	O								
				EPWM30_A	5	O								
				GPIO103	7	IO								
				ADC_EXTCH_XBAROUT6	9	O								
				EPWM30_A	10	O								
E16	E16	E16	PR0_PRU1_GPIO6 PR0_PRU1_GPIO6_CFG_REG 0x5310 01AC 0x0000 05F7	PR0_PRU1_GPIO6	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN0_RX	1	I								
				FSITX2_CLK	3	O								
				TRC_DATA4	4	O								
				GPIO107	7	IO								
D18	D18	D18	PR0_PRU1_GPIO8 PR0_PRU1_GPIO8_CFG_REG 0x5310 01A8 0x0000 05F7	PR0_PRU1_GPIO8	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_D1	2	IO								
				TRC_DATA3	4	O								
				EPWM31_B	5	O								
				GPIO106	7	IO								
				RES0_PWMOUT1	8	O								
				EPWM31_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
C18	C18	C18	PR0_PRU1_GPIO9 PR0_PRU1_GPIO9_CFG_REG 0x5310 01A0 0x0000 05F7	PR0_PRU1_GPIO9	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_CLK	2	IO								
				PR0_UART0_RXD	3	I								
				TRC_DATA1	4	O								
				EPWM30_B	5	O								
				GPIO104	7	IO								
				ADC_EXTCH_XBAROUT7	9	O								
D17	D17	D17	PR0_PRU1_GPIO10 PR0_PRU1_GPIO10_CFG_REG 0x5310 01A4 0x0000 05F7	PR0_PRU1_GPIO10	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				SPI5_D0	2	IO								
				PR0_UART0_TXD	3	O								
				TRC_DATA2	4	O								
				EPWM31_A	5	O								
				GPIO105	7	IO								
				RES0_PWMOUT0	8	O								
				EPWM31_A	10	O								
B18	B18	B18	PR0_PRU1_GPIO11 PR0_PRU1_GPIO11_CFG_REG 0x5310 01CC 0x0000 05F7	PR0_PRU1_GPIO11	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN6_RX	1	I								
				SPI6_CS0	2	IO								
				FSITX3_DATA1	3	O								
				TRC_DATA12	4	O								
				EPWM16_A	5	O								
				GPIO115	7	IO								
B17	B17	B17	PR0_PRU1_GPIO12 PR0_PRU1_GPIO12_CFG_REG 0x5310 01D0 0x0000 05F7	PR0_PRU1_GPIO12	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN6_TX	1	O								
				SPI6_CLK	2	IO								
				FSIRX3_CLK	3	I								
				TRC_DATA13	4	O								
				EPWM16_B	5	O								
				GPIO116	7	IO								
D16	D16	D16	PR0_PRU1_GPIO13 PR0_PRU1_GPIO13_CFG_REG 0x5310 01D4 0x0000 05F7	PR0_PRU1_GPIO13	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN7_RX	1	I								
				SPI6_D0	2	IO								
				FSIRX3_DATA0	3	I								
				TRC_DATA14	4	O								
				XBAROUT11	5	O								
				GPIO117	7	IO								
				RES0_PWMOUT0	8	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
C17	C17	C17	PR0_PRU1_GPIO14 PR0_PRU1_GPIO14_CFG_REG 0x5310 01D8 0x0000 05F7	PR0_PRU1_GPIO14	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN7_TX	1	O								
				SPI6_D1	2	IO								
				FSIRX3_DATA1	3	I								
				TRC_DATA15	4	O								
				XBAROUT12	5	O								
				GPIO118	7	IO								
				RES0_PWMOUT1	8	O								
A17	A17	A17	PR0_PRU1_GPIO15 PR0_PRU1_GPIO15_CFG_REG 0x5310 01C8 0x0000 05F7	PR0_PRU1_GPIO15	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN5_TX	1	O								
				FSITX3_DATA0	3	O								
				TRC_DATA11	4	O								
				GPIO114	7	IO								
C16	C16	C16	PR0_PRU1_GPIO16 PR0_PRU1_GPIO16_CFG_REG 0x5310 01C4 0x0000 05F7	PR0_PRU1_GPIO16	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MCAN5_RX	1	I								
				FSITX3_CLK	3	O								
				TRC_DATA10	4	O								
				GPIO113	7	IO								
C15	C15	C15	PR0_PRU1_GPIO18 PR0_PRU1_GPIO18_CFG_REG 0x5310 01E0 0x0000 05F7	PR0_PRU1_GPIO18	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_TXD	2	O								
				PR0_IEP0_EDIO_DATA_IN_OUT31	3	IO								
				TRC_CTL	4	O								
				XBAROUT14	5	O								
				GPIO120	7	IO								
				EQEP1_B	9	I								
D15	D15	D15	PR0_PRU1_GPIO19 PR0_PRU1_GPIO19_CFG_REG 0x5310 01DC 0x0000 05F7	PR0_PRU1_GPIO19	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_RXD	2	I								
				PR0_IEP0_EDC_SYNC_OUT0	3	O								
				TRC_CLK	4	O								
				XBAROUT13	5	O								
				GPIO119	7	IO								
				EQEP1_A	9	I								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
R17			RGMII1_RXC RGMII1_RXC_CFG_REG 0x5310 0074 0x0000 05F7	RGMII1_RXC	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_REF_CLK	1	IO								
				MII1_RXCLK	2	I								
				FSITX0_CLK	6	O								
				GPIO29	7	IO								
				EQEP2_A	8	I								
				EPWM14_A	10	O								
R18			RGMII1_RX_CTL RGMII1_RX_CTL_CFG_REG 0x5310 0078 0x0000 05F7	RGMII1_RX_CTL	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_RX_ER	1	I								
				MII1_RXDV	2	I								
				FSITX0_DATA0	6	O								
				GPIO30	7	IO								
				EQEP2_B	8	I								
N18			RGMII1_TXC RGMII1_TXC_CFG_REG 0x5310 008C 0x0000 05F7	RGMII1_TXC	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MII1_TXCLK	2	I								
				FSITX1_CLK	6	O								
				GPIO35	7	IO								
				EQEP0_INDEX	8	IO								
				EPWM14_B	10	O								
M18			RGMII1_TX_CTL RGMII1_TX_CTL_CFG_REG 0x5310 0090 0x0000 05F7	RGMII1_TX_CTL	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_TX_EN	1	O								
				MII1_TX_EN	2	O								
				FSITX1_DATA0	6	O								
				GPIO36	7	IO								
				EQEP0_STROBE	8	IO								
				EPWM15_B	10	O								
U17			RGMII1_RD0 RGMII1_RD0_CFG_REG 0x5310 007C 0x0000 05F7	RGMII1_RD0	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_RXD0	1	I								
				MII1_RXD0	2	I								
				FSITX0_DATA1	6	O								
				GPIO31	7	IO								
				EQEP2_STROBE	8	IO								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
T17			RGMII1_RD1 RGMII1_RD1_CFG_REG 0x5310 0080 0x0000 05F7	RGMII1_RD1	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_RXD1	1	I								
				MII1_RXD1	2	I								
				FSIRX0_CLK	6	I								
				GPIO32	7	IO								
				EQEP2_INDEX	8	IO								
U18			RGMII1_RD2 RGMII1_RD2_CFG_REG 0x5310 0084 0x0000 05F7	RGMII1_RD2	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MII1_RXD2	2	I								
				FSIRX0_DATA0	6	I								
				GPIO33	7	IO								
				EQEP0_A	8	I								
T18			RGMII1_RD3 RGMII1_RD3_CFG_REG 0x5310 0088 0x0000 05F7	RGMII1_RD3	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MII1_RXD3	2	I								
				FSIRX0_DATA1	6	I								
				GPIO34	7	IO								
				EQEP0_B	8	I								
P16			RGMII1_TD0 RGMII1_TD0_CFG_REG 0x5310 0094 0x0000 05F7	RGMII1_TD0	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_TXD0	1	O								
				MII1_TXD0	2	O								
				FSITX1_DATA1	6	O								
				GPIO37	7	IO								
				EQEP1_A	8	I								
				EPWM15_A	9	O								
				EPWM15_B	10	O								
P17			RGMII1_TD1 RGMII1_TD1_CFG_REG 0x5310 0098 0x0000 05F7	RGMII1_TD1	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_TXD1	1	O								
				MII1_TXD1	2	O								
				FSIRX1_CLK	6	I								
				GPIO38	7	IO								
				EQEP1_B	8	I								
P18			RGMII1_TD2 RGMII1_TD2_CFG_REG 0x5310 009C 0x0000 05F7	RGMII1_TD2	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				RMII1_CRS_DV	1	I								
				MII1_TXD2	2	O								
				FSIRX1_DATA0	6	I								
				GPIO39	7	IO								
				EQEP1_STROBE	8	IO								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
N17			RGMII1_TD3 RGMII1_TD3_CFG_REG 0x5310 00A0 0x0000 05F7	RGMII1_TD3	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				MII1_TXD3	2	O								
				FSIRX1_DATA1	6	I								
				GPIO40	7	IO								
				EQEP1_INDEX	8	IO								
J16	J16	J16	RSVD_J16	RSVD_J16		RSVD				Reserved	Reserved		Reserved	
	P15	P15	RSVD_P15	RSVD_P15		RSVD				Reserved	Reserved		Reserved	
T4	T4	T4	RSVD_T4	RSVD_T4		RSVD				Reserved	Reserved		Reserved	
U1	U1	U1	RSVD_U1	RSVD_U1		RSVD				Reserved	Reserved		Reserved	
U3	U3	U3	RSVD_U3	RSVD_U3		RSVD				Reserved	Reserved		Reserved	
V2	V2	V2	RSVD_V2	RSVD_V2		RSVD				Reserved	Reserved		Reserved	
D4	D4	D4	SAFETY_ERRORn SAFETY_ERRORn_CFG_REG 0x5310 0230 0x410	SAFETY_ERRORn	0	IO	On / Off / Down	On / NA / Down	0	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
B16	B16	B16	SDFM0_CLK0 SDFM0_CLK0_CFG_REG 0x5310 01E8 0x0000 05F7	CLKOUT1	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO122	7	IO								
				SDFM0_CLK0	8	I								
				EQEP1_STROBE	9	IO								
A16	A16	A16	SDFM0_CLK1 SDFM0_CLK1_CFG_REG 0x5310 01F0 0x0000 05F7	PR0_PRU1_GPIO7	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				CPTS0_TS_SYNC	1	O								
				UART5_RTSn	2	O								
				PR0_IEP0_EDC_SYNC_OUT1	3	O								
				I2C3_SDA	5	IO								
				GPIO124	7	IO								
				SDFM0_CLK1	8	I								
B15	B15	B15	SDFM0_CLK2 SDFM0_CLK2_CFG_REG 0x5310 01F8 0x0000 05F7	UART5_TXD	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				I2C3_SCL	5	IO								
				GPIO126	7	IO								
				SDFM0_CLK2	8	I								
				ADC_EXTCH_XBAROUT8	9	O								
A15	A15	A15	SDFM0_CLK3 SDFM0_CLK3_CFG_REG 0x5310 0200 0x0000 05F7	MCAN3_TX	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART5_RXD	1	I								
				GPIO128	7	IO								
				SDFM0_CLK3	8	I								
				ADC_EXTCH_XBAROUT9	9	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
D14	D14	D14	SDFM0_D0 SDFM0_D0_CFG_REG 0x5310 01EC 0x0000 05F7	PR0_ECAP0_APWM_OUT	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO123	7	IO								
				SDFM0_D0	8	I								
D13	D13	D13	SDFM0_D1 SDFM0_D1_CFG_REG 0x5310 01F4 0x0000 05F7	PR0_PRU1_GPIO17	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART5_CTSn	2	I								
				PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO								
				GPIO125	7	IO								
				SDFM0_D1	8	I								
C13	C13	C13	SDFM0_D2 SDFM0_D2_CFG_REG 0x5310 01FC 0x0000 05F7	UART5_RXD	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO127	7	IO								
				SDFM0_D2	8	I								
				ADC_EXTCH_XBAROUT0	9	O								
C14	C14	C14	SDFM0_D3 SDFM0_D3_CFG_REG 0x5310 0204 0x0000 05F7	MCAN3_RX	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				GPIO129	7	IO								
				SDFM0_D3	8	I								
				ADC_EXTCH_XBAROUT1	9	O								
A11	A11	A11	SPI0_CLK SPI0_CLK_CFG_REG 0x5310 0030 0x0000 05D7	SPI0_CLK	0	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_TXD	1	O								
				LIN3_TXD	2	IO								
				FSITX0_CLK	6	O								
				GPIO12	7	IO								
				ADC_EXTCH_XBAROUT1	9	O								
				SOP2	Bootstrap	IO								
A10	A10	A10	SPI1_CLK SPI1_CLK_CFG_REG 0x5310 0040 0x0000 05F7	SPI1_CLK	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART4_RXD	1	I								
				LIN4_RXD	2	IO								
				XBAROUT2	5	O								
				FSIRX0_CLK	6	I								
				GPIO16	7	IO								
				ADC_EXTCH_XBAROUT5	9	O								
C11	C11	C11	SPI0_CS0 SPI0_CS0_CFG_REG 0x5310 002C 0x0000 05F7	SPI0_CS0	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART3_RXD	1	I								
				LIN3_RXD	2	IO								
				GPIO11	7	IO								
				ADC_EXTCH_XBAROUT0	9	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
C10	C10	C10	SPI0_D0 SPI0_D0_CFG_REG 0x5310 0034 0x0000 05D7	SPI0_D0	0	IO	On / Off / Off	On / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				FSITX0_DATA0	6	O								
				GPIO13	7	IO								
				ADC_EXTCH_XBAROUT2	9	O								
				SOP3	Bootstrap	IO								
B11	B11	B11	SPI0_D1 SPI0_D1_CFG_REG 0x5310 0038 0x0000 05F7	SPI0_D1	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				FSITX0_DATA1	6	O								
				GPIO14	7	IO								
				ADC_EXTCH_XBAROUT3	9	O								
C9	C9	C9	SPI1_CS0 SPI1_CS0_CFG_REG 0x5310 003C 0x0000 05F7	SPI1_CS0	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART4_TXD	1	O								
				LIN4_TXD	2	IO								
				XBAROUT1	5	O								
				GPIO15	7	IO								
				ADC_EXTCH_XBAROUT4	9	O								
B10	B10	B10	SPI1_D0 SPI1_D0_CFG_REG 0x5310 0044 0x0000 05F7	SPI1_D0	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART5_TXD	1	O								
				XBAROUT3	5	O								
				FSIRX0_DATA0	6	I								
				GPIO17	7	IO								
				ADC_EXTCH_XBAROUT6	9	O								
D9	D9	D9	SPI1_D1 SPI1_D1_CFG_REG 0x5310 0048 0x0000 05F7	SPI1_D1	0	IO	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				UART5_RXD	1	I								
				XBAROUT4	5	O								
				FSIRX0_DATA1	6	I								
				GPIO18	7	IO								
				ADC_EXTCH_XBAROUT7	9	O								
B3	B3	B3	TCK TCK_CFG_REG 0x5310 0240 0x210	TCK	0	I	On / NA / Up	On / NA / Up	0	3.3V	VDDSHV0	Yes	HIGH HYST	
C5	C5	C5	TDI TDI_CFG_REG 0x5310 0234 0x6D0	TDI	0	I	On / Off / Up	On / Off / Up	0	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
C4	C4	C4	TDO TDO_CFG_REG 0x5310 0238 0x630	TDO	0	O	Off / Off / Up	Off / NA / Up	0	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
D5	D5	D5	TMS TMS_CFG_REG 0x5310 023C 0x610	TMS	0	IO	On / Off / Up	On / NA / Up	0	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
B7	B7	B7	UART0_CTSn UART0_CTSn_CFG_REG 0x5310 0068 0x0000 05F7	UART0_CTSn	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				I2C2_SDA	1	IO								
				SPI3_D1	2	IO								
				MCAN3_RX	3	I								
				SPI0_CS1	4	IO								
				XBAROUT10	5	O								
				GPIO26	7	IO								
C7	C7	C7	UART0_RTSn UART0_RTSn_CFG_REG 0x5310 0064 0x0000 05F7	UART0_RTSn	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				I2C2_SCL	1	IO								
				SPI3_D0	2	IO								
				MCAN3_TX	3	O								
				XBAROUT9	5	O								
				GPIO25	7	IO								
A7	A7	A7	UART0_RXD UART0_RXD_CFG_REG 0x5310 006C 0x0000 05F7	UART0_RXD	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN0_RXD	1	IO								
				GPIO27	7	IO								
A6	A6	A6	UART0_TXD UART0_TXD_CFG_REG 0x5310 0070 0x0000 05F7	UART0_TXD	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN0_TXD	1	IO								
				GPIO28	7	IO								
L3	L3		UART1_RXD UART1_RXD_CFG_REG 0x5310 012C 0x0000 05F7	UART1_RXD	0	I	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN1_RXD	1	IO								
				OSPI0_LBCLKO	2	O								
				EPWM16_A	5	O								
				GPIO75	7	IO								
				EPWM16_A	10	O								
				EPWM10_A	11	O								
M3	M3		UART1_TXD UART1_TXD_CFG_REG 0x5310 0130 0x0000 05F7	UART1_TXD	0	O	Off / Off / Off	Off / Off / Off	7	3.3V	VDDSHV0	Yes	LVCMOS	PU/PD
				LIN1_TXD	1	IO								
				OSPI0_DQS	2	I								
				EPWM16_B	5	O								
				GPIO76	7	IO								
				EPWM16_B	10	O								

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6, R9	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6, R9	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6, R9	VDD	VDD		PWR				1.2V				
R11, R8	R11, R8	R11, R8	VDDA18	VDDA18		PWR				1.8V				
R6	R6	R6	VDDA18_LDO	VDDA18_LDO		PWR				1.8V				
R4	R4	R4	VDDA18_OSC_PLL	VDDA18_OSC_PLL		PWR				1.8V				
P11, P7, P9	P11, P7, P9	P11, P7, P9	VDDA33	VDDA33		PWR				3.3V				
J15	J15	J15	VDDAR1	VDDAR1		PWR				1.2V				
D10	D10	D10	VDDAR2	VDDAR2		PWR				1.2V				
H3	H3	H3	VDDAR3	VDDAR3		PWR				1.2V				
D6, E15, L4, N15	D6, E15, L4, N15	D6, E15, L4, N15	VDDS18	VDDS18		PWR				1.8V				
T3	T3	T3	VDDS18_LDO	VDDS18_LDO		PWR				1.8V				
D12, D8, H15, H4, L15, P4, R15	D12, D8, H15, H4, L15, P4, R15	D12, D8, H15, H4, L15, P4, R15	VDDS33	VDDS33		PWR				3.3V				
N3	N3	N3	VPP	VPP		PWR				VPP				

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2, V18	A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2	A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2	VSS	VSS		GND					VSS				
P10, P12, P6, P8, R13, R5, V1, V16	P10, P12, P6, P8, R13, R5, V1, V18	P10, P12, P6, P8, R13, R5, V1, V18	VSSA	VSSA		AGND					VSSA				
U2	U2	U2	VSYS_MON	VSYS_MON		A					0.9V	VDDA_CIO		AnalogCIO	

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Table 5-1. Pin Attributes (ZCZ_C, ZCZ_S, ZCZ_F Packages) (continued)

ZCZ_C BALL NUMBER [1]	ZCZ_S BALL NUMBER [1]	ZCZ_F BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL TYPE [13]
C3	C3	C3	WARMRSTn WARMRSTn_CFG_REG 0x5310 022C 0x510	WARMRSTn	0	IO	On / Off / Off	On / NA / Off	0	3.3V	VDDSHV0		FS OD	
T1	T1	T1	XTAL_XI	XTAL_XI		I				1.8V	VDDA18_OSC_PLL	Yes	HFOSC	
R1	R1	R1	XTAL_XO	XTAL_XO		O				1.8V	VDDA18_OSC_PLL		HFOSC	

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5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - ID = Input with open-drain output function
   - OD = Output, with open-drain output function
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

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5.3.1 ADC

Table 5-2. ADC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC0_AIN0	I	ADC Analog Input 0 (+IN0) CMPSSA0: inH (+IN)	V15	V15	V15
ADC0_AIN1	I	ADC Analog Input 1 (-IN0) CMPSSA0: inL (-IN)	U15	U15	U15
ADC0_AIN2	I	ADC Analog Input 2 (+IN1) CMPSSA1: inH (+IN)	T14	T14	T14
ADC0_AIN3	I	ADC Analog Input 3 (-IN1) CMPSSA1: inL (-IN)	U14	U14	U14
ADC0_AIN4	I	ADC Analog Input 4 (+IN2) CMPSSB0: inH/inL (+IN/-IN)	U13	U13	U13
ADC0_AIN5	I	ADC Analog Input 5 (-IN2) CMPSSB1: inH/inL (+IN/-IN)	R14	R14	R14

Table 5-3. ADC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC1_AIN0	I	ADC Analog Input 0 (+IN0) CMPSSA2: inH (+IN)	T11	T11	T11
ADC1_AIN1	I	ADC Analog Input 1 (-IN0) CMPSSA2: inL (-IN)	U11	U11	U11
ADC1_AIN2	I	ADC Analog Input 2 (+IN1) CMPSSA3: inH (+IN)	T12	T12	T12
ADC1_AIN3	I	ADC Analog Input 3 (-IN1) CMPSSA3: inL (-IN)	V12	V12	V12
ADC1_AIN4	I	ADC Analog Input 4 (+IN2) CMPSSB2: inH/inL (+IN/-IN)	U12	U12	U12
ADC1_AIN5	I	ADC Analog Input 5 (-IN2) CMPSSB3: inH/inL (+IN/-IN)	R12	R12	R12

Table 5-4. ADC2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC2_AIN0	I	ADC Analog Input 0 (+IN0) CMPSSA4: inH (+IN)	R10	R10	R10
ADC2_AIN1	I	ADC Analog Input 1 (-IN0) CMPSSA4: inL (-IN)	T10	T10	T10
ADC2_AIN2	I	ADC Analog Input 2 (+IN1) CMPSSA5: inH (+IN)	U10	U10	U10
ADC2_AIN3	I	ADC Analog Input 3 (-IN1) CMPSSA5: inL (-IN)	T9	T9	T9
ADC2_AIN4	I	ADC Analog Input 4 (+IN2) CMPSSB4: inH/inL (+IN/-IN)	V9	V9	V9
ADC2_AIN5	I	ADC Analog Input 5 (-IN2) CMPSSB5: inH/inL (+IN/-IN)	T8	T8	T8

Table 5-5. ADC3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC3_AIN0	I	ADC Analog Input 0 (+IN0) CMPSSA6: inH (+IN)	U7	U7	U7
ADC3_AIN1	I	ADC Analog Input 1 (-IN0) CMPSSA6: inL (-IN)	U8	U8	U8
ADC3_AIN2	I	ADC Analog Input 2 (+IN1) CMPSSA7: inH (+IN)	T7	T7	T7
ADC3_AIN3	I	ADC Analog Input 3 (-IN1) CMPSSA7: inL (-IN)	R7	R7	R7
ADC3_AIN4	I	ADC Analog Input 4 (+IN2) CMPSSB6: inH/inL (+IN/-IN)	V8	V8	V8

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Table 5-5. ADC3 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC3_AIN5	I	ADC Analog Input 5 (-IN2) CMPSSB7: inH/inL (+IN/-IN)	U9	U9	U9

Table 5-6. ADC4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC4_AIN0	I	ADC Analog Input 0 (+IN0) CMPSSA8: inH (+IN)	U6	U6	U6
ADC4_AIN1	I	ADC Analog Input 1 (-IN0) CMPSSA8: inL (-IN)	V5	V5	V5
ADC4_AIN2	I	ADC Analog Input 2 (+IN1) CMPSSA9: inH (+IN)	V4	V4	V4
ADC4_AIN3	I	ADC Analog Input 3 (-IN1) CMPSSA9: inL (-IN)	U5	U5	U5
ADC4_AIN4	I	ADC Analog Input 4 (+IN2) CMPSSB8: inH/inL (+IN/-IN)	V3	V3	V3
ADC4_AIN5	I	ADC Analog Input 5 (-IN2) CMPSSB9: inH/inL (+IN/-IN)	U4	U4	U4

5.3.1.1 ADC-CMPSS Signal Connections

In each ADC, two sets of differential pins shall be shared with pins of two CMPSSA and remaining one pair of differential pins shall be connected to two independent pins of CMPSSB. These pins are demonstrated in Figure 5-1 and Table 5-7 where the CHSEL values determine how the inputs are fed into ADC.

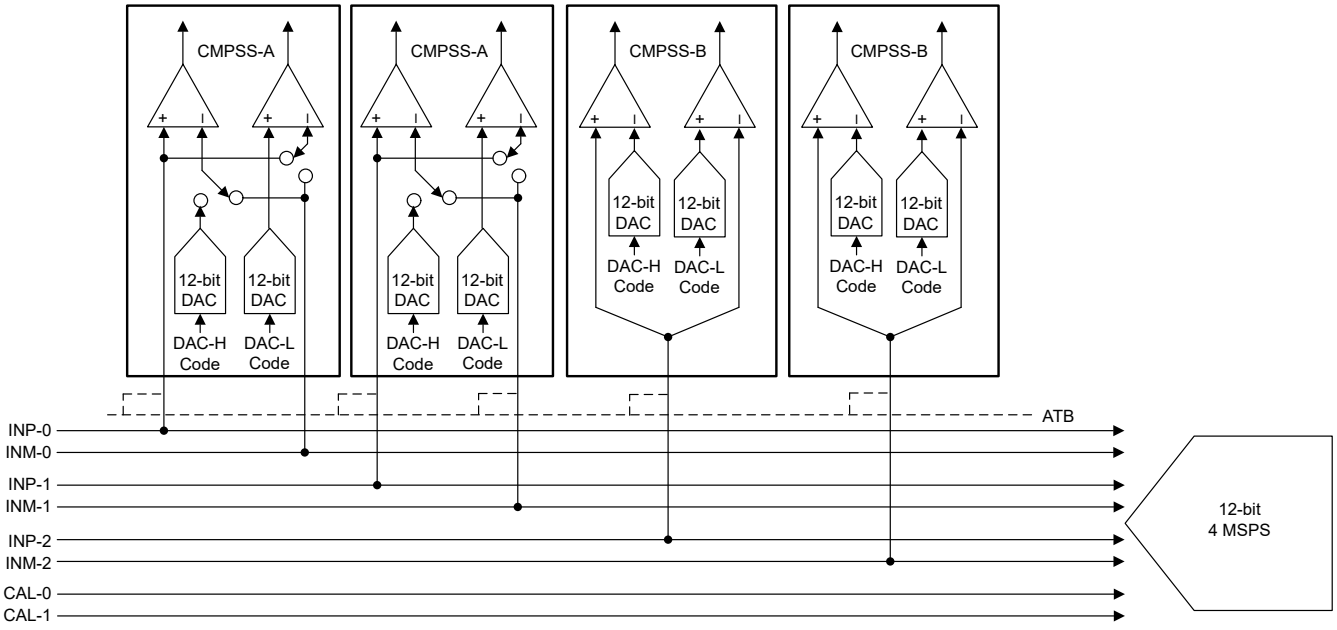

Figure 5-1. CMPSS and ADC Connections

Table 5-7. Connectivity between ADC Inputs to CMPSS Signals

Signal/Pin Name	ADC Input	CMPSS Input
ADC0 Channels		
ADC0_AIN0	ADC0:inp0 (+IN0)	CMPSSA0:inH (+IN)
ADC0_AIN1	ADC0:inm0 (-IN0)	CMPSSA0:inL (-IN)
ADC0_AIN2	ADC0:inp1 (+IN1)	CMPSSA1:inH (+IN)
ADC0_AIN3	ADC0:inm1 (-IN1)	CMPSSA1:inL (-IN)
ADC0_AIN4	ADC0:inp2 (+IN2)	CMPSSB0:inH/inL (+IN/-IN)

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Table 5-7. Connectivity between ADC Inputs to CMPSS Signals (continued)

Signal/Pin Name	ADC Input	CMPSS Input
ADC0_AIN5	ADC0:inm2 (-IN2)	CMPSSB1:inH/inL (+IN/-IN)
ADC_CAL1	ADC0:inm3 (-IN3)	X
ADC_CAL0	ADC0:inp3 (+IN3)	X
ADC1 Channels		
ADC1_AIN0	ADC1:inp0 (+IN0)	CMPSSA2:inH (+IN)
ADC1_AIN1	ADC1:inm0 (-IN0)	CMPSSA2:inL (-IN)
ADC1_AIN2	ADC1:inp1 (+IN1)	CMPSSA3:inH (+IN)
ADC1_AIN3	ADC1:inm1 (-IN1)	CMPSSA3:inL (-IN)
ADC1_AIN4	ADC1:inp2 (+IN2)	CMPSSB2:inH/inL (+IN/-IN)
ADC1_AIN5	ADC1:inm2 (-IN2)	CMPSSB3:inH/inL (+IN/-IN)
ADC_CAL1	ADC1:inm3 (-IN3)	X
ADC_CAL0	ADC1:inp3 (+IN3)	X
ADC2 Channels		
ADC2_AIN0	ADC2:inp0 (+IN0)	CMPSSA4:inH (+IN)
ADC2_AIN1	ADC2:inm0 (-IN0)	CMPSSA4:inL (-IN)
ADC2_AIN2	ADC2:inp1 (+IN1)	CMPSSA5:inH (+IN)
ADC2_AIN3	ADC2:inm1 (-IN1)	CMPSSA5:inL (-IN)
ADC2_AIN4	ADC2:inp2 (+IN2)	CMPSSB4:inH/inL (+IN/-IN)
ADC2_AIN5	ADC2:inm2 (-IN2)	CMPSSB5:inH/inL (+IN/-IN)
ADC_CAL1	ADC2:inm3 (-IN3)	X
ADC_CAL0	ADC2:inp3 (+IN3)	X
ADC3 Channels		
ADC3_AIN0	ADC3:inp0 (+IN0)	CMPSSA6:inH (+IN)
ADC3_AIN1	ADC3:inm0 (-IN0)	CMPSSA6:inL (-IN)
ADC3_AIN2	ADC3:inp1 (+IN1)	CMPSSA7:inH (+IN)
ADC3_AIN3	ADC3:inm1 (-IN1)	CMPSSA7:inL (-IN)
ADC3_AIN4	ADC3:inp2 (+IN2)	CMPSSB6:inH/inL (+IN/-IN)
ADC3_AIN5	ADC3:inm2 (-IN2)	CMPSSB7:inH/inL (+IN/-IN)
ADC_CAL1	ADC3:inm3 (-IN3)	X
ADC_CAL0	ADC3:inp3 (+IN3)	X
ADC4 Channels		
ADC4_AIN0	ADC4:inp0 (+IN0)	CMPSSA8:inH (+IN)
ADC4_AIN1	ADC4:inm0 (-IN0)	CMPSSA8:inL (-IN)
ADC4_AIN2	ADC4:inp1 (+IN1)	CMPSSA9:inH (+IN)
ADC4_AIN3	ADC4:inm1 (-IN1)	CMPSSA9:inL (-IN)
ADC4_AIN4	ADC4:inp2 (+IN2)	CMPSSB8:inH/inL (+IN/-IN)
ADC4_AIN5	ADC4:inm2 (-IN2)	CMPSSB9:inH/inL (+IN/-IN)
ADC_CAL0	ADC4:inp3 (+IN3)	X
ADC_CAL1	ADC4:inm3 (-IN3)	X

Note

In the **ADC Input** column in ADC-CMPSS Signal Connectivity Table above, "inp" stands for positive inputs and "inm" stands for negative inputs.

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5.3.2 ADC Resolver

Table 5-8. ADC_R0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC_R0_AIN0	I	ADC Resolver Analog Input 0		T18	T18
ADC_R0_AIN1	I	ADC Resolver Analog Input 1		T16	T16
ADC_R0_AIN2	I	ADC Resolver Analog Input 2		U18	U18
ADC_R0_AIN3	I	ADC Resolver Analog Input 3		T17	T17

Table 5-9. ADC_R1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC_R1_AIN0	I	ADC Resolver Analog Input 0		R16	R16
ADC_R1_AIN1	I	ADC Resolver Analog Input 1		R18	R18
ADC_R1_AIN2	I	ADC Resolver Analog Input 2		P18	P18
ADC_R1_AIN3	I	ADC Resolver Analog Input 3		P17	P17

Table 5-10. Resolver PWM Output Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RES0_PWMOUT0	O	Resolver PWM Output Signal 0	D16, D17	D16, D17	D16, D17
RES0_PWMOUT1	O	Resolver PWM Output Signal 1	C17, D18	C17, D18	C17, D18

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5.3.3 ADC_CAL

Table 5-11. ADC_CAL Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC_CAL0 (1)	I	ADC Calibration Pin 0	U16	U16	U16
ADC_CAL1 (1)	I	ADC Calibration Pin 1	T15	T15	T15
ADC_CAL2 (2)	A	ADC Calibration Pin 2		U17	U17
ADC_CAL3 (3)	A	ADC Calibration Pin 3		N17	N17

(1) This pin is shared between ADC[0:4] and ADC_R[0:1].
(2) This pin is shared between ADC_R[0].
(3) This pin is shared between ADC_R[1].

5.3.4 ADC VREF

Table 5-12. ADC_VREF Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC_VREFHI_G0	A	ADC Reference (Positive)	V14	V14	V14
ADC_VREFHI_G1 (2)	A	ADC Reference (Positive)	V10	V10	V10
ADC_VREFHI_G2	A	ADC Reference (Positive)	V6	V6	V6
ADC_VREFHI_G3 (5)	A	ADC Reference (Positive)		V17	V17
ADC_VREFLO_G0 (1)	A	ADC Reference (Negative)	V13	V13	V13
ADC_VREFLO_G1 (3)	A	ADC Reference (Negative)	V11	V11	V11
ADC_VREFLO_G2 (4)	A	ADC Reference (Negative)	V7	V7	V7
ADC_VREFLO_G3 (5)	A	ADC Reference (Negative)		V16	V16

(1) This pin should be connected (shorted) to analog ground (VSSA).
(2) This pin can be connected (shorted) to ADC_VREFHI_G0.
(3) This pin can be connected (shorted) to ADC_VREFLO_G0.
(4) This pin can be connected (shorted) to analog ground (VSSA).
(5) This pin only exists on the ZCZ_S package to support ADC_R[0:1]

5.3.5 CPSW

Table 5-13. CPSW0 RGMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	R17	R17	R17
RGMII1_RX_CTL	I	RGMII Receive Control	R18		
RGMII1_TXC	O	RGMII Transmit Clock	N18	N18	N18
RGMII1_TX_CTL	O	RGMII Transmit Control	M18	M18	M18
RGMII1_RD0	I	RGMII Receive Data 0	U17		
RGMII1_RD1	I	RGMII Receive Data 1	T17		
RGMII1_RD2	I	RGMII Receive Data 2	U18		
RGMII1_RD3	I	RGMII Receive Data 3	T18		
RGMII1_TD0	O	RGMII Transmit Data 0	P16	P16	P16
RGMII1_TD1	O	RGMII Transmit Data 1	P17		
RGMII1_TD2	O	RGMII Transmit Data 2	P18		
RGMII1_TD3	O	RGMII Transmit Data 3	N17		

Table 5-14. CPSW0 RGMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	K15	K15	K15
RGMII2_RX_CTL	I	RGMII Receive Control	K16	K16	K16
RGMII2_TXC	O	RGMII Transmit Clock	H18	H18	H18
RGMII2_TX_CTL	O	RGMII Transmit Control	L16	L16	L16
RGMII2_RD0	I	RGMII Receive Data 0	K17	K17	K17
RGMII2_RD1	I	RGMII Receive Data 1	K18	K18	K18

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Table 5-14. CPSW0 RGMII2 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RGMII2_RD2	I	RGMII Receive Data 2	J18	J18	J18
RGMII2_RD3	I	RGMII Receive Data 3	J17	J17	J17
RGMII2_TD0	O	RGMII Transmit Data 0	M16	M16	M16
RGMII2_TD1	O	RGMII Transmit Data 1	M15	M15	M15
RGMII2_TD2	O	RGMII Transmit Data 2	H17	H17	H17
RGMII2_TD3	O	RGMII Transmit Data 3	H16	H16	H16

Table 5-15. CPSW0 RMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	P18		
RMII1_REF_CLK	IO	RMII Reference Clock	R17	R17	R17
RMII1_RX_ER	I	RMII Receive Data Error	R18		
RMII1_TX_EN	O	RMII Transmit Enable	M18	M18	M18
RMII1_RXD0	I	RMII Receive Data 0	U17		
RMII1_RXD1	I	RMII Receive Data 1	T17		
RMII1_TXD0	O	RMII Transmit Data 0	P16	P16	P16
RMII1_TXD1	O	RMII Transmit Data 1	P17		

Table 5-16. CPSW0 RMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	G18	G18	G18
RMII2_REF_CLK	IO	RMII Reference Clock	K15	K15	K15
RMII2_RX_ER	I	RMII Receive Data Error	G17	G17	G17
RMII2_TX_EN	O	RMII Transmit Enable	L16	L16	L16
RMII2_RXD0	I	RMII Receive Data 0	K17	K17	K17
RMII2_RXD1	I	RMII Receive Data 1	K18	K18	K18
RMII2_TXD0	O	RMII Transmit Data 0	M16	M16	M16
RMII2_TXD1	O	RMII Transmit Data 1	M15	M15	M15

Table 5-17. CPSW0 MII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MII1_COL	I	MII Collision Detected	P15		
MII1_CRS	I	MII Carrier Sense	R16		
MII1_RXCLK	I	MII Receive Clock	R17	R17	R17
MII1_RXDV	I	MII Receive Data Valid	R18		
MII1_RX_ER	I	MII Receive Data Error	T16		
MII1_TXCLK	I	MII Transmit Clock	N18	N18	N18
MII1_TX_EN	O	MII Transmit Enable	M18	M18	M18
MII1_RXD0	I	MII Receive Data 0	U17		
MII1_RXD1	I	MII Receive Data 1	T17		
MII1_RXD2	I	MII Receive Data 2	U18		
MII1_RXD3	I	MII Receive Data 3	T18		
MII1_TXD0	O	MII Transmit Data 0	P16	P16	P16
MII1_TXD1	O	MII Transmit Data 1	P17		
MII1_TXD2	O	MII Transmit Data 2	P18		
MII1_TXD3	O	MII Transmit Data 3	N17		

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Table 5-18. CPSW0 MII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MII2_COL	I	MII Collision Detected	F17	F17	F17
MII2_CRS	I	MII Carrier Sense	G18	G18	G18
MII2_RXCLK	I	MII Receive Clock	K15	K15	K15
MII2_RXDV	I	MII Receive Data Valid	K16	K16	K16
MII2_RX_ER	I	MII Receive Error	G17	G17	G17
MII2_TXCLK	I	MII Transmit Clock	H18	H18	H18
MII2_TX_EN	O	MII Transmit Enable	L16	L16	L16
MII2_RXD0	I	MII Receive Data 0	K17	K17	K17
MII2_RXD1	I	MII Receive Data 1	K18	K18	K18
MII2_RXD2	I	MII Receive Data 2	J18	J18	J18
MII2_RXD3	I	MII Receive Data 3	J17	J17	J17
MII2_TXD0	O	MII Transmit Data 0	M16	M16	M16
MII2_TXD1	O	MII Transmit Data 1	M15	M15	M15
MII2_TXD2	O	MII Transmit Data 2	H17	H17	H17
MII2_TXD3	O	MII Transmit Data 3	H16	H16	H16

Table 5-19. MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MDIO0_MDC	O	MDIO Clock	M17	M17	M17
MDIO0_MDIO	IO	MDIO Data	N16	N16	N16

5.3.6 CPTS

Table 5-20. CPTS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output	A16	A16	A16

5.3.7 DAC

Table 5-21. DAC Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
DAC_OUT	O	DAC Output	T5	T5	T5
DAC_VREF0 (1) (2)	A	DAC Voltage Reference 0	T13	T13	T13
DAC_VREF1 (1) (2)	A	DAC Voltage Reference 1	T6	T6	T6

(1) See the *Layout Guidelines* sections for details on connecting these pins.
(2) This pin can be connected (shorted) to VDDA18_LDO.

5.3.8 EPWM

Table 5-22. EPWM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM0_A	O	EPWM Output A	B2	B2	B2
EPWM0_B	O	EPWM Output B	B1	B1	B1

Table 5-23. EPWM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM1_A	O	EPWM Output A	D3	D3	D3
EPWM1_B	O	EPWM Output B	D2, E4	D2, E4	D2, E4

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Table 5-24. EPWM2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM2_A	O	EPWM Output A	C2	C2	C2
EPWM2_B	O	EPWM Output B	C1	C1	C1

Table 5-25. EPWM3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM3_A	O	EPWM Output A	E2	E2	E2
EPWM3_B	O	EPWM Output B	E1, E3	E1, E3	E1, E3

Table 5-26. EPWM4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM4_A	O	EPWM Output A	D1	D1	D1
EPWM4_B	O	EPWM Output B	D2, E4	D2, E4	D2, E4

Table 5-27. EPWM5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM5_A	O	EPWM Output A	F2	F2	F2
EPWM5_B	O	EPWM Output B	F1, G2	F1, G2	F1, G2

Table 5-28. EPWM6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM6_A	O	EPWM Output A	E1, E3	E1, E3	E1, E3
EPWM6_B	O	EPWM Output B	F3	F3	F3

Table 5-29. EPWM7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM7_A	O	EPWM Output A	F4	F4	F4
EPWM7_B	O	EPWM Output B	F1, G4	F1, G4	F1, G4

Table 5-30. EPWM8 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM8_A	O	EPWM Output A	G3	G3	G3
EPWM8_B	O	EPWM Output B	G2, H2	G2, H2	G2, H2

Table 5-31. EPWM9 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM9_A	O	EPWM Output A	G1	G1	G1
EPWM9_B	O	EPWM Output B	H2, J2	H2, J2	H2, J2

Table 5-32. EPWM10 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM10_A	O	EPWM Output A	G4, J4, L3	G4, J4, L3	G4, L3
EPWM10_B	O	EPWM Output B	J3, R3	J3, R3	R3

Table 5-33. EPWM11 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM11_A	O	EPWM Output A	H1	H1	
EPWM11_B	O	EPWM Output B	J1, J2	J1, J2	J2

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Table 5-34. EPWM12 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM12_A	O	EPWM Output A	K2, N2	K2, N2	N2
EPWM12_B	O	EPWM Output B	J1, J4, N1	J1, J4, N1	N1

Table 5-35. EPWM13 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM13_A	O	EPWM Output A	K4, N4	K4, N4	N4
EPWM13_B	O	EPWM Output B	K1, K3	K1, K3	K1

Table 5-36. EPWM14 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM14_A	O	EPWM Output A	R17, V17	R17	R17
EPWM14_B	O	EPWM Output B	N18, T16	N18	N18

Table 5-37. EPWM15 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM15_A	O	EPWM Output A	P15, P16	P16	P16
EPWM15_B	O	EPWM Output B	M18, P16, R16	M18, P16	M18, P16

Table 5-38. EPWM16 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM16_A	O	EPWM Output A	B18, L3	B18, L3	B18, L3
EPWM16_B	O	EPWM Output B	B17, M3	B17, M3	B17, M3

Table 5-39. EPWM17 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM17_A	O	EPWM Output A	B6	B6	B6
EPWM17_B	O	EPWM Output B	A4	A4	A4

Table 5-40. EPWM18 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM18_A	O	EPWM Output A	B5	B5	B5
EPWM18_B	O	EPWM Output B	B4	B4	B4

Table 5-41. EPWM19 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM19_A	O	EPWM Output A	A3	A3	A3
EPWM19_B	O	EPWM Output B	A2	A2	A2

Table 5-42. EPWM20 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM20_A	O	EPWM Output A	C6	C6	C6
EPWM20_B	O	EPWM Output B	A5	A5	A5

Table 5-43. EPWM21 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM21_A	O	EPWM Output A	L17	L17	L17
EPWM21_B	O	EPWM Output B	L18	L18	L18

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Table 5-44. EPWM22 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM22_A	O	EPWM Output A	G17	G17	G17
EPWM22_B	O	EPWM Output B	F17, G18	F17, G18	F17, G18

Table 5-45. EPWM23 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM23_A	O	EPWM Output A	F18, G18	F18, G18	F18, G18
EPWM23_B	O	EPWM Output B	E18, G15	E18, G15	E18, G15

Table 5-46. EPWM24 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM24_A	O	EPWM Output A	K15	K15	K15
EPWM24_B	O	EPWM Output B	K16	K16	K16

Table 5-47. EPWM25 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM25_A	O	EPWM Output A	K17	K17	K17
EPWM25_B	O	EPWM Output B	K18	K18	K18

Table 5-48. EPWM26 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM26_A	O	EPWM Output A	J18	J18	J18
EPWM26_B	O	EPWM Output B	J17	J17	J17

Table 5-49. EPWM27 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM27_A	O	EPWM Output A	H18	H18	H18
EPWM27_B	O	EPWM Output B	H17, L16	H17, L16	H17, L16

Table 5-50. EPWM28 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM28_A	O	EPWM Output A	M16	M16	M16
EPWM28_B	O	EPWM Output B	M15	M15	M15

Table 5-51. EPWM29 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM29_A	O	EPWM Output A	G15, H17	G15, H17	G15, H17
EPWM29_B	O	EPWM Output B	H16	H16	H16

Table 5-52. EPWM30 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM30_A	O	EPWM Output A	F15	F15	F15
EPWM30_B	O	EPWM Output B	C18	C18	C18

Table 5-53. EPWM31 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EPWM31_A	O	EPWM Output A	D17	D17	D17
EPWM31_B	O	EPWM Output B	D18	D18	D18

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5.3.9 EQEP

Table 5-54. EQEP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EQEP0_A	I	EQEP Quadrature Input A	B14, U18	B14	B14
EQEP0_B	I	EQEP Quadrature Input B	A14, T18	A14	A14
EQEP0_INDEX	IO	EQEP Index	D11, N18	D11, N18	D11, N18
EQEP0_STROBE	IO	EQEP Strobe	C12, M18	C12, M18	C12, M18

Table 5-55. EQEP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EQEP1_A	I	EQEP Quadrature Input A	D15, P16	D15, P16	D15, P16
EQEP1_B	I	EQEP Quadrature Input B	C15, P17	C15	C15
EQEP1_INDEX	IO	EQEP Index	N17, P2	P2	P2
EQEP1_STROBE	IO	EQEP Strobe	B16, P18	B16	B16

Table 5-56. EQEP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EQEP2_A (1)	I	EQEP Quadrature Input A	B13, R17	B13, R17	B13, R17
EQEP2_B (2)	ID	EQEP Quadrature Input B	A13, R18	A13	A13
EQEP2_INDEX	IO	EQEP Index	A12, T17	A12	A12
EQEP2_STROBE	IO	EQEP Strobe	B12, U17	B12	B12

(1) EQEP2_A is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(2) EQEP2_B is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

5.3.10 FSI

Table 5-57. FSIRX0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSIRX0_CLK	I	FSI Clock	A10, T17	A10	A10
FSIRX0_DATA0	I	FSI Data 0	B10, U18	B10	B10
FSIRX0_DATA1	I	FSI Data 1	D9, T18	D9	D9

Table 5-58. FSIRX1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSIRX1_CLK	I	FSI Clock	E1, P17	E1	E1
FSIRX1_DATA0	I	FSI Data 0	F3, P18	F3	F3
FSIRX1_DATA1	I	FSI Data 1	F4, N17	F4	F4

Table 5-59. FSIRX2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSIRX2_CLK	I	FSI Clock	G16, J2	G16, J2	G16, J2
FSIRX2_DATA0	I	FSI Data 0	E17, G4	E17, G4	E17, G4
FSIRX2_DATA1	I	FSI Data 1	E18, J3, R3	E18, J3, R3	E18, R3

Table 5-60. FSIRX3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSIRX3_CLK	I	FSI Clock	B17	B17	B17
FSIRX3_DATA0	I	FSI Data 0	D16	D16	D16
FSIRX3_DATA1	I	FSI Data 1	C17	C17	C17

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Table 5-61. FSITX0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSITX0_CLK	O	FSI Clock	A11, R17	A11, R17	A11, R17
FSITX0_DATA0	O	FSI Data 0	C10, R18	C10	C10
FSITX0_DATA1	O	FSI Data 1	B11, U17	B11	B11

Table 5-62. FSITX1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSITX1_CLK	O	FSI Clock	E4, N18	E4, N18	E4, N18
FSITX1_DATA0	O	FSI Data 0	F2, M18	F2, M18	F2, M18
FSITX1_DATA1	O	FSI Data 1	G2, P16	G2, P16	G2, P16

Table 5-63. FSITX2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSITX2_CLK	O	FSI Clock	E16, G3	E16, G3	E16, G3
FSITX2_DATA0	O	FSI Data 0	F16, H2	F16, H2	F16, H2
FSITX2_DATA1	O	FSI Data 1	F18, G1	F18, G1	F18, G1

Table 5-64. FSITX3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
FSITX3_CLK	O	FSI Clock	C16	C16	C16
FSITX3_DATA0	O	FSI Data 0	A17	A17	A17
FSITX3_DATA1	O	FSI Data 1	B18	B18	B18

5.3.11 GPIO

Table 5-65. GPIO Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
GPIO0	IO	General Purpose Input/Output	P1	P1	P1
GPIO1	IO	General Purpose Input/Output	R3	R3	R3
GPIO2	IO	General Purpose Input/Output	N2	N2	N2
GPIO3	IO	General Purpose Input/Output	N1	N1	N1
GPIO4	IO	General Purpose Input/Output	N4	N4	N4
GPIO5	IO	General Purpose Input/Output	M4	M4	M4
GPIO6	IO	General Purpose Input/Output	P3	P3	P3
GPIO7	IO	General Purpose Input/Output	M1	M1	M1
GPIO8	IO	General Purpose Input/Output	L1	L1	L1
GPIO9	IO	General Purpose Input/Output	L2	L2	L2
GPIO10	IO	General Purpose Input/Output	K1	K1	K1
GPIO11	IO	General Purpose Input/Output	C11	C11	C11
GPIO12	IO	General Purpose Input/Output	A11	A11	A11
GPIO13	IO	General Purpose Input/Output	C10	C10	C10
GPIO14	IO	General Purpose Input/Output	B11	B11	B11
GPIO15	IO	General Purpose Input/Output	C9	C9	C9
GPIO16	IO	General Purpose Input/Output	A10	A10	A10
GPIO17	IO	General Purpose Input/Output	B10	B10	B10
GPIO18	IO	General Purpose Input/Output	D9	D9	D9
GPIO19	IO	General Purpose Input/Output	A9	A9	A9
GPIO100	IO	General Purpose Input/Output	M15	M15	M15
GPIO101	IO	General Purpose Input/Output	H17	H17	H17
GPIO102	IO	General Purpose Input/Output	H16	H16	H16
GPIO103	IO	General Purpose Input/Output	F15	F15	F15

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Table 5-65. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
GPIO104	IO	General Purpose Input/Output	C18	C18	C18
GPIO105	IO	General Purpose Input/Output	D17	D17	D17
GPIO106	IO	General Purpose Input/Output	D18	D18	D18
GPIO107	IO	General Purpose Input/Output	E16	E16	E16
GPIO108	IO	General Purpose Input/Output	F16	F16	F16
GPIO109	IO	General Purpose Input/Output	F18	F18	F18
GPIO110	IO	General Purpose Input/Output	G16	G16	G16
GPIO111	IO	General Purpose Input/Output	E17	E17	E17
GPIO112	IO	General Purpose Input/Output	E18	E18	E18
GPIO113	IO	General Purpose Input/Output	C16	C16	C16
GPIO114	IO	General Purpose Input/Output	A17	A17	A17
GPIO115	IO	General Purpose Input/Output	B18	B18	B18
GPIO116	IO	General Purpose Input/Output	B17	B17	B17
GPIO117	IO	General Purpose Input/Output	D16	D16	D16
GPIO118	IO	General Purpose Input/Output	C17	C17	C17
GPIO119	IO	General Purpose Input/Output	D15	D15	D15
GPIO120	IO	General Purpose Input/Output	C15	C15	C15
GPIO121	IO	General Purpose Input/Output	P2	P2	P2
GPIO122	IO	General Purpose Input/Output	B16	B16	B16
GPIO123	IO	General Purpose Input/Output	D14	D14	D14
GPIO124	IO	General Purpose Input/Output	A16	A16	A16
GPIO125	IO	General Purpose Input/Output	D13	D13	D13
GPIO126	IO	General Purpose Input/Output	B15	B15	B15
GPIO127	IO	General Purpose Input/Output	C13	C13	C13
GPIO128	IO	General Purpose Input/Output	A15	A15	A15
GPIO129	IO	General Purpose Input/Output	C14	C14	C14
GPIO130	IO	General Purpose Input/Output	B14	B14	B14
GPIO131	IO	General Purpose Input/Output	A14	A14	A14
GPIO132	IO	General Purpose Input/Output	C12	C12	C12
GPIO133	IO	General Purpose Input/Output	D11	D11	D11
GPIO134 (2)	IOD	General Purpose Input/Output	B13	B13	B13
GPIO135 (3)	IOD	General Purpose Input/Output	A13	A13	A13
GPIO136	IO	General Purpose Input/Output	B12	B12	B12
GPIO137	IO	General Purpose Input/Output	A12	A12	A12
GPIO138	IO	General Purpose Input/Output	M2	M2	M2
GPIO20	IO	General Purpose Input/Output	B9	B9	B9
GPIO21	IO	General Purpose Input/Output	B8	B8	B8
GPIO22	IO	General Purpose Input/Output	A8	A8	A8
GPIO23	IO	General Purpose Input/Output	D7	D7	D7
GPIO24	IO	General Purpose Input/Output	C8	C8	C8
GPIO25	IO	General Purpose Input/Output	C7	C7	C7
GPIO26	IO	General Purpose Input/Output	B7	B7	B7
GPIO27	IO	General Purpose Input/Output	A7	A7	A7
GPIO28	IO	General Purpose Input/Output	A6	A6	A6
GPIO29	IO	General Purpose Input/Output	R17	R17	R17
GPIO30 (1)	IO	General Purpose Input/Output	R18		
GPIO31 (1)	IO	General Purpose Input/Output	U17		
GPIO32 (1)	IO	General Purpose Input/Output	T17		
GPIO33 (1)	IO	General Purpose Input/Output	U18		
GPIO34 (1)	IO	General Purpose Input/Output	T18		

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Table 5-65. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
GPIO35	IO	General Purpose Input/Output	N18	N18	N18
GPIO36	IO	General Purpose Input/Output	M18	M18	M18
GPIO37	IO	General Purpose Input/Output	P16	P16	P16
GPIO38 (1)	IO	General Purpose Input/Output	P17		
GPIO39 (1)	IO	General Purpose Input/Output	P18		
GPIO40 (1)	IO	General Purpose Input/Output	N17		
GPIO41	IO	General Purpose Input/Output	N16	N16	N16
GPIO42	IO	General Purpose Input/Output	M17	M17	M17
GPIO43	IO	General Purpose Input/Output	B2	B2	B2
GPIO44	IO	General Purpose Input/Output	B1	B1	B1
GPIO45	IO	General Purpose Input/Output	D3	D3	D3
GPIO46	IO	General Purpose Input/Output	D2	D2	D2
GPIO47	IO	General Purpose Input/Output	C2	C2	C2
GPIO48	IO	General Purpose Input/Output	C1	C1	C1
GPIO49	IO	General Purpose Input/Output	E2	E2	E2
GPIO50	IO	General Purpose Input/Output	E3	E3	E3
GPIO51	IO	General Purpose Input/Output	D1	D1	D1
GPIO52	IO	General Purpose Input/Output	E4	E4	E4
GPIO53	IO	General Purpose Input/Output	F2	F2	F2
GPIO54	IO	General Purpose Input/Output	G2	G2	G2
GPIO55	IO	General Purpose Input/Output	E1	E1	E1
GPIO56	IO	General Purpose Input/Output	F3	F3	F3
GPIO57	IO	General Purpose Input/Output	F4	F4	F4
GPIO58	IO	General Purpose Input/Output	F1	F1	F1
GPIO59	IO	General Purpose Input/Output	G3	G3	G3
GPIO60	IO	General Purpose Input/Output	H2	H2	H2
GPIO61	IO	General Purpose Input/Output	G1	G1	G1
GPIO62	IO	General Purpose Input/Output	J2	J2	J2
GPIO63	IO	General Purpose Input/Output	G4	G4	G4
GPIO64	IO	General Purpose Input/Output	J3	J3	J3
GPIO65	IO	General Purpose Input/Output	H1	H1	H1
GPIO66	IO	General Purpose Input/Output	J1	J1	J1
GPIO67	IO	General Purpose Input/Output	K2	K2	K2
GPIO68	IO	General Purpose Input/Output	J4	J4	J4
GPIO69	IO	General Purpose Input/Output	K4	K4	K4
GPIO70	IO	General Purpose Input/Output	K3	K3	K3
GPIO71 (1)	IO	General Purpose Input/Output	V17		
GPIO72 (1)	IO	General Purpose Input/Output	T16		
GPIO73 (1)	IO	General Purpose Input/Output	P15		
GPIO74 (1)	IO	General Purpose Input/Output	R16		
GPIO75	IO	General Purpose Input/Output	L3	L3	L3
GPIO76	IO	General Purpose Input/Output	M3	M3	M3
GPIO77	IO	General Purpose Input/Output	B6	B6	B6
GPIO78	IO	General Purpose Input/Output	A4	A4	A4
GPIO79	IO	General Purpose Input/Output	B5	B5	B5
GPIO80	IO	General Purpose Input/Output	B4	B4	B4
GPIO81	IO	General Purpose Input/Output	A3	A3	A3
GPIO82	IO	General Purpose Input/Output	A2	A2	A2
GPIO83	IO	General Purpose Input/Output	C6	C6	C6
GPIO84	IO	General Purpose Input/Output	A5	A5	A5

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Table 5-65. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
GPIO85	IO	General Purpose Input/Output	L17	L17	L17
GPIO86	IO	General Purpose Input/Output	L18	L18	L18
GPIO87	IO	General Purpose Input/Output	G17	G17	G17
GPIO88	IO	General Purpose Input/Output	F17	F17	F17
GPIO89	IO	General Purpose Input/Output	G18	G18	G18
GPIO90	IO	General Purpose Input/Output	G15	G15	G15
GPIO91	IO	General Purpose Input/Output	K15	K15	K15
GPIO92	IO	General Purpose Input/Output	K16	K16	K16
GPIO93	IO	General Purpose Input/Output	K17	K17	K17
GPIO94	IO	General Purpose Input/Output	K18	K18	K18
GPIO95	IO	General Purpose Input/Output	J18	J18	J18
GPIO96	IO	General Purpose Input/Output	J17	J17	J17
GPIO97	IO	General Purpose Input/Output	H18	H18	H18
GPIO98	IO	General Purpose Input/Output	L16	L16	L16
GPIO99	IO	General Purpose Input/Output	M16	M16	M16

(1) This pin is is only supported in the ZCZ_C package option
(2) GPIO134 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(3) GPIO135 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

5.3.12 I2C

Table 5-66. I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
I2C0_SCL (2)	IOD	I2C Clock	A13	A13	A13
I2C0_SDA (1)	IOD	I2C Data	B13	B13	B13

(1) I2C0_SDA is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(2) I2C0_SCL is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

Table 5-67. I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
I2C1_SCL (1)	IO	I2C Clock	B5, D7	B5, D7	B5, D7
I2C1_SDA (2)	IO	I2C Data	A3, C8	A3, C8	A3, C8

(1) I2C1_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.
(2) I2C1_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

Table 5-68. I2C2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
I2C2_SCL (1)	IO	I2C Clock	C6, C7	C6, C7	C6, C7
I2C2_SDA (2)	IO	I2C Data	A5, B7	A5, B7	A5, B7

(1) I2C2_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.
(2) I2C2_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

Table 5-69. I2C3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
I2C3_SCL (2)	IO	I2C Clock	B15, H2	B15, H2	B15, H2
I2C3_SDA (1)	IO	I2C Data	A16, G3	A16, G3	A16, G3

(1) I2C3_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

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(2) I2C3_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

Note

I2C signals that are implemented on an LVCMOS voltage buffer pin can be configured to operate as open-drain outputs by configuring the I2C module to source a constant low output and toggle the output enable. The output buffer drives low when enabled and is high impedance when disabled.

The (I2C OD FS) are the only IO voltage buffers which are fail-safe. These are implemented for I2C0 pins only. Other IOs do not allow any potential greater than (VDD + 0.3V) to be applied. This means you can not source any potential to these pins when power is off. All attached devices that can source a potential to these IOs must be powered from the same power supply that is sourcing the respective IO power rail.

5.3.13 LIN

Table 5-70. LIN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
LIN0_RXD	IO	LIN Receive Data	A7, B6	A7, B6	A7, B6
LIN0_TXD	IO	LIN Transmit Data	A4, A6	A4, A6	A4, A6

Table 5-71. LIN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
LIN1_RXD	IO	LIN Receive Data	A9, L3	A9, L3	A9, L3
LIN1_TXD	IO	LIN Transmit Data	B9, M3	B9, M3	B9, M3

Table 5-72. LIN2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
LIN2_RXD	IO	LIN Receive Data	B8	B8	B8
LIN2_TXD	IO	LIN Transmit Data	A8	A8	A8

Table 5-73. LIN3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
LIN3_RXD	IO	LIN Receive Data	C11	C11	C11
LIN3_TXD	IO	LIN Transmit Data	A11	A11	A11

Table 5-74. LIN4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
LIN4_RXD	IO	LIN Receive Data	A10, D11	A10, D11	A10, D11
LIN4_TXD	IO	LIN Transmit Data	C12, C9	C12, C9	C12, C9

5.3.14 MCAN

Table 5-75. MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN0_RX	I	MCAN Receive Data	B6, E16, M1	B6, E16, M1	B6, E16
MCAN0_TX	O	MCAN Transmit Data	A4, F16, L1	A4, F16, L1	A4, F16

Table 5-76. MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN1_RX	I	MCAN Receive Data	B5, F18, L2	B5, F18, L2	B5, F18
MCAN1_TX	O	MCAN Transmit Data	B4, G16, K1	B4, G16, K1	B4, G16, K1

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Table 5-77. MCAN2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN2_RX	I	MCAN Receive Data	A12	A12	A12
MCAN2_TX	O	MCAN Transmit Data	B12	B12	B12

Table 5-78. MCAN3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN3_RX	I	MCAN Receive Data	B7, C14	B7, C14	B7, C14
MCAN3_TX	O	MCAN Transmit Data	A15, C7	A15, C7	A15, C7

Table 5-79. MCAN4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN4_RX	I	MCAN Receive Data	A3, E17, G1	A3, E17, G1	A3, E17, G1
MCAN4_TX	O	MCAN Transmit Data	A2, E18, J2	A2, E18, J2	A2, E18, J2

Table 5-80. MCAN5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN5_RX	I	MCAN Receive Data	C16, C6, G4	C16, C6, G4	C16, C6, G4
MCAN5_TX	O	MCAN Transmit Data	A17, A5, J3, R3	A17, A5, J3, R3	A17, A5, R3

Table 5-81. MCAN6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN6_RX	I	MCAN Receive Data	B18, H1, V17	B18, H1	B18
MCAN6_TX	O	MCAN Transmit Data	B17, J1, T16	B17, J1	B17

Table 5-82. MCAN7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MCAN7_RX	I	MCAN Receive Data	D16, K2, N2, P15	D16, K2, N2	D16, N2
MCAN7_TX	O	MCAN Transmit Data	C17, J4, N1, R16	C17, J4, N1	C17, N1

5.3.15 SPI (MCSPI)

Table 5-83. SPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI0_CLK (1)	IO	SPI Clock (SOP2)	A11	A11	A11
SPI0_CS0	IO	SPI Chip Select 0	C11	C11	C11
SPI0_CS1	IO	SPI Chip Select 1	B7	B7	B7
SPI0_D0 (2)	IO	SPI Data 0 (SOP3)	C10	C10	C10
SPI0_D1	IO	SPI Data 1	B11	B11	B11

(1) The SPI0_CLK pin is also used as SOP2 bootmode configuration pin.
(2) The SPI0_D0 pin is also used as SOP3 bootmode configuration pin.

Table 5-84. SPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI1_CLK	IO	SPI Clock	A10	A10	A10
SPI1_CS0	IO	SPI Chip Select 0	C9	C9	C9
SPI1_D0	IO	SPI Data 0	B10	B10	B10
SPI1_D1	IO	SPI Data 1	D9	D9	D9

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Table 5-85. SPI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI2_CLK	IO	SPI Clock	B9	B9	B9
SPI2_CS0	IO	SPI Chip Select 0	A9	A9	A9
SPI2_D0	IO	SPI Data 0	B8	B8	B8
SPI2_D1	IO	SPI Data 1	A8	A8	A8

Table 5-86. SPI3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI3_CLK	IO	SPI Clock	C8	C8	C8
SPI3_CS0	IO	SPI Chip Select 0	D7	D7	D7
SPI3_D0	IO	SPI Data 0	C7	C7	C7
SPI3_D1	IO	SPI Data 1	B7	B7	B7

Table 5-87. SPI4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI4_CLK	IO	SPI Clock	B14, L1	B14, L1	B14
SPI4_CS0	IO	SPI Chip Select 0	A14, M1	A14, M1	A14
SPI4_CS1	IO	SPI Chip Select 1	K2, R3	K2, R3	R3
SPI4_D0	IO	SPI Data 0	C12, L2	C12, L2	C12
SPI4_D1	IO	SPI Data 1	D11, K1	D11, K1	D11, K1

Table 5-88. SPI5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI5_CLK	IO	SPI Clock	C18, G2	C18, G2	C18, G2
SPI5_CS0	IO	SPI Chip Select 0	F15, F2	F15, F2	F15, F2
SPI5_D0	IO	SPI Data 0	D17, E1	D17, E1	D17, E1
SPI5_D1	IO	SPI Data 1	D18, F3	D18, F3	D18, F3

Table 5-89. SPI6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI6_CLK	IO	SPI Clock	B17, F1	B17, F1	B17, F1
SPI6_CS0	IO	SPI Chip Select 0	B18, F4	B18, F4	B18, F4
SPI6_D0	IO	SPI Data 0	D16, G3	D16, G3	D16, G3
SPI6_D1	IO	SPI Data 1	C17, H2	C17, H2	C17, H2

Table 5-90. SPI7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SPI7_CLK	IO	SPI Clock	J2, K4, N1	J2, K4, N1	J2, N1
SPI7_CS0	IO	SPI Chip Select 0	G1, J4, N2	G1, J4, N2	G1, N2
SPI7_D0	IO	SPI Data 0	G4, K3, N4	G4, K3, N4	G4, N4
SPI7_D1	IO	SPI Data 1	J3, K1, V17	J3, K1	K1

5.3.16 MMC

Table 5-91. MMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MMC0_CD	I	MMC/SD Card Detect	A5	A5	A5
MMC0_CLK	IO	MMC/SD Clock	B6	B6	B6
MMC0_CMD	IO	MMC/SD Command	A4	A4	A4
MMC0_WP	I	MMC/SD Write Protect	C6	C6	C6
MMC0_D0	IO	MMC/SD Data	B5	B5	B5

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Table 5-91. MMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
MMC0_D1	IO	MMC/SD Data	B4	B4	B4
MMC0_D2	IO	MMC/SD Data	A3	A3	A3
MMC0_D3	IO	MMC/SD Data	A2	A2	A2

5.3.17 OSPI (Shared)

Table 5-92. OSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
OSPI0_CLK	O	OSPI Clock	L2, N2	L2, N2	L2
OSPI0_CLKLB (2)	IO	OSPI Clock Loopback	LB	LB	LB
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock input	M1, M3	M1, M3	M1
OSPI0_ECC_FAIL	I	OSPI ECC Failure Status Pin	A9, H1, K3	A9, H1, K3	K3
OSPI0_LBCLKO (1)	O	OSPI Loopback Clock output	L3	L3	
OSPI0_CSn0	O	OSPI Chip Select 0	H1, P1	H1, P1	H1
OSPI0_CSn1	O	OSPI Chip Select 1	R3	R3	
OSPI0_D0	IO	OSPI Data bit 0 (SOP0)	N1, P1	N1, P1	P1
OSPI0_D1	IO	OSPI Data bit 1 (SOP1)	J1, N4	J1, N4	J1
OSPI0_D2	IO	OSPI Data bit 2	L1, M4	L1, M4	L1
OSPI0_D3	IO	OSPI Data bit 3	K4, P3	K4, P3	K4
OSPI0_D4	IO	OSPI Data bit 4	M1, P3	M1, P3	P3
OSPI0_D5	IO	OSPI Data bit 5	K2, L1	K2, L1	K2
OSPI0_D6	IO	OSPI Data bit 6	L2, M4	L2, M4	M4
OSPI0_D7	IO	OSPI Data bit 7	J4, K1	J4, K1	J4
OSPI0_RESET_OUT0	O	OSPI Reset Out 0	B9, J1, J3	B9, J1, J3	J3
OSPI0_RESET_OUT1	O	OSPI Reset Out 1	A9, H1	A9, H1	

(1) OSPI0_LBCLKO is a clock loopback output signal used for peripheral timing.
(2) OSPI0_CLKLB is a clock loopback signal used internally for retiming purposes.

5.3.18 Power Supply

Table 5-93. Power Supply Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
VDD	PWR	1.2V Core supply	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6, R9	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6, R9	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6, R9
VDDA18	PWR	1.8V Analog supply	R11, R8	R11, R8	R11, R8
VDDA18_LDO (1) (2)	PWR	1.8V Analog LDO Output	R6	R6	R6
VDDA18_OSC_PLL	PWR	1.8V OSC PLL supply	R4	R4	R4
VDDA33	PWR	3.3V Analog supply	P11, P7, P9	P11, P7, P9	P11, P7, P9
VDDAR1	PWR	1.2V SRAM Array supply	J15	J15	J15
VDDAR2	PWR	1.2V SRAM Array supply	D10	D10	D10
VDDAR3	PWR	1.2V SRAM Array supply	H3	H3	H3
VDDS18	PWR	1.8V IO supply	D6, E15, L4, N15	D6, E15, L4, N15	D6, E15, L4, N15
VDDS18_LDO (1) (3)	PWR	1.8V Digital LDO Output	T3	T3	T3
VDDS33	PWR	3.3V IO supply	D12, D8, H15, H4, L15, P4, R15	D12, D8, H15, H4, L15, P4, R15	D12, D8, H15, H4, L15, P4, R15
VPP	PWR	eFuse ROM programming supply	N3	N3	N3

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Table 5-93. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
VSS	GND	Ground	A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2, V18	A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2	A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2
VSSA	AGND	Analog Ground	P10, P12, P6, P8, R13, R5, V1, V16	P10, P12, P6, P8, R13, R5, V1, V18	P10, P12, P6, P8, R13, R5, V1, V18

(1) See the *Layout Guidelines* sections for details on connecting this pin.
(2) PCB should directly route VDDA18_LDO to all of the VDDA18 pins and the VDDA_OSC_PLL pin.
(3) PCB should directly route VDDS18_LDO to all of the VDDS18 pins.

5.3.19 PRU-ICSS

Table 5-94. PRU-ICSS ECAP Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PR0_ECAP0_APWM_OUT	O	PRU-ICSS Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	D14	D14	D14

Table 5-95. PRU-ICSS GPIO Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PR0_PRU0_GPIO0	IO	PRU0 General Purpose Input/Output	K17	K17	K17
PR0_PRU0_GPIO1	IO	PRU0 General Purpose Input/Output	K18	K18	K18
PR0_PRU0_GPIO2	IO	PRU0 General Purpose Input/Output	J18	J18	J18
PR0_PRU0_GPIO3	IO	PRU0 General Purpose Input/Output	J17	J17	J17
PR0_PRU0_GPIO4	IO	PRU0 General Purpose Input/Output	K16	K16	K16
PR0_PRU0_GPIO5	IO	PRU0 General Purpose Input/Output	G17	G17	G17
PR0_PRU0_GPIO6	IO	PRU0 General Purpose Input/Output	K15	K15	K15
PR0_PRU0_GPIO8	IO	PRU0 General Purpose Input/Output	G15	G15	G15
PR0_PRU0_GPIO9	IO	PRU0 General Purpose Input/Output	F17	F17	F17
PR0_PRU0_GPIO10	IO	PRU0 General Purpose Input/Output	G18	G18	G18
PR0_PRU0_GPIO11	IO	PRU0 General Purpose Input/Output	M16	M16	M16
PR0_PRU0_GPIO12	IO	PRU0 General Purpose Input/Output	M15	M15	M15
PR0_PRU0_GPIO13	IO	PRU0 General Purpose Input/Output	H17	H17	H17
PR0_PRU0_GPIO14	IO	PRU0 General Purpose Input/Output	H16	H16	H16
PR0_PRU0_GPIO15	IO	PRU0 General Purpose Input/Output	L16	L16	L16
PR0_PRU0_GPIO16	IO	PRU0 General Purpose Input/Output	H18	H18	H18
PR0_PRU1_GPIO0	IO	PRU1 General Purpose Input/Output	F18	F18	F18
PR0_PRU1_GPIO1	IO	PRU1 General Purpose Input/Output	G16	G16	G16

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Table 5-95. PRU-ICSS GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PR0_PRU1_GPIO2	IO	PRU1 General Purpose Input/Output	E17	E17	E17
PR0_PRU1_GPIO3	IO	PRU1 General Purpose Input/Output	E18	E18	E18
PR0_PRU1_GPIO4	IO	PRU1 General Purpose Input/Output	F16	F16	F16
PR0_PRU1_GPIO5	IO	PRU1 General Purpose Input/Output	F15	F15	F15
PR0_PRU1_GPIO6	IO	PRU1 General Purpose Input/Output	E16	E16	E16
PR0_PRU1_GPIO7	IO	PRU1 General Purpose Input/Output	A16	A16	A16
PR0_PRU1_GPIO8	IO	PRU1 General Purpose Input/Output	D18	D18	D18
PR0_PRU1_GPIO9	IO	PRU1 General Purpose Input/Output	C18	C18	C18
PR0_PRU1_GPIO10	IO	PRU1 General Purpose Input/Output	D17	D17	D17
PR0_PRU1_GPIO11	IO	PRU1 General Purpose Input/Output	B18	B18	B18
PR0_PRU1_GPIO12	IO	PRU1 General Purpose Input/Output	B17	B17	B17
PR0_PRU1_GPIO13	IO	PRU1 General Purpose Input/Output	D16	D16	D16
PR0_PRU1_GPIO14	IO	PRU1 General Purpose Input/Output	C17	C17	C17
PR0_PRU1_GPIO15	IO	PRU1 General Purpose Input/Output	A17	A17	A17
PR0_PRU1_GPIO16	IO	PRU1 General Purpose Input/Output	C16	C16	C16
PR0_PRU1_GPIO17	IO	PRU1 General Purpose Input/Output	D13	D13	D13
PR0_PRU1_GPIO18	IO	PRU1 General Purpose Input/Output	C15	C15	C15
PR0_PRU1_GPIO19	IO	PRU1 General Purpose Input/Output	D15	D15	D15

Table 5-96. PRU-ICSS IEP Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PR0_IEP0_EDC_SYNC_OUT0	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	D15	D15	D15
PR0_IEP0_EDC_SYNC_OUT1	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	A16	A16	A16
PR0_IEP0_EDIO_DATA_IN_OUT30	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/ Output	D13	D13	D13
PR0_IEP0_EDIO_DATA_IN_OUT31	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/ Output	C15	C15	C15

Table 5-97. PRU-ICSS MDIO Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PR0_MDIO0_MDC	O	PRU-ICSS MDIO Clock	L18	L18	L18
PR0_MDIO0_MDIO	IO	PRU-ICSS MDIO Data	L17	L17	L17

Table 5-98. PRU-ICSS UART Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PR0_UART0_CTSn	I	PRU-ICSS UART Clear to Send (Active Low)	F17	F17	F17
PR0_UART0_RTSn	O	PRU-ICSS UART Request to Send (Active Low)	G18	G18	G18
PR0_UART0_RXD	I	PRU-ICSS UART Receive Data	C18	C18	C18
PR0_UART0_TXD	O	PRU-ICSS UART Transmit Data	D17	D17	D17

5.3.20 SDFM

Table 5-99. SDFM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SDFM0_CLK0	I	SDFM Channel 0 Clock	B16	B16	B16
SDFM0_CLK1	I	SDFM Channel 1 Clock	A16	A16	A16
SDFM0_CLK2	I	SDFM Channel 2 Clock	B15	B15	B15
SDFM0_CLK3	I	SDFM Channel 3 Clock	A15	A15	A15
SDFM0_D0	I	SDFM Channel 0 Data	D14	D14	D14

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Table 5-99. SDFM0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SDFM0_D1	I	SDFM Channel 1 Data	D13	D13	D13
SDFM0_D2	I	SDFM Channel 2 Data	C13	C13	C13
SDFM0_D3	I	SDFM Channel 3 Data	C14	C14	C14

Table 5-100. SDFM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SDFM1_CLK0	I	SDFM Channel 0 Clock	B14, B6	B14, B6	B14, B6
SDFM1_CLK1	I	SDFM Channel 1 Clock	B5, C12	B5, C12	B5, C12
SDFM1_CLK2 (1)	I	SDFM Channel 2 Clock	A3, B13	A3, B13	A3, B13
SDFM1_CLK3 (2)	ID	SDFM Channel 3 Clock	A13, C6	A13, C6	A13, C6
SDFM1_D0	I	SDFM Channel 0 Data	A14, A4	A14, A4	A14, A4
SDFM1_D1	I	SDFM Channel 1 Data	B4, D11	B4, D11	B4, D11
SDFM1_D2	I	SDFM Channel 2 Data	A2, B12	A2, B12	A2, B12
SDFM1_D3	I	SDFM Channel 3 Data	A12, A5	A12, A5	A12, A5

(1) SDFM1_CLK2 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(2) SDFM1_CLK3 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

5.3.21 System and Miscellaneous

5.3.21.1 Boot Mode Configuration

Table 5-101. Boot Mode Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
SOP0		Boot Mode configuration bit 0 (OSPI0_D0)	N1	N1	N1
SOP1		Boot Mode configuration bit 1 (OSPI0_D1)	N4	N4	N4
SOP2	IO	Boot Mode configuration bit 2 (SPI0_CLK)	A11	A11	A11
SOP3	IO	Boot Mode configuration bit 3 (SPI0_D0)	C10	C10	C10

5.3.21.2 Clocking

Table 5-102. XTAL Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
XTAL_XI (1)	I	External Crystal (XTAL) Input	T1	T1	T1
XTAL_XO (1)	O	External Crystal (XTAL) Output	R1	R1	R1

(1) The XTAL interface requires a 25 MHz clock source.

Table 5-103. Output Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
CLKOUT0	O	Output Clock 0	M2	M2	M2
CLKOUT1	O	Output Clock 1	B16	B16	B16

Table 5-104. External Reference Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
EXT_REFCLK0	I	External Reference Clock Input	P2	P2	P2

5.3.21.3 Emulation and Debug

Table 5-105. Trace Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
TRC_CLK	O	Trace Clock	D15	D15	D15
TRC_CTL	O	Trace Control	C15	C15	C15
TRC_DATA0	O	Trace Data 0	F15	F15	F15
TRC_DATA1	O	Trace Data 1	C18	C18	C18

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Table 5-105. Trace Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
TRC_DATA2	O	Trace Data 2	D17	D17	D17
TRC_DATA3	O	Trace Data 3	D18	D18	D18
TRC_DATA4	O	Trace Data 4	E16	E16	E16
TRC_DATA5	O	Trace Data 5	F16	F16	F16
TRC_DATA6	O	Trace Data 6	F18	F18	F18
TRC_DATA7	O	Trace Data 7	G16	G16	G16
TRC_DATA8	O	Trace Data 8	E17	E17	E17
TRC_DATA9	O	Trace Data 9	E18	E18	E18
TRC_DATA10	O	Trace Data 10	C16	C16	C16
TRC_DATA11	O	Trace Data 11	A17	A17	A17
TRC_DATA12	O	Trace Data 12	B18	B18	B18
TRC_DATA13	O	Trace Data 13	B17	B17	B17
TRC_DATA14	O	Trace Data 14	D16	D16	D16
TRC_DATA15	O	Trace Data 15	C17	C17	C17

Table 5-106. JTAG Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
TCK	I	JTAG Test Clock Input	B3	B3	B3
TDI	I	JTAG Test Data Input	C5	C5	C5
TDO	O	JTAG Test Data Output	C4	C4	C4
TMS	IO	JTAG Test Mode Select Input	D5	D5	D5

5.3.21.4 SYSTEM

Table 5-107. System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
PORz	I	Device Power-On (PORz) cold reset	R2	R2	R2
SAFETY_ERRORn	IO	ESM Safety Error Signal	D4	D4	D4
WARMRSTn	IO	Warm Reset Request (Input) / Warm Reset Status (Output)	C3	C3	C3

5.3.21.5 VMON

Table 5-108. VMON Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
VSYS_MON (1)	A	External Voltage Monitor with 0.9 V (+/-3%) setpoint.	U2	U2	U2

(1) See the *Electrical Specifications - Safety Comparators* section for additional details on this pin.

5.3.21.6 Reserved

Table 5-109. Reserved Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RSVD_J16	RSVD	Reserved (RSVD_J16). This pin must be connected to 1.2 V supply (VDD).	J16	J16	J16
RSVD_P15	RSVD	Reserved (RSVD_P15). This pin must be left unconnected.		P15	P15
RSVD_T4	RSVD	Reserved (RSVD_T4). This pin must be connected to ground (VSS).	T4	T4	T4
RSVD_U1	RSVD	Reserved (RSVD_U1). This pin must be connected to ground (VSS).	U1	U1	U1
RSVD_U3	RSVD	Reserved (RSVD_U3). This pin must be left unconnected.	U3	U3	U3

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Table 5-109. Reserved Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
RSVD_V2	RSVD	Reserved (RSVD_V2). This pin must be left unconnected.	V2	V2	V2

5.3.22 UART

Table 5-110. UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	A5, B7	A5, B7	A5, B7
UART0_RTSn	O	UART Request to Send (active low)	C6, C7	C6, C7	C6, C7
UART0_RXD	I	UART Receive Data	A7, B6	A7, B6	A7, B6
UART0_TXD	O	UART Transmit Data	A4, A6	A4, A6	A4, A6

Table 5-111. UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	G4	G4	G4
UART1_DCDn	I	UART Data Carrier Detect (Active Low)	J4, N1	J4, N1	N1
UART1_DSRn	I	UART Data Set Ready (Active Low)	V17		
UART1_DTRn	O	UART Data Terminal Ready (Active Low)	K1, K3	K1, K3	K1
UART1_RIn	I	UART Ring Indicator	K4, N4	K4, N4	N4
UART1_RTSn	O	UART Request to Send (active low)	B12, J2	B12, J2	B12, J2
UART1_RXD	I	UART Receive Data	A9, L3	A9, L3	A9, L3
UART1_TXD	O	UART Transmit Data	B9, M3	B9, M3	B9, M3

Table 5-112. UART2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	H1	H1	
UART2_RTSn	O	UART Request to Send (active low)	A12, J3, R3	A12, J3, R3	A12, R3
UART2_RXD	I	UART Receive Data	B5, B8	B5, B8	B5, B8
UART2_TXD	O	UART Transmit Data	A3, A8	A3, A8	A3, A8

Table 5-113. UART3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	K2, N2	K2, N2	N2
UART3_RTSn	O	UART Request to Send (active low)	A2, J1	A2, J1	A2
UART3_RXD	I	UART Receive Data	C11, D15	C11, D15	C11, D15
UART3_TXD	O	UART Transmit Data	A11, C15	A11, C15	A11, C15

Table 5-114. UART4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	A14	A14	A14
UART4_RTSn	O	UART Request to Send (active low)	B14	B14	B14
UART4_RXD	I	UART Receive Data	A10, D11, H2	A10, D11, H2	A10, D11, H2
UART4_TXD	O	UART Transmit Data	C12, C9, G3	C12, C9, G3	C12, C9, G3

Table 5-115. UART5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	D13	D13	D13
UART5_RTSn	O	UART Request to Send (active low)	A16	A16	A16
UART5_RXD	I	UART Receive Data	A15, C13, D9, R16	A15, C13, D9	A15, C13, D9

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Table 5-115. UART5 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
UART5_TXD	O	UART Transmit Data	B10, B15, P15	B10, B15	B10, B15

5.3.23 XBAR

Table 5-116. Output XBAR Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
XBAROUT0	O	OUTPUTXBAR Signal 0	R3	R3	R3
XBAROUT1	O	OUTPUTXBAR Signal 1	C9	C9	C9
XBAROUT2	O	OUTPUTXBAR Signal 2	A10	A10	A10
XBAROUT3	O	OUTPUTXBAR Signal 3	B10	B10	B10
XBAROUT4	O	OUTPUTXBAR Signal 4	D9	D9	D9
XBAROUT5	O	OUTPUTXBAR Signal 5	A9	A9	A9
XBAROUT6	O	OUTPUTXBAR Signal 6	B9	B9	B9
XBAROUT7	O	OUTPUTXBAR Signal 7	D7	D7	D7
XBAROUT8	O	OUTPUTXBAR Signal 8	C8	C8	C8
XBAROUT9	O	OUTPUTXBAR Signal 9	C7	C7	C7
XBAROUT10	O	OUTPUTXBAR Signal 10	B7	B7	B7
XBAROUT11	O	OUTPUTXBAR Signal 11	D16	D16	D16
XBAROUT12	O	OUTPUTXBAR Signal 12	C17	C17	C17
XBAROUT13	O	OUTPUTXBAR Signal 13	D15	D15	D15
XBAROUT14	O	OUTPUTXBAR Signal 14	C15	C15	C15
XBAROUT15	O	OUTPUTXBAR Signal 15	P2	P2	P2

Table 5-117. External ADC Channel Select XBAR Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ZCZ C PIN [4]	ZCZ S PIN [4]	ZCZ F PIN [4]
ADC_EXTCH_XBAROUT0	O	External ADC Channel Select XBAR Signal 0	C11, C13	C11, C13	C11, C13
ADC_EXTCH_XBAROUT1	O	External ADC Channel Select XBAR Signal 1	A11, C14	A11, C14	A11, C14
ADC_EXTCH_XBAROUT2	O	External ADC Channel Select XBAR Signal 2	C10, C12	C10, C12	C10, C12
ADC_EXTCH_XBAROUT3	O	External ADC Channel Select XBAR Signal 3	B11, D11	B11, D11	B11, D11
ADC_EXTCH_XBAROUT4	O	External ADC Channel Select XBAR Signal 4	C9, P15	C9	C9
ADC_EXTCH_XBAROUT5	O	External ADC Channel Select XBAR Signal 5	A10, R16	A10	A10
ADC_EXTCH_XBAROUT6	O	External ADC Channel Select XBAR Signal 6	B10, F15	B10, F15	B10, F15
ADC_EXTCH_XBAROUT7	O	External ADC Channel Select XBAR Signal 7	C18, D9	C18, D9	C18, D9
ADC_EXTCH_XBAROUT8	O	External ADC Channel Select XBAR Signal 8	B15	B15	B15
ADC_EXTCH_XBAROUT9	O	External ADC Channel Select XBAR Signal 9	A15	A15	A15

Pin Connectivity Requirements

Ball Number	Ball Name	Pin Connectivity Requirements
D4	SAFETY_ERRORn	This pin must be connected to ground (VSS) through a separate external pull resistor to ensure it is held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull–down may be used to hold a valid logic low level if no PCB signal trace is connected to the ball.
J16	RSVD_J16	This pin must be connected to 1.2V supply (VDD).
T4 U1	RSVD_T4 RSVD_U1	Each of these pins must be connected (shorted) directly to ground (VSS)
U3 V2	RSVD_U3 RSVD_V2	Each of these pins must be left unconnected.
P15(1)	RSVD_P15(1)	This pin must be left unconnected

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Ball Number	Ball Name	Pin Connectivity Requirements
B3 C5 D5	TCK TDI TMS	Each of these pins must be connected to the corresponding power supply through separate external pull resistors to ensure these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull–up may be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
A13 B13	I2C0_SCL I2C0_SDA	Each of these pins must be connected to the corresponding power supply through separate external pull resistors to ensure these balls are held to a valid logic high level.
N1 N4 A11 C10	QSPI0_D0 (SOP0) QSPI0_D1 (SOP1) SPI0_CLK (SOP2) SPI0_D0 (SOP3)	Each of these pins must be connected to the corresponding power supply or ground (VSS) through separate external pull resistors to ensure these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.
U16 T15	ADC_CAL0 ADC_CAL1	If all ADCx_AINy inputs for all ADC instances (ADC[0:4]_AIN[0:5]) are not used, the ADC_CAL[0:1] analog pins must be connected (shorted) directly to ground (VSS).
U2	VSYS_MON	If VSYS_MON is not used, this pin may be connected (shorted) directly to ground (VSS).
ADC ZCZ PIN	ADC[0:4]_AIN[0:5]	Any unused ADCx_AINy input pin for any ADC instance (ADC[0:4]_AIN[0:5]) must be connected (shorted) directly to ground (VSS).
LVCMOS ZCZ PIN	Any LVCMOS Voltage Buffer Pin	If an associated IOMUX pad configuration register exists for a given pin, it may remain unconnected. After PORz, the LVCMOS voltage buffer is configured to a default state compatible with an unconnected ball.
P1(2) M4(2) P3(2) M1(2) L2(2) H1(2) J1(2) K2(2) J4(2) K4(2) K3(2)	GPIO0(2) GPIO5(2) GPIO6(2) GPIO7(2) GPIO9(2) GPIO65(2) GPIO66(2) GPIO67(2) GPIO68(2) GPIO69(2) GPIO70(2)	ZCZ_F Package only. Each of these pins must be left unconnected with no PCB trace.
L1(2)	GPIO8(2)	ZCZ_F Package only. This pin must be connected to VDDS33 through a separate external 4.7kΩ pull resistor placed as close to the device as possible.
J3(2)	GPIO64(2)	ZCZ_F Package only. OSPI_RESET_OUT0 connection to PORz. In order to reset the on-die OSPI flash module OSPI_RESET_OUT0 must be connected to an open-drain equivalent of PORz.

(1) ZCZ_S and ZCZ_F Package
(2) ZCZ_F Package only

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER		MIN	MAX	UNIT
VDD	1.2V SOC core supply	–0.5	1.5	V
VDDAR1	1.2V SRAM Array Supply 1	–0.5	1.5	V
VDDAR2	1.2V SRAM Array Supply 2	–0.5	1.5	V
VDDAR3	1.2V SRAM Array Supply 3	–0.5	1.5	V
VDDS18	1.8V IO Bias Supply from Bias LDO routed through Board	–0.5	2.1	V
VDDS33	3.3V IO Supply	–0.5	4.0	V
VDDA18_OSC_PLL	1.8V Analog Supply for PLL. Routed from the 1.8V Analog LDO out through Board	–0.5	2.1	V
VDDA33	Analog 3.3V Supply	–0.5	4.0	V
VDDA18	1.8V Analog Supply. Routed from the 1.8V Analog LDO out through Board	–0.5	2.1	V
IO Pin Steady State Voltage	3.3V LVCMOS IO Buffer	–0.3	VDDS33(3) + 0.3	V
	3.3V I2C Open-Drain IO Buffers	–0.3	VDDS33(3) + 0.3	V
	XTAL Pad	–0.5	2.1	V
Transient Overshoot and Undershoot	All Other IO Terminals	–0.3	VDDS33(3) + 0.2 × VDDS33(3) for up to 20% of signal period	V
	XTAL Pad 20% of VDDA18_OSC_PLL for up to 20% of signal period		0.2 × VDDA18_OSC_PLL	V
Latch Up Performance Class II (150°C)	Latch-up I-test Performance (Current-Pulse Injection on each IO pin)		±100	mA
	Latch-up Overvoltage Performance (Voltage Injection on each IO pin)		1.5 × VDDS33	V
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Storage temperature(4)	T_{stg}	–55	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) VDDS33 is the voltage on the corresponding power-supply pin(s) for the IC.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

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6.2 Electrostatic Discharge (ESD) Extended Automotive Ratings

over recommended operating conditions (unless otherwise noted)

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human body model (HBM), per AEC-Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC-Q100-011	All pins	±500	
			Corner balls (A1, A18, V1, V18)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Electrostatic Discharge (ESD) Industrial Ratings

over recommended operating conditions (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.4 Power-On Hours (POH) Summary

over recommended operating conditions (unless otherwise noted)[1] [2] [3]

PARAMETER	INDUSTRIAL	EXTENDED AUTOMOTIVE
Operating Junction Temperature (Tj)	–40°C to 105°C	–40°C to 150°C
POH @ Temp Profile	100K @ 97°C (100% @ 97°C) 70K @ 105°C (100% @ 105°C)	20K @ Automotive Temp Profile[4]

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature, and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) See *Automotive Temperature Profile* section

6.4.1 Automotive Temperature Profile

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
–40	1200	~50	~0.14	6%
75	4000	~167	~0.46	20%
95	13000	~541	~1.48	65%
130	1600	~67	~0.18	8%
150	200	~8.5	~0.023	1%
Total	20000	~833	~2.28	100%

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6.5 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
VDD	1.2V SOC Core Supply		1.140	1.200	1.260	V
VDDAR1, VDDAR2, VDDAR3	SRAM Array Supplies		1.140	1.200	1.260	V
VDDS18	1.8V IO Bias Supply from Bias LDO routed through board		1.710	1.800	1.890	V
VDDS33	3.3V IO Supply		3.135	3.300	3.465	V
VDDA18_OSC_PLL	1.8V Analog supply for PLL. Routed from the Analog LDO out through board		1.710	1.800	1.890	V
VDDA33	Analog 3.3V Supply		3.135	3.300	3.465	V
VDDA18	1.8V Analog supply. Routed from 1.8V Analog LDO out through Board		1.710	1.800	1.890	V
T_A	Free-air temperature	Extended Automotive	–40		125	°C
T_J	Operating junction temperature range	Industrial	–40		105	°C
		Extended Automotive Special Features - C, S	–40		150	°C
		Extended Automotive Special Features - F	–40		125	°C

6.6 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks, device core clocks, and available memory.

DEVICE	GRADE	RAM (MB)	R5FSS (MHz)	HSM (MHz)	ICSS (MHz)	INFRA[1] (MHz)
AM263Px	N	2	400	200	200	200
AM263Px	O	3	400	200	200	200
AM263Px	P	3	200	200	200	200

(1) Infrastructure includes all other modules and IP integrated in the device (such as CBASS/Interconnect and other SoC level peripherals) unless otherwise noted in the table.

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6.7 Power Consumption Summary

Section 6.7.1, *Power Consumption - Maximum* shows the maximum current consumed by each rail and should be used for power supply selection.

6.7.1 Power Consumption - Maximum

over recommended operating conditions (unless otherwise noted)

SUPPLY NAME	PARAMETER	MIN	MAX	UNIT
VDD + VDDARn	Maximum Current Rating for Core Domain		2.8	A
VDDS33	Maximum Current Rating for IO supply		200	mA
VDDA33	Maximum Current Rating for 3.3V Analog supply		200	mA

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6.8 Electrical Characteristics

Note

The interfaces or signals described in Section 6.8.1 *Digital and Analog IO Electrical Characteristics* through Section 6.8.6 *Power Management Unit (PMU)* correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

6.8.1 Digital and Analog IO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
PORz IO					
V_{IH}	High-Level Input Voltage	1.35			V
V_{IL}	Low-Level Input Voltage			0.5	V
V_{HYS}	Hysteresis Voltage at an Input	0.070			V
I_L	Input Leakage Current	–2		2	µA
Warm Reset IO					
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Hysteresis Voltage at an Input	0.347			V
V_{OL}	Low Level Output Voltage, Driver Enabled : I_{OL} = 6mA			0.45	V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–57			µA
TCK IO					
V_{IH}	High-Level Input Voltage	2.15			V
V_{IL}	Low-Level Input Voltage			0.55	V
V_{HYS}	Hysteresis Voltage at an Input	0.4			V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–3.9	8.9	17.2	µA
	Input Leakage Current, Receiver Disabled, Pullup Enabled		106.9	128.2	µA
	Input Leakage Current, Receiver Disabled, Pulldown Enabled		100.3	130.3	µA
I2C OD IOs					
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Hysteresis Voltage at an Input	0.165			V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–18		18	µA
V_{OL}	Low Level Output Voltage, Driver Enabled : I_{OL} = 3mA			0.45	V
All Other LVCMOS					
V_{IH}	High- Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{HYS}	Hysteresis Voltage at an Input	0.265			V
V_{OL}	Low Level Output Voltage, Driver Enabled : I_{OL} = 6mA			0.45	V
V_{OH}	High Level Output Voltage, Driver Enabled : I_{OH} = 6mA	VDDS33(1) – 0.45			V

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over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–18		18	µA
	Input Leakage Current, Receiver Disabled, Pullup Enabled	–243	–100	–19	µA
	Input Leakage Current, Receiver Disabled, Pulldown Enabled	51	100	210	µA

(1) VDDS33 is the voltage on the corresponding power-supply pin on the IC.

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6.8.2 Analog to Digital Converter Characteristics

This section describes the Analog to Digital Converter electrical characteristics required to ensure proper device operation.

6.8.2.1 Analog-to-Digital Converter (ADC)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REFHI}		1.71	1.8	1.89	V
Input Conversion Range (Vin+, Vin-)	Must be < VDDA33	0		32/18 × V_{REFHI}	V
Power-up time				500	µs
Gain error		–5	±3	5	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Same reference group		±4		LSBs
ADC-to-ADC offset error	Same reference group		±2		LSBs
DNL	Controlled environment to minimize input noise	–1	±0.5	1	LSBs
INL	Controlled environment to minimize input noise	–2	±1.0	2	LSBs
SNR	Controlled environment to minimize input noise		68		dB
ENOB (Synchronous Operation)			11		bits
ENOB (Asynchronous Operation)			9.7		bits
ADC-to-ADC isolation	Synchronous operation	–10		10	LSBs
V_{REFHI} input current			400		µA
Conversion time				250	ns
Parasitic Input Capacitance (C_p)(1)			7		pF
Sample/Hold Resistance (R_{on})(1)				1.2	kΩ
Sample/Hold Capacitance (C_h)(1)				8	pF
Input Leakage			0.1	TBD	µA
Power supply (VDDA33)		3.13	3.3	3.46	V
Power supply (VDDA18)		1.71	1.8	1.89	V
Power Consumption (VDDA33)			200		µA
Power Consumption (VDDA18)			700		µA

(1) See *ADC Input Model*

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6.8.2.2 Resolver Analog-to-Digital Converter (ADC_R)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REFHI}		1.71	1.8	1.89	V
Input Conversion Range (Vin+, Vin-)	Must be < VDDA33	0		33/18 × V_{REFHI}	V
Power-up time				500	µs
Gain error		–5	±3	5	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Same reference group		±4		LSBs
ADC-to-ADC offset error	Same reference group		±2		LSBs
DNL	Controlled environment to minimize input noise	–1	±0.5	1	LSBs
INL	Controlled environment to minimize input noise	–2	±1.0	2	LSBs
SNR	Controlled environment to minimize input noise		68		dB
ENOB (Synchronous Operation)			11		bits
ENOB (Asynchronous Operation)			9.7		bits
ADC-to-ADC isolation	Synchronous operation	–10		10	LSBs
V_{REFHI} input current			500		µA
Conversion time			333		ns
Parasitic Input Capacitance (C_p)(1)			7		pF
Sample/Hold Resistance (R_{on})(1)				1.2	kΩ
Sample/Hold Capacitance (C_h)(1)				8	pF
Input Leakage			TBD	TBD	µA
Power supply (VDDA33)		3.13	3.3	3.46	V
Power supply (VDDA18)		1.71	1.8	1.89	V
Power Consumption (VDDA33)			200		µA
Power Consumption (VDDA18)			500		µA

(1) See *ADC Input Model*

6.8.2.3 ADC Input Model

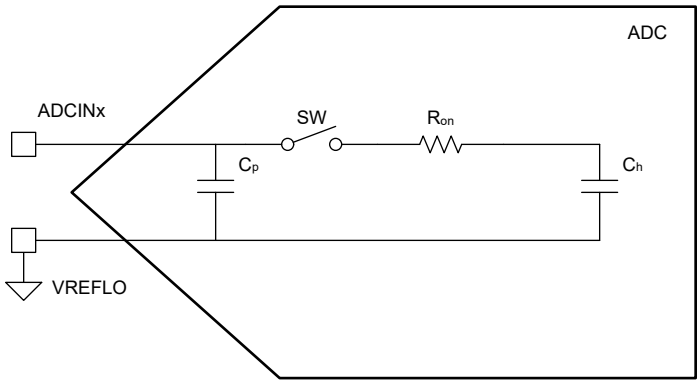

Figure 6-1. ADC Input Model

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6.8.3 Comparator Subsystem A (CMPSSA)

SUBGROUP	PARAMETER	MIN	TYP	MAX	UNIT
Comparator	Power-up time			10	µs
	Comparator input range	0.1		VDDA33(1) – 50mV	V
	Input referred offset error	–20		20	mV
	Hysteresis (H1)		NA		LSB
	Hysteresis (H2)		15		LSB
	Hysteresis (H3)		35		LSB
	Hysteresis (H4)		55		LSB
	Propagation delay		21	50	ns
DAC	DAC_VREF reference voltage	1.71	1.8	1.89	V
	DAC output range	0.1		Minimum of 33/18 × DAC_VREF or VDDA33(1) – 50mV	V
	Static offset error	–45		45	mV
	Static gain error	–2		2	% of FSR
	Static DNL	>–1		4	LSB
	Static INL	–16		16	LSB
	Settling time			1	µs
	Resolution		12		bits
	DAC output disturbance (comparator trip kickback)	–100		100	LSB
	DAC output disturbance (comparator trip kickback)		200		ns
	DAC_VREF loading		37		kΩ
Common	Input Leakage		0.1	TBD	µA
	Power supply (VDDA33)	3.13	3.3	3.46	V
	Power supply (VDDA18)	1.71	1.8	1.89	V
	Power consumption (VDDA33)		900		µA
	Power consumption (VDDA18)		120		µA
	Failsafe Input current injection			10	mA

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

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6.8.4 Comparator Subsystem B (CMPSSB)

SUBGROUP	PARAMETER	MIN	TYP	MAX	UNIT
Comparator	Power-up time			10	µs
	Comparator input range	0.1		VDDA33(1) – 50mV	V
	Input referred offset error	–20		20	mV
	Hysteresis (H1)		NA		LSB
	Hysteresis (H2)		15		LSB
	Hysteresis (H3)		35		LSB
	Hysteresis (H4)		55		LSB
	Propagation delay		21	50	ns
DAC	DAC_VREF reference voltage	1.71	1.8	1.89	V
	DAC output range	0.1		Minimum of 33/18 × DAC_VREF or VDDA33(1) - 50mV	V
	Static offset error	–45		45	mV
	Static gain error	–2		2	% of FSR
	Static DNL	>–1		4	LSB
	Static INL	–16		16	LSB
	Settling time			1	µs
	Resolution		12		bits
	DAC output disturbance (comparator trip kickback)	–100		100	LSB
	DAC output disturbance (comparator trip kickback)		200		ns
	DAC_VREF loading		37		kΩ
Common	Input Leakage		0.1	TBD	µA
	Power supply (VDDA33)	3.13	3.3	3.46	V
	Power supply (VDDA18)	1.71	1.8	1.89	V
	Power consumption (VDDA33)		900		µA
	Power consumption (VDDA18)		120		µA
	Failsafe input current injection			10	mA

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

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6.8.5 Digital-to-Analog Converter (DAC)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time				1	µs
DAC_VREF		1.71	1.8	1.89	V
Voltage output range		0.3		VDDA33(1) – 0.3	V
Trimmed offset error	Offset is checked at Midpoint (code 2048)	–10		10	mV
Gain error	DAC_VREF = 1.8V	–2.5		2.5	% of FSR
DNL	Endpoint corrected	–1		1	LSB
INL	Endpoint corrected	–20		20	LSB
Settling time	Settling to 2 LSBs (~1.6mV) after 0.3V-to-3V transition		2		µs
Resolution			12		bits
Capacitive load	Output drive capability			100	pF
Resistive load	Output drive capability	5			kΩ
DAC_VREF loading	DAC_VREF		64		kΩ
Output noise (100Hz-100KHz)	Integrated noise from 100Hz to 100kHz		1		mVrms
SNR @ 1KHz	2MHz DACVALA update rate, 200kHz output filter		60		dB
Power supply (VDDA33)		3.13	3.3	3.46	V
Power supply (VDDA18)		1.71	1.8	1.89	V
Power Consumption (VDDA33)			850		µA
Power Consumption (VDDA18)			35		µA

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

6.8.6 Power Management Unit (PMU)

over operating junction temperature range (unless otherwise noted)

GROUP	PARAMETER	MIN	TYP	MAX	UNIT
PMU	Power supply (VDDA33)	3.1	3.3	3.46	V
Bandgap	V_{REF} trimmed	0.886	0.9	0.914	V
1.8V LDO	DC accuracy	1.764	1.8	1.836	V
	Transient load regulation	1.71	1.8	1.89	V
	DC Load regulation			5	mV
	Load current	0		60	mA
	Power up time			800	uS
	Inrush current			150	mA
	External decoupling capacitance	–20%	4.7	20%	uF
ADC Reference	Load Regulation		±1		mV
	DC accuracy	1.764	1.8	1.836	V
	Power up time			800	uS
	Inrush current			80	mA
	External decoupling capacitance	–20%	4.7	20%	uF

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6.8.7 Safety Comparators

PARAMETER			MIN	TYP	MAX	UNIT
C0	C0: 1.8V Monitor Threshold		1.40	1.5	1.6	V
C1	BGAP Monitor	Lower Threshold	0.75	0.8	0.85	V
		Upper Threshold	0.935	1	1.065	V
C2	Monitors 1.8V Supply vs BGAP	Lower Threshold	1.47	1.52	1.57	V
		Upper Threshold	2.13	2.195	2.26	V
C3	Monitors 1.2V vs BGAP	Lower Threshold	0.98	1.011	1.041	V
		Upper Threshold	1.407	1.451	1.494	V
C4	Vref Monitor (ROK0)	Lower Threshold	1.56	1.61	1.66	V
		Upper Threshold	2.09	2.16	2.22	V
C5	Monitors IO Bias Supply vs BGAP	Lower Threshold	1.47	1.52	1.57	V
		Upper Threshold	2.13	2.195	2.26	V
C6	Vref Monitor (ROK0B)	Lower Threshold	1.56	1.61	1.66	V
		Upper Threshold	2.09	2.16	2.22	V
C7	System Supply Monitor (VSYS_MON)	Lower Threshold	0.873	0.9	0.927	V
C8	UnderVoltage Threshold		2.59	2.77	2.95	V
C9	Vref Monitor (ROK1)	Lower Threshold	1.56	1.61	1.66	V
		Upper Threshold	2.09	2.16	2.22	V

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6.9 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses.

6.9.1 VPP Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
VDD	Supply voltage range for the core domain during OTP operation	Normal Operation	1.140	1.200	1.260	V
VPP	Supply voltage range for the eFuse ROM domain	Normal Operation	No Connection			V
	Supply voltage range for the eFuse ROM domain during OTP programming	OTP Programming	1.65	1.7	1.75	V
$I_{(VPP)}$	VPP Current	$I_{(VPP)}$			100	mA
T_A	Ambient Temperature	Ambient Temperature	0	30	50	℃

6.9.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-on sequence (for more details, see Section 6.11.2.1, *Power-On and Reset Sequencing*).

6.9.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-on sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in Section 6.9.1, *VPP Specifications*.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

6.9.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse.

CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

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6.10 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Section 6.5, *Recommended Operating Conditions*.

6.10.1 Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	5.4	N/A
$R\Theta_{JB}$	Junction-to-board	5.4	N/A
$R\Theta_{JA}$	Junction-to-free air	18.5	0
$R\Theta_{JA}$	Junction-to-moving air	TBD	1
		TBD	2
		TBD	3
Ψ_{JT}	Junction-to-package top	0.1	0
		TBD	1
		TBD	2
		TBD	3
Ψ_{JB}	Junction-to-board	5.3	0
		TBD	1
		TBD	2
		TBD	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) °C/W = degrees Celsius per watt
(3) m/s = meters per second

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6.11 Timing and Switching Characteristics

Note

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

6.11.1 Timing Parameters and Information

The timing parameter symbols used in *Timing and Switching Characteristics* sections are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 6-1:

Table 6-1. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

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6.11.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation.

6.11.2.1 Power-On and Reset Sequencing

AM263Px attempts to simplify the power reset requirements from previous Sitara MCU devices. There is no sequencing requirement with respect to the primary core digital VDD 1.2V and I/O power 3.3V rails. There are two on-die LDO that are supplied through the VDDS33 and VDDA33 power nets respectively. These on-die LDO generate the required VDDS1V8 and VDDA1V8 1.8V digital and analog power. The AM263Px does require the minimum ramp time be respected for 3.3V power-on. Additional PORz and SOP boot mode latch timing must be respected by the EVM design as well. Figure 6-2 describes the device power-on sequencing.

Table 6-2. AM263Px Power-On Sequencing

PARAMETER		MIN	MAX	UNIT
$t_{Startup}$	Time for 1.2V and 3.3V DC-DC converters to startup after being enabled. This is an arbitrary amount of time - no constraint imposed by the device.	–	–	ms
t_{PGood}	Time for Power Good signals to be generated from DC-DC converters after rails are stable. This is an arbitrary amount of time - no constraint imposed by the device.	–	–	ms
t_{Ramp_3V3}	Ramp time of the VDDS3V3 and VDDA3V3 supplies. This is a requirement imposed by the device.	0.1	–	ms
$t_{SOP_Sampled}$	Time from PORz de-assertion until the SOP[3:0] pins are sampled. This is a device internal pentameter. Sampling happens when the internally generated supplies are stable. For information only. Refer to TSU_SOP and TH_SOP parameters for application usage.	0	–	ms
t_{SU_SOP}	Setup time for SOP relative to PORz assertion.	10	–	µs
t_{H_SOP}	Hold time for SOP relative to WARMRSTn deassertion.	0	–	µs
$t_{WARMRSTn}$	Time from PORz de-assertion until the device de-asserts the WARMRESETn signal.	2.0	–	ms

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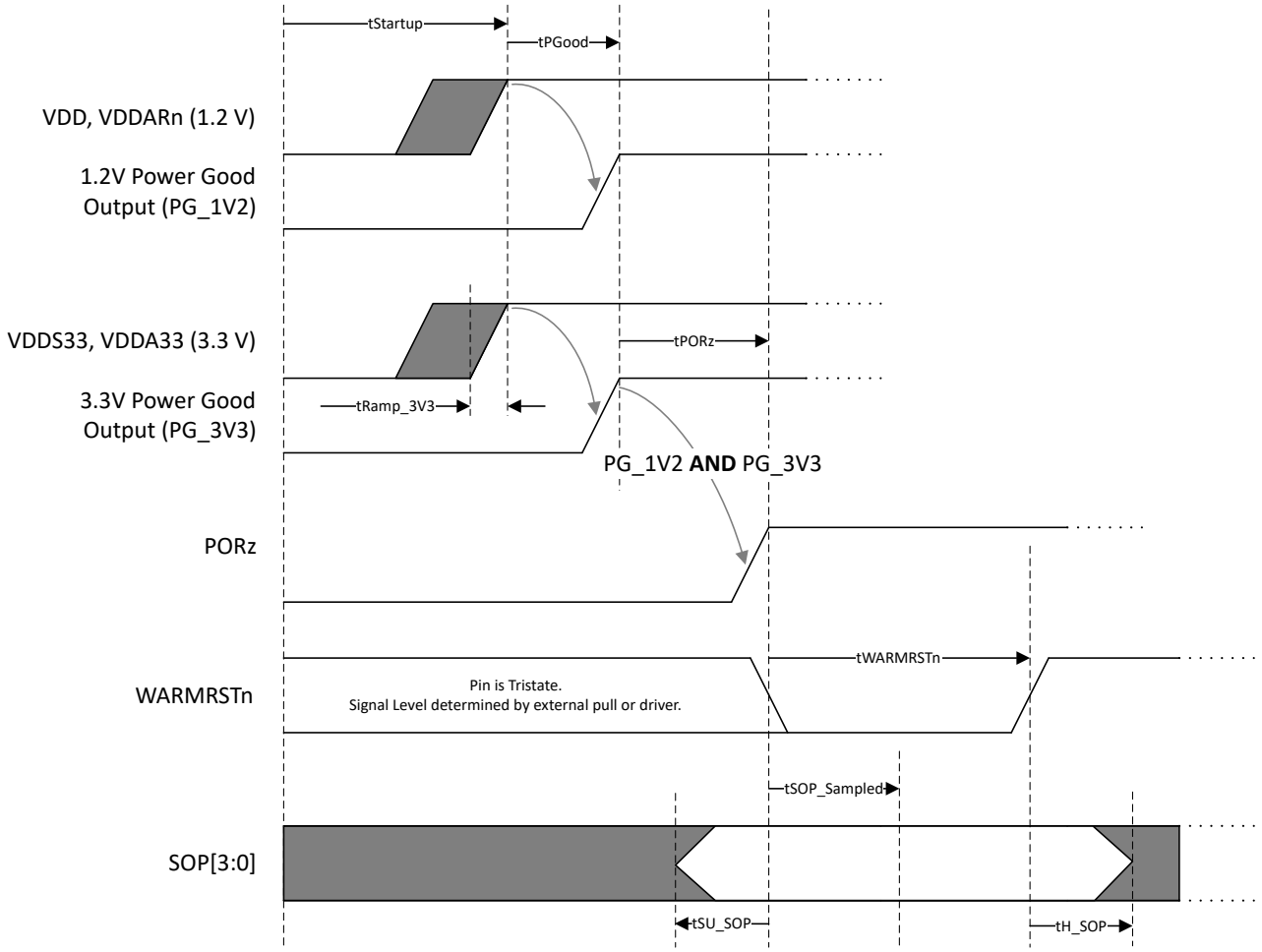

Figure 6-2. Power-On Sequencing

6.11.2.1.1 Power Reset Sequence Description

The following set of steps shall occur on the EVM and AM263Px to boot the device from power-on reset.

1. PORz is held low by the external power supply monitor
2. VDD core digital 1.2V and VDDS3V3/VDDA3V3 3.3V supplies ramp to their nominal voltages
   a. This requires a logical AND be applied to the power good signal generated from each supply
3. SOP[3:0] pins held in their boot latch state
4. After PCB supplied power nets are stable, the external supply monitor will de-assert PORz
5. Device will startup 1.8V on-die LDO
6. After internal supply monitors show externally and internally generated supplies are stable, the SOP[3:0] pin states are latched
7. R5F cores are unhalted and SOP selected boot ROM execution begins

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6.11.2.2 Power-Down Sequencing

Figure 6-3 describes the device power-down sequencing. The order of AM263Px 1.2V and 3.3V does not matter.

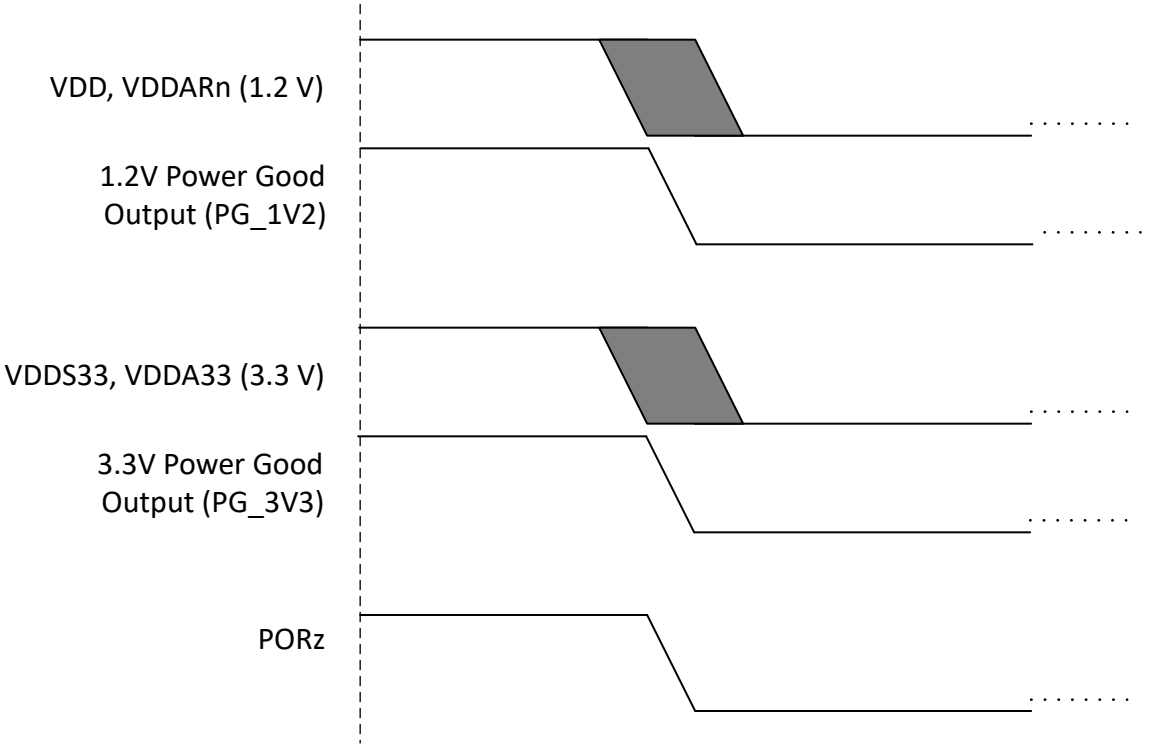

Figure 6-3. Power-Down Sequencing

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6.11.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.3.1 System Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	2	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	3	30	pF

6.11.3.2 Reset Timing

Tables and figures provided in this section define timing requirements and switching characteristics for reset related signals.

6.11.3.2.1 PORz Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES_VALID-PORz)}$	Hold time, PORz active (low) at Power-up after supplies valid (using external crystal)	0		ns
RST3	$t_{w(PORzL)}$	Pulse Width minimum, PORz low after Power-up (without removal of Power or system reference clock XTAL_XI/XO)	1000		ns

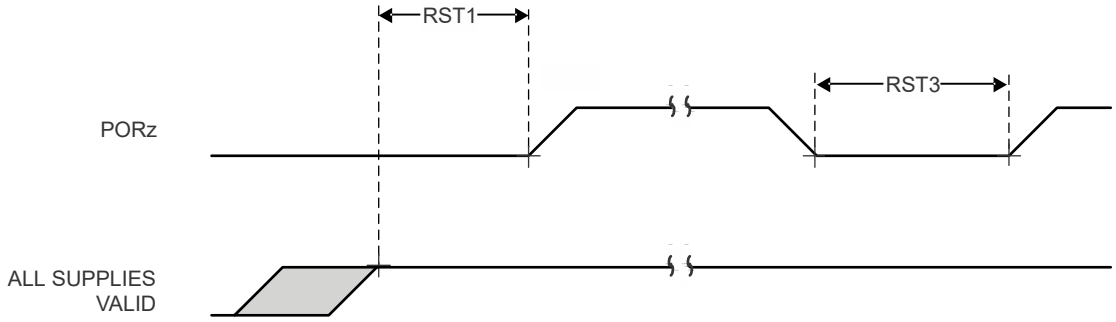

Figure 6-4. PORz Timing Requirements

6.11.3.2.2 WARMRSTn Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST4	$t_{d(PORzL:-WARMRSTnZ)}$	Delay time, PORz active (low) to WARMRSTn high impedance	0	0	ns
RST5	$t_{d(PORzH-WARMRSTnL)}$	Delay time, PORz inactive (high) to WARMRSTn active (low)	0	0	ns
RST6	$t_{d(PORzH-WARMRSTnH)}$	Delay time, PORz inactive (high) to WARMRSTn inactive (high)	2000000	6000000	ns

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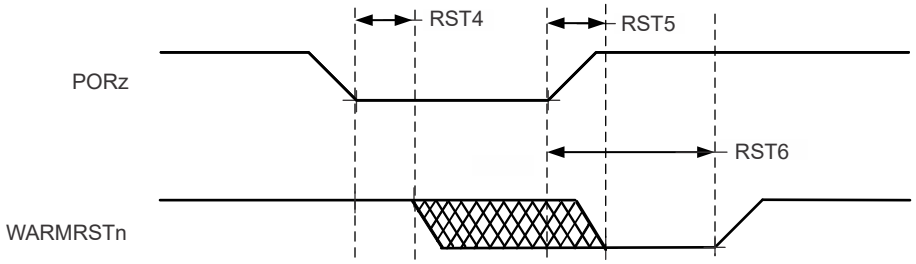

Figure 6-5. WARMRSTn Switching Characteristics

6.11.3.2.3 WARMRSTn Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST10	$t_{w(WARMRSTnL)}$ (1)	Pulse Width minimum, WARMRSTn active (low)	500	16384000	ns

(1) This timing parameter is controlled by the TOP_RCM.WARM_RSTTIME1/2/3 registers. See the Reset section of the Technical Reference Manual for more details.

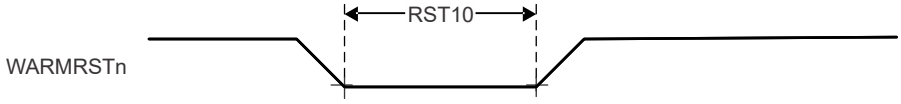

Figure 6-6. WARMRSTn Timing Requirements and Switching Characteristics

6.11.3.3 Safety Signal Timing

Tables and figures provided in this section define switching characteristics for SAFETY_ERRORn.

6.11.3.3.1 SAFETY_ERRORn Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SFTY1	$t_{c(SAFETY_ERRORn)}$	Cycle time minimum, SAFETY_ERRORn (PWM mode enabled)	($P^{(1)} \times H^{(3)}$) + ($P^{(1)} \times L$)(4)		ns
SFTY2	$t_{w(SAFETY_ERRORn)}$	Pulse width minimum, SAFETY_ERRORn active (PWM mode disabled)(5)	$P^{(1)} \times R^{(2)}$		ns
SFTY3	$t_{d(ERROR_CONDITION-SAFETY_ERRORnL)}$	Delay time, ERROR_CONDITION to SAFETY_ERRORn active(5)	$50 \times P^{(1)}$		ns

(1) P = ESM functional clock
(2) R = Error Pin Counter Pre-Load Register count value
(3) H = Error Pin PWM High Pre-Load Register count value
(4) L = Error Pin PWM Low Pre-Load Register count value
(5) When PWM mode is enabled, SAFETY_ERRORn stops toggling after SFTY3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, SAFETY_ERRORn is active low

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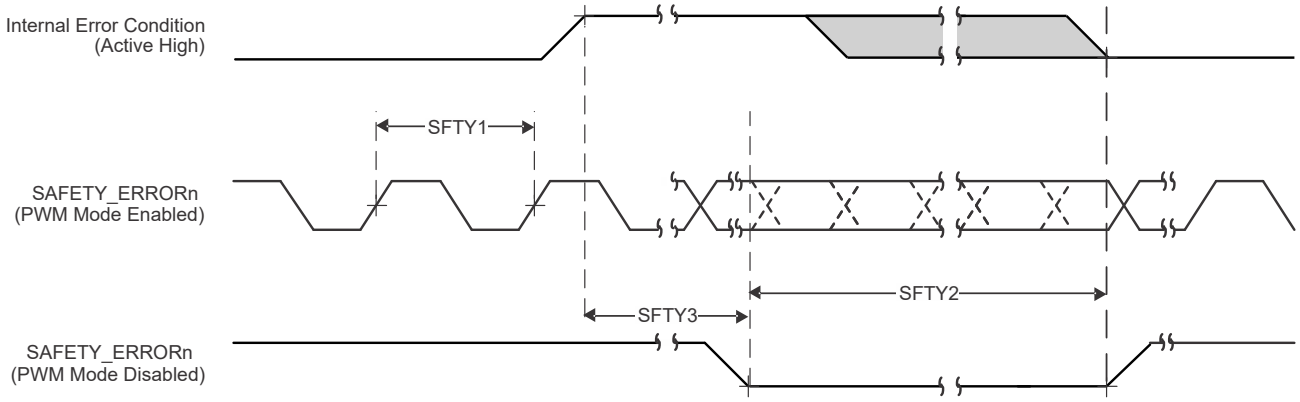

Figure 6-7. MCU_SAFETY_ERRORn Timing Requirements and Switching Characteristics

6.11.4 Clock Specifications

6.11.4.1 Input Clocks / Oscillators

6.11.4.1.1 Crystal Oscillator (XTAL) Parameters

PARAMETER		MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency (Fundamental mode oscillation only)	–50ppm	25	50ppm	MHz
Duty Cycle	Duty cycle output of XTAL	45	50	55	%
CC1	Capacitance of C_{L1} + C_{PCBXI}	12		24	pF
CC2	Capacitance of C_{L2} + C_{PCBXO}	12		24	pF
C_{shunt}	Crystal Circuit Shunt Capacitance			5	pF
ESR_{xtal}	Crystal Effective Series Resistance			46	Ω

6.11.4.1.2 External Clock Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
C_{Pkg}	Shunt Capacitance of package		0.01		pF
P_{xtal}	Power dissipation		$0.5 \times ESR \times (2 \times \pi \times F_{xtal} \times C_L \times 1.8)^2$		W
t_s	Startup time		1.5		ms

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6.11.5 Peripherals

6.11.5.1 2-port Gigabit Ethernet MAC (CPSW)

Note

The CPSW supports two external Ethernet ports and one internal port.

For more details about features and additional description information on the device CPSW (2-port Gigabit Ethernet MAC), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.5.1.1 CPSW MDIO Timing

6.11.5.1.1.1 CPSW MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	10	470	pF

6.11.5.1.1.2 CPSW MDIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{su(MDIO-MDC)}$	Setup time, MDIO_DATA valid before MDIO_CLK high	90		ns
MDIO2	$t_{h(MDC-MDIO)}$	Hold time, MDIO_DATA valid after MDIO_CLK high	0		ns

6.11.5.1.1.3 CPSW MDIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO_CLK	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse duration, MDIO_CLK high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse duration, MDIO_CLK low	160		ns
MDIO7	$t_{d(MDC_MDIO)}$	Delay time, MDIO_CLK low to MDIO_DATA valid	–150	150	ns

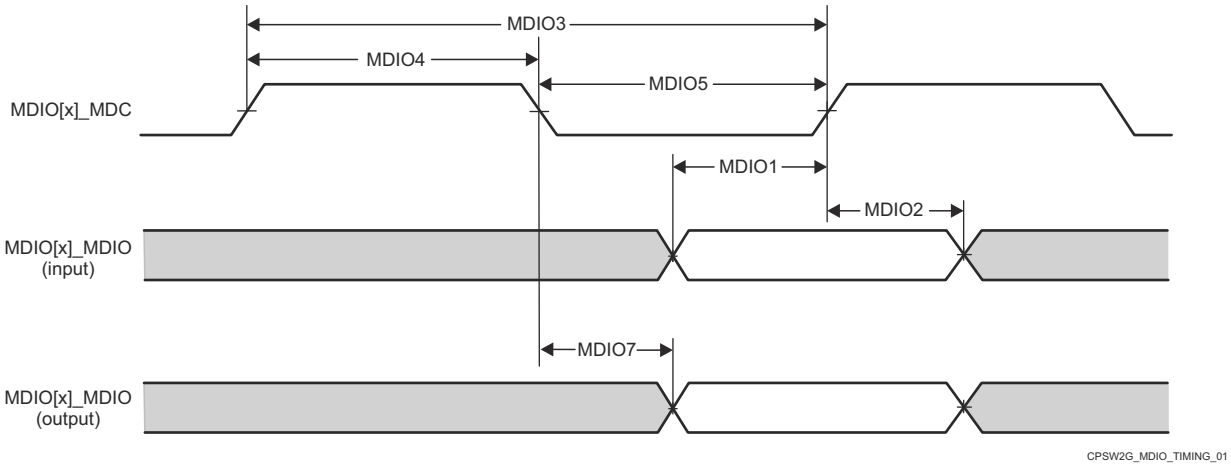

Figure 6-8. CPSW MDIO Timing Requirements and Switching Characteristics

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6.11.5.1.2 CPSW RGMII Timing

6.11.5.1.2.1 CPSW RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		2	20	pF
PCB Connectivity Requirements					
t_d (Trace Mismatch Delay)	Propagation Delay mismatch across all traces	RGMII[x]_RXC RGMII[x]_RD[3:0] RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC RGMII[x]_TD[3:0] RGMII[x]_TX_CTL		50	ps

6.11.5.1.2.2 CPSW RGMII[x]_RCLK Timing Requirements - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	tw(RXCH)	Pulse duration, RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	tw(RXCL)	Pulse duration, RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.11.5.1.2.3 CPSW RGMII[x]_RD[3:0], and RGMII[x]_RCTL Timing Requirements

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RD[3:0] valid before RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX_CTL-RXC)}$	Setup time, RX_CTL valid before RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RD[3:0] valid after RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX_CTL)}$	Hold time, RX_CTL valid after RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns

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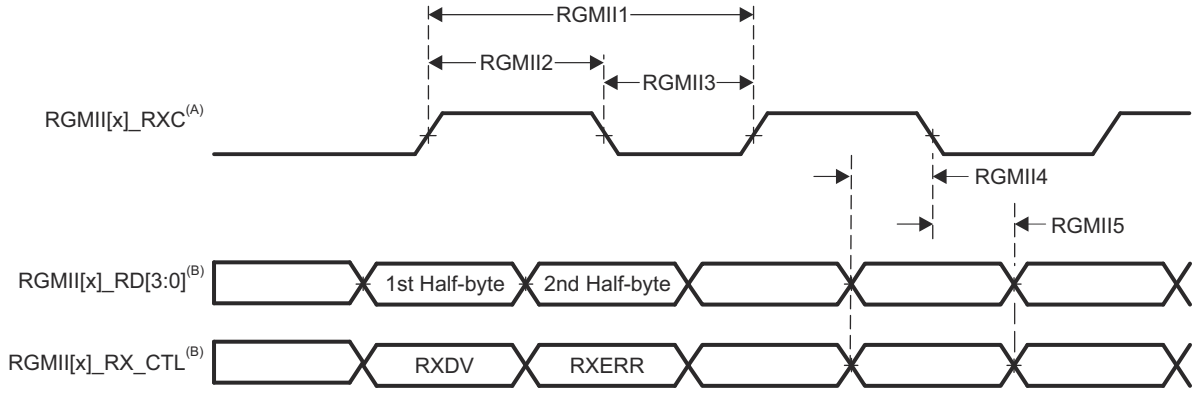

A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

Figure 6-9. CPSW RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

6.11.5.1.2.4 CPSW RGMII[x]_TCLK Switching Characteristics - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.11.5.1.2.5 CPSW RGMII[x]_TD[3:0], and RGMII[x]_TCTL Switching Characteristics - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX_CTL-TXC)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX_CTL)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns

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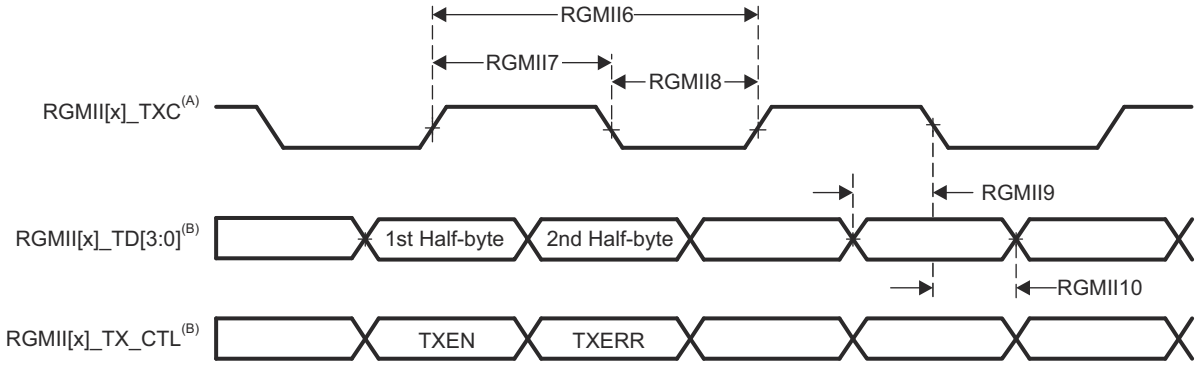

A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is by default enabled after POR.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

Figure 6-10. CPSW RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

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6.11.5.1.3 CPSW RMII Timing

6.11.5.1.3.1 CPSW RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	VDD = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		3	25	pF

6.11.5.1.3.2 CPSW RMII[x]_REFCLK Timing Requirements - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	19.999	20	ns
RMII2	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK High	7	13	ns
RMII3	$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK Low	7	13	ns

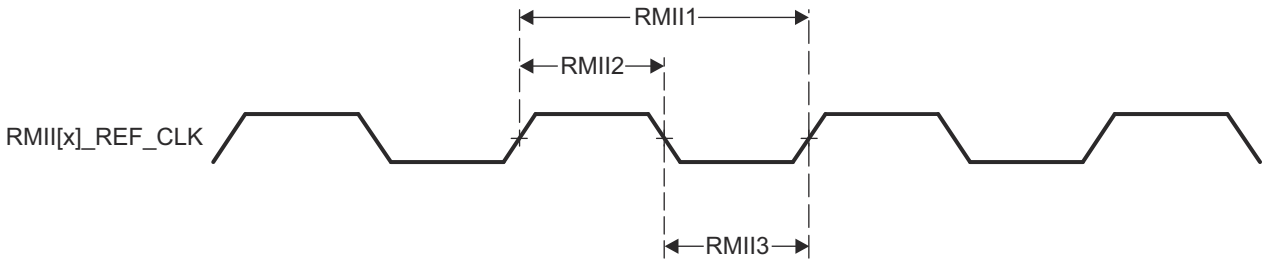

Figure 6-11. CPSW RMII[x]_REF_CLK Timing Requirements – RMII Mode

6.11.5.1.3.3 CPSW RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER Timing Requirements - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF_CLK)}$	Setup time, RXD[1:0] valid before REF_CLK	4		ns
	$t_{su(CRS_DV-REF_CLK)}$	Setup time, CRS_DV valid before REF_CLK	4		ns
	$t_{su(RX_ER-REF_CLK)}$	Setup time, RX_ER valid before REF_CLK	4		ns
RMII5	$t_{h(REF_CLK-RXD)}$	Hold time, RXD[1:0] valid after REF_CLK	2		ns
	$t_{h(REF_CLK-CRS_DV)}$	Hold time, CRS_DV valid after REF_CLK	2		ns
	$t_{h(REF_CLK-RX_ER)}$	Hold time, RX_ER valid after REF_CLK	2		ns

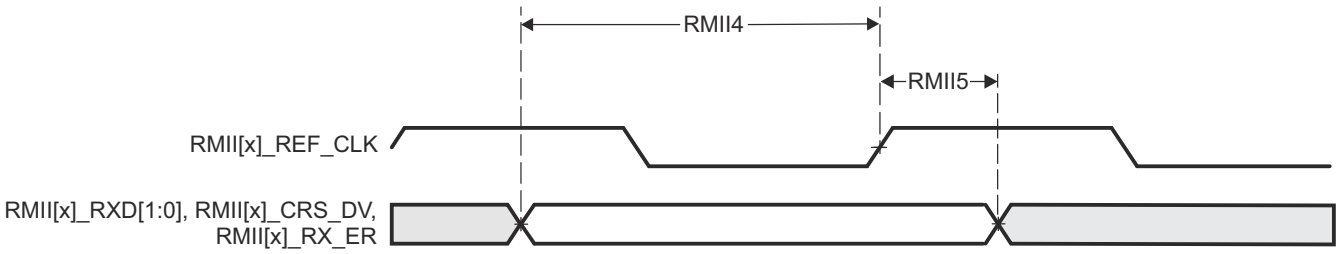

Figure 6-12. CPSW RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

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6.11.5.1.3.4 CPSW RMII[x]_TXD[1:0], and RMII[x]_TXEN Switching Characteristics - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF_CLK-TXD)}$	Delay time, REF_CLK High to TXD[1:0] valid	2	10	ns
	$t_{d(REF_CLK-TXEN)}$	Delay time, REF_CLK to TXEN valid	2	10	ns

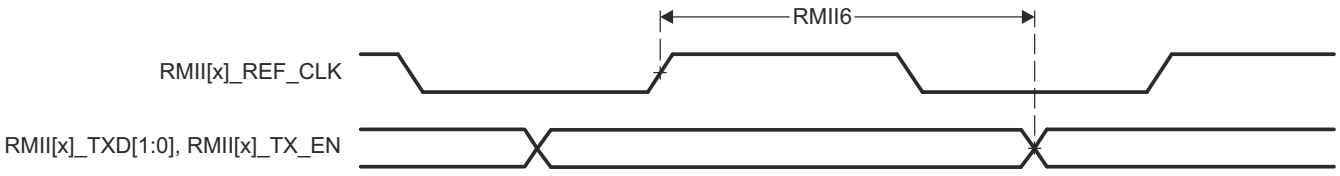

Figure 6-13. CPSW RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

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6.11.5.2 Enhanced Capture (eCAP)

Note

The device has multiple eCAP modules. The generic CAP_ prefix is used to represent the signal names for all eCAP instances.

For more information, see *Enhanced Capture (eCAP) Module* section in the device TRM.

6.11.5.2.1 ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.2.2 ECAP Timing Requirements

NO.	PARAMETER	DESCRIPTION		MIN MAX	UNIT
CAP1	$t_{w(CAP)}$	Capture input pulse width	Asynchronous	(2 + X[2]) × P[1]	ns
			Synchronous	(3 + X[2]) × P[1]	
			With input qualifier	(2 + X[2]) × P[1] + U[3]	

(1) P = sysclk period in ns.
(2) X = value of ECCTL0_TYPE3[QUALPRD] setting.
(3) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode

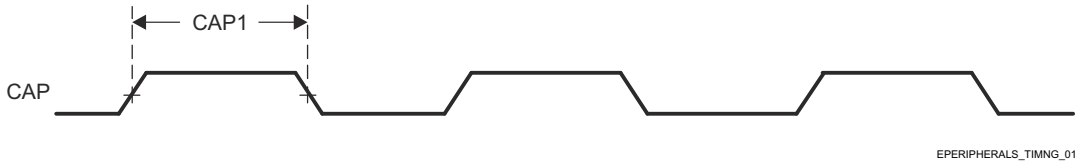

Figure 6-14. ECAP Timings Requirements

6.11.5.2.3 ECAP Switching Characteristics

(1)

NO.	PARAMETER	DESCRIPTION	MIN MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx output high/low	10	ns

(1) Some ECAP signals are pinmuxed with I2C0 SDA and SCL pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

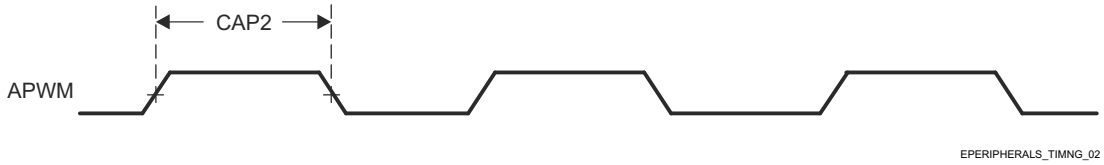

Figure 6-15. ECAP Switching Characteristics

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6.11.5.3 Enhanced Pulse Width Modulation (ePWM)

Note

The device has multiple ePWM modules. The generic EHRPWM_ prefix is used to represent the signal names for all ePWM instances.

For more information, see *Enhanced Pulse Width Modulation (ePWM) Module* section in the device TRM.

6.11.5.3.1 EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.3.2 EPWM Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2P(1)		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	1P(1)		ns

(1) P = sysclk period in ns.

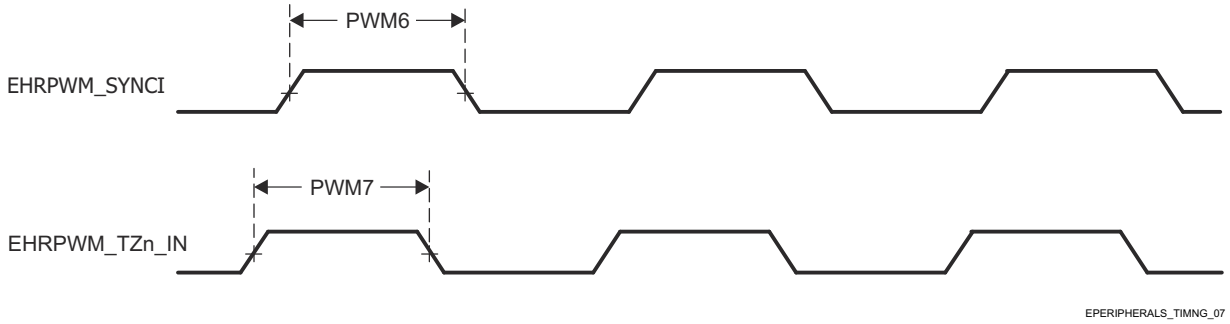

Figure 6-16. EPWM Timing Requirements

6.11.5.3.3 EPWM Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	20		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	8P(1)		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		30	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		30	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	32P(1)		ns

(1) P = sysclk period in ns.

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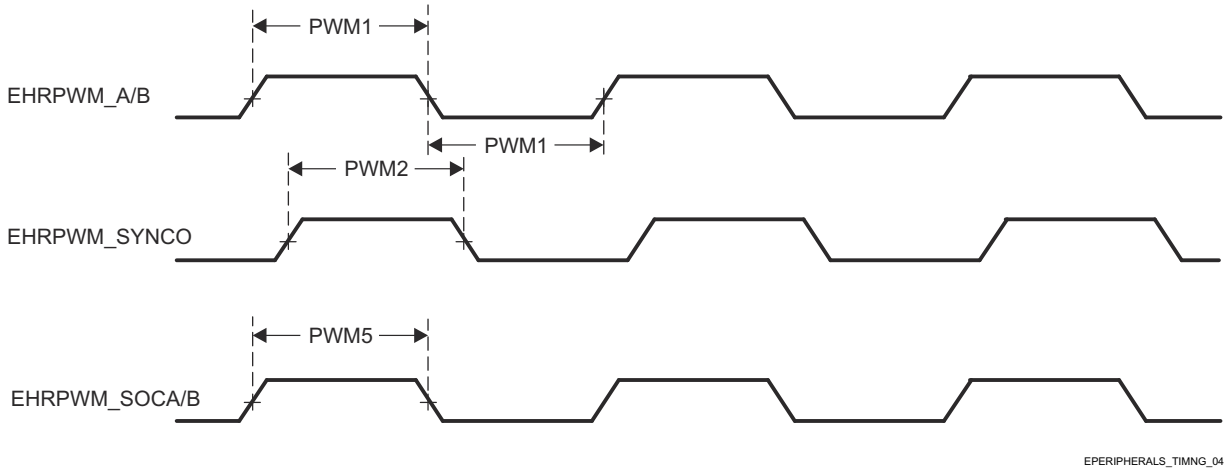

Figure 6-17. EHRPWM Switching Characteristics

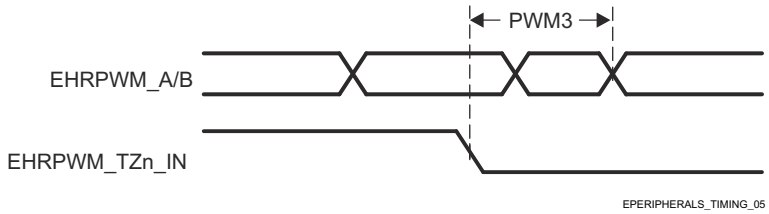

Figure 6-18. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

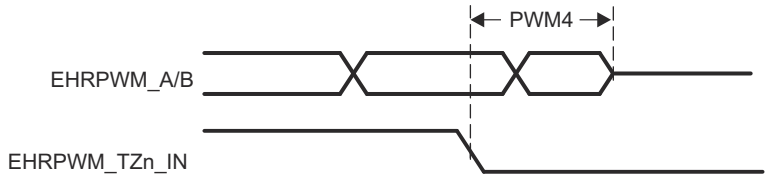

Figure 6-19. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

EPWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size[1]		TBD	TBD	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on VDD. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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6.11.5.4 Enhanced Quadrature Encoder Pulse (eQEP)

Note

The device has multiple eQEP modules. The generic QEP_ prefix is used to represent the signal names for all eQEP instances.

For more information, see *Enhanced Quadrature Encoder Pulse (eQEP) Module* section in the device TRM.

6.11.5.4.1 EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.4.2 EQEP Timing Requirements

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
QEP1	$t_{w(QEPP)}$	QEP input period	Synchronous(3)	3P(1)		ns
			With input qualifier	2 × (P(1) + U(2))		
QEP2	$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous(3)	2 + 3P(1)		ns
			With input qualifier	2P(1) + U(2)		
QEP3	$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous(3)	3P(1)		ns
			With input qualifier	2P(1) + U(2)		
QEP4	$t_{w(STROBH)}$	QEP Strobe High time	Synchronous(3)	3P(1)		ns
			With input qualifier	2P(1) + U(2)		
QEP5	$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous(3)	3P(1)		ns
			With input qualifier	2P(1) + U(2)		

(1) P = sysclk period in ns.
(2) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode.
(3) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

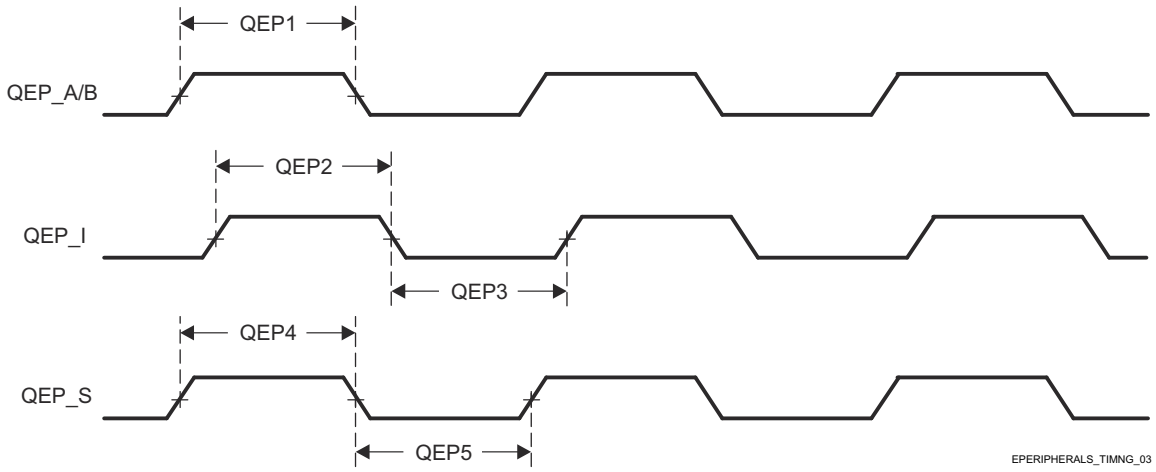

Figure 6-20. EQEP Timing Requirements

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6.11.5.4.3 EQEP Switching Characteristics

(3)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		4 + U(2) + 6P(1)	ns
QEP7	$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		4 + U(2) + 7P(1) + 4	ns

(1) P = sysclk period in ns.
(2) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode.
(3) Some EQEP signals are pinmuxed with I2C0 SDA and SCI pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

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6.11.5.5 Fast Serial Interface (FSI)

Note

The device has multiple FSI modules. FSIn is a generic prefix applied to FSI signal names, where n represents the specific FSI module.

For more information, see *Fast Serial Interface* section in the device TRM.

6.11.5.5.1 FSI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.8	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	7	pF

6.11.5.5.2 FSIRX Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR1	$t_{c(RX_CLK)}$	Cycle time, FSIRXn_CLK	16.67		ns
FSIR2	$t_{w(RX_CLK)}$	Pulse width, FSIRXn_CLK low or FSIRXn_CLK high	0.35P(1) – 1	0.65P(1) + 1	ns
FSIR3	$t_{su(RX_D–RX_CLK)}$	Setup time, FSIRXn_D[0:1] valid before FSIRXn_CLK	1.7		ns
FSIR4	$t_{h(RX_CLK–RX_D)}$	Hold time with respect to both edges of FSIRXn_CLK	2		ns

(1) $P = T_{c(RX_CLK)}$ = RX Interface clock period in ns.

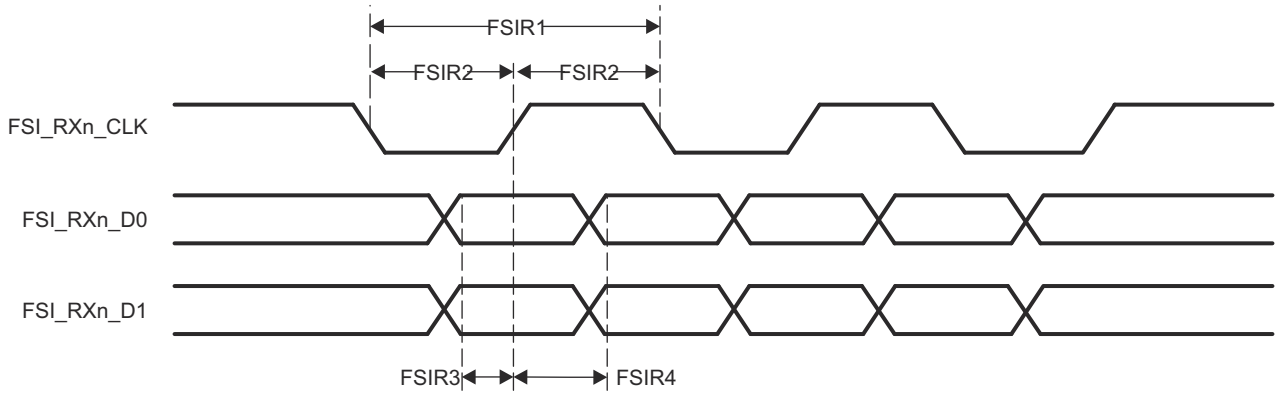

Figure 6-21. FSI Timing Requirements

6.11.5.5.3 FSIRX Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR5	$t_{d(RX_CLK)}$	FSIRXn_CLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
FSIR6	$t_{d(RX_D0)}$	FSIRXn_D0 delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
FSIR7	$t_{d(RX_D1)}$	FSIRXn_D1 delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
FSIR8	$t_{d(DELAY_ELEMENT)}$	Incremental delay of each delay line element for FSIRXn_CLK, FSIRXn_D0, and FSIRXn_D1	0.3	1	ns

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NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR_TDM1	$t_{skew(RX_CLK-TX_TDM_D)}$	Delay skew between FSIRXn_TDM_CLK delay and FSIRXn_TDM_D[0:1]	–3	3	ns
FSIR_TDM2	$t_{skew(RX_CLK-TX_TDM_CLK)}$	Delay time, FSIRXn_CLK input to FSITXn_TDM_CLK output	2	12	ns
FSIR_TDM3	$t_{skew(RX_D0-TX_TDM_D0)}$	Delay time, FSIRXn_D0 input to FSITXn_TDM_D0 output	2	12	ns
FSIR_TDM4	$t_{skew(RX_D1-TX_TDM_D1)}$	Delay time, FSIRXn_D1 input to FSITXn_TDM_D1 output	2	12	ns

6.11.5.5.4 FSITX Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIT1	$t_{c(TX_CLK)}$	Cycle time, FSITXn_CLK	16.67		ns
FSIT2	$t_{w(TX_CLK)}$	Pulse width, FSITXn_CLK low or FSITXn_CLK high	0.5P(1) – 1	0.5P(1) + 1	ns
FSIT3	$td_{(TX_CLK-TX_D)}$	Delay time, FSITXn_Dx valid after FSITXn_CLK high or FSITXn_CLK low	0.25P(1) – 2	0.25P(1) + 2	ns
FSIT4	$t_{d(TXCLKL)}$	FSITXn_CLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
FSIT5	$t_{d(TX_D0)}$	FSITXn_D0 delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
FSIT6	$t_{d(TX_D1)}$	FSITXn_D1 delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
FSIT7	$t_{d(TX_DELAY_ELEMENT)}$	Incremental delay of each delay line element for FSITXn_CLK, FSITXn_D0, and FSITXn_D1	0.3	1	ns
FSIT_TDM1	$t_{skew(TX_TDM_CLK-TX_TDM_D)}$	Delay skew introduced between FSITXn_TDM_CLK delay and FSITXn_TDM_D[0:1] delays	–2.5	2.5	ns
FSIT_TDM2	$t_{skew(TX_TDM_CLK-TX_CLK)}$	Delay time, FSITXn_TDM_CLK input to FSITXn_CLK output	2	12	ns
FSIT_TDM3	$t_{skew(TX_TDM_D0-TX_D0)}$	Delay time, FSITXn_TDM_D0 input to FSITXn_D0 output	2	12	ns
FSIT_TDM4	$t_{skew(TX_TDM_D1-TX_D1)}$	Delay time, FSITXn_TDM_D1 input to FSITXn_D1 output	2	12	ns

(1) P = $t_{c(TX_CLK)}$ = FSITX Interface clock period in ns.

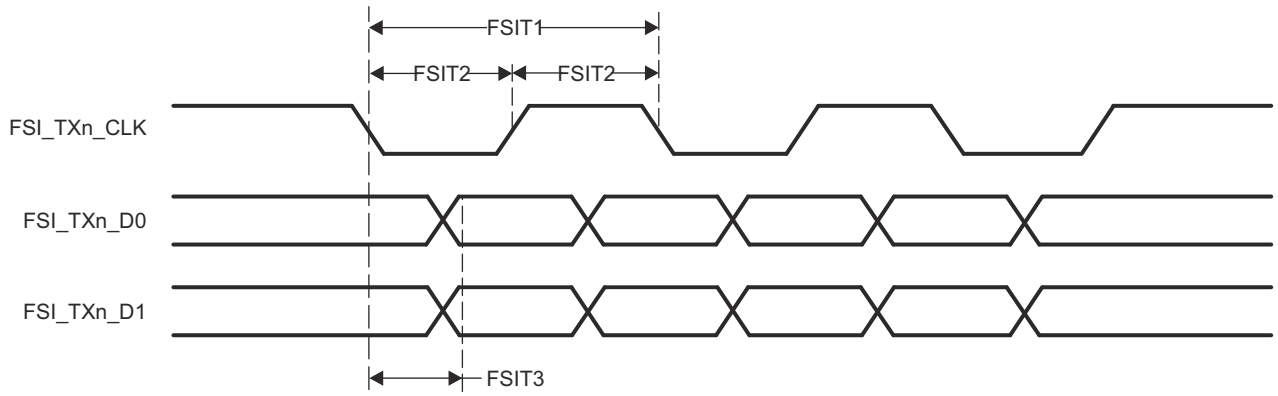

Figure 6-22. FSI Switching Characteristics - FSI Mode

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6.11.5.5.5 FSITX SPI Signaling Mode Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIT4	$t_{c(TX_CLK)}$	Cycle time, FSITXn_CLK	16.67		ns
FSIT5	$t_{w(TX_CLK)}$	Pulse width, FSITXn_CLK low or FSITXn_CLK high	0.5P(1) – 1	0.5P(1) + 1	ns
FSIT6	$t_{d(TX_CLKH–TX_D0)}$	Delay time, FSITXn_CLK high to FSITXn_D0 valid		3	ns
FSIT7	$t_{d(TX_D1-TX_CLK)}$	Delay time, FSITXn_D1 low to FSITXn_CLK high	P(1) – 3		ns
FSIT8	$t_{d(TX_CLK-TX_D1)}$	Delay time, FSITXn_CLK low to FSITXn_D1 high	P(1)		ns

(1) P = $t_{c(TX_CLK)}$ = FSITX Interface clock period in ns.

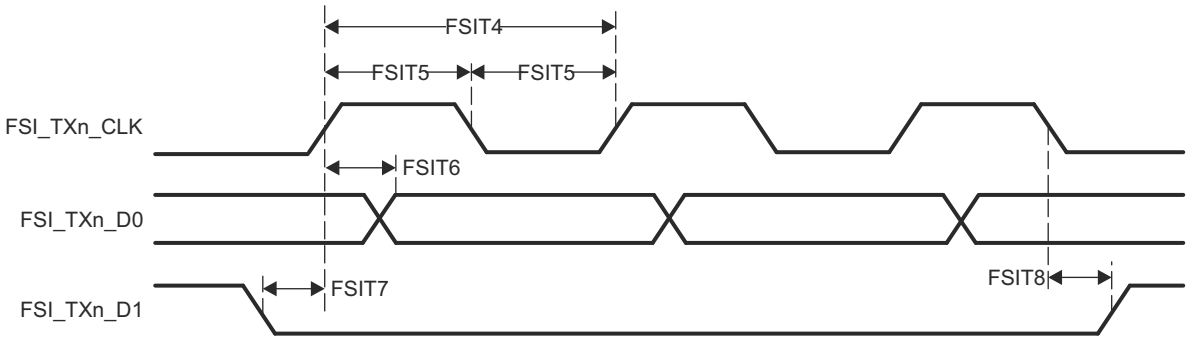

Figure 6-23. FSI Switching Characteristics - SPI Mode

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6.11.5.6 General Purpose Input/Output (GPIO)

For more details about features and additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *General-Purpose Interface (GPIO)* section in the device TRM.

6.11.5.6.1 GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		0.75	6.6	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	LVCMOS	3	10	pF
		I2C OD FS(1)	3	10	pF

(1) A pull-up resistor is required for buffer type *I2C OD FS*.

6.11.5.6.2 GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
D3	$t_{w(GPIO_IN)}$	Minimum Input Pulse Width	LVCMOS	2P(1) + 2		ns
D4			I2C OD FS(2)	2P(1) + 2		ns

(1) P = functional clock period in ns.
(2) A pull-up resistor is required for buffer type *I2C OD FS*.

6.11.5.6.3 GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
D1	$t_{w(GPIO_OUT)}$	Minimum Output Pulse Width	LVCMOS	0.975P(1) – 2		ns
D2	$t_{w(GPIO_OUT)}$	Minimum Output Pulse Width Low	I2C OD FS(2)	2P(1) + 160		ns
D3	$t_{w(GPIO_OUT)}$	Minimum Output Pulse Width High	I2C OD FS(2)	2P(1) + 160		ns

(1) P = functional clock period in ns.
(2) A pull-up resistor is required for buffer type *I2C OD FS*.

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6.11.5.7 Inter-Integrated Circuit (I^2C)

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see the *Inter-Integrated Circuit (I2C)* section in the device TRM.

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6.11.5.7.1 I2C

The device contains four multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I^{2}C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C1, I2C2, and I2C3
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- I2C0
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 3.3V
  - Exceptions:
    - The IOs associated with this port were not design to support Hs-mode.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8V/ns (or 8E+7V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8V/ns.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

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6.11.5.8 Local Interconnect Network (LIN)

Note

The device has multiple LIN modules. LINn is a generic prefix applied to LIN signal names, where n represents the specific LIN module.

For more information, see the *Local Interconnect Network (LIN) Module* section in the device TRM.

6.11.5.8.1 LIN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	20	pF

6.11.5.8.2 LIN Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LIN2	$t_{d(LINn_RX)}$	Delay time, LINn_RX shift register to LINn_RX pin	0	10	ns

6.11.5.8.3 LIN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LIN4	$t_{d(LINn_TX)}$	Delay time, LINn_TX shift register to LINn_TX pin		10	ns

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6.11.5.9 Modular Controller Area Network (MCAN)

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

For more information, see *Controller Area Network (MCAN)* section in the device TRM.

6.11.5.9.1 MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	20	pF

6.11.5.9.2 MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
M1	$t_{d(MCAN_TX)}$	Delay time, transmit shift register to MCANn_TX pin		10	ns
M2	$t_{d(MCAN_RX)}$	Delay time, MCANn_RX pin to receive shift register		10	ns

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6.11.5.10 Serial Peripheral Interface (SPI)

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple SPI modules. The generic SPI_ prefix is used to represent the signal names for all SPI instances.

For more information, see the *Serial Peripheral Interface (SPI)* section in the device TRM.

6.11.5.10.1 SPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	24	pF

6.11.5.10.2 SPI Controller Mode Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Normal Mode					
SM4	$t_{su(MISO-SPICLK)}$	Setup time, spi_d[x] valid before spi_sclk active edge	2		ns
SM5	$t_{h(SPICLK-MISO)}$	Hold time, spi_d[x] valid after spi_sclk active edge	3		ns

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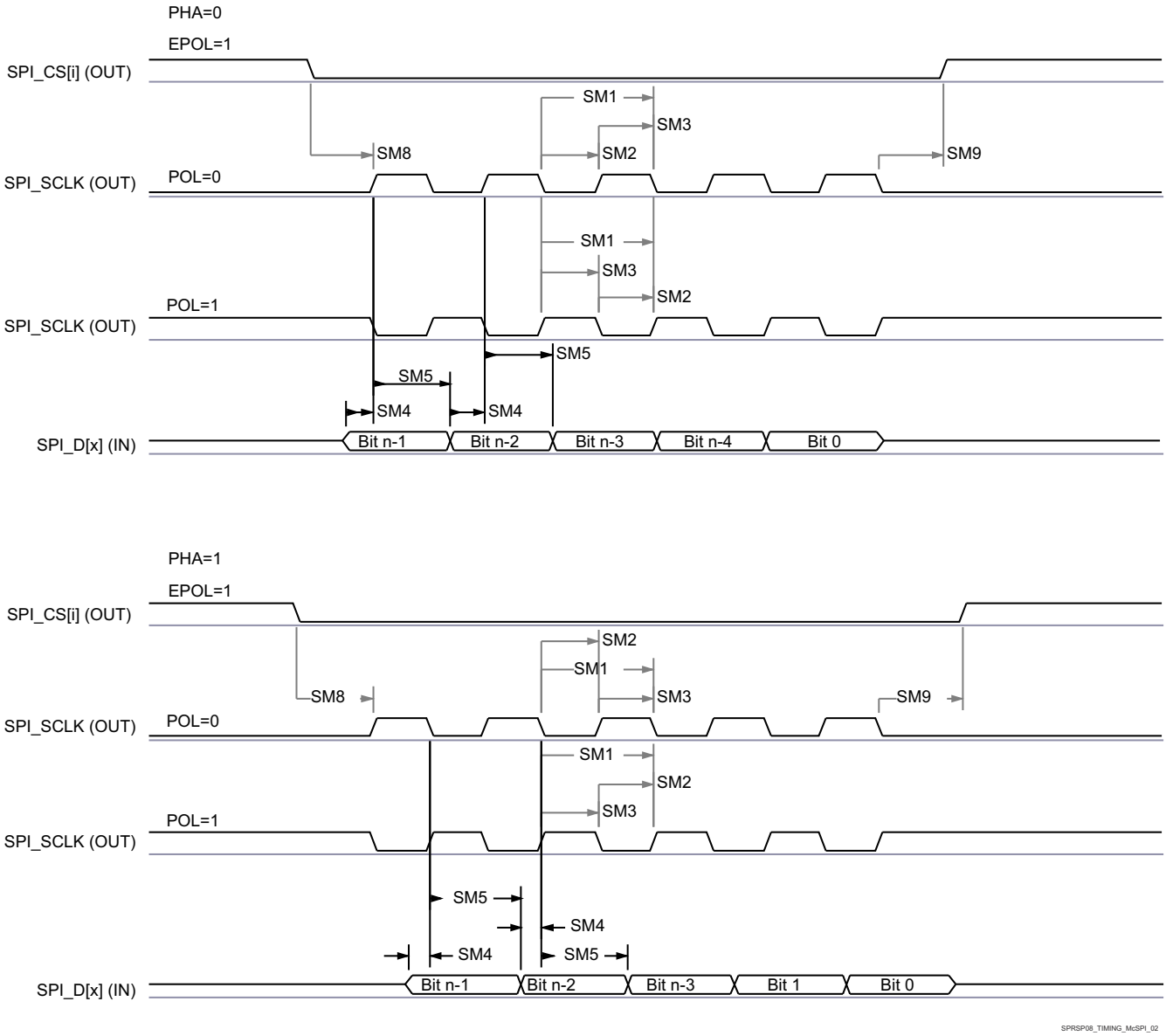

Figure 6-24. SPI Controller Mode Receive Timing

6.11.5.10.3 SPI Controller Mode Switching Characteristics (Clock Phase = 0)

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
Normal Mode						
SM1	$t_{c(SPICLK)}$	Cycle time, spi_sclk		20		ns
SM2	$t_{w(SPICLKL)}$	Typical Pulse duration, spi_sclk low		–1 + 0.5P[1]		ns
SM3	$t_{w(SPICLKH)}$	Typical Pulse duration, spi_sclk high		–1 + 0.5P[1]		ns
SM6	$t_{d(SPICLK-SIMO)}$	Delay time, spi_sclk active edge to spi_d[x] transition		–3	2	ns
SM7	$t_{sk(CS-SIMO)}$	Delay time, spi_cs[x] active to spi_d[x] transition		5		ns
SM8	$t_{d(SPICLK-CS)}$	Delay time, spi_cs[x] active to spi_sclk first edge	PHA = 0	–4 + B[3]		ns
			PHA = 1	–4 + A[2]		ns

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NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
SM9	$t_{d(SPICLK-CS)}$	Delay time, spi_sclk last edge to spi_cs[x] inactive	PHA = 0	–4 + A(2)		ns
			PHA = 1	–4 + B(3)		ns

(1) P = SPICLK period in ns.
(2) When P = 20.8ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(3) B = (TCS + .5) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even >= 2.

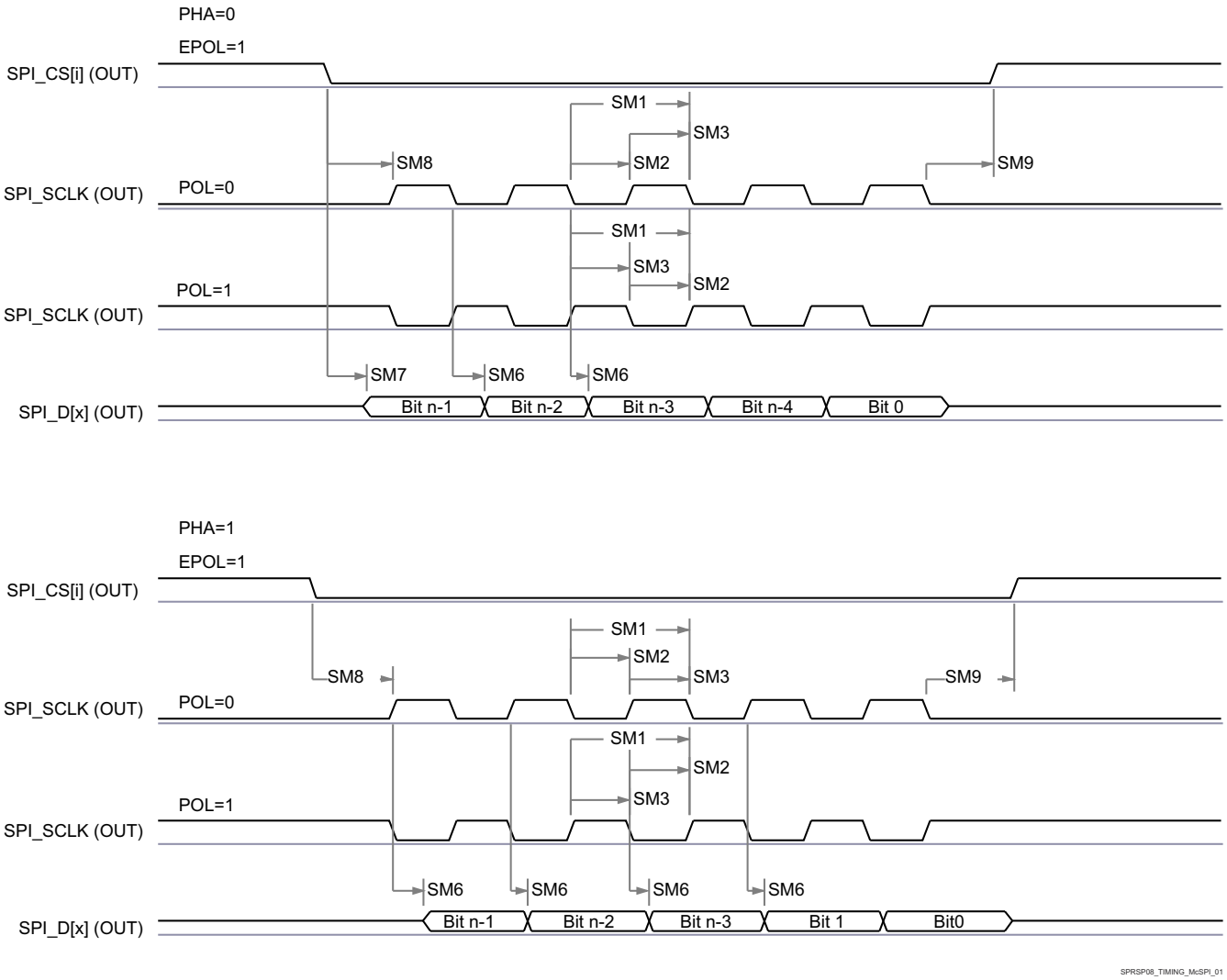

Figure 6-25. SPI Controller Mode Transmit Timing

6.11.5.10.4 SPI Peripheral Mode Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, spi_sclk	40		ns
SS2	$t_{w(SPICLKL)}$	Typical Pulse duration, spi_sclk low	0.45 × P(1)		ns
SS3	$t_{w(SPICLKH)}$	Typical Pulse duration, spi_sclk high	0.45 × P(1)		ns
SS4	$t_{su(SIMO-SPICLK)}$	Setup time, spi_d[x] valid before spi_sclk active edge	5		ns
SS5	th(SPICLK-SIMO)	Hold time, spi_d[x] valid after spi_sclk active edge	5		ns

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NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS8	$t_{su(CS-SPICLK)}$	Setup time, spi_cs[x] valid before spi_sclk first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, spi_cs[x] valid after spi_sclk last edge	5		ns

(1) P = SPICLK period.

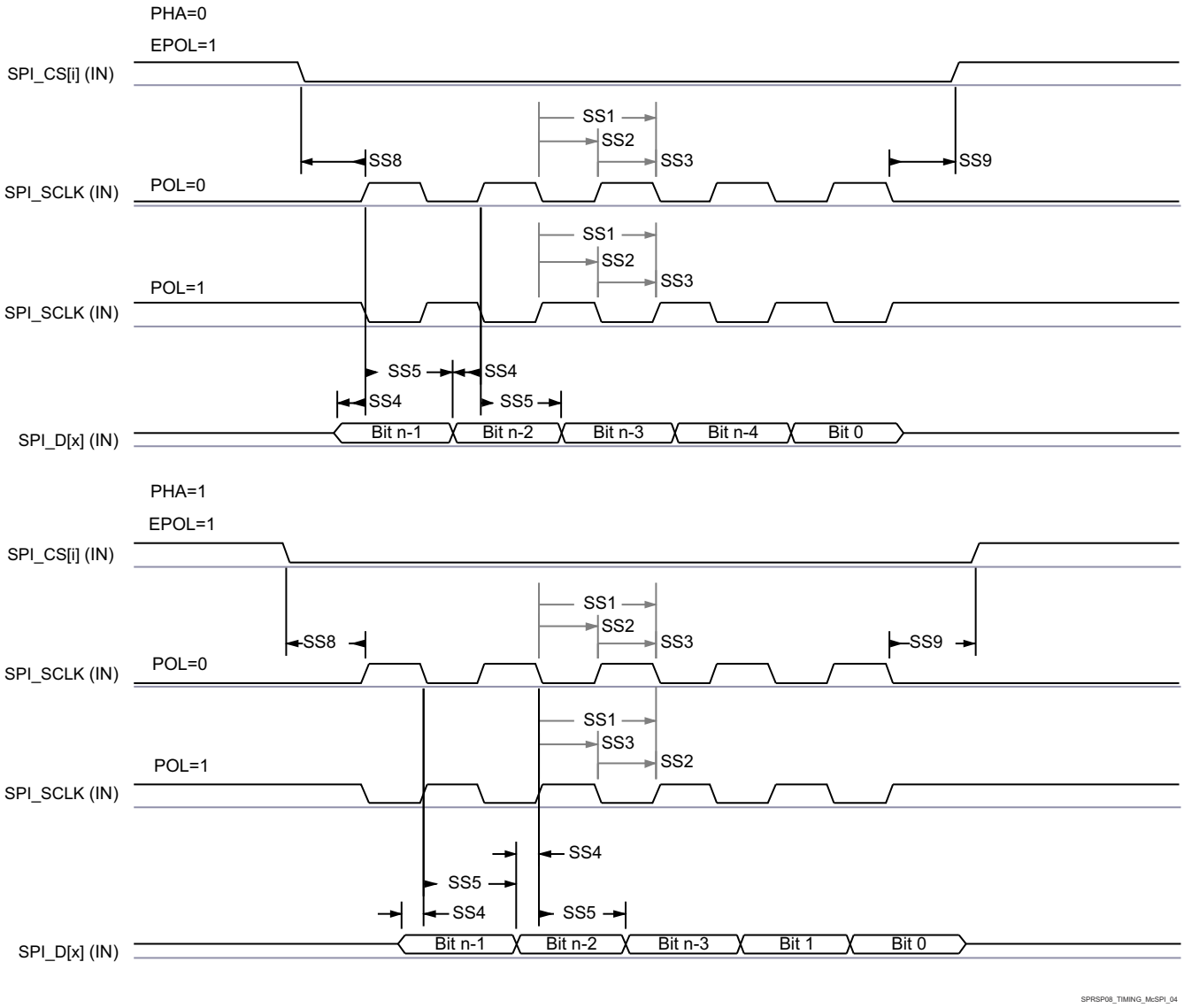

Figure 6-26. SPI Peripheral Mode Receive Timing

6.11.5.10.5 SPI Peripheral Mode Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Normal Mode					
SS6	$t_{d(SPICLK-SOMI)}$	Delay time, spi_sclk active edge to mcspi_somi transition	2	17.12	ns
SS7	$t_{sk(CS-SOMI)}$	Delay time, spi_cs[x] active edge to mcspi_somi transition	20.95		ns

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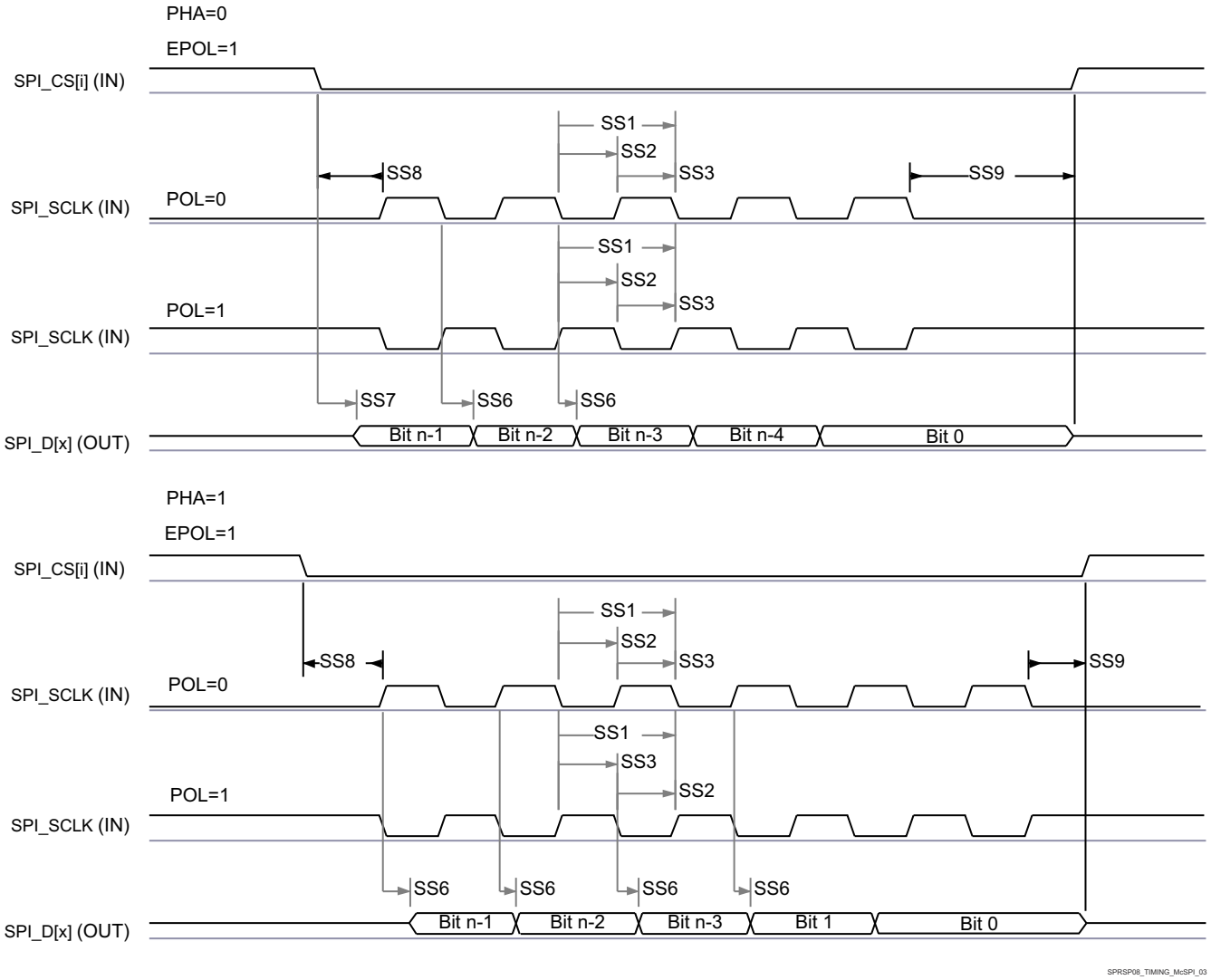

Figure 6-27. SPI Peripheral Mode Transmit Timing

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6.11.5.11 Multi-Media Card/Secure Digital (MMCSD)

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC) and Secure Digital (SD)devices. The MMCSD Host Controller deals with MMC/SD protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC subsection within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

6.11.5.11.1 MMC Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	Default Speed	0.69	2.06	V/ns
		High Speed	0.69	2.06	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	Default Speed	1	10	pF
		High Speed	1	10	pF

6.11.5.11.2 MMC Timing Requirements - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	19.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[3:0] valid before MMC_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[3:0] valid after MMC_CLK rising edge	19.67		ns

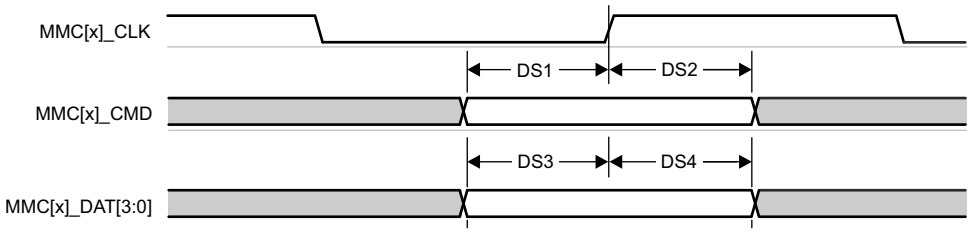

Figure 6-28. MMC – Default Speed – Receive Mode

6.11.5.11.3 MMC Switching Characteristics - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		25	MHz
DS5	$t_{c(clk)}$	Operating period, MMC_CLK		40	ns
DS6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	–14.1	14.1	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition	–14.1	14.1	ns

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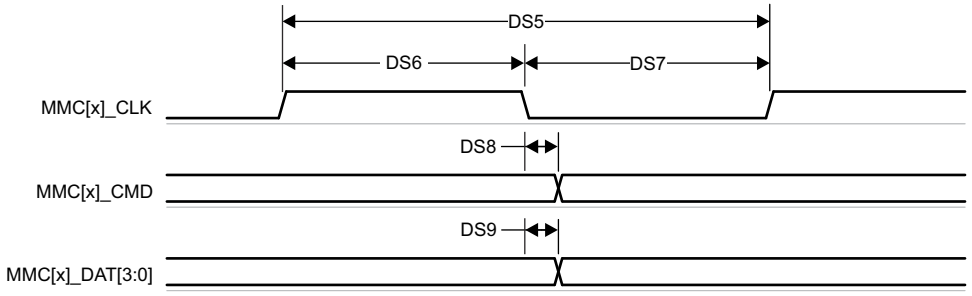

Figure 6-29. MMC – Default Speed – Transmit Mode

6.11.5.11.4 MMC Timing Requirements - SD Card High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	2.15		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	2.67		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[3:0] valid before MMC_CLK rising edge	2.15		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[3:0] valid after MMC_CLK rising edge	2.67		ns

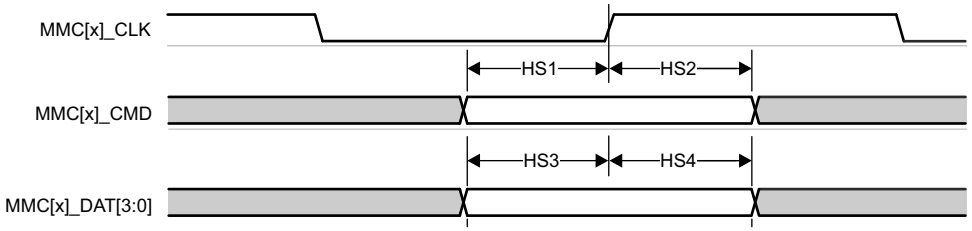

Figure 6-30. MMC – High Speed – Receive Mode

6.11.5.11.5 MMC Switching Characteristics - SD Card High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		50	MHz
HS5	$t_{c(clk)}$	Operating period, MMC_CLK		20	ns
HS6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	–7.35	3.35	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition	–7.35	3.35	ns

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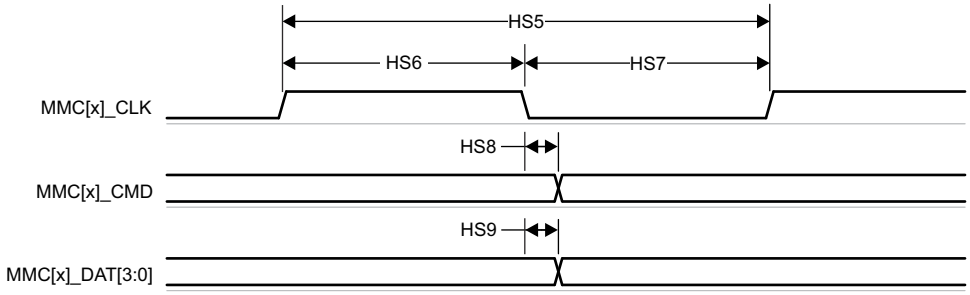

Figure 6-31. MMC – High Speed – Transmit Mode

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6.11.5.12 Octal Serial Peripheral Interface (OSPI)

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0_CLK for Double Data Rate (DDR) transfers. PHY mode supports three clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_LBCLKO pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200MHz, which produces an OSPI0_CLK rate up to 50MHz for SDR mode or 25MHz for DDR mode.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

OSPI PHY Mode defines timing requirements and switching characteristics associated with PHY mode and *OSPI Tap Mode* defines timing requirements and switching characteristics associated with Tap mode.

OSPI Timing Conditions presents timing conditions for OSPI0.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in the device TRM.

6.11.5.12.1 OSPI Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	15	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[1:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

6.11.5.12.2 OSPI PHY Mode

6.11.5.12.2.1 OSPI0 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

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Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

6.11.5.12.2.1.1 OSPI DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

6.11.5.12.2.1.2 OSPI Timing Requirements - PHY Data Training

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns

(1) Minimum setup and hold time requirements for OSPI0_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window.

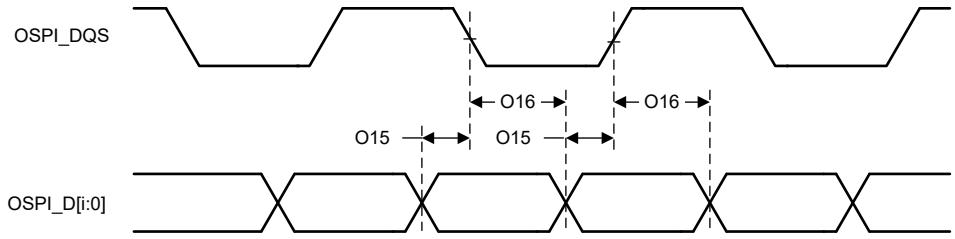

Figure 6-32. . OSPI0 Timing Requirements – PHY Data Training, DDR with DQS

6.11.5.12.2.1.3 OSPI Switching Characteristics - PHY Data Training

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	3.3V, DDR	7.52		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low	DDR	0.475P(1) - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high	DDR	0.475P(1) - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge	DDR	0.475P(1) + (0.975 × M(2) × R(4)) + 0.65TD(5) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 0.175TD(5) + 1	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge	DDR	0.475P(1) + (0.975 × N(3) × R(4)) - 0.65TD(5) - 1	0.525P(1) + (1.025 × N(3) × R(4)) - 0.175TD(5) + 1	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	DDR	(6)	(6)	ns

(1) P = OSPI0_CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window.

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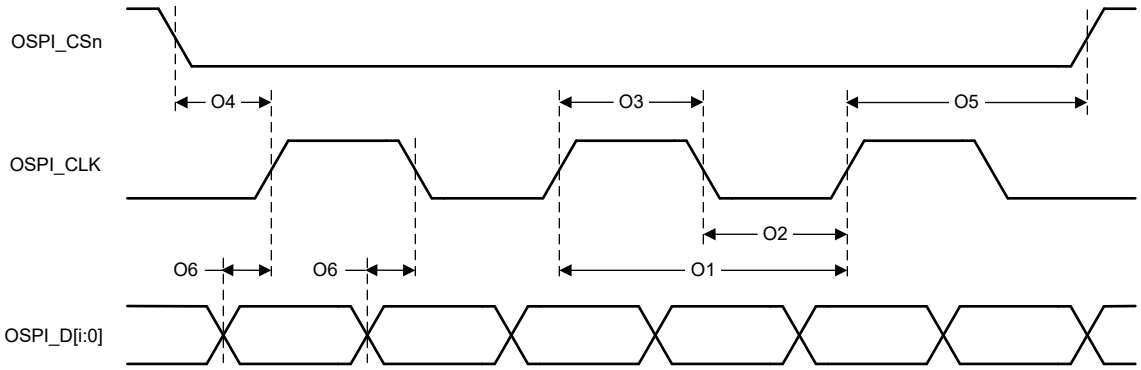

Figure 6-33. OSPI0 Switching Characteristics – PHY DDR Data Training

6.11.5.12.2.2 OSPI0 Without Data Training

Note

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in *OSPI DLL Delay Mapping for PHY SDR Timing Modes* and *OSPI DLL Delay Mapping for PHY DDR Timing Modes*.

6.11.5.12.2.2.1 OSPI0 PHY SDR Timing

6.11.5.12.2.2.1.1 OSPI DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	0x0
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

6.11.5.12.2.2.1.2 OSPI Timing Requirements - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	3.3V, SDR with Internal PHY Loopback	TBD		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	3.3V, SDR with Internal PHY Loopback	TBD		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	3.3V, SDR with External Board Loopback	TBD		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	3.3V, SDR with External Board Loopback	TBD		ns

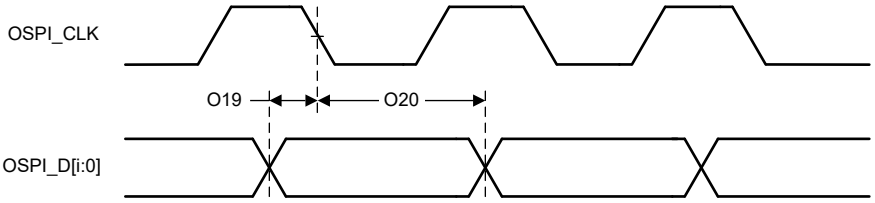

Figure 6-34. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback

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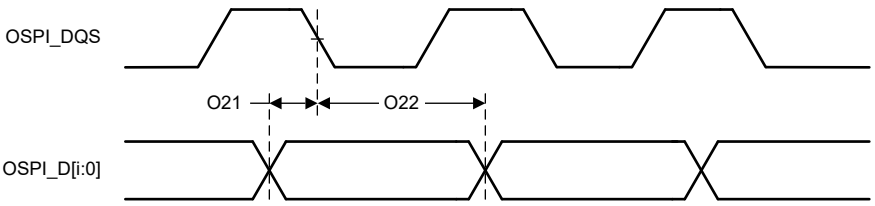

Figure 6-35. OSPI0 Timing Requirements – PHY SDR with External Board Loopback

6.11.5.12.2.2.1.3 OSPI Switching Characteristics - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	3.3V	6.03		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P(1) - 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P(1) - 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		TBD	TBD	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		TBD	TBD	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	3.3V	TBD	TBD	ns

(1) P = CLK cycle time = SCLK period in ns

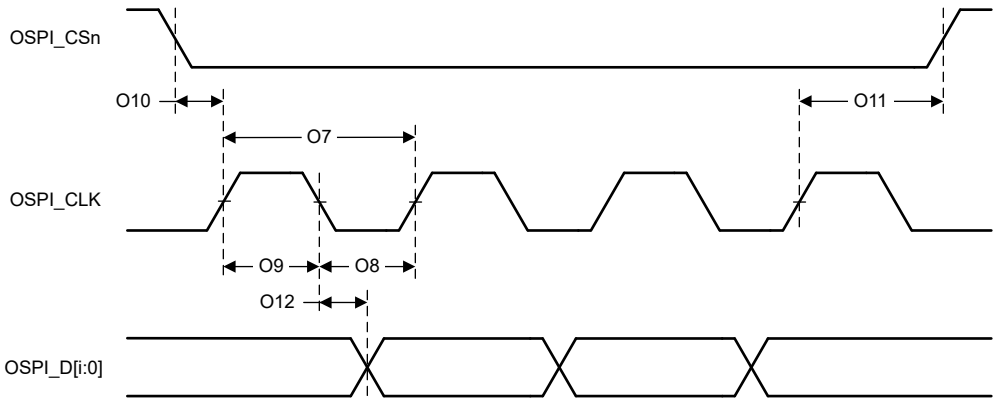

Figure 6-36. OSPI0 Switching Characteristics – PHY SDR

6.11.5.12.2.2.2 OSPI0 PHY DDR Timing

6.11.5.12.2.2.2.1 OSPI DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	TBD
Receive		
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	TBD
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	TBD

6.11.5.12.2.2.2.2 OSPI Timing Requirements - PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	3.3V, DDR with DQS	TBD		ns

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NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O16	$t_{h(LBTCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	3.3V, DDR with DQS	TBD		ns

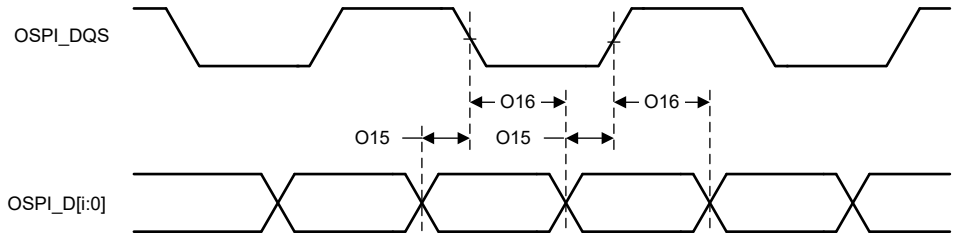

Figure 6-37. OSPI0 Timing Requirements – PHY DDR with External Board Loopback or DQS

6.11.5.12.2.2.3 OSPI Switching Characteristics - PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		19		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P(1) - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P(1) - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		TBD	TBD	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		TBD	TBD	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	3.3V	TBD	TBD	ns

(1) P = OSPI0_CLK cycle time = SCLK period in ns

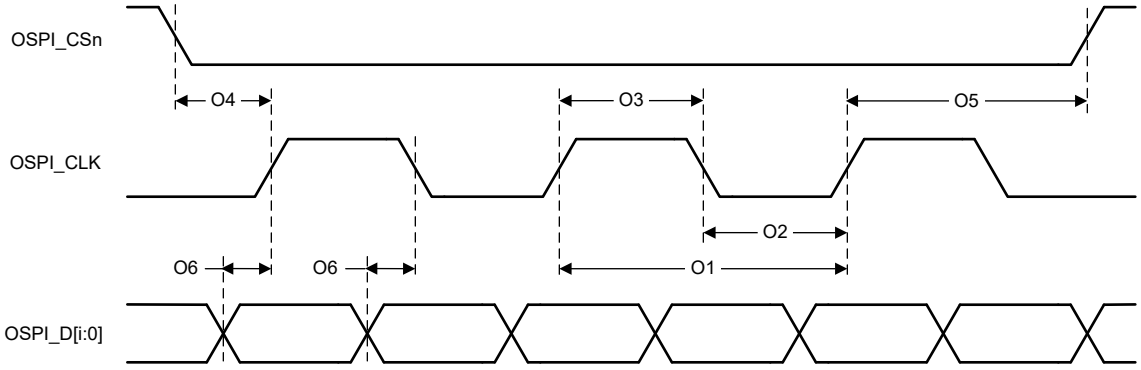

Figure 6-38. OSPI0 Switching Characteristics – PHY DDR

6.11.5.12.3 OSPI Tap Mode

6.11.5.12.3.1 OSPI0 Tap SDR Timing

6.11.5.12.3.1.1 OSPI Timing Requirements - Tap SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	10.4 - (0.975 × T(1) × R(2))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	0.7 + (0.975 × T(1) × R(2))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]

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(2) R = REFCLK cycle time in ns

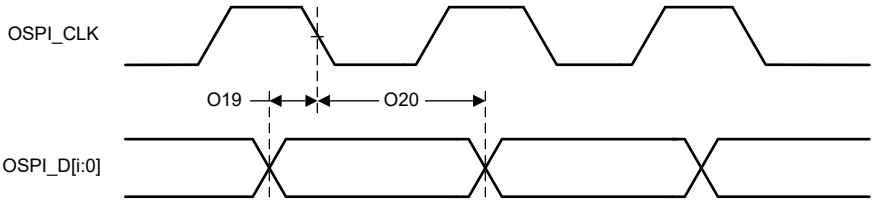

Figure 6-39. OSPI0 Timing Requirements – Tap SDR, No Loopback

6.11.5.12.3.1.2 OSPI Switching Characteristics - Tap SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P(1) - 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P(1) - 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		0.475P(1) + (0.975 × M(2) × R(4)) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 1	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 1	0.525P(1) + (1.025 × N(3) × R(4)) + 1	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		–4.25	7.25	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

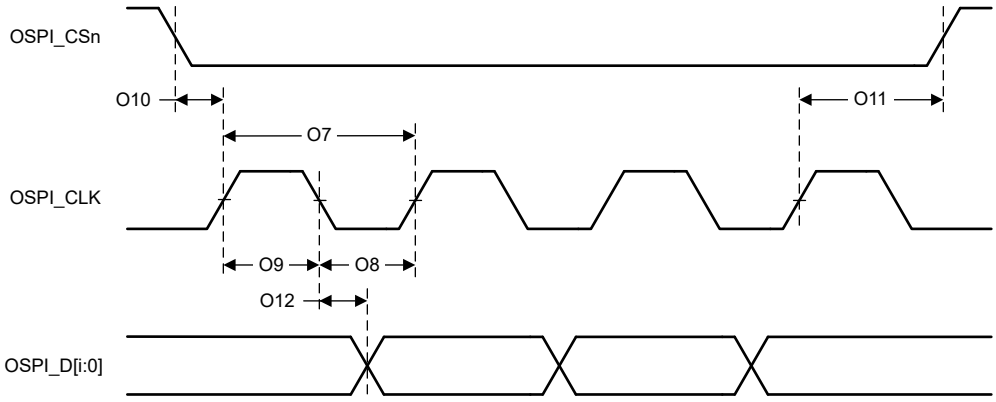

Figure 6-40. OSPI0 Switching Characteristics – Tap SDR, No Loopback

6.11.5.12.3.2 OSPI0 Tap DDR Timing

6.11.5.12.3.2.1 OSPI Timing Requirements - Tap DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	12.04 - (0.975 × T(1) × R(2))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	1.84 + (0.975 × T(1) × R(2))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = REFCLK cycle time in ns

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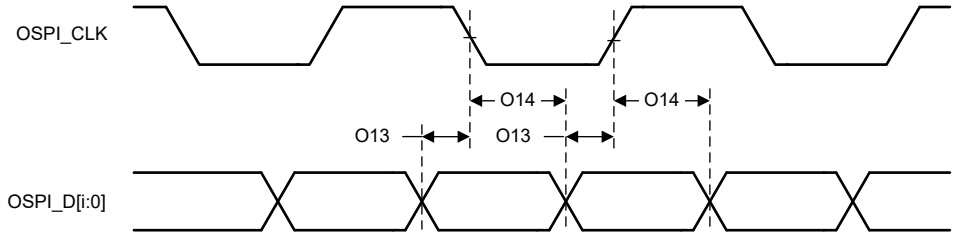

Figure 6-41. OSPI0 Timing Requirements – Tap DDR, No Loopback

6.11.5.12.3.2.2 OSPI Switching Characteristics - Tap DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P(1) - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P(1) - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		0.475P(1) + (0.975 × M(2) × R(4)) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 1	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 1	0.525P(1) + (1.025 × N(3) × R(4)) + 1	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		–17.94 + (0.975 × T(5) × R(4))	–1.56 + (1.025 × T(5) × R(4))	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns
(5) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]

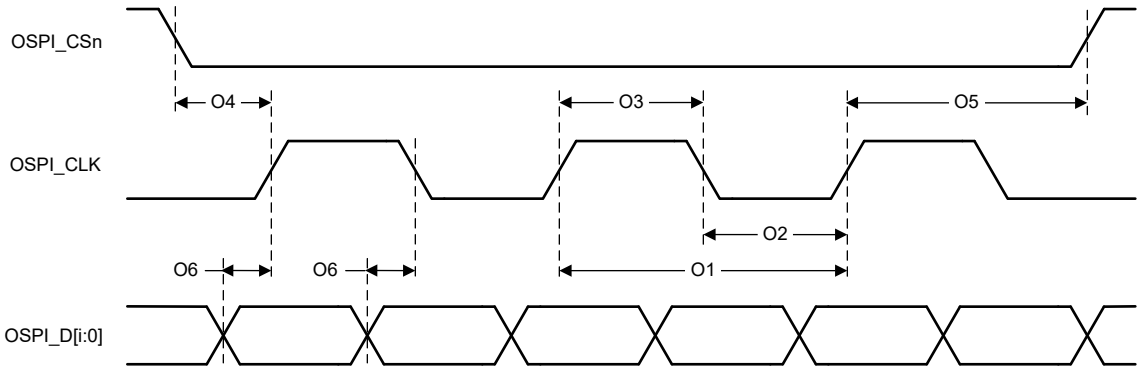

Figure 6-42. OSPI0 Switching Characteristics – Tap DDR, No Loopback

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6.11.5.13 Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)

The device has integrated a single Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS0). The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores in the device.

For more details about features and additional description information on the device PRU-ICSS, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The PRU-ICSS0 supports an internal wrapper multiplexing that expands the device top-level multiplexing.

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6.11.5.13.1 PRU-ICSS Programmable Real-Time Unit (PRU)

Note

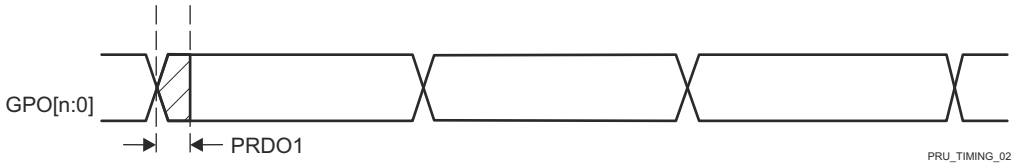
The PRU-ICSS PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

6.11.5.13.1.1 PRU-ICSS PRU Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	30	pF

6.11.5.13.1.2 PRU-ICSS PRU Switching Characteristics - Direct Output Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDO1	$t_{sk(PRU_GPO)}$	PRU_GPO (data out) skew		3	ns



A. n in GPO[n:0] = 19.

Figure 6-43. PRU-ICSS PRU Direct Output Timing

6.11.5.13.1.3 PRU-ICSS PRU Timing Requirements - Parallel Capture Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC1	$t_{c(PRU_CLOCK)}$	Cycle time, PRU_CLOCK	20		ns
PRPC2	$t_{w(PRU_CLOCKL}$	Pulse duration, PRU_CLOCK Low	10		ns
PRPC3	$t_{w(PRU_CLOCKH)}$	Pulse duration, PRU_CLOCK High	10		ns
PRPC4	$t_{su(PRU_DATAIN-PRU_CLK)}$	Setup time, PRU_DATAIN valid before PRU_CLOCK active edge	4		ns
PRPC5	$t_{th(PRU_CLOCK-PRU_DATAIN)}$	Hold time, PRU_DATAIN valid after PRU_CLOCK active edge	0		ns

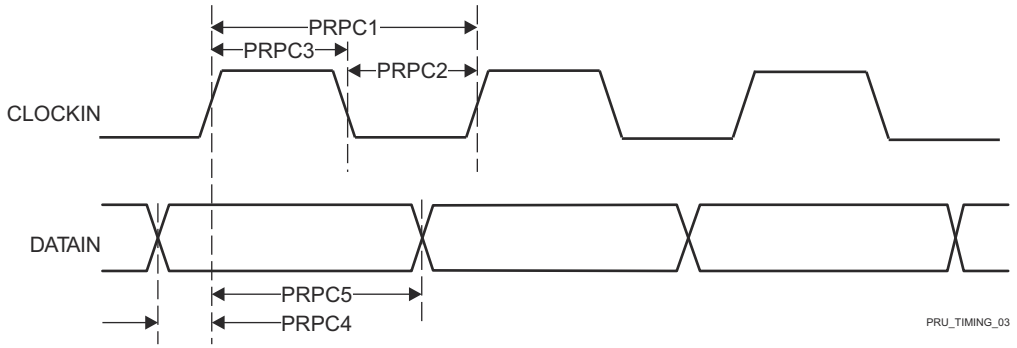


Figure 6-44. PRU-ICSS PRU Parallel Capture Timing Requirements – Rising Edge Mode

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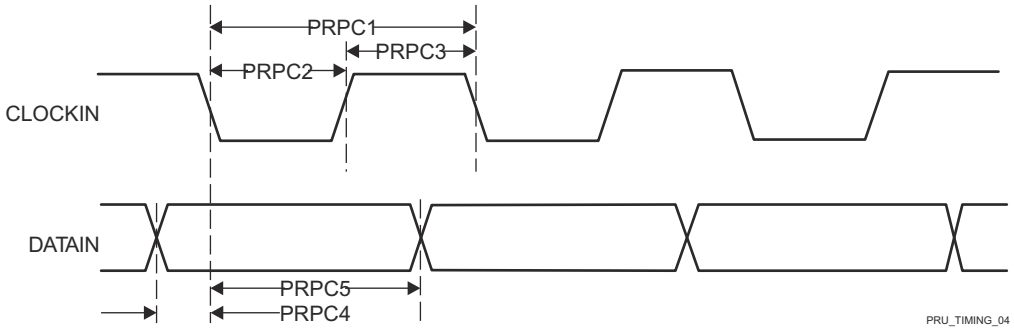

Figure 6-45. PRU-ICSS PRU Parallel Capture Timing Requirements – Falling Edge Mode

6.11.5.13.1.4 PRU-ICSS PRU Timing Requirements - Shift In Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSI1	$t_{w(PRU_DATAINH)}$	Pulse duration, PRU_DATAIN High	2 + 2P(1)		ns
PRSI2	$t_{w(PRU_DATAINL)}$	Pulse duration, PRU_DATAIN Low	2 + 2P(1)		ns

(1) P = Internal shift in clock period, defined by PRU_GPI_DIV0 and PRU0_GPI_DIV1 bit fields in the GPCFGn register.

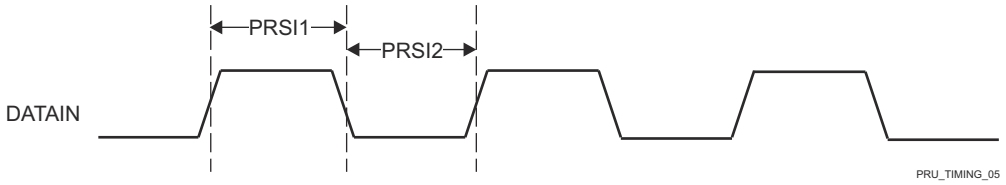

Figure 6-46. PRU-ICSS PRU Shift In Timing

6.11.5.13.1.5 PRU-ICSS PRU Switching Characteristics - Shift Out Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO1	$t_{c(PRU_CLOCKOUT)}$	Cycle time, PRU_CLOCKOUT	10		ns
PRSO2L	$t_{w(PRU_CLOCKOUTL)}$	Pulse duration, PRU_CLOCKOUT Low	–0.3 + 0.475 × P(1) × Z(2)		ns
PRSO2H	$t_{w(PRU_CLOCKOUTH)}$	Pulse duration, PRU_CLOCKOUT High	–0.3 + 0.475 × P(1) × Y(3)		ns
PRSO3	$t_{d(PRU_CLOCKOUT-PRU_DATAOUT)}$	Delay time, PRU_CLOCKOUT to PRU_DATAOUT Valid	0	3	ns

(1) P = Software programmable shift out clock period, defined by PRU0_GP0_Div0 and PRU0_GPO_DIV1 bit fields in the GPCFGn register.

(2) The Z parameter is defined as follows:
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are INTEGERS -or- if PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an EVEN INTEGER then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1).
If PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an ODD INTEGER then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.5).
If PRU0_GPI_DIV0 is an INTEGER and PRU0_GPI_DIV1 is a NON-INTEGER then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.5 * PRU0_GPI_DIV0).
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are NON-INTEGERS then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.25 * PRU0_GPI_DIV0).

(3) The Y parameter is defined as follows:
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are INTEGERS -or- if PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an EVEN INTEGER then,
Y equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1).
If PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an ODD INTEGER then,
Y equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 - 0.5).
If PRU0_GPI_DIV0 is an INTEGER and PRU0_GPI_DIV1 is a NON-INTEGER then,
Y equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 - 0.5 * PRU0_GPI_DIV0).
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are NON-INTEGERS then,
Y1 equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 - 0.25 * PRU0_GPI_DIV0) and

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Y2 equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.25 * PRU0_GPI_DIV0), where Y1 is the first high pulse and Y2 is the second high pulse.

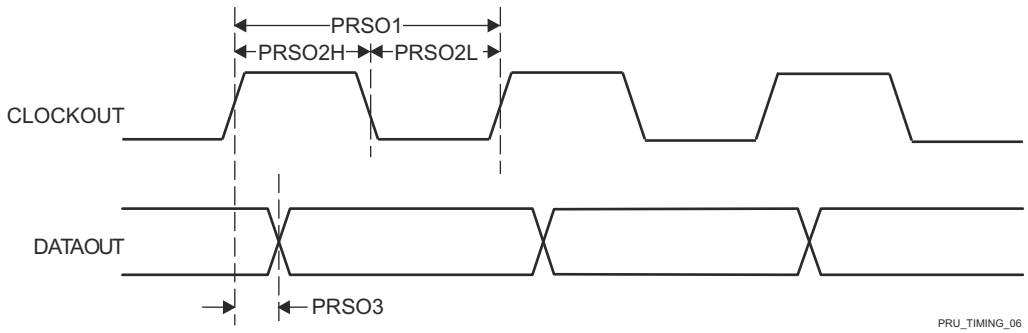

Figure 6-47. PRU-ICSS PRU Shift Out Timing

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6.11.5.13.2 PRU-ICSS PRU Sigma Delta and Peripheral Interface

6.11.5.13.2.1 PRU-ICSS PRU Sigma Delta and Peripheral Interface Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	18	pF

6.11.5.13.2.2 PRU-ICSS PRU Timing Requirements - Sigma Delta Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSD1	$t_{c(SD_CLK)}$	Cycle time, SD_CLK	40		ns
PRSD2L	$t_{w(SD_CLKL)}$	Pulse duration, SD_CLK Low	20		ns
PRSD2H	$t_{w(SD_CLKH)}$	Pulse duration, SD_CLK High	20		ns
PRSD3	$t_{su(SD_D-SDCLK)}$	Setup time, SD_D valid before SD_CLK active edge	10		ns
PRSD4	$t_{su(SDCLK-SD_D)}$	Hold time, SD_D valid after SD_CLK active edge	5		ns

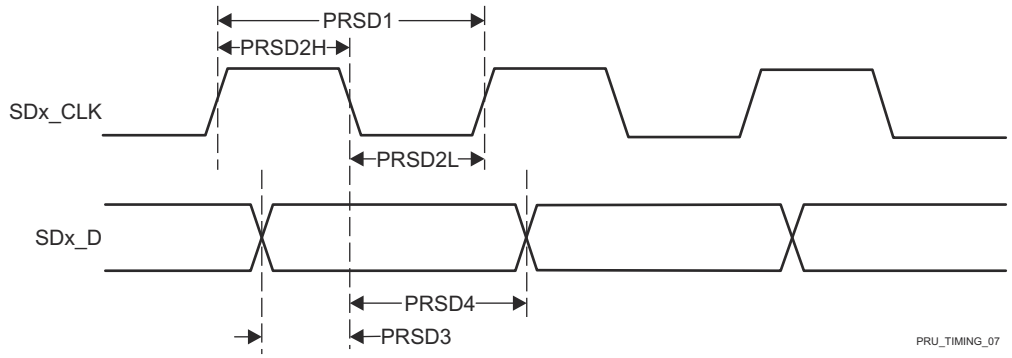

Figure 6-48. PRU-ICSS PRU SD_CLK Falling Active Edge

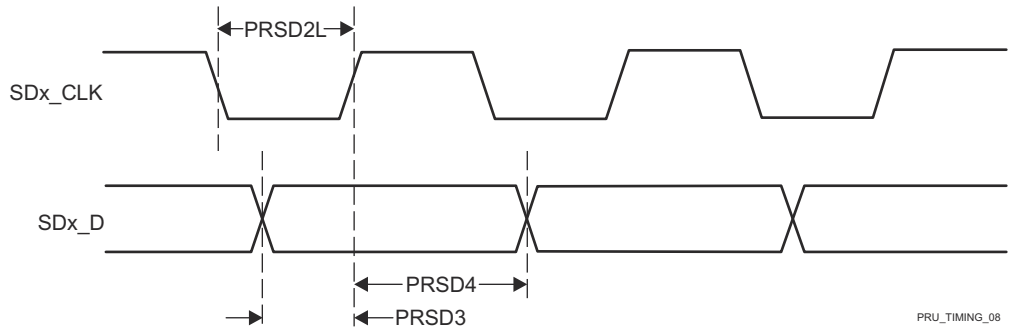

Figure 6-49. PRU-ICSS PRU SD_CLK Rising Active Edge

6.11.5.13.2.3 PRU-ICSS PRU Timing Requirements - Peripheral Interface Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF1	$t_{w(PIF_DATA_INH)}$	Pulse duration, PIF_DATA_IN High	2 + 0.475 × (4 × P(1))		ns
PRPIF2	$t_{w(PIF_DATA_INL)}$	Pulse duration, PIF_DATA_IN Low	2 + 0.475 × (4 × P(1))		ns

(1) P = 1x (or TX) clock period, defined by TX_DIV_FACTOR and TX_DIV_FACTOR_FRAC in the CFG_ED_P<n>_TXCFG register.

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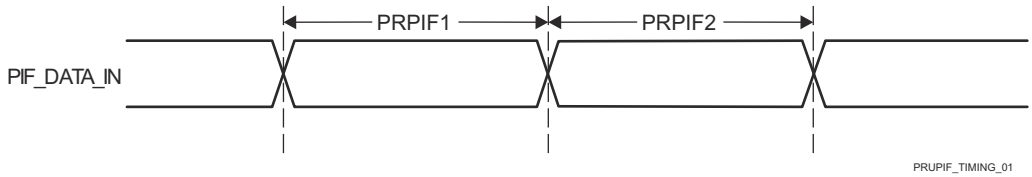

Figure 6-50. PRU-ICSS PRU Peripheral Interface Timing Requirements

6.11.5.13.2.4 PRU-ICSS PRU Switching Characteristics - Peripheral Interface Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF3	$t_{c(PIF_CLK)}$	Cycle time, PIF_CLK	30		ns
PRPIF4	$t_{w(PIF_CLKH)}$	Pulse duration, PIF_CLK High	0.475P(1)		ns
PRPIF5	$t_{w(PIF_CLKL)}$	Pulse duration, PIF_CLK Low	0.475P(1)		ns
PRPIF6	$t_{d(PIF_CLK-PIF_DATA_OUT)}$	Delay time, PIF_CLK fall to PIF_DATA_OUT	–5	5	ns
PRPIF7	$t_{d(PIF_CLK-PIF_DATA_EN)}$	Delay time, PIF_CLK fall to PIF_DATA_EN	–5	5	ns

(1) P = 1x (or TX) clock period, defined by TX_DIV_FACTOR and TX_DIV_FACTOR_FRAC in the CFG_ED_P<n>_TXCFG register.

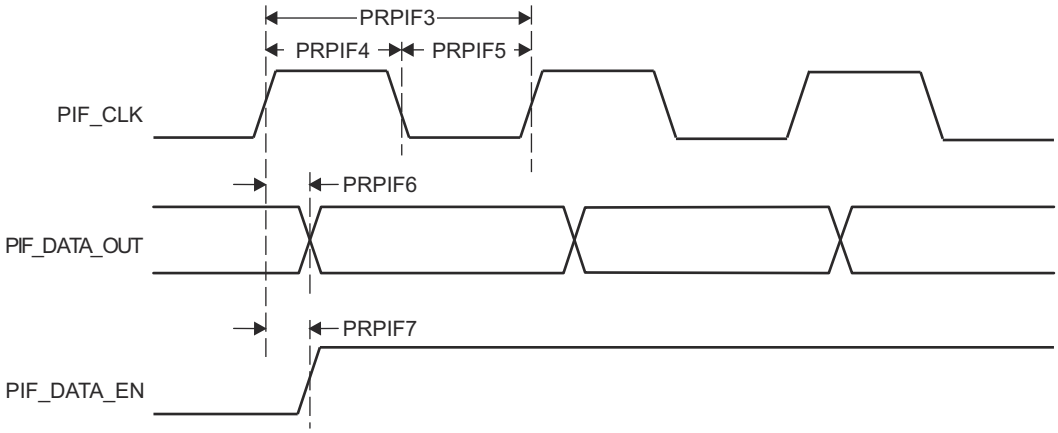

Figure 6-51. PRU-ICSS PRU Peripheral Interface Switching Characteristics

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6.11.5.13.3 PRU-ICSS Pulse Width Modulation (PWM)

6.11.5.13.3.1 PRU-ICSS PWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.13.3.2 PRU-ICSS PWM Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPWM1	$t_{sk(PWM_A/B)}$	PWM_A/B skew		5	ns

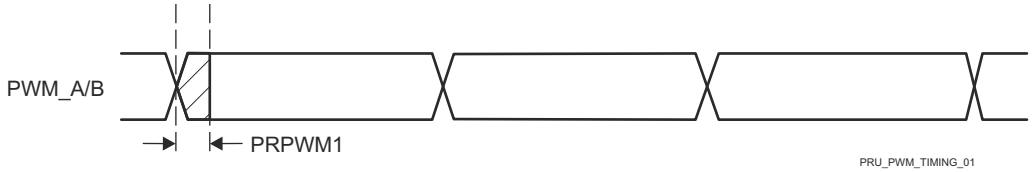

Figure 6-52. PRU-ICSS PWM Timing

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6.11.5.13.4 PRU-ICSS Industrial Ethernet Peripheral (IEP)

6.11.5.13.4.1 PRU-ICSS IEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	7	pF

6.11.5.13.4.2 PRU-ICSS IEP Timing Requirements - Input Validated with SYNCx

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRIEP1	$t_{w(EDC_SYNCx_OUTL)}$	Pulse duration, EDC_SYNCx_OUT Low	–2 + 20P(1)		ns
PRIEP2	$t_{w(EDC_SYNCx_OUTH)}$	Pulse duration, EDC_SYNCx_OUT High	–2 + 20P(1)		ns
PRIEP3	$t_{su(EDIO_DATA_IN-EDC_SYNCx_OUT}$	Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge	20		ns
PRIEP4	$t_{h(EDC_SYNCx_OUT-EDIO_DATA_IN)}$	Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge	20		ns

(1) P = PRU-ICSS IEP clock source period.

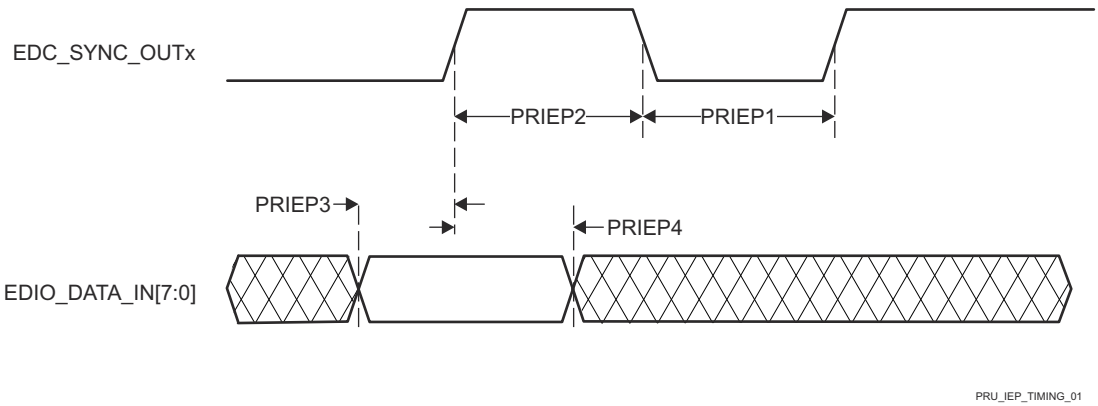

Figure 6-53. PRU-ICSS IEP SYNC Timing Requirements

6.11.5.13.4.3 PRU-ICSS IEP Timing Requirements - Digital IOs

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
IEPIO1	$t_{w(EDIO_OUTVALIDL)}$	Pulse duration, EDIO_OUTVALID Low	–2 + 14P(1)		ns
IEPIO2	$t_{w(EDIO_OUTVALIDH)}$	Pulse duration, EDIO_OUTVALID High	–2 + 32P(1)		ns
IEPIO3	$t_{d(EDIO_OUTVALID-EDIO_DATA_OUT)}$	Delay time, EDIO_OUTVALID to EDIO_DATA OUT	0	18P(1)	ns
IEPIO4	$t_{sk(EDIO_DATA_OUT)}$	EDIO_DATA_OUT skew	6		ns

(1) P = PRU-ICSS IEP clock source period.

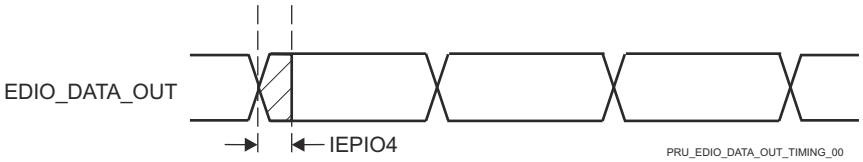

Figure 6-54. PRU-ICSS IEP Digital IOs Timing Requirements

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6.11.5.13.4.4 PRU-ICSS IEP Timing Requirements - LATCHx_IN

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRLA1	$t_{w(EDC_LATCHx_INL)}$	Pulse duration, EDC_LATCHx_IN Low	2 + 3P[1]		ns
PRLA2	$t_{w(EDC_LATCHx_INH)}$	Pulse duration, EDC_LATCHx_IN High	2 + 3P[1]		ns

(1) P = PRU-ICSS IEP clock source period.

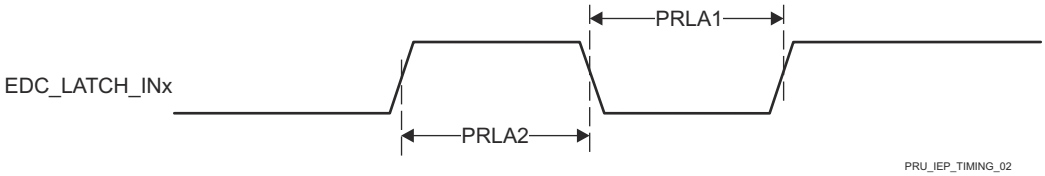

Figure 6-55. PRU-ICSS IEP LATCH_INx Timing Requirements

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6.11.5.13.5 PRU-ICSS Universal Asynchronous Receiver Transmitter (UART)

6.11.5.13.5.1 PRU-ICSS UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.01	0.33	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	30	pF

6.11.5.13.5.2 PRU-ICSS UART Timing Requirements

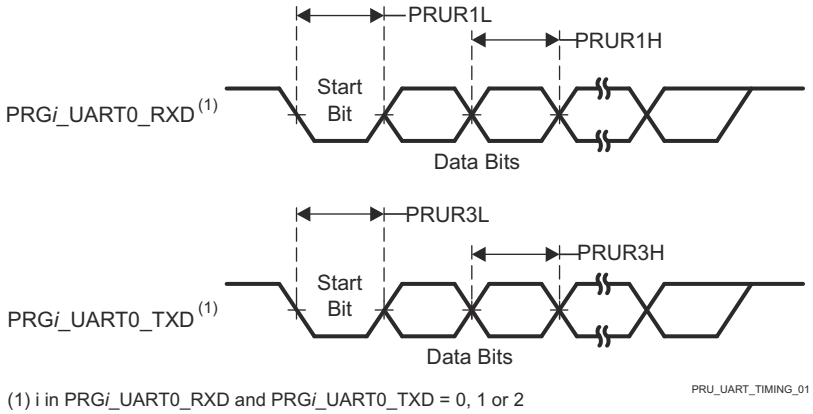
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR1H	$t_{w(RXH)}$	Pulse duration, Receive start, stop, data bit High	U(1)		ns
PRUR1L	$t_{w(RXL)}$	Pulse duration, Receive start, stop, data bit Low	–2 + U(1)		ns

(1) U = UART baud time = 1/programmed baud rate.

6.11.5.13.5.3 PRU-ICSS UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR2	$f_{(baud)}$	Maximum programmable baud rate	U(1)		ns
PRUR3H	$t_{w(TXH)}$	Pulse duration, Transmit start, stop, data bit High	–2 + U(1)		ns

(1) U = UART baud time = 1/programmed baud rate.



(1) i in PRG*i*_UART0_RXD and PRG*i*_UART0_TXD = 0, 1 or 2

Figure 6-56. PRU-ICSS UART Timing Requirements and Switching Characteristics

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6.11.5.13.6 PRU-ICSS Enhanced Capture Peripheral (ECAP)

6.11.5.13.6.1 PRU-ICSS ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.13.6.2 PRU-ICSS ECAP Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP1	$t_{w(CAP)}$	Pulse duration, Capture input (asynchronous)	2 + 2P(1)		ns
PREP2	$t_{w(SYNCI)}$	Pulse duration, Sync input (asynchronous)	2 + 2P(1)		ns

(1) P = core_clk period

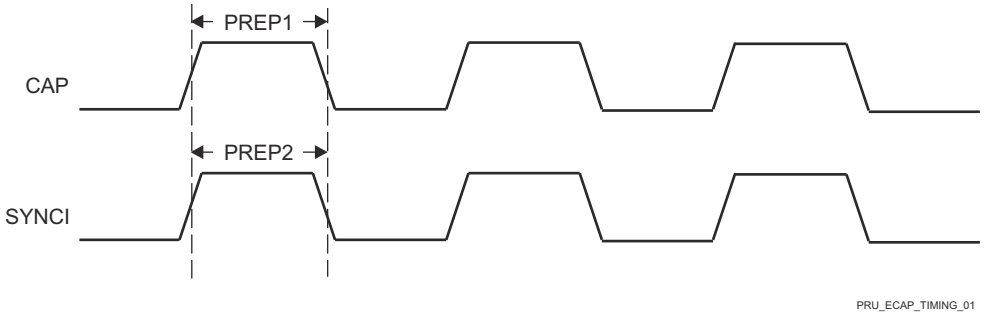

Figure 6-57. PRU-ICSS ECAP Timing

6.11.5.13.6.3 PRU-ICSS ECAP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP3	$t_{w(APWM)}$	Pulse duration, Auxiliary PWM (APWM) output high/low	2P(1)		ns
PREP4	$t_{w(SYNCO)}$	Pulse duration, Sync output (asynchronous)	P(1)		ns

(1) P = core_clk period

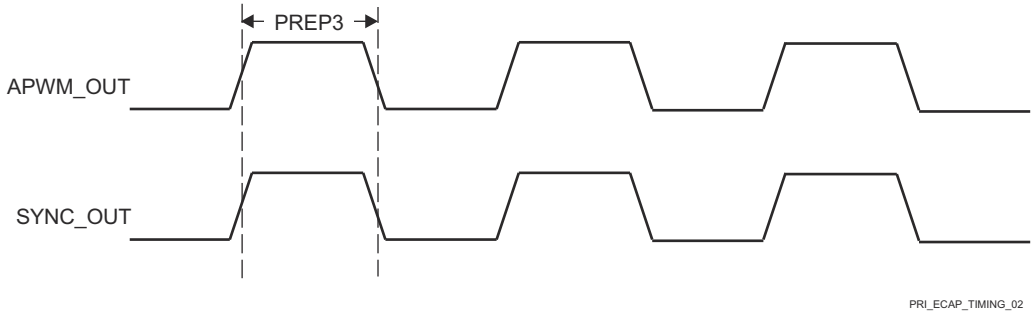

Figure 6-58. PRU-ICSS ECAP Switching Characteristics

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6.11.5.13.7 PRU-ICSS MDIO and MII

6.11.5.13.7.1 PRU-ICSS MDIO Timing

6.11.5.13.7.1.1 PRU-ICSS MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	10	470	pF

6.11.5.13.7.1.2 PRU-ICSS MDIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{su(MDIO-MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(MDC-MDIO)}$	Hold time, MDIO[x]_MDIO valid from MDIO[x]_MDC high	0		ns

6.11.5.13.7.1.3 PRU-ICSS MDIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	–150	150	ns

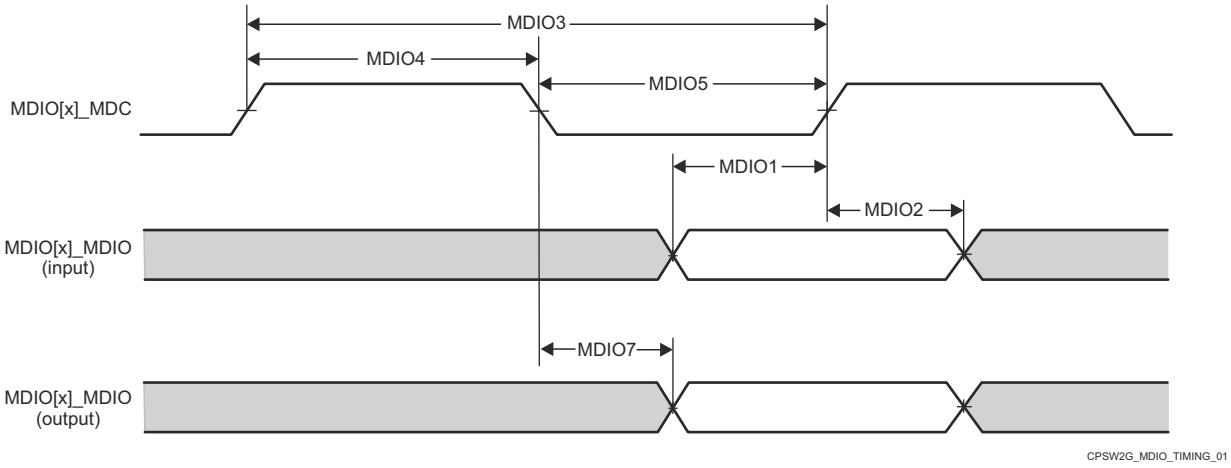

Figure 6-59. PRU-ICSS MDIO Timing Requirements and Switching Characteristics

6.11.5.13.7.2 PRU-ICSS MII Timing

6.11.5.13.7.2.1 PRU-ICSS MII Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				

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PARAMETER		MIN	MAX	UNIT
C_L	Output Load Capacitance	2	20	pF

6.11.5.13.7.2.2 PRU-ICSS MII Timing Requirements - MII[x]_RX_CLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR1	$t_{c(RX_CLK)}$	Cycle time, MII[x]_RX_CLK	10Mbps	399.96	400.04	ns
			100Mbps	39.996	40.004	ns
PMIR2	$t_{w(RX_CLKH)}$	Pulse duration, MII[x]_RX_CLK high	10Mbps	140	260	ns
			100Mbps	14	26	ns
PMIR3	$t_{w(RX_CLKL)}$	Pulse duration, MII[x]_RX_CLK low	10Mbps	140	260	ns
			100Mbps	14	26	ns

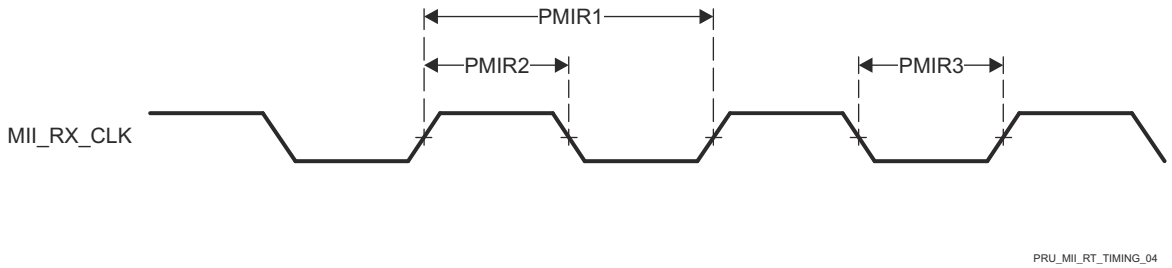

Figure 6-60. PRU-ICSS MII[x]_RX_CLK Timing

6.11.5.13.7.2.3 PRU-ICSS MII Timing Requirements - MII[x]_RXD[3:0], MII[x]_RX_DV, and MII[x]_RX_ER

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR4	$t_{su(RXD-RX_CLK)}$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	10Mbps	8		ns
	$t_{su(RX_DV-RX_CLK)}$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
	$t_{su(RX_ER-RX_CLK)}$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
	$t_{su(RXD-RX_CLK)}$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	100Mbps	8		ns
	$t_{su(RX_DV-RX_CLK)}$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
	$t_{su(RX_ER-RX_CLK)}$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
PMIR5	$t_{h(RX_CLK-RXD)}$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK	10Mbps	8		ns
	$t_{h(RX_CLK-RX_DV)}$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX_CLK-RX_ER)}$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX_CLK-RXD)}$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK	100Mbps	8		ns
	$t_{h(RX_CLK-RX_DV)}$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX_CLK-RX_ER)}$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns

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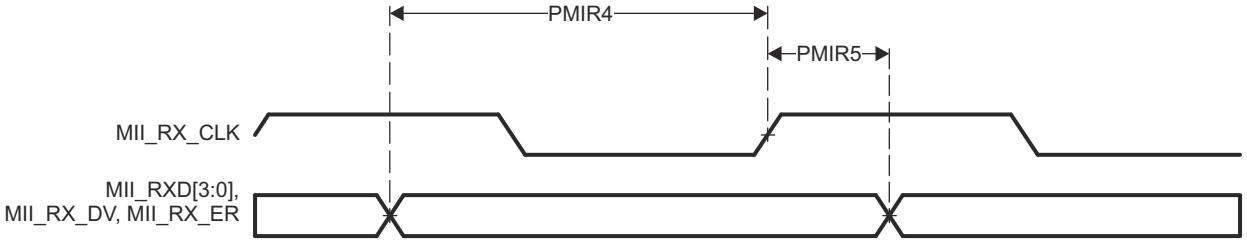

Figure 6-61. PRU-ICSS MII[x]_RXD[3:0], MII[x]_RX_DV, and MII[x]_RX_ER Timing

6.11.5.13.7.2.4 PRU-ICSS MII Switching Characteristics - MII[x]_TX_CLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT1	$t_{c(TX_CLK)}$	Cycle time, MII[x]_TX_CLK	10Mbps	399.96	400.04	ns
			100Mbps	39.996	40.004	ns
PMIT2	$t_{w(TX_CLKH)}$	Pulse duration, MII[x]_TX_CLK high	10Mbps	140	260	ns
			100Mbps	14	26	ns
PMIT3	$t_{w(TX_CLKL)}$	Pulse duration, MII[x]_TX_CLK low	10Mbps	140	260	ns
			100Mbps	14	26	ns

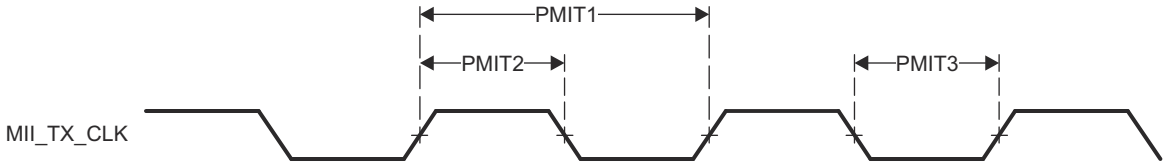

Figure 6-62. PRU-ICSS MII[x]_TX_CLK Timing

6.11.5.13.7.2.5 PRU-ICSS MII Switching Characteristics - MII[x]_TXD[3:0] and MII[x]_TXEN

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT4	$t_{d(TX_CLK-TXD)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TXD[3:0] valid	10Mbps	0	25	ns
	$t_{d(TX_CLK-TX_EN)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TX_EN valid		0	25	ns
	$t_{d(TX_CLK-TXD)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TXD[3:0] valid	100Mbps	0	25	ns
	$t_{d(TX_CLK-TX_EN)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TX_EN valid		0	25	ns

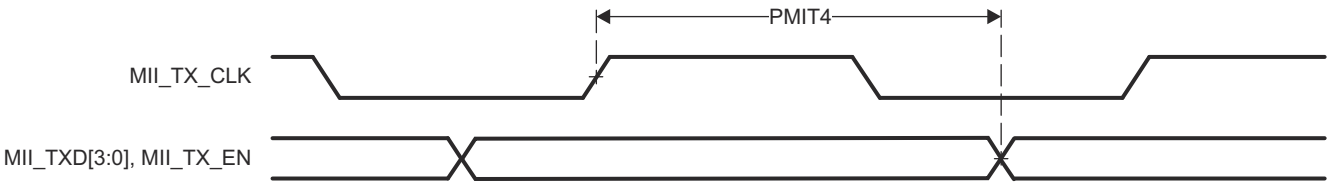

Figure 6-63. PRU-ICSS MII[x]_TXD[3:0], MII[x]_TX_EN Timing

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6.11.5.14 Sigma Delta Filter Module (SDFM)

For more information, see *Sigma Delta Filter Module* section in the device TRM.

6.11.5.14.1 SDFM Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	Mode 0	0.5	5	V/ns

6.11.5.14.2 SDFM Switching Characteristics

(2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M0-1	$t_{c(SDC)}$	Cycle time, SDx_Cy	Mode 0	5P(1)	256P(1)	ns
M0-2	$t_{w(SDCHL)}$	Pulse duration, SDx_Cy (high/low)	Mode 0	2P(1)		ns
M0-3	$t_{sh(SDDV-SDCH)}$	Setup time, SDx_Dy valid before SDx_Cy high	Mode 0	2P(1)		ns
M0-4	$t_{h(SDCH-SDD)}$	Hold time, SDx_Dy wait after SDx_Cy high	Mode 0	2P(1)		ns

(1) P = SYSCLK period in ns.
(2) Some SDFM signals are pinmuxed with I2C0 SDA and SCL pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

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6.11.5.15 Universal Asynchronous Receiver/Transmitter (UART)

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in the device TRM.

6.11.5.15.1 UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	30	pF

6.11.5.15.2 UART Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, high or low	0.95U(1)	1.05U(1)	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, high or low	0.95U(1)		ns

(1) U = UART baud time = 1 / Programmed baud rate.

6.11.5.15.3 UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate	15pF		12	Mbps
			30pF		0.115	
2	$t_{w(TX)}$	Pulse width, transmit data bit, high or low		U(1) – 2.2	U(1) + 2.2	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, high or low		U(1) – 2.2		ns
1	$t_{d(CTS-TX)}$	Delay time, receive CTS bit to transmit data		30		ns

(1) U = UART baud time = 1 / Programmed baud rate.

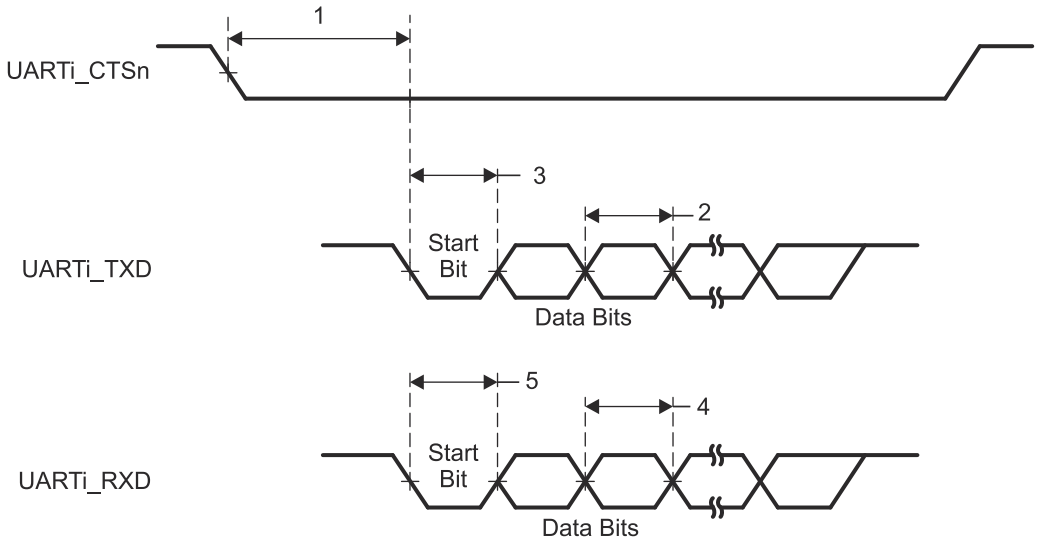

Figure 6-64. UART Timing Requirements and Switching Characteristics

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6.11.6 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections. For more information, see the *On-Chip Debug* section in the device TRM.

6.11.6.1 JTAG

The acronym stands for the **Joint Test Action Group**, the committee of engineers who defined the boundary-scan standard (IEEE std 1149.1). For more details about features and additional description information on the device JTAG interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.6.1.1 JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	2.00	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	15	pF

6.11.6.1.2 JTAG Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time, TCK	40		ns
J2	$t_{w(TCKH)}$	Pulse width, TCK high	16		ns
J3	$t_{w(TCKL)}$	Pulse width, TCK low	16		ns
J4	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	2		
J5	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	15.9		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	15.9		

6.11.6.1.3 JTAG Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time, TCK low to TDO invalid	–0.067005		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		11.89594	ns

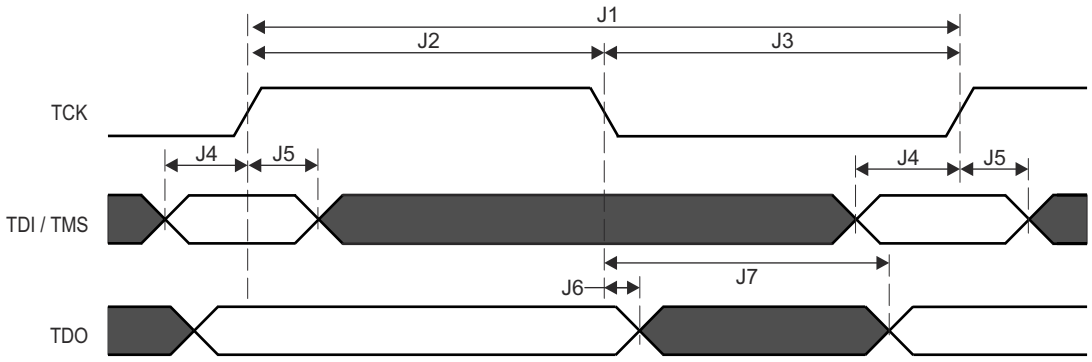

Figure 6-65. JTAG Timing Requirements and Switching Characteristics

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6.11.6.2 Trace

6.11.6.2.1 Debug Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	5	pF
OUTPUT CONDITIONS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces.		200	ps

6.11.6.2.2 Debug Trace Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DBTR1	$tc_{(TRC_CLK)}$	Cycle time, TRC_CLK	9.75		ns
DBTR2	$t_{w(TRC_CLKH)}$	Pulse width, TRC_CLK high	4.13		ns
DBTR3	$t_{w(TRC_CLKL)}$	Pulse width, TRC_CLK low	4.13		ns
DBTR4	$t_{osu(TRC_DATAV-TRC_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.22		ns
DBTR5	$t_{oh(TRC_CLK-TRC-DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.22		ns
DBTR6	$t_{osu(TRC_CTLV-TRC_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.22		ns
DBTR7	$t_{oh(TRC_CLK-TRC_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.22		ns

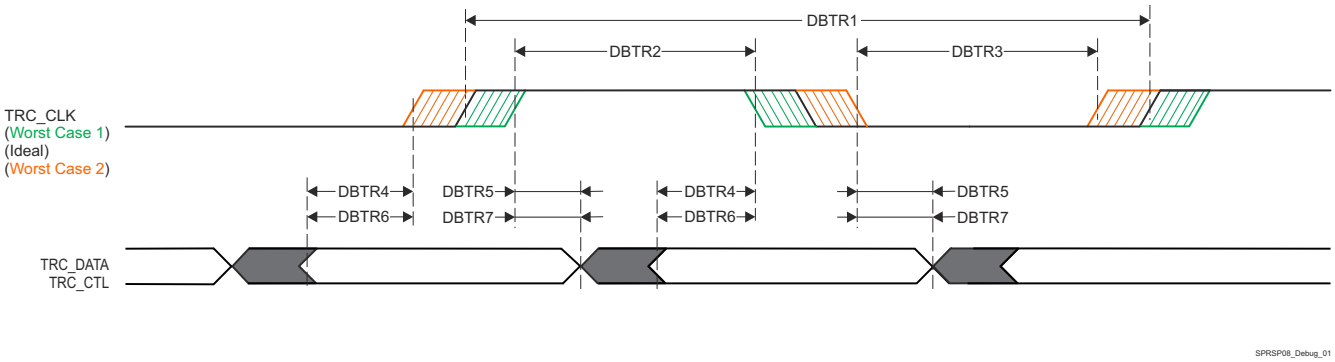

Figure 6-66. Trace Switching Characteristics

6.12 Decoupling Capacitor Requirements

6.12.1 Decoupling Capacitor Requirements

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
C_{VDD}	1.2V VDD (Cap)		10		µF
C_{VDDS33}	3.3V VDDS (Cap)		10		µF
C_{VDDA33}	3.3V VDDA (Cap)		10		µF
C_{VDDS18}	1.8V VDDS (Cap)		0.1		µF
C_{VDDA18}	1.8V VDDA (Cap)		0.1		µF
C_{VPP}	1.7V VPP (Cap)		0.1		µF
C_{VDDS18_LDO}	1.8V LDO VDDS (Cap)		3.3		µF
C_{VDDA18_LDO}	1.8V LDO VDDA (Cap)		4.7		µF
C_{ADC_VREF}	ADC VREFHI (Cap)		4.7		µF

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7 Detailed Description

7.1 Overview

The AM263Px Sitara Arm® Microcontrollers are built to meet the complex real-time processing and control needs of next generation industrial and automotive embedded projects. AM263Px uniquely combines advanced computing with industry leading real-time control peripherals to meet the growing performance needs of applications such as HEV/EV (traction inverters, on-board chargers, and DC-DC converters), motor drives, renewable energy, energy storage, and other general real-time constrained systems. AM263Px combines up to four Cortex-R5F MCUs, a real-time control subsystem (CONTROLSS), a Hardware Security Module (HSM), and one instance of Sitara's PRU-ICSS, making AM263Px designed for advanced motor control and digital power control applications.

The multiple R5F cores are arranged in cluster with 256KB of shared tightly coupled memory (TCM) along with 3MB of shared SRAM. The multiple Arm® cores can be optionally programmed to run in lock-step option for different functional safety configurations. Extensive ECC is included on on-chip memory, peripherals, and interconnect for enhanced reliability. Cryptographic acceleration and secure boot are also available on AM263Px devices in addition to granular firewalls managed by the HSM for developers to design the most secure systems.

The Real-Time Control Subsystem (CONTROLSS) is a revolutionary subsystem integrated into the device. CONTROLSS contains multiple digital and analog control peripherals including: ADC, CMPSS, EPWM, ECAP, and EQEP, among others to enable efficient execution of critical sense/process/actuate real-time signal chain control loops. The integrated crossbar (XBAR) infrastructure enables flexible configuration and routing of external signals to internal ports and internal signals to external pins.

The PRU-ICSS in AM263Px provides the flexible industrial communications capability necessary to run EtherCAT®, PROFINET®, Ethernet/IP™, or for standard Ethernet connectivity and custom I/O interfacing. The PRU also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces. The CPSW interface also provides two standard Ethernet ports.

TI provides a complete set of microcontroller software and development tools for the AM263Px family of microcontrollers in addition to multiple pin-to-pin compatible devices for scalability and ease of use.

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7.2 Processor Subsystems

7.2.1 Arm Cortex-R5F Subsystem

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual-core (split) or lockstep modes of operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC. The device supports up to two R5FSS modules for a total possible 4x functional cores (dual-core mode) or 2x functional cores (lockstep mode).

Note

The Arm® Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating-point Unit (FPU) extension.

For more information, see *R5FSS* section in *Processors and Accelerators* chapter in the device TRM.

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8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Device Connection and Layout Fundamentals

8.1.1 External Oscillator

For more information about External Oscillators, see the Input Clocks / Oscillators section.

8.1.2 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.1.3 OSPI Connections for Flash in Package (ZCZ_F)

The ZCZ_F packages offers an internally connected on-die OSPI flash module (ISSI IS25LX064-LWLA3 OSPI Flash device). Due to the internal connections, the ZCZ_F package comes with additional pin connection requirements. Please reference Pin Connectivity Requirements for pin connectivity requirements and ball names.

- The OSPI_D2 signal (pin L1) doubles as the active low Write Protect input for the internally connected flash device. Therefore, pin L1 must be connected to the relevant source (VDDS33) through a separate 4.7kΩ external pull resistor. This resistor must be placed as close to the device as possible.
- The OSPI_RESET_OUT0 signal (pin J3) must be connected to an open-drain equivalent of PORz in order to reset the on-die OSPI flash module. The open-drain requirement is to prevent a bus contention between the external PORz connection via pin J3 and the package internal connection between the AM263P and the OSPI flash device.
- The remaining pins internally connected for the on-die OSPI flash module (pins P1, M4, P3, M1, L2, H1, J1, K2, J4, K4, and K3) should be left unconnected with no PCB traces.

Pleased see ZCZ_F Package OSPI Connection Requirements for a visualization of the necessary connections.

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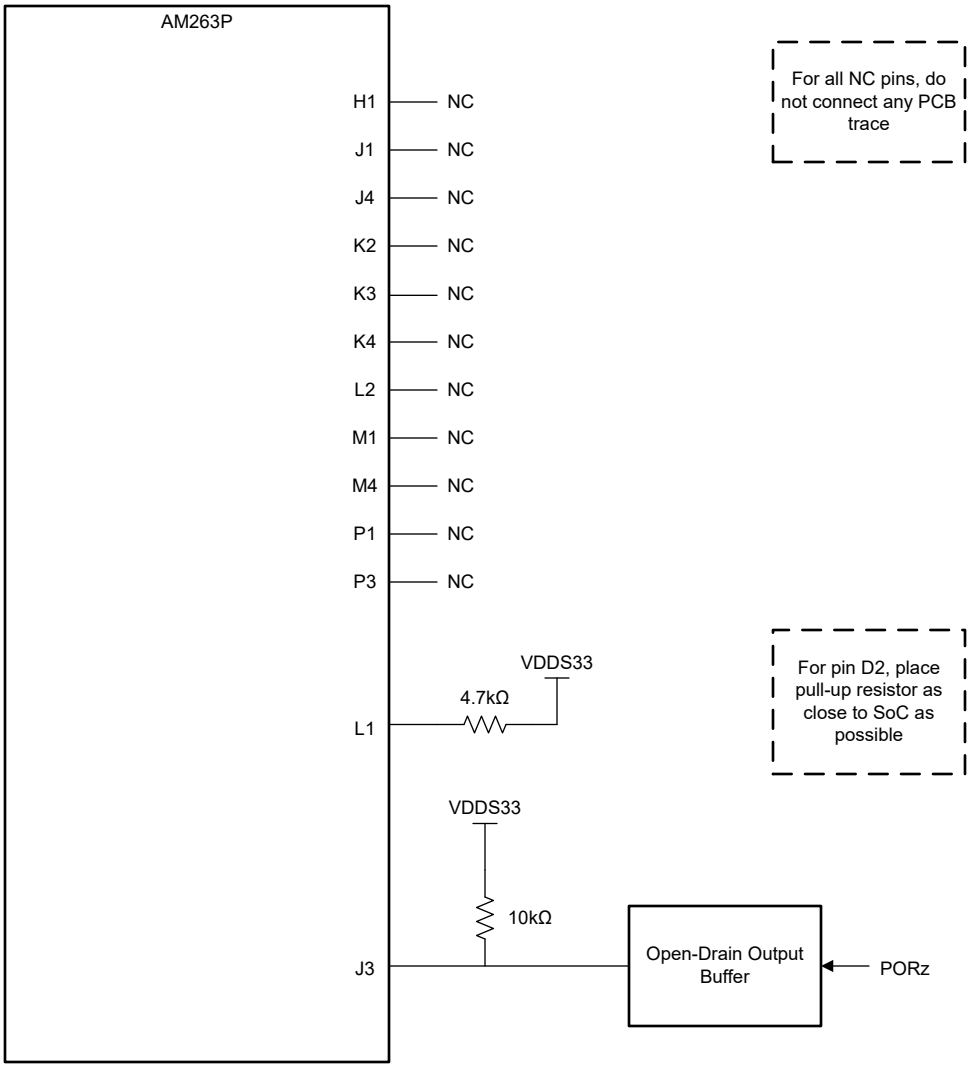

Figure 8-1. ZCZ_F Package OSPI Connection Requirements

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9 Device and Documentation Support

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontrollers (MCUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM263PxAOLFGMZCZQ). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM263Px devices in the ZCZ package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

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9.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

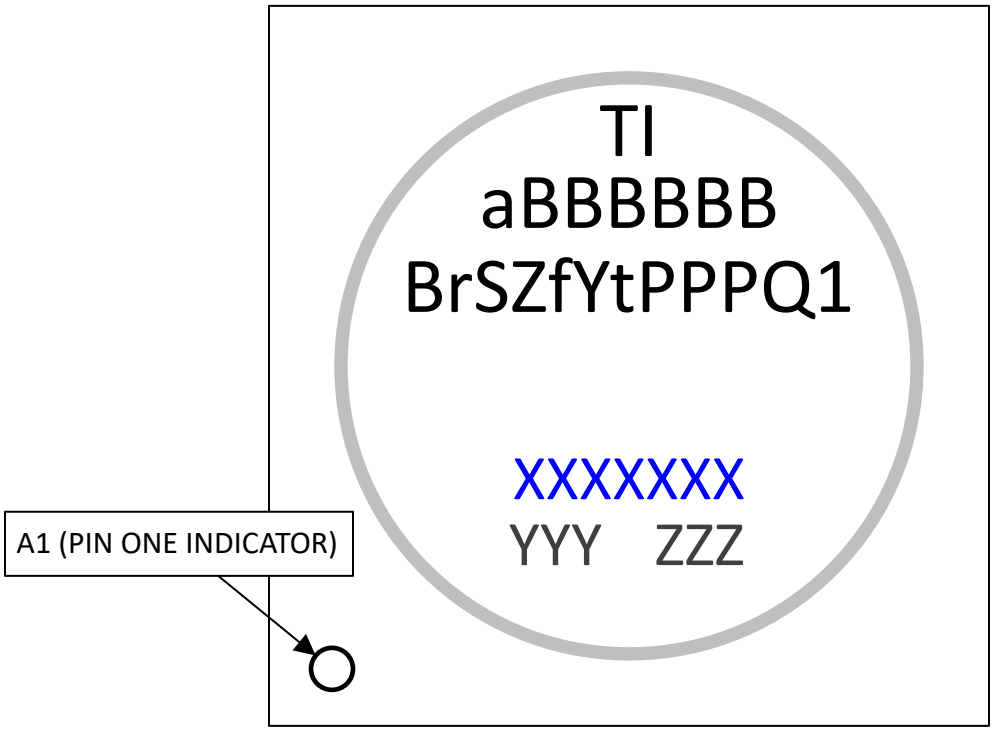

Figure 9-1. Printed Device Reference

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9.1.2 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a[2]	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK[1]	Production
BBBBBBB	Base production part number	AM263P4	See *Device Comparison*.
		AM263P2	
		AM263P1	
r	Device revision	A	SR 1.0
S	Special Features	C	AM263x Compatible Package (ZCZ-C)
		F	AM263Px Sensor Package (ZCZ-F) + SIP Flash-in-Package
		S	AM263Px Sensor Package (ZCZ-S)
Z	Device Operating Performance Points	N	See *Operating Performance Points*.
		O	
		P	
f	Features (see Table 4-1, *Device Comparison*)	D	PRU-ICSS + CAN-FD Supported + Standard Analog
		E	PRU-ICSS + EtherCAT HW Accelerator + CAN-FD Supported + Standard Analog
		F	PRU-ICSS + EtherCAT HW Accelerator + CAN-FD Supported + Pre-integrated Stacks Enabled + Standard Analog
		K	PRU-ICSS + CAN-FD Supported + Enhanced Analog
		L	PRU-ICSS + EtherCAT HW Accelerator + CAN-FD Supported + Enhanced Analog
		M	PRU-ICSS + EtherCAT HW Accelerator + CAN-FD Supported + Pre-integrated Stacks + Enhanced Analog
		N	Reserved
Y	Functional Safety	G	Non-Functional Safety (AM263P1 only)
		F	Functional Safety
PPP	Package Designator	ZCZ	ZCZ NFBGA-N324 (15 mm × 15 mm) Package
Q1	Automotive Designator and Max Junction Temperature[3] (see Section 6.5, *ROC*)	Q1	Auto Qualified (AEC-Q100) –40°C to 150°C - Extended Automotive
		BLANK	Standard –40°C to 105°C - Industrial
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
O			Pin one designator

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Table 9-1. Nomenclature Description (continued)

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
G1			ECAT - Green package designator

(1) BLANK in the symbol or part number is collapsed so there are no gaps between characters.
(2) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
(3) Applies to device max junction temperature.

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9.2 Tools and Software

The following products support development for AM263Px platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool will generate output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents are provided to describe the AM263Px device.

AM263Px Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM263Px family of devices.

AM263Px TRM Register Addendum Details the memory mapped register information for each peripheral and subsystem in the AM263Px family of devices.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from January 8, 2024 to March 15, 2024 (from Revision A (January 2024) to Revision B (March 2024)) — **Page**

- **Global:** Added in pin and signal information for ZCZ_F package....1
- (Features): Added information on OSPI Flash device for SIP package....1
- (Device Comparison): Added JTAG Device ID's....7
- (Related Products): Added reference to AM263P SDK....9
- Pin Attributes: Changed crystal power reference from "VDDS_OSC" to "VDDA18_OSC_PLL"....16
- (OSPI Connections for Flash in Package (ZCZ_F)): Added applications chapter covering ZCZ_F OSPI connections....149

Changes from October 1, 2023 to January 8, 2024 (from Revision * (October 2023) to Revision A (January 2024)) — **Page**

- (Features): Added details on recommended PMIC solution....1
- (Features): Added details on SIP device....1
- (Features): Changed "Up to 140 GPIO" to "Up to 139 GPIO"....1
- (Features): Added MII support....1
- (Device Comparison): Added details on SIP package....7
- (Device Comparison): Changed "Up to 140" in GPIO row to "Up to 139"....7
- (ADC-CMPSS Signal Connections): Added image and paragraph to explain ADC-CMPSS Signal Connections....49
- (Recommended Operating Conditions): Added SIP package T_J details....74
- (SAFETY_ERRORn Switching Characteristics): Updated table note reference from "RST22" to "SFTY3"....93
- (CPSW RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode): Updated table note on internal delay from "always enabled" to "by default enabled after POR."....98

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging information website.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XAM263P4ACOMFZCZ	ACTIVE	NFBGA	ZCZ	324	1	TBD	Call TI	Call TI	-40 to 105		Samples
XAM263P4ASOKFZCZ	ACTIVE	NFBGA	ZCZ	324	1	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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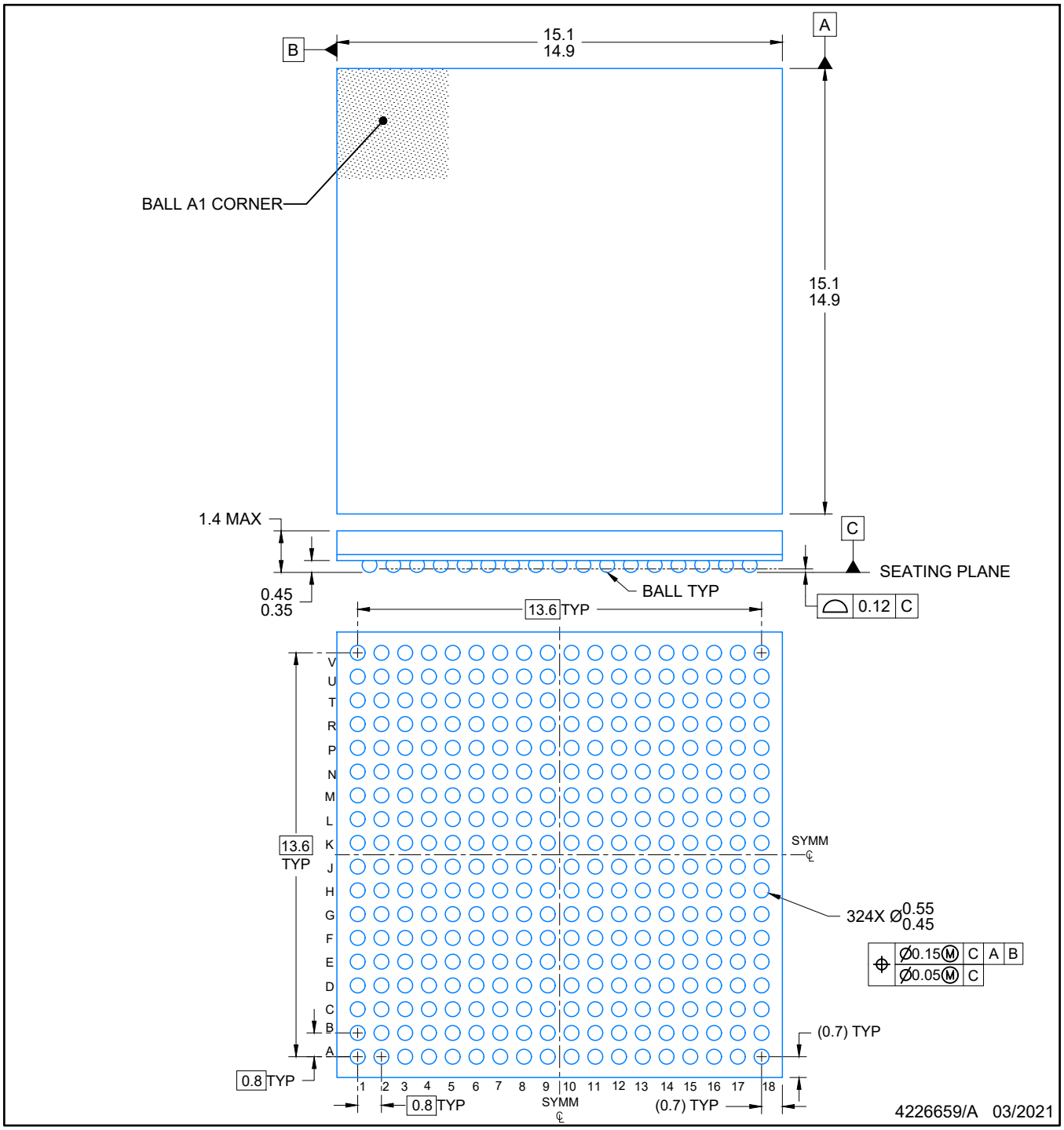
PACKAGE OUTLINE

ZCZ0324A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

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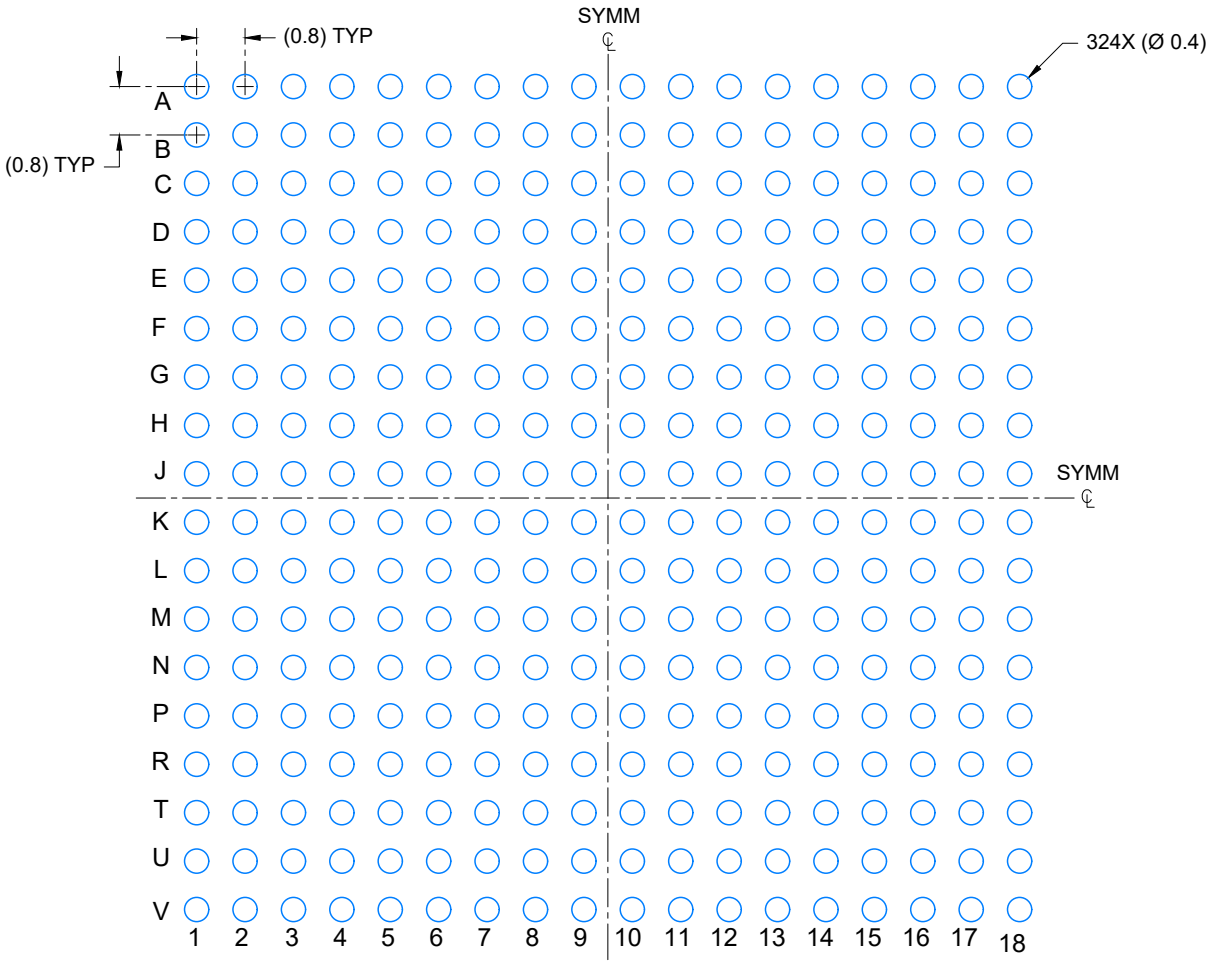
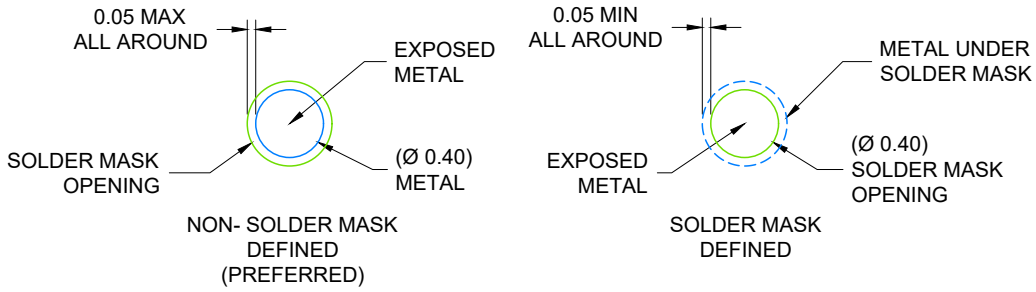
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 8X



SOLDER MASK DETAILS

NOT TO SCALE

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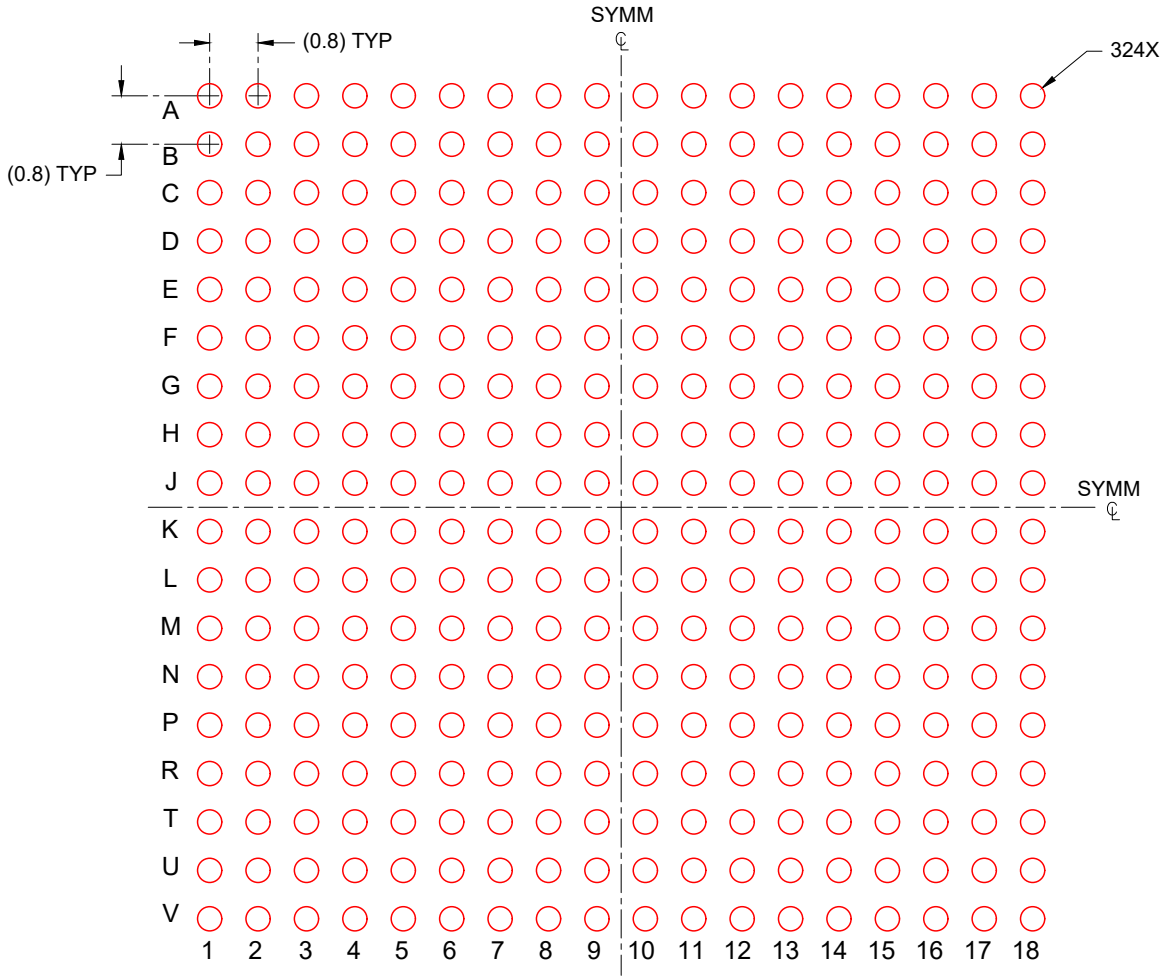
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4226659/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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