



# CSD85301Q2 20 V Dual N-Channel NexFET™ Power MOSFETs

## 1 Features

- Low On-Resistance
- Dual Independent MOSFETs
- Space Saving SON 2 x 2 mm Plastic Package
- Optimized for 5 V Gate Driver
- Avalanche Rated
- Pb and Halogen Free
- RoHS Compliant

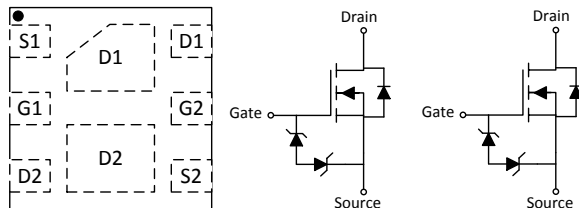
## 2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Adaptor or USB Input Protection for Notebook PCs and Tablets
- Battery Protection

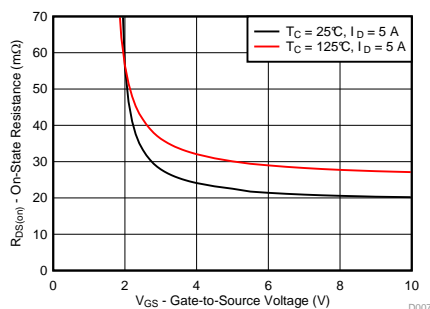
## 3 Description

The CSD85301Q2 is a 20 V, 23 mΩ N-Channel device with dual independent MOSFETs in a SON 2 x 2 mm plastic package. The two FETs were designed to be used in a half bridge configuration for synchronous buck and other power supply applications. Additionally, this part can be used for adaptor, USB input protection and battery charging applications. The dual FETs feature low drain to source on-resistance that minimizes losses and offers low component count for space constrained applications.

Top View and Circuit Image



$R_{DS(on)}$  vs  $V_{GS}$



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	20		V
$Q_g$	Gate Charge Total (4.5 V)	4.2		nC
$Q_{gd}$	Gate Charge Gate to Drain	1.0		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 1.8\text{ V}$	65	mΩ
		$V_{GS} = 2.5\text{ V}$	33	mΩ
		$V_{GS} = 3.8\text{ V}$	25	mΩ
		$V_{GS} = 4.5\text{ V}$	23	mΩ
$V_{GS(th)}$	Threshold Voltage	0.9		V

Ordering Information<sup>(1)</sup>

Device	Media	Qty	Package	Ship
CSD85301Q2	7-Inch Reel	3000	SON 2 x 2 mm Plastic Package	Tape and Reel
CSD85301Q2T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

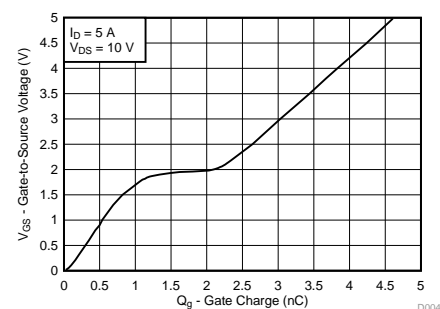
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	±10	V
$I_D$	Continuous Drain Current (Package limited)	5.0	A
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	26	A
$P_D$	Power Dissipation <sup>(2)</sup>	2.3	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	–55 to 150	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 8.7\text{ A}, L = 0.1\text{ mH}, R_G = 25\text{ }\Omega$	3.8	mJ

(1) Max  $R_{\theta JA} = 185\text{ }^\circ\text{C/W}$ , pulse duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 1\%$ .

(2) Typical  $R_{\theta JA} = 55\text{ }^\circ\text{C/W}$  on a 1 inch<sup>2</sup>, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

Gate Charge



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	6.1 Trademarks .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	6.2 Electrostatic Discharge Caution .....	<b>7</b>
<b>3 Description</b> .....	<b>1</b>	6.3 Glossary .....	<b>7</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>7 Mechanical, Packaging, and Orderable Information</b> .....	<b>8</b>
<b>5 Specifications</b> .....	<b>3</b>	7.1 Package Dimensions .....	<b>8</b>
5.1 Electrical Characteristics .....	<b>3</b>	7.2 PCB Land Pattern .....	<b>9</b>
5.2 Thermal Information .....	<b>3</b>	7.3 Recommended Stencil Opening .....	<b>9</b>
5.3 Typical MOSFET Characteristics .....	<b>4</b>	7.4 Q2 Tape and Reel Information .....	<b>10</b>
<b>6 Device and Documentation Support</b> .....	<b>7</b>		

## 4 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-Source Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 16 V			1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 10 V			10	μA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6	0.9	1.2	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 0.5 A	65		99	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 5 A	33		39	mΩ
		V <sub>GS</sub> = 3.8 V, I <sub>D</sub> = 5 A	25		29	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A	23		27	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 2 V, I <sub>D</sub> = 5 A	20			S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 10 V, f = 1 MHz	361		469	pF
C <sub>oss</sub>	Output Capacitance		68		89	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		48		62	pF
R <sub>G</sub>	Series Gate Resistance		7.3			Ω
Q <sub>g</sub>	Gate Charge Total (4.5 V)	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 A	4.2		5.4	nC
Q <sub>gd</sub>	Gate Charge Gate-to-Drain		1.0			nC
Q <sub>gs</sub>	Gate Charge Gate-to-Source		1.1			nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>		0.5			nC
Q <sub>oss</sub>	Output Charge	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V	1.3			nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5 V, I <sub>DS</sub> = 5 A, R <sub>G</sub> = 0 Ω	6			ns
t <sub>r</sub>	Rise Time		26			ns
t <sub>d(off)</sub>	Turn Off Delay Time		14			ns
t <sub>f</sub>	Fall Time		15			ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = 5 A, V <sub>GS</sub> = 0 V	0.8		1.0	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = 10 V, I <sub>F</sub> = 5 A, di/dt = 300 A/μs	7.2			nC
t <sub>rr</sub>	Reverse Recovery Time		14			ns

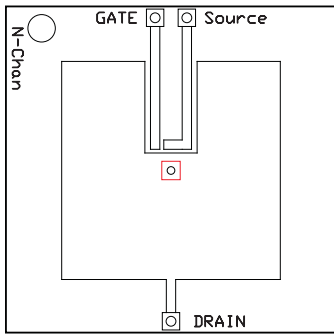
### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)</sup>			70	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance <sup>(2)</sup>			185	

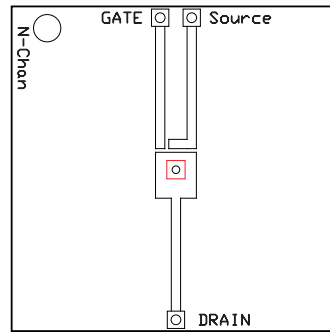
(1) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



M0164-01

Max  $R_{\theta JA} = 70$  when  
mounted on 1 inch<sup>2</sup>  
(6.45 cm<sup>2</sup>) of 2 oz.  
(0.071 mm thick) Cu.

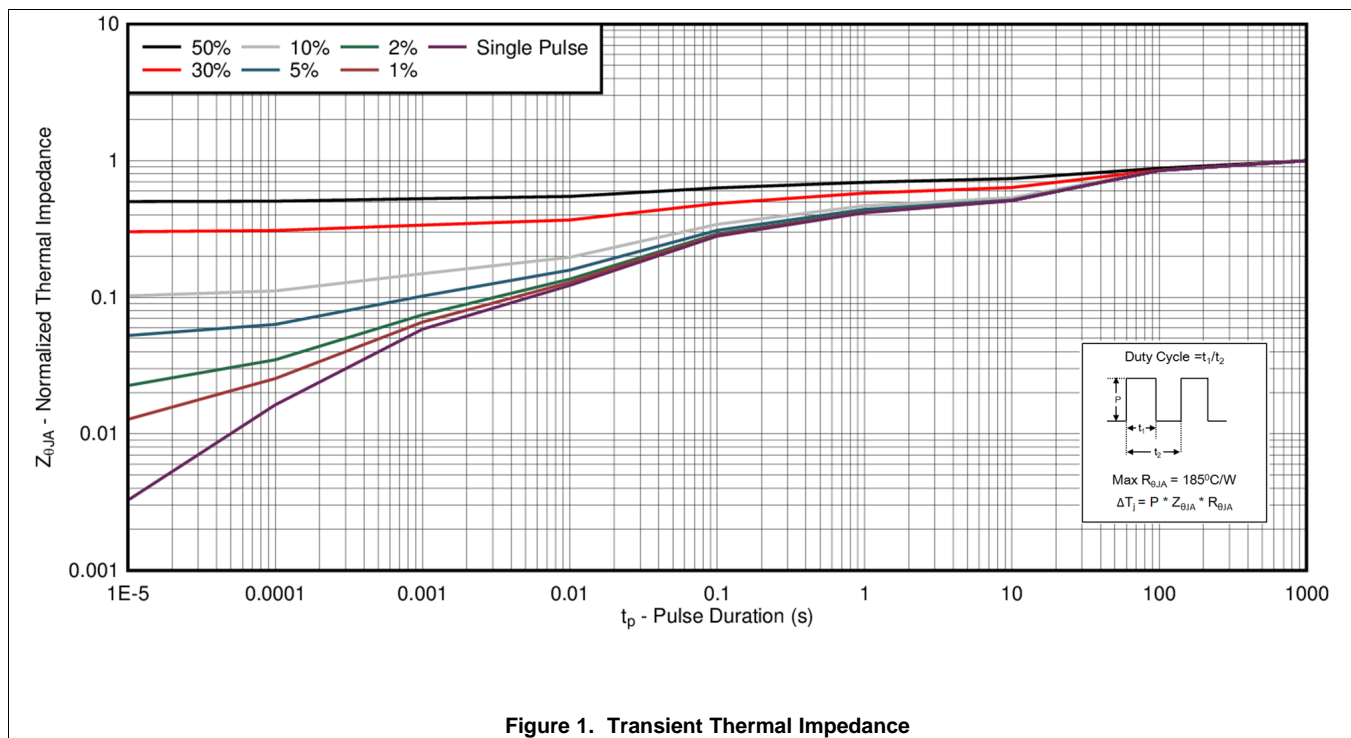


M0164-02

Max  $R_{\theta JA} = 185$  when  
mounted on minimum  
pad area of 2 oz.  
(0.071 mm thick) Cu.

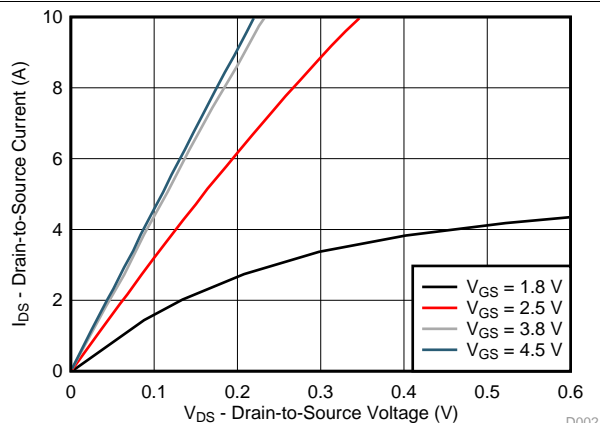
### 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

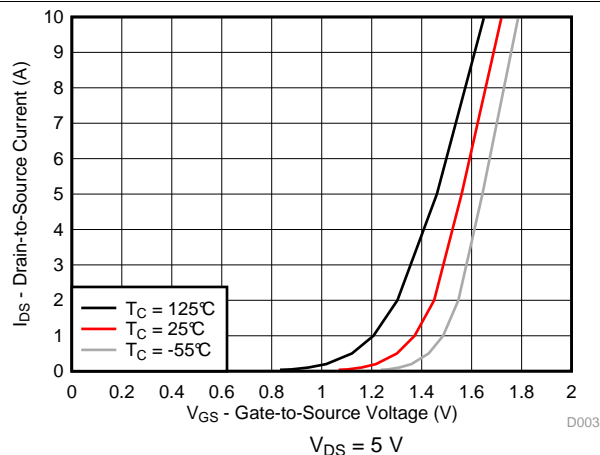


## Typical MOSFET Characteristics (continued)

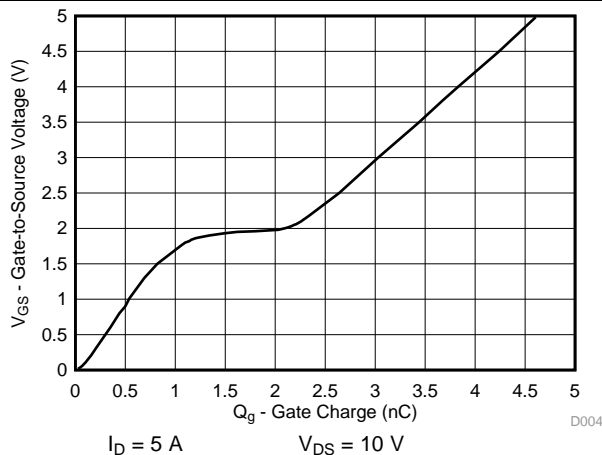
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



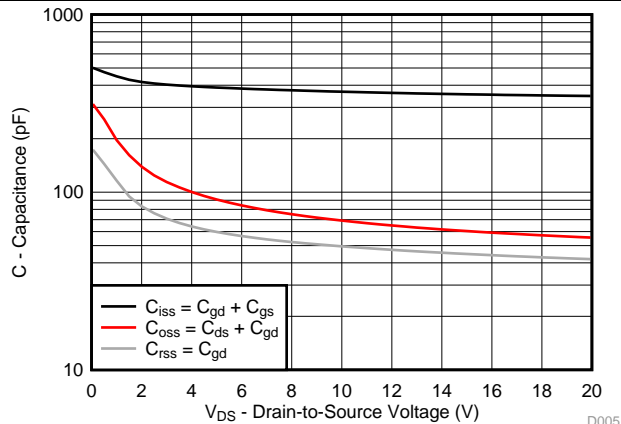
**Figure 2. Saturation Characteristics**



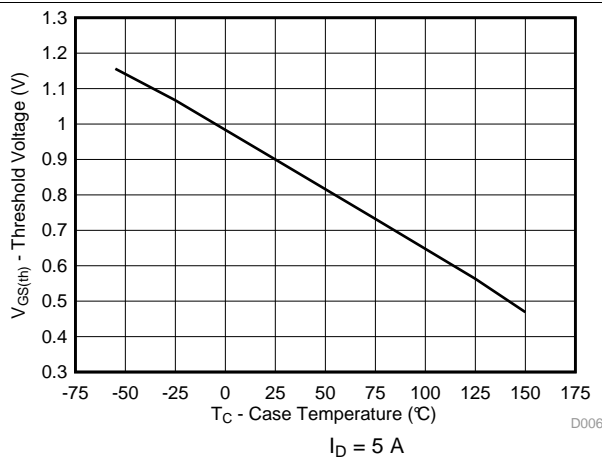
**Figure 3. Transfer Characteristics**



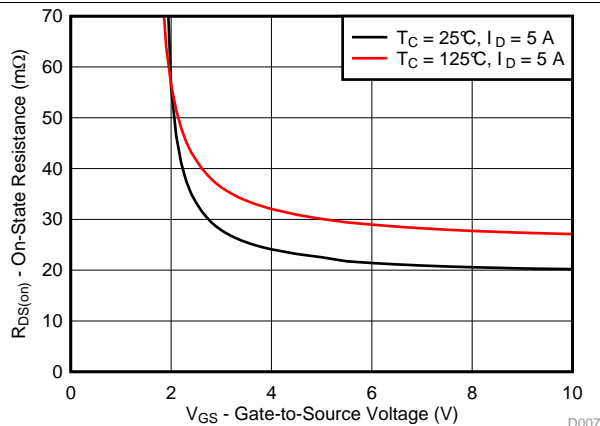
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs Temperature**



**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

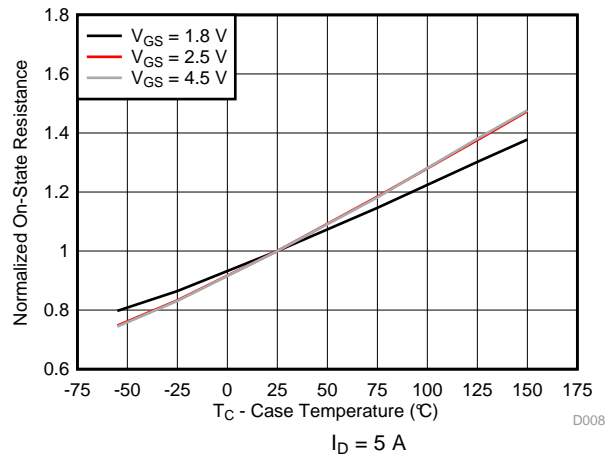


Figure 8. Normalized On-State Resistance vs Temperature

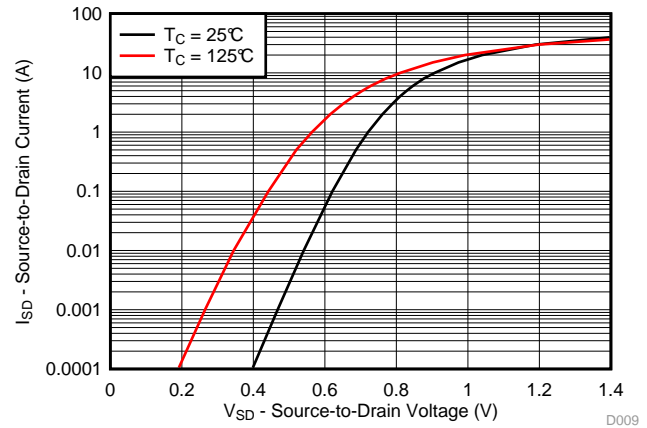


Figure 9. Typical Diode Forward Voltage

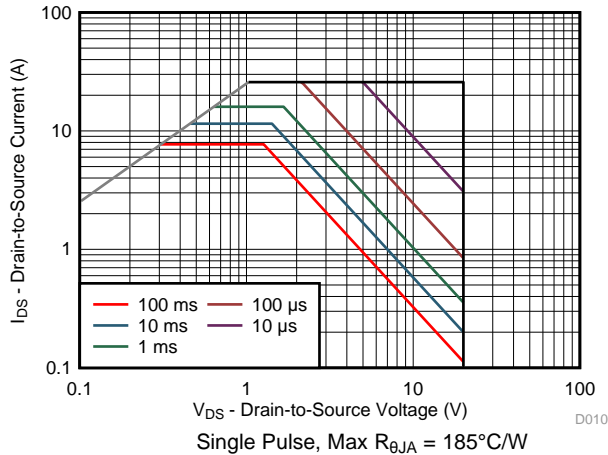


Figure 10. Maximum Safe Operating Area

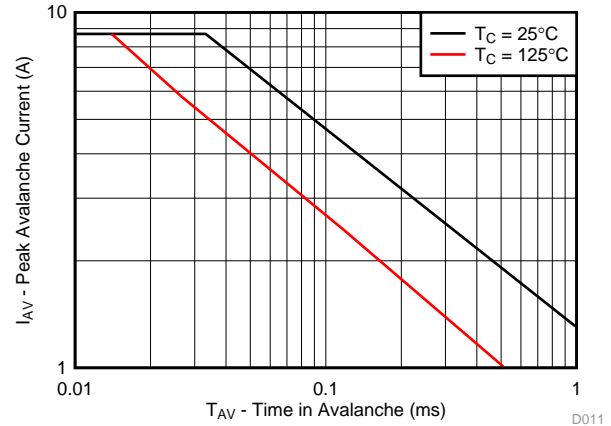


Figure 11. Single Pulse Unclamped Inductive Switching

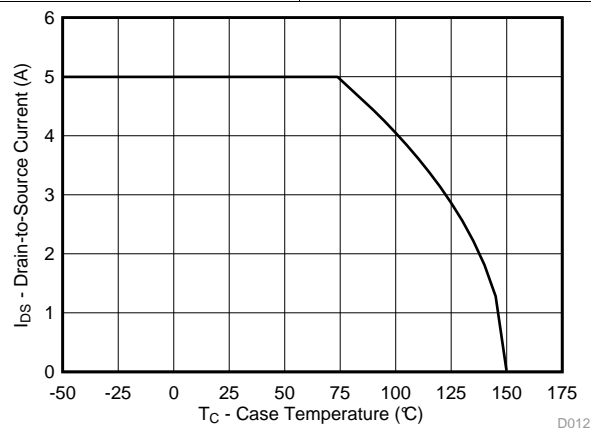


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

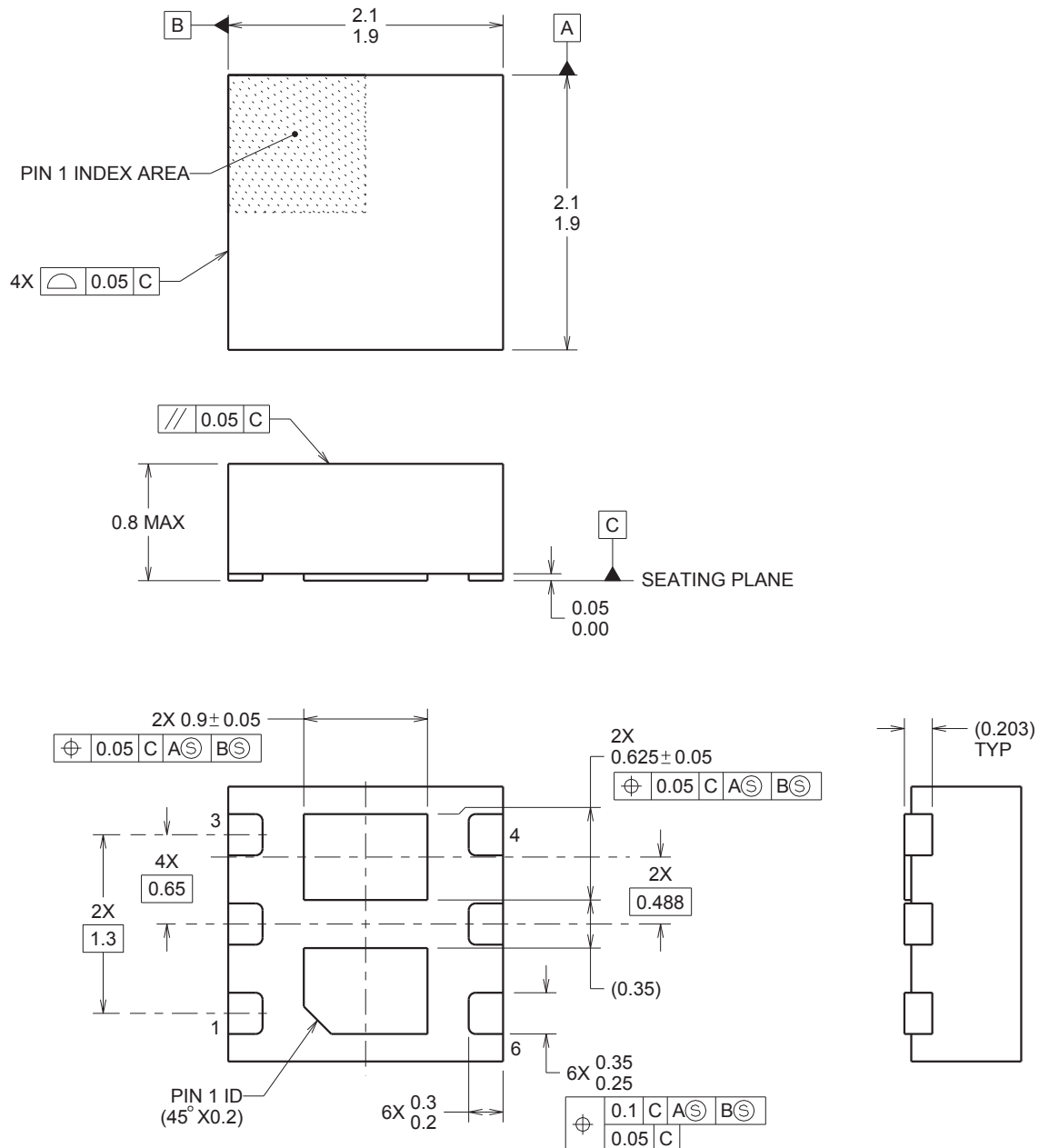
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

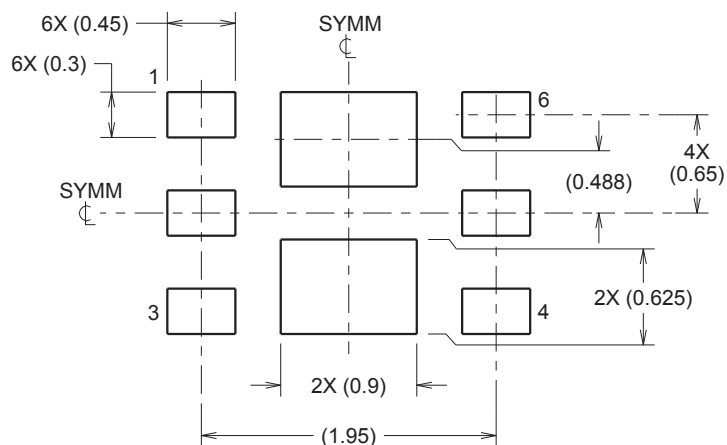
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Package Dimensions



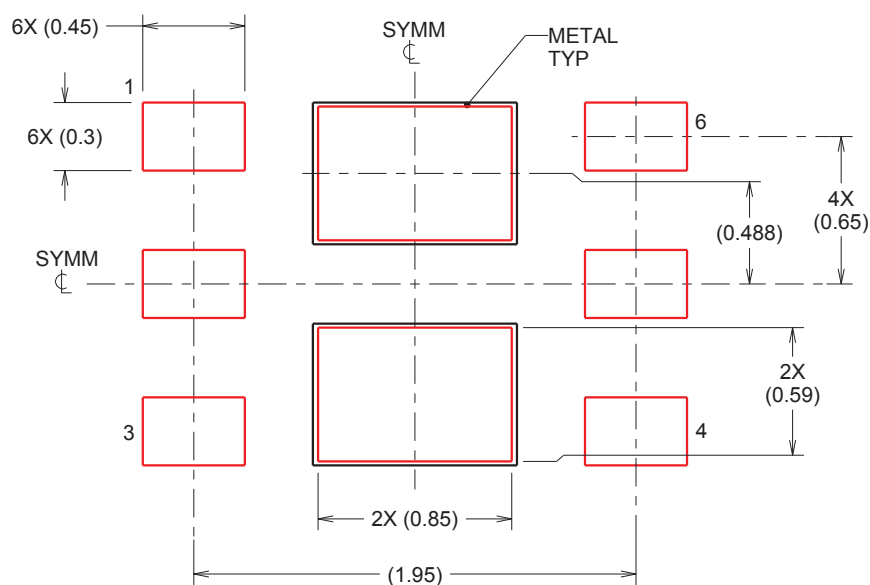
All dimensions are in mm, unless otherwise stated.

## 7.2 PCB Land Pattern



For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise stated.

Product Folder Links: [CSD85301Q2](#)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD85301Q2	ACTIVE	WSON	DLV	6	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM		8531	<a href="#">Samples</a>
CSD85301Q2T	ACTIVE	WSON	DLV	6	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	8531	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

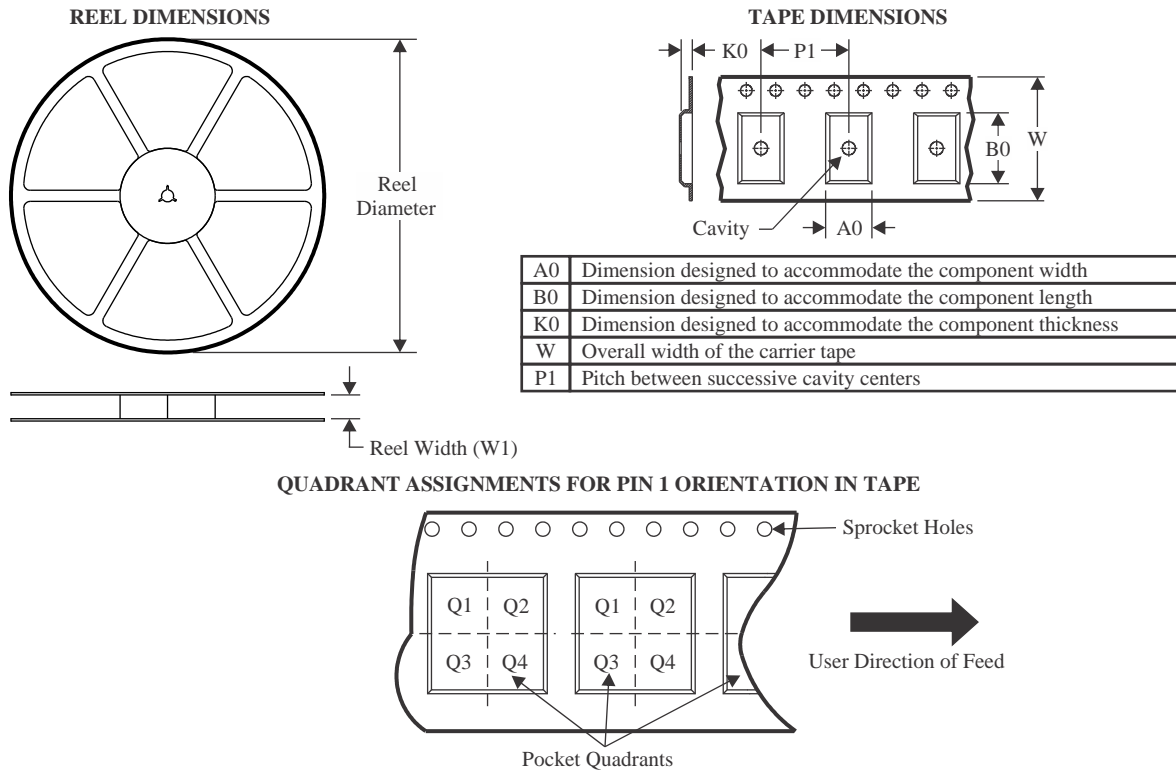
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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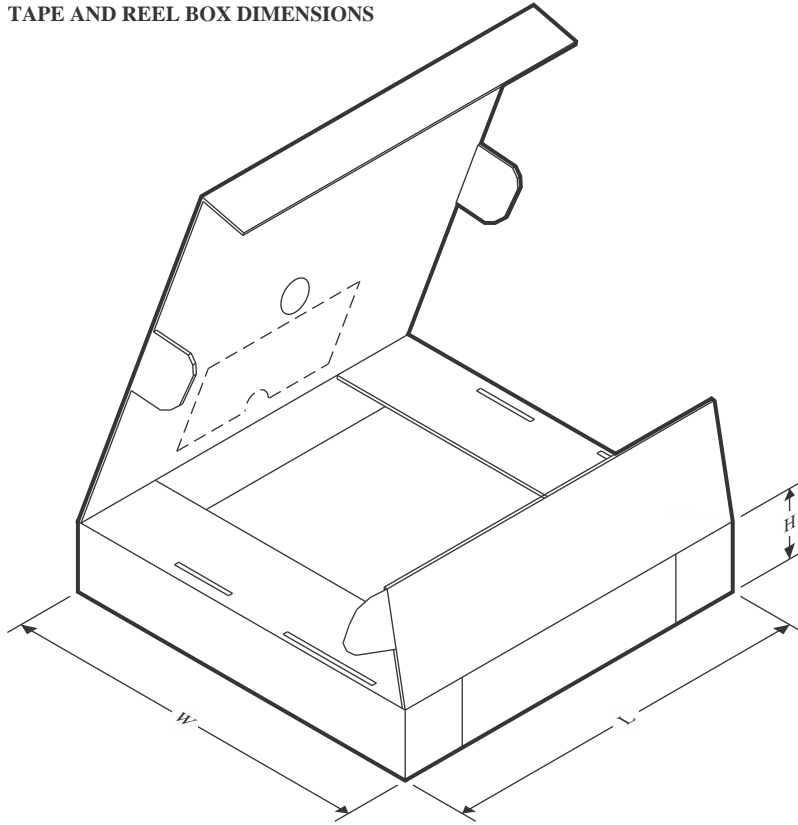
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD85301Q2	WSO	DLV	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD85301Q2T	WSO	DLV	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD85301Q2	WS0N	DLV	6	3000	189.0	185.0	36.0
CSD85301Q2T	WS0N	DLV	6	250	189.0	185.0	36.0

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