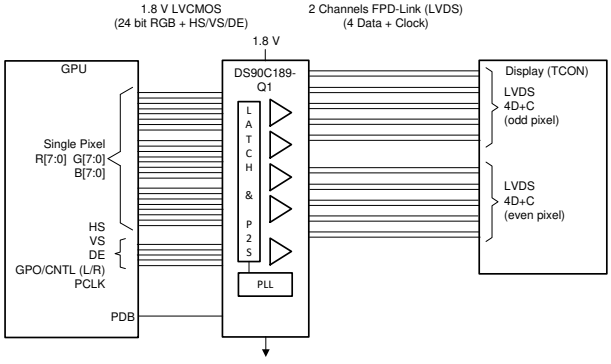
DS90C189-Q1 Low Power, 1.8-V RGB-to-Open LDI (LVDS) Bridge

1 Features

- AEC-Q100 Qualified for Automotive Applications with the Following Specifications:
  - Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level ±8 kV
  - Device CDM ESD Classification Level ±750 V
- 150 mW Typical Power Consumption at 185 MHz (SIDO Mode)
- Drives QXGA and WQXGA Class Displays
- Two Operating Modes:
  - Single Pixel In, Single Pixel Out (SISO): 105 MHz Maximum
  - Single Pixel In, Dual Pixel Out (SIDO): 185 MHz Maximum
- Supports 24-Bit RGB
- Supports 3D+C, 4D+C, 6D+C, 6D+2C, 8D+C, and 8D+2C LVDS Configurations
- Compatible With FPD-Link Devices
- Operates Off a Single 1.8-V Supply
- Interfaces Directly With 1.8-V LVCMOS
- Less Than 10 mW Power Consumption in Sleep Mode
- Spread Spectrum Clock Compatible
- Small 9 mm × 9 mm × 0.9 mm 64-Pin VQFN Package

2 Applications

- Camera Monitor Systems (CMS)
- Automotive Head Units
- Smart Mirrors
- Cluster



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3 Description

The DS90C189-Q1 is a low power bridge for automotive applications that reduces the size of the RGB interface between the host GPU and the Display.

The DS90C189-Q1 Bridge is designed to support single pixel data transmission between a Host and a Flat Panel Display at resolutions of up to QXGA (2048x1536) at 60 Hz. The transmitter converts up to 24 bits (Single Pixel 24-bit color) of 1.8-V LVCMOS data into two channels of 4 data + clock (4D+C) reduced width interface LVDS compatible data streams.

DS90C189-Q1 supports 2 modes of operation.

- In single pixel mode in/out mode, the device can drive up to SXGA+ (1400x1050) at 60 Hz. In this mode, the device converts one bank of 24-bit RGB data to a one channel 4D+C LVDS data stream.
- In single pixel in / dual pixel out mode, the device can drive up to WUXGA+ (1920x1440) at 60 Hz. In this configuration, the device provides single-to-dual pixel conversion and converts one bank of 24-bit RGB data into two channels of 4D+C LVDS streams at half the pixel clock rate.

For all the modes, the device supports 24bpp color.

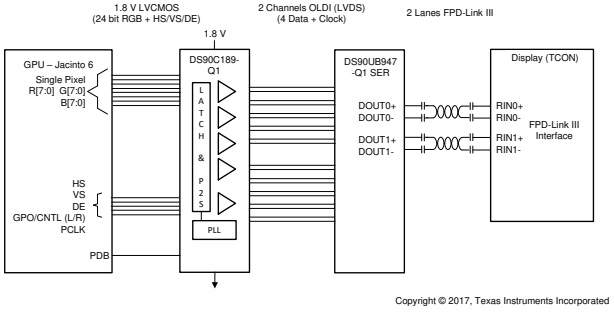
The DS90C189-Q1 is offered in a small 64 pin QFN package and features single 1.8 V supply for minimal power dissipation.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90C189-Q1	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the order addendum at the end of the data sheet.

4 Typical Application Diagrams



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5 Revision History

Changes from Revision A (August 2018) to Revision B (September 2020) **Page**

- Added note on GND tolerance to Abs Max table....6
- Added clarifications on VDD starting from GND during power sequence and power down/power up conditions....23

Changes from Revision * (May 2018) to Revision A (August 2018) **Page**

- Changed device status from Advanced Information to Production Data....1

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6 Pin Configuration and Functions

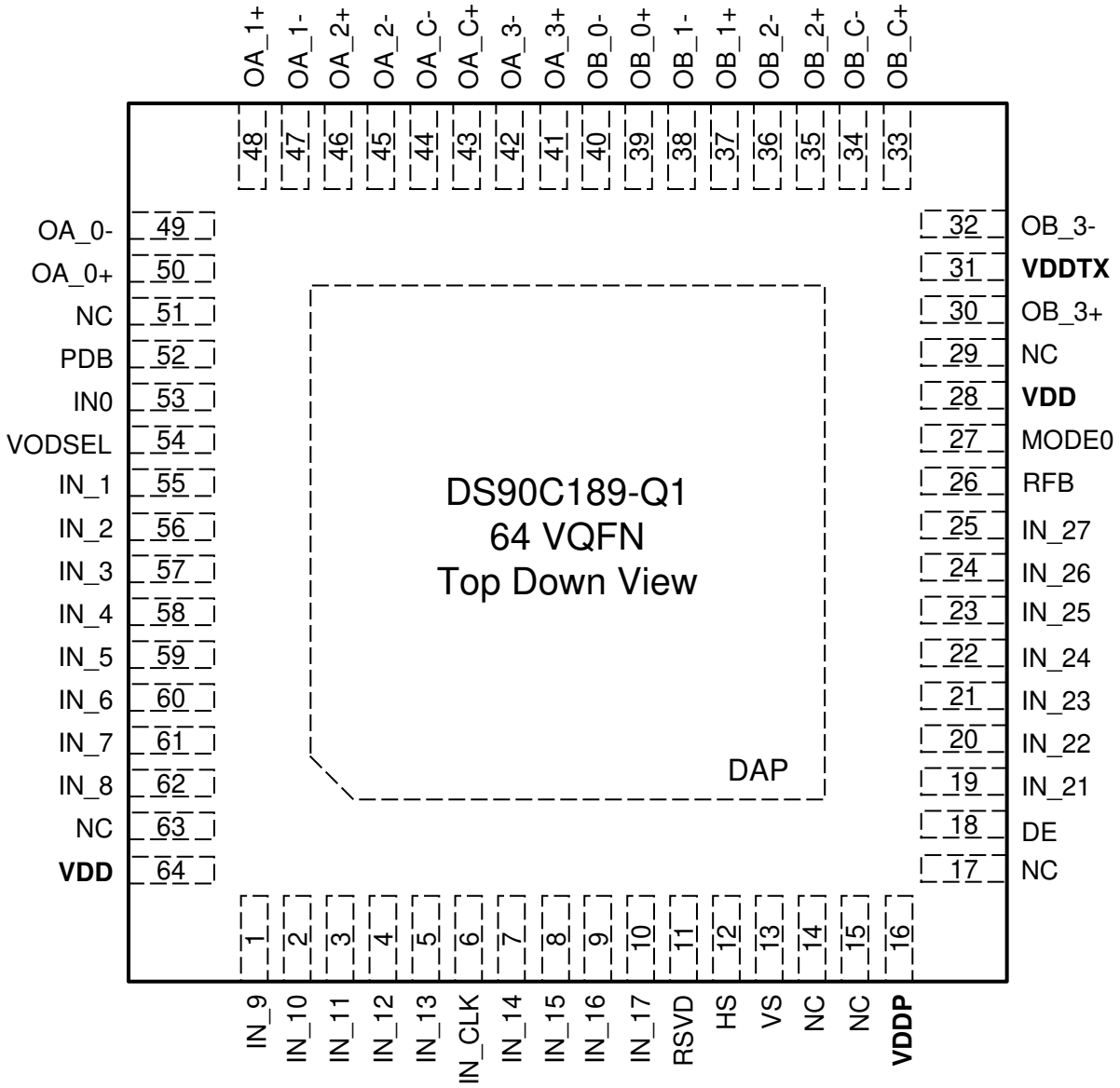

Figure 6-1. RTD Package 64-Pin VQFN Top View

DS90C189 Pin Descriptions

NAME	NO.	I/O	DESCRIPTION
1.8-V LVCMOS VIDEO INPUTS			
IN_[27:21], IN_[17:14], IN_[13:9], IN_[8:1] IN_[0]	25-19, 10-7, 5-1, 62-55, 53	I	Data Inputs Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit. Includes pull down.
HS, VS , DE	12, 13, 18	I	Video Control Signal Inputs - HS = Horizontal Sync, VS = Vertical SYNC, and DE = Data Enable
IN_CLK	6	I	Pixel Input Clock Includes pull down.
1.8-V LVCMOS CONTROL INPUTS			
MODE0	27	I	Mode Control Input (MODE0) - 0= Single In / Single Out 1= Single In / Dual Out Includes pull down.
RFB	26	I	Rising / Falling Clock Edge Select Input - 0 = Falling Edge 1 = Rising Edge Includes pull down.
PDB	52	I	Power Down (Sleep) Control Input - 0 = Sleep (Power Down mode) 1 = Device Active (enabled) Includes pull down.
VODSEL	54	I	VOD Level Select Input - 0 = Low swing 1 = Normal swing Includes pull down.
N/C	14, 15, 17, 29, 51, 63	I	**No Connect Pin – Leave Open**
RSVD	11	I	**Reserved – Tie to Ground.**
LVDS OUTPUTS			
OA_C+ OA_C-	43 44	O	Channel A LVDS Output Clock – Expects 100 Ω termination.
OA_[0]+, OA_[0]-	50 49	O	Channel A LVDS Output Data – Expects 100 Ω termination.
OA_[1]+, OA_[1]-	48 47	O	Channel A LVDS Output Data – Expects 100 Ω termination.
OA_[2]+, OA_[2]-	46 45	O	Channel A LVDS Output Data – Expects 100 Ω termination.
OA_[3]+, OA_[3]-	41 42	O	Channel A LVDS Output Data – Expects 100 Ω termination.
OB_C+, OB_C-	33 34	O	Channel B LVDS Output Clock – Expects 100 Ω termination.
OB_[0]+, OB_[0]-	39 40	O	Channel B LVDS Output Data – Expects 100 Ω termination.
OB_[1]+, OB_[1]-	37 38	O	Channel B LVDS Output Data – Expects 100 Ω termination.
OB_[2]+, OB_[2]-	35 36	O	Channel B LVDS Output Data – Expects 100 Ω termination.
OB_[3]+, OB_[3]-	30 32	O	Channel B LVDS Output Data – Expects 100 Ω termination.
POWER AND GROUND			
V_{DDTX}	31	P	Power supply for LVDS Drivers, 1.8 V.

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NAME	NO.	I/O	DESCRIPTION
V_{DD}	28, 64	P	Power supply pin for core, 1.8 V.
V_{DDP}	16	P	Power supply pin for PLL, 1.8 V.
DAP	DAP	G	**Connect DAP to Ground plane.**

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7 Specifications

7.1 Absolute Maximum Ratings

See (1) (2)

	MIN	MAX	UNIT
Supply Voltage (V_{DD})	−0.3	2.5	V
LVCMOS Input Voltage	−0.3	VDD + 0.3	V
LVDS Driver Output Voltage	−0.3	3.6	V
LVDS Output Short-Circuit Duration	Continuous		
Junction Temperature		150	°C
Storage Temperature (T_{stg})	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) GND tolerance +/-5mV compared to system GND

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±750	

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage	1.71	1.80	1.89	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
Differential Load Impedance	80	100	120	Ω
Supply Noise Voltage			<90	mV_{p-p}

7.4 Thermal Information

THERMAL METRIC(1)		DS90C189-Q1 RTD (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			$0.66V_{DD}$		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		$0.35V_{DD}$	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DD} = 1.71 V to 1.89 V		- 10	±1	+10	µA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω	VODSEL = V_{DD}	160 (320)	340 (680)	500 (1000)	mV (mV_{P-P})
			VODSEL = V_{GND}	110 (220)	220 (440)	400 (800)	mV (mV_{P-P})
ΔV_{OD}	Change in V_{OD} between Complimentary Output States	R_L = 100Ω See Figure 7-3				50	mV
V_{OS}	Offset Voltage	R_L = 100Ω See Figure 7-3		1.09	1.22	1.36	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States	R_L = 100Ω See Figure 7-3				50	mV
I_{OS}	Output Short-Circuit Current	V_{OUT} = GND, VODSEL = V_{DD}			−15.5		mA
SUPPLY CURRENT							
IDDT1	Worst Case Supply Current (includes load current)	Checkerboard pattern, R_L = 100 Ω, VODSEL = V_{DD}, V_{DD} = 1.89 V, See Checker Board Test Pattern	f = 105 MHz, MODE0 = GND (SISO)		50	85	mA
IDDT2			f = 185 MHz, MODE0 = V_{DD} (SIDO)		80	140	mA
IDDTP	Supply Current PRBS-7	MODE0 = V_{DD} (SIDO), f = 150 MHz, R_L = 100 Ω, PRBS-7 Pattern See Typ Current Draw - Single In/ Dual Out Mode - PRBS-7 Data Pattern.	VODSEL = GND, VDD = 1.8		50		mA
			VODSEL = V_{DD}, VDD = 1.8		70		mA
IDDTG	Supply Current 16 Grayscale	MODE0 = V_{DD} (SIDO), f = 150 MHz, R_L = 100 Ω, 16 Grayscale Pattern	VODSEL = GND, VDD = 1.8		53		mA
			VODSEL = V_{DD}, VDD = 1.8		71		mA
IDDZ	Power Down Supply Current	PDB = GND			6	800	µA

7.6 Recommended Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER			MIN	TYP	MAX	UNIT
TCIT	IN_CLK Transition Time Figure 7-5	MODE0 = GND	1		4	ns
		MODE0 = V_{DD}	1		2	ns
TCIP	IN_CLK Period Figure 7-6	MODE0 = GND	9.53	T(1)	40	ns
		MODE0 = V_{DD}	5.40	T	20	ns
TCIH	IN_CLK High Time	See Figure 7-6	0.35T	0.5T	0.65T	ns
TCIL	IN_CLK Low Time		0.35T	0.5T	0.65T	ns

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Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER			MIN	TYP	MAX	UNIT
TXIT	IN_n Transition Time	See Figure 7-5	1.5		0.3T	ns

(1) T = Typical Period of the input Clock.

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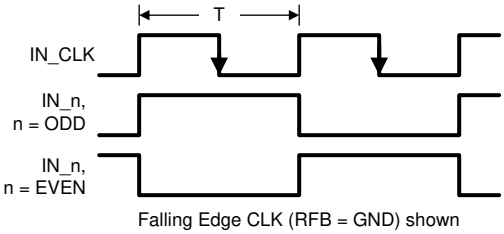
7.7 Switching Characteristics

Over recommended operating supply and temperature ranges unlessotherwise specified.

PARAMETER			MIN	TYP	MAX	UNIT
TSTC	IN_n Setup to IN_CLK	See Figure 7-6	0			ns
THTC	IN_n Hold from IN_CLK	See Figure 7-6	2.5			ns
LLHT	LVDS Low-to-High Transition Time See Figure 7-4			0.33		ns
LHLT	LVDS High-to-Low Transition Time See Figure 7-4			0.33		ns
TBIT	LVDS Output Bit Width	MODE0 = GND		1/7 TCIP		ns
		MODE0 = V_{DD}		2/7 TCIP		ns
TPPOS0	Transmitter Output Pulse Positions Normalized for Bit 0	See Figure 7-9		1		UI
TPPOS1	Transmitter Output Pulse Positions Normalized for Bit 1	See Figure 7-9		2		UI
TPPOS2	Transmitter Output Pulse Positions Normalized for Bit 2	See Figure 7-9		3		UI
TPPOS3	Transmitter Output Pulse Positions Normalized for Bit 3	See Figure 7-9		4		UI
TPPOS4	Transmitter Output Pulse Positions Normalized for Bit 4	See Figure 7-9		5		UI
TPPOS5	Transmitter Output Pulse Positions Normalized for Bit 5	See Figure 7-9		6		UI
TPPOS6	Transmitter Output Pulse Positions Normalized for Bit 6	See Figure 7-9		7		UI
Δ_TPPOS	Variation in Transmitter Pulse Position (Bit 6 — Bit 0)	See Figure 7-9		±0.06		UI
TCCS	LVDS Channel to Channel Skew			110		ps
TJCC	Jitter Cycle-to-Cycle	MODE0 = GND, f = 105 MHz		0.176		UI
TPLLS	Phase Lock Loop Set (Enable Time)	See Figure 7-7		1		ms
TPDD	Powerdown Delay	See Figure 7-8			100	ns
TSD	Latency Delay	MODE0 = GND See Figure 7-11		2*TCIP + 10.54	2*TCIP + 19.38	ns
TLAT	Latency Delay for Single Pixel In / Dual Pixel Out Mode	MODE0 = V_{DD} See Figure 7-10		9*TCIP + 4.19		ns

7.8 AC Timing Diagrams



Falling Edge CLK (RFB = GND) shown

A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.
B. Figure 7-2 shows a falling edge data strobe (IN_CLK).

Figure 7-1. Checker Board Test Pattern

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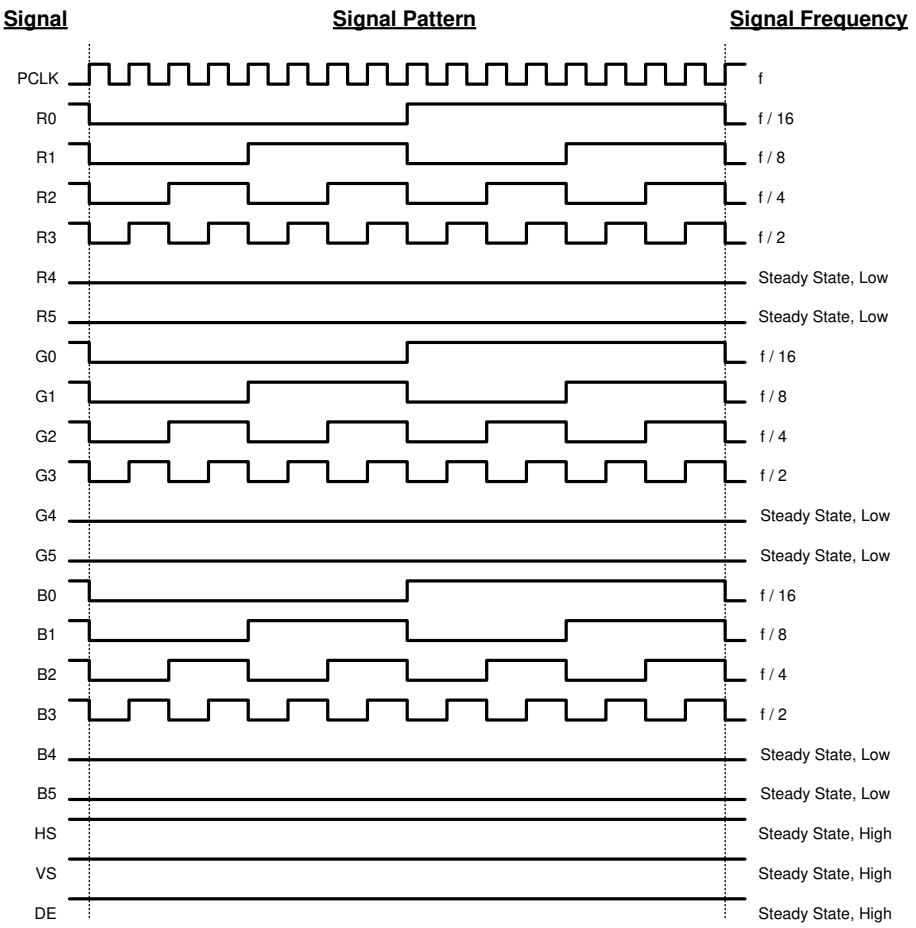

A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.
B. Recommended pin to signal mapping for 18 bits per pixel, customer may choose to define differently. The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
C. Figure 7-2 shows a falling edge data strobe (IN_CLK).

Figure 7-2. “16 Gray Scale” Test Pattern (Falling Edge Clock shown)

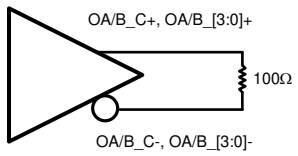

Figure 7-3. DS90C189-Q1 (Transmitter) LVDS Output Load

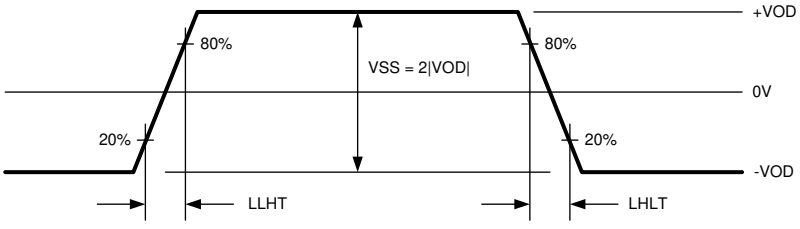

Figure 7-4. LVDS Output Transition Times

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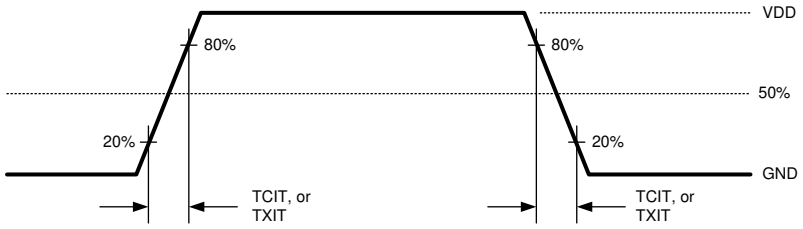

Figure 7-5. LVCMOS Input Transition Times

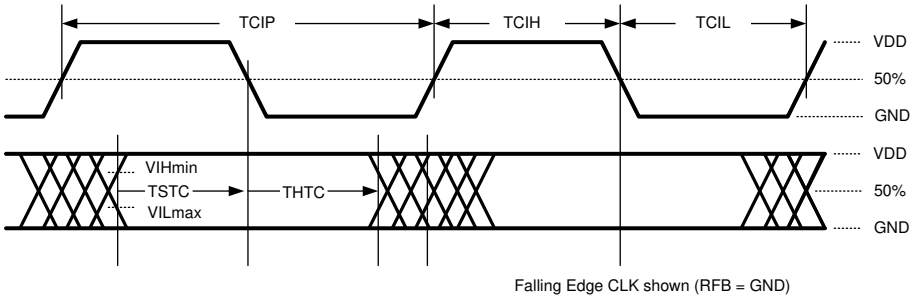

Figure 7-6. LVCMOS Input Setup/Hold and Clock High/Low Times (Falling Edge Strobe)

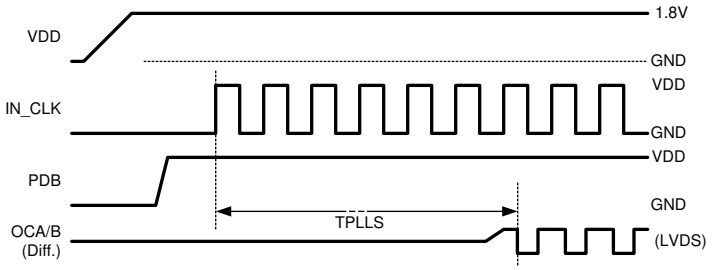

Figure 7-7. Start Up / Phase Lock Loop Set Time

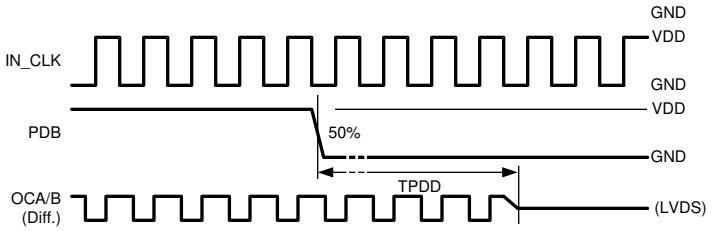

Figure 7-8. Sleep Mode / Power Down Delay

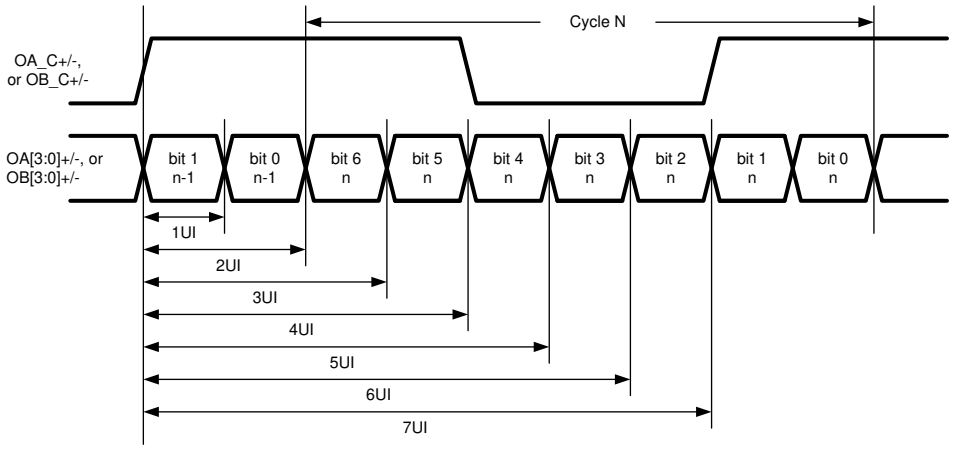

Figure 7-9. LVDS Serial Bit Positions

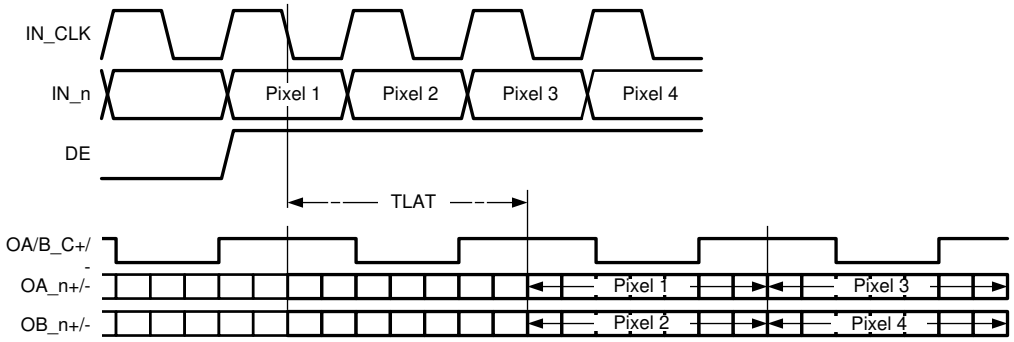

Figure 7-10. Single In, Dual Out Mode Timing and Latency

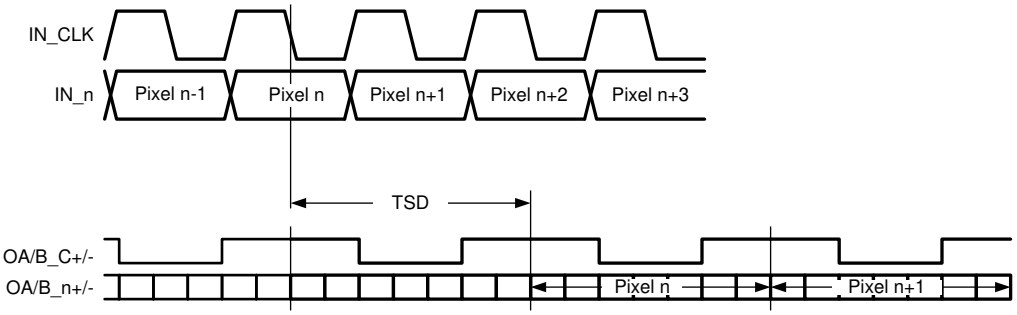

Figure 7-11. Single In, Single Out Mode Timing and Latency

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7.9 Typical Characteristics

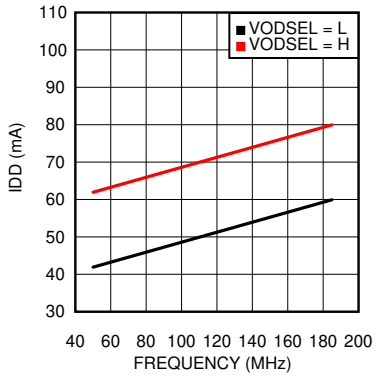

Figure 7-12. Typical Current Draw — Single In/Dual Out Mode — PRBS-7 Data Pattern

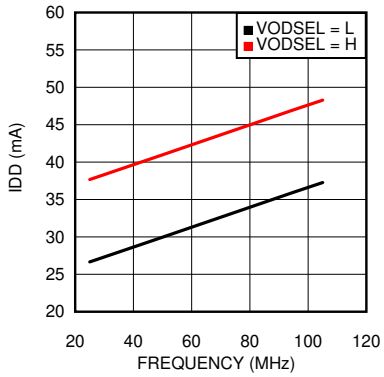

Figure 7-13. Typical Current Draw — Single In/ Single Out Mode — PRBS-7 Data Pattern

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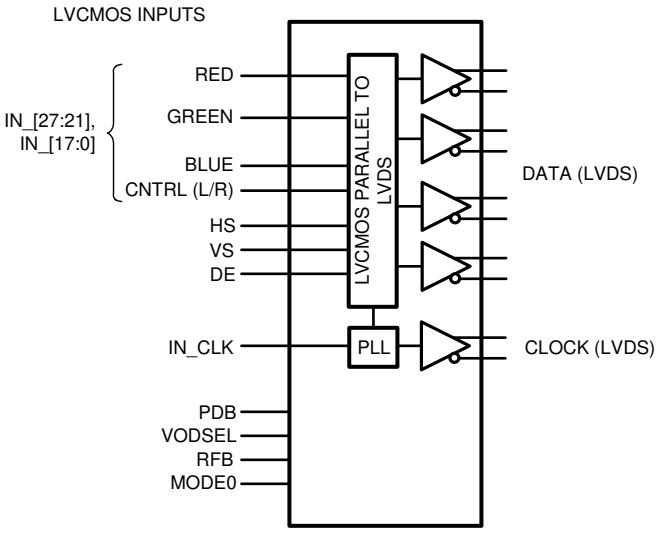
8 Detailed Description

8.1 Overview

DS90C189-Q1 converts a wide parallel LVCMOS input bus into banks of OLDI (LVDS) data. The device can be configured to support RGB-888 (24-bit color) in two main configurations: single pixel in / single pixel out; single pixel in / dual pixel out. The DS90C189-Q1 has power saving features including: selectable VOD and a power down pin control.

8.2 Functional Block Diagrams



DS90C189-Q1
Single Pixel In / Single Pixel Out (SISO)

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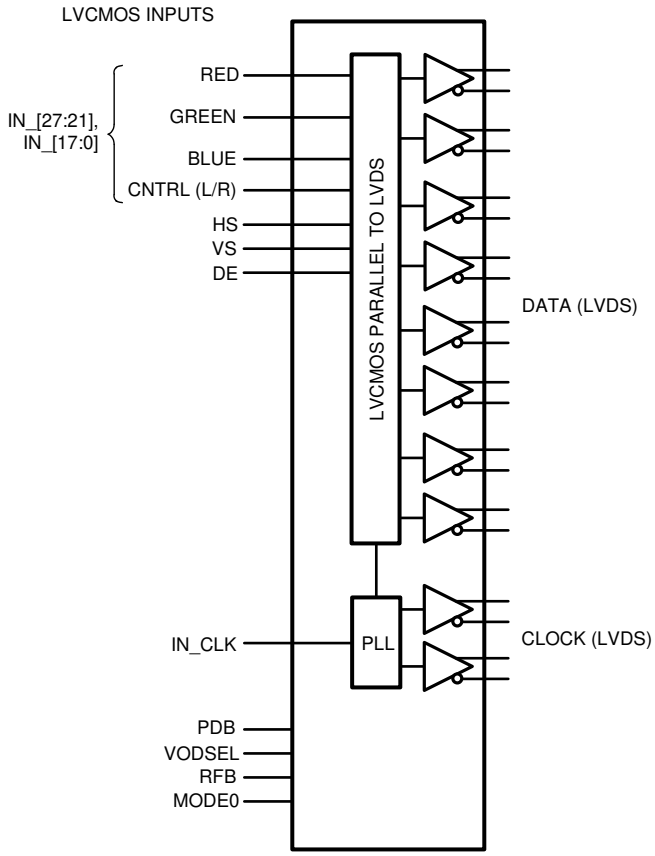

DS90C189-Q1
Single Pixel In / Dual Pixel Out (SIDO)

8.3 Feature Description

8.3.1 AEC-Q100 Qualified

The DS90C189-Q1 is qualified to AEC-Q100 Grade 2 standards and operates from -40°C to +105°C.

8.3.2 ESD Protection

The DS90C189-Q1 has a HBM ESD Classification Level of ±8 kV and CDM ESD Classification Level of ±750 V.

8.3.3 Operating Modes

The DS90C189-Q1 has two operating modes: Single Pixel In, Single Pixel Out (SISO), 25 MHz – 105 MHz and Single Pixel In, Dual Pixel Out (SIDO), 50 MHz – 185 MHz.

8.3.4 LVDS Configurations

The DS90C189-Q1 supports 3D+C, 4D+C, 6D+C, 6D+2C, 8D+C, and 8D+2C LVDS configurations.

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8.4 Device Functional Modes

8.4.1 Device Configuration

The MODE0 pin is used to configure the DS90C189-Q1 into the two main operation modes as shown in the table below.

Table 8-1. Mode Configurations

MODE0	CONFIGURATION
0	Single Pixel Input, Single Pixel Output (SISO)
1	Single Pixel Input, Dual Pixel Output (SIDO)

8.4.2 Single Pixel Input / Single Pixel Output

When MODE0 is set to low, data from IN_[27:21], IN_[17:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- with OA_C+/-.

In this configuration IN_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 700 Mbps (28 bits * 25MHz) to 2.94 Gbps (28 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA_C+/- will operate at the same rate as IN_CLK with a duty cycle ratio of 57:43.

8.4.3 Single Pixel Input / Dual Pixel Output

When MODE0 is HIGH, data from IN_[27:21], IN_[17:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- and OB_[3:0]+/- with OA_C+/- and OB_C+/-. The input LVCMOS data is split into odd and even pixels starting with the odd (first) pixel outputs OA_[3:0]+/- and then the even (second) pixel outputs OB_[3:0]+/-. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data (see Figure 7-10). **The number of clock cycles during blanking must be an EVEN number.** This configuration will allow the user to interface with two FPD-Link receivers or other dual pixel inputs.

In this configuration IN_CLK can range from 50 MHz to 185 MHz, resulting in a total maximum payload of 1.4 Gbps (28 bits * 50 MHz) to 5.18 Gbps (28 bits * 185 MHz). Each LVDS driver will operate at a speed of 7 bits per 2 input clock cycles, resulting in a serial line rate of 175 Mbps to 647.5 Mbps. OA_C+/- and OA_B+/- will operate at ½ the rate as IN_CLK with a duty cycle ratio of 57:43.

In the Single Pixel Input / Dual Pixel Output mode OA_x and OB_x can become misaligned if the clock or data is interrupted or PDB is toggled. If the clock or data is interrupted or PDB is toggled to prevent misalignment the following should be done:

1. Disable the clock and data.
2. Toggle PDB to Low and then High.
3. After PDB settles reset the data pattern and enable the clock and data.

8.4.4 Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the input LVCMOS data is latched on. If RFB is HIGH, input data is latched on the RISING EDGE of the pixel clock (IN_CLK). If RFB is LOW, the input data is latched on the FALLING EDGE of the pixel clock. Note: This can be set independently of receiver's output clock strobe.

Table 8-2. Pixel Clock Edge

RFB	Result
0	FALLING edge
1	RISING edge

8.4.5 Power Management

The DS90C189-Q1 has several features to assist with managing power consumption. The device can be configured through the MODE0 control pin to enable only the required number of LVDS drivers for each application. If no clock is applied to the IN_CLK pin, the DS90C189-Q1 will enter a low power state. To place the DS90C189-Q1 in its lowest power state, the device can be powered down by driving the PDB pin to LOW.

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8.4.6 Sleep Mode (PDB)

The DS90C189-Q1 provides a power down feature. When the device has been powered down, current draw through the supply pins is minimized and the PLL is shut down. The LVDS drivers are also powered down with their outputs pulled to GND through 100-Ω resistors (not tri-stated).

Table 8-3. Power Down Select

PDB	Result
0	SLEEP Mode (default)
1	ACTIVE (enabled)

8.4.7 LVDS Outputs

The DS90C189-Q1's LVDS drivers are compatible with ANSI/TIA/EIA-644-A LVDS receivers. The LVDS drivers can output a power saving low V_{OD}, or a high V_{OD} to enable longer trace and cable lengths by configuring the VODSEL pin.

Table 8-4. VOD Select

VODSEL	Result
0	±220 mV (440 mVpp)
1	±340 mV (680 mVpp)

Any unused LVDS outputs that are not powered down due to the MODE0 pin should be externally terminated differentially with a 100 ohm resistor. For example, when driving a timing controller (TCON) that only requires an 8D + C LVDS interface, rather than 8D + 2C, the unused clock line should be terminated near the package of the DS90C189-Q1. For more information regarding the electrical characteristics of the LVDS outputs, refer to the LVDS DC Characteristics and LVDS Switching Specifications.

8.4.8 LVCMOS Inputs

The DS90C189-Q1 has one bank of 24 data inputs, one set of video control signal (HS, VS and DE) inputs and several device configuration LVCMOS pins. All LVCMOS input pins are designed for 1.8 V LVCMOS logic. All LVCMOS inputs, including clock, data and configuration pins, have an internal pull down resistor to set a default state. If any inputs are unused, they can be left as no connect (NC) or connected to ground.

8.5 Programming

8.5.1 LVDS Interface / TFT Color Data Recommended Mapping

Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application. The DS90C189-Q1 supports two modes of operation for single and dual pixel applications supporting 24bpp color depths.

In the Dual Pixel / 24bpp mode, eight LVDS data lines are provided along with two LVDS clock lines (8D+2C). The Deserializer may utilize one or two clock lines. The 53 bit interface typically assigns 24 bits to RGB for the odd pixel, 24 bits to RGB for the even pixel, 3 bits for the video control signals (HS, VS and DE), 1 bit for odd pixel and 1 bit for even pixel which can be ignored or used for general purpose data, control or L/R signaling.

A reduced width input interface is also supported with a Single-to-Dual Pixel conversion where the data is presented at double rate (same clock edge, 2X speed, see Figure 7-10) and the DE transition is used to flag the first pixel. Also note in the 8D+2C configuration, the three video control signals are sent over **both** the A and B outputs. The DES / TCON may recover one set, or both depending upon its implementation. The Dual Pixel / 24bpp 8D+2C LVDS Interface Mapping is shown in Figure 8-1.

In the Single Pixel / 24bpp mode, four LVDS data lines are provided along with a LVDS clock line (4D+C). The 28 bit interface typically assigns 24 bits to RGB color data, 3 bits to video control (HS, VS and DE) and one spare bit can be ignored, used for L/R signaling or function as a general purpose bit. The Single Pixel / 24bpp 4D+C LVDS Interface Mapping is shown in Figure 8-2.

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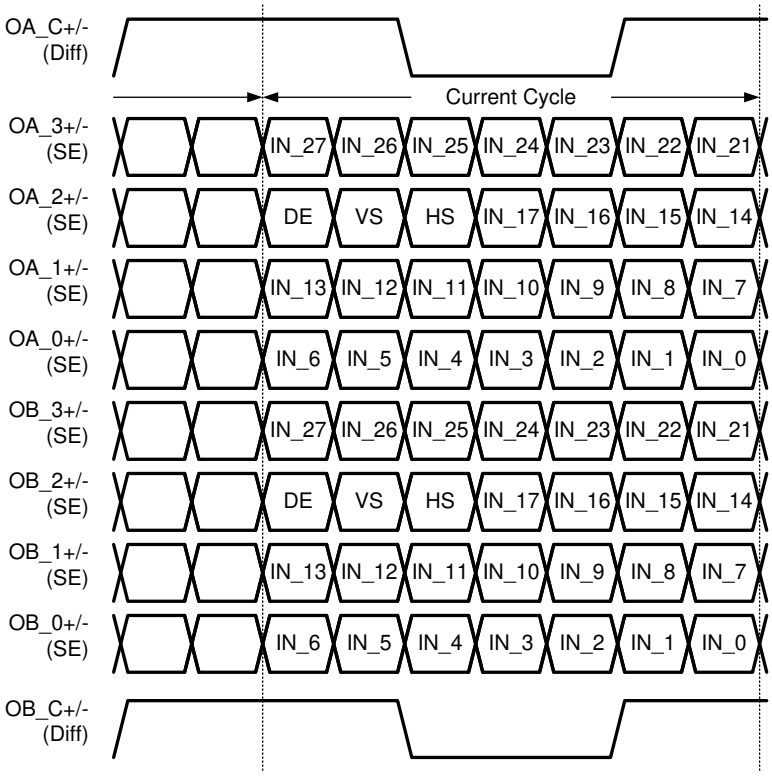

Figure 8-1. Dual Pixel / 24bpp LVDS Mapping

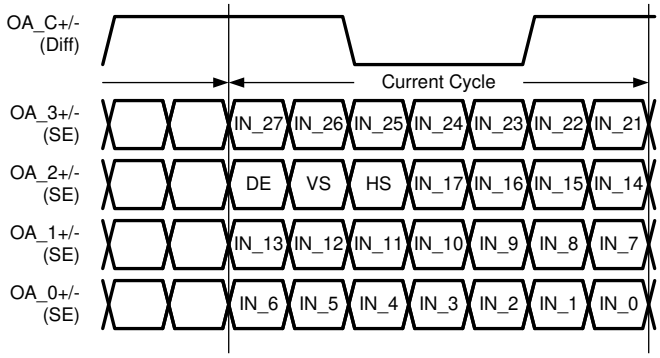

Figure 8-2. Single Pixel / 24bpp LVDS Mapping

8.5.1.1 Color Mapping Information

A defacto color mapping is shown next. Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application.

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Table 8-5. Single Pixel Input / 24bpp / MSB on CH3

DS90C189-Q1 Input	Color Mapping	Note
IN_22	R7	MSB
IN_21	R6	
IN_5	R5	
IN_4	R4	
IN_3	R3	
IN_2	R2	
IN_1	R1	
IN_0	R0	LSB
IN_24	G7	MSB
IN_23	G6	
IN_11	G5	
IN_10	G4	
IN_9	G3	
IN_8	G2	
IN_7	G1	
IN_6	G0	LSB
IN_26	B7	MSB
IN_25	B6	
IN_17	B5	
IN_16	B4	
IN_15	B3	
IN_14	B2	
IN_13	B1	
IN_12	B0	
DE	DE	Data Enable(1)
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
IN_27	GP	General Purpose

(1) See section *Section 8.4.3*.

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Table 8-6. Single Pixel Input / 24bpp / LSB on CH3

DS90C189-Q1 Input	Color Mapping	Note
IN_5	R7	MSB
IN_4	R6	
IN_3	R5	
IN_2	R4	
IN_1	R3	
IN_0	R2	
IN_22	R1	
IN_21	R0	LSB
IN_11	G7	MSB
IN_10	G6	
IN_9	G5	
IN_8	G4	
IN_7	G3	
IN_6	G2	
IN_24	G1	
IN_23	G0	LSB
IN_17	B7	MSB
IN_16	B6	
IN_15	B5	
IN_14	B4	
IN_13	B3	
IN_12	B2	
IN_26	B1	
IN_25	B0	
DE	DE	Data Enable(1)
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
IN_27	GP	General Purpose

(1) See section *Section 8.4.3*.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90C189-Q1 is a Low Power Bridge for automotive application that reduces the size of the RGB interface between the host GPU and the Display. It is designed to support single pixel data transmission between Host and Flat Panel Display up to QXGA (2048x1536) at 60 Hz resolutions. The transmitter converts up to 24 bits (Single Pixel 24 bit color) of 1.8-V LVCMOS data into two channels of 4 data + clock (4D+C) reduced width interface LVDS compatible data streams.

9.2 Typical Application

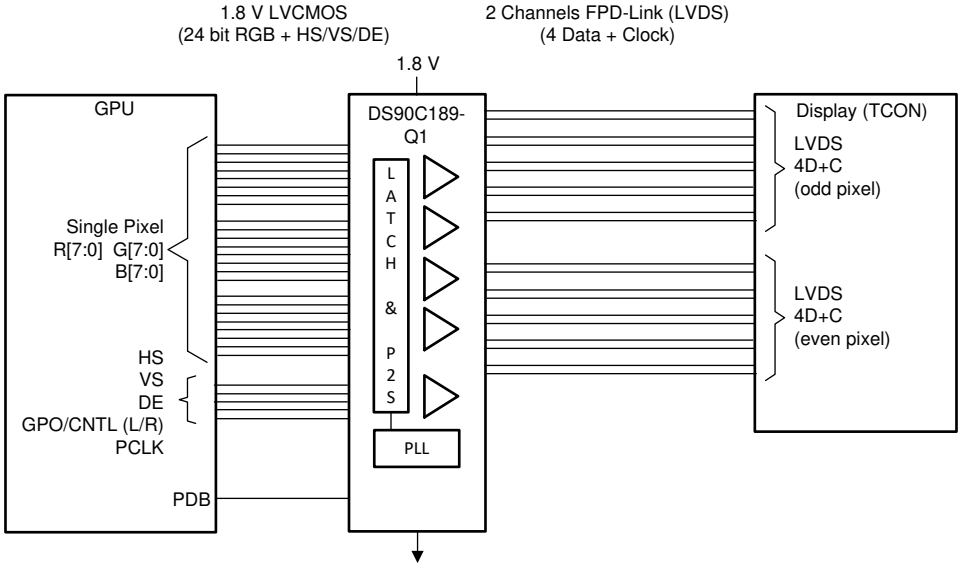

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Figure 9-1. Single Pixel In Dual Pixel Out (SIDO) Mode

9.2.1 Design Requirements

The DS90C189-Q1 is used to convert 24-bit color to two channels of LVDS datastreams.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Supply	1.8V
Display Driven	SXGA+, WUXGA+
Pixel Depth	24 bits

9.2.2 Detailed Design Procedure

9.2.2.1 LVDS Interconnect Guidelines

Refer to the *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use differential connectors when above 500 Mbps
- Minimize skew within the pair
- Use the S/2S/3S rule in spacings
  - S = space between the pairs
  - 2S = space between pairs
  - 3S = space to LVCMOS signals
- Place ground vias next to signal vias when changing between layers
- When a signal changes reference planes, place a bypass cap and vias between the new and old reference plane

For more tips and detailed suggestions regarding high speed board layout principles, see the LVDS Owner's Manual at http://www.ti.com/lvds

9.2.3 Application Curves

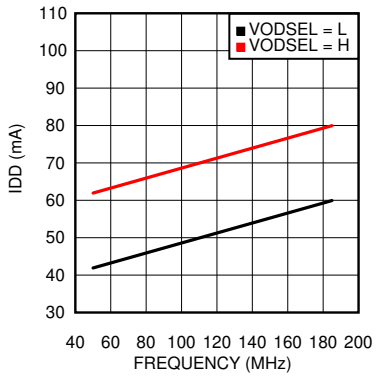

Figure 9-2. Typical Current Draw - Single In/Dual Out Mode - PRBS-7 Data Pattern

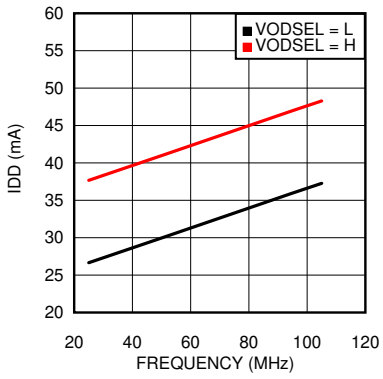

Figure 9-3. Typical Current Draw - Single In/Single Out Mode - PRBS-7 Data Pattern

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10 Power Supply Recommendations

10.1 Power Up Sequence

The VDD power supply ramp should start from GND +/-5mV and ramp monotonically to the recommended supply voltage. The V_{DD} power supply pins do not require a specific power on sequence and can be powered on in any order. However, the PDB pin should only be set to logic HIGH once the power sent to all supply pins is stable. Active data inputs should not be applied to the DS90C189-Q1 until all of the input power pins have been powered on, settled to the recommended operating voltage and the PDB pin has be set to logic HIGH.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (DS90C189-Q1 PDB input initially LOW):

1. Ensure that all supply pins are at GND +/-5mV
2. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
3. Toggle DS90C189-Q1 power down pin to PDB = V_{DD}.
4. Enable clock and wait for additional 0-200ms to ensure display noise won't occur.
5. Enable video source output; start sending black video data.
6. Send >1ms of black video data; this allows the DS90C189-Q1 to be phase locked, and the display to show black data first.
7. Start sending true image data.
8. Enable backlight.

Power Down sequence (DS90C189-Q1 PDB input initially HIGH):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set DS90C189-Q1 power down pin to PDB = GND.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.
6. Ensure that VDD supply discharges to GND +/- 5mV before starting the next power up sequence. If rapid power off/on system behavior is required, then it is recommended to utilize a discharge circuit to ensure VDD returns to GND +/- 5mV between power off/on conditions

10.2 Power Supply Filtering

The DS90C189-Q1 has several power supply pins at 1.8 V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of at least one 0.1µF capacitor placed on each pin, with an additional 4.7 µF - 22 µF capacitor placed on the PLL supply pin (VDDP). 0.01 µF capacitors are typically recommended for each pin. Additional filtering including ferrite beads may be necessary for noisy systems. It is recommended to place a 0 ohm resistor at the bypass capacitors that connect to each power pin to allow for additional filtering if needed. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 µF — 100 µF range.

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11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense pcbs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency. Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

For more information on the VQFN package, refer to the *AN-1187 Leadless Leadframe Package (LLP)* application note (SNOA401).

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11.2 Layout Example

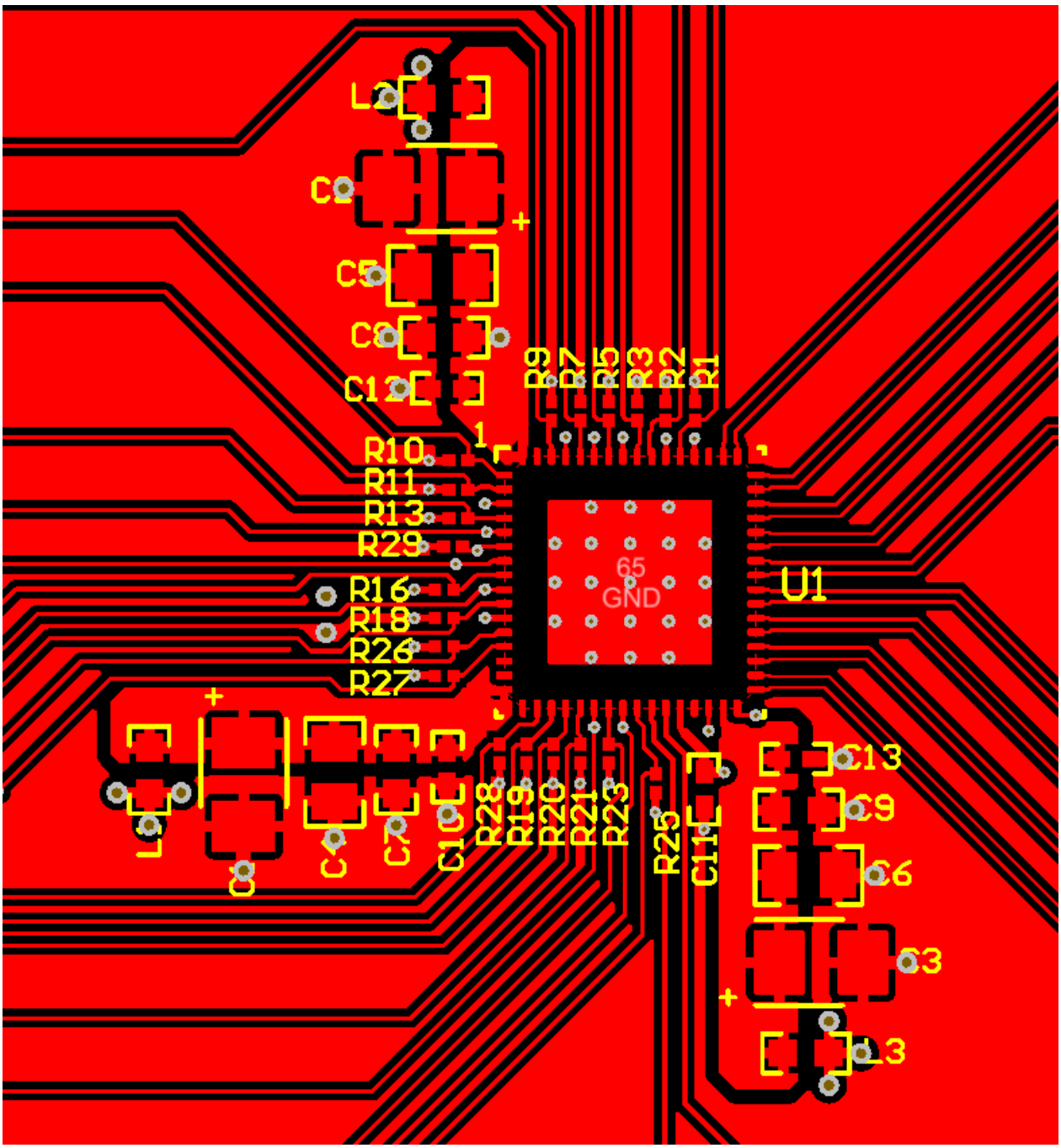

Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see:

- *LVDS Owner's Manual* (SNLA187)
- *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008)
- *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035)
- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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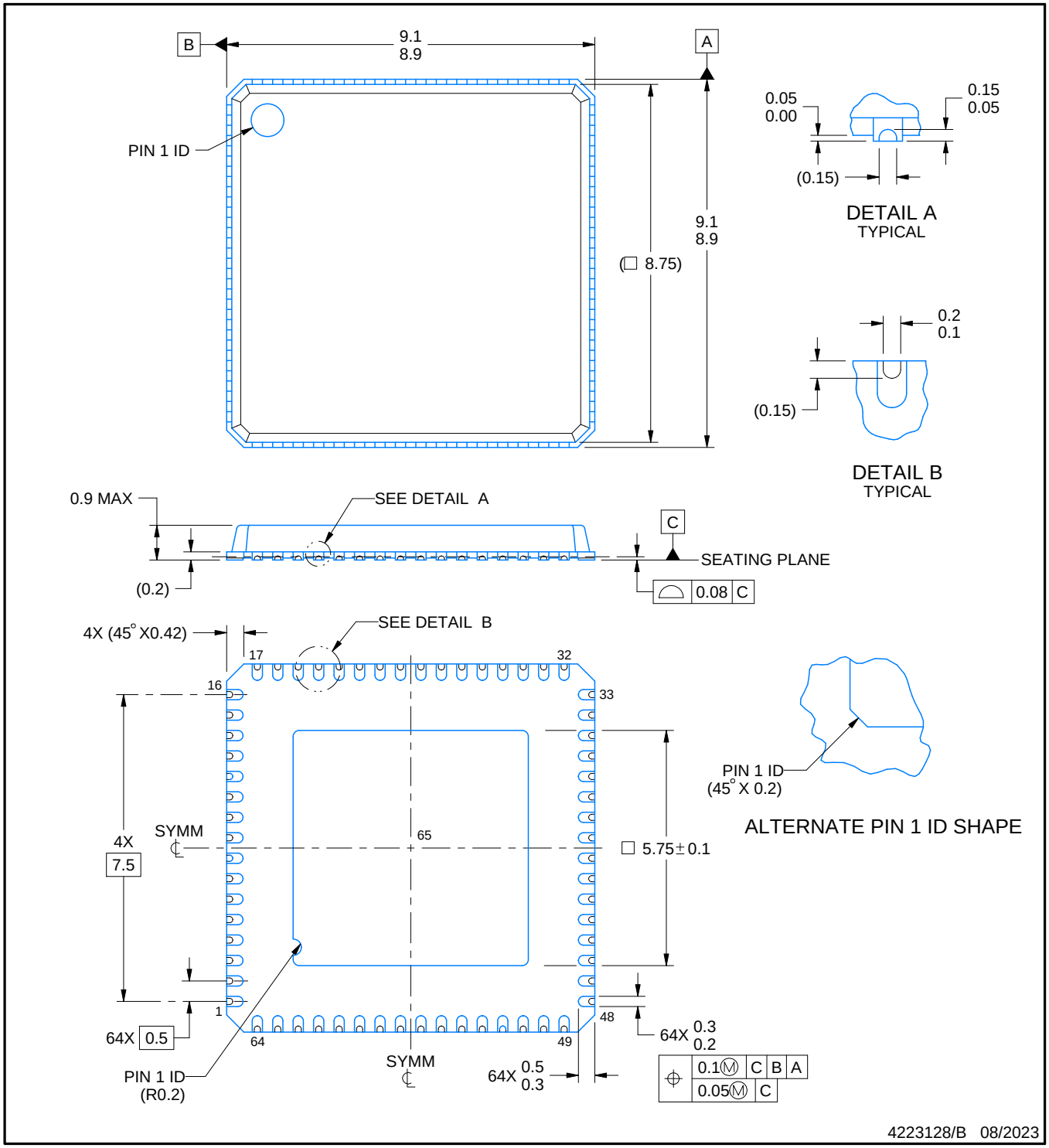
RTD0064F

PACKAGE OUTLINE

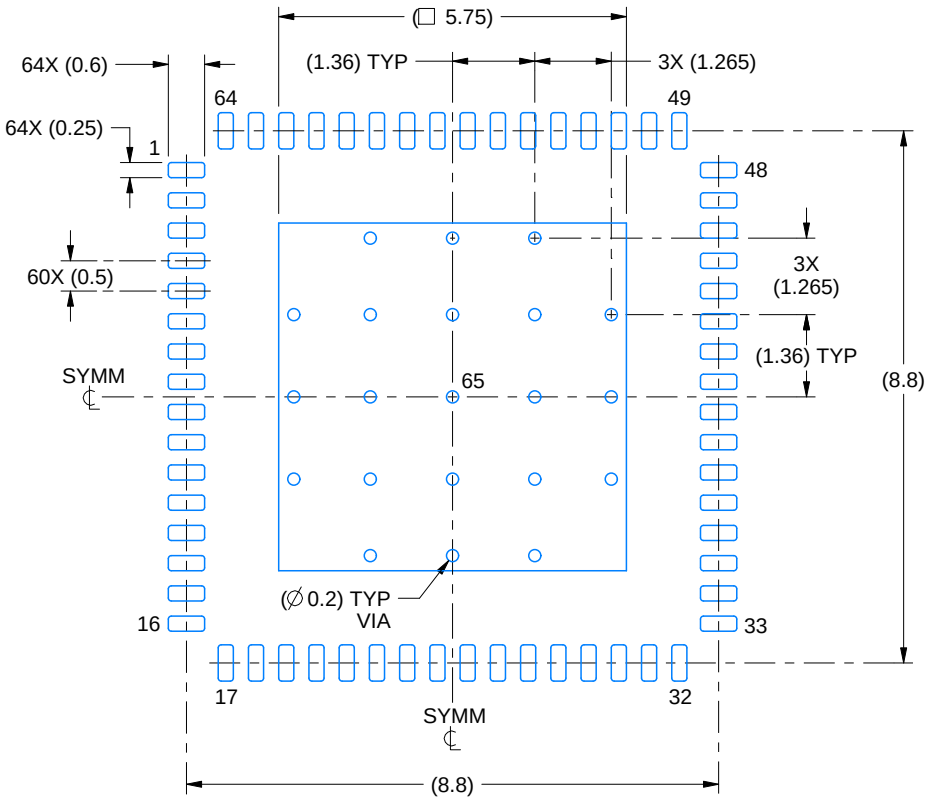
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

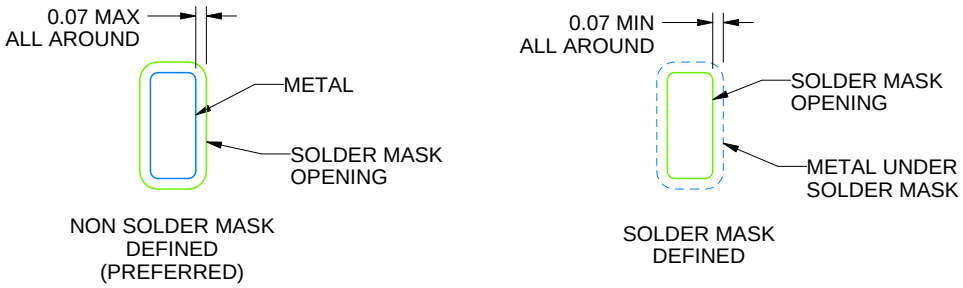


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

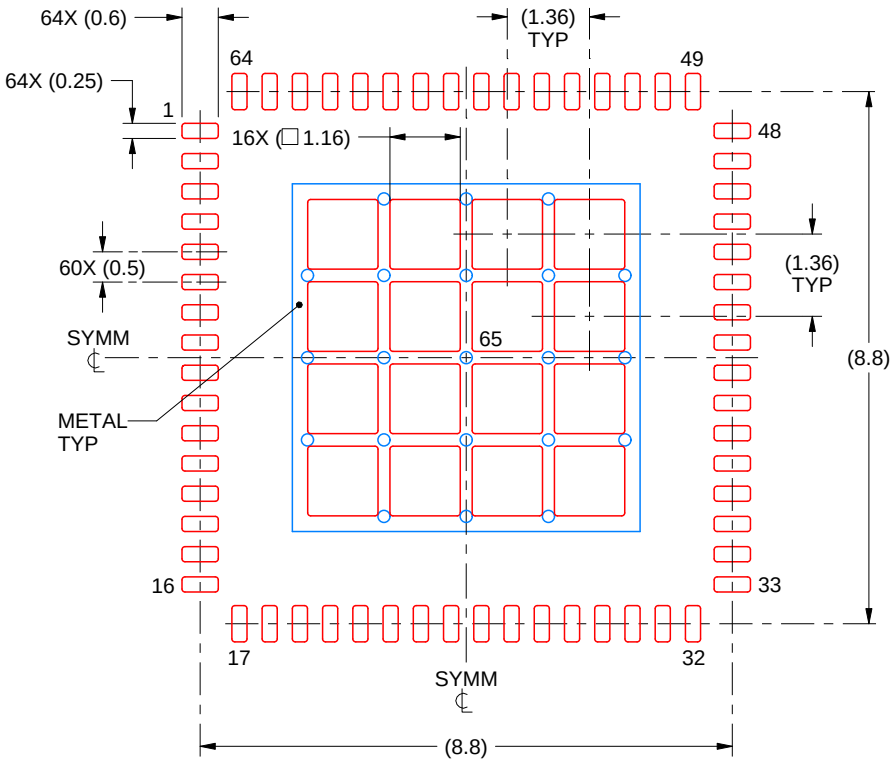


SOLDER MASK DETAILS

4223128/B 08/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

4223128/B 08/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C189TWRTDRQ1	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 115	DS90C189Q	Samples
DS90C189TWRTDTQ1	ACTIVE	VQFN	RTD	64	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 115	DS90C189Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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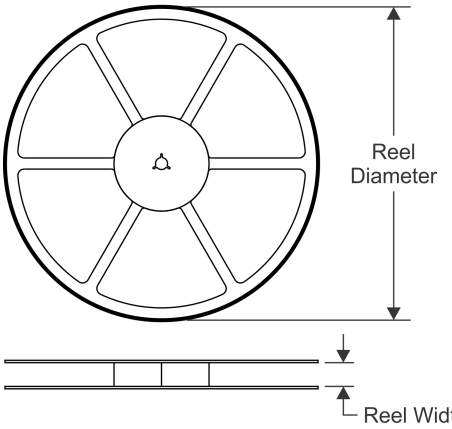
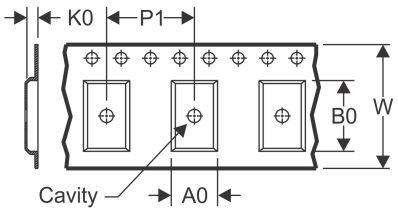
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

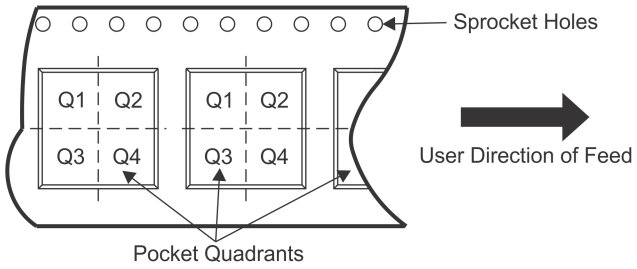


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

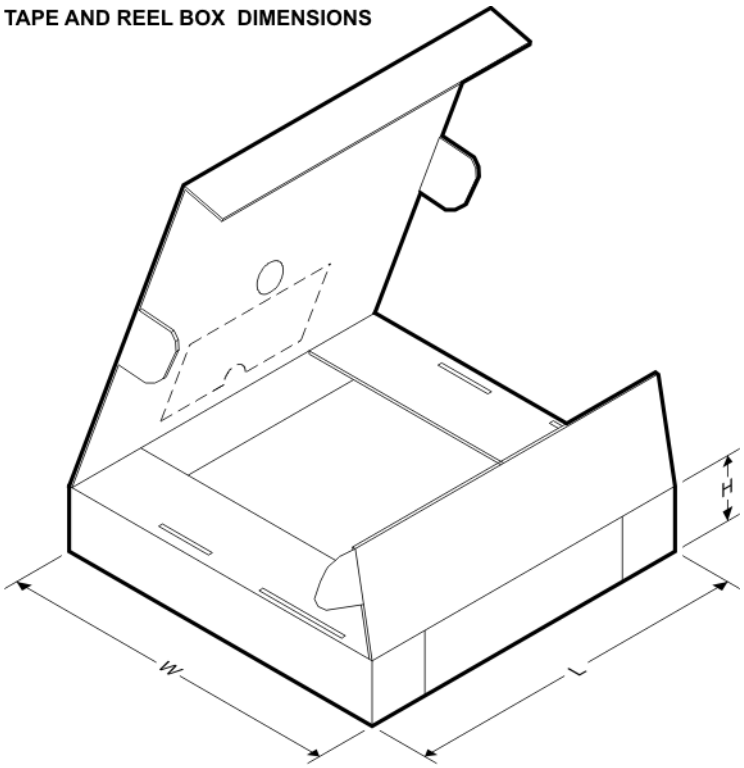
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C189TWRTDRQ1	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90C189TWRTDTQ1	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

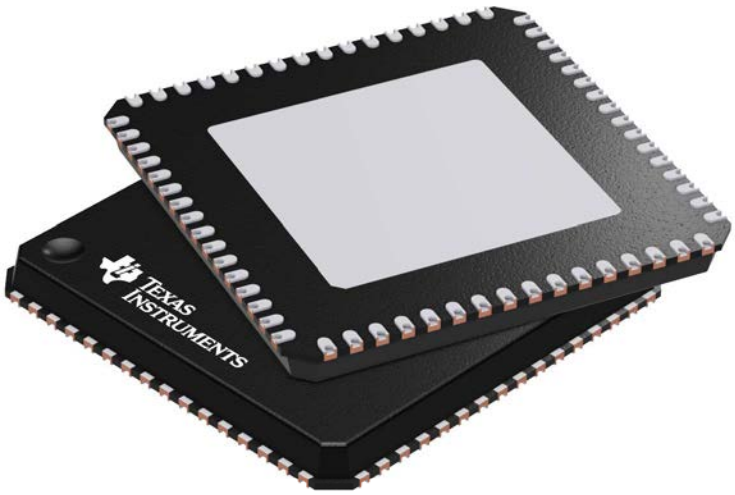
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C189TWRTDRQ1	VQFN	RTD	64	2500	367.0	367.0	38.0
DS90C189TWRTDTQ1	VQFN	RTD	64	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RTD 64

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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