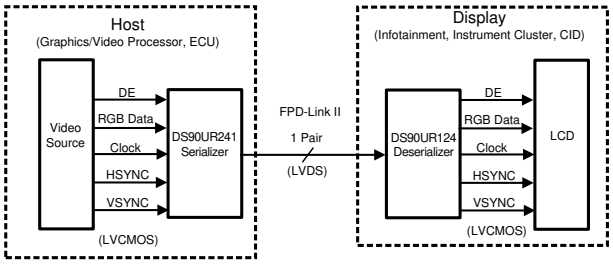
DS90URxxx-Q1 5MHz to 43MHz DC-Balanced 24-Bit FPD-Link II Serializer and Deserializer Chipset

1 Features

- Supports displays with 18-bit color depth
- 5MHz to 43MHz Pixel clock
- Automotive-grade product AEC-Q100 grade 2 qualified
- 24:1 Interface compression
- Embedded clock with DC balancing supports AC-coupled data transmission
- Capable to drive up to 10 meters shielded twisted-pair cable
- No reference clock required (deserializer)
- Meets ISO 10605 ESD – greater than 8kV HBM ESD structure
- Hot plug support
- EMI reduction – serializer accepts spread spectrum input; data randomization and shuffling on serial link; deserializer provides adjustable PTO (Progressive Turnon) LVCMOS outputs
- @Speed BIST (Built-In Self-Test) to validate LVDS transmission path
- Individual power-down controls for both transmitter and receiver
- Power supply range 3.3V ±10%
- 48-pin TQFP package for transmitter and 64-pin TQFP package for receiver
- Temperature range: –40°C to 105°C
- Backward-compatible mode with DS90C241/ DS90C124

2 Applications

- Automotive central information displays
- Automotive instrument cluster displays
- Automotive heads-up displays
- Remote camera-based driver assistance systems



Applications Diagram

3 Description

The DS90URxxx-Q1 chipset translates a 24-bit parallel bus into a fully transparent data/control FPD-Link II LVDS serial stream with embedded clock information. This chipset is designed for driving graphical data to displays requiring 18-bit color depth: RGB666 + HS, VS, DE + three additional general-purpose data channels. This single serial stream simplifies transferring a 24-bit bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. The device saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

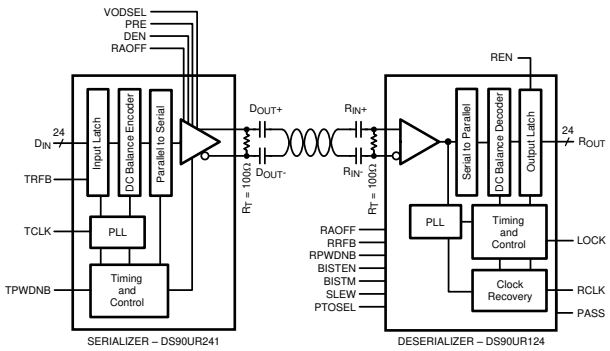
The DS90URxxx-Q1 incorporates FPD-Link II LVDS signaling on the high-speed I/O. FPD-Link II LVDS provides a low-power and low-noise environment for reliably transferring data over a serial transmission path. By optimizing the Serializer output edge rate for the operating frequency range, EMI is further reduced.

In addition, the device features pre-emphasis to boost signals over longer distances using lossy cables. Internal DC-balanced encoding and decoding is used to support AC-coupled interconnects. Using TI's proprietary random lock, the parallel data of the Serializer are randomized to the Deserializer without the need of REFCLK.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
DS90UR124-Q1	TQFP (64)	10.00mm × 10.00mm
DS90UR241-Q1	TQFP (48)	7.00mm × 7.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

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4 Pin Configuration and Functions

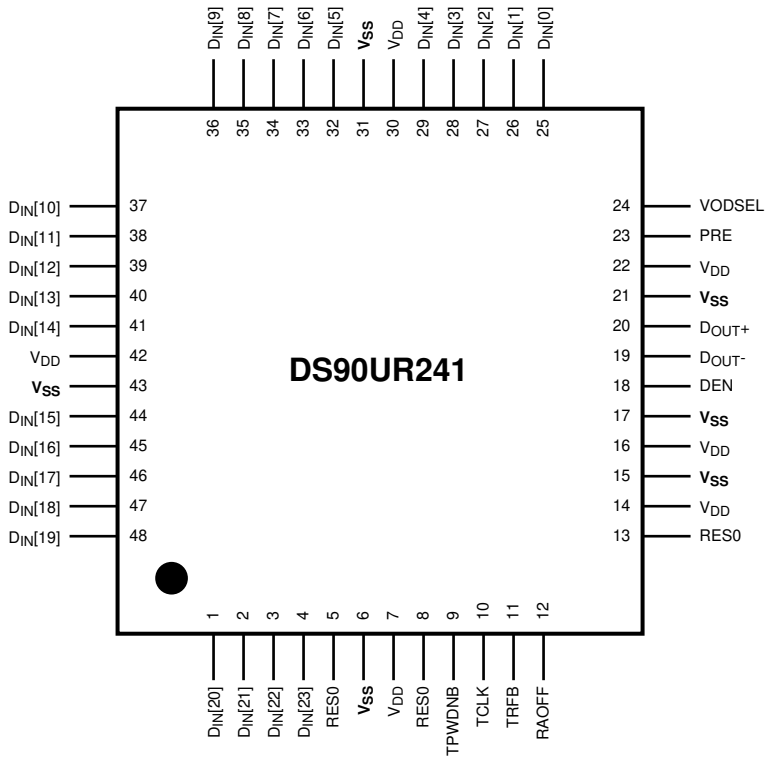


Figure 4-1. PFB Package
48-Pin TQFP
Top View

Table 4-1. Pin Functions: PFB Package

PIN		I/O	DESCRIPTION
NO.	NAME		
LVCMOS PARALLEL INTERFACE PINS			
4-1, 48-44, 41-32, 29-25	D_{IN}[23:0]	LVCMOS_I	Transmitter Parallel Interface Data Input Pins. Tie LOW if unused; do not float.
10	TCLK	LVCMOS_I	Transmitter Parallel Interface Clock Input Pin. Strobe edge set by TRFB configuration pin.
CONTROL AND CONFIGURATION PINS			
18	DEN	LVCMOS_I	Transmitter Data Enable DEN = H; LVDS Driver Outputs are Enabled (ON). DEN = L; LVDS Driver Outputs are Disabled (OFF), Transmitter LVDS Driver D_{OUT} (+/-) Outputs are in Tri-state, PLL still operational and locked to TCLK.
23	PRE	LVCMOS_I	Pre-emphasis Level Select PRE = NC (No Connect); Pre-emphasis is Disabled (OFF). Pre-emphasis is active when input is tied to VSS through external resistor R_{PRE}. Resistor value determines pre-emphasis level. Recommended value R_{PRE} ≥ 6kΩ; I_{max} = [48 / R_{PRE}], $R_{PRE\ min}$ = 6kΩ
12	RAOFF	LVCMOS_I	Randomizer Control Input Pin RAOFF = H, Backwards compatible mode for use with DS90**C**124 Deserializer. RAOFF = L; Additional randomization ON (Default), Selects 2E7 LSFR setting. See Table 6-1 for more details.
5, 8, 13	RES0	LVCMOS_I	Reserved. This pin **must** be tied LOW.

Table 4-1. Pin Functions: PFB Package (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
9	TPWDNB	LVCMOS_I	Transmitter Power Down Bar TPWDNB = H; Transmitter is Enabled and ON TPWDNB = L; Transmitter is in power down mode (Sleep), LVDS Driver D_{OUT} (+/-) Outputs are in Tri-state stand-by mode, PLL is shutdown to minimize power consumption.
11	TRFB	LVCMOS_I	Transmitter Clock Edge Select Pin TRFB = H; Parallel Interface Data is strobed on the Rising Clock Edge. TRFB = L; Parallel Interface Data is strobed on the Falling Clock Edge
24	VODSEL	LVCMOS_I	VOD Level Select VODSEL = L; LVDS Driver Output is ±500 mV (R_L = 100Ω) VODSEL = H; LVDS Driver Output is ±900 mV (R_L = 100Ω) For normal applications, set this pin LOW. For long cable applications where a larger VOD is required, set this pin HIGH.
LVDS SERIAL INTERFACE PINS			
20	D_{OUT+}	LVDS_O	Transmitter LVDS True **(+)** Output. This output is intended to be loaded with a 100Ω load to the D_{OUT+} pin. The interconnect must be AC coupled to this pin with a 100nF capacitor.
19	D_{OUT-}	LVDS_O	Transmitter LVDS Inverted **(-)** Output This output is intended to be loaded with a 100Ω load to the D_{OUT-} pin. The interconnect must be AC coupled to this pin with a 100nF capacitor.
POWER / GROUND PINS			
22	VDD	VDD	Analog Voltage Supply, LVDS Output POWER
16	VDD	VDD	Analog Voltage Supply, VCO POWER
14	VDD	VDD	Analog Voltage Supply, PLL POWER
30	VDD	VDD	Digital Voltage Supply, Serializer POWER
7	VDD	VDD	Digital Voltage Supply, Serializer Logic POWER
42	VDD	VDD	Digital Voltage Supply, Serializer INPUT POWER
21	VSS	GND	Analog Ground, LVDS Output GROUND
17	VSS	GND	Analog Ground, VCO GROUND
15	VSS	GND	Analog Ground, PLL GROUND
31	VSS	GND	Digital Ground, Serializer GROUND
6	VSS	GND	Digital Ground, Serializer Logic GROUND
43	VSS	GND	Digital Ground, Serializer Input GROUND

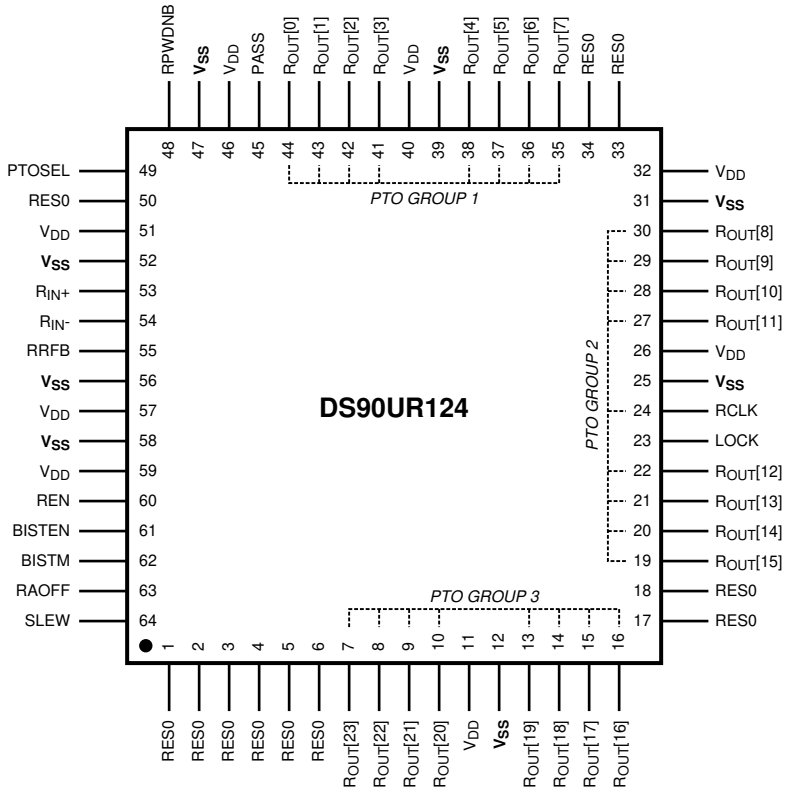


Figure 4-2. PAG Package
64-Pin TQFP
Top View

Table 4-2. Pin Functions: PAG Package

PIN		I/O	DESCRIPTION
NO.	NAME		
LVCMOS PARALLEL INTERFACE PINS			
24	RCLK	LVCMOS_O	Parallel Interface Clock Output Pin. Strobe edge set by RRFB configuration pin.
35-38, 41-44	R_{OUT}[7:0]	LVCMOS_O	Receiver Parallel Interface Data Outputs – Group 1
19-22, 27-30	R_{OUT}[15:8]	LVCMOS_O	Receiver Parallel Interface Data Outputs – Group 2
7-10, 13-16	R_{OUT}[23:16]	LVCMOS_O	Receiver Parallel Interface Data Outputs – Group 3
CONTROL AND CONFIGURATION PINS			
23	LOCK	LVCMOS_O	LOCK indicates the status of the receiver PLL LOCK = H; receiver PLL is locked LOCK = L; receiver PLL is unlocked, R_{OUT}[23-0] and RCLK are at Tri-state.
49	PTOSEL	LVCMOS_I	Progressive Turn On Operation Selection PTO = H; R_{OUT}[23:0] are grouped into three groups of eight, with each group switching about ±1 UI to ±2 UI apart relative to RCLK. *(Figure 5-15)* PTO = L; PTO Spread Mode, R_{OUT}[23:0] outputs are spread ±1 UI to ±2 UI and RCLK spread ±1 UI. *(Figure 5-16)* See Applications Information section for more details.
63	RAOFF	LVCMOS_I	Randomizer Control Input Pin (See Table 2 for more details.) RAOFF = H, Backwards compatible mode for use with DS90**C**241 Serializer. RAOFF = L; Additional randomization ON (Default), Selects 2E7 LSFR setting.
60	REN	LVCMOS_I	Receiver Data Enable REN = H; R_{OUT}[23-0] and RCLK are Enabled (ON). REN = L; R_{OUT}[23-0] and RCLK are Disabled (OFF), Receiver R_{OUT}[23-0] and RCLK Outputs are in Tri-state, PLL still operational and locked to TCLK.

Table 4-2. Pin Functions: PAG Package (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
50	RES0	LVCMOS_I	Reserved. This pin **MUST** be tied LOW.
1-6, 17, 18, 33, 34	RES0	NC	No Connection. Pins are not physically connected to the die. Recommendation is to leave pin open or tie to LOW.
48	RPWDNB	LVCMOS_I	Receiver Power Down Bar RPWDNB = H; Receiver is Enabled and ON RPWDNB = L; Receiver is in power down mode (Sleep), R_{OUT}[23-0], RCLK, and LOCK are in Tri-state standby mode, PLL is shutdown to minimize power consumption.
55	RRFB	LVCMOS_I	Receiver Clock Edge Select Pin RRFB = H; R_{OUT} LVCMOS Outputs strobed on the Rising Clock Edge. RRFB = L; R_{OUT} LVCMOS Outputs strobed on the Falling Clock Edge.
64	SLEW	LVCMOS_I	LVCMOS Output Slew Rate Control SLEW = L; Low drive output at 2mA (default) SLEW = H; High drive output at 4mA
BIST MODE PINS (See *Section Application and Implementation* for more details.)			
61	BISTEN	LVCMOS_I	Control Pin for BIST Mode Enable BISTEN = L; Default at Low, Normal Mode. BISTEN = H; BIST mode active. When BISTEN = H and DS90UR241 DIN[23:0] = Low or Floating; device goes to BIST mode accordingly. Check PASS output pin for test status.
62	BISTM	LVCMOS_I	BIST Mode selection. Control pin for which Deserializer is set for BIST reporting mode. BISTM = L; Default at Low, Status of all R_{OUT} with respective bit error on cycle-by-cycle basis BISTM = H; Total accumulated bit error count provided on ROUT[7:0] (binary counter up to 255)
45	PASS	LVCMOS_O	Pass flag output for @Speed BIST Test operation. PASS = L; BIST failure PASS = H; LOCK = H before BIST can be enabled, then $1x10^{-9}$ error rate achieved across link.
LVDS SERIAL INTERFACE PINS			
53	R_{IN+}	LVDS_I	Receiver LVDS True **(+)** Input — This input is intended to be terminated with a 100Ω load to the R_{IN+} pin. The interconnect must be AC Coupled to this pin with a 100nF capacitor.
54	R_{IN-}	LVDS_I	Receiver LVDS Inverted **(−)** Input — This input is intended to be terminated with a 100Ω load to the R_{IN-} pin. The interconnect must be AC Coupled to this pin with a 100nF capacitor.
POWER / GROUND PINS			
51	VDD	VDD	Analog LVDS Voltage Supply, POWER
59	VDD	VDD	Analog Voltage Supply, PLL POWER
57	VDD	VDD	Analog Voltage supply, PLL VCO POWER
32	VDD	VDD	Digital Voltage Supply, LOGIC POWER
46	VDD	VDD	Digital Voltage Supply, LOGIC POWER
40	VDD	VDD	Digital Voltage Supply, LVCMOS Output POWER
26	VDD	VDD	Digital Voltage Supply, LVCMOS Output POWER
11	VDD	VDD	Digital Voltage Supply, LVCMOS Output POWER
52	VSS	GND	Analog LVDS GROUND
58	VSS	GND	Analog Ground, PLL GROUND
56	VSS	GND	Analog Ground, PLL VCO GROUND
31	VSS	GND	Digital Ground, Logic GROUND
47	VSS	GND	Digital Ground, LOGIC GROUND
39	VSS	GND	Digital Ground, LVCMOS Output GROUND
25	VSS	GND	Digital Ground, LVCMOS Output GROUND
12	VSS	GND	Digital Ground, LVCMOS Output GROUND

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

				MIN	MAX	UNIT
Supply Voltage (V_{DD})				–0.3	4	V
LVCMOS Input Voltage				–0.3	V_{DD} +0.3	V
LVCMOS Output Voltage				–0.3	V_{DD} +0.3	V
LVDS Receiver Input Voltage				–0.3	+3.9	V
LVDS Driver Output Voltage				–0.3	+3.9	V
LVDS Output Short Circuit Duration					10	ms
Junction Temperature					150	°C
Lead Temperature (Soldering, 4 seconds)					260	°C
Maximum Package Power Dissipation Capacity(2)	Package Derating:	DS90UR241 − 48L TQFP	$R_{\theta JA}$		45.8 (4L); 75.4 (2L)	°C/W
			$R_{\theta JC}$		21.0	
		DS90UR124 − 64L TQFP	$R_{\theta JA}$		42.8 (4L); 67.2 (2L)	
			$R_{\theta JC}$		14.6	
Storage temperature, T_{stg}				–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $1/R_{\theta JA}$ °C/W above +25°C

5.2 ESD Ratings

				VALUE	UNIT
DS90UR241-Q1 IN PFB PACKAGE					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	≥±8000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 12, 13, 24, 25, 36, 37, and 48)	±1000	
			Other pins	±1000	
		(ISO10605)(2)	Contact Discharge (20, 19)	±10000	
			Air Discharge (20, 19)	±30000	
DS90UR124-Q1 IN PAG PACKAGE					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	≥±8000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 16, 17, 32, 33, 48, 49, and 64)	±1000	
			Other pins	±1000	
		(ISO10605)(2)	Contact Discharge (R_{IN+}, R_{IN-})	±10000	
			Air Discharge (R_{IN+}, R_{IN-})	±30000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) R_D = 2kΩ, C_S = 330pF

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	–40	25	105	°C
Clock Rate	5		43	MHz
Supply Noise			±100	mV_{P-P}

5.4 Thermal Information

THERMAL METRIC(1)		DS90UR124-Q1 PAG [TQFP] 64 PINS	DS90UR241-Q1 PFB [TQFP] 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.1	64.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.0	14.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	30.4	30.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	
ψ_{JB}	Junction-to-board characterization parameter	30.0	29.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS							
V_{IH}	High-Level Input Voltage		**Tx:** D_{IN}[0:23], TCLK, TPWDNB, DEN, TRFB, RAOFF, VODSEL, RES0. **Rx:** RPWDNB, RRFB, REN, PTOSEL, BISTEN, BISTM, SLEW, RES0.	2		V_{DD}	V
V_{IL}	Low-Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18mA			–0.8	–1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V	**Tx:** D_{IN}[0:23], TCLK, TPWDNB, DEN, TRFB, RAOFF, RES0. **Rx:** RRFB, REN, PTOSEL, BISTEN, BISTM, SLEW, RES0.	–10	±2	10	µA
			Rx: RPWDNB	–20	±5	20	
V_{OH}	High-Level Output Voltage	I_{OH} = −2mA, SLEW = L I_{OH} = −4mA, SLEW = H	**Rx:** R_{OUT}[0:23], RCLK, LOCK, PASS.	2.3	3	V_{DD}	V
V_{OL}	Low-Level Output Voltage	I_{OL} = 2mA, SLEW = L I_{OL} = 4mA, SLEW = H		GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		–40	–70	–110	mA
I_{OZ}	Tri-state Output Current	RPWDNB, REN = 0V, V_{OUT} = 0V or V_{DD}	**Rx:** R_{OUT}[0:23], RCLK, LOCK, PASS.	–30	±0.4	30	µA
LVDS DC SPECIFICATIONS							
V_{TH}	Differential Threshold High Voltage	V_{CM} = 1.8V	**Rx:** R_{IN+}, R_{IN-}			50	mV
V_{TL}	Differential Threshold Low Voltage			–50			mV
I_{IN}	Input Current	V_{IN} = 2.4V, V_{DD} = 3.6V			±100	±250	µA
		V_{IN} = 0V, V_{DD} = 3.6V			±100	±250	

5.5 Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
V_{OD}	Output Differential Voltage (D_{OUT+})–(D_{OUT-})	R_L = 100Ω, without pre-emphasis Figure 5-10	VODSEL = L	**Tx:** D_{OUT+}, D_{OUT-}	380	500	630	mV
			VODSEL = H		500	900	1100	
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω, without pre-emphasis	VODSEL = L			1	50	mV
			VODSEL = H					
V_{OS}	Offset Voltage	R_L = 100Ω, without pre-emphasis	VODSEL = L		1	1.25	1.50	V
			VODSEL = H					
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω, without pre-emphasis	VODSEL = L			3	50	mV
			VODSEL = H					
I_{OS}	Output Short Circuit Current	D_{OUT} = 0V, D_{IN} = H, TPWDNB = 2.4V	VODSEL = L		–2	–5	–8	mA
			VODSEL = H		–4.5	–7.9	–14	
I_{OZ}	Tri-state Output Current	TPWDNB = 0V, D_{OUT} = 0V OR V_{DD}			–15	±1	15	µA
		TPWDNB = 2.4V, DEN = 0V D_{OUT} = 0V OR V_{DD}			–15	±1	15	
		TPWDNB = 2.4V, DEN = 2.4V, D_{OUT} = 0V OR V_{DD} NO LOCK (NO TCLK)			–15	±1	15	
SER/DES SUPPLY CURRENT (DVDD*, PVDD* AND AVDD* PINS) **DIGITAL, PLL, AND ANALOG VDDS*								
I_{DDT}	Serializer Total Supply Current (includes load current)	R_L = 100Ω, PRE = OFF, RAOFF = H, VODSEL = L		f = 43MHz, checkerboard pattern Figure 5-1		60	85	mA
		R_L = 100Ω, PRE = 12kΩ, RAOFF = H, VODSEL = L				65	90	
		R_L = 100Ω, PRE = OFF, RAOFF = H, VODSEL = H		f = 43MHz, random pattern		66	90	
I_{DDTZ}	Serializer Supply Current Power-down	TPWDNB = 0V (All other LVCMOS Inputs = 0V)					45	µA
I_{DDR}	Deserializer Total Supply Current (includes load current)	C_L = 4pF, SLEW = H		f = 43MHz, checkerboard pattern LVCMOS Output Figure 5-2		85	105	mA
		C_L = 4pF, SLEW = H		f = 43MHz, random pattern LVCMOS Output		80	100	
I_{DDRZ}	Deserializer Supply Current Power-down	RPWDNB = 0V (All other LVCMOS Inputs = 0V, R_{IN+}/R_{IN-} = 0V)					50	µA

5.6 Serializer Input Timing Requirements for TCLK

over recommended operating supply and temperature ranges unless otherwise specified

			MIN	NOM	MAX	UNIT
t_{TCP}	Transmit Clock Period	Figure 5-5	23.25	T	200	ns
t_{TCIH}	Transmit Clock High Time		0.3 T	0.5 T	0.7 T	ns
t_{TCIL}	Transmit Clock Low Time		0.3 T	0.5 T	0.7 T	ns
t_{CLKT}	TCLK Input Transition Time	Figure 5-4		2.5		ns
t_{JIT}	TCLK Input Jitter	f = 43MHz			±100	ps
		f = 33MHz			±130	

5.7 Serializer Switching Characteristics

over recommended operating supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LLHT}	LVDS Low-to-High Transition Time	R_L = 100Ω, VODSEL = L, C_L = 10pF to GND, Figure 5-3		245	550	ps
t_{LHLT}	LVDS High-to-Low Transition Time			264	550	ps
t_{DIS}	D_{IN} (0:23) Setup to TCLK	R_L = 100Ω, C_L = 10pF to GND Figure 5-5	4			ns
t_{DIH}	D_{IN} (0:23) Hold from TCLK		4			ns
t_{HZD}	D_{OUT} ± HIGH to Tri-state Delay	R_L = 100Ω, C_L = 10pF to GND Figure 5-6		10	15	ns
t_{LZD}	D_{OUT} ± LOW to Tri-state Delay			10	15	ns
t_{ZHD}	D_{OUT} ± Tri-state to HIGH Delay			75	150	ns
t_{ZLD}	D_{OUT} ± Tri-state to LOW Delay			75	150	ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω			10	ms
t_{SD}	Serializer Delay	R_L = 100Ω, PRE = OFF, RAOFF = L, TRFB = H, Figure 5-8	3.5T+2		3.5T+10	ns
		R_L = 100Ω, PRE = OFF, RAOFF = L, TRFB = L, Figure 5-8	3.5T+2		3.5T+10	
TxOUT_E_O	**TxOUT_E**ye_**O**pening. TxOUT_E_O centered on (tBIT/)2	5MHz–43MHz, R_L = 100Ω, C_L = 10pF to GND, RANDOM pattern Figure 5-9	0.76	0.84		UI

5.8 Deserializer Switching Characteristics

over recommended operating supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{RCP}	**R**eceiver out **C**lock **P**eriod	t_{RCP} = t_{TCP}, PTOSEL = H	RCLK Figure 5-15	23.25	T	200	ns
t_{RDC}	**R**CLK **D**uty **C**ycle	PTOSEL = H, SLEW = L		45%	50%	55%	
t_{CLH}	LV**C**MOS **L**ow-to-**H**igh Transition Time	C_L = 4pF (lumped load), SLEW = H	R_{OUT} [0:23], RCLK, LOCK		1.5	2.5	ns
t_{CHL}	LV**C**MOS **H**igh-to-**L**ow Transition Time				1.5	2.5	ns
t_{CLH}	LV**C**MOS **L**ow-to-**H**igh Transition Time	C_L = 4pF (lumped load), SLEW = L	R_{OUT} [0:23], RCLK, LOCK		2.0	3.5	ns
t_{CHL}	LV**C**MOS **H**igh-to-**L**ow Transition Time				2.0	3.5	ns

5.8 Deserializer Switching Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{ROS}	**R** $_{OUT}$ (0:7) **S**etup Data to RCLK (Group 1)	PTOSEL = L, SLEW = H, Figure 5-16	R_{OUT}[0:7]	(0.35)× t_{RCP}	(0.5×t_{RCP})– 3 UI		ns
t_{ROH}	**R** $_{OUT}$ (0:7) **H**old Data to RCLK (Group 1)			(0.35)× t_{RCP}	(0.5×t_{RCP})– 3 UI		ns
t_{ROS}	**R** $_{OUT}$ (8:15) **S**etup Data to RCLK (Group 2)	PTOSEL = L, SLEW = H, Figure 5-16	R_{OUT} [8:15], LOCK	(0.35)× t_{RCP}	(0.5×t_{RCP})– 3 UI		ns
t_{ROH}	**R** $_{OUT}$ (8:15) **H**old Data to RCLK (Group 2)			(0.35)× t_{RCP}	(0.5×t_{RCP})– 3 UI		ns
t_{ROS}	**R** $_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)		R_{OUT} [16:23]	(0.35)× t_{RCP}	(0.5×t_{RCP})– 3 UI		ns
t_{ROH}	**R** $_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)			(0.35)× t_{RCP}	(0.5×t_{RCP})– 3 UI		ns
t_{ROS}	**R** $_{OUT}$ (0:7) **S**etup Data to RCLK (Group 1)	PTOSEL = H, SLEW = H, Figure 5-15	R_{OUT}[0:7]	(0.35)× t_{RCP}	(0.5×t_{RCP})– 2 UI		ns
t_{ROH}	**R** $_{OUT}$ (0:7) **H**old Data to RCLK (Group 1)			(0.35)× t_{RCP}	(0.5×t_{RCP}) +2 UI		ns
t_{ROS}	**R** $_{OUT}$ (8:15) **S**etup Data to RCLK (Group 2)		R_{OUT} [8:15], LOCK	(0.35)× t_{RCP}	(0.5×t_{RCP}) −1 UI		ns
t_{ROH}	**R** $_{OUT}$ (8:15) **H**old Data to RCLK (Group 2)			(0.35)× t_{RCP}	(0.5×t_{RCP}) +1 UI		ns
t_{ROS}	**R** $_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)		R_{OUT} [16:23]	(0.35)× t_{RCP}	(0.5×t_{RCP}) +1 UI		ns
t_{ROH}	**R** $_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)			(0.35)× t_{RCP}	(0.5×t_{RCP})– 1 UI		ns
t_{HZR}	**H**IGH to Tri-state Delay	PTOSEL = H, Figure 5-14	R_{OUT} [0:23], RCLK, LOCK		3	10	ns
t_{LZR}	**L**OW to Tri-state Delay				3	10	ns
t_{ZHR}	Tri-state to **H**IGH Delay				3	10	ns
t_{ZLR}	Tri-state to **L**OW Delay				3	10	ns
t_{DD}	**D**eserializer **D**elay	PTOSEL = H, Figure 5-12	RCLK		[5+(5/56)]T+ 3.7	[5+(5/56)]T +8	ns
t_{DSR}	Deserializer PLL Lock Time from Powerdown	See Figure 5-14	5MHz			128k*T	ms
			43MHz			128k*T	
RxIN_TOL-L	**R**eceiver **IN**put **TOL**erance **L**eft	See Figure 5-17	5MHz–43MHz			0.25	UI
RxIN_TOL-R	**R**eceiver **IN**put **TOL**erance **R**ight	See Figure 5-17	5MHz–43MHz			0.25	UI

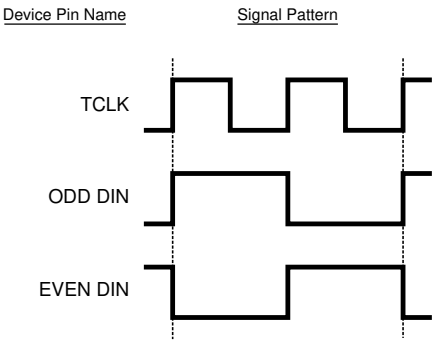


Figure 5-1. Serializer Input Checkerboard Pattern

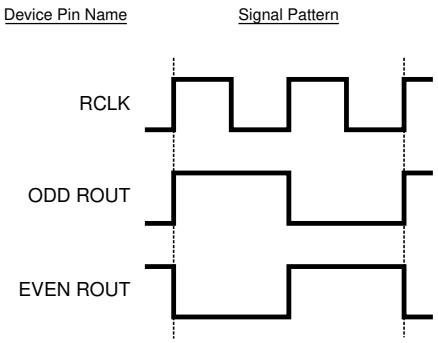


Figure 5-2. Deserializer Output Checkerboard Pattern

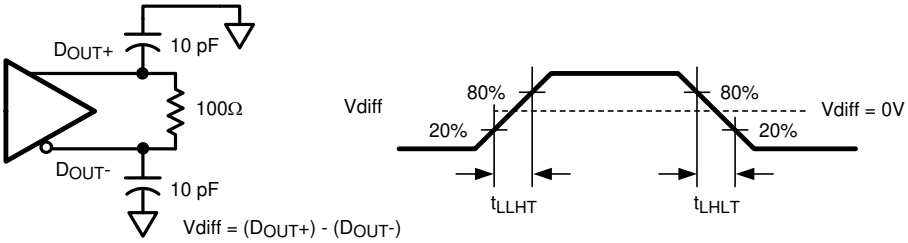


Figure 5-3. Serializer LVDS Output Load and Transition Times

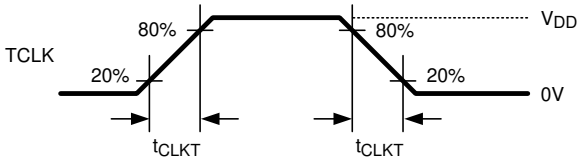


Figure 5-4. Serializer Input Clock Transition Times

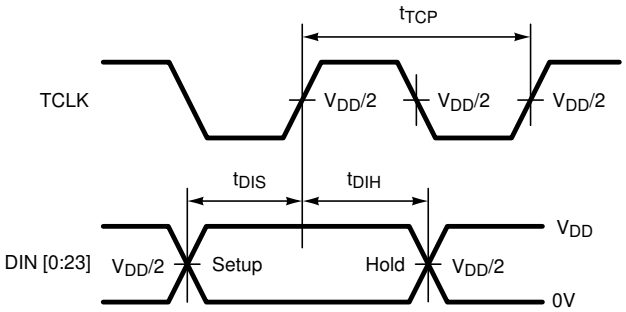


Figure 5-5. Serializer Setup and Hold Times

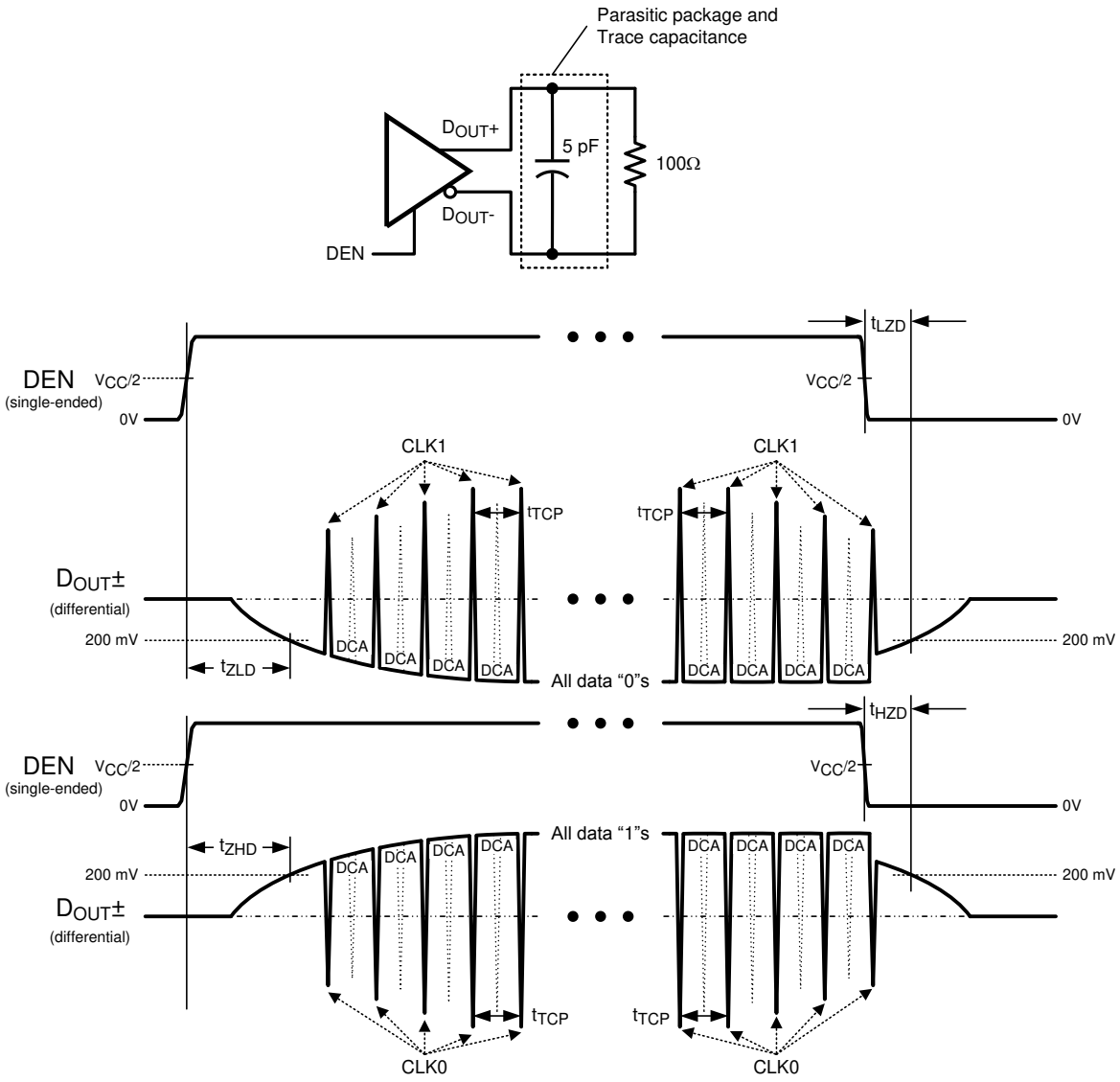


Figure 5-6. Serializer Tri-State Test Circuit and Delay

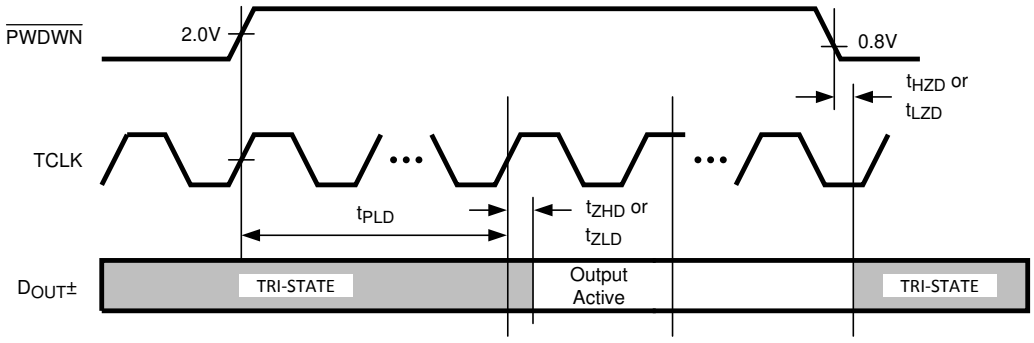


Figure 5-7. Serializer PLL Lock Time, and TPWDNB Tri-State Delays

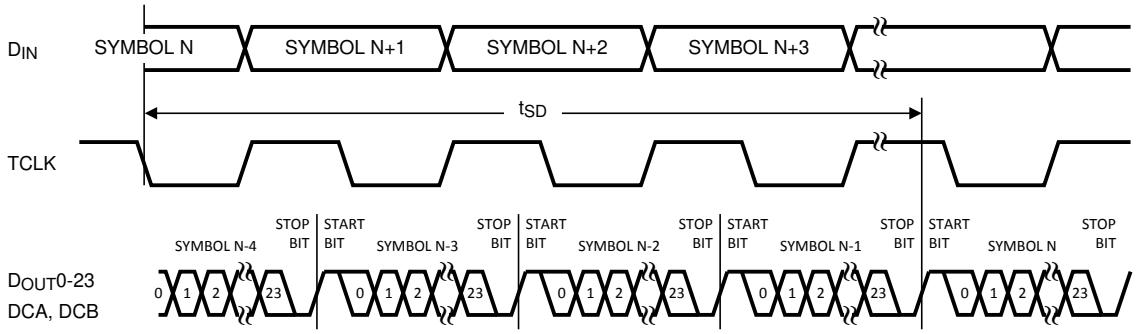


Figure 5-8. Serializer Delay

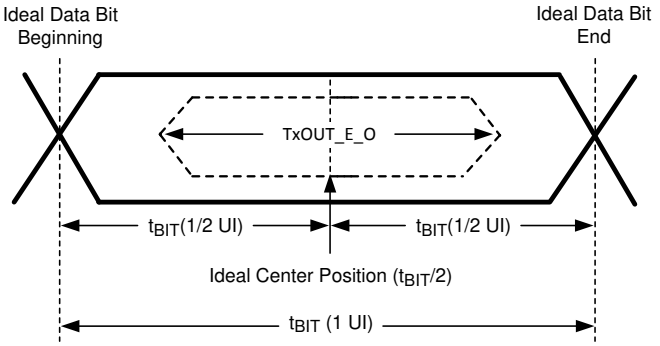
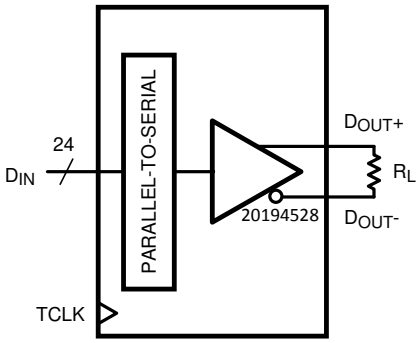


Figure 5-9. Transmitter Output Eye Opening (TxOUT_E_O)



VOD = (D_{OUT+}) – (D_{OUT-})
Differential output signal is shown as (D_{OUT+}) – (D_{OUT-}), device in Data Transfer mode.

Figure 5-10. Serializer V_{OD} Diagram

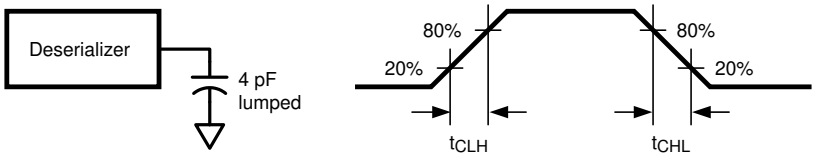


Figure 5-11. Deserializer LVCMOS Output Load and Transition Times

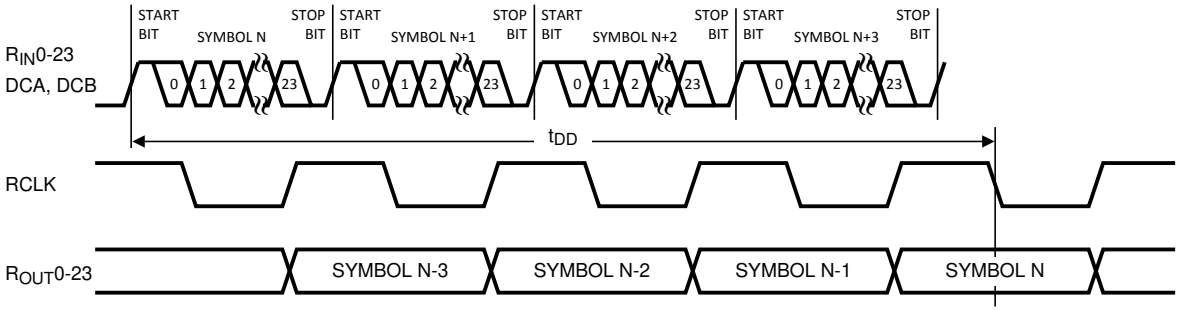
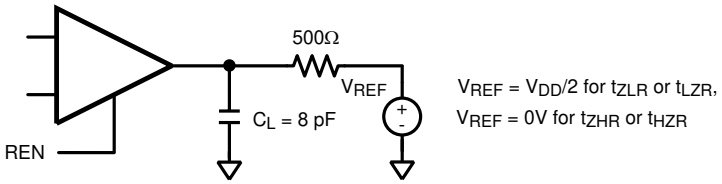


Figure 5-12. Deserializer Delay



NOTE:
C_L includes instrumentation and fixture capacitance within 6 cm of R_{OUT} [23:0].

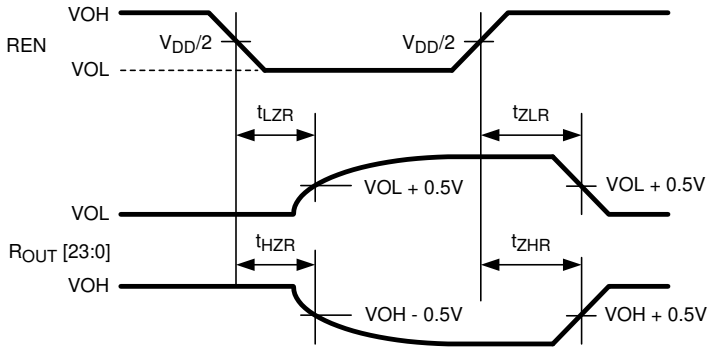


Figure 5-13. Deserializer Tri-State Test Circuit and Timing

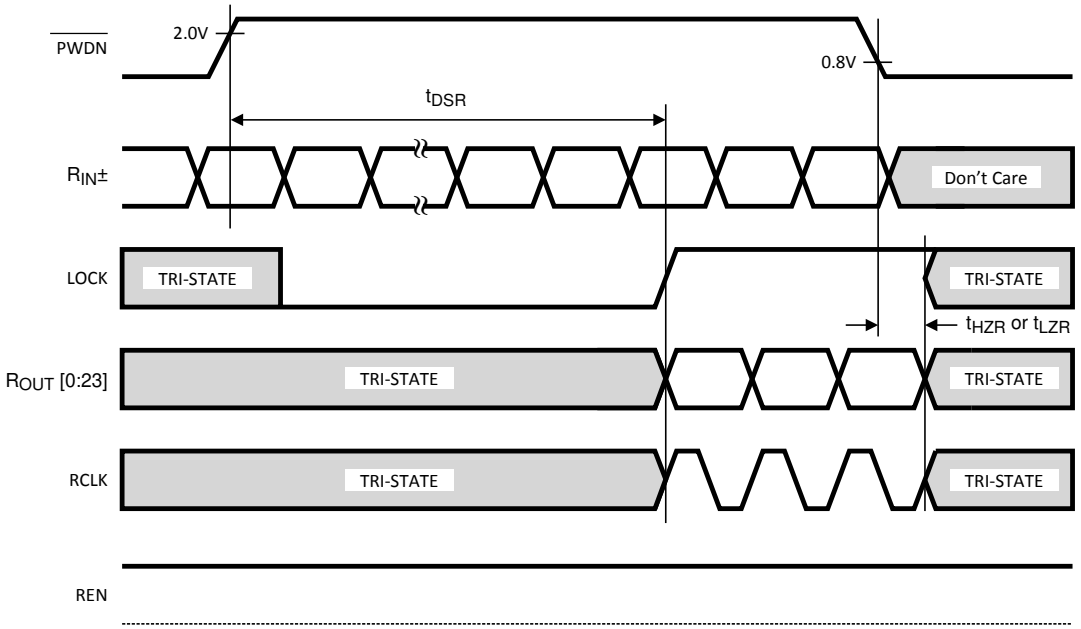


Figure 5-14. Deserializer PLL Lock Times and RPWDNB Tri-State Delay

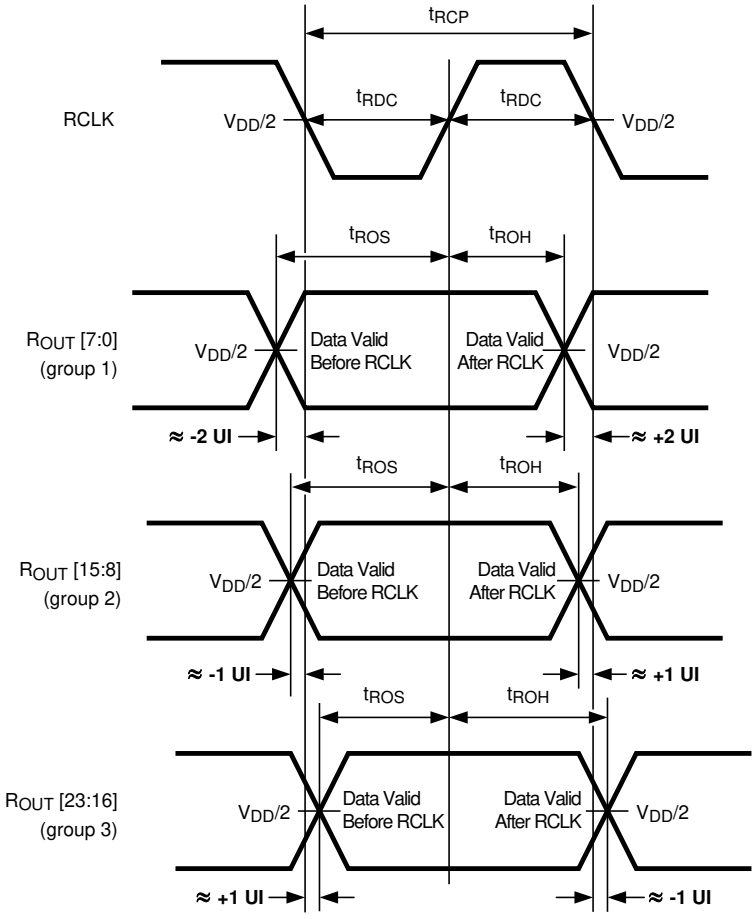
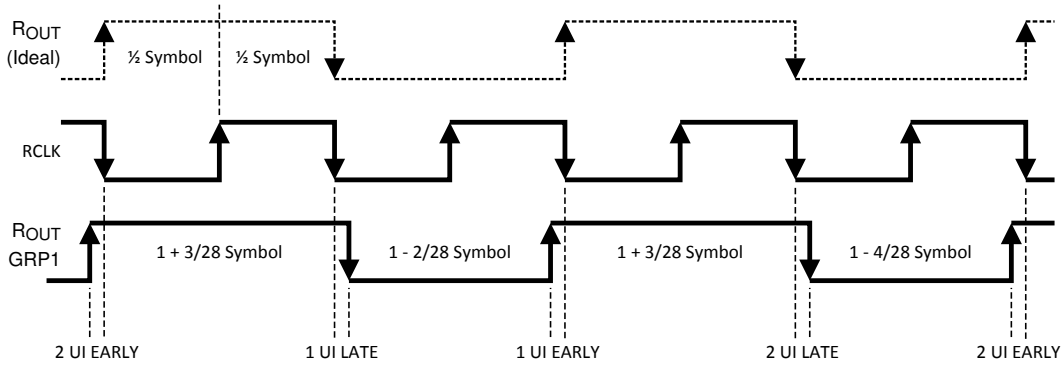
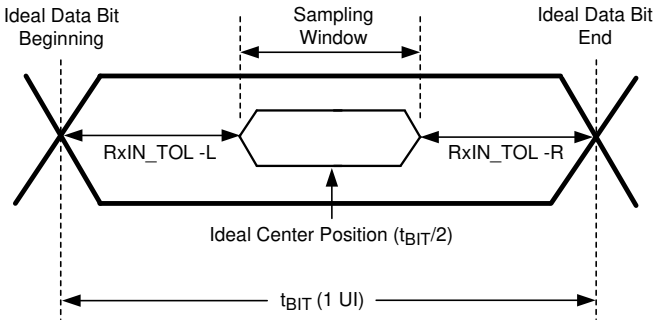


Figure 5-15. Deserializer Setup and Hold Times and PTO, PTOSEL = H



Group 1 will be latched internally by sequence of (early 2UI, late 1UI, early 1UI, late 2UI).
Group 2 will be latched internally by sequence of (late 1UI, early 1UI, late 2UI, early 2UI).
Group 3 will be latched internally by sequence of (early 1UI, late 2UI, early 2UI, late 1UI).

Figure 5-16. Deserializer Setup and Hold Times and PTO Spread, PTOSEL = L



RxIN_TOL_L is the ideal noise margin on the left of the figure, with respect to ideal.
RxIN_TOL_R is the ideal noise margin on the right of the figure, with respect to ideal.

Figure 5-17. Receiver Input Tolerance (RxIN_TOL) and Sampling Window

5.9 Typical Characteristics

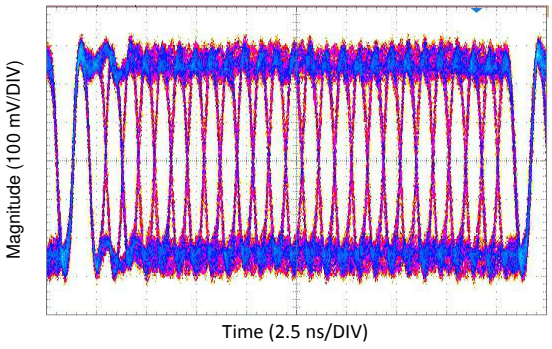


Figure 5-18. DS90UR241 DOUT± With PCLK at 43MHz Measured at RIN± Termination

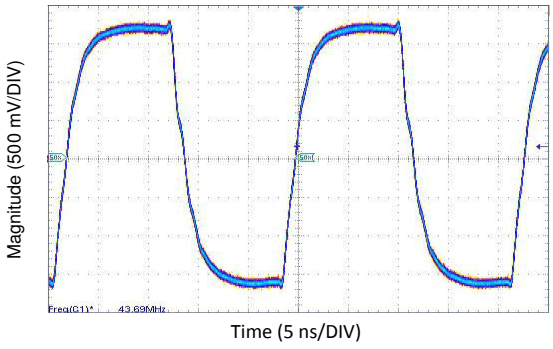


Figure 5-19. DS90UR124 PCLK Output at 43MHz

6 Detailed Description

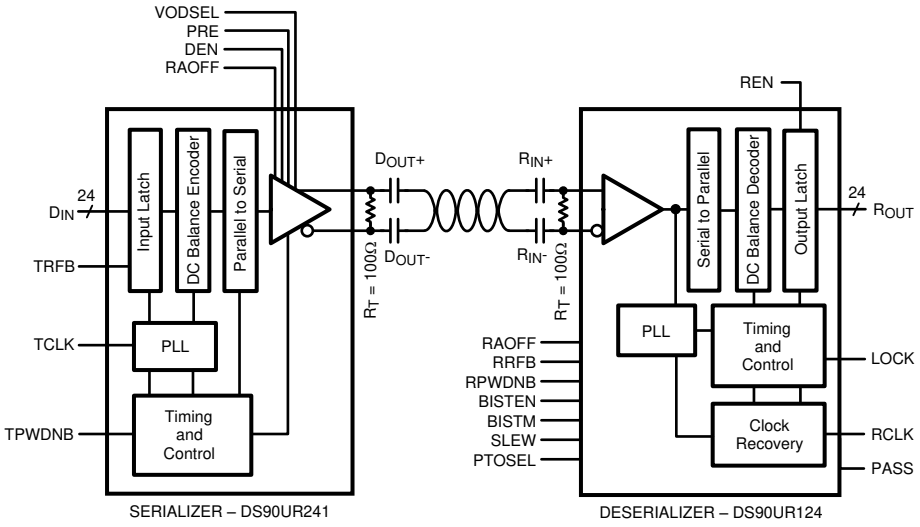
6.1 Overview

The DS90UR241 Serializer and DS90UR124 Deserializer chipset is an easy-to-use transmitter and receiver pair that sends 24-bits of parallel LVCMOS data over a single serial LVDS link from 120 Mbps to 1.03 Gbps throughput. The DS90UR241 transforms a 24-bit wide parallel LVCMOS data into a single high speed LVDS serial data stream with embedded clock and scrambles / DC Balances the data to enhance signal quality to support AC coupling. The DS90UR124 receives the LVDS serial data stream and converts it back into a 24-bit wide parallel data and recovered clock. The 24-bit Serializer/Deserializer chipset is designed to transmit data up to 10 meters over shielded twisted pair (STP) at clock speeds from 5MHz to 43MHz.

The Deserializer can attain lock to a data stream without the use of a separate reference clock source, greatly simplifying system complexity and overall cost. The Deserializer synchronizes to the Serializer regardless of data pattern, delivering true automatic “plug and lock” performance. It will lock to the incoming serial stream without the need of special training patterns or sync characters. The Deserializer recovers the clock and data by extracting the embedded clock information and validating data integrity from the incoming data stream and then deserializes the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the LOCK output high when lock occurs.

In addition, the Deserializer also supports an optional @SPEED BIST (Built In Self Test) mode, BIST error flag, and LOCK status reporting pin. Signal quality on the wide parallel output is controlled by the SLEW control and bank slew (PTOSEL) inputs to help reduce noise and system EMI. Each device has a power down control to enable efficient operation in various applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Initialization and Locking Mechanism

Initialization of the DS90UR241 and DS90UR124 must be established before each device sends or receives data. Initialization refers to synchronizing the Serializer’s and Deserializer’s PLL’s together. After the Serializers locks to the input clock source, the Deserializer synchronizes to the Serializers as the second and final initialization step.

Step 1: When V_{DD} is applied to both Serializer and/or Deserializer, the respective outputs are held in Tri-state and internal circuitry is disabled by on-chip power-on circuitry. When V_{DD} reaches V_{DD} OK (approximately 2.2V) the PLL in Serializer begins locking to a clock input. For the Serializer, the local clock is the transmit clock, TCLK. The Serializer outputs are held in Tri-state while the PLL locks to the TCLK. After locking to TCLK, the Serializer block is now ready to send data patterns. The Deserializer output remains in Tri-state while the PLL

locks to the embedded clock information in serial data stream. Also, the Deserializer LOCK output remains low until the PLL locks to incoming data and sync-pattern on the RIN± pins.

Step 2: The Deserializer PLL acquires lock to a data stream without requiring the Serializer to send special patterns. The Serializer that is generating the stream to the Deserializer automatically sends random (non-repetitive) data patterns during this step of the Initialization State. The Deserializer locks onto embedded clock within the specified amount of time. An embedded clock and data recovery (CDR) circuit locks to the incoming bit stream to recover the high-speed receive bit clock and re-time incoming data. The CDR circuit expects a coded input bit stream. For the Deserializer to lock to a random data stream from the Serializer, it performs a series of operations to identify the rising clock edge and validates data integrity, then locks to it. Because this locking procedure is independent on the data pattern, total random locking duration can vary. At the point when the Deserializer's CDR locks to the embedded clock, the LOCK pin goes high and valid RCLK/data appears on the outputs. Note that the LOCK signal is synchronous to valid data appearing on the outputs. The Deserializer's LOCK pin is a convenient way to ensure data integrity is achieved on receiver side.

6.3.2 Data Transfer

After Serializer lock is established, the inputs DIN0–DIN23 are used to input data to the Serializer. Data is clocked into the Serializer by the TCLK input. The edge of TCLK used to strobe the data is selectable via the TRFB pin. TRFB high selects the rising edge for clocking data and low selects the falling edge. The Serializer outputs (DOUT±) are intended to drive point-to-point connections.

CLK1, CLK0, DCA, DCB are four overhead bits transmitted along the single LVDS serial data stream (Figure 7-9). The CLK1 bit is always high and the CLK0 bit is always low. The CLK1 and CLK0 bits function as the embedded clock bits in the serial stream. DCB functions as the DC Balance control bit and does not require any pre-coding of data on transmit side. The DC Balance bit is used to minimize the short and long-term DC bias on the signal lines. This bit operates by selectively sending the data either unmodified or inverted. The DCA bit is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are integrated and automatically performed within Serializer and Deserializer.

The chipset supports clock frequency ranges of 5MHz to 43MHz. Every clock cycle, 24 databits are sent along with 4 additional overhead control bits. Thus the line rate is 1.20Gbps maximum (140Mbps minimum). The link is extremely efficient at 86% (24/28). Twenty five (24 data + 1 clock) plus associated ground signals are reduced to only 1 single LVDS pair providing a compression ratio of better then 25 to 1.

In the serialized data stream, data/embedded clock & control bits (24+4 bits) are transmitted from the Serializer data output (DOUT±) at 28 times the TCLK frequency. For example, if TCLK is 43MHz, the serial rate is 43 × 28 = 1.20 Giga bits per second. Since only 24 bits are from input data, the serial "payload" rate is 24 times the TCLK frequency. For instance, if TCLK = 43MHz, the payload data rate is 43 x 24 = 1.03Gbps. TCLK is provided by the data source and must be in the range of 5MHz to 43MHz nominal. The Serializer outputs (DOUT±) can drive a point-to-point connection as shown in Figure 7-8. The outputs transmit data when the enable pin (DEN) is high and TPWDNB is high. The DEN pin can be used to Tri-state the outputs when driven low.

When the Deserializer channel attains lock to the input from a Serializer, it drives its LOCK pin high and synchronously delivers valid data and recovered clock on the output. The Deserializer locks onto the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock to the RCLK pin. The recovered clock (RCLK output pin) is synchronous to the data on the ROUT[23:0] pins. While LOCK is high, data on ROUT[23:0] is valid. Otherwise, ROUT[23:0] is invalid. The polarity of the RCLK edge is controlled by the RRFB input. ROUT[23:0], LOCK and RCLK outputs will each drive a maximum of 4pF load with a 43MHz clock. REN controls Tri-state for ROUTn and the RCLK pin on the Deserializer.

6.3.3 Resynchronization

If the Deserializer loses lock, it will automatically try to re-establish lock. For example, if the embedded clock edge is not detected one time in succession, the PLL loses lock and the LOCK pin is driven low. The Deserializer then enters the operating mode where it tries to lock to a random data stream. It looks for the embedded clock edge, identifies it, and then proceeds through the locking process.

The logic state of the LOCK signal indicates whether the data on ROUT is valid; when it is high, the data is valid. The system may monitor the LOCK pin to determine whether data on the ROUT is valid.

6.3.4 Powerdown

The Powerdown state is a low power sleep mode that the Serializer and Deserializer may use to reduce power when no data is being transferred. The TPWDNB and RPWDNB are used to set each device into powerdown mode, which reduces supply current to the µA range. The Serializer enters powerdown when the TPWDNB pin is driven low. In powerdown, the PLL stops and the outputs go into Tri-state, disabling load current and reducing current supply. To exit Powerdown, TPWDNB must be driven high. When the Serializer exits Powerdown, its PLL must lock to TCLK before it is ready for the Initialization state. The system must then allow time for Initialization before data transfer can begin. The Deserializer enters powerdown mode when RPWDNB is driven low. In powerdown mode, the PLL stops and the outputs enter Tri-state. To bring the Deserializer block out of the powerdown state, the system drives RPWDNB high.

Both the Serializer and Deserializer must reinitialize and relock before data can be transferred. The Deserializer will initialize and assert LOCK high when it is locked to the embedded clock.

6.3.5 Tri-State

For the Serializer, Tri-state is entered when the DEN or TPWDNB pin is driven low. This will Tri-state both driver output pins (DOUT+ and DOUT−). When DEN is driven high, the serializer will return to the previous state as long as all other control pins remain static (TPWDNB, TRFB).

When you drive the REN or RPWDNB pin low, the Deserializer enters Tri-state. Consequently, the receiver output pins (ROUT0–ROUT23) and RCLK will enter Tri-state. The LOCK output remains active, reflecting the state of the PLL. The Deserializer input pins are high impedance during receiver powerdown (RPWDNB low) and power-off (V_{DD} = 0V).

6.3.6 Pre-Emphasis

The DS90UR241 features a Pre-Emphasis function used to compensate for long or lossy transmission media. Cable drive is enhanced with a user selectable Pre-Emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance is limited by the loss characteristics and quality of the media. Pre-Emphasis adds extra current during LVDS logic transition to reduce the cable loading effects and increase driving distance. In addition, Pre-Emphasis helps provide faster transitions, increased eye openings, and improved signal integrity. The ability of the DS90UR241 to use the Pre-Emphasis feature extends the transmission distance up to 10 meters in most cases.

To enable the Pre-Emphasis function, the “PRE” pin requires one external resistor (Rpre) to Vss to set the additional current level. Values of Rpre must be between 6kΩ and 100MΩ. Values less than 6kΩ must not be used. A lower input resistor value on the ”PRE” pin increases the magnitude of dynamic current during data transition. The additional source current is based on the following formula: PRE = (R_{PRE} ≥ 6kΩ); I_{MAX} = [48 / R_{PRE}]. For example if Rpre = 15kΩ , then the Pre-Emphasis current is increase by an additional 3.2mA.

The amount of Pre-Emphasis for a given media depends on the transmission distance of the application. In general, too much Pre-Emphasis can cause over or undershoot at the receiver input pins. This can result in excessive noise, crosstalk and increased power dissipation. For short cables or distances, Pre-Emphasis may not be required. Signal quality measurements are recommended to determine the proper amount of Pre-Emphasis for each application.

6.3.7 AC-Coupling and Termination

The DS90UR241 and DS90UR124 supports AC-coupled interconnects through integrated DC balanced encoding/decoding scheme. To use the Serializer and Deserializer in an AC-coupled application, insert external AC-coupling capacitors in series in the LVDS signal path as illustrated in Figure 7-8. The Deserializer input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal V_{CM} to +1.8V. With AC signal coupling, capacitors provide the AC-coupling path to the signal input.

For the high-speed LVDS transmissions, the smallest available package must be used for the AC-coupling capacitor. This helps minimize degradation of signal quality due to package parasitics. The most common used capacitor value for the interface is a 100nF (0.1uF). NPO class 1 or X7R class 2 type capacitors are recommended. 50 WVDC must be the minimum used for the best system-level ESD performance.

A termination resistor across DOUT± and RIN± is also required for proper operation to be obtained. The termination resistor must be equal to the differential impedance of the media being driven and in the range of 90 to 132Ω. 100Ω is a typical value common used with standard 100Ω transmission media. This resistor is required for control of reflections and also completes the current loop. Place the resistor as close to the Serializer DOUT± outputs and Deserializer RIN± inputs to minimize the stub length from the pins. To match with the deferential impedance on the transmission line, the LVDS I/O are terminated with 100Ω resistors on Serializer DOUT± outputs pins and Deserializer RIN± input pins.

6.3.7.1 Receiver Termination Option 1

A single 100Ω termination resistor is placed across the RIN± pins (see Figure 7-8). This provides the signal termination at the Receiver inputs. Other options may be used to increase noise tolerance.

6.3.7.2 Receiver Termination Option 2

For additional EMI tolerance, two 50Ω resistors can be used in place of the single 100Ω resistor. A small capacitor is tied from the center point of the 50Ω resistors to ground (see Figure 7-10). This provides a high-frequency low impedance path for noise suppression. Value is not critical, 4.7nF can be used with general applications.

6.3.7.3 Receiver Termination Option 3

For high noise environments, an additional voltage divider network may be connected to the center point. This has the advantage of a providing a DC low-impedance path for noise suppression. Use resistor values in the range of 100Ω-2KΩ for the pullup and pulldown. Ratio the resistor values to bias the center point at 1.8V. For example (see Figure 7-11): V_{DD}=3.3 V, Rpullup=1 KΩ, Rpulldown=1.2 KΩ; or Rpullup=100Ω, Rpulldown=120Ω (strongest). The smaller values will consume more bias current, but will provide enhanced noise suppression.

6.3.8 Signal Quality Enhancers

The DS90UR124 Deserializer supports two signal quality enhancers. The SLEW pin is used to increase the drive strength of the LVCMOS outputs when driving heavy loads. SLEW allows output drive strength for high or low current drive. Default setting is LOW for low drive at 2mA and HIGH for high drive at 4mA.

There are two types of Progressive Turnon modes (Fixed and PTO Frequency Spread) to help reduce EMI: simultaneous switching noise and system ground bounce. The PTOSEL pin introduces bank skew in the data/clock outputs to limit the number of outputs switching simultaneously. For Fixed-PTO mode, the Deserializer ROUT[23:0] outputs are grouped into three groups of eight, with each group switching about 2 or 1 UI apart in phase from RCLK for Group 1 and Groups 2, 3, respectively (see Figure 5-15). In the PTO Frequency Spread mode, ROUT[23:0] are also grouped into three groups of eight, with each group is separated out of phase with the adjacent groups (see Figure 5-16) per every 4 cycles. Note that in the PTO Frequency Spread operating mode RCLK is also spreading and separated by 1 UI.

6.3.9 @SPEED-BIST Test Feature

To assist vendors with test verification, the DS90UR241 and DS90UR124 is equipped with built-in self-test (BIST) capability to support both system manufacturing and field diagnostics. BIST mode is intended to check the entire high-speed serial link at full link-speed, without the use of specialized and expensive test equipment. This feature provides a simple method for a system host to perform diagnostic testing of both Serializer and Deserializer. The BIST function is easily configured through the 2 control pins on the DS90UR124. When the BIST mode is activated, the Serializer has the ability to transfer an internally generated PRBS data pattern. This pattern traverses across interconnecting links to the Deserializer. The DS90UR124 includes an on-chip PRBS pattern verification circuit that checks the data pattern for bit errors and reports any errors on the data output pins on the Deserializer.

The @SPEED-BIST feature uses 2 signal pins (BISTEN and BISTM) on the DS90UR124 Deserializer. The BISTEN and BISTM pins together determine the functions of the BIST mode. The BISTEN signal (HIGH) activates the test feature on the Deserializer. After the BIST mode is enabled, all the data input channels DIN[23:0] on the DS90UR241 Serializer must be set logic LOW or floating in order for Deserializer to start accepting data. An input clock signal (TCLK) for the Serializer must also be applied during the entire BIST operation. The BISTM pin selects error reporting status mode of the BIST function. When BIST is configured in the error status mode (BISTM = LOW), each of the ROUT[23:0] outputs correspond to bit errors on a cycle-by-cycle basis. The result of bit mismatches are indicated on the respective parallel inputs on the ROUT[23:0] data output pins. In the BIST error-count accumulator mode (BISTM = HIGH), an 8-bit counter on ROUT[7:0] is used to represent the number of errors detected (0 to 255 max). The successful completion of the BIST test is reported on the PASS pin on the Deserializer. The Deserializer's PLL must first be locked to make sure the PASS status is valid. The PASS status pin stay LOW and then transition to HIGH once a BER of $1x10^{-9}$ is achieved across the transmission link.

6.3.10 Backward-Compatible Mode With DS90C241 and DS90C124

The RAOFF pin allows a backward-compatible mode with DS90C241 and DS90C124 devices. To interface with either DS90C241 Serializer or DS90C124 Deserializer, the RAOFF pin on DS90UR241 or DS90UR124 must be tied HIGH to disable the additional LSFR coding. For normal operation directly with DS90UR241 to DS90UR124, RAOFF pins are set LOW. See Table 6-1 and Table 6-2 for more details.

6.4 Device Functional Modes

Table 6-1. DS90UR241 Serializer Truth Table

TPWDNB (Pin 9)	DEN (Pin 18)	RAOFF (Pin 12)	Tx PLL Status (Internal)	LVDS Outputs (Pins 19 and 20)
L	X	X	X	Hi-Z
H	L	X	X	Hi-Z
H	H	X	Not Locked	Hi-Z
H	H	L	Locked	Serialized Data with Embedded Clock (DS90**UR**124 compatible)
H	H	H	Locked	Serialized Data with Embedded Clock (DS90**C**124 compatible)

Table 6-2. DS90UR124 Deserializer Truth Table

RPWDNB (Pin 48)	REN (Pin 60)	RAOFF (Pin 63)	Rx PLL Status (Internal)	ROUTn and RCLK (See Pin Diagram)	LOCK (Pin 23)
L	X	X	X	Hi Z	Hi Z
H	L	X	X	Hi Z	L = PLL Unocked; H = PLL Locked
H	H	X	Not Locked	Hi Z	L
H	H	L	Locked	Data and RCLK Active (DS90**UR**241 compatible)	H
H	H	H	Locked	Data and RCLK Active (DS90**C**241 compatible)	H

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

1.1 Using the DS90UR241 and DS90UR124

The DS90UR241/DS90UR124 Serializer/Deserializer (SERDES) pair sends 24 bits of parallel LVCMOS data over a serial LVDS link up to 1.03 Gbps. Serialization of the input data is accomplished using an onboard PLL at the Serializer which embeds clock with the data. The Deserializer extracts the clock/control information from the incoming data stream and deserializes the data. The Deserializer monitors the incoming clock information to determine lock status and will indicate lock by asserting the LOCK output high.

1.2 Display Application

The DS90URxxx-Q1 chipset is intended for interface between a host (graphics processor) and a Display and supports an 18-bit color depth (RGB666) and up to 1280 × 480 display formats. In a RGB666 configuration 18 color bits (R[5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and 3 control bits (VS, HS and DE) along with 3 spare bits are supported across the serial link with PCLK rates from 5 to 43MHz.

1.3 Typical Application Connection

Figure 7-1 shows a typical application of the DS90UR241 Serializer (SER). The LVDS outputs use a 100Ω termination and 100nF coupling capacitors to the line. Bypass capacitors are placed near the power supply pins. At a minimum, three 0.1uF capacitors must be used for local bypassing. A system GPO (General Purpose Output) controls the TPWDNB pin. In this application the TRFB pin is tied High to latch data on the rising edge of the TCLK. The DEN signal is not used and is tied High also. The application is to the companion Deserializer (DS90UR124) so the RAOFF pin is tied low to scramble the data and improve link signal quality. In this application the link is typical, therefore the VODSEL pin is tied Low for the standard LVDS swing. The pre-emphasis input uses a resistor to ground to set the amount of pre-emphasis desired by the application.

Figure 7-5 shows a typical application of the DS90UR124 Deserializer (DES). The LVDS inputs use a 100Ω termination and 100nF coupling capacitors to the line. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1uF capacitors must be used for local bypassing. A system GPO (general-purpose output) controls the RPWDNB pin. In this application the RRFB pin is tied High to strobe the data on the rising edge of the RCLK. The REN signal is not used and is tied High also. The application is to the companion Serializer (DS90UR241) so the RAOFF pin is tied low to descramble the data. Output (LVCMOS) signal quality is set by the SLEW pin, and the PTOSEL pin can be used to reduce simultaneous output switching by introducing a small amount of delay between output banks.

2 Typical Applications

2.1 DS90UR241-Q1 Typical Application Connection

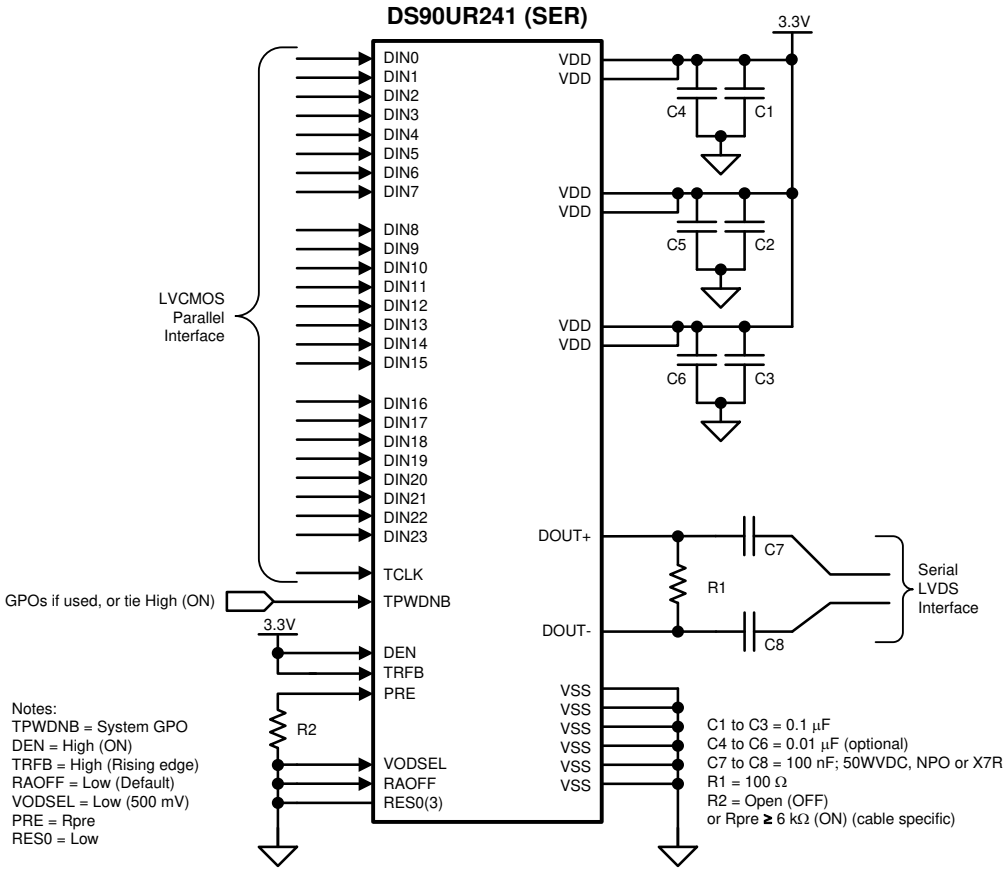


Figure 7-1. DS90UR241 Connection Diagram

2.1.1 Design Requirements

Table 7-1. DS90UR241 Design Parameter

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3V
AC Coupling Capacitor for DOUT±	100nF
DOUT± External Termination	100Ω
PCLK Frequency	33MHz

2.1.2 Detailed Design Procedure

Figure 7-1 shows a typical application of the DS90UR241 serializer for an 33MHz 18-bit Color Display Application. The DOUT± outputs must have a series external 0.1uF AC-coupling capacitor and 100Ω parallel termination on the high-speed serial lines. The serializer does not have an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, three 0.1uF capacitors must be used for local device bypassing. Additional capacitors may be needed as the number and values of the capacitors depends on meeting the power noise specification of the part. Ferrite beads may be needed on the VDDs for effective noise suppression. The interface to the graphics source is with 3.3V LVCMOS levels. An RC delay is placed on the PDB signal to delay the enabling of the device until power is stable.

2.1.2.1 Power Considerations

An all LVCMOS design of the Serializer and Deserializer makes them inherently low-power devices. Additionally, the constant current source nature of the LVDS outputs minimizes the slope of the speed vs. I_{DD} curve of LVCMOS designs.

2.1.2.2 Noise Margin

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably recover data. Various environmental and systematic factors include:

- Serializer: V_{DD} noise, TCLK jitter (noise bandwidth and out-of-band noise)
- Media: ISI, V_{CM} noise
- Deserializer: V_{DD} noise

For a graphical representation of noise margin, see Figure 5-17.

2.1.2.3 Transmission Media

The Serializer and Deserializer are to be used in point-to-point configuration, through a PCB trace, or through twisted pair cable. In a point-to-point configuration, the transmission media needs be terminated at both ends of the transmitter and receiver pair. Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. In most applications that involve cables, the transmission distance is determined on data rates involved, acceptable bit error rate and transmission medium.

The resulting signal quality at the receiving end of the transmission media can be assessed by monitoring the differential eye opening of the serial data stream. The Receiver Input Tolerance and Differential Threshold Voltage specifications define the acceptable data eye opening. A differential probe must be used to measure across the termination resistor at the DS90UR124 inputs. Figure 7-2 illustrates the eye opening and relationship to the Receiver Input Tolerance and Differential Threshold Voltage specifications.

2.1.2.4

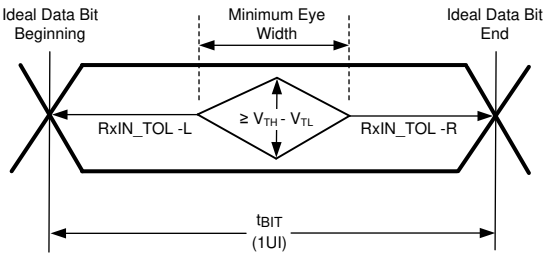


Figure 7-2. Receiver Input Eye Opening

2.1.2.5 Live Link Insertion

The Serializer and Deserializer devices support live pluggable applications. The automatic receiver lock to random data “plug and go” hot insertion capability allows the DS90UR124 to attain lock to the active data stream during a live insertion event.

2.1.3 Application Curves

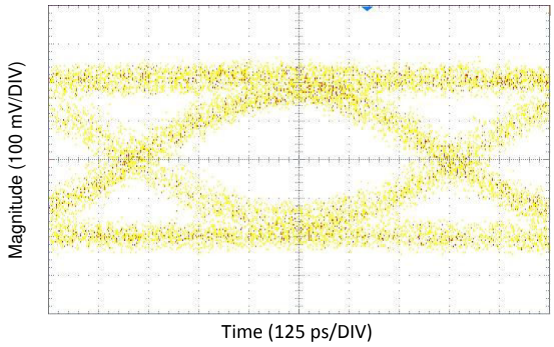


Figure 7-3. DS90UR241 DOUT± at 1.2 Gbps Measured at RIN± Termination; VODSEL=LOW

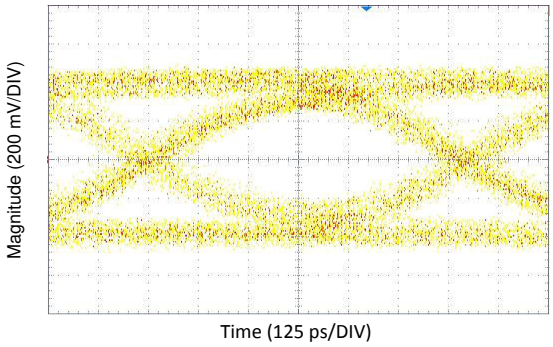


Figure 7-4. DS90UR241 DOUT± at 1.2 Gbps Measured at RIN± Termination; VODSEL=HIGH

2.2 DS90UR124 Typical Application Connection

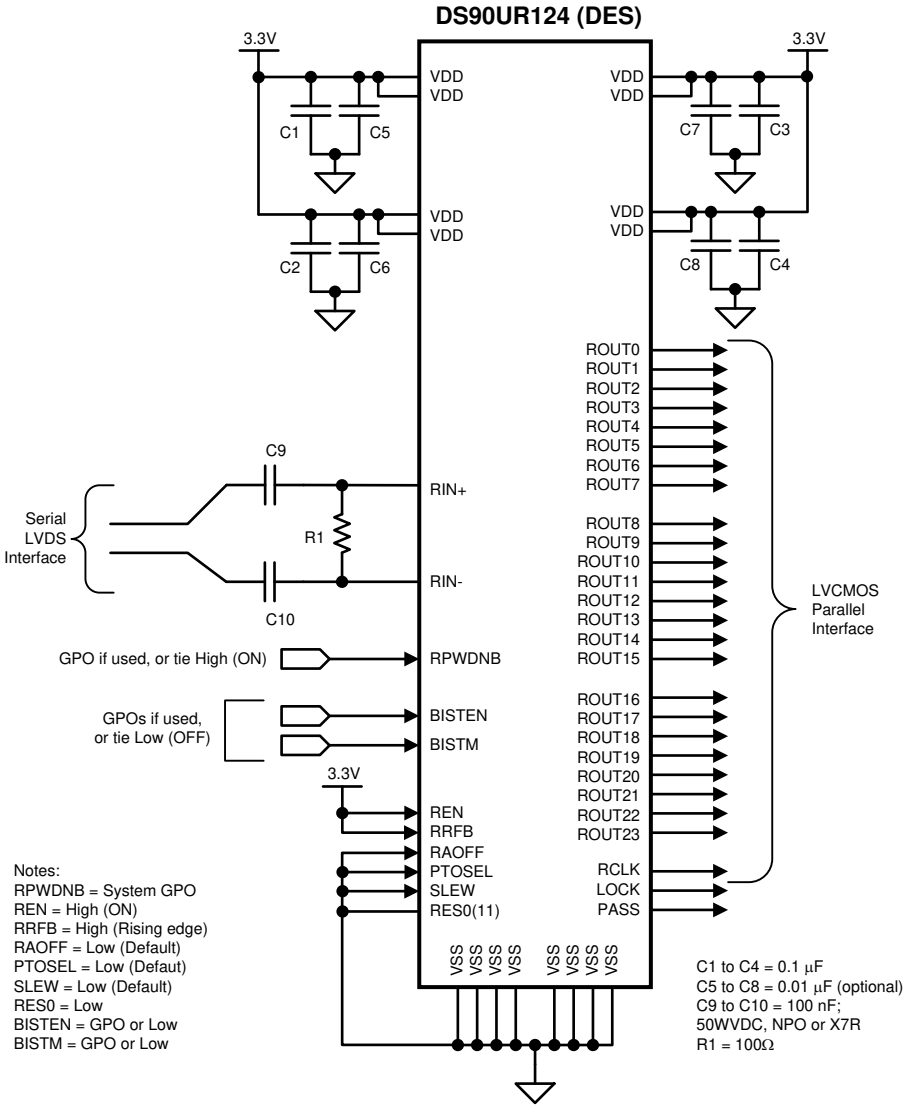


Figure 7-5. DS90UR124 Connection Diagram

2.2.1 Design Requirements

Table 7-2. DS90UR124 Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD	3.3V
DS90UR124-Q1 AC-Coupling Capacitor for RIN±	100nF
DS90UR124-Q1 Termination for RIN±	100Ω

2.2.2 Detailed Design Procedure

Figure 7-5 shows a typical application of the DS90UR124 deserializer for an 33MHz 18-bit Color Display Application. The RIN± inputs must have an external series 0.1uF AC-coupling capacitor and 100Ω parallel termination on the high-speed serial lines. The deserializer does not have an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1uF capacitors must be used for local device bypassing. Ferrite beads are needed on the VDDs for effective noise suppression. Additional capacitors are needed as the number and values of the capacitors depends on meeting the power noise specification of the

part. The interface to the display is with 3.3V LVCMOS levels. An RC delay is placed on the PDB signal to delay the enabling of the device until power is stable.

2.2.3 Application Curves

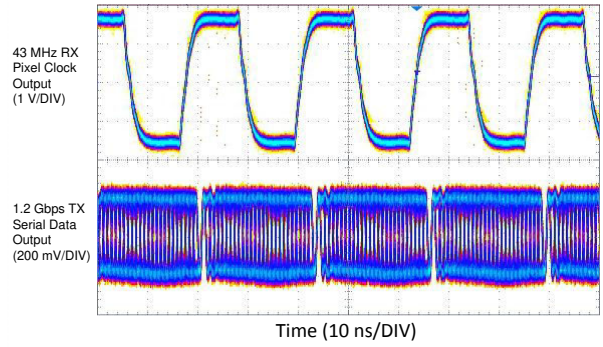


Figure 7-6. DS90UR241 Serial Stream and DS90UR124 43MHz PCLK Output

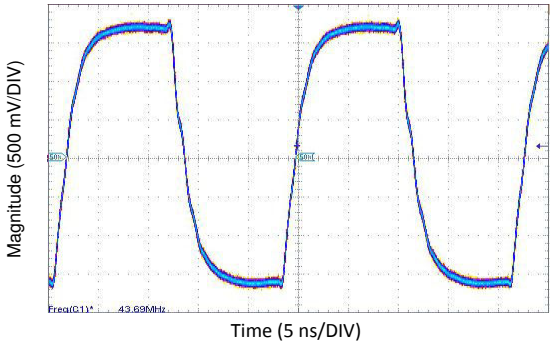


Figure 7-7. DS90UR124 PCLK Output at 43MHz (Enlarged)

3 Power Supply Recommendations

This device is designed to operate from an input core voltage supply of 3.3V. Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter can be used to provide clean power to sensitive circuits such as PLLs.

4 Layout

4.1 Layout Guidelines

4.1.1 PCB Layout and Power System Considerations

Circuit board layout and stack-up for the LVDS SERDES devices should be designed to provide low-noise power feed to the device. Good layout practice separates high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance can be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors can use values in the range of 0.01µF to 0.1µF. Tantalum capacitors can be in the range of 2.2µF to 10µF. Voltage rating of the tantalum capacitors must be at least 5× the power supply voltage being used.

Surface-mount capacitors are recommended due to smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20MHz to 30MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a 4-layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100Ω are typically recommended for LVDS interconnect. The closely coupled lines help to make sure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications, termination must be located at both ends of the devices. Nominal value is 100Ω to match the differential impedance of the line. Place the resistor as close to the transmitter DOUT± outputs and receiver RIN± inputs as possible to minimize the resulting stub between the termination resistor and device.

4.1.2 LVDS Interconnect Guidelines

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the *LVDS Owner's Manual* (SNLA187) - available in PDF format from the TI web site at: www.ti.com/lvds

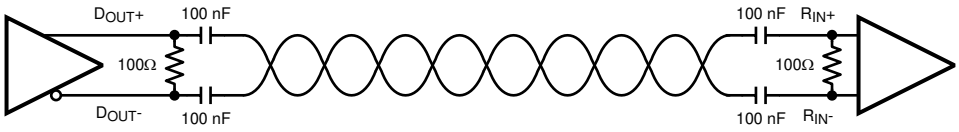
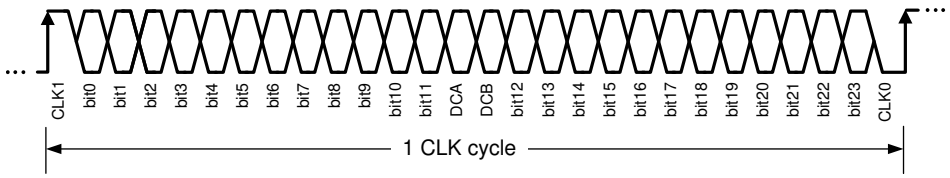


Figure 7-8. AC-Coupled Application



*Note: bits [0-23] are not physically located in positions shown above since bits [0-23] are scrambled and DC Balanced

Figure 7-9. Single Serialized LVDS Bitstream*

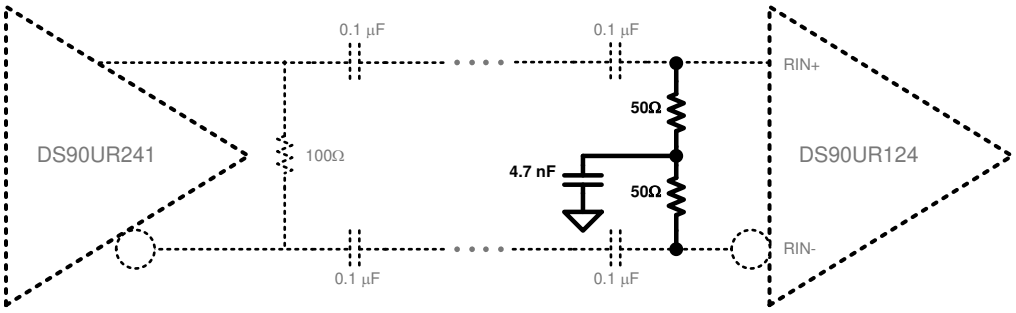


Figure 7-10. Receiver Termination Option 2

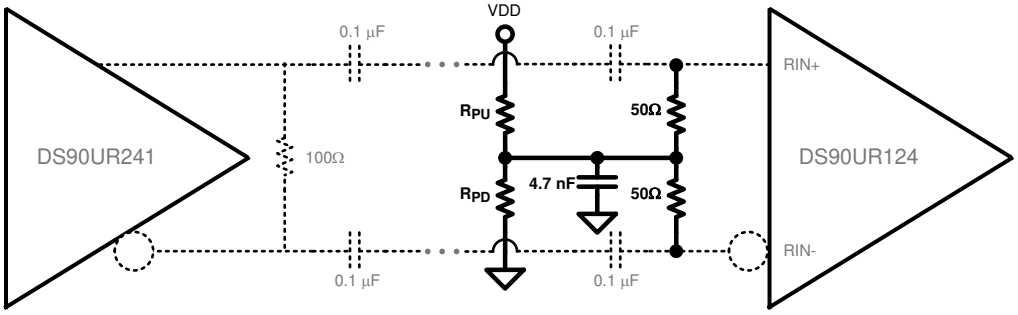


Figure 7-11. Receiver Termination Option 3

4.2 Layout Examples

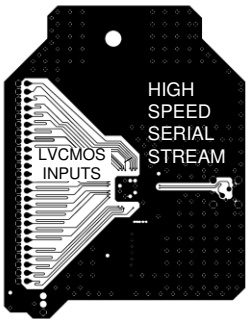


Figure 7-12. Example DS90UR241-Q1 EMC Layout

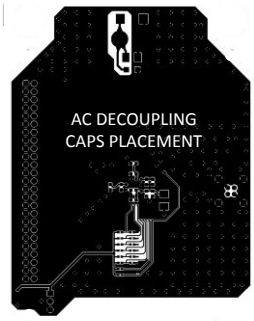


Figure 7-13. DS90UR241-Q1 EMC EVM Layer 4

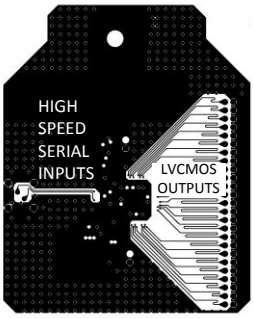


Figure 7-14. Example DS90UR124-Q1 EMC Layout

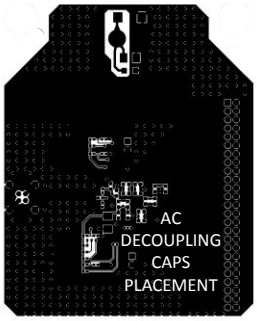


Figure 7-15. DS90UR124-Q1 EMC EVM Layer 4

7 Device and Documentation Support

7.1 Device Support

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation see the following:

- *LVDS Interconnect Guidelines AN-1108*, SNLA008
- *LVDS Interconnect Guidelines AN-905*, SNLA035

7.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (April 2015) to Revision P (August 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed ESD CDM rating for all pins from +/-12.5kV to +/-1kV	7

Changes from Revision N (March 2013) to Revision O (April 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision M (March 2013) to Revision N (March 2013)	Page
• Changed layout of National Data Sheet to TI format	23

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UR124IVS/NOPB	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 IVS
DS90UR124IVS/NOPB.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 IVS
DS90UR124IVSX/NOPB	Active	Production	TQFP (PAG) | 64	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 IVS
DS90UR124IVSX/NOPB.A	Active	Production	TQFP (PAG) | 64	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 IVS
DS90UR124QVS/NOPB	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 QVS
DS90UR124QVS/NOPB.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 QVS
DS90UR124QVSX/NOPB	Active	Production	TQFP (PAG) | 64	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 QVS
DS90UR124QVSX/NOPB.A	Active	Production	TQFP (PAG) | 64	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR124 QVS
DS90UR241IVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1IVS
DS90UR241IVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1IVS
DS90UR241IVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1IVS
DS90UR241IVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1IVS
DS90UR241QVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1QVS
DS90UR241QVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1QVS
DS90UR241QVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1QVS
DS90UR241QVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90UR24 1QVS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DS90UR124, DS90UR124-Q1, DS90UR241, DS90UR241-Q1 :

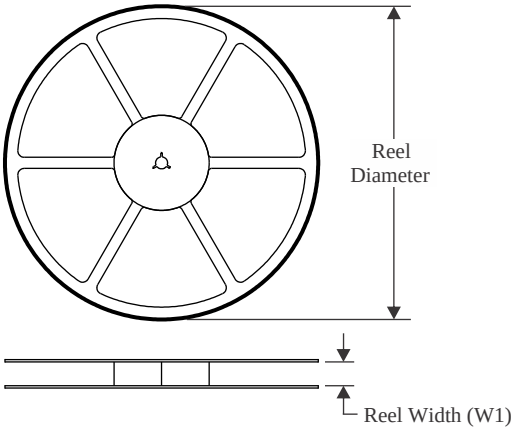
- Catalog : DS90UR124, DS90UR241
- Automotive : DS90UR124-Q1, DS90UR241-Q1

NOTE: Qualified Version Definitions:

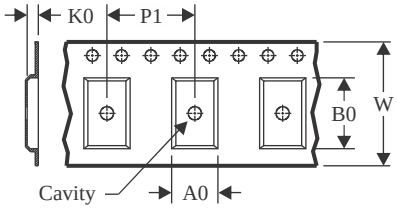
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

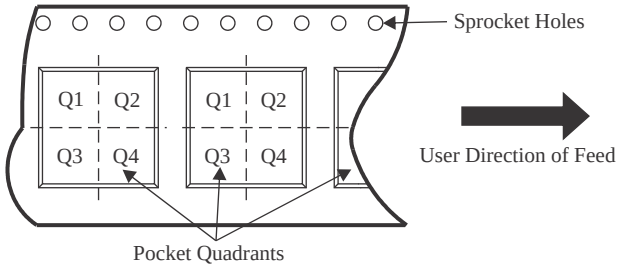


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

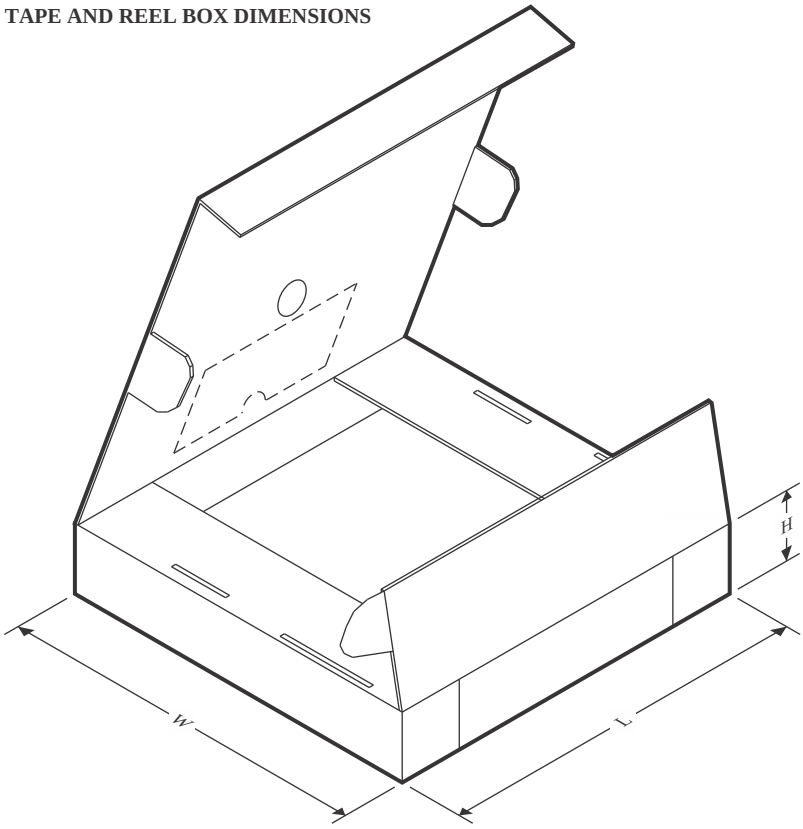
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UR124IVSX/NOPB	TQFP	PAG	64	1000	330.0	24.4	13.0	13.0	1.45	16.0	24.0	Q2
DS90UR124QVSX/NOPB	TQFP	PAG	64	1000	330.0	24.4	13.0	13.0	1.45	16.0	24.0	Q2
DS90UR241IVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2
DS90UR241QVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2

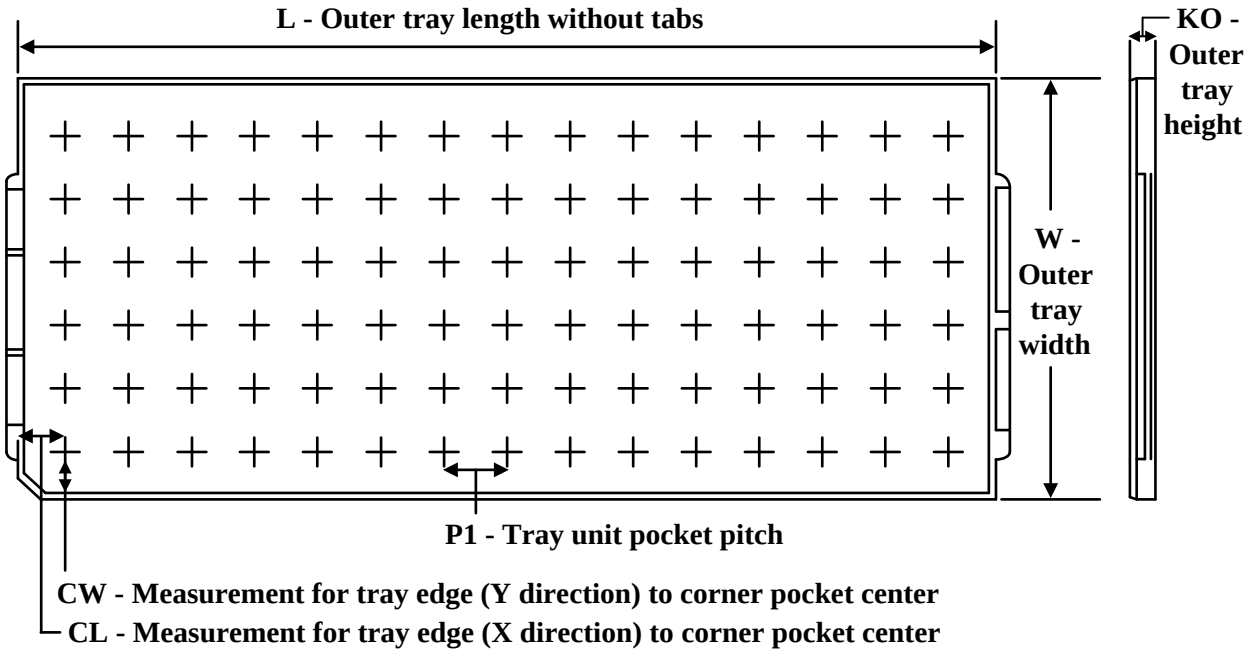
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UR124IVSX/NOPB	TQFP	PAG	64	1000	356.0	356.0	45.0
DS90UR124QVSX/NOPB	TQFP	PAG	64	1000	356.0	356.0	45.0
DS90UR241IVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0
DS90UR241QVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0

TRAY

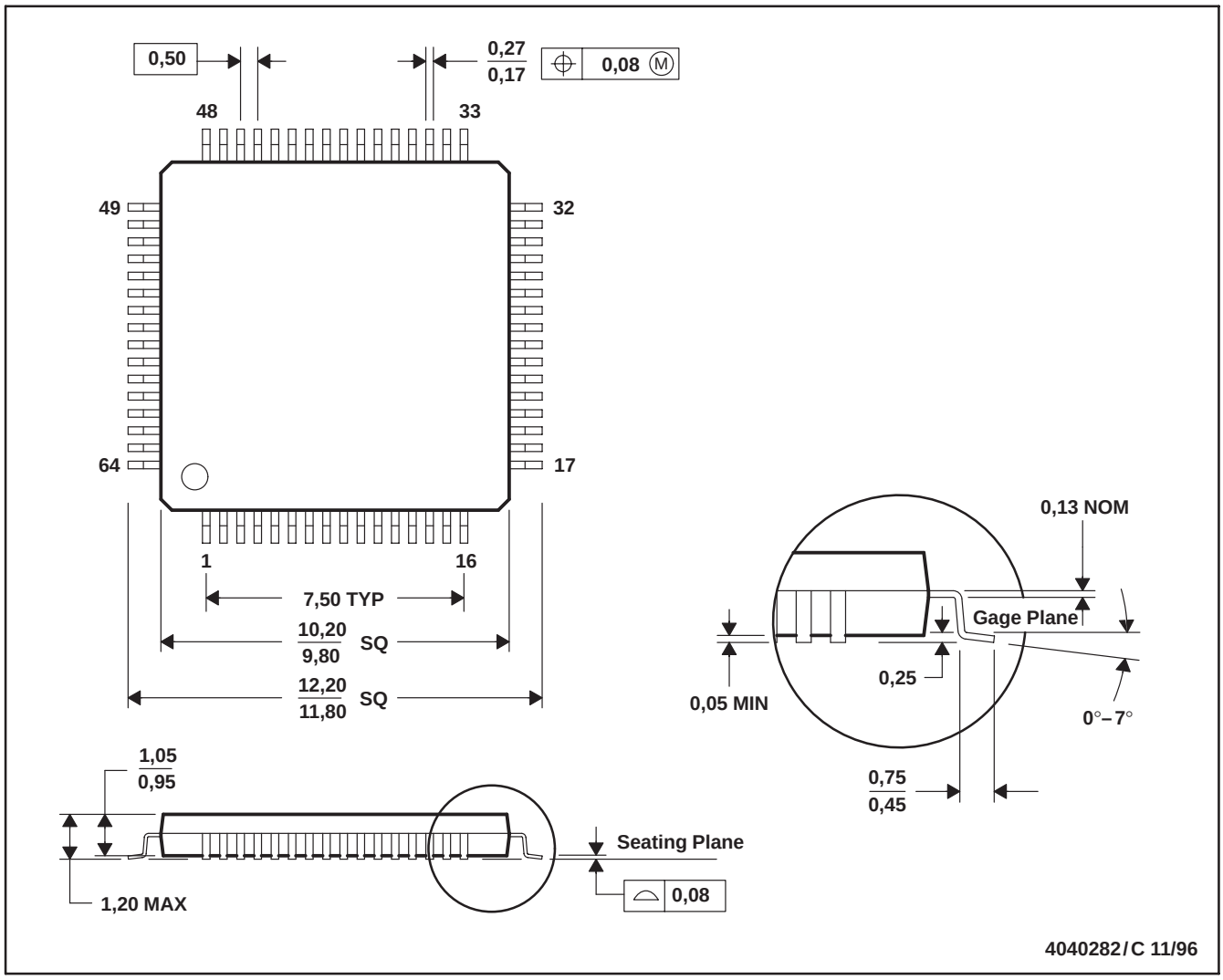


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS90UR124IVS/NOPB	PAG	TQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
DS90UR124IVS/ NOPB.A	PAG	TQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
DS90UR124QVS/NOPB	PAG	TQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
DS90UR124QVS/ NOPB.A	PAG	TQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
DS90UR241IVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90UR241IVS/ NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90UR241QVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90UR241QVS/ NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



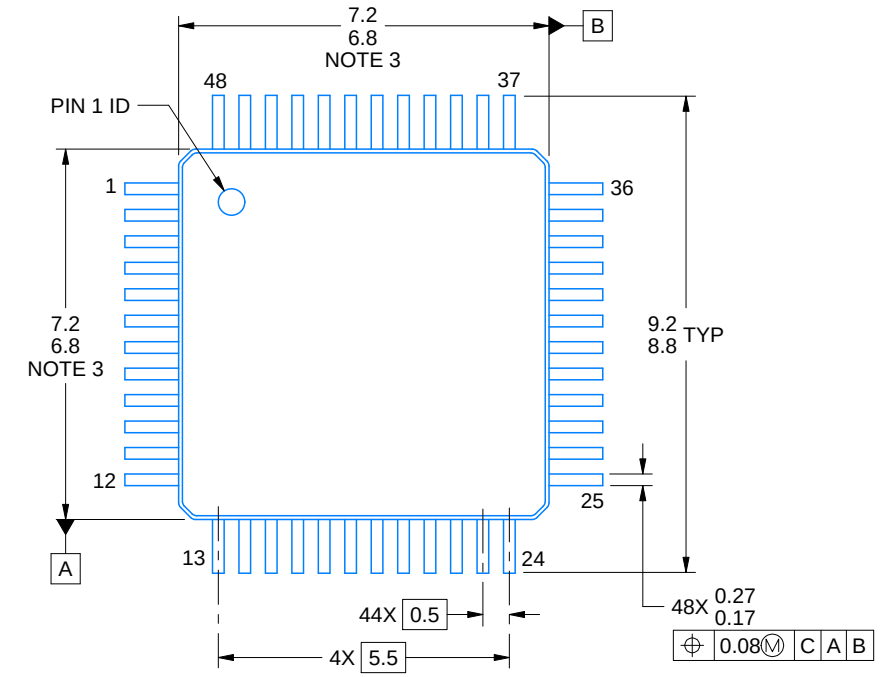
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

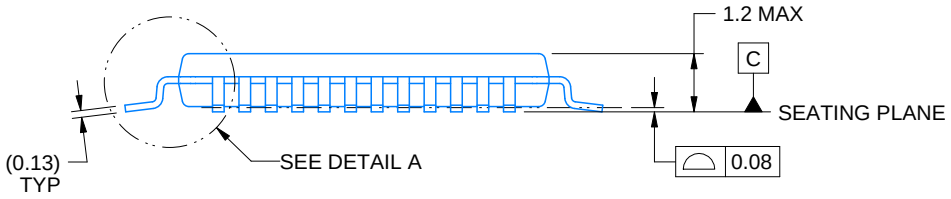
PACKAGE OUTLINE

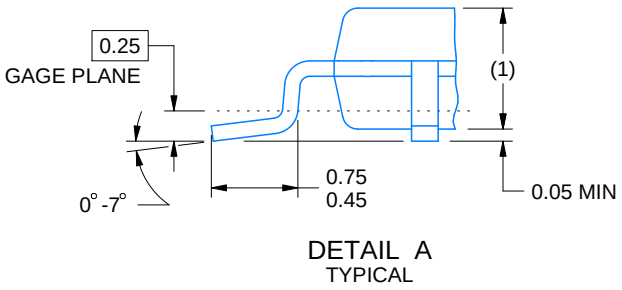
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK







DETAIL A
TYPICAL

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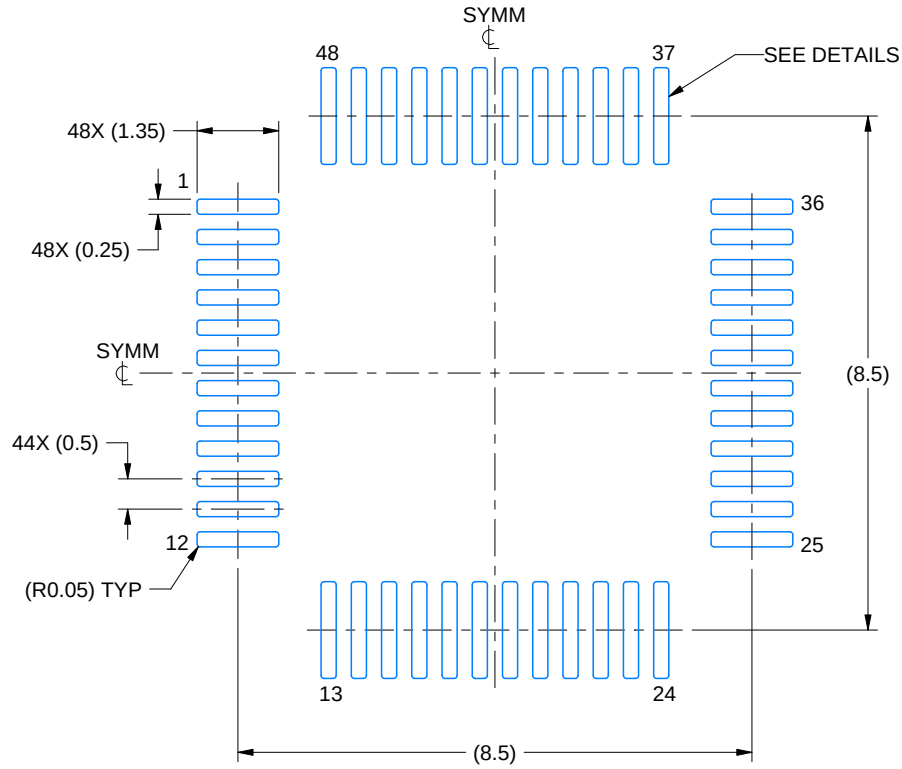
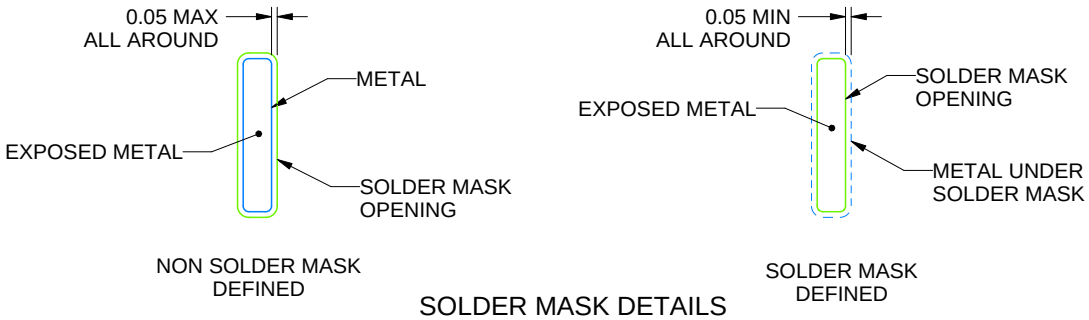
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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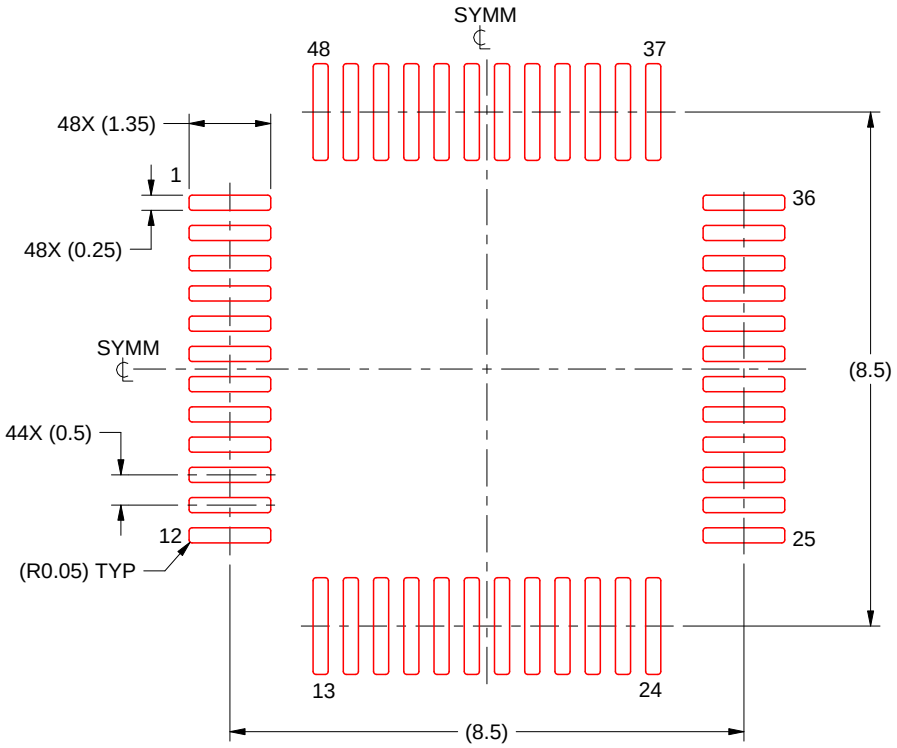
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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