# ISO774x-Q1 Automotive, High-Speed, Reinforced Quad-Channel Digital Isolators

## 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: –40°C to 125°C ambient operating temperature
- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISO7740-Q1, ISO7741-Q1, ISO7742-Q1
- 100 Mbps data rate
- Robust isolation barrier:
  - >30-year projected lifetime at 1500 $V_{RMS}$ working voltage
  - Up to 5700 $V_{RMS}$ isolation rating
  - Up to 12.8 kV surge capability
  - ±100 kV/µs typical CMTI
- Wide supply range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V level translation
- Default output *high* (ISO774x) and *low* (ISO774xF) options
- Low power consumption, typical 1.5 mA per channel at 1 Mbps
- Low propagation delay: 10.7 ns typical (5-V Supplies)
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Extra-wide SOIC (DWW-16), wide-SOIC (DW-16) and QSOP (DBQ-16) package options
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 61010-1, IEC 62368-1, IEC 60601-1, and GB 4943.1 certifications

## 2 Applications

- Hybrid, electric and powertrain system (EV/HEV)
  - Battery management system (BMS)
  - On-board charger
  - Traction inverter
  - DC/DC converter
  - Inverter and motor control

## 3 Description

The ISO774x-Q1 automotive devices are high-performance, quad-channel digital isolators with 5700 $V_{RMS}$ (DWW package), 5000 $V_{RMS}$ (DW package) and 3000 $V_{RMS}$ (DBQ package) isolation ratings per UL 1577. This family of devices has reinforced insulation ratings according to VDE, CSA, TUV and CQC.

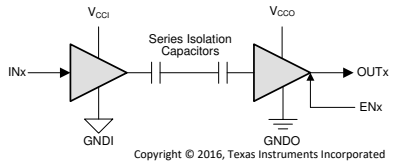
The ISO774x-Q1 devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide ($SiO_2$) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7740-Q1 device has all four channels in the same direction, the ISO7741-Q1 device has three forward and one reverse-direction channels, and the ISO7742-Q1 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is *high* for devices without suffix F and *low* for devices with suffix F. See the *Device Functional Modes* section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as CAN and LIN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO774x-Q1 devices have been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO774x-Q1 devices are available in 16-pin wide SOIC (DW) and QSOP (DBQ) packages. ISO7741-Q1 is also available in extra-wide SOIC (DWW) package.

**Device Information**

| PART NUMBER(1) | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ISO7741-Q1 | SOIC (DWW) | 10.30 mm × 14.0 mm |
| ISO7740-Q1<br>ISO7741-Q1<br>ISO7742-Q1 | SOIC (DW) | 10.30 mm × 7.50 mm |
| | SSOP (DBQ) | 4.90 mm × 3.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




$V_{CCI}$=Input supply, $V_{CCO}$=Output supply
GNDI=Input ground, GNDO=Output ground

**Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (July 2023) to Revision F (August 2023) | Page |
|---|---|
| • Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations | 9 |
| • Updated electrical and switching characteristics to match device performance | 14 |

| Changes from Revision D (October 2020) to Revision E (July 2023) | Page |
|---|---|
| • Changed standard name from: "DIN VDE V 0884-11:2017-01" to: "DIN EN IEC 60747-17 (VDE 0884-17)" throughout the document | 1 |
| • Removed standard revision and year references from all standard names throughout the document | 1 |
| • Added Maximum impulse voltage ($V_{IMP}$) specification per DIN EN IEC 60747-17 (VDE 0884-17) | 10 |
| • Changed test conditions and values of Maximum surge isolation voltage ($V_{IOSM}$) specification per DIN EN IEC 60747-17 (VDE 0884-17) | 10 |
| • Clarified method b test conditions of Apparent charge ($q_{PD}$) | 10 |
| • Removed references to standard IEC/EN/CSA 60950-1 throughout the document | 12 |
| • Switched the labels for $V_{CC1}$ falling and $V_{CC2}$ rising in the graph legend of *Power Supply Undervoltage Threshold vs Free-Air Temperature* | 24 |

| Changes from Revision C (February 2020) to Revision D (October 2020) | Page |
|---|---|
| • Added Functional Safety bullet in Section 1 | 1 |

| Changes from Revision B (June 2018) to Revision C (February 2020) | Page |
|---|---|
| • Made editorial and cosmetic changes throughout the document | 1 |


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- Changed From: "Isolation Barrier Life: >40 Years" To: " >100-year projected lifetime at 1500 $V_{RMS}$ working voltage" in Section 1 ..... 1
- Added "Up to 5700 $V_{RMS}$ isolation rating" in Section 1 ..... 1
- Added "Up to 12.8 kV surge capability" in Section 1 ..... 1
- Added "±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier" in Section 1 ..... 1
- Changed VDE standard name From: DIN V VDE V 0884-11:2017-01 To: DIN VDE V 0884-11:2017-01 throughout the document ..... 1
- Deleted "All Certifications Complete except CQC Approval of DBQ-16 Package Devices" in Section 1 ..... 1
- Updated list of applications in Section 2 section ..... 1
- Updated Figure 3-1 to show two isolation capacitors in series per channel instead of a single isolation capacitor ..... 1
- Added "Contact discharge per IEC 61000-4-2" specification of ±8000 V ..... 7
- Added the following table note to Data rate specification: "100 Mbps is the maximum specified data rate, although higher data rates are possible" ..... 8
- Changed ISO7741-Q1 $P_{D1}$ or Maximum power dissipation by side-1 from 50mW to 75 mW and $P_{D2}$ or Maximum power dissipation by side-2 from 150mW to 125 mW ..... 9
- Changed DW-16 package values of $V_{IORM}$ from 1414 $V_{PK}$ to 2121 $V_{PK}$ and and $V_{IOWM}$ from 1000 $V_{RMS}$ and 1414 $V_{DC}$ to 1500 $V_{RMS}$ and 2121 $V_{DC}$ ..... 10
- Modified test conditions of $V_{IOWM}$ and $V_{IOSM}$ ..... 10
- Updated table title to "Safety-Related Certifications" and updated certification information ..... 12
- Corrected ground symbol for 'Input (ISO774xF)' schematic in Section 8.4.1 ..... 31
- Updated Figure 9-1 by changing CAN transceiver From: SN65HVD231Q To: TCAN1042-Q1 and transformer driver From: SN6501-Q1 To: SN6505x-Q1 ..... 32
- Added SN6505x-Q1 reference in Section 10 section ..... 35
- Added '*How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*' application report to Section 12.1 section ..... 37
- Added SN6505x-Q1 data sheet reference in Section 12.1 section ..... 37

**Changes from Revision A (May 2018) to Revision B (June 2018)** **Page**

- Changed the isolation rating of the DBQ package from 2500 $V_{RMS}$ to 3000 $V_{RMS}$ ..... 1
- Moved the HBM and CDM values from the *Featues* section to the *ESD Ratings* table ..... 7
- Changed $V_{IOTM}$ from 3600 $V_{PK}$ to 4242 $V_{PK}$ for the DBQ package ..... 10
- Added $V_{TEST}$ to the conditions for the maximum transient isolation voltage parameter ..... 10
- Changed method b1 $V_{ini}$ condition for apparent charge ..... 10
- Changed all "plan to certify" to "Certified" and all "Certification Planned" to the proper certification number ..... 12
- Changed CMTI TYP value from 75kV/µs to 100 kV/µs in all Electrical Characteristics tables ..... 14
- Changed the $t_{DO}$ TYP value from 6µs to 0.1µs and the MAX value from 9µs to 0.3µs in all Switching Characteristics tables ..... 20
- Switched the line colors for $V_{CC}$ at 2.5 V and $V_{CC}$ at 3.3 V in Figure 6-14 ..... 24
- Switched the labels for $V_{CC1}$ falling and $V_{CC2}$ rising in the graph legend of *Power Supply Undervoltage Threshold vs Free-Air Temperature* ..... 24

**Changes from Revision * (November 2016) to Revision A (May 2018)** **Page**

- Updated the Safety-Related Certifications table ..... 12
- Changed minimum CMTI from 40 to 85 in all Electrical Characteristics tables ..... 14

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## 5 Pin Configuration and Functions

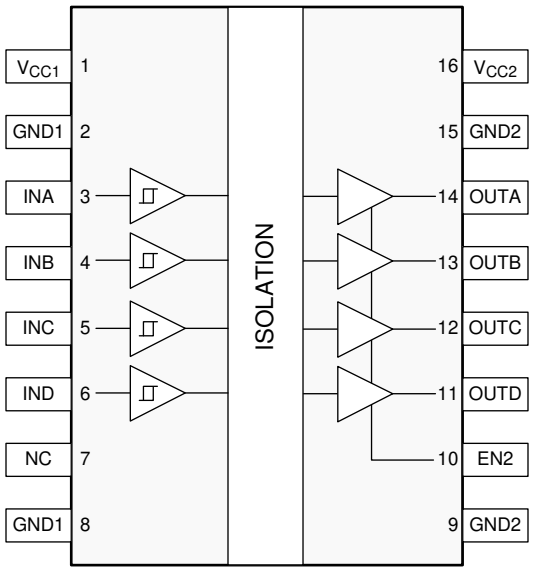



**Figure 5-1. ISO7740-Q1 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View**


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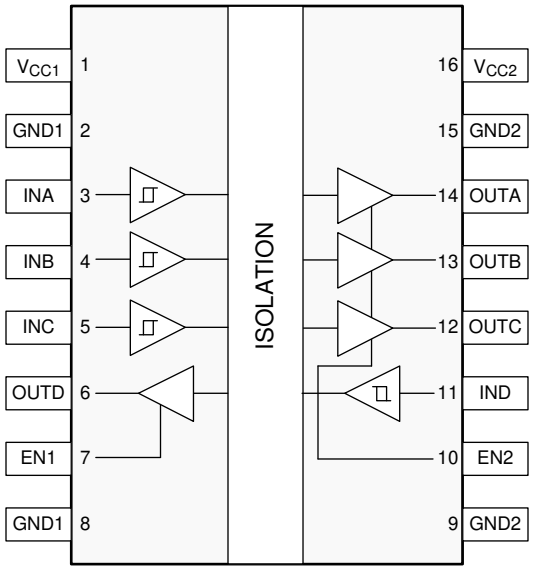



**Figure 5-2. ISO7741-Q1DWW, DW and DBQ Packages 16-Pin SOIC-Extra-WB, SOIC-WB and QSOP Top View**

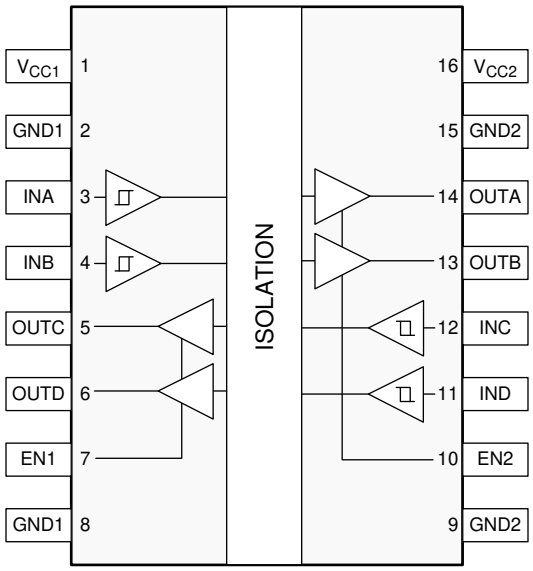



**Figure 5-3. ISO7742-Q1 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View**

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## Pin Functions

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | ISO7740-Q1 | ISO7741-Q1 | ISO7742-Q1 | | |
| EN1 | — | 7 | 7 | I | Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. |
| EN2 | 10 | 10 | 10 | I | Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| GND1 | 2 | 2 | 2 | — | Ground connection for $V_{CC1}$ |
| | 8 | 8 | 8 | | |
| GND2 | 9 | 9 | 9 | — | Ground connection for $V_{CC2}$ |
| | 15 | 15 | 15 | | |
| INA | 3 | 3 | 3 | I | Input, channel A |
| INB | 4 | 4 | 4 | I | Input, channel B |
| INC | 5 | 5 | 12 | I | Input, channel C |
| IND | 6 | 11 | 11 | I | Input, channel D |
| NC | 7 | — | — | — | Not connected |
| OUTA | 14 | 14 | 14 | O | Output, channel A |
| OUTB | 13 | 13 | 13 | O | Output, channel B |
| OUTC | 12 | 12 | 5 | O | Output, channel C |
| OUTD | 11 | 6 | 6 | O | Output, channel D |
| $V_{CC1}$ | 1 | 1 | 1 | — | Power supply, side 1 |
| $V_{CC2}$ | 16 | 16 | 16 | — | Power supply, side 2 |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

See(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage (2) | -0.5 | 6 | V |
| V | Voltage at INx, OUTx, ENx | -0.5 | $V_{CCX}$ + 0.5 (3) | V |
| $I_O$ | Output current | -15 | 15 | mA |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 HBM ESD Classification Level 3A (1) | ±6000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 V CDM ESD Classification Level C6 | ±1500 | V |
| | | Contact discharge per IEC 61000-4-2; Isolation barrier withstand test (2) (3) | ±8000 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply Voltage | | 2.25 | | 5.5 | V |
| $V_{CC(UVLO+)}$ | UVLO threshold when supply voltage is rising | | | 2 | 2.25 | V |
| $V_{CC(UVLO-)}$ | UVLO threshold when supply voltage is falling | | 1.7 | 1.8 | | V |
| $V_{HYS(UVLO)}$ | Supply voltage UVLO hysteresis | | 100 | 200 | | mV |
| $I_{OH}$ | High level output current | $V_{CCO}$ = 5 V (1) | -4 | | | mA |
| | | $V_{CCO}$ = 3.3 V | -2 | | | |
| | | $V_{CCO}$ = 2.5 V | -1 | | | |
| $I_{OL}$ | Low level output current | $V_{CCO}$ = 5 V | | | 4 | mA |
| | | $V_{CCO}$ = 3.3 V | | | 2 | |
| | | $V_{CCO}$ = 2.5 V | | | 1 | |
| $V_{IH}$ | High level Input voltage | | 0.7 x $V_{CCI}$ (1) | | $V_{CCI}$ | V |
| $V_{IL}$ | Low level Input voltage | | 0 | | 0.3 x $V_{CCI}$ | V |
| DR | Data Rate(2) | | 0 | | 100 | Mbps |
| $T_A$ | Ambient temperature | | -40 | 25 | 125 | °C |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$.
(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | ISO774x-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | DWW (SOIC) | DW (SOIC) | DBQ (QSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 58.3 | 83.4 | 109 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.4 | 46 | 54.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 30.5 | 48 | 51.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.1 | 19.1 | 14.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 29.8 | 47.5 | 51.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7740-Q1** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L =$ 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 210 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 45 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 165 | mW |
| **ISO7741-Q1** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L =$ 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 210 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 75 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 135 | mW |
| **ISO7742-Q1** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L =$ 15 pF, Input a 50-MHz 50% duty cycle square wave | | | 210 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 105 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 105 | mW |

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## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | | | UNIT |
|---|---|---|---|---|---|---|
| | | | DWW-16 | DW-16 | DBQ-16 | |
| CLR | External clearance(1) | Shortest terminal-to-terminal distance through air | >14.5 | >8 | >3.7 | mm |
| CPG | External creepage(1) | Shortest terminal-to-terminal distance across the package surface | >14.5 | >8 | >3.7 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | >17 | >17 | >17 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | >600 | >600 | >600 | V |
| | Material group | According to IEC 60664-1 | I | I | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 300 $V_{RMS}$ | I-IV | I-IV | I-III | |
| | | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | I-IV | n/a | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-IV | I-III | n/a | |
| **DIN EN IEC 60747-17 (VDE 0884-17)** (2) | | | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2828 | 2121 | 566 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum working isolation voltage | AC voltage; Time dependent dielectric breakdown (TDDB) Test; See Insulation Lifetime Projection Data | 2000 | 1500 | 400 | $V_{RMS}$ |
| | | DC voltage | 2828 | 2121 | 566 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production) | 8000 | 8000 | 4242 | $V_{PK}$ |
| $V_{IMP}$ | Maximum impulse voltage(3) | Tested in air, 1.2/50-µs waveform per IEC 62368-1 | 9600 | 8000 | 4000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(4) | $V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1 | 12800 | 12800 | 10000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(5) | Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m$ = 10 s | ≤5 | ≤5 | ≤5 | pC |
| | | Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m$ = 10 s | ≤5 | ≤5 | ≤5 | |
| | | Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini}$ = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m$ = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2) | ≤5 | ≤5 | ≤5 | |
| $C_{IO}$ | Barrier capacitance, input to output(6) | $V_{IO}$ = 0.4 x sin (2πft), f = 1 MHz | ~1 | ~1 | ~1 | pF |
| $R_{IO}$ | Isolation resistance(6) | $V_{IO}$ = 500 V, $T_A$ = 25°C | $>10^{12}$ | $>10^{12}$ | $>10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | $>10^{11}$ | $>10^{11}$ | $>10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | $>10^{9}$ | $>10^{9}$ | $>10^{9}$ | |
| | Pollution degree | | 2 | 2 | 2 | |
| | Climatic category | | 55/125/21 | 55/125/21 | 55/125/21 | |
| **UL 1577** | | | | | | |
| $V_{ISO}$ | Maximum withstanding isolation voltage | $V_{TEST} = V_{ISO}$ , t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1 s (100% production) | 5700 | 5000 | 3000 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package.


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(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

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## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17) | Certified according to IEC 62368-1 and IEC 60601-1 | Certified according to UL 1577 Component Recognition Program | Certified according to GB 4943.1 | Certified according to EN 61010-1 and EN 62368-1 |
| Maximum transient isolation voltage, 8000 $V_{PK}$ (DWW-16, DW-16, Reinforced) and 4242 $V_{PK}$ (DBQ-16); Maximum repetitive peak isolation voltage, 2828 $V_{PK}$ (DWW-16, Reinforced), 2121 $V_{PK}$ (DW-16, Reinforced) and 566 $V_{PK}$ (DBQ-16); Maximum surge isolation voltage, 12800 $V_{PK}$ (DWW-16, DW-16, Reinforced) and 10000 $V_{PK}$ (DBQ-16) | Reinforced insulation per CSA 62368-1 and IEC 62368-1, 1450 $V_{RMS}$ (DWW-16), 600 $V_{RMS}$ (DW-16) and 370 $V_{RMS}$ (DBQ-16) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 400 $V_{RMS}$ (DWW-16) and 250 $V_{RMS}$ (DW-16) max working voltage | DWW-16: Single Protection, 5700 $V_{RMS}$; DW-16: Single protection, 5000 $V_{RMS}$; DBQ-16: Single protection, 3000 $V_{RMS}$ | DWW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 1450 $V_{RMS}$ maximum working voltage; DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 $V_{RMS}$ maximum working voltage; DBQ-16: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 $V_{RMS}$ maximum working voltage | 5700 $V_{RMS}$ (DWW-16), 5000 $V_{RMS}$ (DW-16) and 3000 $V_{RMS}$ (DBQ-16) Reinforced insulation per EN 61010-1 up to working voltage of 1000 $V_{RMS}$ (DWW-16), 600 $V_{RMS}$ (DW-16) and 300 $V_{RMS}$ (DBQ-16); 5700 $V_{RMS}$ (DWW-16), 5000 $V_{RMS}$ (DW-16) and 3000 $V_{RMS}$ (DBQ-16) Reinforced insulation per EN 62368-1 up to working voltage of 1450 $V_{RMS}$ (DWW-16), 600 $V_{RMS}$ (DW-16) and 370 $V_{RMS}$ (DBQ-16) |
| Reinforced certificate: 40040142 | Master contract number: 220991 | File number: E181974 | Certificate numbers: CQC15001121716 (DWx-16) CQC18001199097 (DBQ-16) | Client ID number: 77311 |

## 6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DWW-16 PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 58.3 °C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-1 | | | 390 | mA |
| | | $R_{\theta JA}$ = 58.3 °C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-1 | | | 596 | mA |
| | | $R_{\theta JA}$ = 58.3 °C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-1 | | | 780 | mA |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 58.3 °C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-4 | | | 2144 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |
| **DW-16 PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ =83.4°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-2 | | | 273 | mA |
| | | $R_{\theta JA}$ = 83.4°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-2 | | | 416 | |
| | | $R_{\theta JA}$ = 83.4°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-2 | | | 545 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 83.4°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-5 | | | 1499 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |
| **DBQ-16 PACKAGE** | | | | | | |


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Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ =109°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-3 | | | 209 | mA |
| | | $R_{\theta JA}$ = 109°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-3 | | | 319 | |
| | | $R_{\theta JA}$ = 109°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-3 | | | 417 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 109°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 6-6 | | | 1147 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in Section 6.4 is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.

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## 6.9 Electrical Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -4 mA; See Figure 7-1 | $V_{CCO}$ - 0.4 (1) | 4.8 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; See Figure 7-1 | | 0.2 | 0.4 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | 0.6 x $V_{CCI}$ | 0.7 x $V_{CCI}$ | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | 0.4 x $V_{CCI}$ | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | 0.2 x $V_{CCI}$ | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx or ENx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CCI}$ or 0 V, $V_{CM}$ = 1200 V; See Figure 7-4 | 85 | 100 | | kV/µs |
| $C_I$ | Input Capacitance (2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 1 MHz, $V_{CC}$ = 5 V | | 2 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.


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## 6.10 Supply Current Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7740-Q1** | | | | | | | |
| Supply current - Disable | EN2 = 0 V; $V_I$ = $V_{CC1}$ (1)(ISO7740-Q1); $V_I$ = 0 V (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 1.2 | 2.3 | mA |
| | | | $I_{CC2}$ | | 0.3 | 0.8 | |
| | EN2 = 0 V; $V_I$ = 0 V (1)(ISO7740-Q1); $V_I$ = $V_{CC1}$ (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 5.5 | 7.8 | |
| | | | $I_{CC2}$ | | 0.3 | 0.8 | |
| Supply current - DC signal | EN2 = $V_{CC2}$; $V_I$ = $V_{CC1}$ (1)(ISO7740-Q1); $V_I$ = 0 V (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 1.2 | 2.3 | |
| | | | $I_{CC2}$ | | 2 | 3.6 | |
| | EN2 = $V_{CC2}$; $V_I$ = 0 V (ISO7740-Q1); $V_I$ = $V_{CC1}$ (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 5.5 | 7.8 | |
| | | | $I_{CC2}$ | | 2.2 | 3.9 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 3.3 | 4.7 | |
| | | | $I_{CC2}$ | | 2.3 | 4 | |
| | | 10 Mbps | $I_{CC1}$ | | 3.4 | 4.9 | |
| | | | $I_{CC2}$ | | 4.2 | 6.4 | |
| | | 100 Mbps | $I_{CC1}$ | | 3.8 | 6.6 | |
| | | | $I_{CC2}$ | | 22.7 | 29.5 | |
| **ISO7741-Q1** | | | | | | | |
| Supply current - Disable | EN1 = EN2 = 0 V; $V_I$ = $V_{CCI}$ (ISO7741-Q1); $V_I$ = 0 V (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 1 | 2.2 | mA |
| | | | $I_{CC2}$ | | 0.8 | 1.6 | |
| | EN1 = EN2 = 0 V; $V_I$ = 0 V (ISO7741-Q1); $V_I$ = $V_{CCI}$ (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 4.3 | 6.3 | |
| | | | $I_{CC2}$ | | 1.8 | 2.8 | |
| Supply current - DC signal | EN1 = EN2 = $V_{CCI}$; $V_I$ = $V_{CCI}$ (1)(ISO7741-Q1); $V_I$ = 0 V (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 1.5 | 2.9 | |
| | | | $I_{CC2}$ | | 2 | 3.7 | |
| | EN1 = EN2 = $V_{CCI}$; $V_I$ = 0 V (ISO7741-Q1); $V_I$ = $V_{CCI}$ (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 4.8 | 6.8 | |
| | | | $I_{CC2}$ | | 3.2 | 5.2 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 3.2 | 4.8 | |
| | | | $I_{CC2}$ | | 2.8 | 4.6 | |
| | | 10 Mbps | $I_{CC1}$ | | 3.7 | 5.5 | |
| | | | $I_{CC2}$ | | 4.2 | 6.4 | |
| | | 100 Mbps | $I_{CC1}$ | | 8.6 | 12.5 | |
| | | | $I_{CC2}$ | | 18 | 24 | |
| **ISO7742-Q1** | | | | | | | |
| Supply current - Disable | EN1 = EN2 = 0 V; $V_I$ = $V_{CCI}$ (1)(ISO7742-Q1); $V_I$ = 0 V (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 0.9 | 2 | mA |
| | EN1 = EN2 = 0 V; $V_I$ = 0 V (1)(ISO7742-Q1); $V_I$ = $V_{CCI}$ (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 3 | 4.6 | |
| Supply current - DC signal | EN1 = EN2 = $V_{CCI}$; $V_I$ = $V_{CCI}$ (1)(ISO7742-Q1); $V_I$ = 0 V (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 1.7 | 3.5 | |
| | EN1 = EN2 = $V_{CCI}$; $V_I$ = 0 V (ISO7742-Q1); $V_I$ = $V_{CCI}$ (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 4 | 6 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$, $I_{CC2}$ | | 3 | 4.9 | |
| | | 10 Mbps | $I_{CC1}$, $I_{CC2}$ | | 4 | 6 | |
| | | 100 Mbps | $I_{CC1}$, $I_{CC2}$ | | 13.4 | 18.3 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

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## 6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -2mA; See Figure 7-1 | $V_{CCO}$ - 0.3 (1) | 3.2 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2mA; See Figure 7-1 | | 0.1 | 0.3 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | 0.6 x $V_{CCI}$ | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | 0.4 x $V_{CCI}$ | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | 0.2 x $V_{CCI}$ | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx or ENx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CCI}$ or 0 V, $V_{CM}$ = 1200 V; See Figure 7-4 | 85 | 100 | | kV/µs |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$


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## 6.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7740-Q1** | | | | | | | |
| Supply current - Disable | EN2 = 0 V; $V_I$ = $V_{CC1}$ (1)(ISO7740-Q1); $V_I$ = 0 V (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 1.2 | 2.3 | mA |
| | | | $I_{CC2}$ | | 0.3 | 0.7 | |
| | EN2 = 0 V; $V_I$ = 0 V (1)(ISO7740-Q1); $V_I$ = $V_{CC1}$ (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 5.5 | 7.8 | |
| | | | $I_{CC2}$ | | 0.3 | 0.7 | |
| Supply current - DC signal | EN2 = $V_{CC2}$; $V_I$ = $V_{CC1}$ (1)(ISO7740-Q1); $V_I$ = 0 V (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 1.2 | 2.2 | |
| | | | $I_{CC2}$ | | 1.9 | 3.6 | |
| | EN2 = $V_{CC2}$; $V_I$ = 0 V (ISO7740-Q1); $V_I$ = $V_{CC1}$ (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 5.5 | 7.8 | |
| | | | $I_{CC2}$ | | 2.2 | 3.9 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 3.3 | 4.7 | |
| | | | $I_{CC2}$ | | 2.2 | 3.9 | |
| | | 10 Mbps | $I_{CC1}$ | | 3.4 | 4.7 | |
| | | | $I_{CC2}$ | | 3.6 | 5.6 | |
| | | 100 Mbps | $I_{CC1}$ | | 3.3 | 5.7 | |
| | | | $I_{CC2}$ | | 17 | 22.3 | |
| **ISO7741-Q1** | | | | | | | |
| Supply current - Disable | EN1 = EN2 = 0 V; $V_I$ = $V_{CCI}$ (ISO7741-Q1); $V_I$ = 0 V (ISO7741-Q1with F suffix) | | $I_{CC1}$ | | 1 | 2.1 | mA |
| | | | $I_{CC2}$ | | 0.8 | 1.5 | |
| | EN1 = EN2 = 0 V; $V_I$ = 0 V (ISO7741-Q1); $V_I$ = $V_{CCI}$ (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 4.3 | 6.3 | |
| | | | $I_{CC2}$ | | 1.9 | 2.7 | |
| Supply current - DC signal | EN1 = EN2 = $V_{CCI}$; $V_I$ = $V_{CCI}$ (1)(ISO7741-Q1); $V_I$ = 0 V (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 1.5 | 2.8 | |
| | | | $I_{CC2}$ | | 2 | 3.7 | |
| | EN1 = EN2 = $V_{CCI}$; $V_I$ = 0 V (ISO7741-Q1); $V_I$ = $V_{CCI}$ (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 4.8 | 6.8 | |
| | | | $I_{CC2}$ | | 3.2 | 5.1 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 3.2 | 4.7 | |
| | | | $I_{CC2}$ | | 2.7 | 4.5 | |
| | | 10 Mbps | $I_{CC1}$ | | 3.5 | 5.2 | |
| | | | $I_{CC2}$ | | 3.7 | 5.8 | |
| | | 100 Mbps | $I_{CC1}$ | | 6.8 | 10 | |
| | | | $I_{CC2}$ | | 13.7 | 18.6 | |
| **ISO7742-Q1** | | | | | | | |
| Supply current - Disable | EN1 = EN2 = 0 V; $V_I$ = $V_{CCI}$ (1)(ISO7742-Q1); $V_I$ = 0 V (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 0.9 | 2 | mA |
| | EN1 = EN2 = 0 V; $V_I$ = 0 V (1)(ISO7742-Q1); $V_I$ = $V_{CCI}$ (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 3 | 4.6 | |
| Supply current - DC signal | EN1 = EN2 = $V_{CCI}$; $V_I$ = $V_{CCI}$ (1)(ISO7742-Q1); $V_I$ = 0 V (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 1.7 | 3.4 | |
| | EN1 = EN2 = $V_{CCI}$; $V_I$ = 0 V (ISO7742-Q1); $V_I$ = $V_{CCI}$ (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 4 | 5.9 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.9 | 4.8 | |
| | | 10 Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.6 | 5.6 | |
| | | 100 Mbps | $I_{CC1}$, $I_{CC2}$ | | 10.3 | 14.4 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

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## 6.13 Electrical Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -1mA; See Figure 7-1 | $V_{CCO}$ - 0.2(1) | 2.45 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1mA; See Figure 7-1 | | 0.05 | 0.2 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | 0.6 x $V_{CCI}$ | 0.7 x $V_{CCI}$ | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | 0.4 x $V_{CCI}$ | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | 0.2 x $V_{CCI}$ | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx or ENx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CCI}$ or 0 V, $V_{CM}$ = 1200 V; See Figure 7-4 | 85 | 100 | | kV/µs |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$


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## 6.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO7740-Q1** | | | | | | | |
| Supply current - Disable | EN2 = 0 V; $V_I$ = $V_{CC1}$ (1)(ISO7740-Q1); $V_I$ = 0 V (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 1.2 | 2.2 | mA |
| | | | $I_{CC2}$ | | 0.3 | 0.7 | |
| | EN2 = 0 V; $V_I$ = 0 V (1)(ISO7740-Q1); $V_I$ = $V_{CC1}$ (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 5.5 | 7.8 | |
| | | | $I_{CC2}$ | | 0.3 | 0.7 | |
| Supply current - DC signal | EN2 = $V_{CC2}$; $V_I$ = $V_{CC1}$ (1)(ISO7740-Q1); $V_I$ = 0 V (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 1.2 | 2.2 | |
| | | | $I_{CC2}$ | | 1.9 | 3.6 | |
| | EN2 = $V_{CC2}$; $V_I$ = 0 V (ISO7740-Q1); $V_I$ = $V_{CC1}$ (ISO7740-Q1 with F suffix) | | $I_{CC1}$ | | 5.4 | 7.8 | |
| | | | $I_{CC2}$ | | 2.2 | 3.9 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 3.3 | 4.7 | |
| | | | $I_{CC2}$ | | 2.2 | 3.9 | |
| | | 10 Mbps | $I_{CC1}$ | | 3.4 | 4.8 | |
| | | | $I_{CC2}$ | | 3.2 | 5.1 | |
| | | 100 Mbps | $I_{CC1}$ | | 3.2 | 5.5 | |
| | | | $I_{CC2}$ | | 13 | 17.7 | |
| **ISO7741-Q1** | | | | | | | |
| Supply current - Disable | EN1 = EN2 = 0 V; $V_I$ = $V_{CCI}$ (ISO7741-Q1); $V_I$ = 0 V (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 1 | 5.7 | mA |
| | | | $I_{CC2}$ | | 0.8 | 2.8 | |
| | EN1 = EN2 = 0 V; $V_I$ = 0 V (ISO7741-Q1); $V_I$ = $V_{CCI}$ (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 4.3 | 6.3 | |
| | | | $I_{CC2}$ | | 1.8 | 2.8 | |
| Supply current - DC signal | EN1 = EN2 = $V_{CCI}$; $V_I$ = $V_{CCI}$ (1)(ISO7741-Q1); $V_I$ = 0 V (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 1.4 | 2.9 | |
| | | | $I_{CC2}$ | | 2 | 3.9 | |
| | EN1 = EN2 = $V_{CCI}$; $V_I$ = 0 V (ISO7741-Q1); $V_I$ = $V_{CCI}$ (ISO7741-Q1 with F suffix) | | $I_{CC1}$ | | 4.7 | 6.8 | |
| | | | $I_{CC2}$ | | 3.2 | 5.21 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$ | | 3.1 | 4.8 | |
| | | | $I_{CC2}$ | | 2.7 | 4.7 | |
| | | 10 Mbps | $I_{CC1}$ | | 3.4 | 5.2 | |
| | | | $I_{CC2}$ | | 3.5 | 5.64 | |
| | | 100 Mbps | $I_{CC1}$ | | 5.6 | 8.7 | |
| | | | $I_{CC2}$ | | 10.8 | 15 | |
| **ISO7742-Q1** | | | | | | | |
| Supply current - Disable | EN1 = EN2 = 0 V; $V_I$ = $V_{CCI}$ (1)(ISO7742-Q1); $V_I$ = 0 V (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 0.9 | 1.9 | mA |
| | EN1 = EN2 = 0 V; $V_I$ = 0 V (1)(ISO7742-Q1); $V_I$ = $V_{CCI}$ (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 3 | 4.6 | |
| Supply current - DC signal | EN1 = EN2 = $V_{CCI}$; $V_I$ = $V_{CCI}$ (1)(ISO7742-Q1); $V_I$ = 0 V (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 1.7 | 3.4 | |
| | EN1 = EN2 = $V_{CCI}$; $V_I$ = 0 V (ISO7742-Q1); $V_I$ = $V_{CCI}$ (ISO7742-Q1 with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 4 | 5.9 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15 pF | 1 Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.9 | 4.7 | |
| | | 10 Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.4 | 5.4 | |
| | | 100 Mbps | $I_{CC1}$, $I_{CC2}$ | | 8.3 | 11.9 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

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## 6.15 Switching Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 7-1 | 6 | 10.7 | 17 | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | 0 | 5.9 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same-direction channels | | | 4 | ns |
| $t_{sk(pp)}$ | Part-to-part skew time(3) | | | | 4.4 | ns |
| $t_r$ | Output signal rise time | See Figure 7-1 | | 2.4 | 3.9 | ns |
| $t_f$ | Output signal fall time | | | 2.4 | 3.9 | ns |
| $t_{PHZ}$ | Disable propagation delay, high-to-high impedance output | See Figure 7-2 | | 14 | 22 | ns |
| $t_{PLZ}$ | Disable propagation delay, low-to-high impedance output | | | 13 | 20 | ns |
| $t_{PZH}$ | Enable propagation delay, high impedance-to-high output for ISO774x | | | 11.5 | 20 | ns |
| | Enable propagation delay, high impedance-to-high output for ISO774x with F suffix | | | 3 | 8.5 | µs |
| $t_{PZL}$ | Enable propagation delay, high impedance-to-low output for ISO774x | | | 2.5 | 8.5 | µs |
| | Enable propagation delay, high impedance-to-low output for ISO774x with F suffix | | | 7 | 20 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7V. See Figure 7-4 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 100 Mbps | | 0.8 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.


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## 6.16 Switching Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 7-1 | 6 | 12 | 18.5 | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | 0.1 | 5.9 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same-direction channels | | | 4.4 | ns |
| $t_{sk(pp)}$ | Part-to-part skew time(3) | | | | 5 | ns |
| $t_r$ | Output signal rise time | See Figure 7-1 | | 1.3 | 3 | ns |
| $t_f$ | Output signal fall time | | | 1.3 | 3 | ns |
| $t_{PHZ}$ | Disable propagation delay, high-to-high impedance output | See Figure 7-2 | | 17 | 31 | ns |
| $t_{PLZ}$ | Disable propagation delay, low-to-high impedance output | | | 17 | 30 | ns |
| $t_{PZH}$ | Enable propagation delay, high impedance-to-high output for ISO774x | | | 17 | 30 | ns |
| | Enable propagation delay, high impedance-to-high output for ISO774x with F suffix | | | 3.2 | 8.5 | µs |
| $t_{PZL}$ | Enable propagation delay, high impedance-to-low output for ISO774x | | | 3.2 | 8.5 | µs |
| | Enable propagation delay, high impedance-to-low output for ISO774x with F suffix | | | 17 | 30 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7V. See Figure 7-4 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 100 Mbps | | 0.9 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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## 6.17 Switching Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 7-1 | 7.5 | 13 | 21 | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | 0.2 | 5.9 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same-direction channels | | | 4.4 | ns |
| $t_{sk(pp)}$ | Part-to-part skew time(3) | | | | 5.3 | ns |
| $t_r$ | Output signal rise time | See Figure 7-1 | | 1 | 3.5 | ns |
| $t_f$ | Output signal fall time | | | 1 | 3.5 | ns |
| $t_{PHZ}$ | Disable propagation delay, high-to-high impedance output | See Figure 7-2 | | 22 | 41 | ns |
| $t_{PLZ}$ | Disable propagation delay, low-to-high impedance output | | | 22 | 40 | ns |
| $t_{PZH}$ | Enable propagation delay, high impedance-to-high output for ISO774x | | | 18 | 40 | ns |
| | Enable propagation delay, high impedance-to-high output for ISO774x with F suffix | | | 3.3 | 8.5 | µs |
| $t_{PZL}$ | Enable propagation delay, high impedance-to-low output for ISO774x | | | 3.3 | 8.5 | µs |
| | Enable propagation delay, high impedance-to-low output for ISO774x with F suffix | | | 18 | 40 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.7V. See Figure 7-4 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 100 Mbps | | 0.7 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.


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## 6.18 Insulation Characteristics Curves

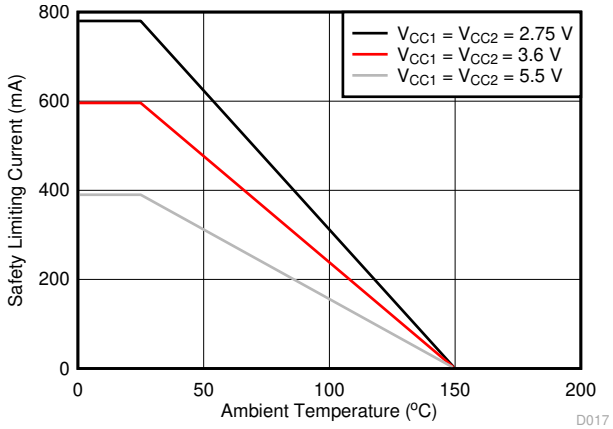



**Figure 6-1. Thermal Derating Curve for Safety Limiting Current for DWW-16 Package**

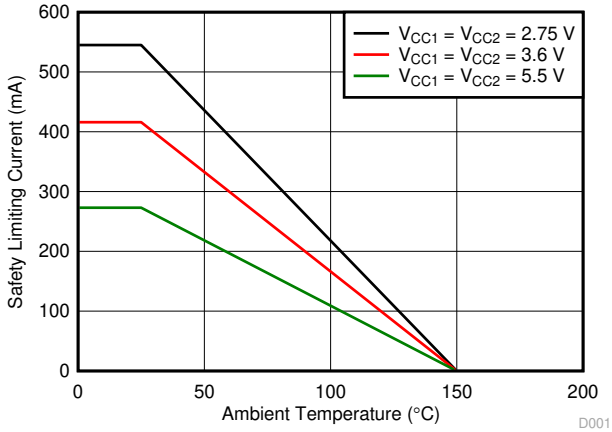



**Figure 6-2. Thermal Derating Curve for Safety Limiting Current for DW-16 Package**

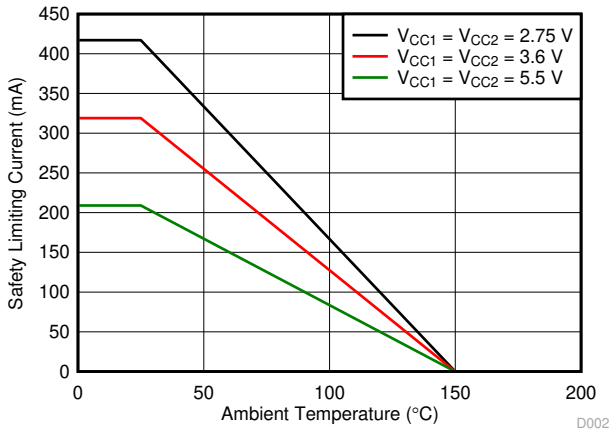



**Figure 6-3. Thermal Derating Curve for Safety Limiting Current for DBQ-16 Package**

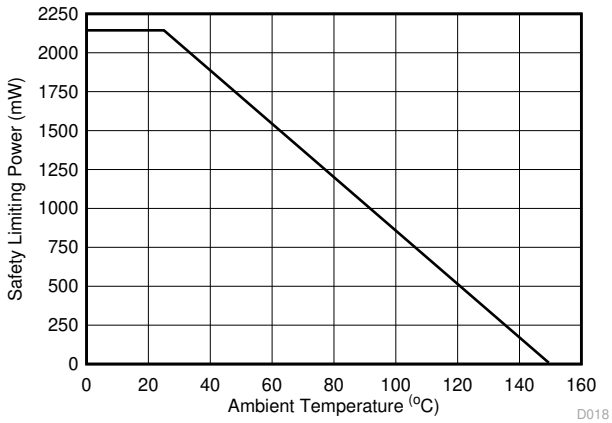



**Figure 6-4. Thermal Derating Curve for Safety Limiting Power for DWW-16 Package**

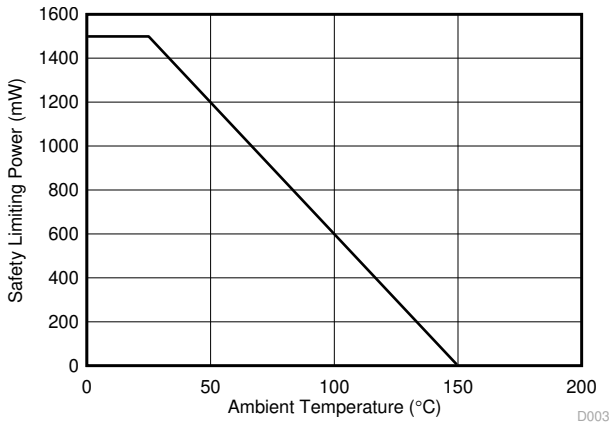



**Figure 6-5. Thermal Derating Curve for Safety Limiting Power for DW-16 Package**

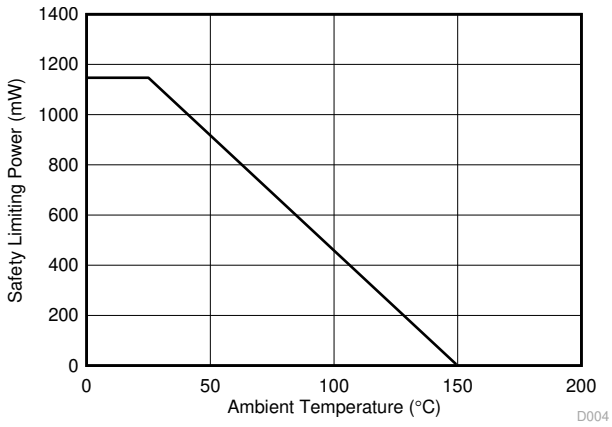



**Figure 6-6. Thermal Derating Curve for Safety Limiting Power for DBQ-16 Package**

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## 6.19 Typical Characteristics

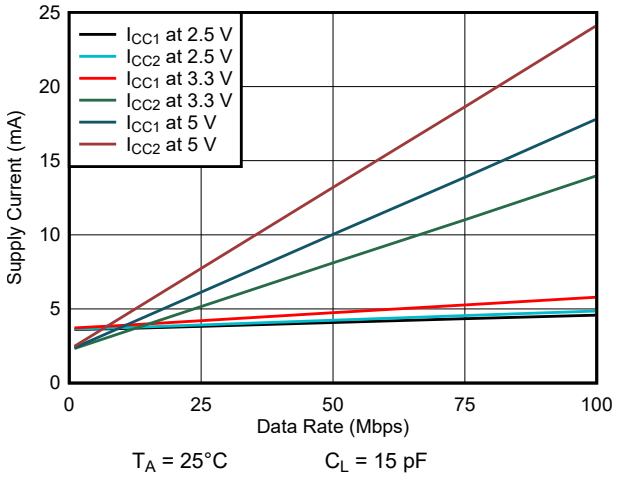



**Figure 6-7. ISO7740-Q1 Supply Current vs Data Rate (With 15-pF Load)**

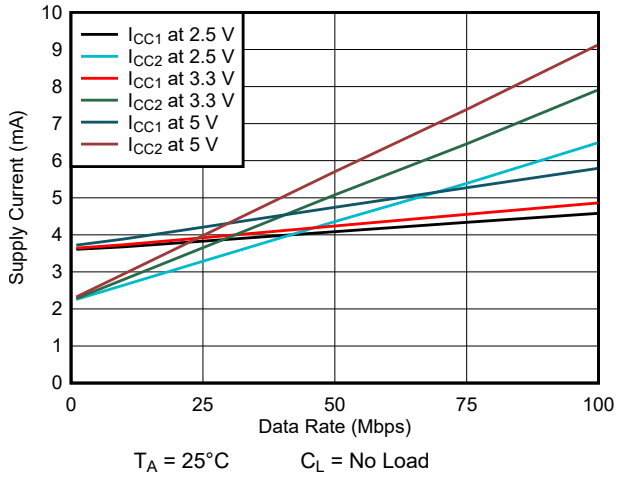



**Figure 6-8. ISO7740-Q1 Supply Current vs Data Rate (With No Load)**

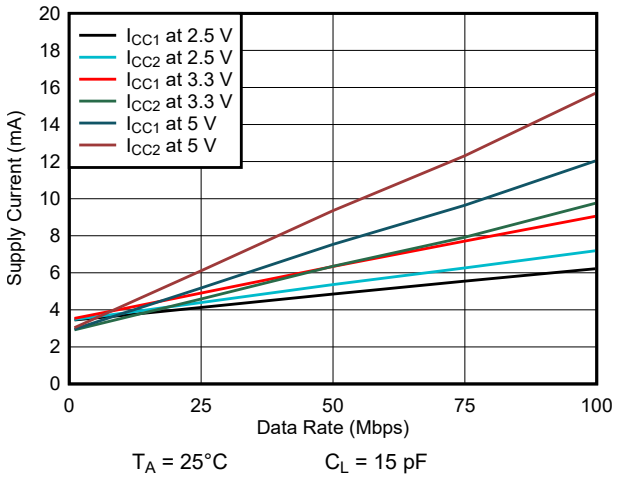



**Figure 6-9. ISO7741-Q1 Supply Current vs Data Rate (With 15-pF Load)**

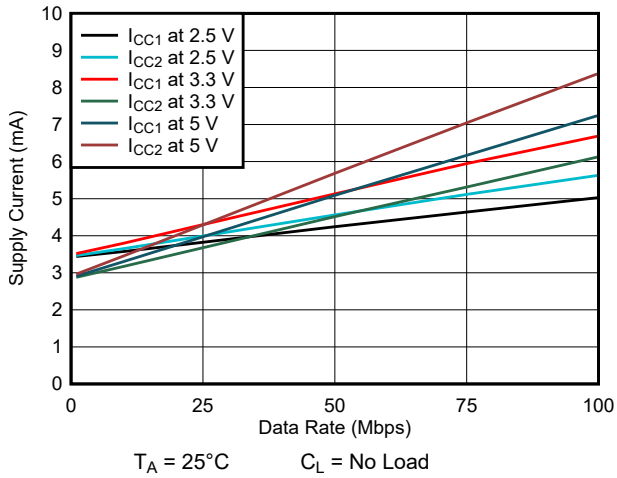



**Figure 6-10. ISO7741-Q1 Supply Current vs Data Rate (With No Load)**

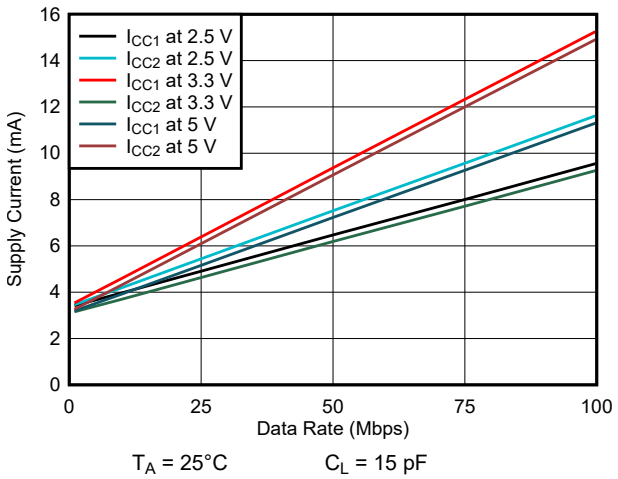



**Figure 6-11. ISO7742-Q1 Supply Current vs Data Rate (With 15-pF Load)**

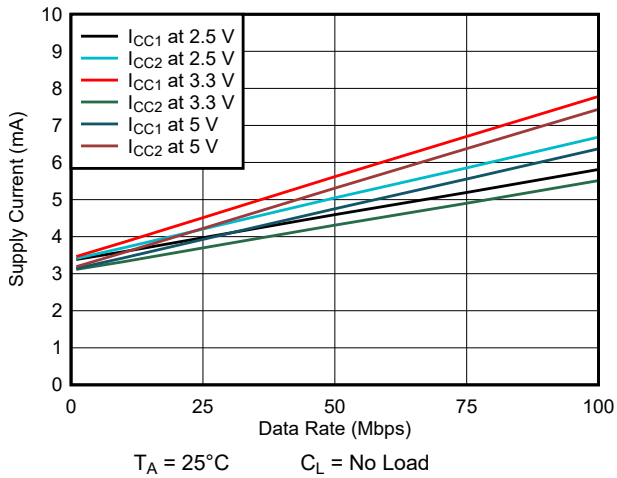
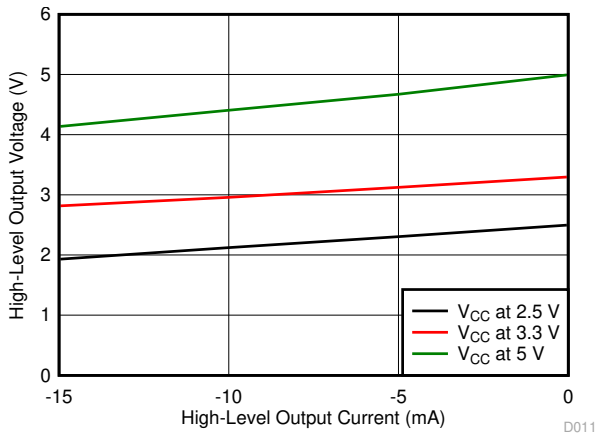


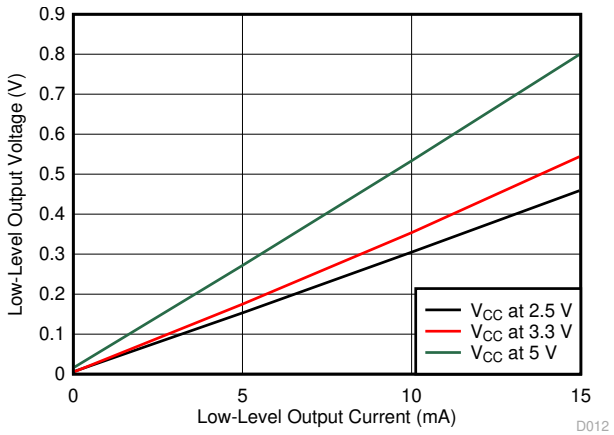

**Figure 6-12. ISO7742-Q1 Supply Current vs Data Rate (With No Load)**


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$T_A$ = 25°C

**Figure 6-13. High-Level Output Voltage vs High-level Output Current**




$T_A$ = 25°C

**Figure 6-14. Low-Level Output Voltage vs Low-Level Output Current**

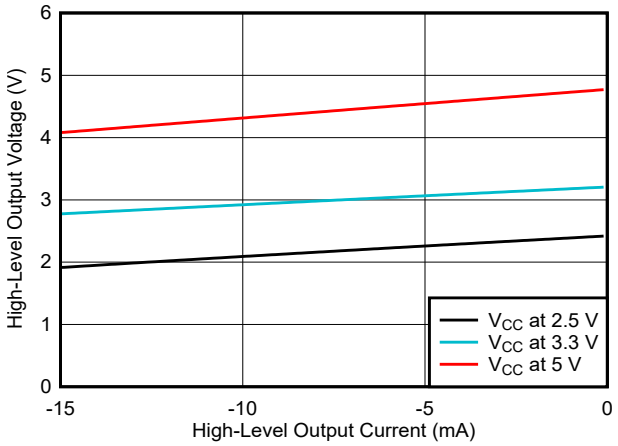



**Figure 6-15. Power Supply Undervoltage Threshold vs Free-Air Temperature**

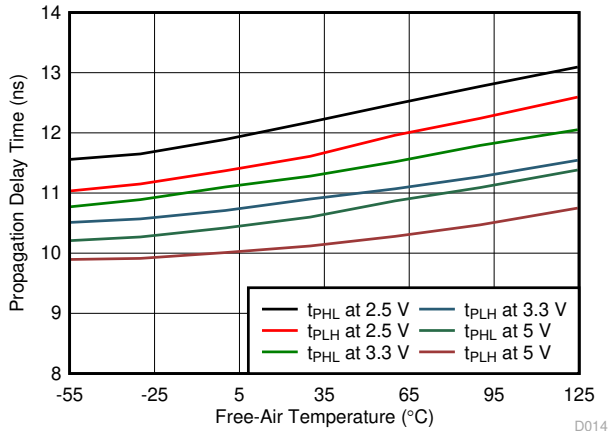
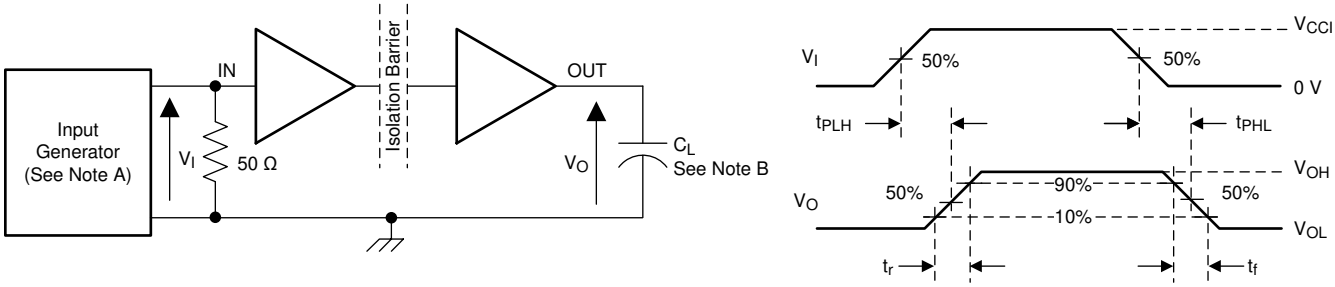



**Figure 6-16. Propagation Delay Time vs Free-Air Temperature**

# 7 Parameter Measurement Information

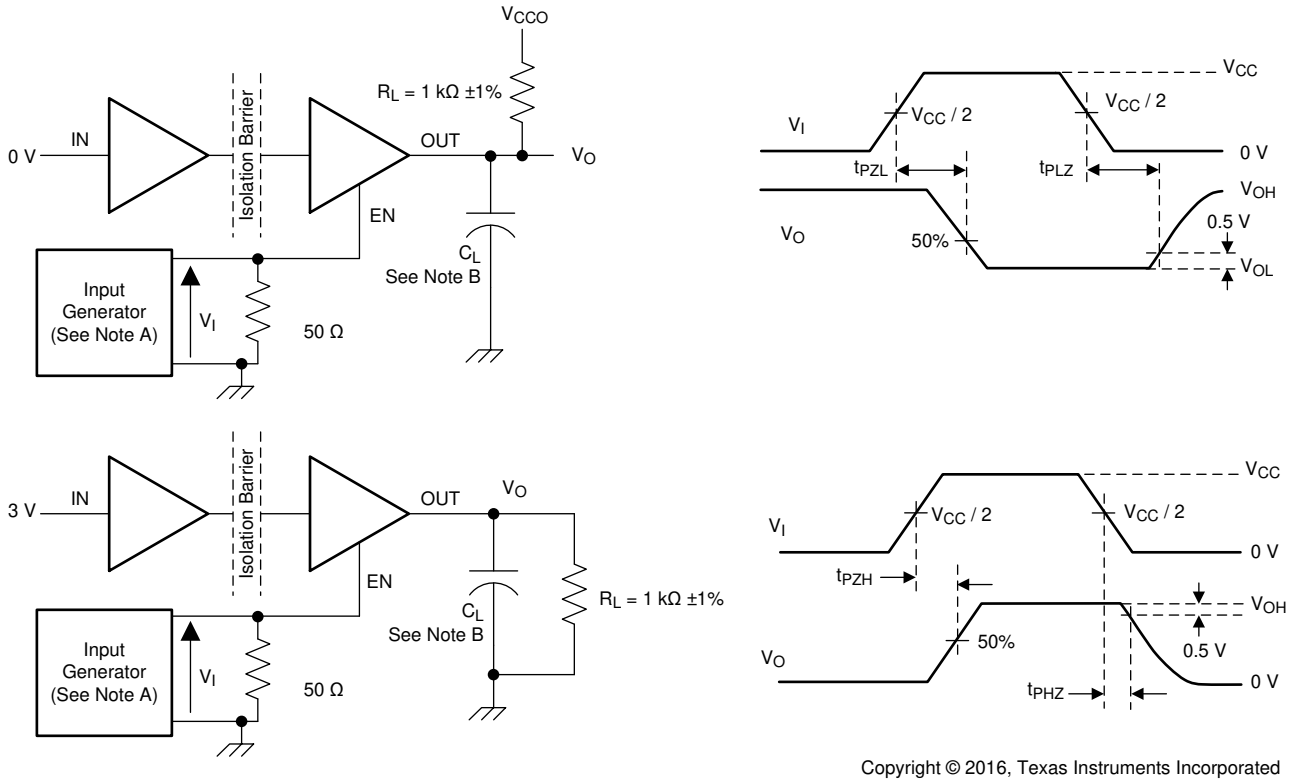



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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3ns, $Z_O$ = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms**



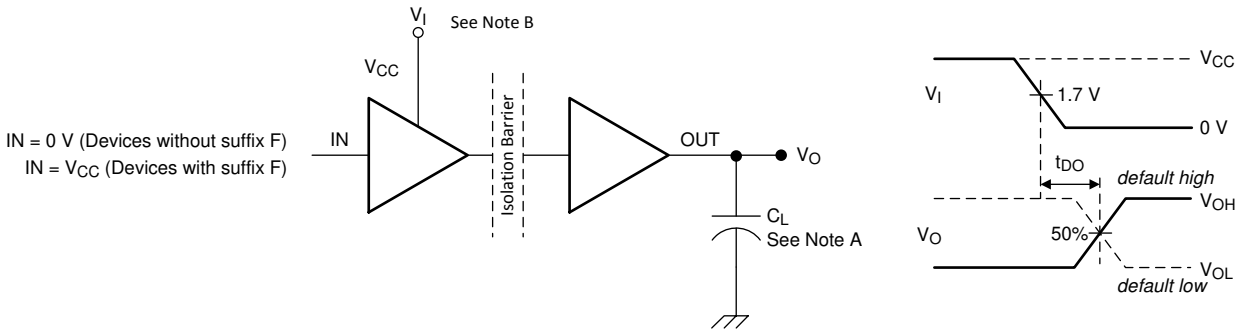

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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50 Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

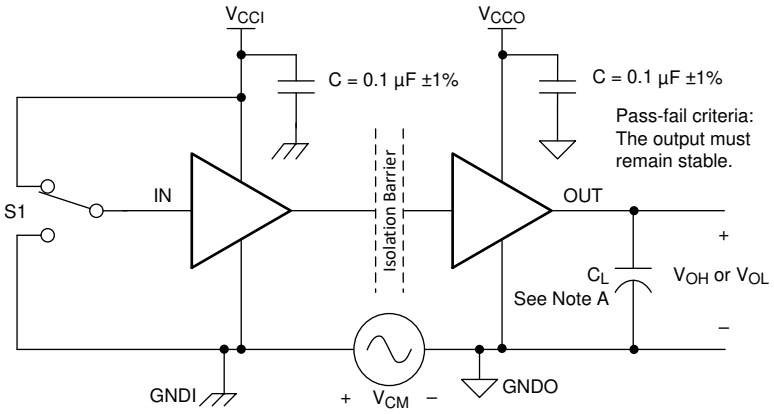
**Figure 7-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform**


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A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. Power Supply Ramp Rate = 10 mV/ns

**Figure 7-3. Default Output Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

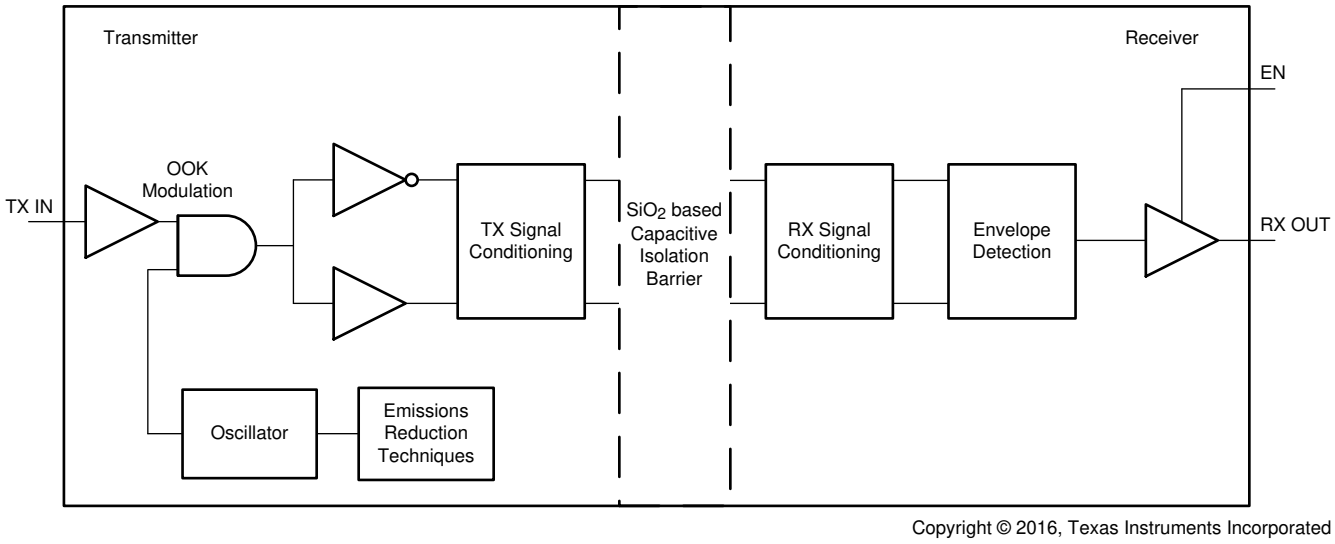
**Figure 7-4. Common-Mode Transient Immunity Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The ISO774x-Q1 family of devices an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO774x-Q1 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 8-1, shows a functional block diagram of a typical channel.

## 8.2 Functional Block Diagram




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**Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

Figure 8-2 shows a conceptual detail of how the ON-OFF keying scheme works.

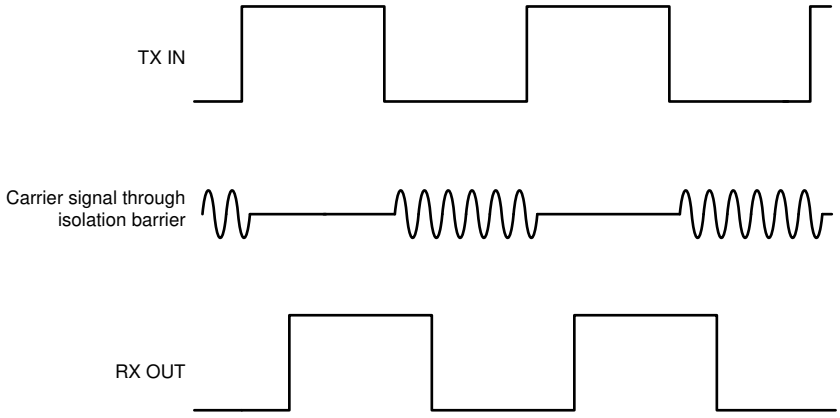



**Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme**


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## 8.3 Feature Description

Table 8-1 provides an overview of the device features.

**Table 8-1. Device Features**

| PART NUMBER | CHANNEL DIRECTION | MAXIMUM DATA RATE | DEFAULT OUTPUT | PACKAGE | RATED ISOLATION(1) |
|---|---|---|---|---|---|
| ISO7740-Q1 | 4 Forward, 0 Reverse | 100 Mbps | High | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7740-Q1 with F suffix | 4 Forward, 0 Reverse | 100 Mbps | Low | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7741-Q1 | 3 Forward, 1 Reverse | 100 Mbps | High | DWW-16 | 5700 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7741-Q1 with F suffix | 3 Forward, 1 Reverse | 100 Mbps | Low | DWW-16 | 5700 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7742-Q1 | 2 Forward, 2 Reverse | 100 Mbps | High | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7742-Q1 with F suffix | 2 Forward, 2 Reverse | 100 Mbps | Low | DW-16 | 5000 $V_{RMS}$ / 8000 $V_{PK}$ |
| | | | | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |

(1) See Section 6.7 for detailed isolation ratings.

### 8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO774x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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## 8.4 Device Functional Modes

Table 8-2 lists the functional modes for the ISO774x-Q1 devices.

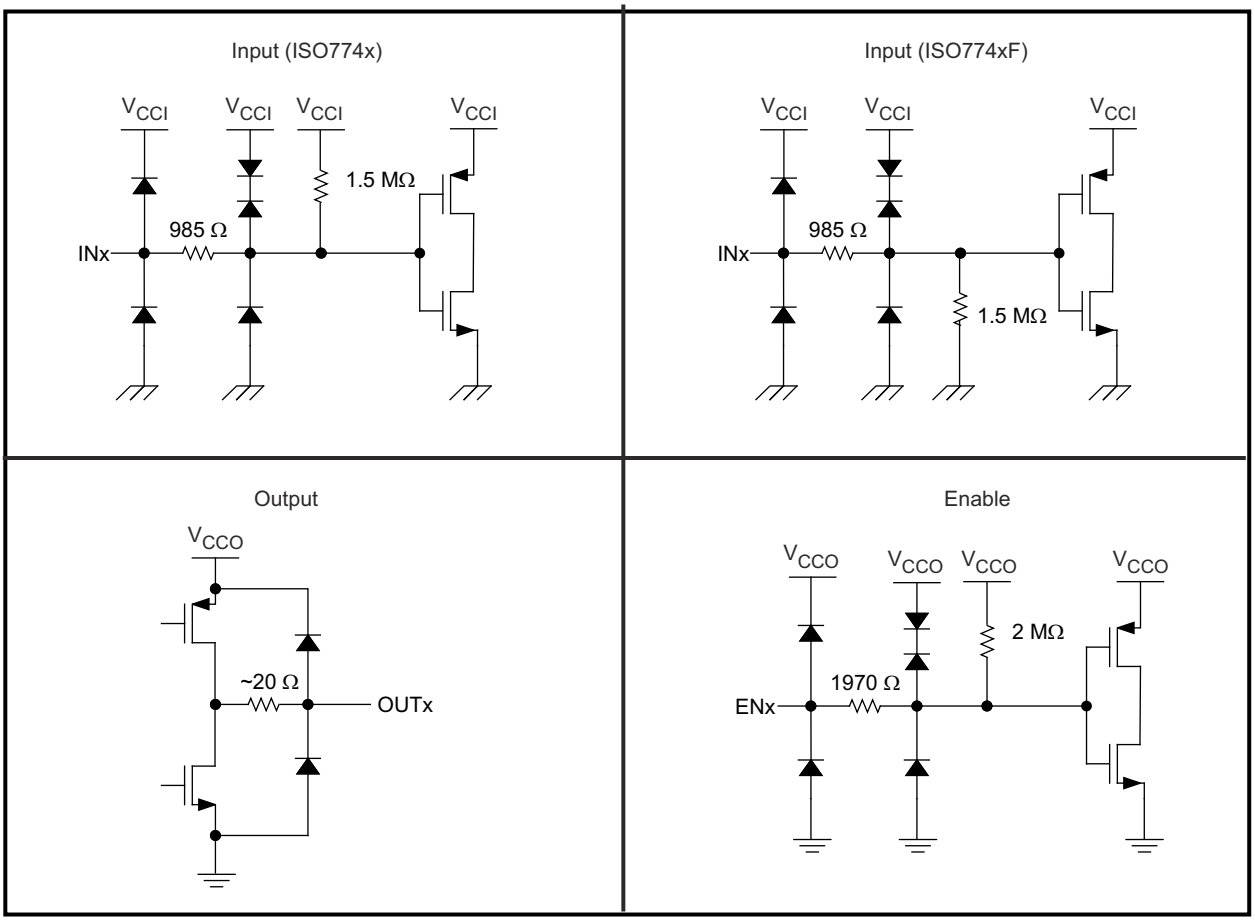
**Table 8-2. Function Table**

| $V_{CCI}$ (1) | $V_{CCO}$ | INPUT (INx)(3) | OUTPUT ENABLE (ENx) | OUTPUT (OUTx) | COMMENTS |
|---|---|---|---|---|---|
| PU | PU | H | H or open | H | Normal Operation:<br>A channel output assumes the logic state of its input. |
| | | L | H or open | L | |
| | | Open | H or open | Default | Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO774x-Q1 and *Low* for ISO774x-Q1 with F suffix. |
| X | PU | X | L | Z | A low value of output enable causes the outputs to be high-impedance. |
| PD | PU | X | H or open | Default | Default mode: When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO774x-Q1 and *Low* for ISO774x-Q1 with F suffix.<br>When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.<br>When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| X | PD | X | X | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined(2).<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$; PU = Powered up ($V_{CC}$ ≥ 2.25 V); PD = Powered down ($V_{CC}$ ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) The outputs are in undetermined state when 1.7 V < $V_{CCI}$, $V_{CCO}$ < 2.25 V.
(3) A strongly driven input signal can weakly power the floating $V_{CC}$ through an internal protection diode and cause undetermined output.


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### 8.4.1 Device I/O Schematics




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**Figure 8-3. Device I/O Schematics**

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ISO774x-Q1 devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption. The ISO774x-Q1 devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, $V_{CC1}$ and $V_{CC2}$. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

## 9.2 Typical Application

Figure 9-1 shows the typical isolated CAN interface implementation.

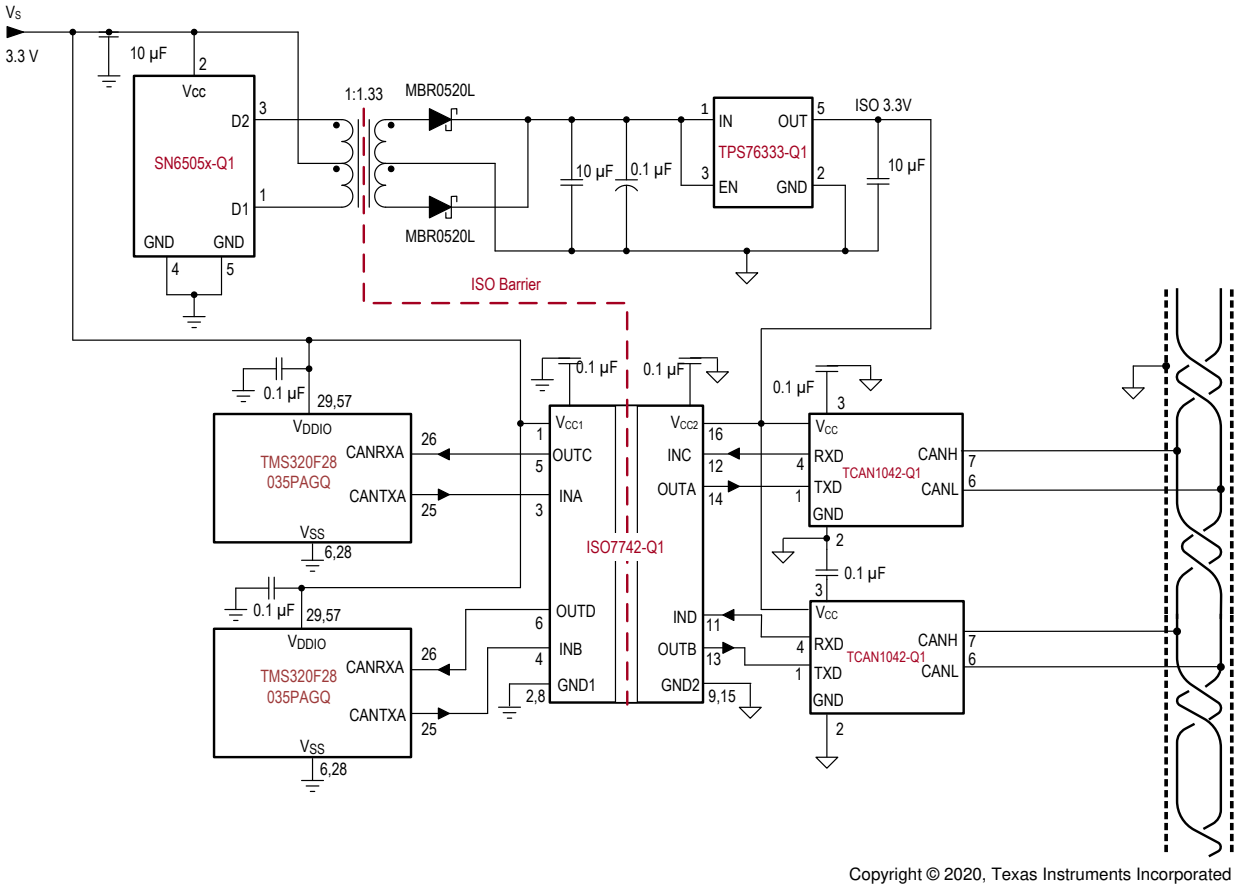



**Figure 9-1. Typical Isolated CAN Application Circuit**


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### 9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 9-1.

**Table 9-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage, $V_{CC1}$ and $V_{CC2}$ | 2.25 to 5.5 V |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1 µF |
| Decoupling capacitor from $V_{CC2}$ and GND2 | 0.1 µF |

### 9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO774x-Q1 family of devices only require two external bypass capacitors to operate.

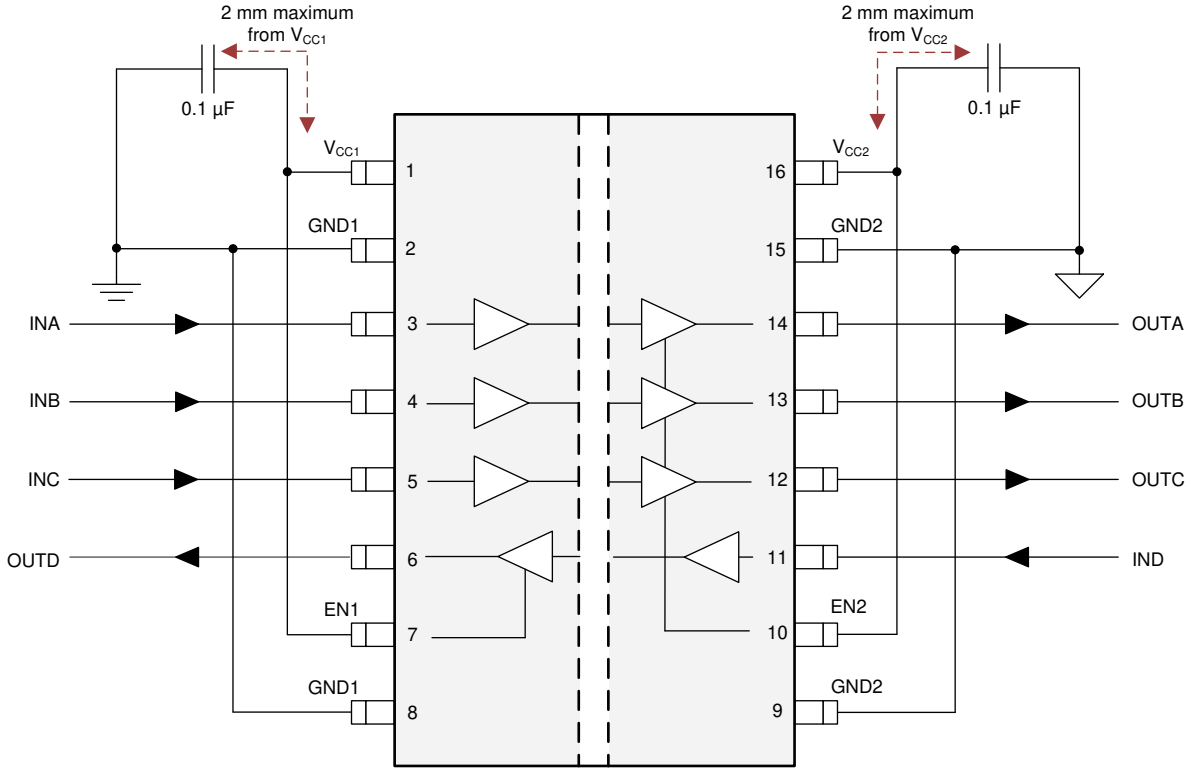



**Figure 9-2. Typical ISO774x-Q1 Circuit Hook-up**

The DWW package provides wider creepage and clearance without the need for two isolators in series or an extra isolated power supply, saving design cost and board space. For more details, please refer to the technical document *How to Meet the Higher Isolation Creepage & Clearance Needs in Automotive Applications*.

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### 9.2.3 Application Curve

The following typical eye diagrams of the ISO774x-Q1 family of devices indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

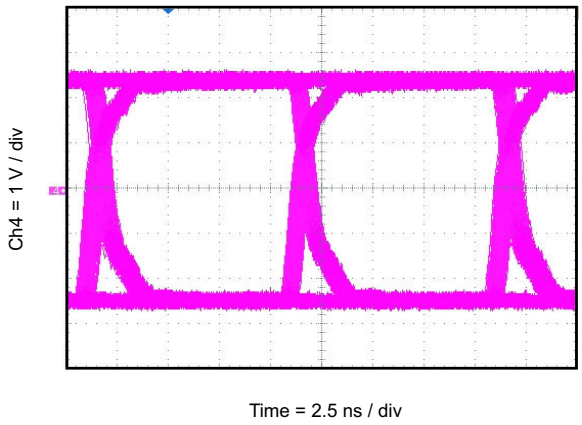



**Figure 9-3. Eye Diagram at 100 Mbps PRBS $2^{16}$ – 1, 5 V and 25°C**

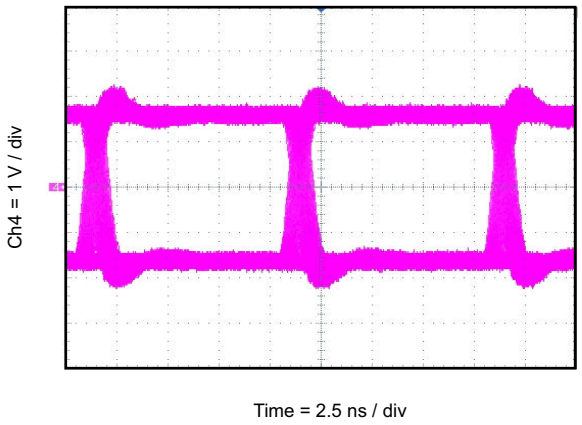



**Figure 9-4. Eye Diagram at 100 Mbps PRBS $2^{16}$ – 1, 3.3 V and 25°C**

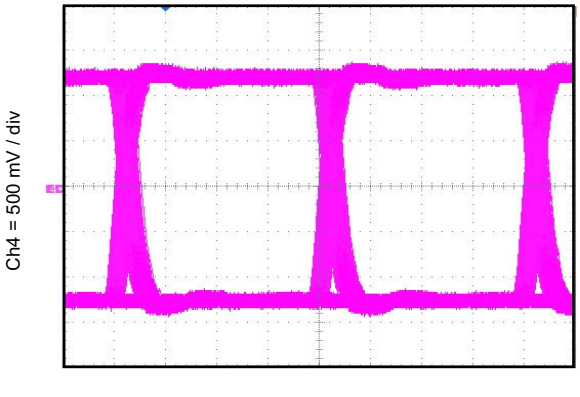



**Figure 9-5. Eye Diagram at 100 Mbps PRBS $2^{16}$ – 1, 2.5 V and 25°C**

#### *9.2.3.1 Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 9-6 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 9-7 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 $V_{RMS}$ with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 $V_{RMS}$. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years. The insulation withstand capability of DWW-16 package is 2000 $V_{RMS}$ with a corresponding lifetime of 34 years. DBQ-16 package at 400 $V_{RMS}$ working voltage has a much longer lifetime than both DW-16 and DWW-16 packages.


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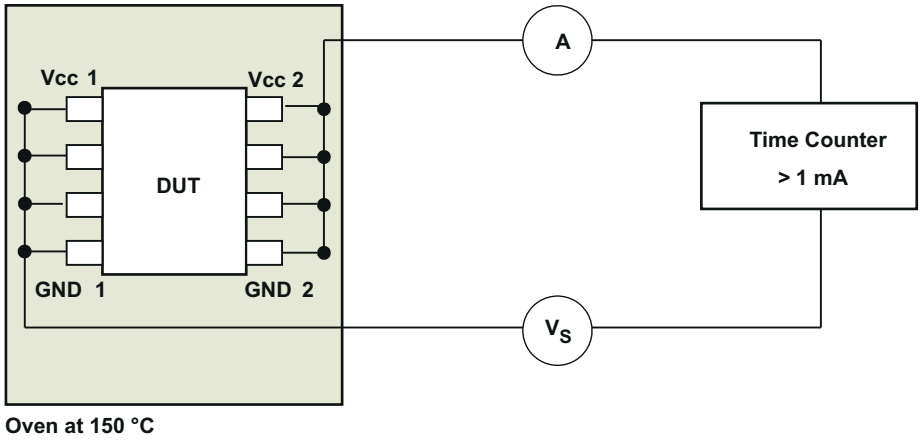



**Figure 9-6. Test Setup for Insulation Lifetime Measurement**

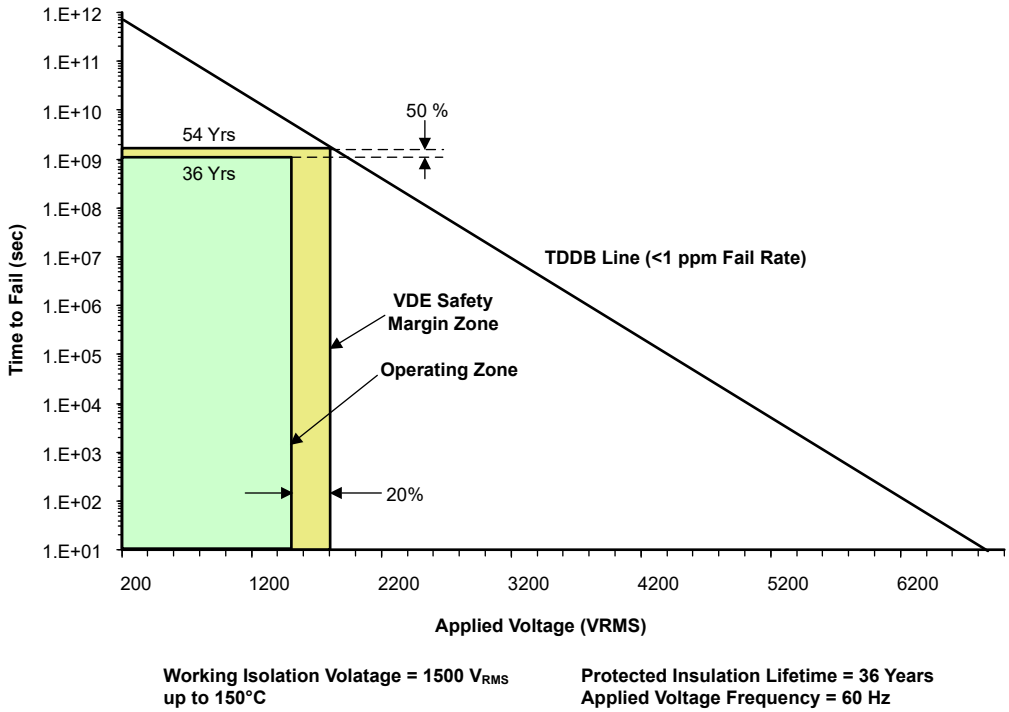



**Figure 9-7. Insulation Lifetime Projection Data**

## 10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins ($V_{CC1}$ and $V_{CC2}$). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1 or SN6505B-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* and *SN6505x-Q1 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheets.

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# 11 Layout

## 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

### 11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

## 11.2 Layout Example

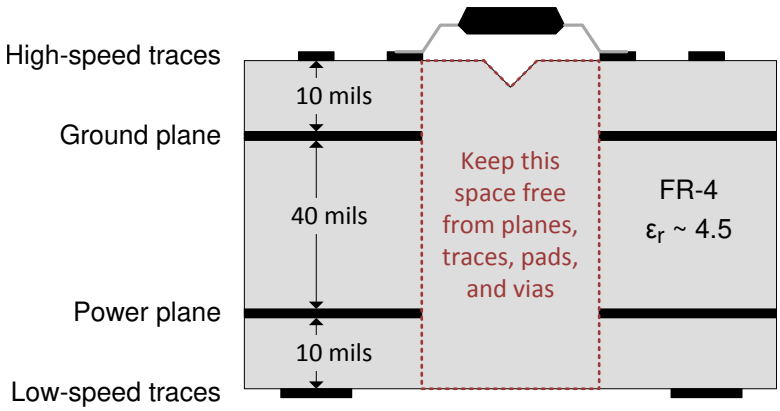



**Figure 11-1. Layout Example Schematic**


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems* application report
- Texas Instruments, SN6501-Q1 *Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, SN6505x-Q1 *Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, TCAN1042-Q1 *Automotive fault protected CAN transceiver with CAN FD* data sheet
- Texas Instruments, TMS320F28035 *Piccolo™ Microcontrollers* data sheet
- Texas Instruments, TPS76333-Q1 *Low-Power 150-mA Low-Dropout Linear Regulators* data sheet

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 12-1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| ISO7740-Q1 | Click here | Click here | Click here | Click here | Click here |
| ISO7741-Q1 | Click here | Click here | Click here | Click here | Click here |
| ISO7742-Q1 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.5 Trademarks

Piccolo™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7740FQDBQQ1 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7740FQ | Samples |
| ISO7740FQDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7740FQ | Samples |
| ISO7740FQDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7740FQ | Samples |
| ISO7740FQDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (ISO7740F, ISO7740 FQ) | Samples |
| ISO7740QDBQQ1 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7740Q | Samples |
| ISO7740QDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7740Q | Samples |
| ISO7740QDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7740Q | Samples |
| ISO7740QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (ISO7740, ISO7740Q ) | Samples |
| ISO7741FQDBQQ1 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7741FQ | Samples |
| ISO7741FQDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7741FQ | Samples |
| ISO7741FQDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7741FQ | Samples |
| ISO7741FQDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (ISO7741F, ISO7741 FQ) | Samples |
| ISO7741FQDWWQ1 | ACTIVE | SOIC | DWW | 16 | 45 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7741FQ | Samples |
| ISO7741FQDWWRQ1 | ACTIVE | SOIC | DWW | 16 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7741FQ | Samples |
| ISO7741QDBQQ1 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7741Q | Samples |
| ISO7741QDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7741Q | Samples |
| ISO7741QDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7741Q | Samples |
| ISO7741QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (ISO7741, ISO7741Q ) | Samples |
| ISO7741QDWWQ1 | ACTIVE | SOIC | DWW | 16 | 45 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7741Q | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7741QDWWRQ1 | ACTIVE | SOIC | DWW | 16 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7741Q | Samples |
| ISO7742FQDBQQ1 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7742FQ | Samples |
| ISO7742FQDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7742FQ | Samples |
| ISO7742FQDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7742FQ | Samples |
| ISO7742FQDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (ISO7742F, ISO7742 FQ) | Samples |
| ISO7742QDBQQ1 | ACTIVE | SSOP | DBQ | 16 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7742Q | Samples |
| ISO7742QDBQRQ1 | ACTIVE | SSOP | DBQ | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7742Q | Samples |
| ISO7742QDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7742Q | Samples |
| ISO7742QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | (ISO7742, ISO7742Q ) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISO7740-Q1, ISO7741-Q1, ISO7742-Q1 :**

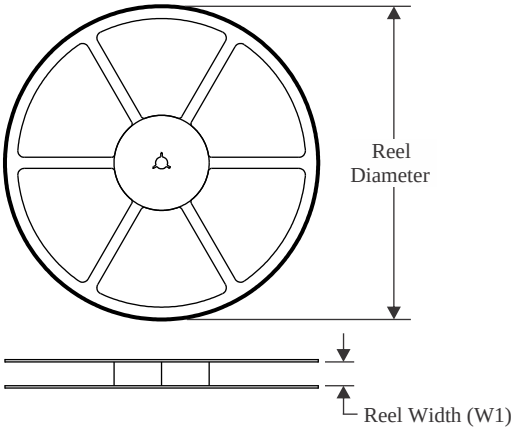
- Catalog : ISO7740, ISO7741, ISO7742

NOTE: Qualified Version Definitions:

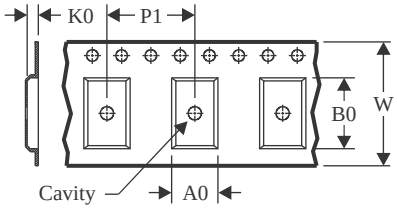
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

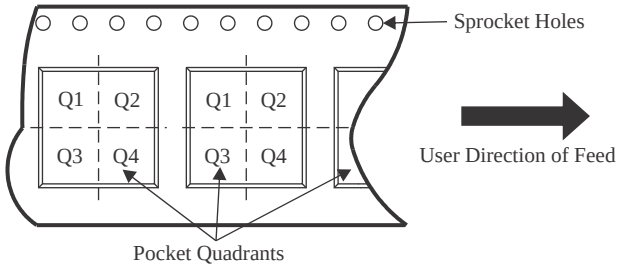



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

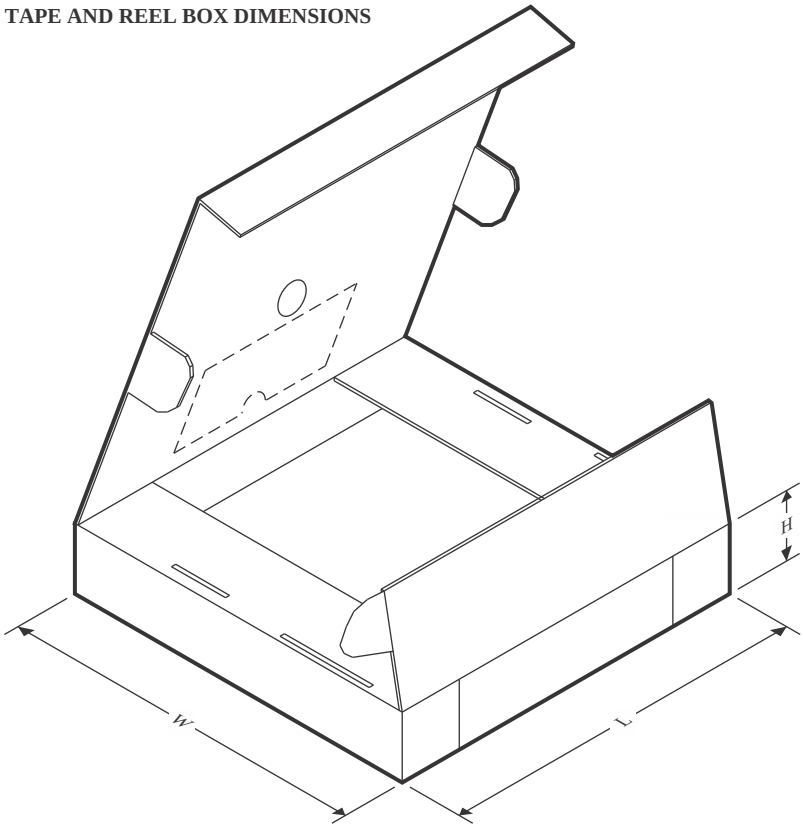



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7740FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7740FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7740FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7740FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7740FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7740QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7740QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7740QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7740QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7740QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7741FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741FQDWWRQ1 | SOIC | DWW | 16 | 1000 | 330.0 | 24.4 | 18.0 | 10.0 | 3.0 | 20.0 | 24.0 | Q1 |
| ISO7741QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7741QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7741QDWWRQ1 | SOIC | DWW | 16 | 1000 | 330.0 | 24.4 | 18.0 | 10.0 | 3.0 | 20.0 | 24.0 | Q1 |
| ISO7742FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7742FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7742FQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7742QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7742QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7742QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7742QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7742QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

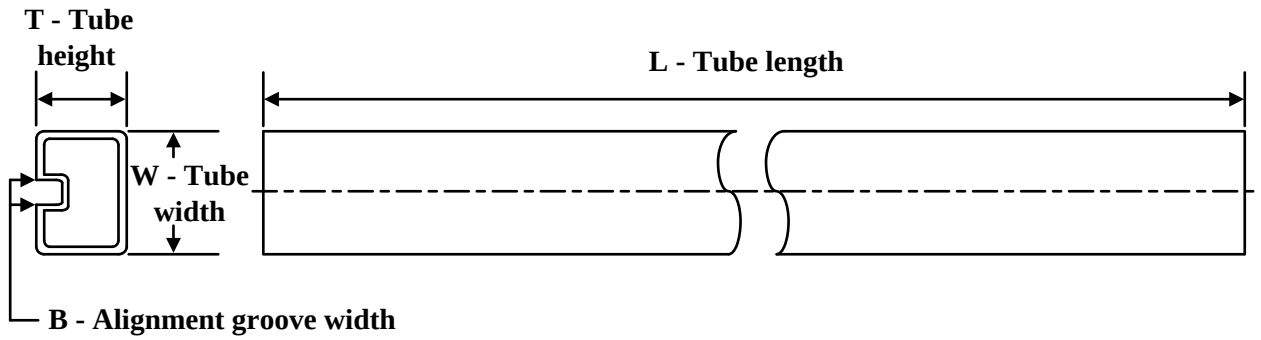



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7740FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7740FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7740FQDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7740FQDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7740FQDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 45.0 |
| ISO7740QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7740QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7740QDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7740QDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7740QDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 45.0 |
| ISO7741FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7741FQDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 45.0 |
| ISO7741FQDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7741FQDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7741FQDWWRQ1 | SOIC | DWW | 16 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO7741QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7741QDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7741QDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 45.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7741QDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7741QDWWRQ1 | SOIC | DWW | 16 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO7742FQDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7742FQDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| ISO7742FQDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 45.0 |
| ISO7742QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7742QDBQRQ1 | SSOP | DBQ | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| ISO7742QDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7742QDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 45.0 |
| ISO7742QDWRQ1 | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

## TUBE




*All dimensions are nominal

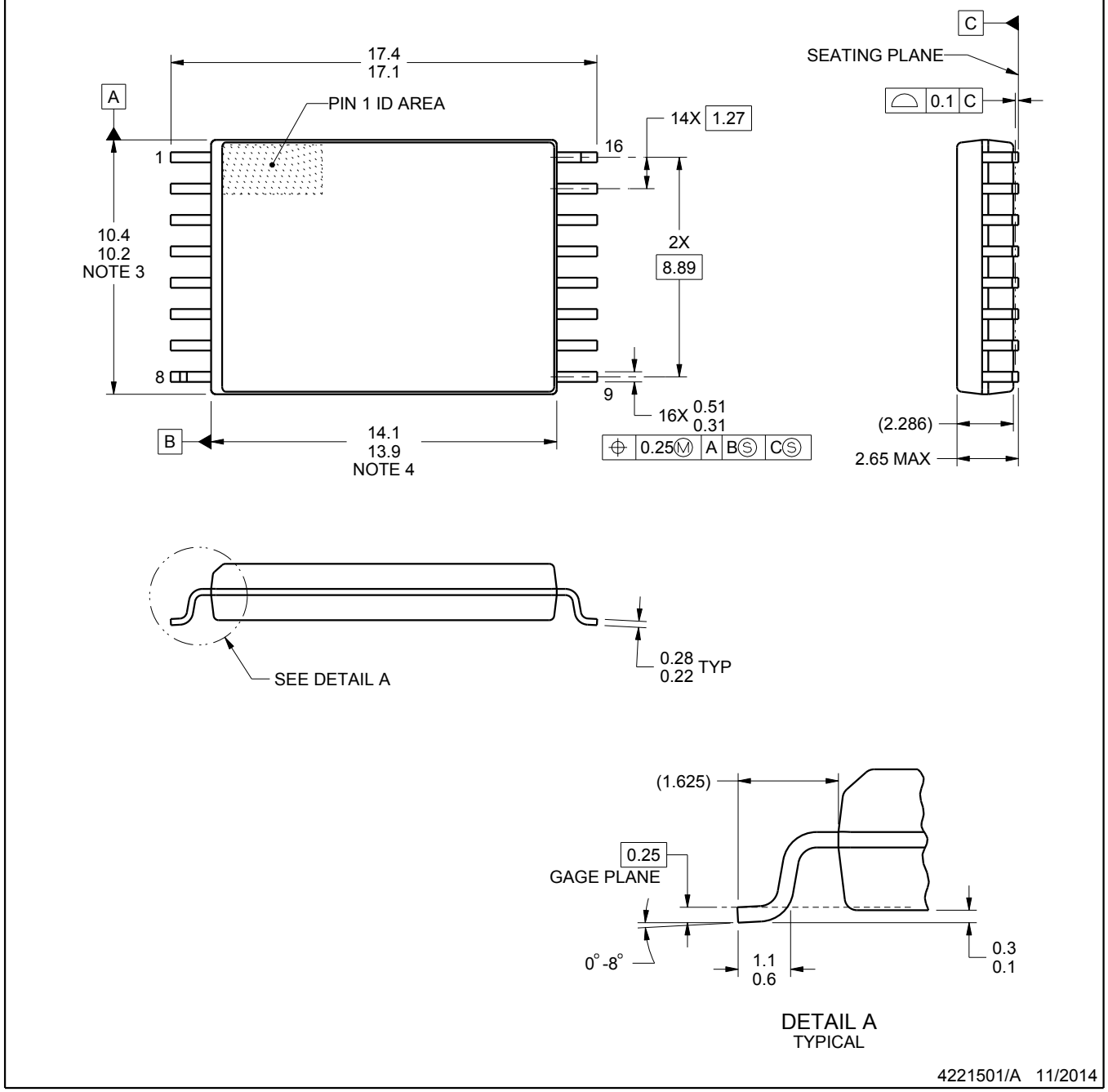
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| ISO7740FQDBQQ1 | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7740FQDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7740FQDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7740QDBQQ1 | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7740QDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7740QDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7741FQDBQQ1 | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7741FQDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7741FQDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7741FQDWWQ1 | DWW | SOIC | 16 | 45 | 507 | 20 | 5000 | 9 |
| ISO7741QDBQQ1 | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7741QDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7741QDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7741QDWWQ1 | DWW | SOIC | 16 | 45 | 507 | 20 | 5000 | 9 |
| ISO7742FQDBQQ1 | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7742FQDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7742FQDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| ISO7742QDBQQ1 | DBQ | SSOP | 16 | 75 | 505.46 | 6.76 | 3810 | 4 |
| ISO7742QDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| ISO7742QDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |

# PACKAGE OUTLINE

## DWW0016A

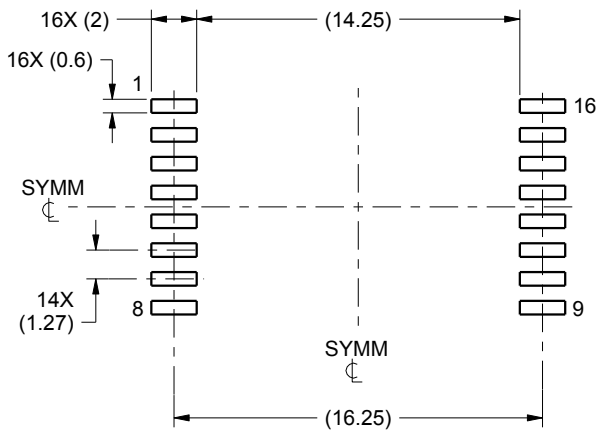
## SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

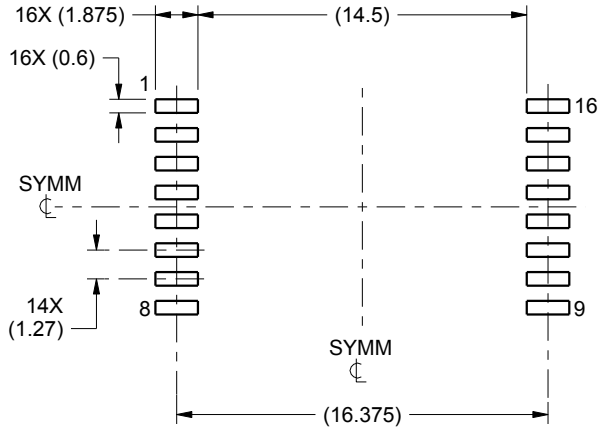



NOTES:

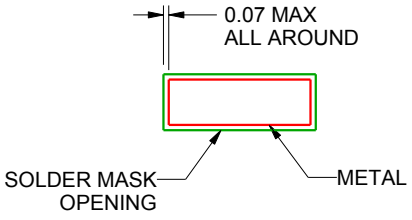
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.



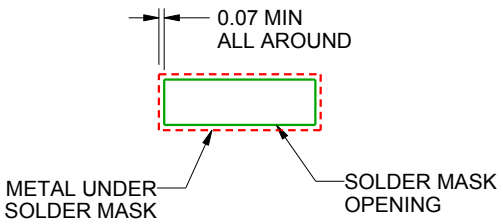

LAND PATTERN EXAMPLE
STANDARD
SCALE:3X




LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X




NON SOLDER MASK
DEFINED
(PREFERRED)



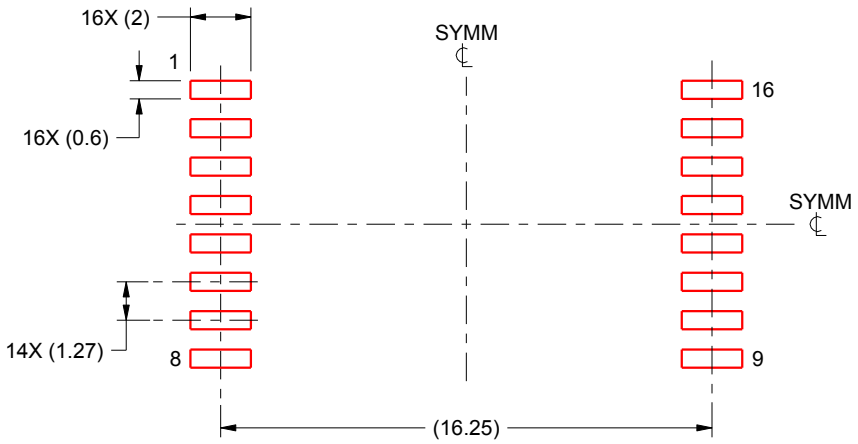

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

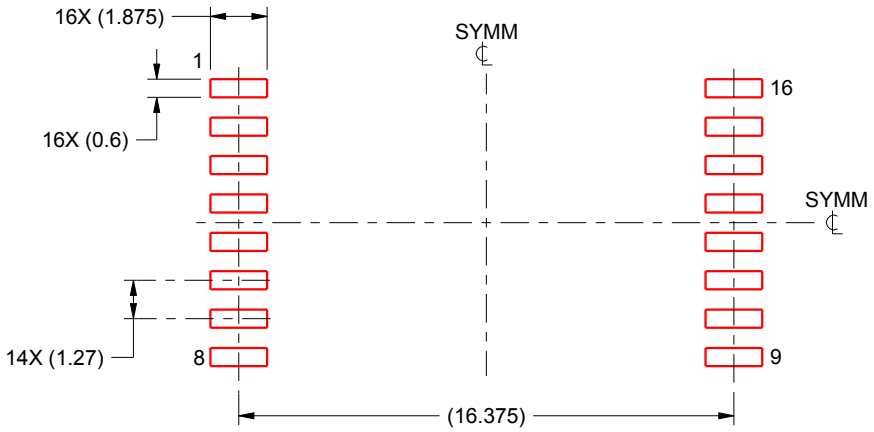
4221501/A 11/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X




SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221501/A 11/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

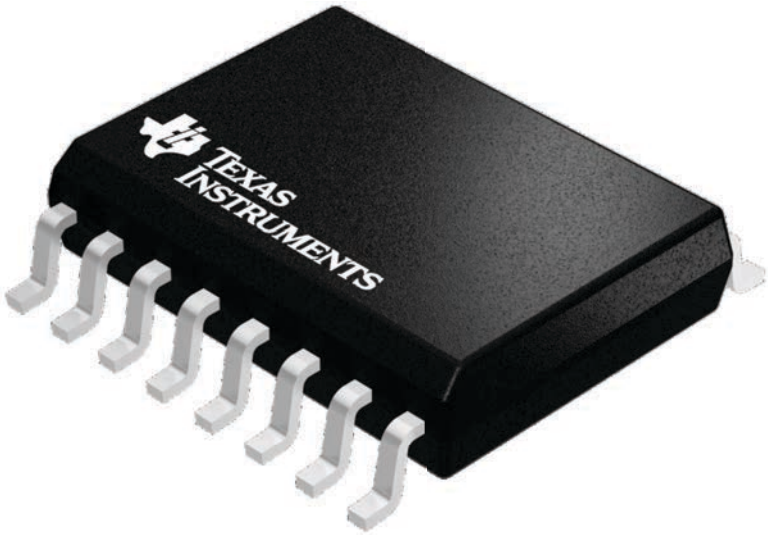
## DW 16

## SOIC - 2.65 mm max height

**7.5 x 10.3, 1.27 mm pitch**

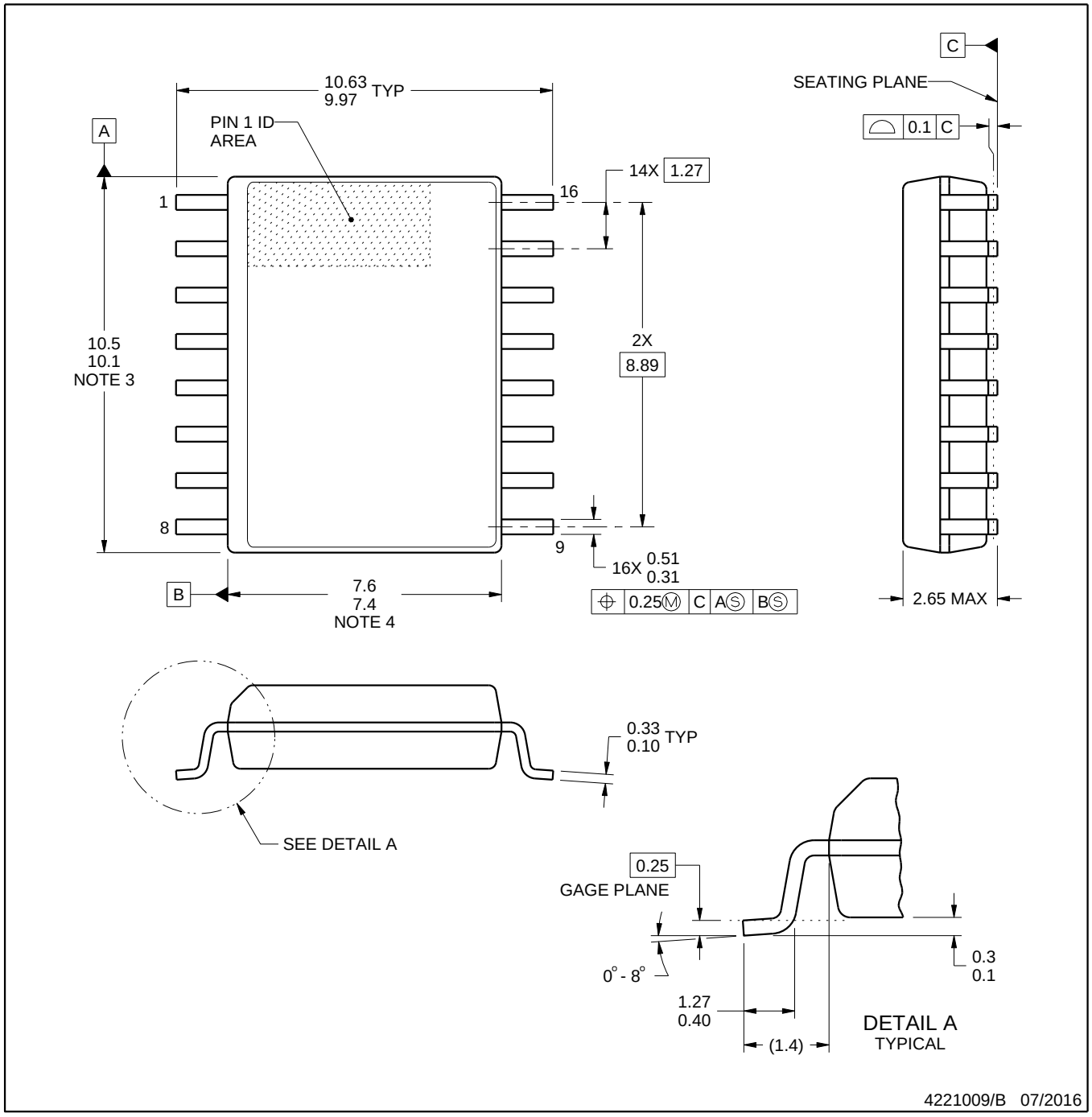
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



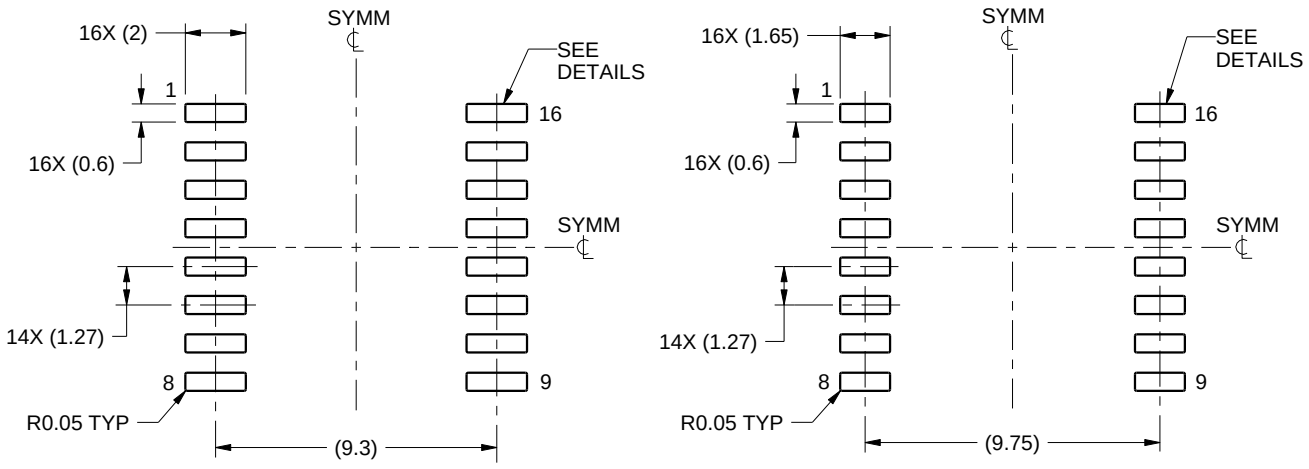

4224780/A

SOIC




NOTES:

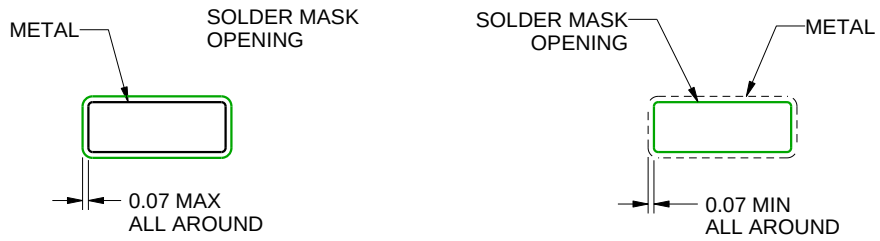
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

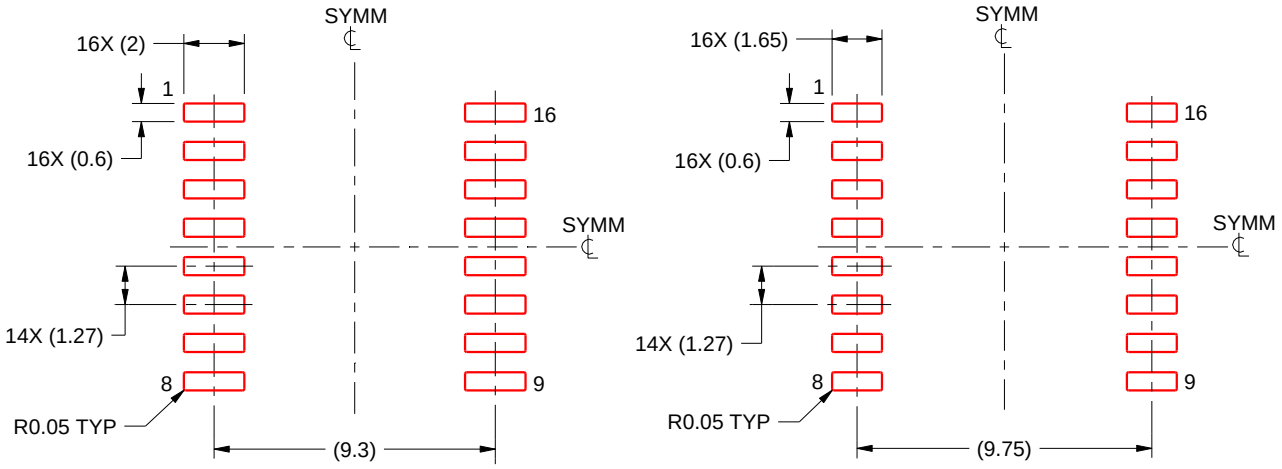
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

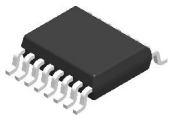
HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

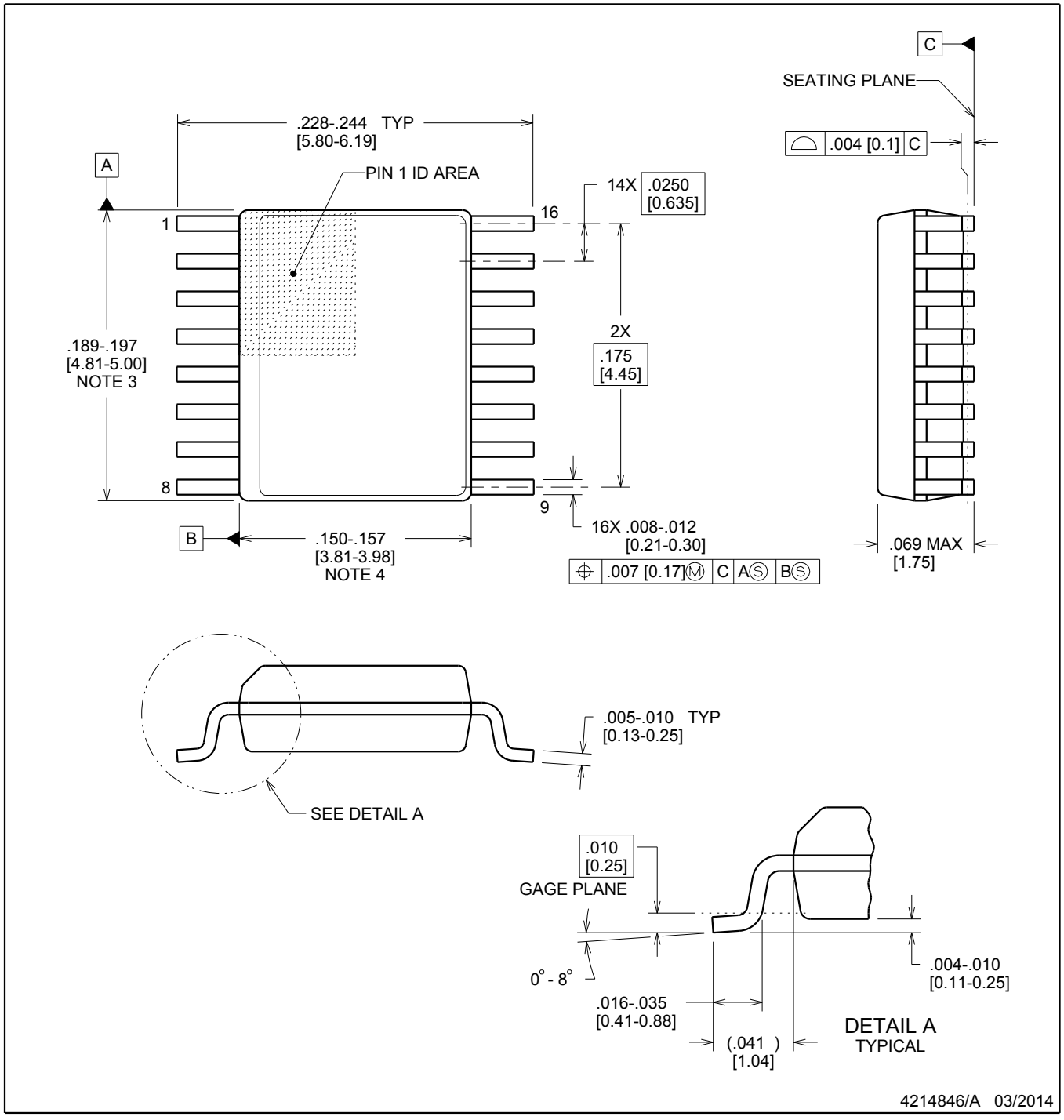


# PACKAGE OUTLINE

## DBQ0016A

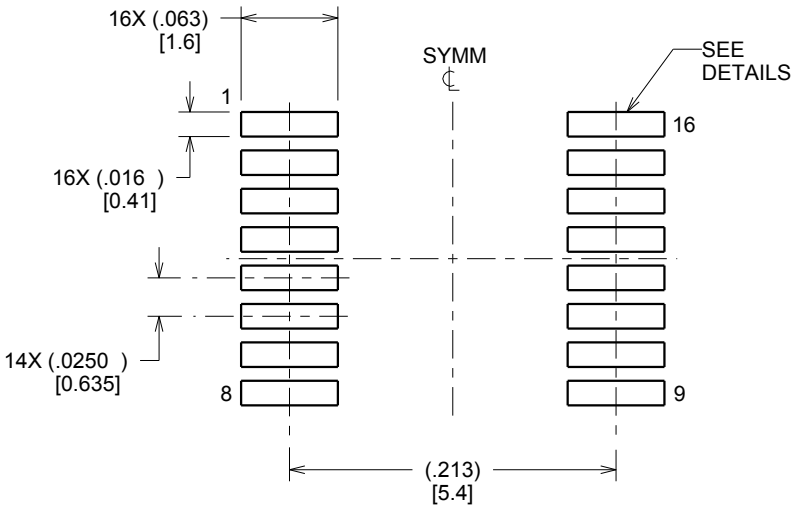
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

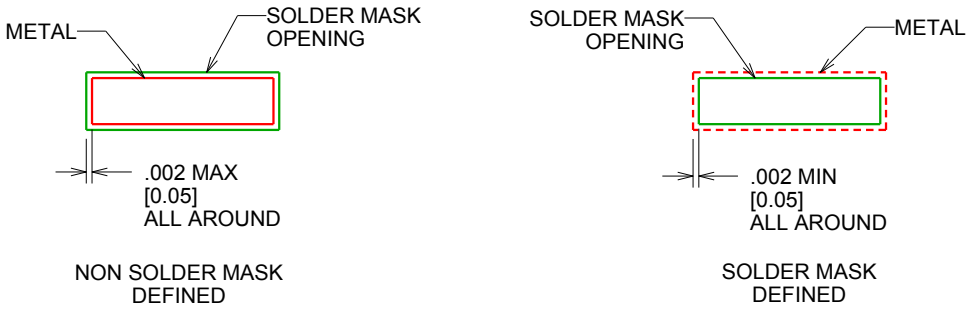



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

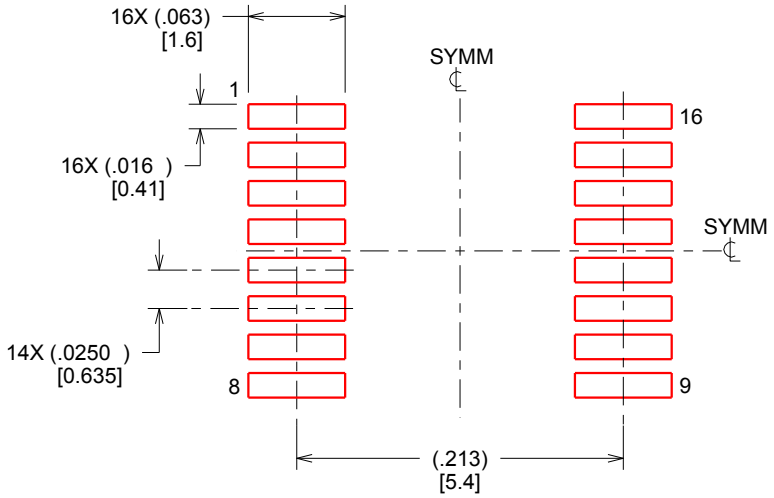
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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