TEXAS INSTRUMENTS

OPA333, OPA2333

SBOS351E – MARCH 2006 – REVISED DECEMBER 2015

OPAx333 1.8-V, *micro*Power, CMOS Operational Amplifiers, Zero-Drift Series

1 Features

- Low Offset Voltage: 10 µV (Maximum)
- Zero Drift: 0.05 µV/°C (Maximum)
- 0.01-Hz to 10-Hz Noise: 1.1 μV_{PP}
- Quiescent Current: 17 µA
- Single-Supply Operation
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- *micro*Size Packages: SC70 and SOT23

2 Applications

- Transducers
- Temperature Measurements
- Electronic Scales
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

3 Description

The OPAx333 series of CMOS operational amplifiers use a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 µV, maximum) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) can be used. These devices are optimized for low-voltage, single-supply operation.

The OPAx333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

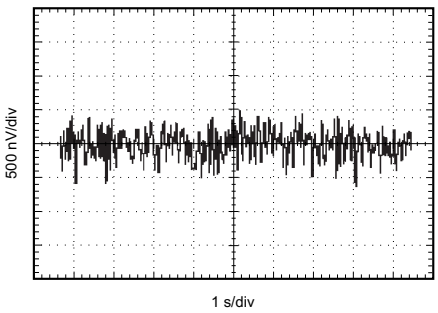
The OPA333 (single version) is available in the 5-pin SOT-23, SOT, and 8-pin SOIC packages, while the OPA2333 (dual version) is available in the 8-pin VSON, SOIC, and VSSOP packages. All versions are specified for operation from –40°C to 125°C.

Device Information(1)

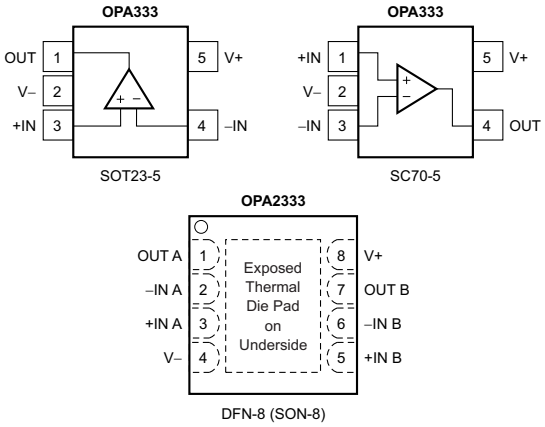
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA333	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT (5)	2.00 mm x 1.25 mm
	SOIC (8)	4.90 mm × 3.90 mm
OPA2333	VSON (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

0.1-Hz to 10-Hz Noise



OPAx333 Pinout Diagrams



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2013) to Revision E — **Page**

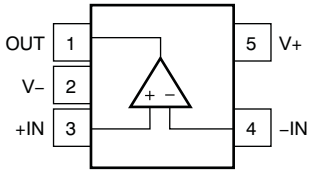
- Added *Pin Configuration and Functions* section, *ESD Ratings* and *Thermal Information* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (May 2007) to Revision D — **Page**

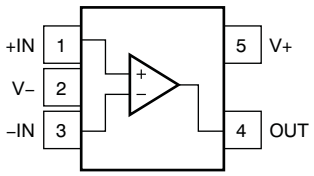
- Changed data sheet format to most current standard look and feel ... 1
- Added OPA2333 DFN-8 pinout to front page ... 1
- Changed 2nd *signal input terminals* parameter in the Absolute Maximum Ratings from "voltage" to "current" (typo) ... 5
- Added Table 1 ... 8

5 Pin Configuration and Functions

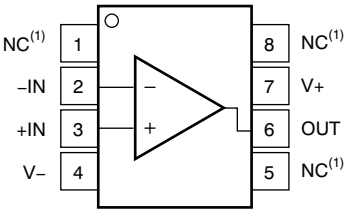
OPA333 DBV Package
5-Pin SOT
Top View



OPA333 DCK Package
5-Pin SC70
Top View



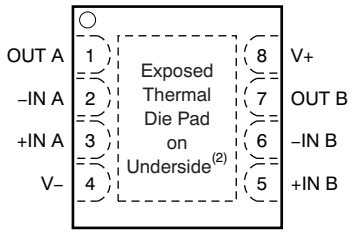
OPA333 D Package
8-Pin SOIC
Top View



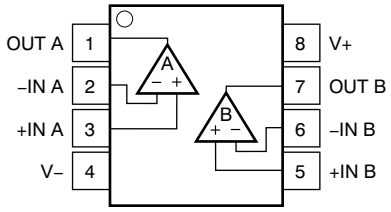
Pin Functions: OPA333

PIN				I/O	DESCRIPTION
NAME	SOIC	SOT	SC70		
+IN	3	3	1	I	Noninverting input
–IN	2	4	3	I	Inverting input
NC	1, 5, 8	—	—	—	No internal connection (can be left floating)
OUT	6	1	4	O	Output
V+	7	5	5	—	Positive (highest) power supply
V–	4	2	2	—	Negative (lowest) power supply

OPA2333 DRB Package
8-Pin VSON With Exposed Thermal Pad
Top View



OPA2333 D or DGK Package
8-Pin SOIC or VSSOP
Top View



Pin Functions: OPA2333

PIN			I/O	DESCRIPTION
NAME	VSON	SOIC, VSSOP		
+IN	—	—	I	Noninverting input
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
–IN	—	—	I	Inverting input
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
OUT	—	—	O	Output
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V+	8	8	—	Positive (highest) power supply
V–	4	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Voltage	Supply	7		V
	Signal input terminals(2)	–0.3	(V+) + 0.3	
Current	Signal input terminals(2)	–1	1	mA
	Output short-circuit(3)	Continuous		
Operating junction temperature, T_J			150	°C
Operating temperature, T_A		–40	150	
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage, V_S	1.8	5.5	V
Specified temperature	–40	125	°C

6.4 Thermal Information: OPA333

THERMAL METRIC(1)		OPA333			UNIT
		D (SOIC)	DBV (SOT)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.6	61.7	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2333

THERMAL METRIC(1)		OPA2333			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (VSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	180.3	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.0	2.4	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	22.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	10.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		2	10	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		0.02	0.05	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5.5 V, T_A = –40°C to 125°C		1	5	µV/V
	Long-term stability(1)			See note (1)		µV
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A= 25°C		±70	±200	pA
		T_A = –40°C to 125°C		±150		
I_{OS}	Input offset current			±140	±400	
NOISE						
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz		1.1		
i_n	Input current noise	f = 10 Hz		100		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to 125°C	106	130		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ, T_A = –40°C to 125°C	106	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = +1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	R_L = 10 kΩ		30	50	mV
		R_L = 10 kΩ, T_A = –40°C to 125°C			70	
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive			See *Typical Characteristics*		
	Open-loop output impedance	f = 350 kHz, I_O = 0 A		2		kΩ
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 A		17	25	µA
		T_A = –40°C to 125°C			28	
	Turn-on time	V_S = +5 V		100		µs
TEMPERATURE						
T_A	Specified range		–40		125	°C
	Operating range		–40		150	°C
T_{stg}	Storage range		–65		150	°C

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

6.7 Typical Characteristics

Table 1. List of Typical Characteristics

TITLE	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Production Distribution	Figure 2
Open-Loop Gain vs Frequency	Figure 3
Common-Mode Rejection Ratio vs Frequency	Figure 4
Power-Supply Rejection Ratio vs Frequency	Figure 5
Output Voltage Swing vs Output Current	Figure 6
Input Bias Current vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Quiescent Current vs Temperature	Figure 9
Large-Signal Step Response	Figure 10
Small-Signal Step Response	Figure 11
Positive Overvoltage Recovery	Figure 12
Negative Overvoltage Recovery	Figure 13
Settling Time vs Closed-Loop Gain	Figure 14
Small-Signal Overshoot vs Load Capacitance	Figure 15
0.1-Hz to 10-Hz Noise	Figure 16
Current and Voltage Noise Spectral Density vs Frequency	Figure 17

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

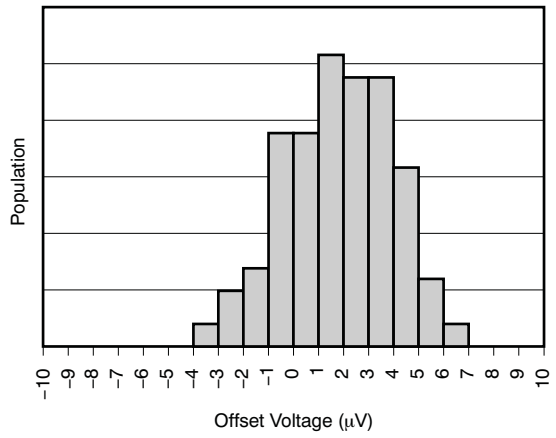


Figure 1. Offset Voltage Production Distribution

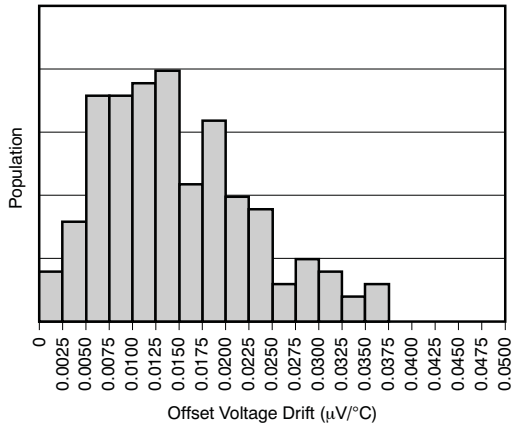


Figure 2. Offset Voltage Drift Production Distribution

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

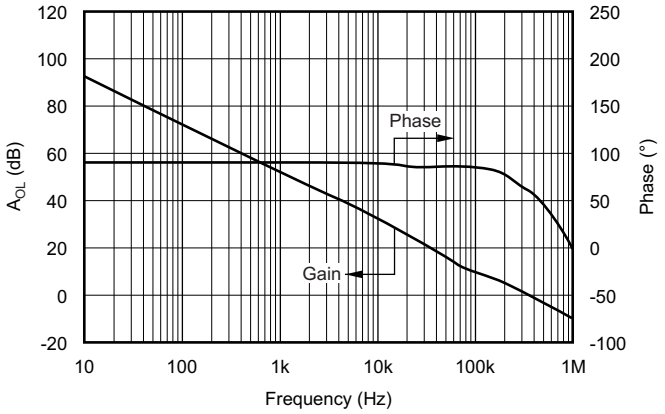


Figure 3. Open-Loop Gain and Phase vs Frequency

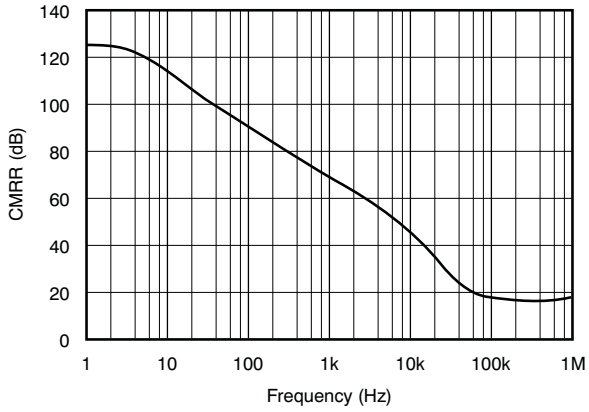


Figure 4. Common-Mode Rejection Ratio vs Frequency

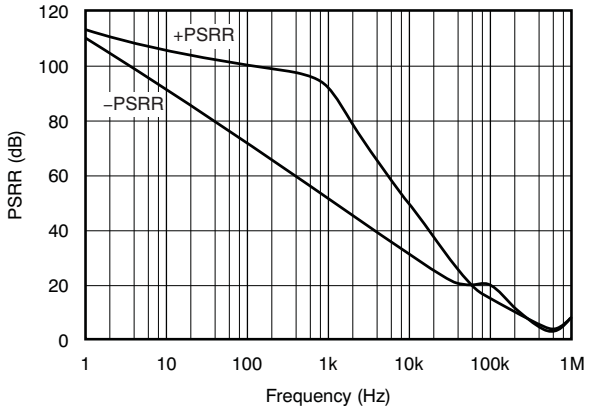


Figure 5. Power-Supply Rejection Ratio vs Frequency

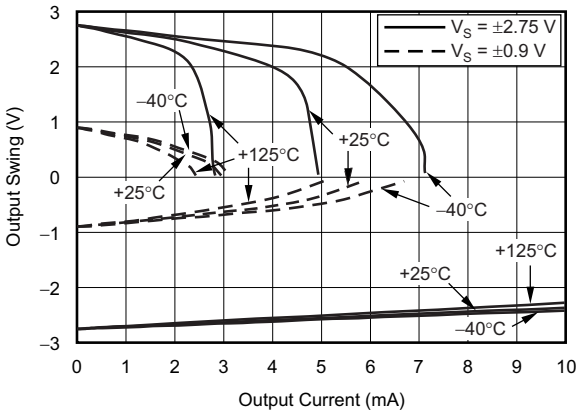


Figure 6. Output Voltage Swing vs Output Current

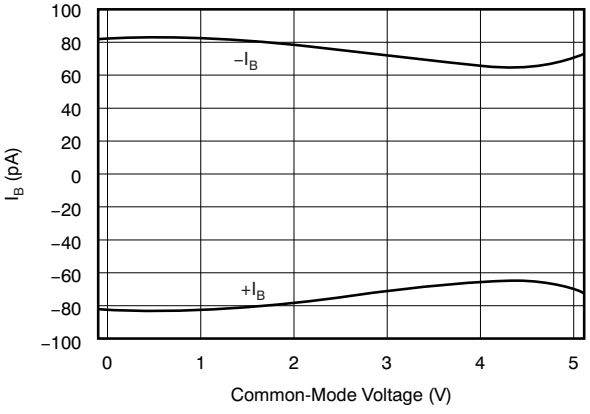


Figure 7. Input Bias Current vs Common-Mode Voltage

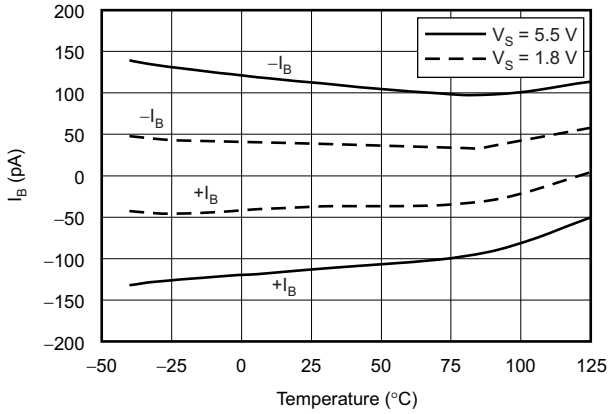


Figure 8. Input Bias Current vs Temperature

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

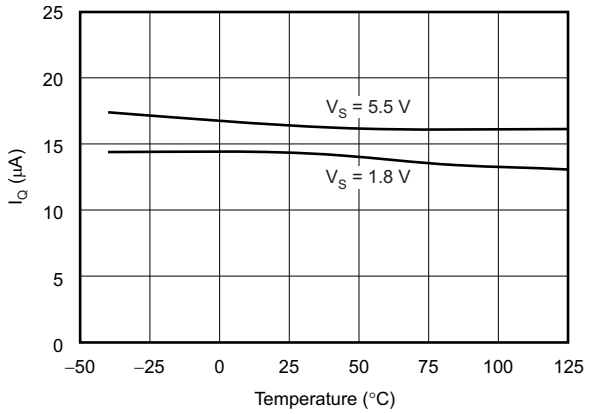


Figure 9. Quiescent Current vs Temperature

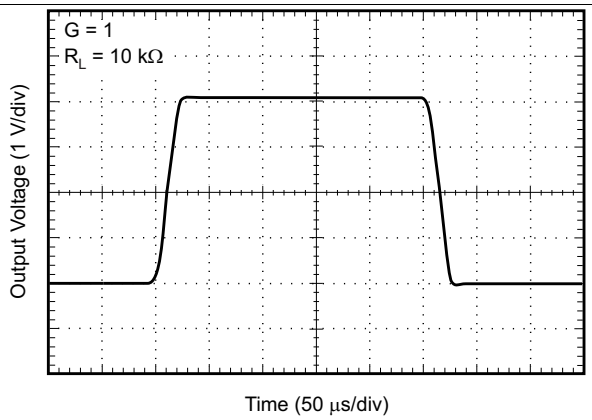


Figure 10. Large-Signal Step Response

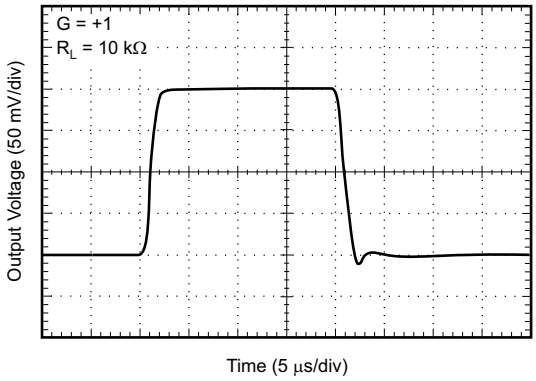


Figure 11. Small-Signal Step Response

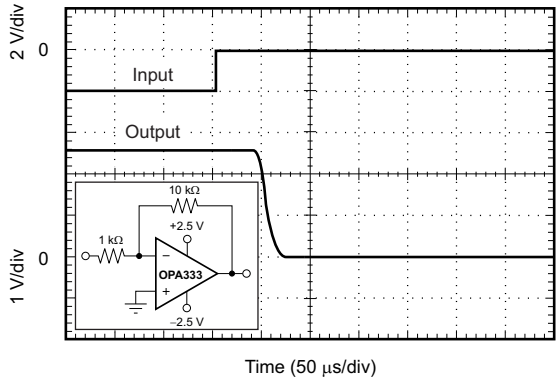


Figure 12. Positive Overvoltage Recovery

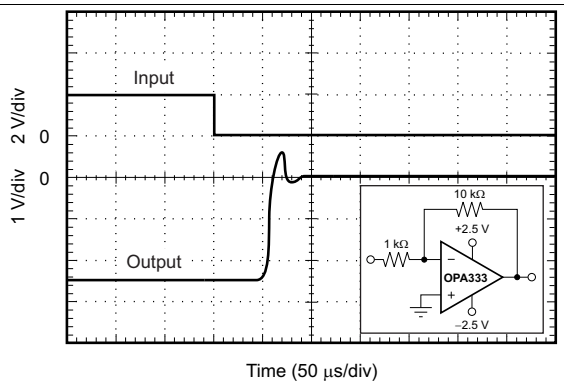


Figure 13. Negative Overvoltage Recovery

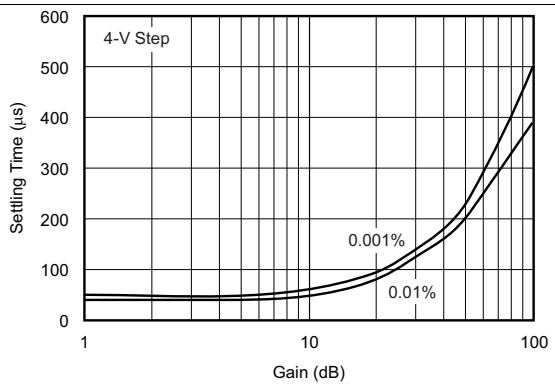


Figure 14. Settling Time vs Closed-Loop Gain

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF, unless otherwise noted.

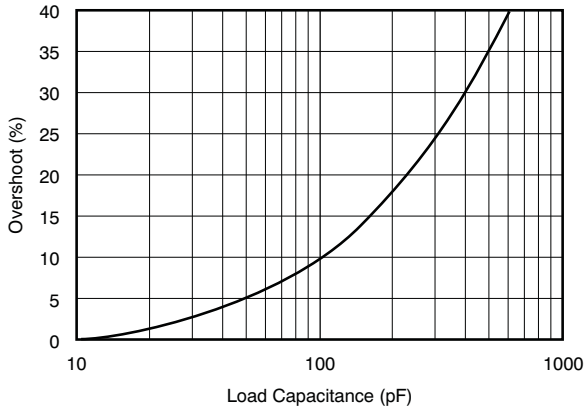


Figure 15. Small-Signal Overshoot vs Load Capacitance

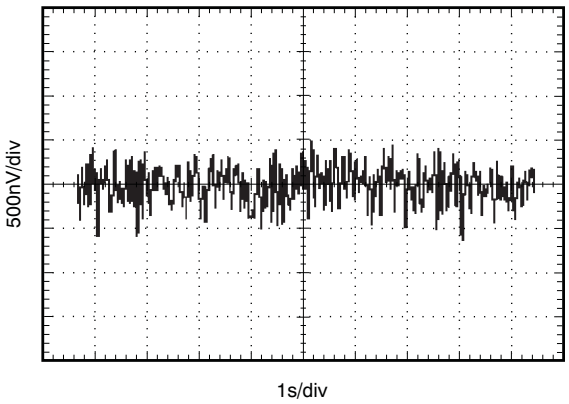


Figure 16. 0.1-Hz to 10-Hz Noise

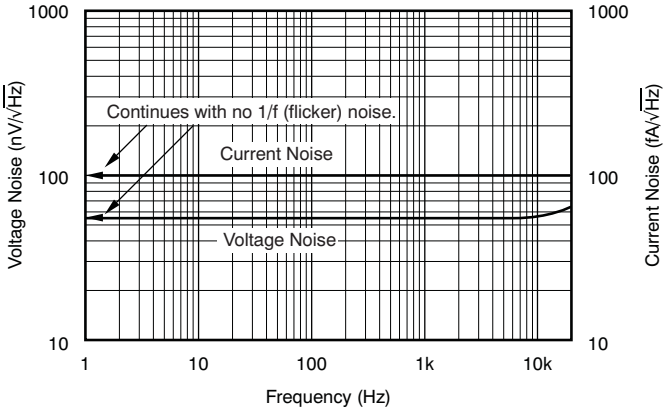


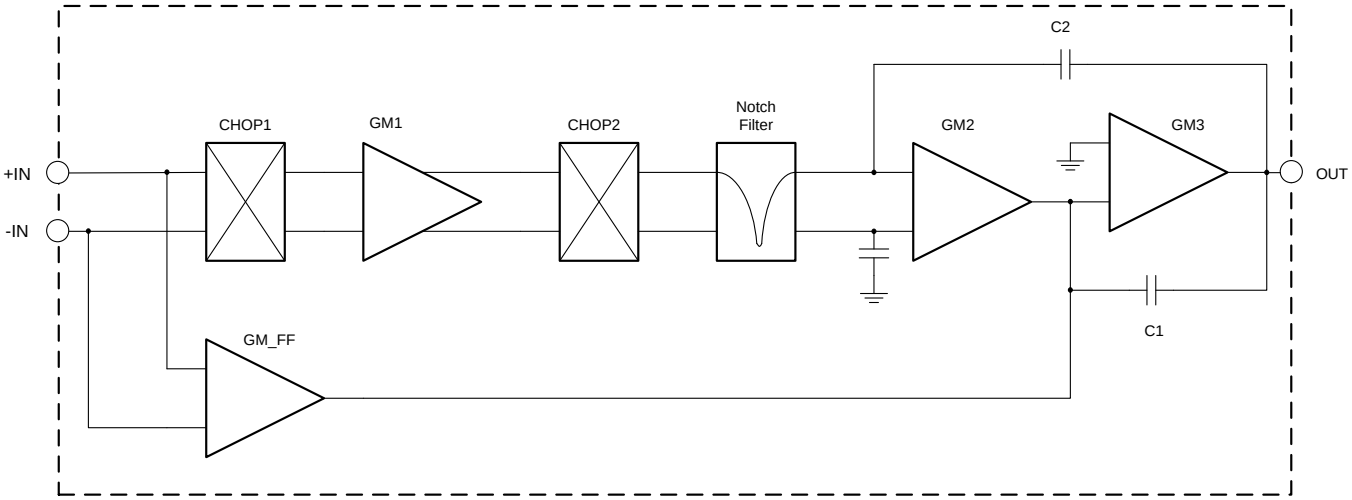
Figure 17. Current and Voltage Noise Spectral Density vs Frequency

7 Detailed Description

7.1 Overview

The OPAx333 is a family of Zero-Drift, low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The Zero-Drift architecture provides ultra low offset voltage and near-zero offset voltage drift.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA333 and OPA2333 are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 µV/°C or higher, depending on materials used.

7.3.1 Operating Voltage

The OPA333 and OPA2333 operational amplifiers operate over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section.

CAUTION

Supply voltages higher than +7 V (absolute maximum) can permanently damage the device.

Feature Description (continued)

7.3.2 Input Voltage

The OPA333 and OPA2333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 70 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

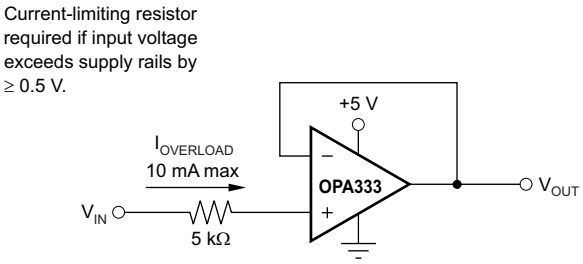


Figure 18. Input Current Protection

7.3.3 Internal Offset Correction

The OPA333 and OPA2333 operational amplifiers use an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.4 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good, single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA333 and OPA2333 can be made to swing to, or slightly below, ground on a single-supply power source. This swing is achieved with the use of the use of another resistor and an additional, more negative power supply than the operational amplifier negative supply. A pulldown resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 19.

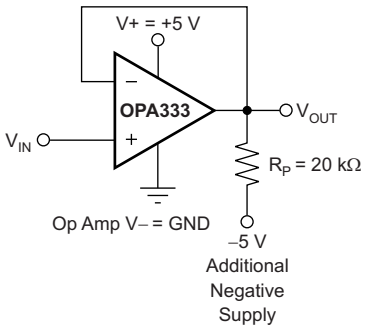


Figure 19. V_{OUT} Range to Ground

Feature Description (continued)

The OPA333 and OPA2333 have an output stage that allows the output voltage to be pulled to the negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333 and OPA2333 are characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ.

NOTE

This configuration increases the current consumption by several hundreds of microamps.

Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns after the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

7.3.5 DFN Package

The OPA2333 is offered in an DFN-8 package (also known as *SON*). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard PCB assembly techniques. See Application Reports SLUA271, *QFN/SON PCB Attachment* and SCBA017, *Quad Flatpack No-Lead Logic Packages*, both are available for download at www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the package should be connected to V– or left unconnected.

7.4 Device Functional Modes

The OPAx333 device has a single functional mode. The device is powered on as long as the power supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx333 family is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Applications

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 20 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 21 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333 facilitate excellent dc accuracy for the circuit.

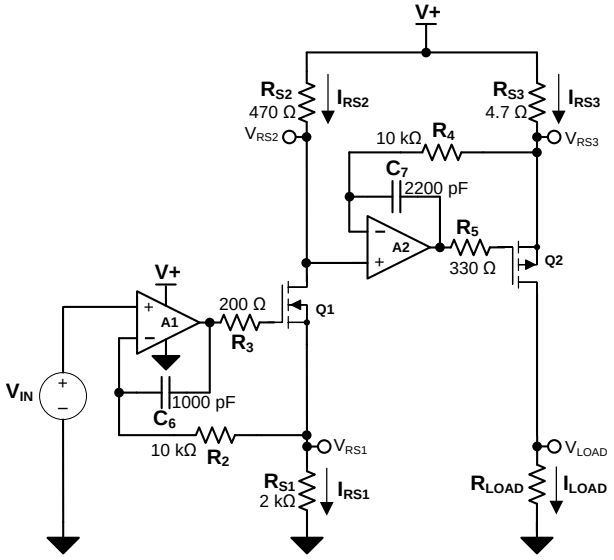


Figure 20. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

8.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2333 CMOS operational amplifier is a high-precision, 5-uV offset, 0.05-µV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2333 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2333 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in TIPD102.

8.2.1.3 Application Curve

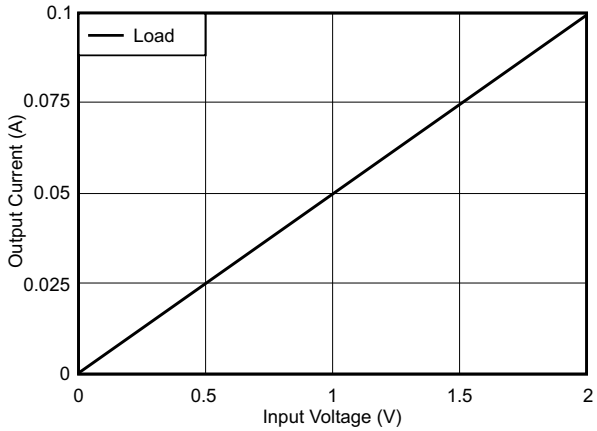


Figure 21. Measured Transfer Function for High-Side V-I Converter

Typical Applications (continued)

8.2.2 Precision, Low-Level Voltage-to-Current (V-I) Converter

The circuit shown in Figure 22 is a precision, low-level voltage-to-current (V-I) converter. The converter translates in input voltage of 0 V to 5 V and output current of 0 µA to 5 µA. Figure 23 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA333 facilitate excellent dc accuracy for the circuit. Figure 24 shows the calibrated error for the entire range of the circuit.

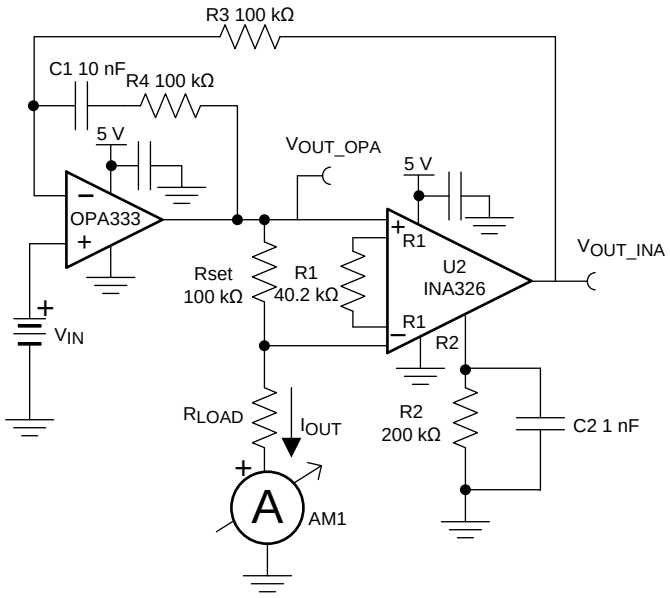


Figure 22. Low-Level, Precision V-I Converter

8.2.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 5 V DC
- Output: 0 µA to 5 µA DC

8.2.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, R_{SET}, and the instrumentation amplifier (INA) gain. During operation, the input voltage divided by the INA gain appears across the set resistor in Equation 1:

$$V_{SET} = V_{IN}/G_{INA} \quad (1)$$

The current through R_{SET} must flow through the load, so I_{OUT} is V_{SET} / R_{SET}. I_{OUT} remains a well-regulated current as long as the total voltage across R_{SET} and R_{LOAD} does not violate the output limits of the operational amplifier or the input common-mode limits of the INA. The voltage across the set resistor (V_{SET}) is the input voltage divided by the INA gain (that is, V_{SET} = 1 V / 10 = 0.1 V). The current is determined by V_{SET} and R_{SET} shown in Equation 2:

$$I_{OUT} = V_{SET} / R_{SET} = 0.1\ V / 100\ k\Omega = 1\ \mu A \quad (2)$$

A detailed error analysis, design procedure, and additional measured results are given in TIPD107.

Typical Applications (continued)

8.2.2.3 Application Curves

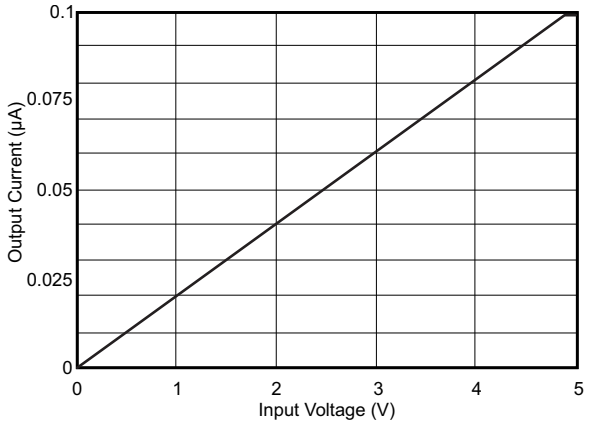


Figure 23. Measured Transfer Function for Low-Level Precision V-I

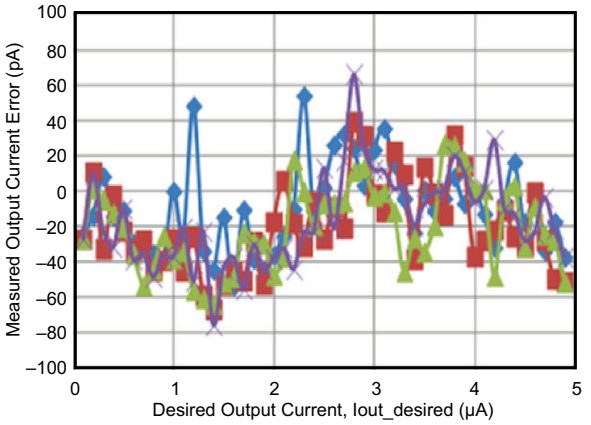


Figure 24. Calibrated Output Error for Low-Level V-I

8.2.3 Composite Amplifier

The circuit shown in Figure 25 is a composite amplifier used to drive the reference on the ADS8881. The OPA333 provides excellent dc accuracy, and the THS4281 allows the output of the circuit to respond quickly to the transient current requirements of a typical SAR data converter reference input. The ADS8881 system was optimized for THD and achieved a measured performance of –110 dB. The linearity of the ADC is shown Figure 26.

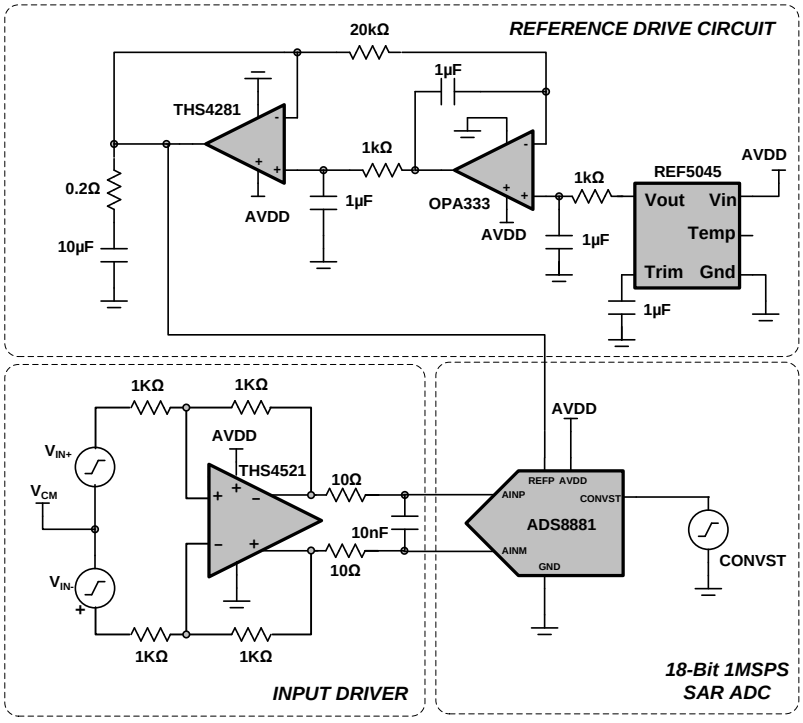


Figure 25. Composite Amplifier Reference Driver Circuit

Typical Applications (continued)

8.2.3.1 Design Requirements

The design requirements for this block design are:

- System Supply Voltage: 5 V DC
- ADC Supply Voltage: 3.3 V DC
- ADC Sampling Rate: 1 MSPS
- ADC Reference Voltage (VREF): 4.5 V DC
- ADC Input Signal: A differential input signal with amplitude of V_{pk} = 4.315 V (–0.4 dBFS to avoid clipping) and frequency, f_{IN} = 10 kHz are applied to each differential input of the ADC

8.2.3.2 Detailed Design Procedure

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver design. The circuit comprises the critical analog circuit blocks, the input driver, anti-aliasing filter, and the reference driver. Each analog circuit block should be carefully designed based on the ADC performance specifications in order to maximize the distortion and noise performance of the data acquisition system while consuming low power. The diagram includes the most important specifications for each individual analog block. This design systematically approaches the design of each analog circuit block to achieve a 16-bit, low-noise and low-distortion data acquisition system for a 10-kHz sinusoidal input signal. The first step in the design requires an understanding of the requirement of extremely low distortion input driver amplifier. This understanding helps in the decision of an appropriate input driver configuration and selection of an input amplifier to meet the system requirements. The next important step is the design of the anti-aliasing RC-filter to attenuate ADC kick-back noise while maintaining the amplifier stability. The final design challenge is to design a high-precision reference driver circuit, which would provide the required value VREF with low offset, drift, and noise contributions.

In designing a very low distortion data acquisition block, it is important to understand the sources of nonlinearity. Both the ADC and the input driver introduce nonlinearity in a data acquisition block. To achieve the lowest distortion, the input driver for a high-performance SAR ADC must have a distortion that is negligible against the ADC distortion. This parameter requires the input driver distortion to be 10 dB lower than the ADC THD. This stringent requirement ensures that overall THD of the system is not degraded by more than –0.5 dB.

$$THD_{AMP} < THD_{ADC} - 10\ dB \quad (3)$$

It is therefore important to choose an amplifier that meets the above criteria to avoid the system THD from being limited by the input driver. The amplifier nonlinearity in a feedback system depends on the available loop gain. A detailed error analysis, design procedure, and additional measured results are given in TIPD115.

8.2.3.3 Application Curve

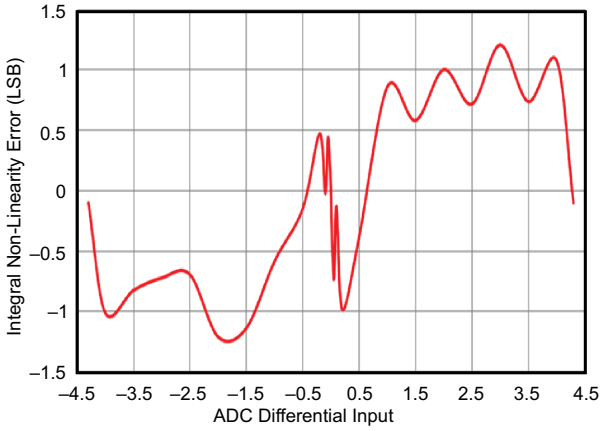


Figure 26. Linearity of the ADC8881 System

8.3 System Examples

8.3.1 Temperature Measurement Application

Figure 27 shows a temperature measurement application.

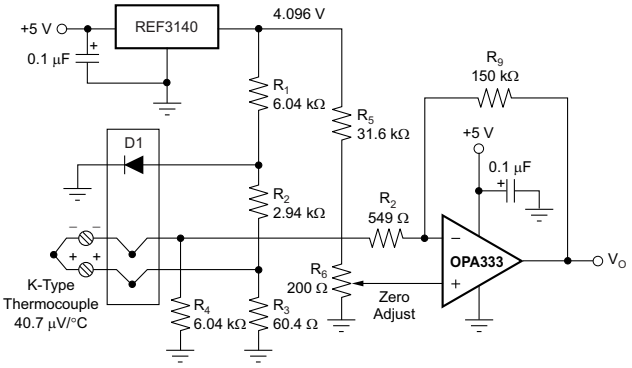


Figure 27. Temperature Measurementf

8.3.2 Single Operational Amplifier Bridge Amplifier Application

Figure 28 shows the basic configuration for a bridge amplifier.

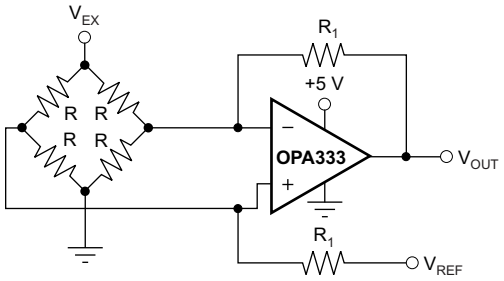
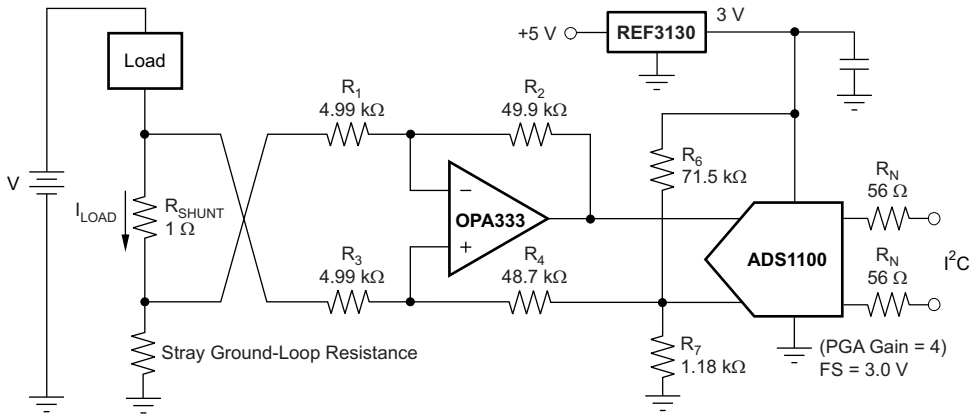


Figure 28. Single Operational Amplifier Bridge Amplifier

8.3.3 Low-Side Current Monitor Application

A low-side current shunt monitor is shown in Figure 29. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.

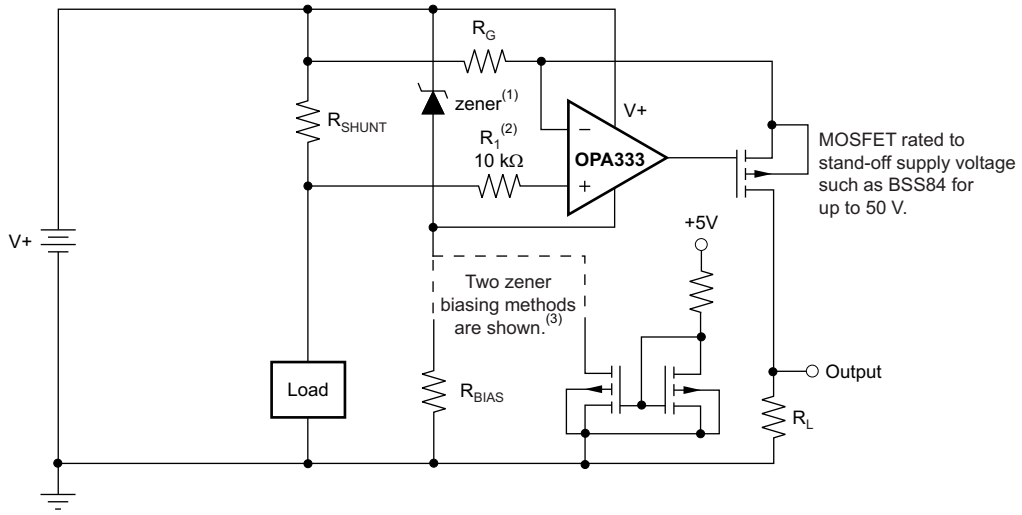


NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 29. Low-Side Current Monitor

8.3.4 Other Applications

Additional application ideas are shown in Figure 30 through Figure 33.



(1) Zener rated for op amp supply capability (that is, 5.1 V for OPA333).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual N-MOSFETs (FDG6301N, NTJD4001N, or Si1034).

Figure 30. High-Side Current Monitor

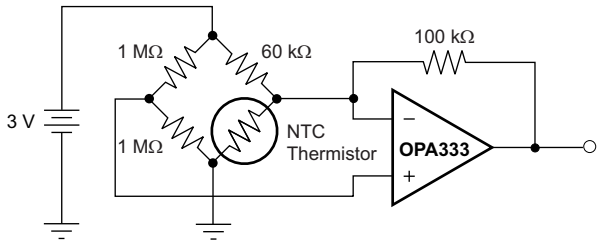


Figure 31. Thermistor Measurement

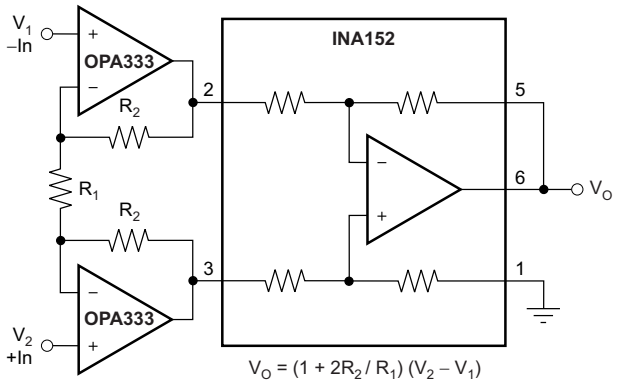
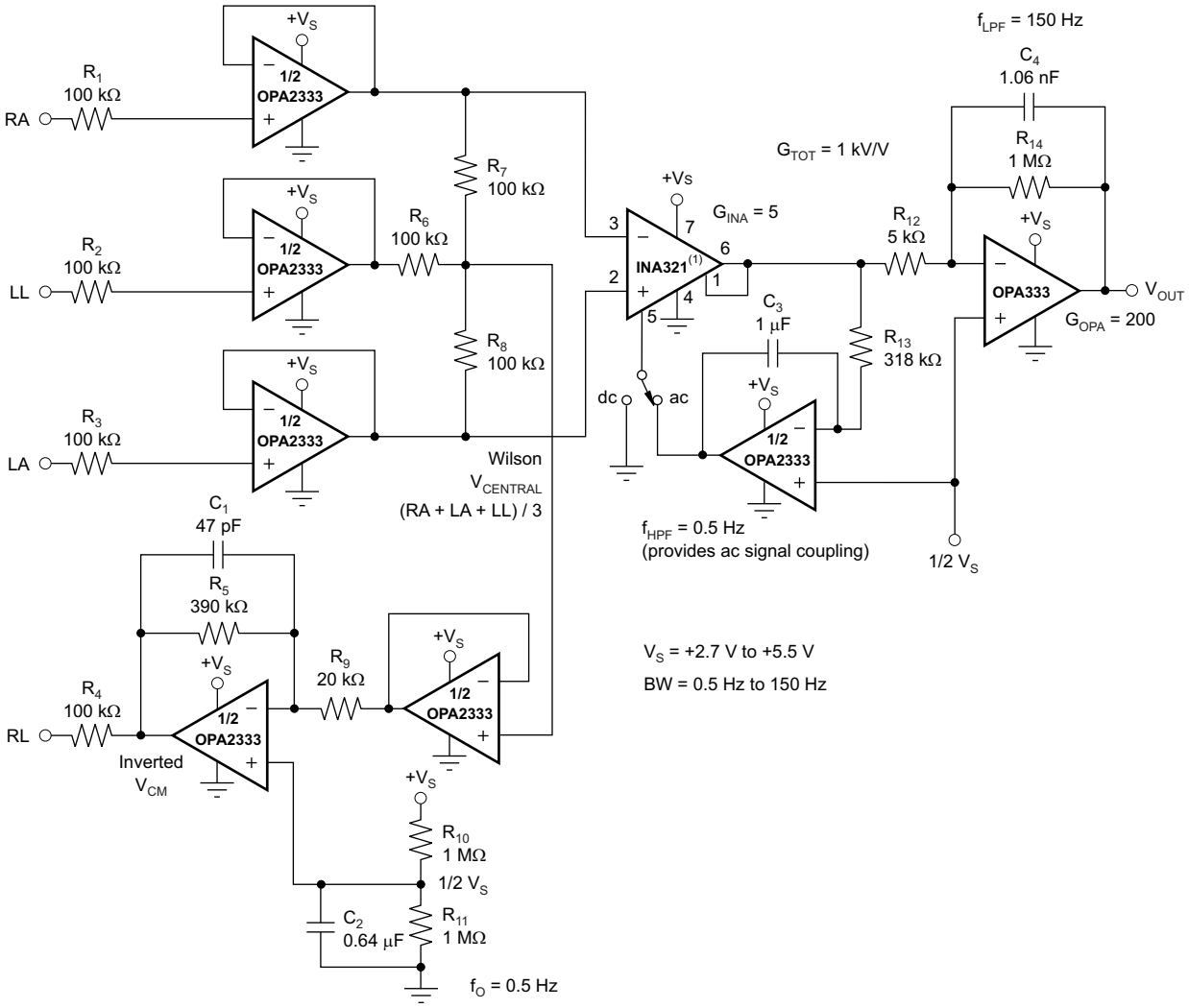


Figure 32. Precision Instrumentation Amplifier



(1) Other instrumentation amplifiers can be used, such as the INA326, which has lower noise, but higher quiescent current.

Figure 33. Single-Supply, Very Low Power, ECG Circuit

9 Power Supply Recommendations

The OPAx333 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

10 Layout

10.1 Layout Guidelines

10.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

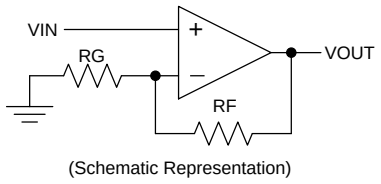
Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA333 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

10.1.2 DFN Layout Guidelines

Solder the exposed leadframe die pad on the DFN package to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

10.2 Layout Example



(Schematic Representation)

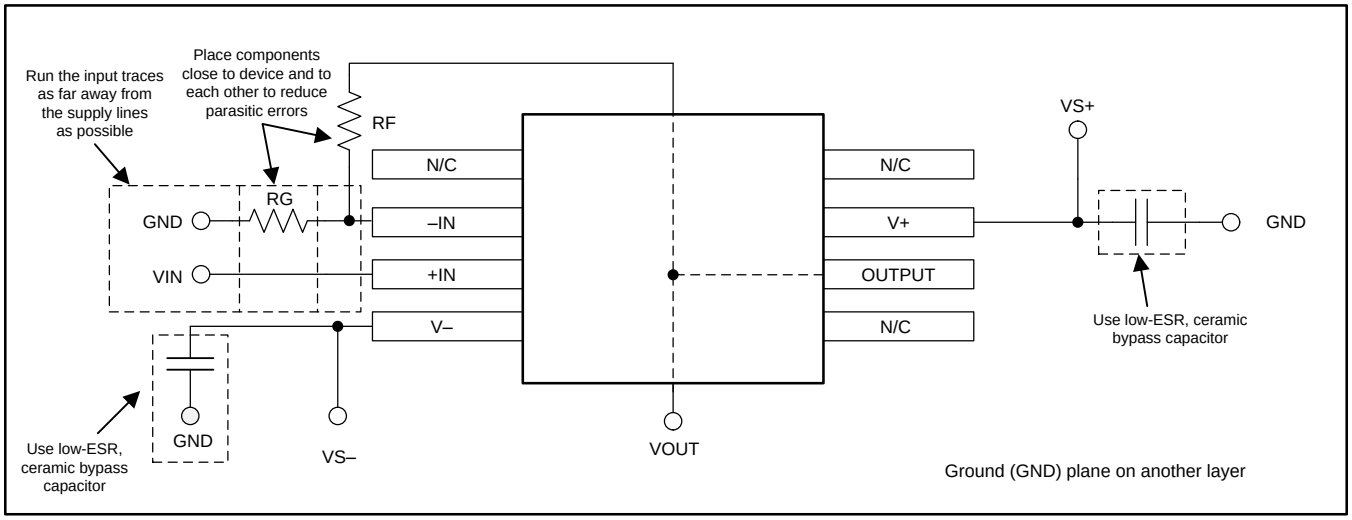


Figure 34. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support on this product, see the following:

- *High-Side V-I Converter, 0 V to 2 V to 0 mA to 100 mA, 1% Full-Scale Error,* TIPD102
- *Low-Level V-to-I Converter Reference Design, 0-V to 5-V Input to 0-µA to 5-µA Output,* TIPD107
- *18-Bit, 1-MSPS, Serial Interface, microPower, Truly-Differential Input, SAR ADC,* ADS8881
- *Very Low-Power, High-Speed, Rail-To-Rail Input/Output, Voltage Feedback Operational Amplifier,* THS4281
- *Data Acquisition Optimized for Lowest Distortion, Lowest Noise, 18-bit, 1-MSPS Reference Design,* TIPD115
- *Self-Calibrating, 16-Bit Analog-to-Digital Converter,* ADS1100
- *20-ppm/Degrees C Max, 100-µA, SOT23-3 Series Voltage Reference,* REF3130
- *Precision, Low Drift, CMOS Instrumentation Amplifier, INA326,* INA326

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *QFN/SON PCB Attachment*, SLUA271
- *Quad Flatpack No-Lead Logic Packages*, SCBA017

11.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA333	Click here	Click here	Click here	Click here	Click here
OPA2333	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2333AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA2333AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA2333AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA2333AIDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA333AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples
OPA333AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA333AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples
OPA333AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2333, OPA333 :

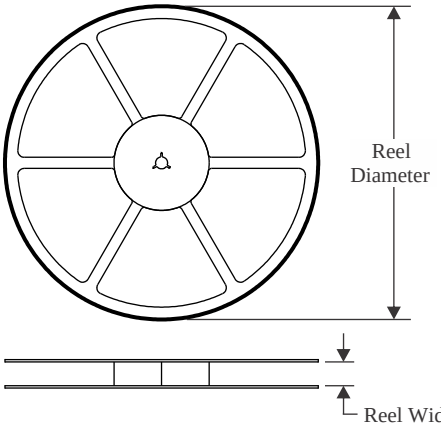
- Automotive : OPA2333-Q1, OPA333-Q1

NOTE: Qualified Version Definitions:

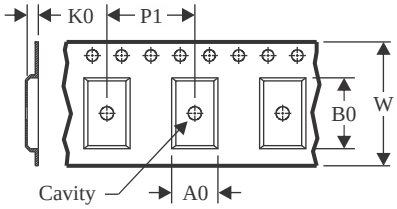
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

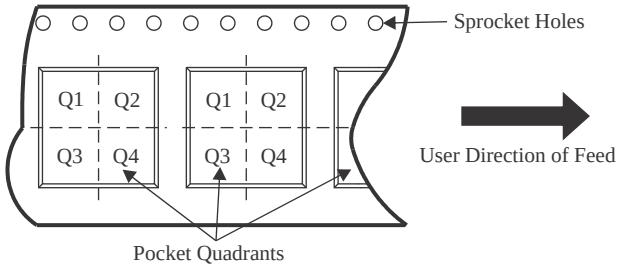


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

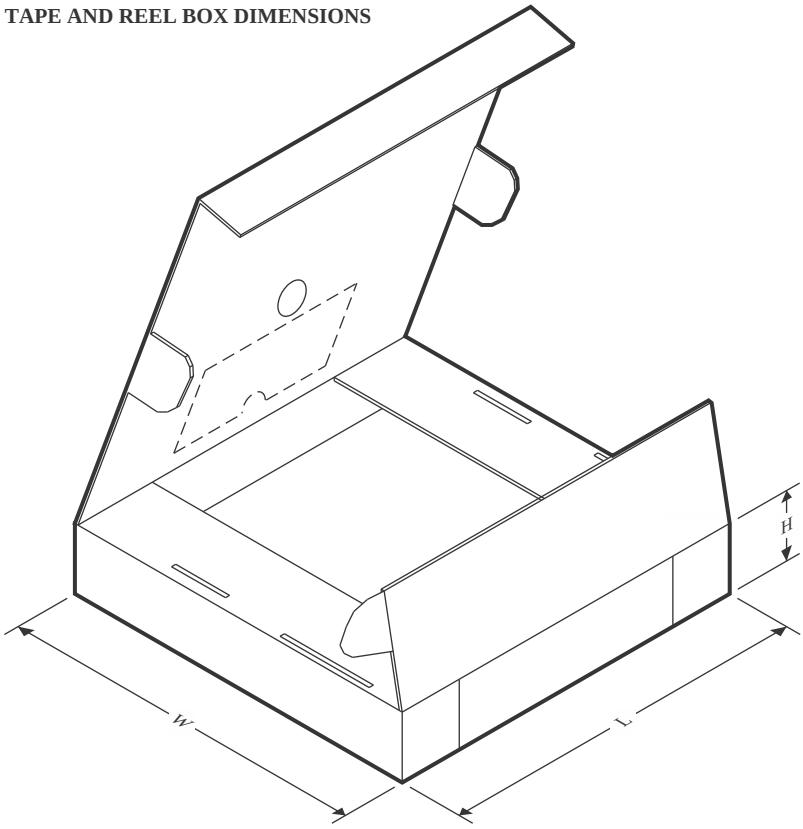
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2333AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2333AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA333AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA333AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA333AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA333AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

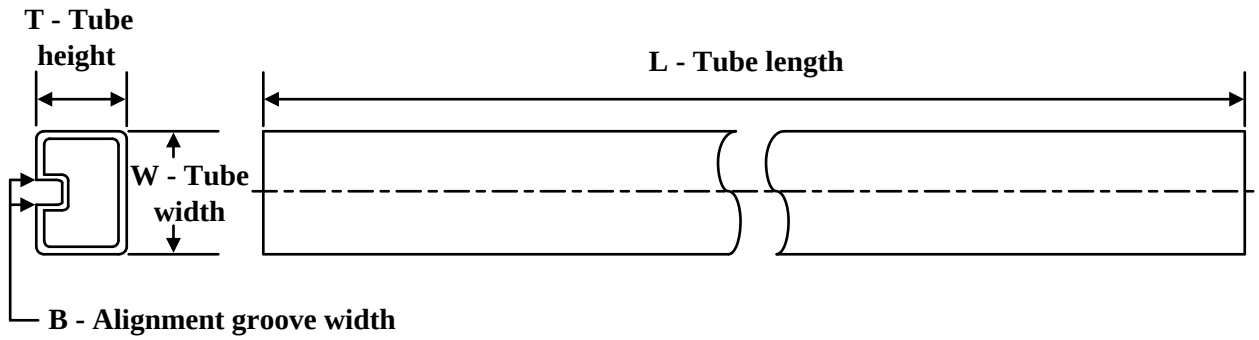
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2333AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2333AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2333AIDRBR	SON	DRB	8	3000	356.0	356.0	35.0
OPA2333AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA333AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA333AIDBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
OPA333AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA333AIDCKR	SC70	DCK	5	3000	200.0	183.0	25.0
OPA333AIDCKT	SC70	DCK	5	250	200.0	183.0	25.0
OPA333AIDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2333AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2333AIDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA333AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA333AIDG4	D	SOIC	8	75	506.6	8	3940	4.32

GENERIC PACKAGE VIEW

DRB 8

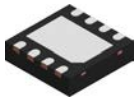
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

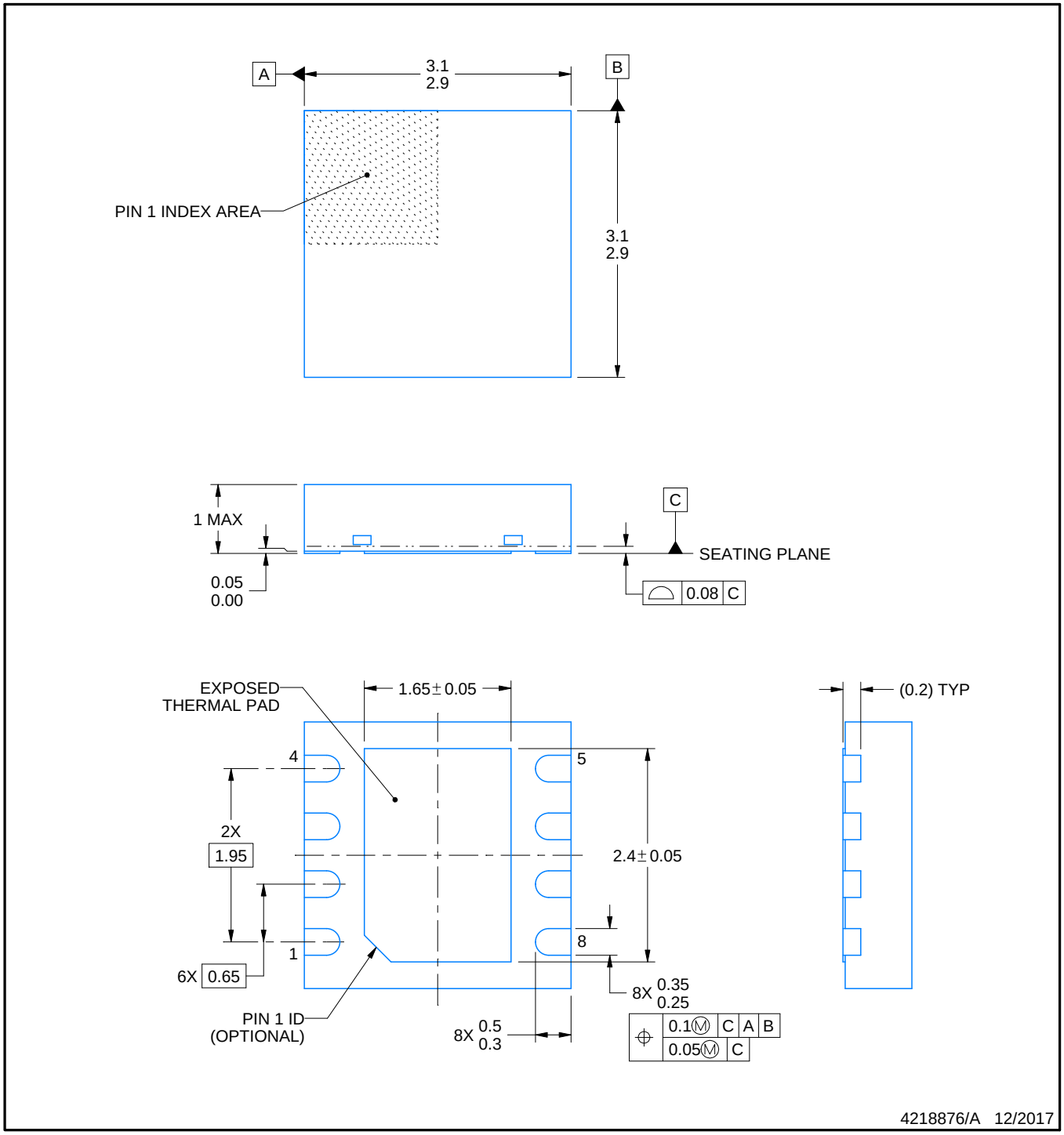
DRB0008B



PACKAGE OUTLINE

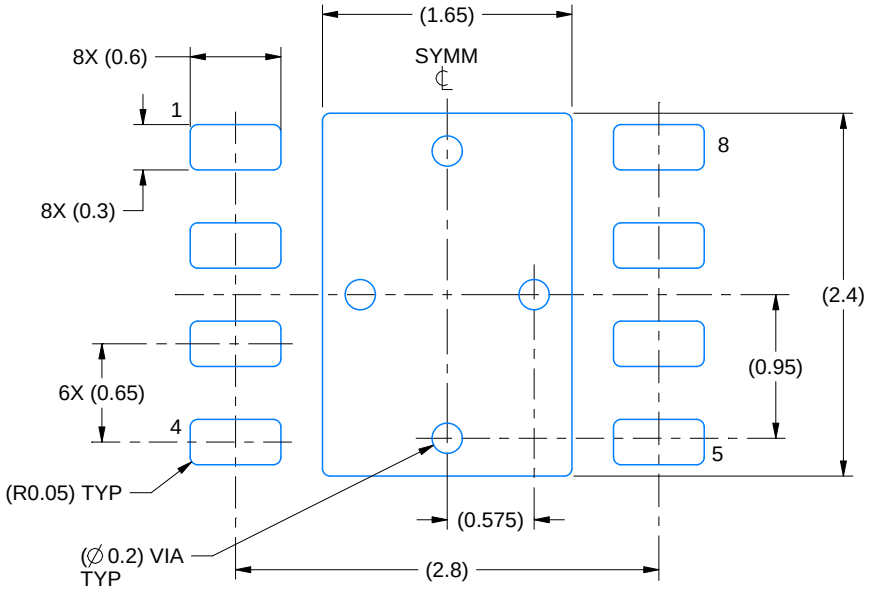
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

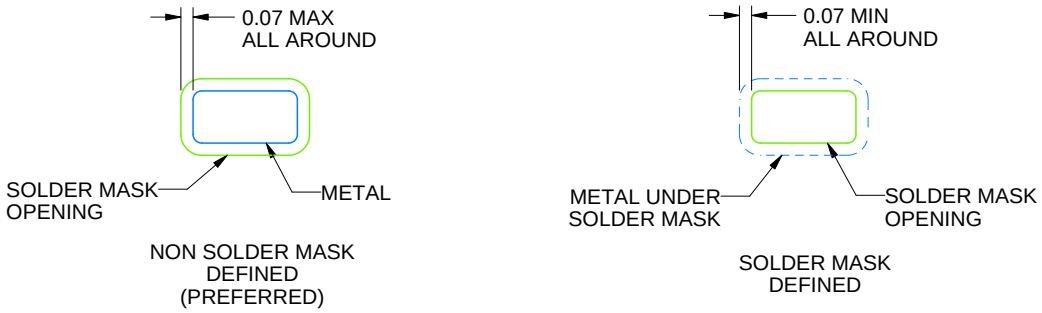


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

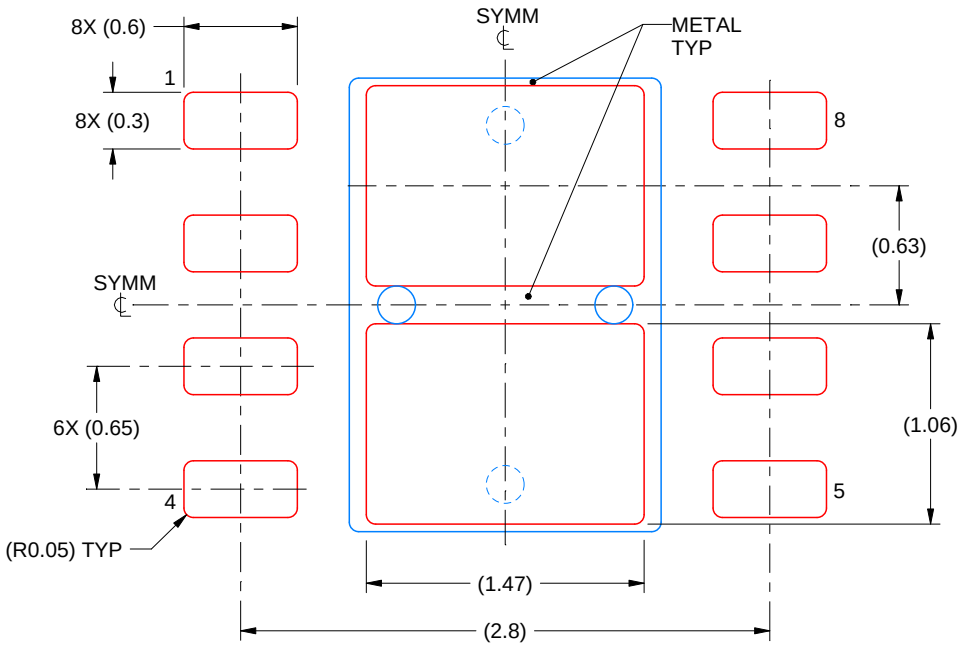


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

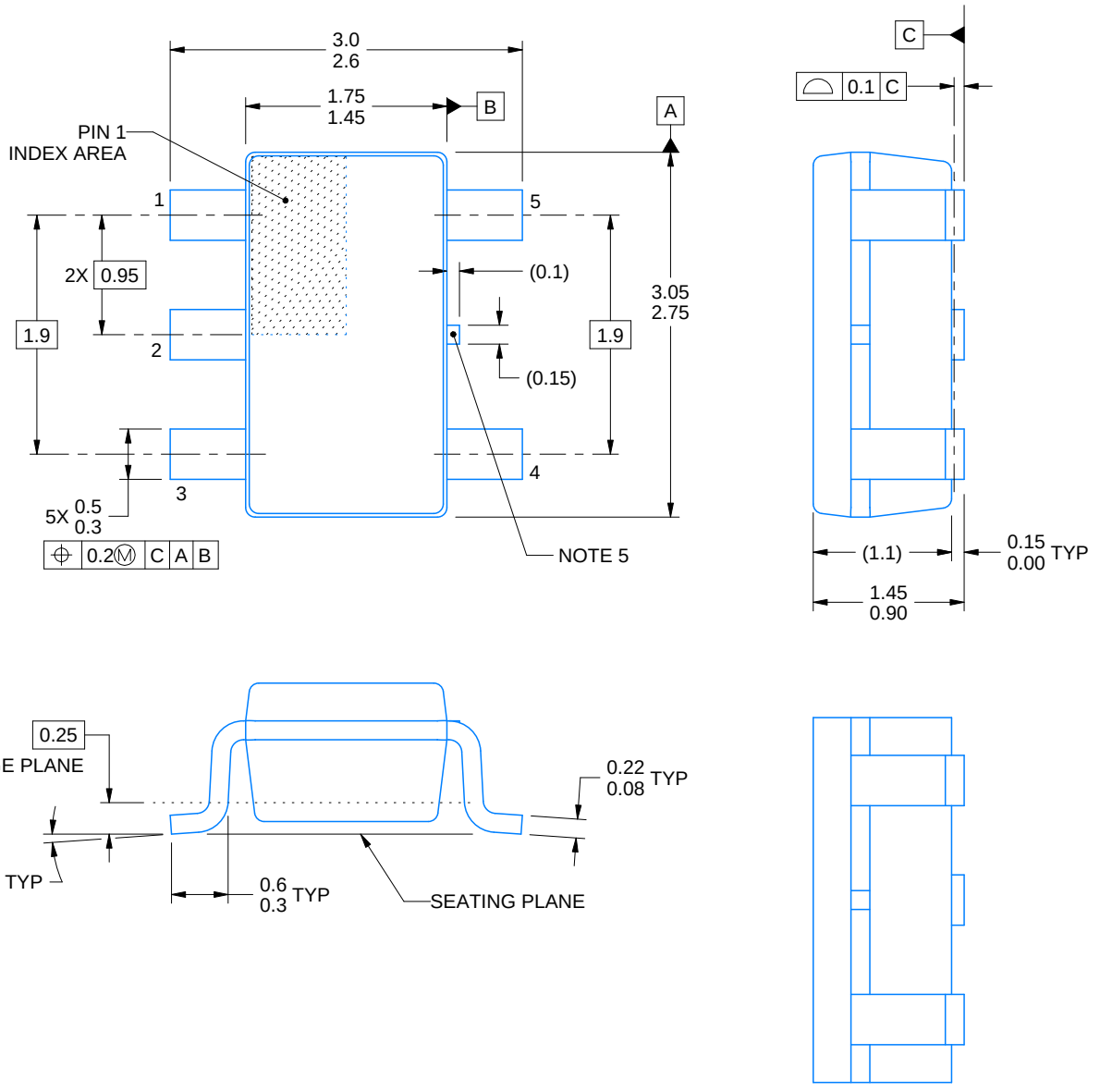
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

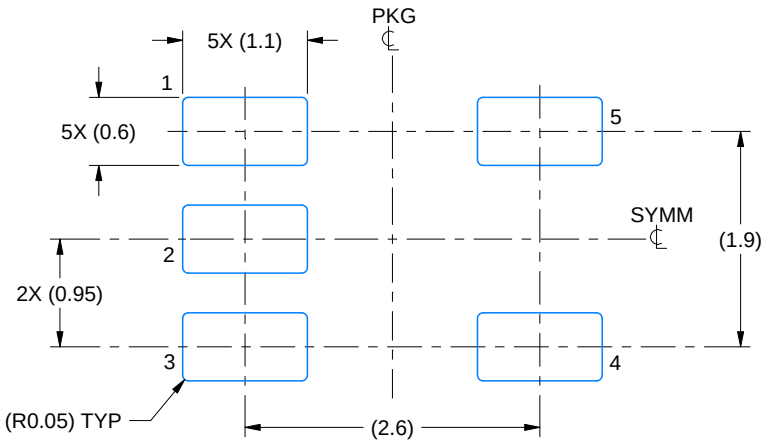


ALTERNATIVE PACKAGE SINGULATION VIEW

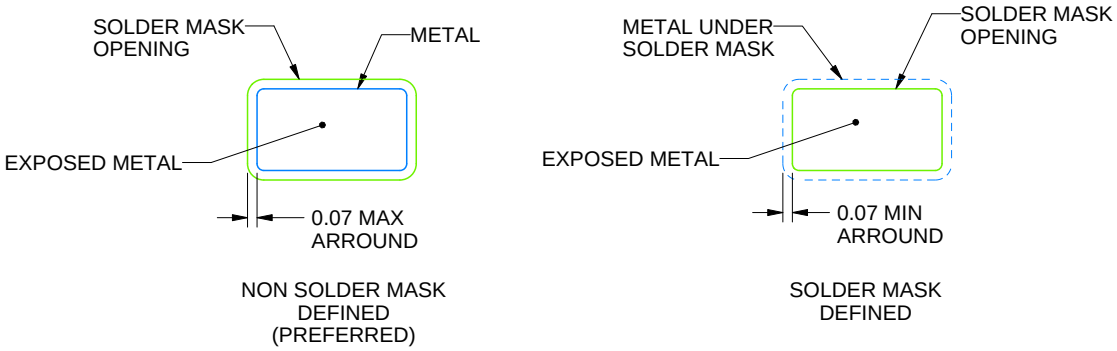
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

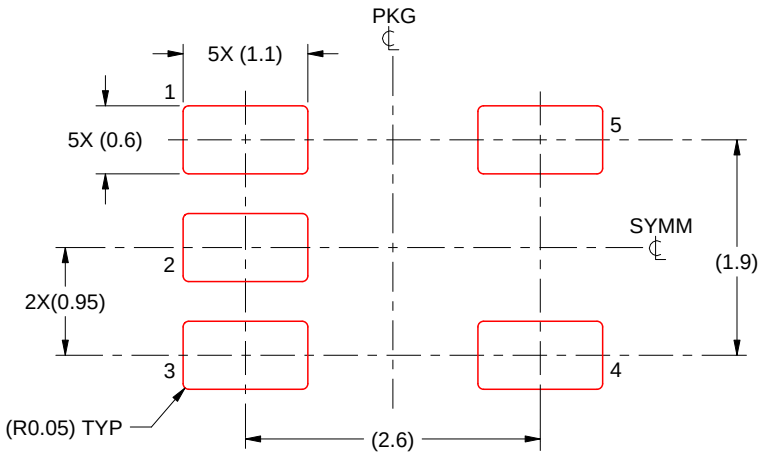


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

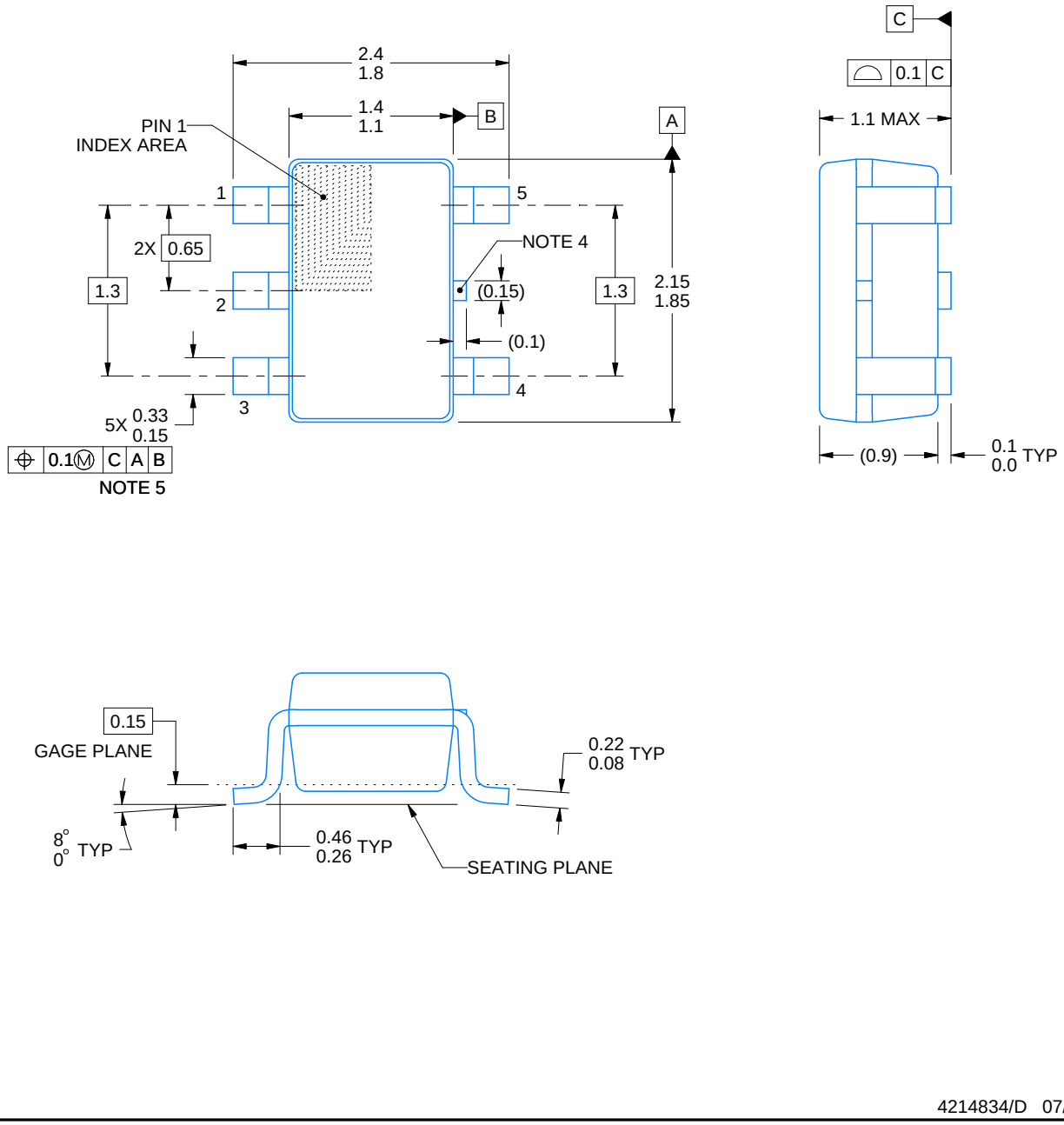
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

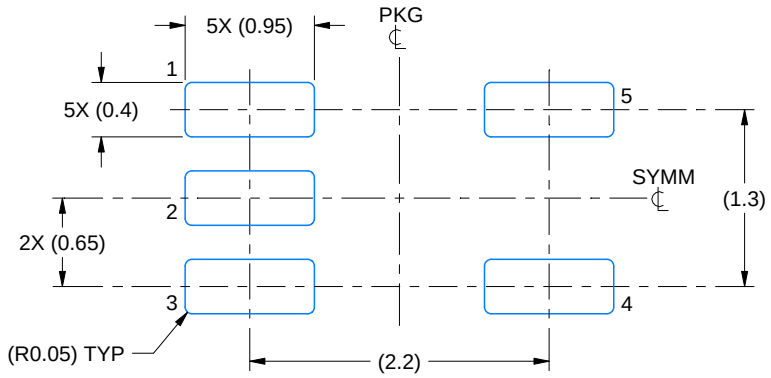
SMALL OUTLINE TRANSISTOR



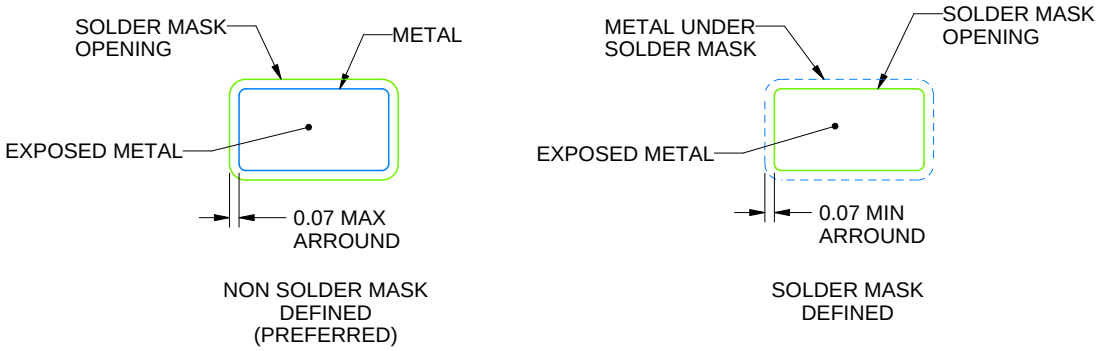
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

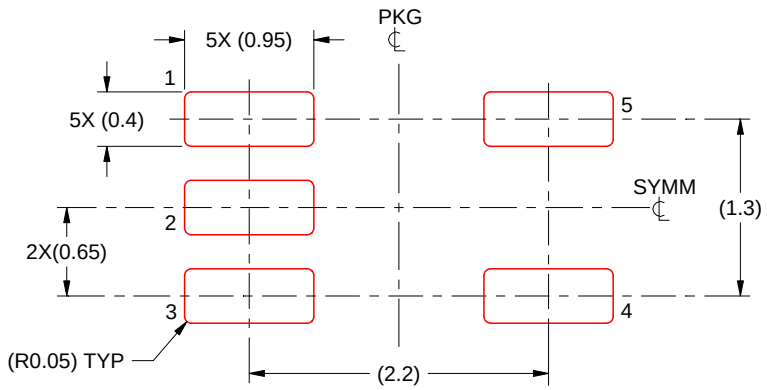


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

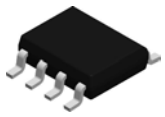


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

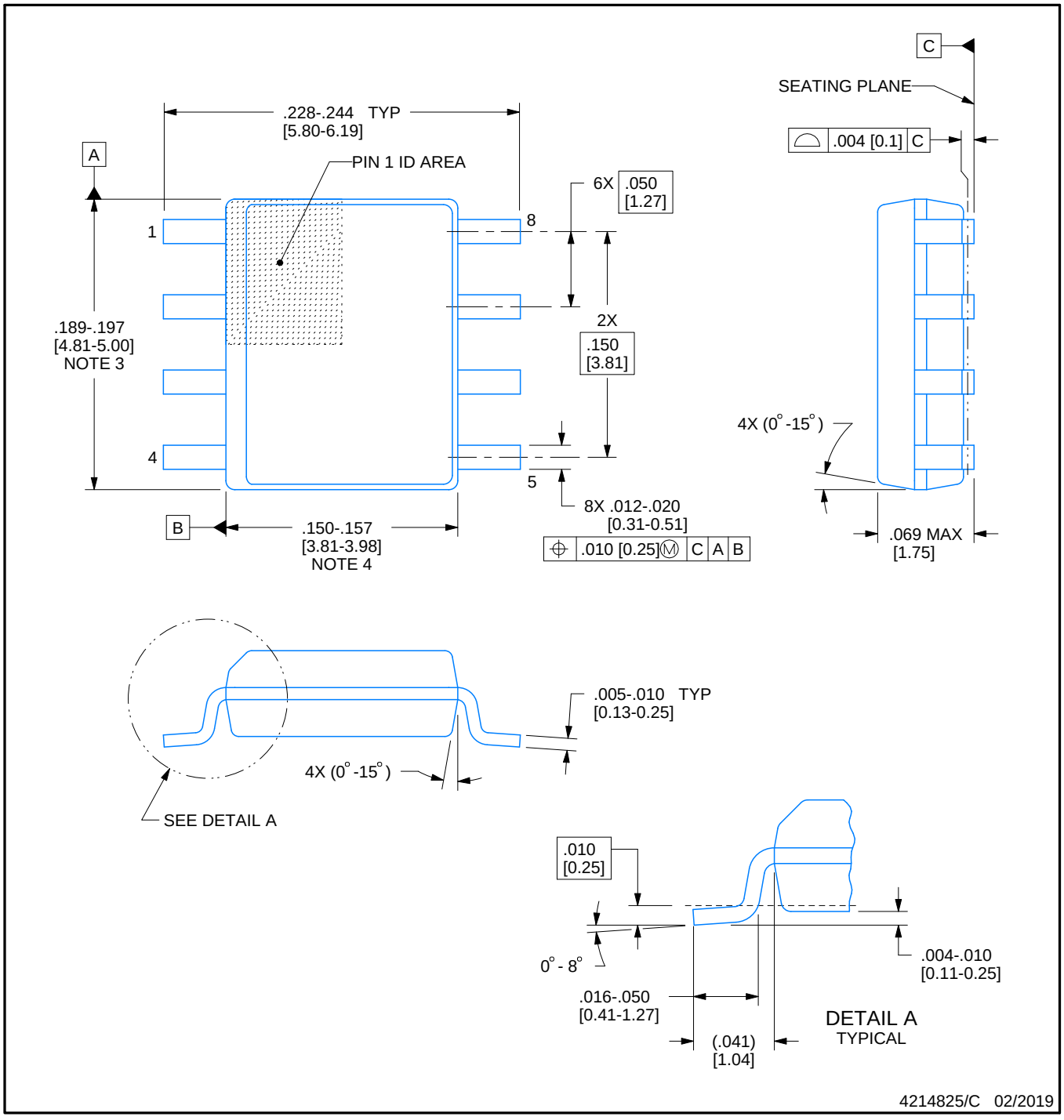


PACKAGE OUTLINE

D0008A

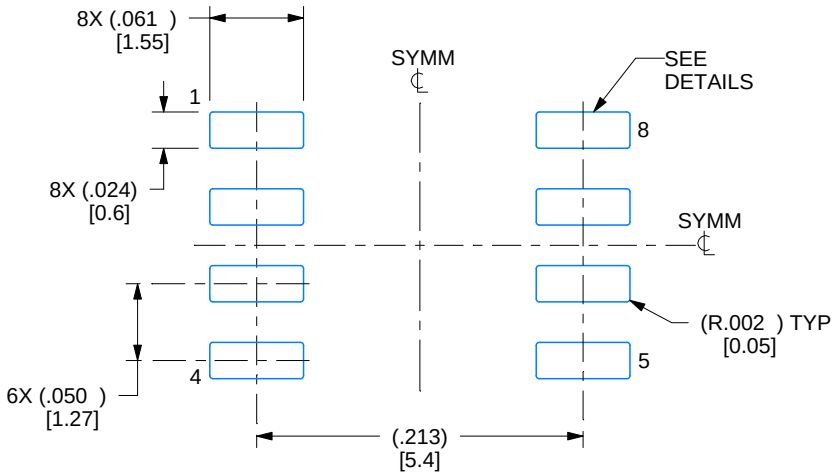
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

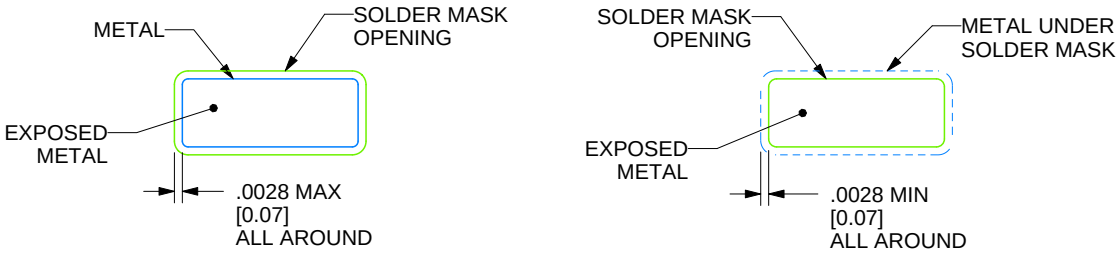


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

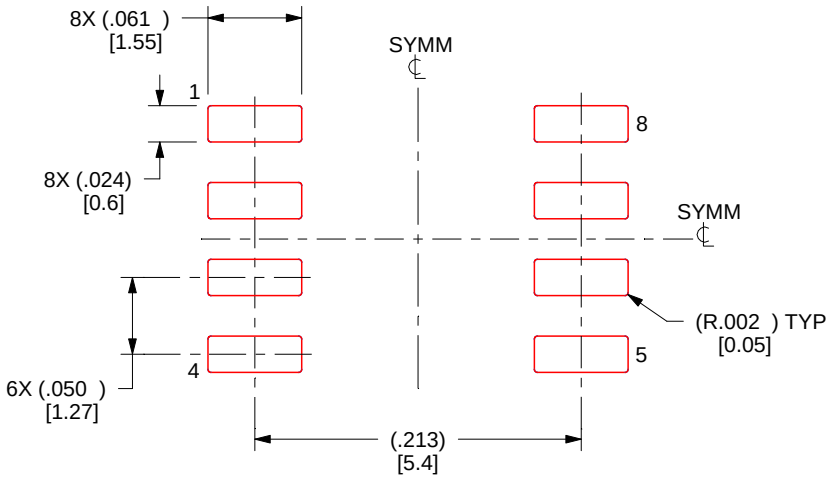
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



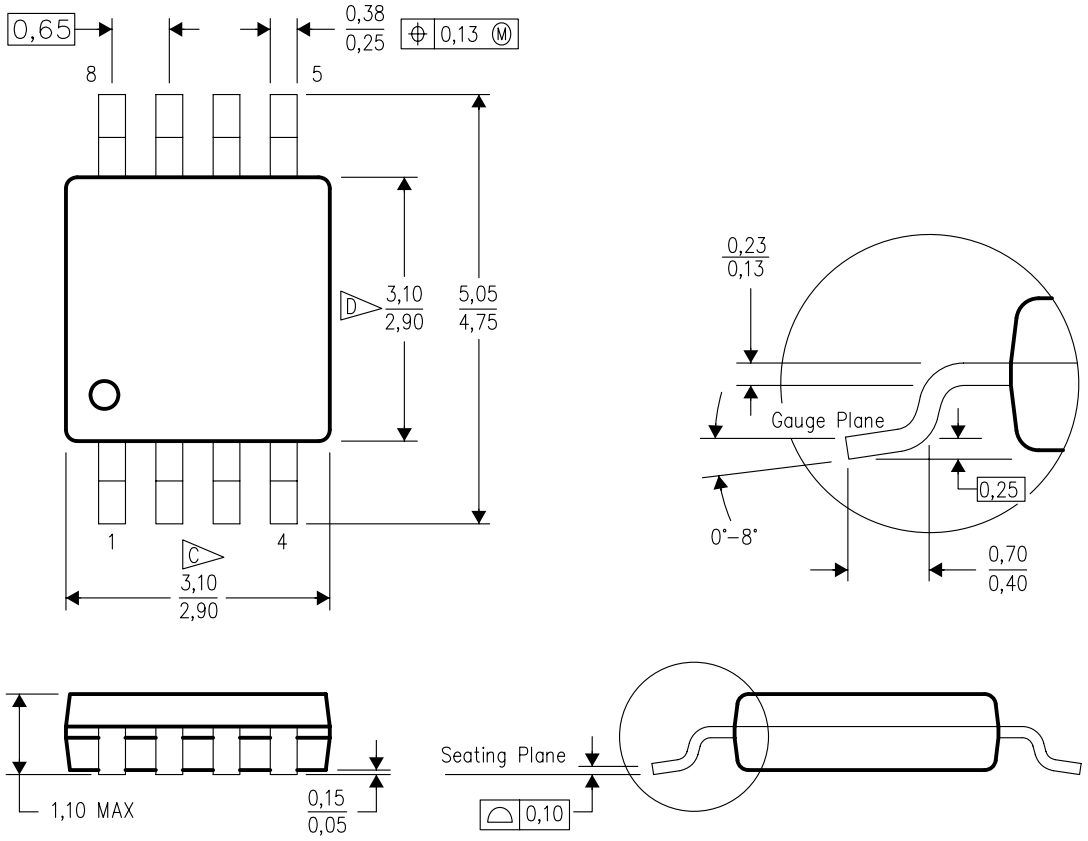
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

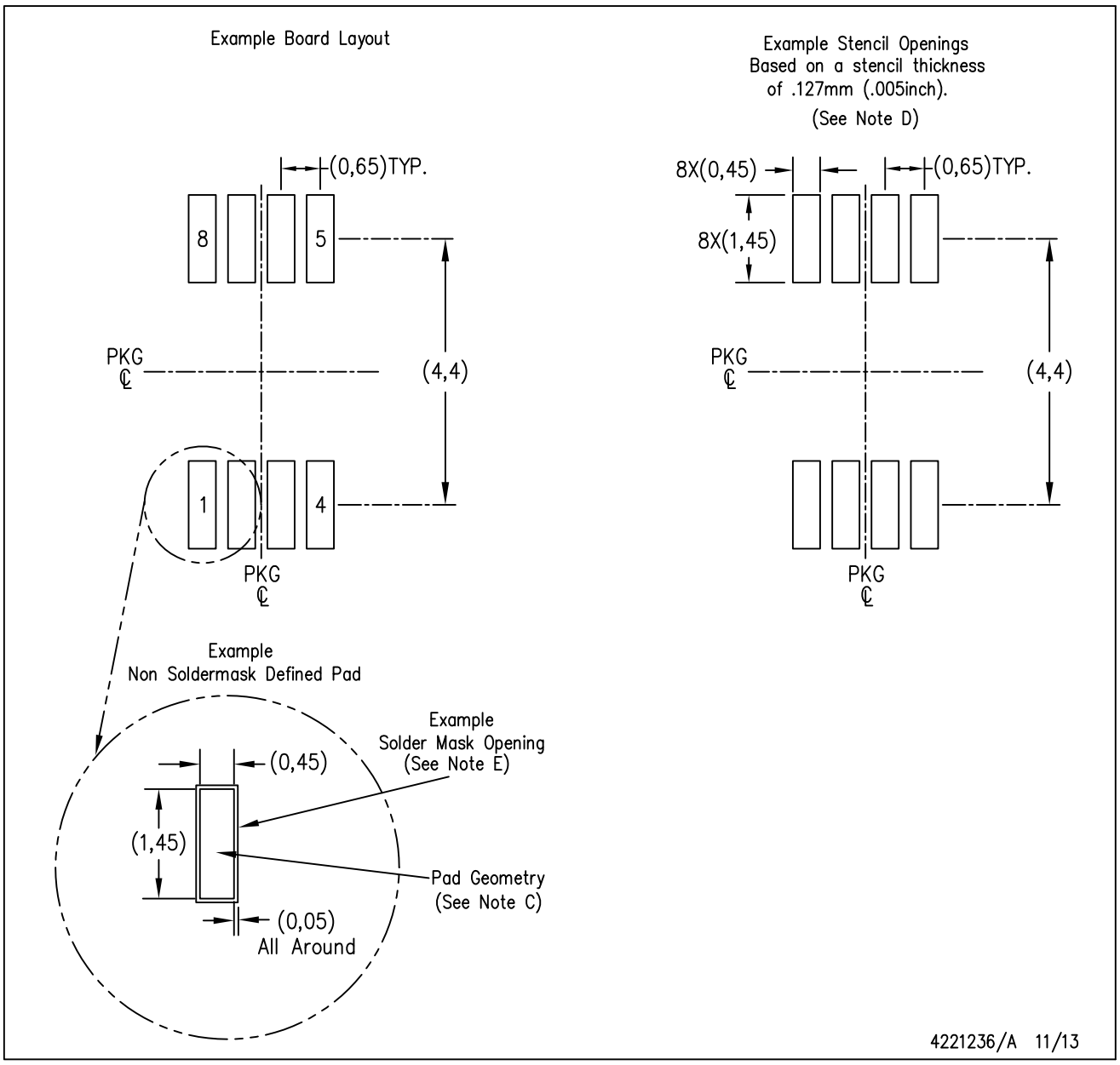
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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