TMS320F28P65x Real-Time Microcontrollers

1 Features

Real-time Processing

- Contains up to three CPUs: two 32-bit C28x DSP CPUs and one CLA CPU, all running at 200 MHz
- Delivers a total processing power equivalent to 1000-MHz Arm® Cortex®-M7 based device on real-time signal chain performance (see the *Real-time Benchmarks Showcasing C2000™ Control MCU's Optimized Signal Chain Application Note*)
- C28x DSP architecture
  - IEEE 754 double-precision (64-bit) Floating-Point Unit (FPU)
  - Trigonometric Math Unit (TMU)
  - Fast Integer Division (FINTDIV)
  - CRC engine and instructions (VCRC)
- Control Law Accelerator (CLA) CPU
  - IEEE 754 single-precision floating-point
  - Executes code independently of C28x CPUs

Memory

- 1.28MB of CPU-mappable flash (ECC-protected) with 5 flash banks
- 248KB of RAM (Enhanced Parity-protected)
- External Memory Interface (EMIF) with ASRAM, SDRAM support or ASIC/FPGA

Analog Subsystem

- Three Analog-to-Digital Converters (ADCs)
  - 16-bit mode, 1.19 MSPS each
  - 12-bit mode, 3.92 MSPS each
  - Up to 40 single-ended or 19 differential inputs
  - Separate sample-and-hold (S/H) on each ADC to enable simultaneous measurements
  - Hardware post-processing of conversions
  - Hardware oversampling (up to 128x) and undersampling modes, with accumulation, averaging and outlier rejection
  - 24 redundant input channels for flexibility
  - Automatic comparison of conversion results for functional safety applications
- 11 windowed comparators with 12-bit Digital-to-Analog Converter (DAC) references
  - DAC with slope compensation – enabling peak current and valley current mode control
  - Connection options for internal temperature sensor and ADC reference
- Two 12-bit buffered DAC outputs

Control Peripherals

- 36 Pulse Width Modulator (PWM) channels, all with 150-ps high-resolution capability (HRPWM)
  - Minimum Dead-Band Logic (MINDB), Illegal Combo Logic (ICL), and other special features (that is, Diode Emulation [DE]) support
  - Enable Matrix Converters, Multilevel Converters, and Resonant Converters support without additional external logic
- Seven Enhanced Capture (eCAP) modules
  - High-resolution Capture (HRCAP) available on two of the seven eCAP modules
  - Two new monitor units for edge, pulse width, and period that can be coupled with ePWM strobes and trip events
  - Increased 256 inputs for more capture options
  - New ADC SOC generation capability
  - eCAP can also be used for additional PWM
  - Six Enhanced Quadrature Encoder Pulse (eQEP) modules
  - 16 Sigma-Delta Filter Module (SDFM) input channels, 2 independent filters per channel
  - Embedded Pattern Generator (EPG)
- Configurable Logic Block
  - Six logic tiles to augment existing peripheral capability or define customized logic to reduce or remove external CPLD/FPGA
  - Supports Encoder interfaces without the need of FPGA
  - Enables customized PWM generation for power conversion

Communications Peripherals

- EtherCAT® SubordinateDevice (or SubDevice) Controller (ESC)
- USB 2.0 (MAC + PHY)
- Fast Serial Interface (FSI) enabling up to 200Mbps data exchange across isolation
- Four high-speed (up to 50-MHz) SPI ports
- Four Serial Communications Interfaces (SCI) (support UART)
- Two high-speed (25Mbps) Universal Asynchronous Receiver/Transmitters (UARTs)
- Two I2C interfaces (400Kbps)
- External boot option via SPI/ SCI/I2C
- Two UART-compatible Local Interconnect Network (LIN) Modules (support SCI)
- Power-Management Bus (PMBus) interface (supports I2C)
- One Controller Area Network (CAN/DCAN)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

- Two CAN FD/MCAN Controller Area Networks with Flexible Data Rate

System Peripherals

- Two 6-channel Direct Memory Access (DMA) controllers
- 185 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins
- Expanded Peripheral Interrupt controller (ePIE)
- Low-power mode (LPM) support
- Embedded Real-time Analysis and Diagnostic (ERAD)
- Background CRC (BGCRC)

Security Peripherals

- Advanced Encryption Standard (AES-128, 192, 256) accelerator
- Security
  - JTAGLOCK
  - Zero-pin boot
  - Dual-zone security
- Unique Identification (UID) number

Safety Peripherals

- Easier implementation with Reciprocal comparison
- Lockstep on C28x CPU 2
- Memory Power-On Self-Test (MPOST)
- Hardware Built-in Self-Test (HWBIST)
- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 and IEC 61508 system design
  - Systematic capability up to ASIL D and SIL 3 targeted
  - Hardware capability up to ASIL B and SIL 2 targeted
- Safety-related certification
  - ISO 26262 and IEC 61508 certification up to ASIL B and SIL 2 by TÜV SÜD planned

Clock and System Control

- Two internal 10-MHz oscillators
- On-chip crystal oscillator
- 2*APLL, BOR, Redundant interrupt vector RAM
- Windowed watchdog timer module
- Missing clock detection circuitry
- Dual-clock Comparator (DCC)
- Live Firmware Update (LFU)
  - Fast context switching from old to new firmware with or without a power cycle
- 1.2-V core, 3.3-V I/O design
  - Internal VREG for 1.2-V generation
  - Brownout reset (BOR) circuit

Package options:

- Lead-free, green packaging
- 256-ball New Fine Pitch Ball Grid Array (nFBGA) [ZEJ suffix], 13 mm × 13 mm/0.8-mm pitch
- 176-pin PowerPAD™ Thermally Enhanced Low-profile Quad Flatpack (HLQFP) [PTP suffix], 26 mm × 26 mm/0.5-mm pitch
- 169-ball New Fine Pitch Ball Grid Array (nFBGA) [NMR suffix], 9 mm × 9 mm/0.65-mm pitch
- 100-pin PowerPAD™ Thermally Enhanced Thin Quad Flatpack (HTQFP) [PZP suffix], 16 mm × 16 mm/0.5-mm pitch

Temperature

- Ambient (T_A): –40°C to 125°C (industrial and automotive qualified)

2 Applications

- Servo drive control module
- Robot Servo Drive
- CNC control
- Mobile robot motor control
- HVAC large commercial motor control
- Linear motor segment controller
- Central inverter
- String inverter
- Power Conversion System
- DC Fast Charging Station
- Inverter & motor control
- Industrial AC-DC
- Three phase UPS
- Single phase online UPS
- Merchant network and server PSU
- On-board (OBC) & wireless charger
- Automotive HVAC compressor module
- Headlight

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3 Description

The TMS320F28P65x (F28P65x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of IGBT, GaN, and SiC technologies.

These include such applications as:

- Industrial motor drives
- Motor control
  - Traction inverter motor control
  - HVAC motor control
  - Mobile robot motor control
- Solar inverters
  - Central inverter
  - Micro inverter
  - String inverter
- Digital power
- Electrical vehicles and transportation
- EV charging infrastructure
- Energy Storage systems
- Industrial & collaborative robot
- Industrial machine & machine tools
- Industrial mobile robot

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 200 MIPS of signal-processing performance in each core for floating- or fixed-point code running from either on-chip flash or SRAM. This is equivalent to the 400-MHz processing power on a Cortex®-M7 based device (C28x DSP core gives two times more performance than the Cortex®-M7 core).The C28x CPU is further boosted by the Trigonometric Math Unit (TMU) and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems. Extended instruction sets enable IEEE double-precision 64-bit floating-point math. Finally, the Control Law Accelerator (CLA) enables an additional 200 MIPS per core of independent processing ability. This is equivalent to the 280-MHz processing power on a Cortex®-M7 based device (CLA CPU gives 40% more performance than the Cortex®-M7 core).

The lockstep dual-CPU comparator option has been added in the secondary C28x CPU along with ePIE and DMA for detection of permanent and transient faults. To allow fast context switching from existing to new firmware, hardware enhancements for Live Firmware Update (LFU) have been added to F28P65x.

High-performance analog blocks are tightly integrated with the processing and control units to provide optimal real-time signal chain performance. The Analog-to-Digital Converter (ADC) has been enhanced with up to 40 analog channels, 22 of which have general-purpose input/output (GPIO) capability. Implementation of oversampling is greatly simplified with hardware improvement. For safety-critical ADC conversions, a hardware redundancy checker has been added that provides the ability to compare ADC conversion results from multiple ADC modules for consistency without additional CPU cycles. Thirty-six frequency-independent PWMs, all with high-resolution capability, enable control of multiple power stages, from 3-phase inverters to advanced multilevel power topologies. The PWMs have been enhanced with Minimum Dead-Band Logic (MINDL) and Illegal Combo Logic (ICL) features.

The inclusion of the Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

An EtherCAT SubDevice Controller and other industry-standard protocols like CAN FD and USB 2.0 are available on this device. The Fast Serial Interface (FSI) enables up to 200 Mbps of robust communications across an isolation boundary.

As a highly connected device, the F28P65x also offers various security enablers to help designers implement their cyber security strategy and support features like hardware encryption, secure JTAG and secure Boot.

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From a safety standpoint, F28P65x supports numerous safety enablers. For more details, see *Industrial Functional Safety for C2000™ Real-Time Microcontrollers* and *Automotive Functional Safety for C2000™ Real-Time Microcontrollers*.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD28P65X evaluation board and download C2000Ware.

Device Information

PART NUMBER[1]	PACKAGE[2]	PACKAGE SIZE[3]	PROCESSORS	EtherCAT®	LOCKSTEP	FLASH SIZE
TMS320F28P650DK9	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA, CPU2	Yes	Yes	1.28MB
	NMR (nFBGA, 169)	9 mm x 9 mm				
	PTP (HLQFP, 176)	26 mm x 26 mm				
TMS320F28P650DK8[4]	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA, CPU2	–	Yes	
	NMR (nFBGA, 169)	9 mm x 9 mm				
	PTP (HLQFP, 176)	26 mm x 26 mm				
TMS320F28P650DK7[4]	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA, CPU2	Yes	–	
	NMR (nFBGA, 169)	9 mm x 9 mm				
	PTP (HLQFP, 176)	26 mm x 26 mm				
TMS320F28P650SK7[4]	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA	Yes	–	
	NMR (nFBGA, 169)	9 mm x 9 mm				
	PTP (HLQFP, 176)	26 mm x 26 mm				
TMS320F28P659DK8-Q1[4]	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA, CPU2	–	Yes	
	PTP (HLQFP, 176)	26 mm x 26 mm				
	PZP (HTQFP, 100)	16 mm x 16 mm				
TMS320F28P650DK6	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA, CPU2	–	–	
	NMR (nFBGA, 169)	9 mm x 9 mm				
	PTP (HLQFP, 176)	26 mm x 26 mm				
	PZP (HTQFP, 100)	16 mm x 16 mm				
TMS320F28P650SK6[4]	ZEJ (nFBGA, 256)	13 mm x 13 mm	CPU1+CLA	–	–	
	NMR (nFBGA, 169)	9 mm x 9 mm				
	PTP (HLQFP, 176)	26 mm x 26 mm				
	PZP (HTQFP, 100)	16 mm x 16 mm				
TMS320F28P659DH8-Q1[4]	PZP (HTQFP, 100)	16 mm x 16 mm	CPU1+CLA, CPU2	–	Yes	768KB
TMS320F28P659SH6-Q1[4]	PTP (HLQFP, 176)	26 mm x 26 mm	CPU1+CLA	–	–	
	PZP (HTQFP, 100)	16 mm x 16 mm				
TMS320F28P650DH6[4]	PZP (HTQFP, 100)	16 mm x 16 mm	CPU1+CLA, CPU2	–	–	
TMS320F28P650SH7[4]	NMR (nFBGA, 169)	9 mm x 9 mm	CPU1+CLA	Yes	–	
	PTP (HLQFP, 176)	26 mm x 26 mm				
TMS320F28P650SH6[4]	NMR (nFBGA, 169)	9 mm x 9 mm	CPU1+CLA	–	–	
	PTP (HLQFP, 176)	26 mm x 26 mm				
	PZP (HTQFP, 100)	16 mm x 16 mm				

(1) For more information on these devices, see the *Device Comparison* table.
(2) For more information, see the *Mechanical, Packaging, and Orderable Information* section.
(3) The package size (length x width) is a nominal value and includes pins, where applicable.
(4) Preview information (not Production Data).

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3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

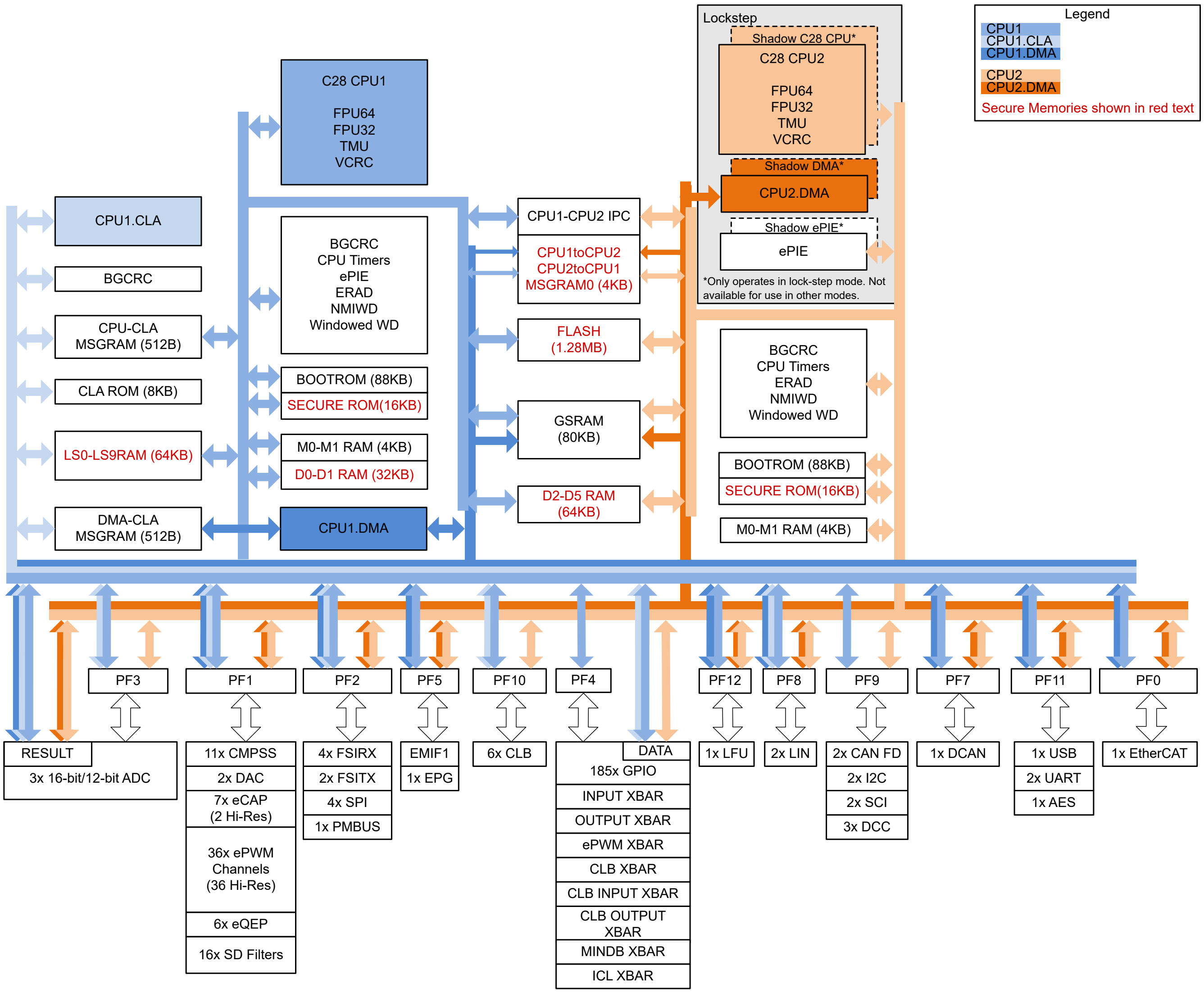

Figure 3-1. Functional Block Diagram

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4 Device Comparison

The *Device Comparison* table lists the features of each F28P65x device.

Table 4-1. Device Comparison

<table>
<tr><th colspan="3">FEATURE(1) (5)</th><th>F28P650DK(6)</th><th>F28P650DH (7)</th><th>F28P650SK (7)</th><th>F28P650SH (7)</th><th>F28P659DK-Q1(7)</th><th>F28P659DH-Q1(7)</th><th>F28P659SH-Q1(7)</th></tr>
<tr><td colspan="10">C28x Subsystem</td></tr>
<tr><td rowspan="6">C28x</td><td colspan="2">Number</td><td colspan="2">2</td><td colspan="2">1</td><td colspan="2">2</td><td>1</td></tr>
<tr><td colspan="2">Frequency (MHz)</td><td colspan="7">200</td></tr>
<tr><td colspan="2">32-bit and 64-bit Floating-Point Unit (FPU)</td><td colspan="7">Yes</td></tr>
<tr><td colspan="2">VCRC</td><td colspan="7">Yes</td></tr>
<tr><td colspan="2">TMU - Type 1</td><td colspan="7">Yes</td></tr>
<tr><td colspan="2">C28x Lockstep (LCM)</td><td>F28P650DK8, F28P650DK9</td><td colspan="3">No</td><td>F28P659DK8-Q1</td><td>F28P659DH8-Q1</td><td>No</td></tr>
<tr><td rowspan="2">CLA - Type 2</td><td colspan="2">Number</td><td colspan="7">1 (available only in CPU1)</td></tr>
<tr><td colspan="2">Frequency (MHz)</td><td colspan="7">200</td></tr>
<tr><td colspan="3">MIPS</td><td colspan="2">600 (CPU1+CLA, CPU2)</td><td colspan="2">400 (CPU1+CLA)</td><td colspan="2">600 (CPU1+CLA, CPU2)</td><td>400 (CPU1+CLA)</td></tr>
<tr><td colspan="3">C28x Flash</td><td>1.28MB</td><td>768KB</td><td>1.28MB</td><td>768KB</td><td>1.28MB</td><td>768KB</td><td>768KB</td></tr>
<tr><td rowspan="4">C28x RAM</td><td colspan="2">Dedicated RAM</td><td colspan="2">104KB</td><td colspan="2">100KB</td><td colspan="2">104KB</td><td>100KB</td></tr>
<tr><td colspan="2">Local Shared RAM</td><td colspan="2">64K</td><td colspan="2">64KB</td><td colspan="2">64KB</td><td>64KB</td></tr>
<tr><td colspan="2">Global Shared RAM</td><td colspan="2">80KB (Shared between CPUs)</td><td colspan="2">80KB</td><td colspan="2">80KB (Shared between CPUs)</td><td>80KB</td></tr>
<tr><td colspan="2">Total RAM</td><td colspan="2">248KB</td><td colspan="2">244KB</td><td colspan="2">248KB</td><td>244KB</td></tr>
<tr><td colspan="3">Background Cyclic Redundancy Check (BGCRC) module - Type 2</td><td colspan="2">3 (1 per CPU and CLA)</td><td colspan="2">2 (1 per CPU and CLA)</td><td colspan="2">3 (1 per CPU and CLA)</td><td>2 (1 per CPU and CLA)</td></tr>
<tr><td colspan="3">Embedded Pattern Generator (EPG) - Type 0</td><td colspan="7">Yes</td></tr>
<tr><td colspan="3">Configurable Logic Block (CLB)</td><td colspan="7">6 tiles</td></tr>
<tr><td colspan="3">32-bit CPU Timers</td><td colspan="2">6 (3 per CPU)</td><td colspan="2">3</td><td colspan="2">6 (3 per CPU)</td><td>3</td></tr>
<tr><td colspan="3">6-Channel DMA - Type 0</td><td colspan="2">2 (1 per CPU)</td><td colspan="2">1</td><td colspan="2">2 (1 per CPU)</td><td>1</td></tr>
<tr><td colspan="3">Security: JTAGLOCK, Zero-pin boot, Dual-zone security</td><td colspan="7">Yes</td></tr>
<tr><td colspan="3">Advanced Encryption Standard (AES) Accelerator</td><td colspan="7">1</td></tr>
<tr><td colspan="3">Embedded Real-time Analysis and Diagnostic (ERAD) - Type 2</td><td colspan="7">Yes</td></tr>
<tr><td rowspan="4">EMIF</td><td rowspan="4">EMIF1 (16-bit or 32-bit)</td><td>256-ball ZEJ</td><td colspan="3" rowspan="3">1</td><td>N/A</td><td>1</td><td rowspan="3">N/A(5)</td><td rowspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td rowspan="2">1</td><td>N/A</td></tr>
<tr><td>176-pin PTP</td><td>1</td><td>1</td></tr>
<tr><td>100-pin PZP</td><td colspan="7">No</td></tr>
<tr><td colspan="3">External Interrupts</td><td colspan="7">5</td></tr>
<tr><td rowspan="21">GPIO</td><td rowspan="4">GPIO</td><td>256-ball ZEJ</td><td colspan="3">163</td><td>N/A</td><td>163</td><td rowspan="3">N/A</td><td rowspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td colspan="4">98</td><td>N/A</td></tr>
<tr><td>176-pin PTP</td><td colspan="5">106</td><td>106</td></tr>
<tr><td>100-pin PZP</td><td colspan="7">49</td></tr>
<tr><td rowspan="4">AGPIO (shared with GPIO and ADC Inputs)</td><td>256-ball ZEJ</td><td colspan="3">22</td><td>N/A</td><td>22</td><td rowspan="3">N/A</td><td rowspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td colspan="4">21</td><td>N/A</td></tr>
<tr><td>176-pin PTP</td><td colspan="5">22</td><td>22</td></tr>
<tr><td>100-pin PZP</td><td colspan="7">11</td></tr>
<tr><td colspan="2">JTAG and Oscillator GPIO</td><td colspan="7">4 (TDI, TDO, X1, X2)</td></tr>
<tr><td rowspan="4">Total GPIO (excluding JTAG and X1.X2)</td><td>256-ball ZEJ</td><td colspan="3">185</td><td>N/A</td><td>185</td><td rowspan="3">N/A</td><td rowspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td colspan="4">119</td><td>N/A</td></tr>
<tr><td>176-pin PTP</td><td colspan="5">128</td><td>128</td></tr>
<tr><td>100-pin PZP</td><td colspan="7">60</td></tr>
<tr><td rowspan="4">AIO (input only)</td><td>256-ball ZEJ</td><td colspan="3">18</td><td>N/A</td><td>18</td><td rowspan="3">N/A</td><td rowspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td colspan="4">13</td><td>N/A</td></tr>
<tr><td>176-pin PTP</td><td colspan="5">14</td><td>14</td></tr>
<tr><td>100-pin PZP</td><td colspan="7">13</td></tr>
<tr><td rowspan="4">Total GPIO and AIO</td><td>256-ball ZEJ</td><td colspan="3">203</td><td>N/A</td><td>203</td><td rowspan="3">N/A</td><td rowspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td colspan="4">132</td><td>N/A</td></tr>
<tr><td>176-pin PTP</td><td colspan="5">142</td><td>142</td></tr>
<tr><td>100-pin PZP</td><td colspan="7">73</td></tr>
</table>

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Table 4-1. Device Comparison (continued)

FEATURE[1] [5]			F28P650DK[6]	F28P650DH [7]	F28P650SK [7]	F28P650SH [7]	F28P659DK-Q1[7]	F28P659DH-Q1[7]	F28P659SH-Q1[7]
Message RAM	CPU1, CPU2		4KB (2KB each direction between CPUs)		–		4KB (2KB each direction between CPUs)		–
	C28x CPUs and CLAs		512 bytes (256 bytes per direction)		512 bytes (256 bytes per direction)		512 bytes (256 bytes per direction)		512 bytes (256 bytes per direction)
	DMAs and CLAs		512 bytes (256 bytes per direction)		512 bytes (256 bytes per direction)		512 bytes (256 bytes per direction)		512 bytes (256 bytes per direction)
Non-maskable Interrupt Watchdog (NMIWD) timers			2 (1 per CPU)		1		2 (1 per CPU)		1
Watchdog (WD) timers			2 (1 per CPU)		1		2 (1 per CPU)		1
C28x Analog Peripherals									
Analog-to-Digital Converter (ADC) (Configurable as 12-bit or 16-bit) - Type 4			3						
ADC 16-bit mode	MSPS		1.19						
	Conversion Time (ns)[2]		840						
ADC 12-bit mode	MSPS		3.92						
	Conversion Time (ns)[2]		255						
ADC Input channels (single-ended mode)		256-ball ZEJ	40			N/A	40	N/A	N/A
		169-ball NMR	34				N/A		
		176-pin PTP	36						36
		100-pin PZP	24						
ADC Input channels (differential mode)		256-ball ZEJ	19			N/A	19	N/A	N/A
		169-ball NMR	17				N/A		
		176-pin PTP	18						18
		100-pin PZP	11						
Temperature Sensor			1						
Comparator subsystem (CMPSS) (each CMPSS has two comparators and two internal DACs) - Type 6			11						
Buffered Digital-to-Analog Converter (DAC) - Type 1			2						
C28x Control Peripherals									
eCAP/HRCAP - Type 3	Total inputs		7						
	High-resolution channels		2 (eCAP6 and eCAP7)						
ePWM/HRPWM - Type 5	Total channels		36						
	High-resolution channels		36						
eQEP modules - Type 2			6						
SDFM channels - Type 2			16						
C28x Communications Peripherals									
Fast Serial Interface (FSI) RX - Type 2			4						
Fast Serial Interface (FSI) TX - Type 2			2						
Inter-Integrated Circuit (I2C) - Type 1			2						
Power Management Bus (PMBus) - Type 0			1						
Local Interconnect Network (LIN) - Type 1 (UART-compatible)			2						
Serial Communications Interface (SCI) (UART-compatible) - Type 0			2						
Serial Peripheral Interface (SPI) - Type 2			4						
Controller Area Network (CAN) 2.0B - Type 0[3]			1						
CAN with Flexible Data-Rate (CAN-FD) - Type 2			2						
Ethernet for Control Automation Technology (EtherCAT)		256-ball ZEJ	F28P650DK9, F28P650DK7	No	F28P650SK7, F28P650SH7		No		
		169-ball NMR							
		176-pin PTP							
		100-pin PZP	No						
High Speed Universal Asynchronous Receiver-Transmitter (UART)			2						
Universal Serial Bus (USB) - Type 0			1						

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Table 4-1. Device Comparison (continued)

<table>
<tr><th colspan="2">FEATURE[1] [5]</th><th>F28P650DK[6]</th><th>F28P650DH [7]</th><th>F28P650SK [7]</th><th>F28P650SH [7]</th><th>F28P659DK-Q1[7]</th><th>F28P659DH-Q1[7]</th><th>F28P659SH-Q1[7]</th></tr>
<tr><td colspan="9">Temperature, Package and Qualification</td></tr>
<tr><td rowspan="4">Package Options[4]</td><td>256-ball ZEJ</td><td rowspan="4" colspan="4">F28P650DH6,F28P650DK9,F28P650DK8,F28P650DK7, F28P650DK6,F28P650SH6 F28P650SH7,F28P650SK7, F28P650SK6</td><td>F28P659DK8-Q1</td><td colspan="2">N/A</td></tr>
<tr><td>169-ball NMR</td><td colspan="3">N/A</td></tr>
<tr><td>176-pin PTP</td><td>F28P659DK8-Q1</td><td>N/A</td><td>F28P659SH6-Q1</td></tr>
<tr><td>100-pin PZP</td><td colspan="3">F28P659DK8-Q1,F28P659DH8-Q1, F28P659SH6-Q1</td></tr>
<tr><td colspan="2">Junction temperature (T_J)</td><td colspan="7">–40°C to 150°C</td></tr>
<tr><td colspan="2">Free-Air temperature (T_A)</td><td colspan="7">–40°C to 125°C</td></tr>
</table>

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the *C2000 Real-Time Control MCU Peripherals Reference Guide*.
(2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
(3) The CAN module uses the IP known as DCAN. This document uses the names CAN and DCAN interchangeably to reference this peripheral.
(4) The suffix -Q1 refers to AEC Q100 qualification for automotive applications.
(5) "N/A" on the feature entry indicates that the corresponding package type in not available.
(6) Information on the TMS320F28P650DK**9** and TMS320F28P650DK**6** devices is Production Data.
Information on the TMS320F28P650DK**7** and TMS320F28P650DK**8** devices is preview information only (not Production Data).
(7) Preview information (not Production Data).

4.1 Related Products

TMS320F2837xD Real-Time Dual-Core Microcontrollers
The F2837xD series sets a new standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU accelerators. New capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

TMS320F2837xS Real-Time Microcontrollers
The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the TMS320F2807x series.

TMS320F2838x Real-Time Microcontrollers
The F2838x series offers more performance, larger pin counts, flash memory sizes, peripheral and wide variety of connectivity options. The F2838x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

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5 Pin Configuration and Functions

5.1 Pin Diagrams

Figure 5-1 shows the ball assignments on the 256-ball ZEJ New Fine Pitch Ball Grid Array (nFBGA). Figure 5-2 to Figure 5-5 show the ball assignments on the 256-ball ZEJ nFBGA in quadrants.

Figure 5-6 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack.

Figure 5-7 shows the ball assignments on the 169-ball NMR nFGBA. Figure 5-8 to Figure 5-11 show the ball assignments on the 167-ball NMR nFBGA in quadrants.

Figure 5-12 shows the pin assignments on the 100-pin PZP PowerPAD Thermally Enhanced Thin Quad Flatpack.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T	VSSA	B0/VDAC	B1/DACC_OUT	VREFLOB	VSSA	VDDA	A9, GPIO212	A10, GPIO213	GPIO126	GPIO130	VDD3VFL	GPIO222/ TDI	TMS	GPIO132	VDDIO	VSS
R	A14/B14/ C14	A15/B15/ C15	B2	VREFHIB	B13	A8, GPIO211	B10, GPIO219	A11, GPIO214	GPIO127	GPIO33	VDD3VFL	GPIO223/ TDO	TCK	GPIO134	GPIO41	GPIO48
P	A0/DACA_OUT	A1	B3	B11	B7, GPIO208	A7, GPIO210	B4, GPIO215	B8, GPIO217	GPIO115	GPIO34	GPIO29	GPIO36	GPIO40	GPIO50	GPIO49	GPIO224/ ERRORSTS
N	VDDA	VSSA	A2	A3	B6, GPIO207	A6, GPIO209	B5, GPIO216	B9, GPIO218	GPIO101	GPIO35	GPIO28	GPIO37	GPIO131	GPIO51	GPIO52	GPIO53
M	VREFLOA	VREFHIA	VSSA	A4	A5	C4, GPIO205	GPIO123	GPIO125	GPIO128	GPIO119	GPIO120	GPIO38	GPIO54	GPIO55	GPIO56	GPIO57
L	VREFLOC	VREFHIC	C10	C2	C3, GPIO206	C5, GPIO204	GPIO122	GPIO124	GPIO129	GPIO30	GPIO26	GPIO39	GPIO58	GPIO59	GPIO60	GPIO105
K	C13	C11	C8, GPIO202	C7, GPIO198	C6, GPIO203	VSS	VDDIO	VDD	VDD	VDDIO	GPIO66	GPIO65	GPIO64	GPIO63	GPIO62	GPIO61
J	C1, GPIO200	C9, GPIO201	GPIO113	GPIO114	VDDIO	VSS	VSS	VSS	VSS	VDDIO	VDD	GPIO44	GPIO45	GPIO32	GPIO133	VREGENZ
H	C0, GPIO199	GPIO110	GPIO111	GPIO112	VDDIO	VSS	VSS	VSS	VSS	VSS	GPIO116	GPIO147	GPIO141	GPIO142	GPIO145	GPIO146
G	GPIO23	GPIO108	GPIO109	GPIO12	VSS	VDD	VDDIO	VDDIO	VSS	VSS	VSS	GPIO103	GPIO27	XRSn	VDDOSC	GPIO221, X2
F	GPIO106	GPIO107	GPIO18	GPIO100	GPIO168	GPIO165	GPIO6	GPIO0	VDD	VDD	GPIO151	GPIO81	GPIO77	GPIO46	VSSOSC	GPIO220, X1
E	GPIO9	GPIO98	GPIO17	GPIO11	GPIO167	GPIO91	GPIO5	GPIO24	GPIO161	GPIO157	GPIO152	GPIO82	GPIO78	GPIO47	VDDIO	GPIO42
D	GPIO8	GPIO21	GPIO16	GPIO10	GPIO94	GPIO90	GPIO4	GPIO31	GPIO84	GPIO158	GPIO153	GPIO83	GPIO79	GPIO73	GPIO67	GPIO43
C	GPIO99	GPIO20	GPIO15	GPIO97	GPIO93	GPIO89	GPIO3	GPIO164	GPIO85	GPIO159	GPIO154	GPIO148	GPIO102	GPIO74	GPIO70	GPIO68
B	VDDIO	GPIO19	GPIO14	GPIO96	GPIO166	GPIO88	GPIO2	GPIO163	GPIO86	GPIO160	GPIO155	GPIO149	GPIO104	GPIO75	GPIO71	GPIO69
A	VSS	GPIO22	GPIO13	GPIO95	GPIO92	GPIO7	GPIO1	GPIO162	GPIO87	GPIO25	GPIO156	GPIO150	GPIO80	GPIO76	GPIO72	VSS

Not to scale

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-1. 256-Ball ZEJ New Fine Pitch Ball Grid Array (Bottom View)

	1	2	3	4	5	6	7	8
T	VSSA	B0/VDAC	B1/DACC _OUT	VREFLOB	VSSA	VDDA	A9, GPIO212	A10, GPIO213
R	A14/B14/ C14	A15/B15/ C15	B2	VREFHIB	B13	A8, GPIO211	B10, GPIO219	A11, GPIO214
P	A0/DACA _OUT	A1	B3	B11	B7, GPIO208	A7, GPIO210	B4, GPIO215	B8, GPIO217
N	VDDA	VSSA	A2	A3	B6, GPIO207	A6, GPIO209	B5, GPIO216	B9, GPIO218
M	VREFLOA	VREFHIA	VSSA	A4	A5	C4, GPIO205	GPIO123	GPIO125
L	VREFLOC	VREFHIC	C10	C2	C3, GPIO206	C5, GPIO204	GPIO122	GPIO124
K	C13	C11	C8, GPIO202	C7, GPIO198	C6, GPIO203	VSS	VDDIO	VDD
J	C1, GPIO200	C9, GPIO201	GPIO113	GPIO114	VDDIO	VSS	VSS	VSS
H	C0, GPIO199	GPIO110	GPIO111	GPIO112	VDDIO	VSS	VSS	VSS

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-2. 256-Ball ZEJ New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 1]

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	9	10	11	12	13	14	15	16
T	GPIO126	GPIO130	VDD3VFL	GPIO222/ TDI	TMS	GPIO132	VDDIO	VSS
R	GPIO127	GPIO33	VDD3VFL	GPIO223/ TDO	TCK	GPIO134	GPIO41	GPIO48
P	GPIO115	GPIO34	GPIO29	GPIO36	GPIO40	GPIO50	GPIO49	GPIO224/ ERRORSTS
N	GPIO101	GPIO35	GPIO28	GPIO37	GPIO131	GPIO51	GPIO52	GPIO53
M	GPIO128	GPIO119	GPIO120	GPIO38	GPIO54	GPIO55	GPIO56	GPIO57
L	GPIO129	GPIO30	GPIO26	GPIO39	GPIO58	GPIO59	GPIO60	GPIO105
K	VDD	VDDIO	GPIO66	GPIO65	GPIO64	GPIO63	GPIO62	GPIO61
J	VSS	VDDIO	VDD	GPIO44	GPIO45	GPIO32	GPIO133	VREGENZ
H	VSS	VSS	GPIO116	GPIO147	GPIO141	GPIO142	GPIO145	GPIO146

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-3. 256-Ball ZEJ New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 2]

	1	2	3	4	5	6	7	8
G	GPIO23	GPIO108	GPIO109	GPIO12	VSS	VDD	VDDIO	VDDIO
F	GPIO106	GPIO107	GPIO18	GPIO100	GPIO168	GPIO165	GPIO6	GPIO0
E	GPIO9	GPIO98	GPIO17	GPIO11	GPIO167	GPIO91	GPIO5	GPIO24
D	GPIO8	GPIO21	GPIO16	GPIO10	GPIO94	GPIO90	GPIO4	GPIO31
C	GPIO99	GPIO20	GPIO15	GPIO97	GPIO93	GPIO89	GPIO3	GPIO164
B	VDDIO	GPIO19	GPIO14	GPIO96	GPIO166	GPIO88	GPIO2	GPIO163
A	VSS	GPIO22	GPIO13	GPIO95	GPIO92	GPIO7	GPIO1	GPIO162

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-4. 256-Ball ZEJ New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 3]

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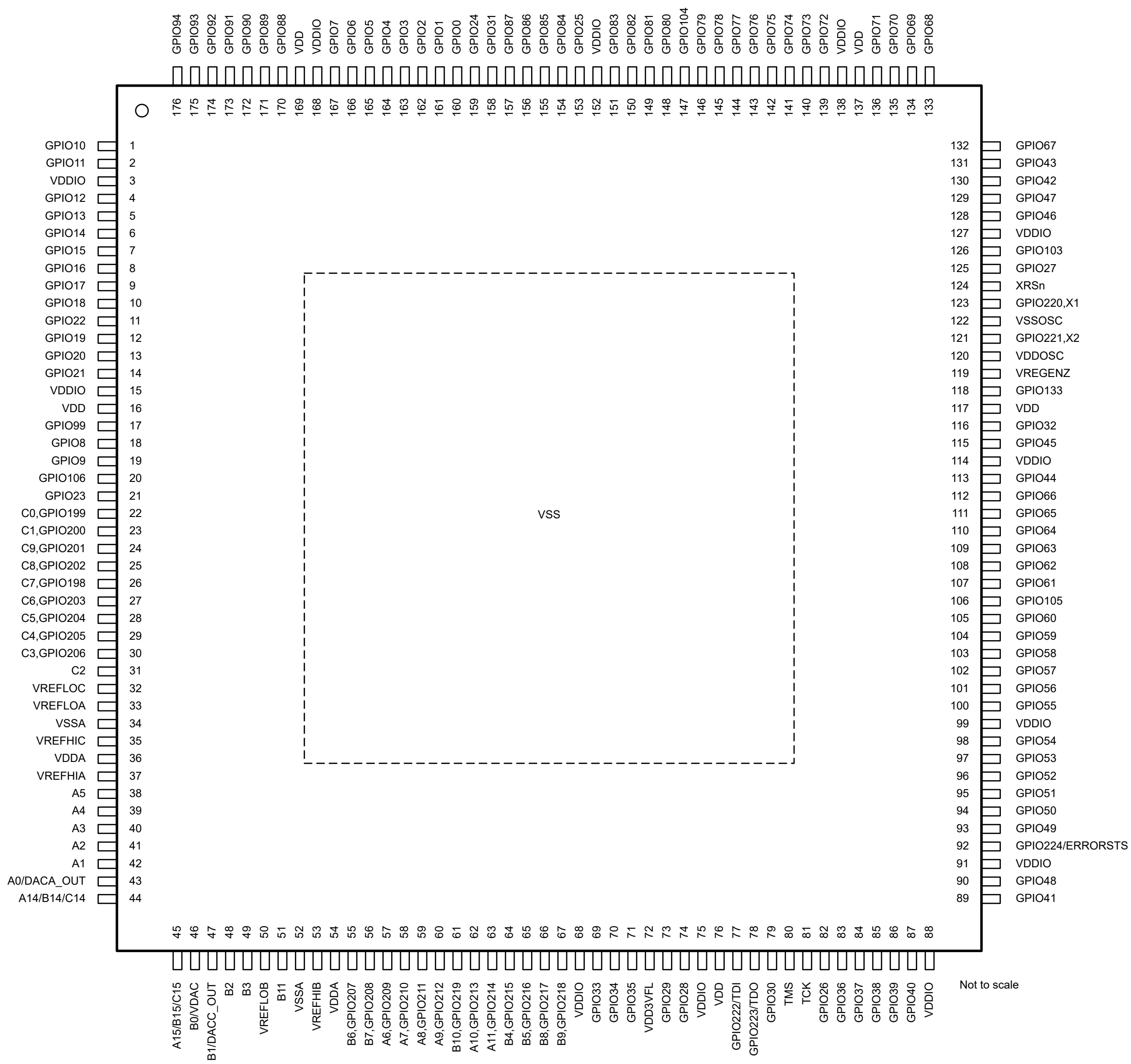
	9	10	11	12	13	14	15	16
G	VSS	VSS	VSS	GPIO103	GPIO27	XRSn	VDDOSC	GPIO221, X2
F	VDD	VDD	GPIO151	GPIO81	GPIO77	GPIO46	VSSOSC	GPIO220, X1
E	GPIO161	GPIO157	GPIO152	GPIO82	GPIO78	GPIO47	VDDIO	GPIO42
D	GPIO84	GPIO158	GPIO153	GPIO83	GPIO79	GPIO73	GPIO67	GPIO43
C	GPIO85	GPIO159	GPIO154	GPIO148	GPIO102	GPIO74	GPIO70	GPIO68
B	GPIO86	GPIO160	GPIO155	GPIO149	GPIO104	GPIO75	GPIO71	GPIO69
A	GPIO87	GPIO25	GPIO156	GPIO150	GPIO80	GPIO76	GPIO72	VSS

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-5. 256-Ball ZEJ New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 4]



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-6. 176-Pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack (Top View)

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	1	2	3	4	5	6	7	8	9	10	11	12	13
N	VSSA	B0/VDAC	B1/DACC _OUT	VREFLOB	VSSA	B5, GPIO216	B9, GPIO218	GPIO35	GPIO222/ TDI	TMS	GPIO36	GPIO40	VSS
M	A14/B14/ C14	A15/B15/ C15	B2	VREFHIB	VDDA	B4, GPIO215	B8, GPIO217	VDD3VFL	GPIO223/ TDO	TCK	GPIO37	GPIO41	GPIO48
L	VSSA	VDDA	A0/DACA _OUT	B3	A10, GPIO213	A11, GPIO214	GPIO33	GPIO29	GPIO30	GPIO26	GPIO38	GPIO224/ ERRORSTS	GPIO49
K	VREFLOA	VREFHIA	A1	B7, GPIO208	A7, GPIO210	A9, GPIO212	GPIO34	GPIO28	GPIO50	GPIO51	GPIO52	GPIO53	GPIO54
J	VREFLOC	VREFHIC	A2	B6, GPIO207	A6, GPIO209	A8, GPIO211	VSS	VDDIO	VDD	GPIO58	GPIO57	GPIO56	GPIO55
H	A5	A4	A3	C2	C3, GPIO206	C4, GPIO205	VSS	VSS	VDDIO	GPIO62	GPIO61	GPIO105	GPIO59
G	C1, GPIO200	C9, GPIO201	C8, GPIO202	C7, GPIO198	C6, GPIO203	C5, GPIO204	VSS	VSS	VDD	GPIO66	GPIO65	GPIO64	GPIO63
F	C0, GPIO199	GPIO23	GPIO9	VDDIO	VDD	VDDIO	VDD	VDDIO	VSS	GPIO44	GPIO45	GPIO32	GPIO133
E	GPIO20	GPIO21	GPIO8	GPIO99	GPIO90	GPIO5	GPIO0	GPIO80	GPIO76	VREGENZ	VDDOSC	VSSOSC	GPIO221, X2
D	GPIO19	GPIO22	GPIO18	GPIO17	GPIO89	GPIO4	GPIO24	GPIO82	GPIO77	GPIO103	GPIO27	XRSn	GPIO220, X1
C	GPIO13	GPIO14	GPIO15	GPIO16	GPIO88	GPIO3	GPIO87	GPIO83	GPIO78	GPIO73	GPIO43	GPIO42	VDDIO
B	GPIO12	GPIO11	GPIO10	GPIO91	GPIO7	GPIO2	GPIO86	GPIO25	GPIO79	GPIO74	GPIO71	GPIO69	GPIO68
A	VSS	GPIO94	GPIO93	GPIO92	GPIO6	GPIO1	GPIO85	GPIO84	GPIO104	GPIO75	GPIO72	GPIO70	VSS

Not to scale

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-7. 169-Ball NMR New Fine Pitch Ball Grid Array (Bottom View)

	1	2	3	4	5	6	7
N	VSSA	B0/VDAC	B1/DACC _OUT	VREFLOB	VSSA	B5, GPIO216	B9, GPIO218
M	A14/B14/ C14	A15/B15/ C15	B2	VREFHIB	VDDA	B4, GPIO215	B8, GPIO217
L	VSSA	VDDA	A0/DACA _OUT	B3	A10, GPIO213	A11, GPIO214	GPIO33
K	VREFLOA	VREFHIA	A1	B7, GPIO208	A7, GPIO210	A9, GPIO212	GPIO34
J	VREFLOC	VREFHIC	A2	B6, GPIO207	A6, GPIO209	A8, GPIO211	VSS
H	A5	A4	A3	C2	C3, GPIO206	C4, GPIO205	VSS
G	C1, GPIO200	C9, GPIO201	C8, GPIO202	C7, GPIO198	C6, GPIO203	C5, GPIO204	VSS

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-8. 169-Ball NMR New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 1]

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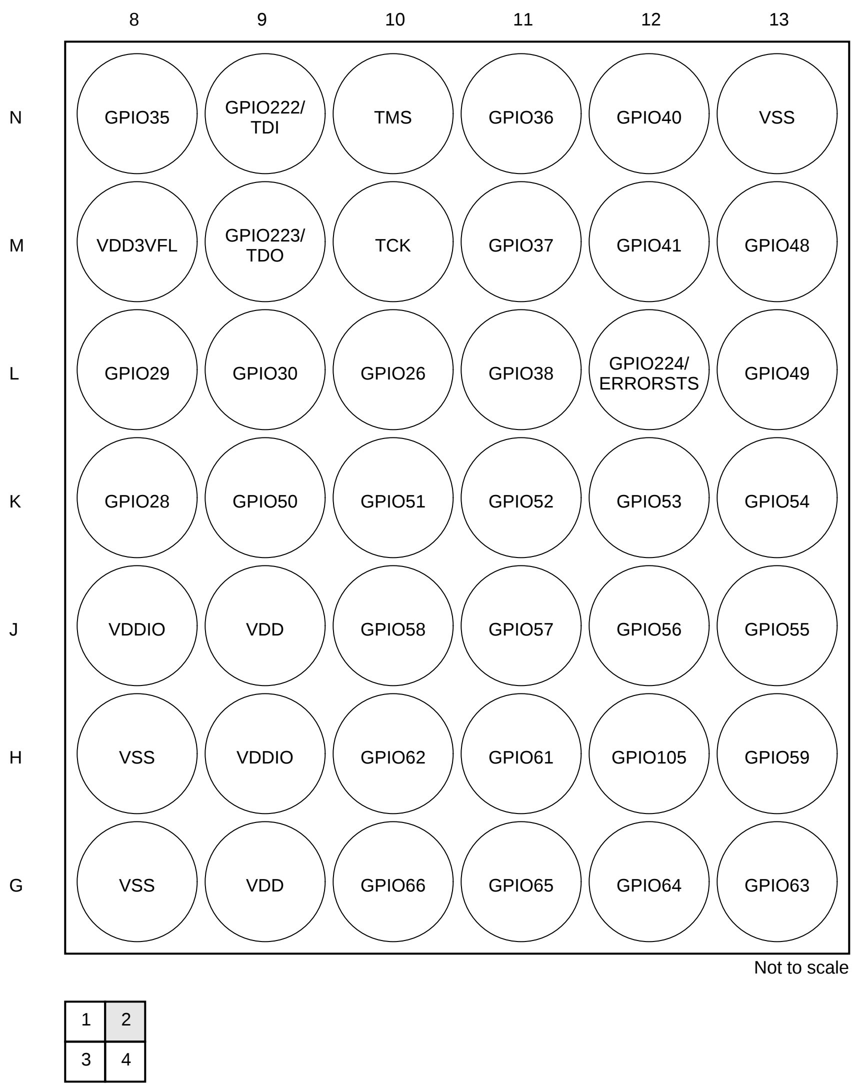
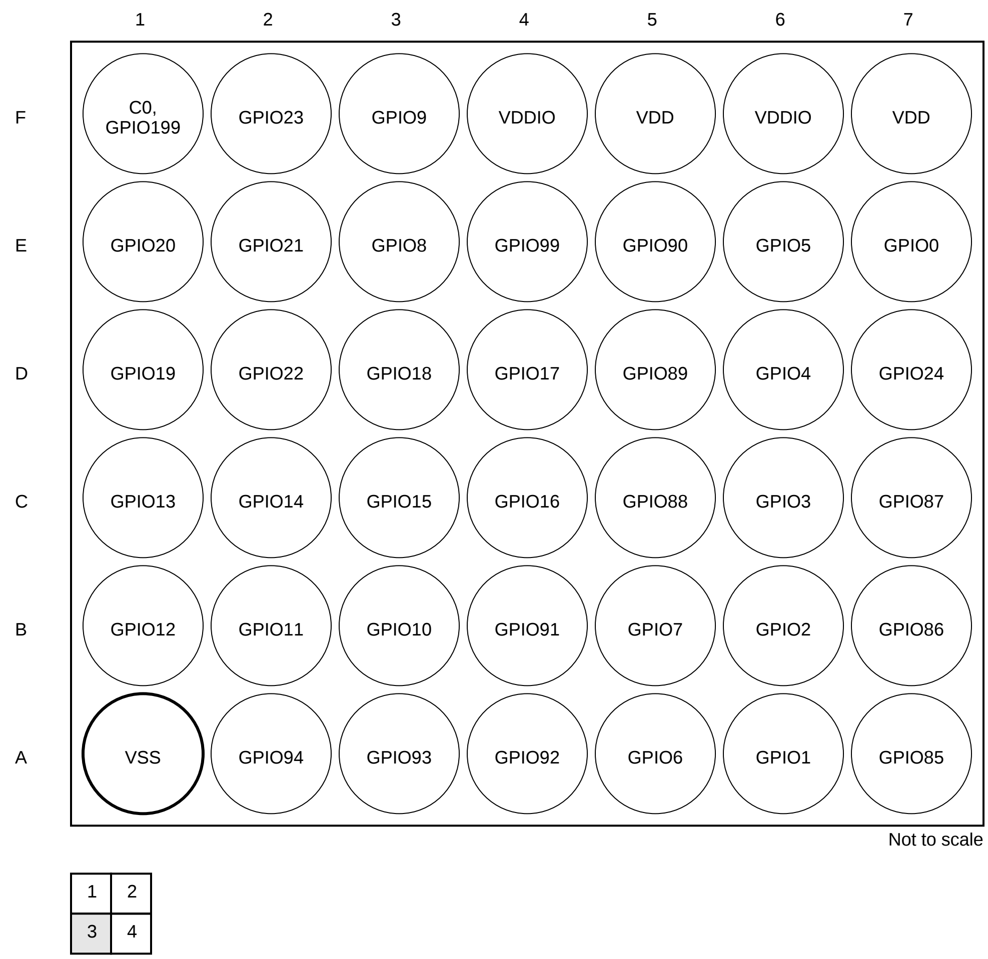


A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-9. 169-Ball NMR New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 2]



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-10. 169-Ball NMR New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 3]

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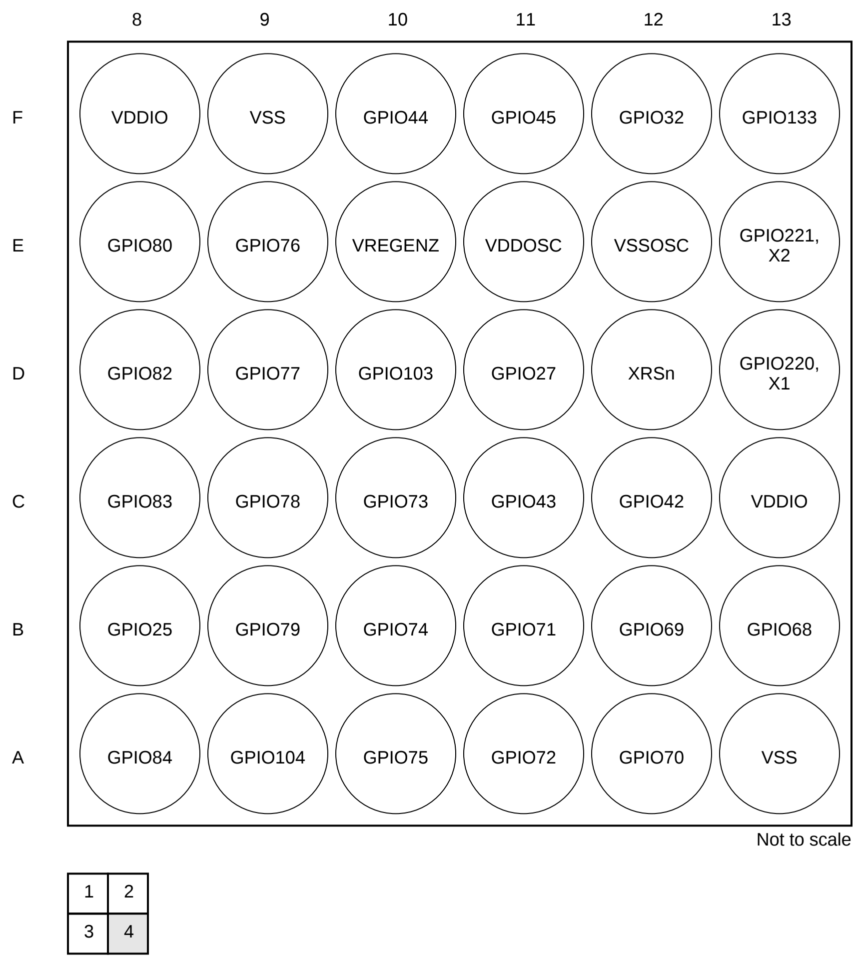

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-11. 169-Ball NMR New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 4]

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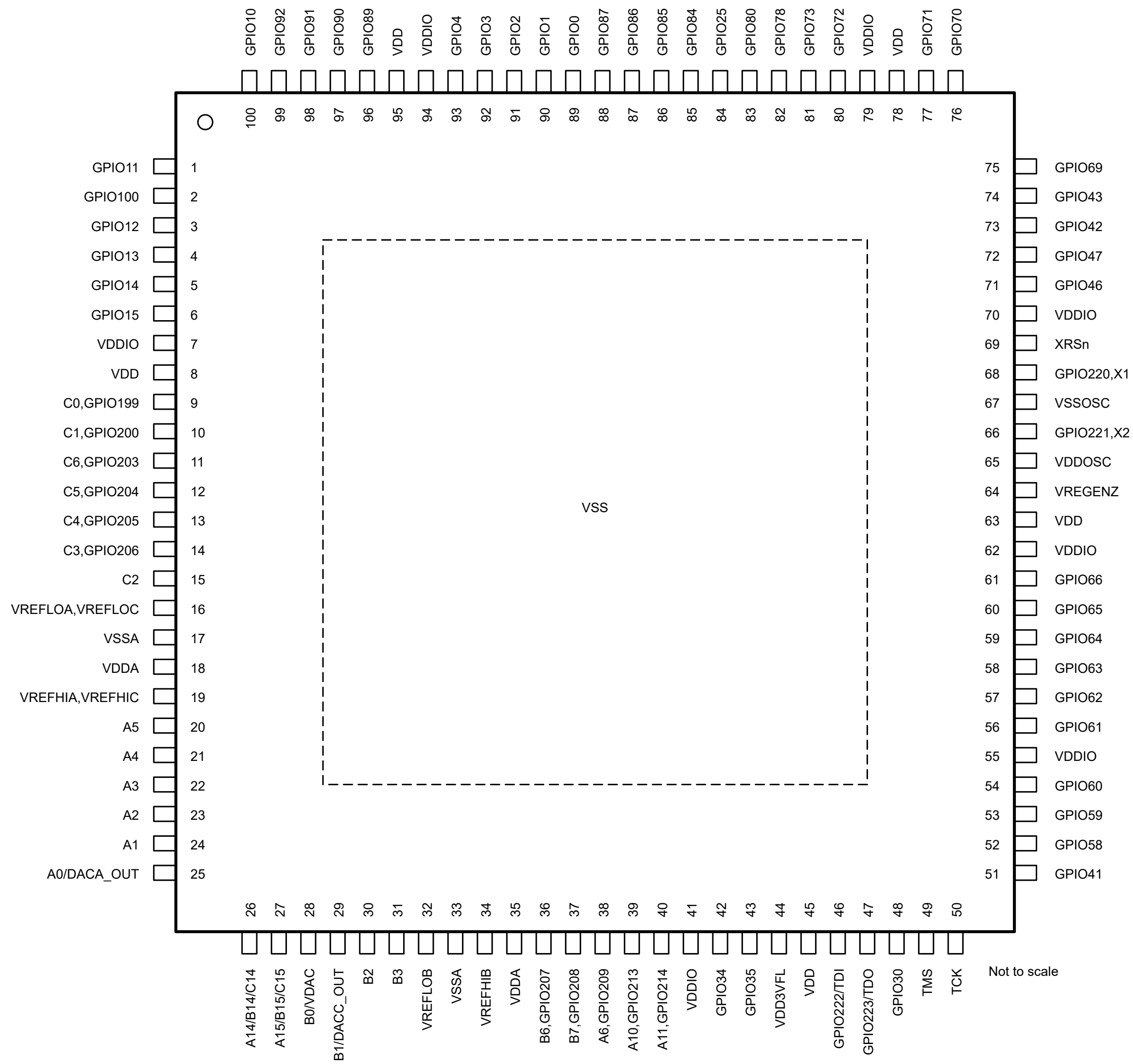

A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-12. 100-Pin PZP PowerPAD™ Thermally Enhanced Thin Quad Flatpack (Top View)

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5.2 Pin Attributes

Table 5-1. Pin Attributes

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
				ANALOG			
A0		P1	43	L3	25	I	ADC-A Input 0
CMP1_HP1						I	CMPSS-1 High Comparator Positive Input 1
CMP1_LP1						I	CMPSS-1 Low Comparator Positive Input 1
CMP9_HN0						I	CMPSS-9 High Comparator Negative Input 0
CMP9_LN0						I	CMPSS-9 Low Comparator Negative Input 0
DACA_OUT						O	Buffered DAC-A Output.
AIO227	0, 4, 8, 12					I	Analog Pin Used For Digital Input 227
A1		P2	42	K3	24	I	ADC-A Input 1
CMP1_HN1						I	CMPSS-1 High Comparator Negative Input 1
CMP1_HP2						I	CMPSS-1 High Comparator Positive Input 2
CMP1_LN1						I	CMPSS-1 Low Comparator Negative Input 1
CMP1_LP2						I	CMPSS-1 Low Comparator Positive Input 2
AIO228	0, 4, 8, 12					I	Analog Pin Used For Digital Input 228
A2		N3	41	J3	23	I	ADC-A Input 2
CMP1_HP0						I	CMPSS-1 High Comparator Positive Input 0
CMP1_LP0						I	CMPSS-1 Low Comparator Positive Input 0
CMP2_HN1						I	CMPSS-2 High Comparator Negative Input 1
CMP2_LN1						I	CMPSS-2 Low Comparator Negative Input 1
AIO229	0, 4, 8, 12					I	Analog Pin Used For Digital Input 229
A3		N4	40	H3	22	I	ADC-A Input 3
CMP1_HN0						I	CMPSS-1 High Comparator Negative Input 0
CMP1_HP3						I	CMPSS-1 High Comparator Positive Input 3
CMP1_LN0						I	CMPSS-1 Low Comparator Negative Input 0
AIO230	0, 4, 8, 12					I	Analog Pin Used For Digital Input 230
A4		M4	39	H2	21	I	ADC-A Input 4
CMP2_HP0						I	CMPSS-2 High Comparator Positive Input 0
CMP2_LP0						I	CMPSS-2 Low Comparator Positive Input 0
AIO231	0, 4, 8, 12					I	Analog Pin Used For Digital Input 231
A5		M5	38	H1	20	I	ADC-A Input 5
CMP2_HN0						I	CMPSS-2 High Comparator Negative Input 0
CMP2_HP3						I	CMPSS-2 High Comparator Positive Input 3
CMP2_LN0						I	CMPSS-2 Low Comparator Negative Input 0
CMP9_LP2						I	CMPSS-9 Low Comparator Positive Input 2
AIO232	0, 4, 8, 12					I	Analog Pin Used For Digital Input 232
A6		N6	57	J5	38	I	ADC-A Input 6
CMP7_HP0						I	CMPSS-7 High Comparator Positive Input 0
CMP7_LP0						I	CMPSS-7 Low Comparator Positive Input 0
GPIO209						I/O	General-Purpose Input Output 209 This pin also has digital mux functions which are described in the GPIO section of this table.
A7		P6	58	K5		I	ADC-A Input 7
CMP4_LP3						I	CMPSS-4 Low Comparator Positive Input 3
CMP7_HN0						I	CMPSS-7 High Comparator Negative Input 0
CMP7_LN0						I	CMPSS-7 Low Comparator Negative Input 0
CMP9_HP2						I	CMPSS-9 High Comparator Positive Input 2
GPIO210						I/O	General-Purpose Input Output 210 This pin also has digital mux functions which are described in the GPIO section of this table.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
A8		R6	59	J6		I	ADC-A Input 8
CMP8_HP0						I	CMPSS-8 High Comparator Positive Input 0
CMP8_LP0						I	CMPSS-8 Low Comparator Positive Input 0
GPIO211						I/O	General-Purpose Input Output 211 This pin also has digital mux functions which are described in the GPIO section of this table.
A9		T7	60	K6		I	ADC-A Input 9
CMP5_LP3						I	CMPSS-5 Low Comparator Positive Input 3
CMP8_HN0						I	CMPSS-8 High Comparator Negative Input 0
CMP8_LN0						I	CMPSS-8 Low Comparator Negative Input 0
GPIO212						I/O	General-Purpose Input Output 212 This pin also has digital mux functions which are described in the GPIO section of this table.
A10		T8	62	L5	39	I	ADC-A Input 10
CMP8_HN1						I	CMPSS-8 High Comparator Negative Input 1
CMP8_HP1						I	CMPSS-8 High Comparator Positive Input 1
CMP8_LN1						I	CMPSS-8 Low Comparator Negative Input 1
CMP8_LP1						I	CMPSS-8 Low Comparator Positive Input 1
GPIO213						I/O	General-Purpose Input Output 213 This pin also has digital mux functions which are described in the GPIO section of this table.
A11		R8	63	L6	40	I	ADC-A Input 11
CMP8_HP2						I	CMPSS-8 High Comparator Positive Input 2
CMP8_LP2						I	CMPSS-8 Low Comparator Positive Input 2
GPIO214						I/O	General-Purpose Input Output 214 This pin also has digital mux functions which are described in the GPIO section of this table.
A14		R1	44	M1	26	I	ADC-A Input 14
B14						I	ADC-B Input 14
C14						I	ADC-C Input 14
CMP4_HP0						I	CMPSS-4 High Comparator Positive Input 0
CMP4_LP0						I	CMPSS-4 Low Comparator Positive Input 0
AIO225	0, 4, 8, 12					I	Analog Pin Used For Digital Input 225
A15		R2	45	M2	27	I	ADC-A Input 15
B15						I	ADC-B Input 15
C15						I	ADC-C Input 15
CMP4_HN0						I	CMPSS-4 High Comparator Negative Input 0
CMP4_HP3						I	CMPSS-4 High Comparator Positive Input 3
CMP4_LN0						I	CMPSS-4 Low Comparator Negative Input 0
AIO226	0, 4, 8, 12					I	Analog Pin Used For Digital Input 226
B0		T2	46	N2	28	I	ADC-B Input 0
CMP3_HP1						I	CMPSS-3 High Comparator Positive Input 1
CMP3_LP1						I	CMPSS-3 Low Comparator Positive Input 1
CMP11_HN0						I	CMPSS-11 High Comparator Negative Input 0
CMP11_LN0						I	CMPSS-11 Low Comparator Negative Input 0
VDAC						I	Optional external reference voltage for on-chip DACs.
AIO233	0, 4, 8, 12					I	Analog Pin Used For Digital Input 233
B1		T3	47	N3	29	I	ADC-B Input 1
CMP3_HP2						I	CMPSS-3 High Comparator Positive Input 2
CMP3_LP2						I	CMPSS-3 Low Comparator Positive Input 2
DACC_OUT						O	Buffered DAC-C Output.
AIO234	0, 4, 8, 12					I	Analog Pin Used For Digital Input 234

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
B2		R3	48	M3	30	I	ADC-B Input 2
CMP3_HP0						I	CMPSS-3 High Comparator Positive Input 0
CMP3_LP0						I	CMPSS-3 Low Comparator Positive Input 0
AIO235	0, 4, 8, 12					I	Analog Pin Used For Digital Input 235
B3		P3	49	L4	31	I	ADC-B Input 3
CMP1_LP3						I	CMPSS-1 Low Comparator Positive Input 3
CMP3_HN0						I	CMPSS-3 High Comparator Negative Input 0
CMP3_LN0						I	CMPSS-3 Low Comparator Negative Input 0
AIO236	0, 4, 8, 12					I	Analog Pin Used For Digital Input 236
B4		P7	64	M6		I	ADC-B Input 4
CMP5_HN1						I	CMPSS-5 High Comparator Negative Input 1
CMP5_HP1						I	CMPSS-5 High Comparator Positive Input 1
CMP5_LN1						I	CMPSS-5 Low Comparator Negative Input 1
CMP5_LP1						I	CMPSS-5 Low Comparator Positive Input 1
GPIO215						I/O	General-Purpose Input Output 215 This pin also has digital mux functions which are described in the GPIO section of this table.
B5		N7	65	N6		I	ADC-B Input 5
CMP5_HP2						I	CMPSS-5 High Comparator Positive Input 2
CMP5_LP2						I	CMPSS-5 Low Comparator Positive Input 2
GPIO216						I/O	General-Purpose Input Output 216 This pin also has digital mux functions which are described in the GPIO section of this table.
B6		N5	55	J4	36	I	ADC-B Input 6
CMP7_HN1						I	CMPSS-7 High Comparator Negative Input 1
CMP7_HP1						I	CMPSS-7 High Comparator Positive Input 1
CMP7_LN1						I	CMPSS-7 Low Comparator Negative Input 1
CMP7_LP1						I	CMPSS-7 Low Comparator Positive Input 1
GPIO207						I/O	General-Purpose Input Output 207 This pin also has digital mux functions which are described in the GPIO section of this table.
B7		P5	56	K4	37	I	ADC-B Input 7
CMP3_HN1						I	CMPSS-3 High Comparator Negative Input 1
CMP3_LN1						I	CMPSS-3 Low Comparator Negative Input 1
CMP7_HP2						I	CMPSS-7 High Comparator Positive Input 2
CMP7_LP2						I	CMPSS-7 Low Comparator Positive Input 2
GPIO208						I/O	General-Purpose Input Output 208 This pin also has digital mux functions which are described in the GPIO section of this table.
B8		P8	66	M7		I	ADC-B Input 8
CMP2_HP1						I	CMPSS-2 High Comparator Positive Input 1
CMP2_LP1						I	CMPSS-2 Low Comparator Positive Input 1
CMP10_HN0						I	CMPSS-10 High Comparator Negative Input 0
CMP10_LN0						I	CMPSS-10 Low Comparator Negative Input 0
GPIO217						I/O	General-Purpose Input Output 217 This pin also has digital mux functions which are described in the GPIO section of this table.

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
B9		N8	67	N7		I	ADC-B Input 9
CMP2_HP2						I	CMPSS-2 High Comparator Positive Input 2
CMP2_LP2						I	CMPSS-2 Low Comparator Positive Input 2
CMP9_HN1						I	CMPSS-9 High Comparator Negative Input 1
CMP9_LN1						I	CMPSS-9 Low Comparator Negative Input 1
GPIO218						I/O	General-Purpose Input Output 218 This pin also has digital mux functions which are described in the GPIO section of this table.
B10		R7	61			I	ADC-B Input 10
CMP4_HN1						I	CMPSS-4 High Comparator Negative Input 1
CMP4_HP1						I	CMPSS-4 High Comparator Positive Input 1
CMP4_LN1						I	CMPSS-4 Low Comparator Negative Input 1
CMP4_LP1						I	CMPSS-4 Low Comparator Positive Input 1
GPIO219						I/O	General-Purpose Input Output 219 This pin also has digital mux functions which are described in the GPIO section of this table.
B11		P4	51			I	ADC-B Input 11
CMP4_HP2						I	CMPSS-4 High Comparator Positive Input 2
CMP4_LP2						I	CMPSS-4 Low Comparator Positive Input 2
AIO240	0, 4, 8, 12					I	Analog Pin Used For Digital Input 240
B13		R5				I	ADC-B Input 13
CMP9_HP0						I	CMPSS-9 High Comparator Positive Input 0
CMP9_LP0						I	CMPSS-9 Low Comparator Positive Input 0
AIO238	0, 4, 8, 12					I	Analog Pin Used For Digital Input 238
C0		H1	22	F1	9	I	ADC-C Input 0
CMP6_HN1						I	CMPSS-6 High Comparator Negative Input 1
CMP6_HP1						I	CMPSS-6 High Comparator Positive Input 1
CMP6_LN1						I	CMPSS-6 Low Comparator Negative Input 1
CMP6_LP1						I	CMPSS-6 Low Comparator Positive Input 1
GPIO199						I/O	General-Purpose Input Output 199 This pin also has digital mux functions which are described in the GPIO section of this table.
C1		J1	23	G1	10	I	ADC-C Input 1
CMP6_HP2						I	CMPSS-6 High Comparator Positive Input 2
CMP6_LP2						I	CMPSS-6 Low Comparator Positive Input 2
GPIO200						I/O	General-Purpose Input Output 200 This pin also has digital mux functions which are described in the GPIO section of this table.
C2		L4	31	H4	15	I	ADC-C Input 2
CMP6_HP0						I	CMPSS-6 High Comparator Positive Input 0
CMP6_LP0						I	CMPSS-6 Low Comparator Positive Input 0
AIO237	0, 4, 8, 12					I	Analog Pin Used For Digital Input 237
C3		L5	30	H5	14	I	ADC-C Input 3
CMP3_LP3						I	CMPSS-3 Low Comparator Positive Input 3
CMP6_HN0						I	CMPSS-6 High Comparator Negative Input 0
CMP6_LN0						I	CMPSS-6 Low Comparator Negative Input 0
GPIO206						I/O	General-Purpose Input Output 206 This pin also has digital mux functions which are described in the GPIO section of this table.

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
C4		M6	29	H6	13	I	ADC-C Input 4
CMP5_HP0						I	CMPSS-5 High Comparator Positive Input 0
CMP5_LP0						I	CMPSS-5 Low Comparator Positive Input 0
CMP10_HN1						I	CMPSS-10 High Comparator Negative Input 1
CMP10_LN1						I	CMPSS-10 Low Comparator Negative Input 1
GPIO205						I/O	General-Purpose Input Output 205 This pin also has digital mux functions which are described in the GPIO section of this table.
C5		L6	28	G6	12	I	ADC-C Input 5
CMP2_LP3						I	CMPSS-2 Low Comparator Positive Input 3
CMP5_HN0						I	CMPSS-5 High Comparator Negative Input 0
CMP5_LN0						I	CMPSS-5 Low Comparator Negative Input 0
GPIO204						I/O	General-Purpose Input Output 204 This pin also has digital mux functions which are described in the GPIO section of this table.
C6		K5	27	G5	11	I	ADC-C Input 6
CMP10_HP1						I	CMPSS-10 High Comparator Positive Input 1
CMP10_LP1						I	CMPSS-10 Low Comparator Positive Input 1
GPIO203						I/O	General-Purpose Input Output 203 This pin also has digital mux functions which are described in the GPIO section of this table.
C7		K4	26	G4		I	ADC-C Input 7
CMP11_HP1						I	CMPSS-11 High Comparator Positive Input 1
CMP11_LP1						I	CMPSS-11 Low Comparator Positive Input 1
GPIO198						I/O	General-Purpose Input Output 198 This pin also has digital mux functions which are described in the GPIO section of this table.
C8		K3	25	G3		I	ADC-C Input 8
CMP10_HP2						I	CMPSS-10 High Comparator Positive Input 2
CMP10_LP2						I	CMPSS-10 Low Comparator Positive Input 2
GPIO202						I/O	General-Purpose Input Output 202 This pin also has digital mux functions which are described in the GPIO section of this table.
C9		J2	24	G2		I	ADC-C Input 9
CMP11_HP2						I	CMPSS-11 High Comparator Positive Input 2
CMP11_LP2						I	CMPSS-11 Low Comparator Positive Input 2
GPIO201						I/O	General-Purpose Input Output 201 This pin also has digital mux functions which are described in the GPIO section of this table.
C10		L3				I	ADC-C Input 10
CMP10_HP0						I	CMPSS-10 High Comparator Positive Input 0
CMP10_LP0						I	CMPSS-10 Low Comparator Positive Input 0
AIO241	0, 4, 8, 12					I	Analog Pin Used For Digital Input 241
C11		K2				I	ADC-C Input 11
CMP11_HP0						I	CMPSS-11 High Comparator Positive Input 0
CMP11_LP0						I	CMPSS-11 Low Comparator Positive Input 0
AIO242	0, 4, 8, 12					I	Analog Pin Used For Digital Input 242
C13		K1				I	ADC-C Input 13
CMP9_HP1						I	CMPSS-9 High Comparator Positive Input 1
CMP9_LP1						I	CMPSS-9 Low Comparator Positive Input 1
CMP11_HN1						I	CMPSS-11 High Comparator Negative Input 1
CMP11_LN1						I	CMPSS-11 Low Comparator Negative Input 1
AIO239	0, 4, 8, 12					I	Analog Pin Used For Digital Input 239

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
VREFHIA		M2	37	K2	19	I	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. NOTE: Do not load this pin externally
VREFHIB		R4	53	M4	34	I	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. NOTE: Do not load this pin externally
VREFHIC		L2	35	J2	19	I	ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. NOTE: Do not load this pin externally
VREFLOA		M1	33	K1	16	I	ADC-A Low Reference
VREFLOB		T4	50	N4	32	I	ADC-B Low Reference
VREFLOC		L1	32	J1	16	I	ADC-C Low Reference
GPIO							
GPIO0	0, 4, 8, 12	F8	160	E7	89	I/O	General-Purpose Input Output 0
EPWM1_A	1					O	ePWM-1 Output A
CLB_OUTPUTXBAR1	5					O	CLB Output X-BAR Output 1
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_A13	9					O	External Memory Interface 1 address line 13
ESC_GPI0	10					I	EtherCAT General-Purpose Input 0
FSITXA_D0	13					O	FSITX-A Primary Data Output
GPIO1	0, 4, 8, 12	A7	161	A6	90	I/O	General-Purpose Input Output 1
EPWM1_B	1					O	ePWM-1 Output B
CLB_OUTPUTXBAR2	5					O	CLB Output X-BAR Output 2
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF1_A14	9					O	External Memory Interface 1 address line 14
ESC_GPI1	10					I	EtherCAT General-Purpose Input 1
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output
GPIO2	0, 4, 8, 12	B7	162	B6	91	I/O	General-Purpose Input Output 2
EPWM2_A	1					O	ePWM-2 Output A
OUTPUTXBAR1	5					O	Output X-BAR Output 1
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
UARTA_TX	7					I/O	UART-A Serial Data Transmit
EMIF1_A15	9					O	External Memory Interface 1 address line 15
ESC_GPI2	10					I	EtherCAT General-Purpose Input 2
FSITXA_CLK	13					O	FSITX-A Output Clock
GPIO3	0, 4, 8, 12	C7	163	C6	92	I/O	General-Purpose Input Output 3
EPWM2_B	1					O	ePWM-2 Output B
OUTPUTXBAR2	2, 5					O	Output X-BAR Output 2
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
UARTA_RX	7					I/O	UART-A Serial Data Receive
ESC_GPI3	10					I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13					I	FSIRX-A Primary Data Input

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO4	0, 4, 8, 12	D7	164	D6	93	I/O	General-Purpose Input Output 4
EPWM3_A	1					O	ePWM-3 Output A
OUTPUTXBAR3	5					O	Output X-BAR Output 3
CANA_TX	6					O	CAN-A Transmit
MCANA_TX	9					O	CAN/CAN FD-A Transmit
ESC_GPI4	10					I	EtherCAT General-Purpose Input 4
FSIRXA_D1	13					I	FSIRX-A Optional Additional Data Input
GPIO5	0, 4, 8, 12	E7	165	E6		I/O	General-Purpose Input Output 5
EPWM3_B	1					O	ePWM-3 Output B
OUTPUTXBAR3	3					O	Output X-BAR Output 3
CLB_OUTPUTXBAR3	5					O	CLB Output X-BAR Output 3
CANA_RX	6					I	CAN-A Receive
MCANA_RX	9					I	CAN/CAN FD-A Receive
ESC_GPI5	10					I	EtherCAT General-Purpose Input 5
FSIRXA_CLK	13					I	FSIRX-A Input Clock
GPIO6	0, 4, 8, 12	F7	166	A5		I/O	General-Purpose Input Output 6
EPWM4_A	1					O	ePWM-4 Output A
OUTPUTXBAR4	2					O	Output X-BAR Output 4
EXTSYNCOUT	3					O	External ePWM Synchronization Pulse
EQEP3_A	5					I	eQEP-3 Input A
MCANB_TX	6					O	CAN/CAN FD-B Transmit
LINA_TX	7					O	LIN-A Transmit
EMIF1_DQM0	9					O	External Memory Interface 1 Input/output mask for byte 0
ESC_GPI6	10					I	EtherCAT General-Purpose Input 6
FSITXB_D0	13					O	FSITX-B Primary Data Output
GPIO7	0, 4, 8, 12	A6	167	B5		I/O	General-Purpose Input Output 7
EPWM4_B	1					O	ePWM-4 Output B
OUTPUTXBAR5	3					O	Output X-BAR Output 5
EQEP3_B	5					I	eQEP-3 Input B
MCANB_RX	6					I	CAN/CAN FD-B Receive
LINA_RX	7					I	LIN-A Receive
EMIF1_DQM1	9					O	External Memory Interface 1 Input/output mask for byte 1
ESC_GPI7	10					I	EtherCAT General-Purpose Input 7
FSITXB_D1	13					O	FSITX-B Optional Additional Data Output
GPIO8	0, 4, 8, 12	D1	18	E3		I/O	General-Purpose Input Output 8
EPWM5_A	1					O	ePWM-5 Output A
EMIF1_RAS	2					O	External Memory Interface 1 row address strobe
ADCSOCAO	3					O	ADC Start of Conversion A Output for External ADC (from ePWM modules)
EQEP3_STROBE	5					I/O	eQEP-3 Strobe
SCIA_TX	6					O	SCI-A Transmit Data
CLB_OUTPUTXBAR4	7					O	CLB Output X-BAR Output 4
MCANA_TX	9					O	CAN/CAN FD-A Transmit
ESC_GPO0	10					O	EtherCAT General-Purpose Output 0
FSITXB_CLK	13					O	FSITX-B Output Clock
FSITXA_D1	14					O	FSITX-A Optional Additional Data Output
FSIRXA_D0	15					I	FSIRX-A Primary Data Input

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO9	0, 4, 8, 12	E1	19	F3		I/O	General-Purpose Input Output 9
EPWM5_B	1					O	ePWM-5 Output B
SCIB_TX	2					O	SCI-B Transmit Data
OUTPUTXBAR6	3					O	Output X-BAR Output 6
EQEP3_INDEX	5					I/O	eQEP-3 Index
SCIA_RX	6					I	SCI-A Receive Data
ESC_GPO1	10					O	EtherCAT General-Purpose Output 1
FSIRXB_D0	13					I	FSIRX-B Primary Data Input
FSITXA_D0	14					O	FSITX-A Primary Data Output
FSIRXA_CLK	15					I	FSIRX-A Input Clock
GPIO10	0, 4, 8, 12	D4	1	B3	100	I/O	General-Purpose Input Output 10
EPWM6_A	1					O	ePWM-6 Output A
EMIF1_CAS	2					O	External Memory Interface 1 column address strobe
ADCSOCBO	3					O	ADC Start of Conversion B Output for External ADC (from ePWM modules)
EQEP1_A	5					I	eQEP-1 Input A
SCIB_TX	6					O	SCI-B Transmit Data
SD4_C1	7					I	SDFM-4 Channel 1 Clock Input
MCANA_RX	9					I	CAN/CAN FD-A Receive
CLB_OUTPUTXBAR5	10					O	CLB Output X-BAR Output 5
ESC_TX0_DATA0	11					O	EtherCAT MII Transmit-0 Data-0
FSIRXB_D1	13					I	FSIRX-B Optional Additional Data Input
FSITXA_CLK	14					O	FSITX-A Output Clock
FSIRXA_D1	15					I	FSIRX-A Optional Additional Data Input
GPIO11	0, 4, 8, 12	E4	2	B2	1	I/O	General-Purpose Input Output 11
EPWM6_B	1					O	ePWM-6 Output B
SCIB_RX	2, 6					I	SCI-B Receive Data
OUTPUTXBAR7	3					O	Output X-BAR Output 7
EQEP1_B	5					I	eQEP-1 Input B
SD4_D1	7					I	SDFM-4 Channel 1 Data Input
ESC_GPO3	10					O	EtherCAT General-Purpose Output 3
ESC_TX0_DATA1	11					O	EtherCAT MII Transmit-0 Data-1
FSIRXB_CLK	13					I	FSIRX-B Input Clock
FSIRXA_D1	14					I	FSIRX-A Optional Additional Data Input
PMBUSA_ALERT	15					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
GPIO12	0, 4, 8, 12	G4	4	B1	3	I/O	General-Purpose Input Output 12
EPWM7_A	1					O	ePWM-7 Output A
CLB_OUTPUTXBAR6	2					O	CLB Output X-BAR Output 6
ADCSOCAO	3					O	ADC Start of Conversion A Output for External ADC (from ePWM modules)
EQEP1_STROBE	5					I/O	eQEP-1 Strobe
SCIA_TX	6					O	SCI-A Transmit Data
SD4_C2	7					I	SDFM-4 Channel 2 Clock Input
EMIF1_A1	9					O	External Memory Interface 1 address line 1
ESC_GPO4	10					O	EtherCAT General-Purpose Output 4
ESC_TX0_DATA2	11					O	EtherCAT MII Transmit-0 Data-2
FSIRXC_D0	13					I	FSIRX-C Primary Data Input
FSIRXA_D0	14					I	FSIRX-A Primary Data Input
PMBUSA_CTL	15					I/O	PMBus-A Control Signal - Target Input/Controller Output

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO13	0, 4, 8, 12	A3	5	C1	4	I/O	General-Purpose Input Output 13
EPWM7_B	1					O	ePWM-7 Output B
CLB_OUTPUTXBAR7	2					O	CLB Output X-BAR Output 7
EQEP5_STROBE	3					I/O	eQEP-5 Strobe
EQEP1_INDEX	5					I/O	eQEP-1 Index
SCIA_RX	6					I	SCI-A Receive Data
SD4_D2	7					I	SDFM-4 Channel 2 Data Input
EMIF1_CS0n	9					O	External Memory Interface 1 chip select 0
ESC_GPO5	10					O	EtherCAT General-Purpose Output 5
ESC_TX0_DATA3	11					O	EtherCAT MII Transmit-0 Data-3
FSIRXC_D1	13					I	FSIRX-C Optional Additional Data Input
FSIRXA_CLK	14					I	FSIRX-A Input Clock
PMBUSA_SDA	15					I/OD	PMBus-A Open-Drain Bidirectional Data
GPIO14	0, 4, 8, 12	B3	6	C2	5	I/O	General-Purpose Input Output 14
EPWM8_A	1					O	ePWM-8 Output A
SCIB_TX	2					O	SCI-B Transmit Data
EQEP5_INDEX	3					I/O	eQEP-5 Index
LINA_TX	5					O	LIN-A Transmit
OUTPUTXBAR3	6					O	Output X-BAR Output 3
OUTPUTXBAR8	7					O	Output X-BAR Output 8
ESC_GPO6	10					O	EtherCAT General-Purpose Output 6
ESC_PHY1_LINKSTATUS	11					I	EtherCAT PHY-1 Link Status
FSIRXC_CLK	13					I	FSIRX-C Input Clock
EMIF1_D17	14					I/O	External Memory Interface 1 data line 17
PMBUSA_SCL	15					I/OD	PMBus-A Open-Drain Bidirectional Clock
GPIO15	0, 4, 8, 12	C3	7	C3	6	I/O	General-Purpose Input Output 15
EPWM8_B	1					O	ePWM-8 Output B
SCIB_RX	2					I	SCI-B Receive Data
LINA_RX	5					I	LIN-A Receive
OUTPUTXBAR4	6					O	Output X-BAR Output 4
CLB_OUTPUTXBAR8	7					O	CLB Output X-BAR Output 8
ESC_GPO7	10					O	EtherCAT General-Purpose Output 7
EQEP5_A	11					I	eQEP-5 Input A
FSIRXD_D0	13					I	FSIRX-D Primary Data Input
EMIF1_DQM2	15					O	External Memory Interface 1 Input/output mask for byte 2
GPIO16	0, 4, 8, 12	D3	8	C4		I/O	General-Purpose Input Output 16
SPIA_PICO	1					I/O	SPI-A Peripheral In, Controller Out (PICO)
OUTPUTXBAR7	3					O	Output X-BAR Output 7
EPWM9_A	5					O	ePWM-9 Output A
SD1_D1	7					I	SDFM-1 Channel 1 Data Input
EQEP5_B	11					I	eQEP-5 Input B
FSIRXD_D1	13					I	FSIRX-D Optional Additional Data Input
ESC_RX1_CLK	15					I	EtherCAT MII Receive-1 Clock

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO17	0, 4, 8, 12	E3	9	D4		I/O	General-Purpose Input Output 17
SPIA_POCI	1					I/O	SPI-A Peripheral Out, Controller In (POCI)
OUTPUTXBAR8	3					O	Output X-BAR Output 8
EPWM9_B	5					O	ePWM-9 Output B
SD1_C1	7					I	SDFM-1 Channel 1 Clock Input
EQEP5_STROBE	11					I/O	eQEP-5 Strobe
FSIRXD_CLK	13					I	FSIRX-D Input Clock
ESC_RX1_DV	15					I	EtherCAT MII Receive-1 Data Valid
GPIO18	0, 4, 8, 12	F3	10	D3		I/O	General-Purpose Input Output 18
SPIA_CLK	1					I/O	SPI-A Clock
SCIB_TX	2					O	SCI-B Transmit Data
CANA_RX	3					I	CAN-A Receive
EPWM10_A	5					O	ePWM-10 Output A
SD1_D2	7					I	SDFM-1 Channel 2 Data Input
MCANA_RX	9					I	CAN/CAN FD-A Receive
EMIF1_CS2n	10					O	External Memory Interface 1 chip select 2
EQEP5_INDEX	11					I/O	eQEP-5 Index
ESC_RX1_ERR	15					I	EtherCAT MII Receive-1 Error
GPIO19	0, 4, 8, 12	B2	12	D1		I/O	General-Purpose Input Output 19
SPIA_PTE	1					I/O	SPI-A Peripheral Transmit Enable (PTE)
SCIB_RX	2					I	SCI-B Receive Data
CANA_TX	3					O	CAN-A Transmit
EPWM10_B	5					O	ePWM-10 Output B
SD1_C2	7					I	SDFM-1 Channel 2 Clock Input
MCANA_TX	9					O	CAN/CAN FD-A Transmit
EMIF1_CS3n	10					O	External Memory Interface 1 chip select 3
ESC_TX1_DATA3	15					O	EtherCAT MII Transmit-1 Data-3
GPIO20	0, 4, 8, 12	C2	13	E1		I/O	General-Purpose Input Output 20
EQEP1_A	1					I	eQEP-1 Input A
EPWM11_A	5					O	ePWM-11 Output A
SD1_D3	7					I	SDFM-1 Channel 3 Data Input
MCANB_TX	9					O	CAN/CAN FD-B Transmit
EMIF1_BA0	10					O	External Memory Interface 1 bank address 0
SPIC_PICO	14					I/O	SPI-C Peripheral In, Controller Out (PICO)
ESC_TX1_DATA2	15					O	EtherCAT MII Transmit-1 Data-2
GPIO21	0, 4, 8, 12	D2	14	E2		I/O	General-Purpose Input Output 21
EQEP1_B	1					I	eQEP-1 Input B
EPWM11_B	5					O	ePWM-11 Output B
SD1_C3	7					I	SDFM-1 Channel 3 Clock Input
MCANB_RX	9					I	CAN/CAN FD-B Receive
EMIF1_BA1	10					O	External Memory Interface 1 bank address 1
SPIC_POCI	14					I/O	SPI-C Peripheral Out, Controller In (POCI)
ESC_TX1_DATA1	15					O	EtherCAT MII Transmit-1 Data-1

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO22	0, 4, 8, 12	A2	11	D2		I/O	General-Purpose Input Output 22
EQEP1_STROBE	1					I/O	eQEP-1 Strobe
SCIB_TX	3					O	SCI-B Transmit Data
EPWM12_A	5					O	ePWM-12 Output A
SPIB_CLK	6					I/O	SPI-B Clock
SD1_D4	7					I	SDFM-1 Channel 4 Data Input
MCANA_TX	9					O	CAN/CAN FD-A Transmit
EMIF1_RAS	10					O	External Memory Interface 1 row address strobe
SPIC_CLK	14					I/O	SPI-C Clock
ESC_TX1_DATA0	15					O	EtherCAT MII Transmit-1 Data-0
GPIO23	0, 4, 8, 12	G1	21	F2		I/O	General-Purpose Input Output 23
EQEP1_INDEX	1					I/O	eQEP-1 Index
SCIB_RX	3					I	SCI-B Receive Data
EPWM12_B	5					O	ePWM-12 Output B
SPIB_PTE	6					I/O	SPI-B Peripheral Transmit Enable (PTE)
SD1_C4	7					I	SDFM-1 Channel 4 Clock Input
MCANA_RX	9					I	CAN/CAN FD-A Receive
EMIF1_CAS	10					O	External Memory Interface 1 column address strobe
SPIC_PTE	14					I/O	SPI-C Peripheral Transmit Enable (PTE)
ESC_PHY_RESETn	15					O	EtherCAT PHY Active Low Reset
GPIO24	0, 4, 8, 12	E8	159	D7		I/O	General-Purpose Input Output 24
OUTPUTXBAR1	1					O	Output X-BAR Output 1
EQEP2_A	2					I	eQEP-2 Input A
LINB_TX	5					O	LIN-B Transmit
SPIB_PICO	6					I/O	SPI-B Peripheral In, Controller Out (PICO)
SD2_D1	7					I	SDFM-2 Channel 1 Data Input
PMBUSA_SCL	9					I/OD	PMBus-A Open-Drain Bidirectional Clock
EMIF1_DQM0	10					O	External Memory Interface 1 Input/output mask for byte 0
EPWM13_A	13					O	ePWM-13 Output A
ESC_RX0_DATA1	14					I	EtherCAT MII Receive-0 Data-1
ESC_RX0_CLK	15					I	EtherCAT MII Receive-0 Clock
GPIO25	0, 4, 8, 12	A10	153	B8	84	I/O	General-Purpose Input Output 25
OUTPUTXBAR2	1					O	Output X-BAR Output 2
EQEP2_B	2					I	eQEP-2 Input B
LINB_RX	5					I	LIN-B Receive
SPIB_POCI	6					I/O	SPI-B Peripheral Out, Controller In (POCI)
SD2_C1	7					I	SDFM-2 Channel 1 Clock Input
PMBUSA_SDA	9					I/OD	PMBus-A Open-Drain Bidirectional Data
EMIF1_DQM1	10					O	External Memory Interface 1 Input/output mask for byte 1
EQEP5_B	11					I	eQEP-5 Input B
EPWM13_B	13					O	ePWM-13 Output B
FSITXA_D1	14					O	FSITX-A Optional Additional Data Output
ESC_RX0_DV	15					I	EtherCAT MII Receive-0 Data Valid

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO26	0, 4, 8, 12	L11	82	L10		I/O	General-Purpose Input Output 26
OUTPUTXBAR3	1, 5					O	Output X-BAR Output 3
EQEP2_INDEX	2					I/O	eQEP-2 Index
SPIB_CLK	6					I/O	SPI-B Clock
SD2_D2	7					I	SDFM-2 Channel 2 Data Input
PMBUSA_ALERT	9					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
EMIF1_DQM2	10					O	External Memory Interface 1 Input/output mask for byte 2
ESC_MDIO_CLK	11					O	EtherCAT MDIO Clock
EPWM14_A	13					O	ePWM-14 Output A
FSITXA_D0	14					O	FSITX-A Primary Data Output
ESC_RX0_ERR	15					I	EtherCAT MII Receive-0 Error
GPIO27	0, 4, 8, 12	G13	125	D11		I/O	General-Purpose Input Output 27
OUTPUTXBAR4	1, 5					O	Output X-BAR Output 4
EQEP2_STROBE	2					I/O	eQEP-2 Strobe
SPIB_PTE	6					I/O	SPI-B Peripheral Transmit Enable (PTE)
SD2_C2	7					I	SDFM-2 Channel 2 Clock Input
PMBUSA_CTL	9					I/O	PMBus-A Control Signal - Target Input/Controller Output
EMIF1_DQM3	10					O	External Memory Interface 1 Input/output mask for byte 3
ESC_MDIO_DATA	11					I/O	EtherCAT MDIO Data
EPWM14_B	13					O	ePWM-14 Output B
FSITXA_CLK	14					O	FSITX-A Output Clock
ESC_RX0_DATA0	15					I	EtherCAT MII Receive-0 Data-0
GPIO28	0, 4, 8, 12	N11	74	K8		I/O	General-Purpose Input Output 28
SCIA_RX	1					I	SCI-A Receive Data
EMIF1_CS4n	2					O	External Memory Interface 1 chip select 4
UARTA_RX	3					I/O	UART-A Serial Data Receive
OUTPUTXBAR5	5					O	Output X-BAR Output 5
EQEP3_A	6					I	eQEP-3 Input A
SD2_D3	7					I	SDFM-2 Channel 3 Data Input
EMIF1_CS2n	9					O	External Memory Interface 1 chip select 2
EPWM15_A	13					O	ePWM-15 Output A
ESC_RX0_DATA1	15					I	EtherCAT MII Receive-0 Data-1
GPIO29	0, 4, 8, 12	P11	73	L8		I/O	General-Purpose Input Output 29
SCIA_TX	1					O	SCI-A Transmit Data
EMIF1_SDCKE	2					O	External Memory Interface 1 SDRAM clock enable
UARTA_TX	3					I/O	UART-A Serial Data Transmit
OUTPUTXBAR6	5					O	Output X-BAR Output 6
EQEP3_B	6					I	eQEP-3 Input B
SD2_C3	7					I	SDFM-2 Channel 3 Clock Input
EMIF1_CS3n	9					O	External Memory Interface 1 chip select 3
ESC_LATCH0	10					I	EtherCAT Latch Signal Input 0
ESC_I2C_SDA	11					I/OC	EtherCAT I2C Data
EPWM15_B	13					O	ePWM-15 Output B
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
ESC_RX0_DATA2	15					I	EtherCAT MII Receive-0 Data-2

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO30	0, 4, 8, 12	L10	79	L9	48	I/O	General-Purpose Input Output 30
CANA_RX	1					I	CAN-A Receive
EMIF1_CLK	2					O	External Memory Interface 1 clock
MCANA_RX	3					I	CAN/CAN FD-A Receive
OUTPUTXBAR7	5					O	Output X-BAR Output 7
EQEP3_STROBE	6					I/O	eQEP-3 Strobe
SD2_D4	7					I	SDFM-2 Channel 4 Data Input
EMIF1_CS4n	9					O	External Memory Interface 1 chip select 4
ESC_LATCH1	10					I	EtherCAT Latch Signal Input 1
ESC_I2C_SCL	11					I/OC	EtherCAT I2C Clock
EPWM16_A	13					O	ePWM-16 Output A
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
SPID_PICO	15					I/O	SPI-D Peripheral In, Controller Out (PICO)
GPIO31	0, 4, 8, 12	D8	158			I/O	General-Purpose Input Output 31
CANA_TX	1					O	CAN-A Transmit
EMIF1_WEn	2					O	External Memory Interface 1 write enable
MCANA_TX	3					O	CAN/CAN FD-A Transmit
OUTPUTXBAR8	5					O	Output X-BAR Output 8
EQEP3_INDEX	6					I/O	eQEP-3 Index
SD2_C4	7					I	SDFM-2 Channel 4 Clock Input
EMIF1_RNW	9					O	External Memory Interface 1 read not write
I2CA_SDA	10					I/OD	I2C-A Open-Drain Bidirectional Data
EPWM16_B	13					O	ePWM-16 Output B
SPID_POCI	15					I/O	SPI-D Peripheral Out, Controller In (POCI)
GPIO32	0, 4, 8, 12	J14	116	F12		I/O	General-Purpose Input Output 32
I2CA_SDA	1					I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_CS0n	2					O	External Memory Interface 1 chip select 0
SPIA_PICO	3					I/O	SPI-A Peripheral In, Controller Out (PICO)
EQEP4_A	5					I	eQEP-4 Input A
LINB_TX	6					O	LIN-B Transmit
CLB_OUTPUTXBAR1	7					O	CLB Output X-BAR Output 1
EMIF1_OEn	9					O	External Memory Interface 1 output enable
I2CA_SCL	10					I/OD	I2C-A Open-Drain Bidirectional Clock
SPID_CLK	15					I/O	SPI-D Clock
GPIO33	0, 4, 8, 12	R10	69	L7		I/O	General-Purpose Input Output 33
I2CA_SCL	1					I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF1_RNW	2					O	External Memory Interface 1 read not write
SPIA_POCI	3					I/O	SPI-A Peripheral Out, Controller In (POCI)
EQEP4_B	5					I	eQEP-4 Input B
CLB_OUTPUTXBAR2	7					O	CLB Output X-BAR Output 2
EMIF1_BA0	9					O	External Memory Interface 1 bank address 0
ESC_LED_ERR	11					O	EtherCAT Error LED
SPID_PTE	15					I/O	SPI-D Peripheral Transmit Enable (PTE)

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO34	0, 4, 8, 12	P10	70	K7	42	I/O	General-Purpose Input Output 34
OUTPUTXBAR1	1					O	Output X-BAR Output 1
EMIF1_CS2n	2					O	External Memory Interface 1 chip select 2
SPIA_CLK	3					I/O	SPI-A Clock
EQEP4_STROBE	5					I/O	eQEP-4 Strobe
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
CLB_OUTPUTXBAR3	7					O	CLB Output X-BAR Output 3
EMIF1_BA1	9					O	External Memory Interface 1 bank address 1
ESC_LATCH0	10					I	EtherCAT Latch Signal Input 0
EPWM18_A	11					O	ePWM-18 Output A
SCIA_TX	13					O	SCI-A Transmit Data
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
GPIO35	0, 4, 8, 12	N10	71	N8	43	I/O	General-Purpose Input Output 35
SCIA_RX	1, 13					I	SCI-A Receive Data
EMIF1_CS3n	2					O	External Memory Interface 1 chip select 3
SPIA_PTE	3					I/O	SPI-A Peripheral Transmit Enable (PTE)
EQEP4_INDEX	5					I/O	eQEP-4 Index
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
CLB_OUTPUTXBAR4	7					O	CLB Output X-BAR Output 4
EMIF1_A0	9					O	External Memory Interface 1 address line 0
ESC_LATCH1	10					I	EtherCAT Latch Signal Input 1
EPWM18_B	11					O	ePWM-18 Output B
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
GPIO36	0, 4, 8, 12	P12	83	N11		I/O	General-Purpose Input Output 36
SCIA_TX	1					O	SCI-A Transmit Data
EMIF1_WAIT	2					I	External Memory Interface 1 Asynchronous SRAM WAIT
CANA_RX	6					I	CAN-A Receive
CLB_OUTPUTXBAR5	7					O	CLB Output X-BAR Output 5
EMIF1_A1	9					O	External Memory Interface 1 address line 1
MCANA_RX	10					I	CAN/CAN FD-A Receive
SD1_D1	13					I	SDFM-1 Channel 1 Data Input
EMIF1_WEn	14					O	External Memory Interface 1 write enable
GPIO37	0, 4, 8, 12	N12	84	M11		I/O	General-Purpose Input Output 37
OUTPUTXBAR2	1					O	Output X-BAR Output 2
EMIF1_OEn	2					O	External Memory Interface 1 output enable
EPWM18_A	3					O	ePWM-18 Output A
CANA_TX	6					O	CAN-A Transmit
CLB_OUTPUTXBAR6	7					O	CLB Output X-BAR Output 6
EMIF1_A2	9					O	External Memory Interface 1 address line 2
MCANA_TX	10					O	CAN/CAN FD-A Transmit
SD1_D2	13					I	SDFM-1 Channel 2 Data Input
EMIF1_D24	14					I/O	External Memory Interface 1 data line 24

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO38	0, 4, 8, 12	M12	85	L11		I/O	General-Purpose Input Output 38
EMIF1_A0	2					O	External Memory Interface 1 address line 0
EPWM18_B	3					O	ePWM-18 Output B
UARTA_TX	5					I/O	UART-A Serial Data Transmit
SCIB_TX	6					O	SCI-B Transmit Data
CLB_OUTPUTXBAR7	7					O	CLB Output X-BAR Output 7
EMIF1_A3	9					O	External Memory Interface 1 address line 3
SD1_D3	13					I	SDFM-1 Channel 3 Data Input
EMIF1_CS2n	14					O	External Memory Interface 1 chip select 2
GPIO39	0, 4, 8, 12	L12	86			I/O	General-Purpose Input Output 39
EMIF1_A1	2					O	External Memory Interface 1 address line 1
UARTA_RX	5					I/O	UART-A Serial Data Receive
SCIB_RX	6					I	SCI-B Receive Data
CLB_OUTPUTXBAR8	7					O	CLB Output X-BAR Output 8
EMIF1_A4	9					O	External Memory Interface 1 address line 4
ESC_MDIO_DATA	10					I/O	EtherCAT MDIO Data
ESC_LED_RUN	11					O	EtherCAT Run LED
SD1_D4	13					I	SDFM-1 Channel 4 Data Input
FSIRXD_CLK	14					I	FSIRX-D Input Clock
GPIO40	0, 4, 8, 12	P13	87	N12		I/O	General-Purpose Input Output 40
EMIF1_A2	2					O	External Memory Interface 1 address line 2
EPWM13_A	3					O	ePWM-13 Output A
MCANB_RX	5					I	CAN/CAN FD-B Receive
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
SD4_C3	7					I	SDFM-4 Channel 3 Clock Input
ESC_GPO2	9					O	EtherCAT General-Purpose Output 2
CLB_OUTPUTXBAR1	10					O	CLB Output X-BAR Output 1
SD2_C1	13					I	SDFM-2 Channel 1 Clock Input
ESC_I2C_SDA	14					I/OC	EtherCAT I2C Data
GPIO41	0, 4, 8, 12	R15	89	M12	51	I/O	General-Purpose Input Output 41
EMIF1_A3	2					O	External Memory Interface 1 address line 3
EPWM13_B	3					O	ePWM-13 Output B
MCANB_TX	5					O	CAN/CAN FD-B Transmit
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
SD4_D3	7					I	SDFM-4 Channel 3 Data Input
CLB_OUTPUTXBAR2	10					O	CLB Output X-BAR Output 2
SD2_D1	13					I	SDFM-2 Channel 1 Data Input
ESC_I2C_SCL	14					I/OC	EtherCAT I2C Clock
FSIRXD_CLK	15					I	FSIRX-D Input Clock
GPIO42	0, 4, 8, 12	E16	130	C12	73	I/O	General-Purpose Input Output 42
EPWM14_A	3					O	ePWM-14 Output A
EQEP4_A	5					I	eQEP-4 Input A
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
SD4_C4	7					I	SDFM-4 Channel 4 Clock Input
CLB_OUTPUTXBAR5	10					O	CLB Output X-BAR Output 5
UARTA_TX	11					I/O	UART-A Serial Data Transmit
FSIRXD_D0	14					I	FSIRX-D Primary Data Input
SCIA_TX	15					O	SCI-A Transmit Data
USB0DM	ALT					O	USB-0 PHY differential data

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO43	0, 4, 8, 12	D16	131	C11	74	I/O	General-Purpose Input Output 43
EPWM14_B	3					O	ePWM-14 Output B
EQEP4_B	5					I	eQEP-4 Input B
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
SD4_D4	7					I	SDFM-4 Channel 4 Data Input
CLB_OUTPUTXBAR6	10					O	CLB Output X-BAR Output 6
UARTA_RX	11					I/O	UART-A Serial Data Receive
FSIRXD_D1	14					I	FSIRX-D Optional Additional Data Input
SCIA_RX	15					I	SCI-A Receive Data
USB0DP	ALT					O	USB-0 PHY differential data
GPIO44	0, 4, 8, 12	J12	113	F10		I/O	General-Purpose Input Output 44
SPID_POCI	1					I/O	SPI-D Peripheral Out, Controller In (POCI)
EMIF1_A4	2					O	External Memory Interface 1 address line 4
MCANB_RX	3					I	CAN/CAN FD-B Receive
SD3_C4	6					I	SDFM-3 Channel 4 Clock Input
UARTB_TX	7					I/O	UART-B Serial Data Transmit
CLB_OUTPUTXBAR6	10					O	CLB Output X-BAR Output 6
FSIRXD_CLK	13					I	FSIRX-D Input Clock
ESC_TX1_CLK	14					I	EtherCAT MII Transmit-1 Clock
GPIO45	0, 4, 8, 12	J13	115	F11		I/O	General-Purpose Input Output 45
SPID_PTE	1					I/O	SPI-D Peripheral Transmit Enable (PTE)
EMIF1_A5	2					O	External Memory Interface 1 address line 5
MCANB_TX	3					O	CAN/CAN FD-B Transmit
SD3_D4	6					I	SDFM-3 Channel 4 Data Input
UARTB_RX	7					I/O	UART-B Serial Data Receive
CLB_OUTPUTXBAR7	10					O	CLB Output X-BAR Output 7
ESC_TX1_ENA	14					I/O	EtherCAT MII Transmit-1 Enable
GPIO46	0, 4, 8, 12	F14	128		71	I/O	General-Purpose Input Output 46
EPWM4_A	1					O	ePWM-4 Output A
EMIF1_A6	2					O	External Memory Interface 1 address line 6
EPWM14_A	3					O	ePWM-14 Output A
SCIA_RX	6					I	SCI-A Receive Data
SD3_C4	7					I	SDFM-3 Channel 4 Clock Input
ESC_MDIO_CLK	14					O	EtherCAT MDIO Clock
GPIO47	0, 4, 8, 12	E14	129		72	I/O	General-Purpose Input Output 47
EPWM4_B	1					O	ePWM-4 Output B
EMIF1_A7	2					O	External Memory Interface 1 address line 7
EPWM14_B	3					O	ePWM-14 Output B
SCIA_TX	6					O	SCI-A Transmit Data
SD4_C3	7					I	SDFM-4 Channel 3 Clock Input
ESC_MDIO_DATA	14					I/O	EtherCAT MDIO Data
GPIO48	0, 4, 8, 12	R16	90	M13		I/O	General-Purpose Input Output 48
OUTPUTXBAR3	1					O	Output X-BAR Output 3
EMIF1_A8	2					O	External Memory Interface 1 address line 8
SCIA_TX	6					O	SCI-A Transmit Data
SD1_D1	7					I	SDFM-1 Channel 1 Data Input
SD2_C2	13					I	SDFM-2 Channel 2 Clock Input
ESC_PHY_CLK	14					O	EtherCAT PHY Clock

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO49	0, 4, 8, 12	P15	93	L13		I/O	General-Purpose Input Output 49
OUTPUTXBAR4	1					O	Output X-BAR Output 4
EMIF1_A9	2					O	External Memory Interface 1 address line 9
SCIA_RX	6					I	SCI-A Receive Data
SD1_C1	7					I	SDFM-1 Channel 1 Clock Input
EMIF1_A5	9					O	External Memory Interface 1 address line 5
SD2_D1	13					I	SDFM-2 Channel 1 Data Input
FSITXA_D0	14					O	FSITX-A Primary Data Output
GPIO50	0, 4, 8, 12	P14	94	K9		I/O	General-Purpose Input Output 50
EQEP1_A	1					I	eQEP-1 Input A
EMIF1_A10	2					O	External Memory Interface 1 address line 10
EPWM15_A	3					O	ePWM-15 Output A
SPIC_PICO	6					I/O	SPI-C Peripheral In, Controller Out (PICO)
SD1_D2	7					I	SDFM-1 Channel 2 Data Input
EMIF1_A6	9					O	External Memory Interface 1 address line 6
ESC_LATCH0	11					I	EtherCAT Latch Signal Input 0
SD2_D2	13					I	SDFM-2 Channel 2 Data Input
FSITXA_D1	14					O	FSITX-A Optional Additional Data Output
GPIO51	0, 4, 8, 12	N14	95	K10		I/O	General-Purpose Input Output 51
EQEP1_B	1					I	eQEP-1 Input B
EMIF1_A11	2					O	External Memory Interface 1 address line 11
EPWM15_B	3					O	ePWM-15 Output B
SPIC_POCI	6					I/O	SPI-C Peripheral Out, Controller In (POCI)
SD1_C2	7					I	SDFM-1 Channel 2 Clock Input
EMIF1_A7	9					O	External Memory Interface 1 address line 7
ESC_LATCH1	11					I	EtherCAT Latch Signal Input 1
SD2_D3	13					I	SDFM-2 Channel 3 Data Input
FSITXA_CLK	14					O	FSITX-A Output Clock
GPIO52	0, 4, 8, 12	N15	96	K11		I/O	General-Purpose Input Output 52
EQEP1_STROBE	1					I/O	eQEP-1 Strobe
EMIF1_A12	2					O	External Memory Interface 1 address line 12
EPWM16_A	3					O	ePWM-16 Output A
SPIC_CLK	6					I/O	SPI-C Clock
SD1_D3	7					I	SDFM-1 Channel 3 Data Input
EMIF1_A8	9					O	External Memory Interface 1 address line 8
ESC_MDIO_CLK	11					O	EtherCAT MDIO Clock
SD2_D4	13					I	SDFM-2 Channel 4 Data Input
FSIRXA_D0	14					I	FSIRX-A Primary Data Input
GPIO53	0, 4, 8, 12	N16	97	K12		I/O	General-Purpose Input Output 53
EQEP1_INDEX	1					I/O	eQEP-1 Index
EMIF1_D31	2					I/O	External Memory Interface 1 data line 31
SPIC_PTE	6					I/O	SPI-C Peripheral Transmit Enable (PTE)
SD1_C3	7					I	SDFM-1 Channel 3 Clock Input
EMIF1_A9	9					O	External Memory Interface 1 address line 9
ESC_MDIO_DATA	11					I/O	EtherCAT MDIO Data
SD1_C1	13					I	SDFM-1 Channel 1 Clock Input
FSIRXA_D1	14					I	FSIRX-A Optional Additional Data Input

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO54	0, 4, 8, 12	M13	98	K13		I/O	General-Purpose Input Output 54
SPIA_PICO	1					I/O	SPI-A Peripheral In, Controller Out (PICO)
EMIF1_D30	2					I/O	External Memory Interface 1 data line 30
EQEP2_A	5					I	eQEP-2 Input A
SCIB_TX	6					O	SCI-B Transmit Data
SD1_D4	7					I	SDFM-1 Channel 4 Data Input
EMIF1_A10	9					O	External Memory Interface 1 address line 10
ESC_PHY_CLK	11					O	EtherCAT PHY Clock
SD1_C2	13					I	SDFM-1 Channel 2 Clock Input
FSIRXA_CLK	14					I	FSIRX-A Input Clock
GPIO55	0, 4, 8, 12	M14	100	J13		I/O	General-Purpose Input Output 55
SPIA_POCI	1					I/O	SPI-A Peripheral Out, Controller In (POCI)
EMIF1_D29	2					I/O	External Memory Interface 1 data line 29
EPWM16_B	3					O	ePWM-16 Output B
EQEP2_B	5					I	eQEP-2 Input B
SCIB_RX	6					I	SCI-B Receive Data
SD1_C4	7					I	SDFM-1 Channel 4 Clock Input
EMIF1_D0	9					I/O	External Memory Interface 1 data line 0
ESC_PHY0_LINKSTATUS	11					I	EtherCAT PHY-0 Link Status
SD1_C3	13					I	SDFM-1 Channel 3 Clock Input
FSITXB_D0	14					O	FSITX-B Primary Data Output
GPIO56	0, 4, 8, 12	M15	101	J12		I/O	General-Purpose Input Output 56
SPIA_CLK	1					I/O	SPI-A Clock
EMIF1_D28	2					I/O	External Memory Interface 1 data line 28
EPWM17_A	3					O	ePWM-17 Output A
EQEP2_STROBE	5					I/O	eQEP-2 Strobe
SD2_D1	7					I	SDFM-2 Channel 1 Data Input
EMIF1_D1	9					I/O	External Memory Interface 1 data line 1
I2CA_SDA	10					I/OD	I2C-A Open-Drain Bidirectional Data
ESC_TX0_ENA	11					I/O	EtherCAT MII Transmit-0 Enable
SD1_C4	13					I	SDFM-1 Channel 4 Clock Input
FSITXB_CLK	14					O	FSITX-B Output Clock
GPIO57	0, 4, 8, 12	M16	102	J11		I/O	General-Purpose Input Output 57
SPIA_PTE	1					I/O	SPI-A Peripheral Transmit Enable (PTE)
EMIF1_D27	2					I/O	External Memory Interface 1 data line 27
EPWM17_B	3					O	ePWM-17 Output B
EQEP2_INDEX	5					I/O	eQEP-2 Index
SD2_C1	7					I	SDFM-2 Channel 1 Clock Input
EMIF1_D2	9					I/O	External Memory Interface 1 data line 2
I2CA_SCL	10					I/OD	I2C-A Open-Drain Bidirectional Clock
ESC_TX0_CLK	11					I	EtherCAT MII Transmit-0 Clock
SD3_D3	13					I	SDFM-3 Channel 3 Data Input
FSITXB_D1	14					O	FSITX-B Optional Additional Data Output

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO58	0, 4, 8, 12	L13	103	J10	52	I/O	General-Purpose Input Output 58
SPIA_PICO	1, 15					I/O	SPI-A Peripheral In, Controller Out (PICO)
EMIF1_D26	2					I/O	External Memory Interface 1 data line 26
EPWM8_A	3					O	ePWM-8 Output A
OUTPUTXBAR1	5					O	Output X-BAR Output 1
SPIB_CLK	6					I/O	SPI-B Clock
SD2_D2	7					I	SDFM-2 Channel 2 Data Input
EMIF1_D3	9					I/O	External Memory Interface 1 data line 3
ESC_LED_LINK0_ACTIVE	10					O	EtherCAT Link-0 Active
CANA_RX	11					I	CAN-A Receive
SD2_C2	13					I	SDFM-2 Channel 2 Clock Input
FSIRXB_D0	14					I	FSIRX-B Primary Data Input
GPIO59	0, 4, 8, 12	L14	104	H13	53	I/O	General-Purpose Input Output 59
EPWM5_A	1					O	ePWM-5 Output A
EMIF1_D25	2					I/O	External Memory Interface 1 data line 25
EPWM8_B	3					O	ePWM-8 Output B
OUTPUTXBAR2	5					O	Output X-BAR Output 2
SPIB_PTE	6					I/O	SPI-B Peripheral Transmit Enable (PTE)
SD2_C2	7					I	SDFM-2 Channel 2 Clock Input
EMIF1_D4	9					I/O	External Memory Interface 1 data line 4
ESC_LED_LINK1_ACTIVE	10					O	EtherCAT Link-1 Active
CANA_TX	11					O	CAN-A Transmit
SD2_C3	13					I	SDFM-2 Channel 3 Clock Input
FSIRXB_D1	14					I	FSIRX-B Optional Additional Data Input
SPIA_POCI	15					I/O	SPI-A Peripheral Out, Controller In (POCI)
GPIO60	0, 4, 8, 12	L15	105		54	I/O	General-Purpose Input Output 60
EPWM3_B	1					O	ePWM-3 Output B
EMIF1_D24	2					I/O	External Memory Interface 1 data line 24
ESC_LATCH0	3					I	EtherCAT Latch Signal Input 0
OUTPUTXBAR3	5					O	Output X-BAR Output 3
SPIB_PICO	6					I/O	SPI-B Peripheral In, Controller Out (PICO)
SD2_D3	7					I	SDFM-2 Channel 3 Data Input
EMIF1_D5	9					I/O	External Memory Interface 1 data line 5
ESC_LED_ERR	10					O	EtherCAT Error LED
SD2_C4	13					I	SDFM-2 Channel 4 Clock Input
FSIRXB_CLK	14					I	FSIRX-B Input Clock
SPIA_CLK	15					I/O	SPI-A Clock
GPIO61	0, 4, 8, 12	K16	107	H11	56	I/O	General-Purpose Input Output 61
EPWM17_B	1					O	ePWM-17 Output B
EMIF1_D23	2					I/O	External Memory Interface 1 data line 23
ESC_LATCH1	3					I	EtherCAT Latch Signal Input 1
OUTPUTXBAR4	5					O	Output X-BAR Output 4
SPIB_POCI	6					I/O	SPI-B Peripheral Out, Controller In (POCI)
SD2_C3	7					I	SDFM-2 Channel 3 Clock Input
EMIF1_D6	9					I/O	External Memory Interface 1 data line 6
ESC_LED_RUN	10					O	EtherCAT Run LED
CANA_RX	14					I	CAN-A Receive
SPIA_PTE	15					I/O	SPI-A Peripheral Transmit Enable (PTE)

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO62	0, 4, 8, 12	K15	108	H10	57	I/O	General-Purpose Input Output 62
SCIA_RX	1					I	SCI-A Receive Data
EMIF1_D22	2					I/O	External Memory Interface 1 data line 22
ESC_MDIO_CLK	3					O	EtherCAT MDIO Clock
EQEP3_A	5					I	eQEP-3 Input A
CANA_RX	6					I	CAN-A Receive
SD2_D4	7					I	SDFM-2 Channel 4 Data Input
EMIF1_D7	9					I/O	External Memory Interface 1 data line 7
ESC_LED_STATE_RUN	10					O	EtherCAT LED State Run
CANA_TX	14					O	CAN-A Transmit
GPIO63	0, 4, 8, 12	K14	109	G13	58	I/O	General-Purpose Input Output 63
SCIA_TX	1					O	SCI-A Transmit Data
EMIF1_D21	2					I/O	External Memory Interface 1 data line 21
EPWM9_A	3					O	ePWM-9 Output A
EQEP3_B	5					I	eQEP-3 Input B
CANA_TX	6					O	CAN-A Transmit
SD2_C4	7					I	SDFM-2 Channel 4 Clock Input
EMIF1_RNW	9					O	External Memory Interface 1 read not write
EMIF1_BA0	10					O	External Memory Interface 1 bank address 0
SD1_D1	13					I	SDFM-1 Channel 1 Data Input
ESC_RX1_DATA0	14					I	EtherCAT MII Receive-1 Data-0
SPIB_PICO	15					I/O	SPI-B Peripheral In, Controller Out (PICO)
GPIO64	0, 4, 8, 12	K13	110	G12	59	I/O	General-Purpose Input Output 64
EMIF1_D20	2					I/O	External Memory Interface 1 data line 20
EPWM9_B	3					O	ePWM-9 Output B
EQEP3_STROBE	5					I/O	eQEP-3 Strobe
SCIA_RX	6					I	SCI-A Receive Data
EMIF1_WAIT	9					I	External Memory Interface 1 Asynchronous SRAM WAIT
EMIF1_BA1	10					O	External Memory Interface 1 bank address 1
SD1_C1	13					I	SDFM-1 Channel 1 Clock Input
ESC_RX1_DATA1	14					I	EtherCAT MII Receive-1 Data-1
SPIB_POCI	15					I/O	SPI-B Peripheral Out, Controller In (POCI)
GPIO65	0, 4, 8, 12	K12	111	G11	60	I/O	General-Purpose Input Output 65
EMIF1_D19	2					I/O	External Memory Interface 1 data line 19
EPWM10_A	3					O	ePWM-10 Output A
EQEP3_INDEX	5					I/O	eQEP-3 Index
SCIA_TX	6					O	SCI-A Transmit Data
EMIF1_WEn	9					O	External Memory Interface 1 write enable
FSITXB_CLK	11					O	FSITX-B Output Clock
SD1_D2	13					I	SDFM-1 Channel 2 Data Input
ESC_RX1_DATA2	14					I	EtherCAT MII Receive-1 Data-2
SPIB_CLK	15					I/O	SPI-B Clock

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO66	0, 4, 8, 12	K11	112	G10	61	I/O	General-Purpose Input Output 66
EQEP6_B	1					I	eQEP-6 Input B
EMIF1_D18	2					I/O	External Memory Interface 1 data line 18
EPWM10_B	3					O	ePWM-10 Output B
I2CB_SDA	6					I/OD	I2C-B Open-Drain Bidirectional Data
EMIF1_OEn	9					O	External Memory Interface 1 output enable
FSITXB_D1	11					O	FSITX-B Optional Additional Data Output
SD1_C2	13					I	SDFM-1 Channel 2 Clock Input
ESC_RX1_DATA3	14					I	EtherCAT MII Receive-1 Data-3
SPIB_PTE	15					I/O	SPI-B Peripheral Transmit Enable (PTE)
GPIO67	0, 4, 8, 12	D15	132			I/O	General-Purpose Input Output 67
EMIF1_D17	2					I/O	External Memory Interface 1 data line 17
EPWM17_A	3					O	ePWM-17 Output A
LINB_TX	5					O	LIN-B Transmit
ESC_I2C_SDA	11					I/OC	EtherCAT I2C Data
SD1_D3	13					I	SDFM-1 Channel 3 Data Input
GPIO68	0, 4, 8, 12	C16	133	B13		I/O	General-Purpose Input Output 68
EMIF1_D16	2					I/O	External Memory Interface 1 data line 16
EPWM17_B	3					O	ePWM-17 Output B
LINB_RX	5					I	LIN-B Receive
ESC_I2C_SCL	11					I/OC	EtherCAT I2C Clock
SD1_C3	13					I	SDFM-1 Channel 3 Clock Input
ESC_PHY1_LINKSTATUS	14					I	EtherCAT PHY-1 Link Status
GPIO69	0, 4, 8, 12	B16	134	B12	75	I/O	General-Purpose Input Output 69
EMIF1_D15	2					I/O	External Memory Interface 1 data line 15
EPWM11_A	3					O	ePWM-11 Output A
I2CB_SCL	6					I/OD	I2C-B Open-Drain Bidirectional Clock
FSITXB_D0	11					O	FSITX-B Primary Data Output
SD1_D4	13					I	SDFM-1 Channel 4 Data Input
ESC_RX1_CLK	14					I	EtherCAT MII Receive-1 Clock
SPIC_PICO	15					I/O	SPI-C Peripheral In, Controller Out (PICO)
GPIO70	0, 4, 8, 12	C15	135	A12	76	I/O	General-Purpose Input Output 70
EMIF1_D14	2					I/O	External Memory Interface 1 data line 14
EPWM11_B	3					O	ePWM-11 Output B
CANA_RX	5					I	CAN-A Receive
SCIB_TX	6					O	SCI-B Transmit Data
UARTB_TX	7					I/O	UART-B Serial Data Transmit
MCANA_RX	9					I	CAN/CAN FD-A Receive
FSIRXB_D0	11					I	FSIRX-B Primary Data Input
SD1_C4	13					I	SDFM-1 Channel 4 Clock Input
ESC_RX1_DV	14					I	EtherCAT MII Receive-1 Data Valid
SPIC_POCI	15					I/O	SPI-C Peripheral Out, Controller In (POCI)

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO71	0, 4, 8, 12	B15	136	B11	77	I/O	General-Purpose Input Output 71
EMIF1_D13	2					I/O	External Memory Interface 1 data line 13
EPWM12_A	3					O	ePWM-12 Output A
CANA_TX	5					O	CAN-A Transmit
SCIB_RX	6					I	SCI-B Receive Data
UARTB_RX	7					I/O	UART-B Serial Data Receive
MCANA_TX	9					O	CAN/CAN FD-A Transmit
SD3_D1	13					I	SDFM-3 Channel 1 Data Input
ESC_RX1_ERR	14					I	EtherCAT MII Receive-1 Error
SPIC_CLK	15					I/O	SPI-C Clock
GPIO72	0, 4, 8, 12	A15	139	A11	80	I/O	General-Purpose Input Output 72
EQEP6_STROBE	1					I/O	eQEP-6 Strobe
EMIF1_D12	2					I/O	External Memory Interface 1 data line 12
EPWM12_B	3					O	ePWM-12 Output B
OUTPUTXBAR8	5					O	Output X-BAR Output 8
UARTA_TX	6					I/O	UART-A Serial Data Transmit
MCANB_RX	9					I	CAN/CAN FD-B Receive
SD3_C1	13					I	SDFM-3 Channel 1 Clock Input
ESC_TX1_DATA3	14					O	EtherCAT MII Transmit-1 Data-3
SPIC_PTE	15					I/O	SPI-C Peripheral Transmit Enable (PTE)
GPIO73	0, 4, 8, 12	D14	140	C10	81	I/O	General-Purpose Input Output 73
EQEP6_INDEX	1					I/O	eQEP-6 Index
EMIF1_D11	2					I/O	External Memory Interface 1 data line 11
XCLKOUT	3					O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
OUTPUTXBAR6	5					O	Output X-BAR Output 6
UARTA_RX	6					I/O	UART-A Serial Data Receive
EPWM5_B	7					O	ePWM-5 Output B
MCANB_TX	9					O	CAN/CAN FD-B Transmit
SD4_D4	10					I	SDFM-4 Channel 4 Data Input
SD2_D2	13					I	SDFM-2 Channel 2 Data Input
ESC_TX1_DATA2	14					O	EtherCAT MII Transmit-1 Data-2
GPIO74	0, 4, 8, 12	C14	141	B10		I/O	General-Purpose Input Output 74
EPWM8_A	1					O	ePWM-8 Output A
EMIF1_D10	2					I/O	External Memory Interface 1 data line 10
EQEP5_A	6					I	eQEP-5 Input A
MCANA_TX	9					O	CAN/CAN FD-A Transmit
SD1_D4	10					I	SDFM-1 Channel 4 Data Input
SD2_C2	13					I	SDFM-2 Channel 2 Clock Input
ESC_TX1_DATA1	14					O	EtherCAT MII Transmit-1 Data-1
GPIO75	0, 4, 8, 12	B14	142	A10		I/O	General-Purpose Input Output 75
EPWM8_B	1					O	ePWM-8 Output B
EMIF1_D9	2					I/O	External Memory Interface 1 data line 9
EQEP5_B	6					I	eQEP-5 Input B
SPID_CLK	7					I/O	SPI-D Clock
MCANA_RX	9					I	CAN/CAN FD-A Receive
CLB_OUTPUTXBAR8	10					O	CLB Output X-BAR Output 8
SD2_D3	13					I	SDFM-2 Channel 3 Data Input
ESC_TX1_DATA0	14					O	EtherCAT MII Transmit-1 Data-0

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO76	0, 4, 8, 12	A14	143	E9		I/O	General-Purpose Input Output 76
EPWM9_A	1					O	ePWM-9 Output A
EMIF1_D8	2					I/O	External Memory Interface 1 data line 8
EQEP5_STROBE	6					I/O	eQEP-5 Strobe
SD3_C1	7					I	SDFM-3 Channel 1 Clock Input
SD4_D4	10					I	SDFM-4 Channel 4 Data Input
SD2_C3	13					I	SDFM-2 Channel 3 Clock Input
ESC_PHY_RESETn	14					O	EtherCAT PHY Active Low Reset
GPIO77	0, 4, 8, 12	F13	144	D9		I/O	General-Purpose Input Output 77
EPWM9_B	1					O	ePWM-9 Output B
EMIF1_D7	2					I/O	External Memory Interface 1 data line 7
EQEP5_INDEX	6					I/O	eQEP-5 Index
SD3_D1	7					I	SDFM-3 Channel 1 Data Input
SD1_D4	10					I	SDFM-1 Channel 4 Data Input
SD2_D4	13					I	SDFM-2 Channel 4 Data Input
ESC_RX0_CLK	14					I	EtherCAT MII Receive-0 Clock
GPIO78	0, 4, 8, 12	E13	145	C9	82	I/O	General-Purpose Input Output 78
EPWM10_A	1					O	ePWM-10 Output A
EMIF1_D6	2					I/O	External Memory Interface 1 data line 6
EQEP2_A	6					I	eQEP-2 Input A
SD3_C2	7					I	SDFM-3 Channel 2 Clock Input
SD4_D4	10					I	SDFM-4 Channel 4 Data Input
SD2_C4	13					I	SDFM-2 Channel 4 Clock Input
ESC_RX0_DV	14					I	EtherCAT MII Receive-0 Data Valid
GPIO79	0, 4, 8, 12	D13	146	B9		I/O	General-Purpose Input Output 79
EPWM10_B	1					O	ePWM-10 Output B
EMIF1_D5	2					I/O	External Memory Interface 1 data line 5
ERRORSTS	5					O	Error Status Output. This signal requires an external pulldown.
EQEP2_B	6					I	eQEP-2 Input B
SD3_D2	7					I	SDFM-3 Channel 2 Data Input
SD2_D1	13					I	SDFM-2 Channel 1 Data Input
ESC_RX0_ERR	14					I	EtherCAT MII Receive-0 Error
GPIO80	0, 4, 8, 12	A13	148	E8	83	I/O	General-Purpose Input Output 80
EPWM11_A	1					O	ePWM-11 Output A
EMIF1_D4	2					I/O	External Memory Interface 1 data line 4
ERRORSTS	5					O	Error Status Output. This signal requires an external pulldown.
EQEP2_STROBE	6					I/O	eQEP-2 Strobe
SD3_C3	7					I	SDFM-3 Channel 3 Clock Input
SD1_D4	10					I	SDFM-1 Channel 4 Data Input
SD2_C1	13					I	SDFM-2 Channel 1 Clock Input
ESC_RX0_DATA0	14					I	EtherCAT MII Receive-0 Data-0
GPIO81	0, 4, 8, 12	F12	149			I/O	General-Purpose Input Output 81
EPWM11_B	1					O	ePWM-11 Output B
EMIF1_D3	2					I/O	External Memory Interface 1 data line 3
EQEP2_INDEX	6					I/O	eQEP-2 Index
SD3_D3	7					I	SDFM-3 Channel 3 Data Input
ESC_RX0_DATA1	14					I	EtherCAT MII Receive-0 Data-1

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO82	0, 4, 8, 12	E12	150	D8		I/O	General-Purpose Input Output 82
EPWM12_A	1					O	ePWM-12 Output A
EMIF1_D2	2					I/O	External Memory Interface 1 data line 2
SD3_C2	13					I	SDFM-3 Channel 2 Clock Input
ESC_RX0_DATA2	14					I	EtherCAT MII Receive-0 Data-2
GPIO83	0, 4, 8, 12	D12	151	C8		I/O	General-Purpose Input Output 83
EPWM12_B	1					O	ePWM-12 Output B
EMIF1_D1	2					I/O	External Memory Interface 1 data line 1
SD3_D2	13					I	SDFM-3 Channel 2 Data Input
ESC_RX0_DATA3	14					I	EtherCAT MII Receive-0 Data-3
GPIO84	0, 4, 8, 12	D9	154	A8	85	I/O	General-Purpose Input Output 84
EPWM12_B	1					O	ePWM-12 Output B
EMIF1_D1	2					I/O	External Memory Interface 1 data line 1
EMIF1_CS4n	3					O	External Memory Interface 1 chip select 4
SCIA_TX	5					O	SCI-A Transmit Data
EQEP6_A	6					I	eQEP-6 Input A
SD3_D2	9					I	SDFM-3 Channel 2 Data Input
UARTA_TX	11					I/O	UART-A Serial Data Transmit
SD3_C2	13					I	SDFM-3 Channel 2 Clock Input
ESC_TX0_ENA	14					I/O	EtherCAT MII Transmit-0 Enable
ESC_RX0_DATA3	15					I	EtherCAT MII Receive-0 Data-3
GPIO85	0, 4, 8, 12	C9	155	A7	86	I/O	General-Purpose Input Output 85
EPWM13_A	1					O	ePWM-13 Output A
EMIF1_D0	2					I/O	External Memory Interface 1 data line 0
SCIA_RX	5					I	SCI-A Receive Data
EQEP6_B	6					I	eQEP-6 Input B
SD3_D1	7					I	SDFM-3 Channel 1 Data Input
UARTA_RX	11					I/O	UART-A Serial Data Receive
SD3_D3	13					I	SDFM-3 Channel 3 Data Input
ESC_TX0_CLK	14					I	EtherCAT MII Transmit-0 Clock
EMIF1_DQM2	15					O	External Memory Interface 1 Input/output mask for byte 2
GPIO86	0, 4, 8, 12	B9	156	B7	87	I/O	General-Purpose Input Output 86
EPWM13_B	1					O	ePWM-13 Output B
EMIF1_A13	2					O	External Memory Interface 1 address line 13
EMIF1_CAS	3					O	External Memory Interface 1 column address strobe
SCIB_TX	5					O	SCI-B Transmit Data
EQEP6_STROBE	6					I/O	eQEP-6 Strobe
SD3_C3	13					I	SDFM-3 Channel 3 Clock Input
ESC_PHY0_LINKSTATUS	14					I	EtherCAT PHY-0 Link Status
GPIO87	0, 4, 8, 12	A9	157	C7	88	I/O	General-Purpose Input Output 87
EPWM14_A	1					O	ePWM-14 Output A
EMIF1_A14	2					O	External Memory Interface 1 address line 14
EMIF1_RAS	3					O	External Memory Interface 1 row address strobe
SCIB_RX	5					I	SCI-B Receive Data
EQEP6_INDEX	6					I/O	eQEP-6 Index
EMIF1_DQM3	9					O	External Memory Interface 1 Input/output mask for byte 3
SD3_D4	13					I	SDFM-3 Channel 4 Data Input
ESC_TX0_DATA0	14					O	EtherCAT MII Transmit-0 Data-0

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO88	0, 4, 8, 12	B6	170	C5		I/O	General-Purpose Input Output 88
EPWM14_B	1					O	ePWM-14 Output B
EMIF1_A15	2					O	External Memory Interface 1 address line 15
EMIF1_DQM0	3					O	External Memory Interface 1 Input/output mask for byte 0
EMIF1_DQM1	9					O	External Memory Interface 1 Input/output mask for byte 1
SD3_C4	13					I	SDFM-3 Channel 4 Clock Input
ESC_TX0_DATA1	14					O	EtherCAT MII Transmit-0 Data-1
GPIO89	0, 4, 8, 12	C6	171	D5	96	I/O	General-Purpose Input Output 89
EPWM15_A	1					O	ePWM-15 Output A
EMIF1_A16	2					O	External Memory Interface 1 address line 16
EMIF1_DQM1	3					O	External Memory Interface 1 Input/output mask for byte 1
SD1_D3	7					I	SDFM-1 Channel 3 Data Input
EMIF1_CAS	9					O	External Memory Interface 1 column address strobe
SD4_D1	13					I	SDFM-4 Channel 1 Data Input
ESC_TX0_DATA2	14					O	EtherCAT MII Transmit-0 Data-2
SPID_PTE	15					I/O	SPI-D Peripheral Transmit Enable (PTE)
GPIO90	0, 4, 8, 12	D6	172	E5	97	I/O	General-Purpose Input Output 90
EPWM15_B	1					O	ePWM-15 Output B
EMIF1_A17	2					O	External Memory Interface 1 address line 17
EMIF1_DQM2	3					O	External Memory Interface 1 Input/output mask for byte 2
SD1_C3	7					I	SDFM-1 Channel 3 Clock Input
EMIF1_RAS	9					O	External Memory Interface 1 row address strobe
SD4_C1	13					I	SDFM-4 Channel 1 Clock Input
ESC_TX0_DATA3	14					O	EtherCAT MII Transmit-0 Data-3
SPID_CLK	15					I/O	SPI-D Clock
GPIO91	0, 4, 8, 12	E6	173	B4	98	I/O	General-Purpose Input Output 91
EPWM16_A	1					O	ePWM-16 Output A
EMIF1_A18	2					O	External Memory Interface 1 address line 18
EMIF1_DQM3	3					O	External Memory Interface 1 Input/output mask for byte 3
I2CA_SDA	6					I/OD	I2C-A Open-Drain Bidirectional Data
SD4_D2	7					I	SDFM-4 Channel 2 Data Input
EMIF1_DQM2	9					O	External Memory Interface 1 Input/output mask for byte 2
PMBUSA_SCL	10					I/OD	PMBus-A Open-Drain Bidirectional Clock
CLB_OUTPUTXBAR1	14					O	CLB Output X-BAR Output 1
SPID_PICO	15					I/O	SPI-D Peripheral In, Controller Out (PICO)

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO92	0, 4, 8, 12	A5	174	A4	99	I/O	General-Purpose Input Output 92
EPWM16_B	1					O	ePWM-16 Output B
EMIF1_A19	2					O	External Memory Interface 1 address line 19
EMIF1_BA1	3					O	External Memory Interface 1 bank address 1
I2CA_SCL	6					I/OD	I2C-A Open-Drain Bidirectional Clock
SD4_C2	7					I	SDFM-4 Channel 2 Clock Input
EMIF1_DQM0	9					O	External Memory Interface 1 Input/output mask for byte 0
PMBUSA_SDA	10					I/OD	PMBus-A Open-Drain Bidirectional Data
FSIRXD_CLK	11					I	FSIRX-D Input Clock
CLB_OUTPUTXBAR2	14					O	CLB Output X-BAR Output 2
SPID_POCI	15					I/O	SPI-D Peripheral Out, Controller In (POCI)
GPIO93	0, 4, 8, 12	C5	175	A3		I/O	General-Purpose Input Output 93
EPWM17_A	1					O	ePWM-17 Output A
EMIF1_BA0	3					O	External Memory Interface 1 bank address 0
SD4_D3	7					I	SDFM-4 Channel 3 Data Input
PMBUSA_ALERT	10					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
ESC_TX1_CLK	11					I	EtherCAT MII Transmit-1 Clock
CLB_OUTPUTXBAR3	14					O	CLB Output X-BAR Output 3
SPID_CLK	15					I/O	SPI-D Clock
GPIO94	0, 4, 8, 12	D5	176	A2		I/O	General-Purpose Input Output 94
EPWM17_B	1					O	ePWM-17 Output B
SD4_C3	7					I	SDFM-4 Channel 3 Clock Input
EMIF1_BA1	9					O	External Memory Interface 1 bank address 1
PMBUSA_CTL	10					I/O	PMBus-A Control Signal - Target Input/Controller Output
ESC_TX1_ENA	11					I/O	EtherCAT MII Transmit-1 Enable
CLB_OUTPUTXBAR4	14					O	CLB Output X-BAR Output 4
SPID_PTE	15					I/O	SPI-D Peripheral Transmit Enable (PTE)
GPIO95	0, 4, 8, 12	A4				I/O	General-Purpose Input Output 95
EPWM18_A	1					O	ePWM-18 Output A
EQEP4_A	2					I	eQEP-4 Input A
SD1_D1	6					I	SDFM-1 Channel 1 Data Input
ESC_GPO10	10					O	EtherCAT General-Purpose Output 10
CLB_OUTPUTXBAR5	14					O	CLB Output X-BAR Output 5
GPIO96	0, 4, 8, 12	B4				I/O	General-Purpose Input Output 96
EPWM18_B	1					O	ePWM-18 Output B
EQEP4_B	2					I	eQEP-4 Input B
EQEP1_A	5					I	eQEP-1 Input A
SD1_C1	6					I	SDFM-1 Channel 1 Clock Input
ESC_GPO11	10					O	EtherCAT General-Purpose Output 11
CLB_OUTPUTXBAR6	14					O	CLB Output X-BAR Output 6
GPIO97	0, 4, 8, 12	C4				I/O	General-Purpose Input Output 97
EQEP4_STROBE	2					I/O	eQEP-4 Strobe
EQEP1_B	5					I	eQEP-1 Input B
SD1_D2	6					I	SDFM-1 Channel 2 Data Input
ESC_GPI17	10					I	EtherCAT General-Purpose Input 17
CLB_OUTPUTXBAR7	14					O	CLB Output X-BAR Output 7

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO98	0, 4, 8, 12	E2				I/O	General-Purpose Input Output 98
EQEP4_INDEX	2					I/O	eQEP-4 Index
EQEP1_STROBE	5					I/O	eQEP-1 Strobe
SD1_C2	6					I	SDFM-1 Channel 2 Clock Input
ESC_GPI18	10					I	EtherCAT General-Purpose Input 18
CLB_OUTPUTXBAR8	14					O	CLB Output X-BAR Output 8
GPIO99	0, 4, 8, 12	C1	17	E4		I/O	General-Purpose Input Output 99
EMIF1_DQM3	2					O	External Memory Interface 1 Input/output mask for byte 3
EPWM8_A	3					O	ePWM-8 Output A
EQEP1_INDEX	5					I/O	eQEP-1 Index
SD4_D4	7					I	SDFM-4 Channel 4 Data Input
ESC_GPI21	10					I	EtherCAT General-Purpose Input 21
EMIF1_D17	14					I/O	External Memory Interface 1 data line 17
GPIO100	0, 4, 8, 12	F4			2	I/O	General-Purpose Input Output 100
SPIA_PICO	1					I/O	SPI-A Peripheral In, Controller Out (PICO)
EMIF1_BA1	2					O	External Memory Interface 1 bank address 1
EPWM9_A	3					O	ePWM-9 Output A
EQEP2_A	5					I	eQEP-2 Input A
SPIC_PICO	6					I/O	SPI-C Peripheral In, Controller Out (PICO)
SD4_C4	7					I	SDFM-4 Channel 4 Clock Input
SD1_D1	9					I	SDFM-1 Channel 1 Data Input
ESC_GPI0	10					I	EtherCAT General-Purpose Input 0
FSIRXD_D1	11					I	FSIRX-D Optional Additional Data Input
FSITXA_D0	13					O	FSITX-A Primary Data Output
EMIF1_D24	14					I/O	External Memory Interface 1 data line 24
GPIO101	0, 4, 8, 12	N9				I/O	General-Purpose Input Output 101
EPWM18_A	1					O	ePWM-18 Output A
EQEP2_B	5					I	eQEP-2 Input B
SPIC_POCI	6					I/O	SPI-C Peripheral Out, Controller In (POCI)
ESC_GPI1	10					I	EtherCAT General-Purpose Input 1
EMIF1_A5	11					O	External Memory Interface 1 address line 5
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output
GPIO102	0, 4, 8, 12	C13				I/O	General-Purpose Input Output 102
EPWM18_B	1					O	ePWM-18 Output B
EQEP2_STROBE	5					I/O	eQEP-2 Strobe
SPIC_CLK	6					I/O	SPI-C Clock
ESC_GPI2	10					I	EtherCAT General-Purpose Input 2
EMIF1_A6	11					O	External Memory Interface 1 address line 6
FSITXA_CLK	13					O	FSITX-A Output Clock
GPIO103	0, 4, 8, 12	G12	126	D10		I/O	General-Purpose Input Output 103
EMIF1_BA0	2					O	External Memory Interface 1 bank address 0
EPWM8_B	3					O	ePWM-8 Output B
EQEP2_INDEX	5					I/O	eQEP-2 Index
SPIC_PTE	6					I/O	SPI-C Peripheral Transmit Enable (PTE)
SD4_C4	7					I	SDFM-4 Channel 4 Clock Input
ESC_GPI3	10					I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13					I	FSIRX-A Primary Data Input

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO104	0, 4, 8, 12	B13	147	A9		I/O	General-Purpose Input Output 104
I2CA_SDA	1					I/OD	I2C-A Open-Drain Bidirectional Data
EPWM18_A	2					O	ePWM-18 Output A
EQEP3_A	5					I	eQEP-3 Input A
SD3_D1	6					I	SDFM-3 Channel 1 Data Input
ESC_GPI4	10					I	EtherCAT General-Purpose Input 4
FSIRXA_D1	13					I	FSIRX-A Optional Additional Data Input
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
GPIO105	0, 4, 8, 12	L16	106	H12		I/O	General-Purpose Input Output 105
I2CA_SCL	1					I/OD	I2C-A Open-Drain Bidirectional Clock
EPWM18_B	2					O	ePWM-18 Output B
EQEP3_B	5					I	eQEP-3 Input B
SD3_C1	6					I	SDFM-3 Channel 1 Clock Input
ESC_GPI5	10					I	EtherCAT General-Purpose Input 5
FSIRXA_CLK	13					I	FSIRX-A Input Clock
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
GPIO106	0, 4, 8, 12	F1	20			I/O	General-Purpose Input Output 106
EPWM16_A	1					O	ePWM-16 Output A
EMIF1_A10	2					O	External Memory Interface 1 address line 10
EQEP3_STROBE	5					I/O	eQEP-3 Strobe
SD3_D2	6					I	SDFM-3 Channel 2 Data Input
ESC_GPI6	10					I	EtherCAT General-Purpose Input 6
FSITXB_D0	13					O	FSITX-B Primary Data Output
GPIO107	0, 4, 8, 12	F2				I/O	General-Purpose Input Output 107
EPWM16_B	1					O	ePWM-16 Output B
EQEP3_INDEX	5					I/O	eQEP-3 Index
SD3_C2	6					I	SDFM-3 Channel 2 Clock Input
ESC_GPI7	10					I	EtherCAT General-Purpose Input 7
FSITXB_D1	13					O	FSITX-B Optional Additional Data Output
GPIO108	0, 4, 8, 12	G2				I/O	General-Purpose Input Output 108
EPWM17_A	1					O	ePWM-17 Output A
EMIF1_A12	2					O	External Memory Interface 1 address line 12
EQEP5_A	5					I	eQEP-5 Input A
SD3_D3	6					I	SDFM-3 Channel 3 Data Input
ESC_GPI8	10					I	EtherCAT General-Purpose Input 8
FSITXB_CLK	13					O	FSITX-B Output Clock
GPIO109	0, 4, 8, 12	G3				I/O	General-Purpose Input Output 109
EPWM17_B	1					O	ePWM-17 Output B
EMIF1_A11	2					O	External Memory Interface 1 address line 11
EQEP5_B	5					I	eQEP-5 Input B
SD3_C3	6					I	SDFM-3 Channel 3 Clock Input
ESC_GPI9	10					I	EtherCAT General-Purpose Input 9
GPIO110	0, 4, 8, 12	H2				I/O	General-Purpose Input Output 110
EMIF1_D31	1					I/O	External Memory Interface 1 data line 31
EQEP5_STROBE	5					I/O	eQEP-5 Strobe
SD3_D4	6					I	SDFM-3 Channel 4 Data Input
ESC_GPI10	10					I	EtherCAT General-Purpose Input 10
FSIRXB_D0	13					I	FSIRX-B Primary Data Input

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO111	0, 4, 8, 12	H3				I/O	General-Purpose Input Output 111
EMIF1_D30	1					I/O	External Memory Interface 1 data line 30
EQEP5_INDEX	5					I/O	eQEP-5 Index
SD3_C4	6					I	SDFM-3 Channel 4 Clock Input
ESC_GPI11	10					I	EtherCAT General-Purpose Input 11
FSIRXB_D1	13					I	FSIRX-B Optional Additional Data Input
GPIO112	0, 4, 8, 12	H4				I/O	General-Purpose Input Output 112
EMIF1_D29	1					I/O	External Memory Interface 1 data line 29
SD1_D3	7					I	SDFM-1 Channel 3 Data Input
ESC_GPI12	10					I	EtherCAT General-Purpose Input 12
FSIRXB_CLK	13					I	FSIRX-B Input Clock
GPIO113	0, 4, 8, 12	J3				I/O	General-Purpose Input Output 113
EMIF1_D28	1					I/O	External Memory Interface 1 data line 28
SD1_C3	7					I	SDFM-1 Channel 3 Clock Input
ESC_GPI13	10					I	EtherCAT General-Purpose Input 13
GPIO114	0, 4, 8, 12	J4				I/O	General-Purpose Input Output 114
EMIF1_D27	1					I/O	External Memory Interface 1 data line 27
SD1_D4	7					I	SDFM-1 Channel 4 Data Input
ESC_GPI14	10					I	EtherCAT General-Purpose Input 14
GPIO115	0, 4, 8, 12	P9				I/O	General-Purpose Input Output 115
EMIF1_D26	1					I/O	External Memory Interface 1 data line 26
OUTPUTXBAR5	5					O	Output X-BAR Output 5
SD1_C4	7					I	SDFM-1 Channel 4 Clock Input
ESC_GPI15	10					I	EtherCAT General-Purpose Input 15
FSIRXC_D0	13					I	FSIRX-C Primary Data Input
GPIO116	0, 4, 8, 12	H11				I/O	General-Purpose Input Output 116
OUTPUTXBAR6	5					O	Output X-BAR Output 6
ESC_GPI16	10					I	EtherCAT General-Purpose Input 16
FSIRXC_D1	13					I	FSIRX-C Optional Additional Data Input
GPIO119	0, 4, 8, 12	M10				I/O	General-Purpose Input Output 119
EMIF1_D25	1					I/O	External Memory Interface 1 data line 25
MCANB_TX	5					O	CAN/CAN FD-B Transmit
ESC_GPI19	10					I	EtherCAT General-Purpose Input 19
FSIRXD_D1	13					I	FSIRX-D Optional Additional Data Input
GPIO120	0, 4, 8, 12	M11				I/O	General-Purpose Input Output 120
EMIF1_D24	1					I/O	External Memory Interface 1 data line 24
MCANB_RX	5					I	CAN/CAN FD-B Receive
ESC_GPI20	10					I	EtherCAT General-Purpose Input 20
FSIRXD_CLK	13					I	FSIRX-D Input Clock
GPIO122	0, 4, 8, 12	L7				I/O	General-Purpose Input Output 122
EMIF1_D23	1					I/O	External Memory Interface 1 data line 23
SPIC_PICO	6					I/O	SPI-C Peripheral In, Controller Out (PICO)
SD1_D1	7					I	SDFM-1 Channel 1 Data Input
ESC_GPI22	10					I	EtherCAT General-Purpose Input 22
GPIO123	0, 4, 8, 12	M7				I/O	General-Purpose Input Output 123
EMIF1_D22	1					I/O	External Memory Interface 1 data line 22
SPIC_POCI	6					I/O	SPI-C Peripheral Out, Controller In (POCI)
SD1_C1	7					I	SDFM-1 Channel 1 Clock Input
ESC_GPI23	10					I	EtherCAT General-Purpose Input 23

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO124	0, 4, 8, 12	L8				I/O	General-Purpose Input Output 124
EMIF1_D21	1					I/O	External Memory Interface 1 data line 21
SPIC_CLK	6					I/O	SPI-C Clock
SD1_D2	7					I	SDFM-1 Channel 2 Data Input
ESC_GPI24	10					I	EtherCAT General-Purpose Input 24
GPIO125	0, 4, 8, 12	M8				I/O	General-Purpose Input Output 125
EMIF1_D20	1					I/O	External Memory Interface 1 data line 20
SPIC_PTE	6					I/O	SPI-C Peripheral Transmit Enable (PTE)
SD1_C2	7					I	SDFM-1 Channel 2 Clock Input
ESC_GPI25	10					I	EtherCAT General-Purpose Input 25
ESC_LATCH0	14					I	EtherCAT Latch Signal Input 0
GPIO126	0, 4, 8, 12	T9				I/O	General-Purpose Input Output 126
EMIF1_D19	1					I/O	External Memory Interface 1 data line 19
SPID_PICO	6					I/O	SPI-D Peripheral In, Controller Out (PICO)
SD1_D3	7					I	SDFM-1 Channel 3 Data Input
ESC_GPI26	10					I	EtherCAT General-Purpose Input 26
ESC_LATCH1	14					I	EtherCAT Latch Signal Input 1
GPIO127	0, 4, 8, 12	R9				I/O	General-Purpose Input Output 127
EMIF1_D18	1					I/O	External Memory Interface 1 data line 18
SPID_POCI	6					I/O	SPI-D Peripheral Out, Controller In (POCI)
SD1_C3	7					I	SDFM-1 Channel 3 Clock Input
ESC_GPI27	10					I	EtherCAT General-Purpose Input 27
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
GPIO128	0, 4, 8, 12	M9				I/O	General-Purpose Input Output 128
EMIF1_D17	1					I/O	External Memory Interface 1 data line 17
SPID_CLK	6					I/O	SPI-D Clock
SD1_D4	7					I	SDFM-1 Channel 4 Data Input
ESC_GPI28	10					I	EtherCAT General-Purpose Input 28
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
GPIO129	0, 4, 8, 12	L9				I/O	General-Purpose Input Output 129
EMIF1_D16	1					I/O	External Memory Interface 1 data line 16
SPID_PTE	6					I/O	SPI-D Peripheral Transmit Enable (PTE)
SD1_C4	7					I	SDFM-1 Channel 4 Clock Input
ESC_GPI29	10					I	EtherCAT General-Purpose Input 29
ESC_TX1_ENA	14					I/O	EtherCAT MII Transmit-1 Enable
GPIO130	0, 4, 8, 12	T10				I/O	General-Purpose Input Output 130
EPWM13_A	1					O	ePWM-13 Output A
SD2_D1	7					I	SDFM-2 Channel 1 Data Input
ESC_GPI30	10					I	EtherCAT General-Purpose Input 30
ESC_TX1_CLK	14					I	EtherCAT MII Transmit-1 Clock
GPIO131	0, 4, 8, 12	N13				I/O	General-Purpose Input Output 131
EPWM13_B	1					O	ePWM-13 Output B
SD2_C1	7					I	SDFM-2 Channel 1 Clock Input
ESC_GPI31	10					I	EtherCAT General-Purpose Input 31
ESC_TX1_DATA0	14					O	EtherCAT MII Transmit-1 Data-0
GPIO132	0, 4, 8, 12	T14				I/O	General-Purpose Input Output 132
EPWM14_A	1					O	ePWM-14 Output A
SD2_D2	7					I	SDFM-2 Channel 2 Data Input
ESC_GPO0	10					O	EtherCAT General-Purpose Output 0
ESC_TX1_DATA1	14					O	EtherCAT MII Transmit-1 Data-1

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO133	0, 4, 8, 12	J15	118	F13		I/O	General-Purpose Input Output 133
EMIF1_A11	1					O	External Memory Interface 1 address line 11
EPWM9_A	2					O	ePWM-9 Output A
SD2_C2	7					I	SDFM-2 Channel 2 Clock Input
ESC_LED_STATE_RUN	11					O	EtherCAT LED State Run
GPIO134	0, 4, 8, 12	R14				I/O	General-Purpose Input Output 134
EPWM14_B	1					O	ePWM-14 Output B
SD2_D3	7					I	SDFM-2 Channel 3 Data Input
ESC_GPO1	10					O	EtherCAT General-Purpose Output 1
SD2_C1	13					I	SDFM-2 Channel 1 Clock Input
ESC_TX1_DATA2	14					O	EtherCAT MII Transmit-1 Data-2
GPIO141	0, 4, 8, 12	H13				I/O	General-Purpose Input Output 141
EPWM15_A	1					O	ePWM-15 Output A
SCIB_TX	6					O	SCI-B Transmit Data
ESC_GPO8	10					O	EtherCAT General-Purpose Output 8
ESC_RX1_DATA2	14					I	EtherCAT MII Receive-1 Data-2
GPIO142	0, 4, 8, 12	H14				I/O	General-Purpose Input Output 142
EPWM15_B	1					O	ePWM-15 Output B
SCIB_RX	6					I	SCI-B Receive Data
ESC_GPO9	10					O	EtherCAT General-Purpose Output 9
ESC_RX1_DATA3	14					I	EtherCAT MII Receive-1 Data-3
GPIO145	0, 4, 8, 12	H15				I/O	General-Purpose Input Output 145
EPWM1_A	1					O	ePWM-1 Output A
MCANB_TX	6					O	CAN/CAN FD-B Transmit
ESC_GPO12	10					O	EtherCAT General-Purpose Output 12
ESC_LED_ERR	14					O	EtherCAT Error LED
GPIO146	0, 4, 8, 12	H16				I/O	General-Purpose Input Output 146
EPWM1_B	1					O	ePWM-1 Output B
MCANB_RX	6					I	CAN/CAN FD-B Receive
ESC_GPO13	10					O	EtherCAT General-Purpose Output 13
ESC_LED_RUN	14					O	EtherCAT Run LED
GPIO147	0, 4, 8, 12	H12				I/O	General-Purpose Input Output 147
EPWM2_A	1					O	ePWM-2 Output A
EQEP5_A	6					I	eQEP-5 Input A
ESC_GPO14	10					O	EtherCAT General-Purpose Output 14
ESC_LED_STATE_RUN	14					O	EtherCAT LED State Run
GPIO148	0, 4, 8, 12	C12				I/O	General-Purpose Input Output 148
EPWM2_B	1					O	ePWM-2 Output B
EQEP5_B	6					I	eQEP-5 Input B
ESC_GPO15	10					O	EtherCAT General-Purpose Output 15
ESC_PHY0_LINKSTATUS	14					I	EtherCAT PHY-0 Link Status
GPIO149	0, 4, 8, 12	B12				I/O	General-Purpose Input Output 149
EPWM3_A	1					O	ePWM-3 Output A
EQEP5_STROBE	6					I/O	eQEP-5 Strobe
ESC_GPO16	10					O	EtherCAT General-Purpose Output 16
ESC_PHY1_LINKSTATUS	14					I	EtherCAT PHY-1 Link Status

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO150	0, 4, 8, 12	A12				I/O	General-Purpose Input Output 150
EPWM3_B	1					O	ePWM-3 Output B
EQEP5_INDEX	6					I/O	eQEP-5 Index
ESC_GPO17	10					O	EtherCAT General-Purpose Output 17
ESC_I2C_SDA	14					I/OC	EtherCAT I2C Data
GPIO151	0, 4, 8, 12	F11				I/O	General-Purpose Input Output 151
EPWM4_A	1					O	ePWM-4 Output A
PMBUSA_SCL	6					I/OD	PMBus-A Open-Drain Bidirectional Clock
ESC_GPO18	10					O	EtherCAT General-Purpose Output 18
FSITXA_D0	13					O	FSITX-A Primary Data Output
ESC_I2C_SCL	14					I/OC	EtherCAT I2C Clock
GPIO152	0, 4, 8, 12	E11				I/O	General-Purpose Input Output 152
EPWM4_B	1					O	ePWM-4 Output B
PMBUSA_SDA	6					I/OD	PMBus-A Open-Drain Bidirectional Data
ESC_GPO19	10					O	EtherCAT General-Purpose Output 19
FSITXA_D1	13					O	FSITX-A Optional Additional Data Output
ESC_MDIO_CLK	14					O	EtherCAT MDIO Clock
GPIO153	0, 4, 8, 12	D11				I/O	General-Purpose Input Output 153
EPWM5_A	1					O	ePWM-5 Output A
PMBUSA_ALERT	6					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
ESC_GPO20	10					O	EtherCAT General-Purpose Output 20
FSITXA_CLK	13					O	FSITX-A Output Clock
ESC_MDIO_DATA	14					I/O	EtherCAT MDIO Data
GPIO154	0, 4, 8, 12	C11				I/O	General-Purpose Input Output 154
EPWM5_B	1					O	ePWM-5 Output B
PMBUSA_CTL	6					I/O	PMBus-A Control Signal - Target Input/Controller Output
ESC_GPO21	10					O	EtherCAT General-Purpose Output 21
FSIRXA_D0	13					I	FSIRX-A Primary Data Input
ESC_PHY_CLK	14					O	EtherCAT PHY Clock
GPIO155	0, 4, 8, 12	B11				I/O	General-Purpose Input Output 155
EPWM6_A	1					O	ePWM-6 Output A
ESC_GPO22	10					O	EtherCAT General-Purpose Output 22
FSIRXA_D1	13					I	FSIRX-A Optional Additional Data Input
ESC_PHY_RESETn	14					O	EtherCAT PHY Active Low Reset
GPIO156	0, 4, 8, 12	A11				I/O	General-Purpose Input Output 156
EPWM6_B	1					O	ePWM-6 Output B
ESC_GPO23	10					O	EtherCAT General-Purpose Output 23
FSIRXA_CLK	13					I	FSIRX-A Input Clock
ESC_TX0_ENA	14					I/O	EtherCAT MII Transmit-0 Enable
GPIO157	0, 4, 8, 12	E10				I/O	General-Purpose Input Output 157
EPWM7_A	1					O	ePWM-7 Output A
ESC_GPO24	10					O	EtherCAT General-Purpose Output 24
FSITXB_D0	13					O	FSITX-B Primary Data Output
ESC_TX0_CLK	14					I	EtherCAT MII Transmit-0 Clock
GPIO158	0, 4, 8, 12	D10				I/O	General-Purpose Input Output 158
EPWM7_B	1					O	ePWM-7 Output B
ESC_GPO25	10					O	EtherCAT General-Purpose Output 25
FSITXB_D1	13					O	FSITX-B Optional Additional Data Output
ESC_TX0_DATA0	14					O	EtherCAT MII Transmit-0 Data-0

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO159	0, 4, 8, 12	C10				I/O	General-Purpose Input Output 159
EPWM8_A	1					O	ePWM-8 Output A
ESC_GPO26	10					O	EtherCAT General-Purpose Output 26
FSITXB_CLK	13					O	FSITX-B Output Clock
ESC_TX0_DATA1	14					O	EtherCAT MII Transmit-0 Data-1
GPIO160	0, 4, 8, 12	B10				I/O	General-Purpose Input Output 160
EPWM8_B	1					O	ePWM-8 Output B
ESC_GPO27	10					O	EtherCAT General-Purpose Output 27
FSIRXB_D0	13					I	FSIRX-B Primary Data Input
ESC_TX0_DATA2	14					O	EtherCAT MII Transmit-0 Data-2
GPIO161	0, 4, 8, 12	E9				I/O	General-Purpose Input Output 161
EPWM9_A	1					O	ePWM-9 Output A
ESC_GPO28	10					O	EtherCAT General-Purpose Output 28
FSIRXB_D1	13					I	FSIRX-B Optional Additional Data Input
ESC_TX0_DATA3	14					O	EtherCAT MII Transmit-0 Data-3
GPIO162	0, 4, 8, 12	A8				I/O	General-Purpose Input Output 162
EPWM9_B	1					O	ePWM-9 Output B
ESC_GPO29	10					O	EtherCAT General-Purpose Output 29
FSIRXB_CLK	13					I	FSIRX-B Input Clock
ESC_RX0_DV	14					I	EtherCAT MII Receive-0 Data Valid
GPIO163	0, 4, 8, 12	B8				I/O	General-Purpose Input Output 163
EPWM10_A	1					O	ePWM-10 Output A
ESC_GPO30	10					O	EtherCAT General-Purpose Output 30
FSIRXC_D0	13					I	FSIRX-C Primary Data Input
ESC_RX0_CLK	14					I	EtherCAT MII Receive-0 Clock
GPIO164	0, 4, 8, 12	C8				I/O	General-Purpose Input Output 164
EPWM10_B	1					O	ePWM-10 Output B
ESC_GPO31	10					O	EtherCAT General-Purpose Output 31
FSIRXC_D1	13					I	FSIRX-C Optional Additional Data Input
ESC_RX0_ERR	14					I	EtherCAT MII Receive-0 Error
GPIO165	0, 4, 8, 12	F6				I/O	General-Purpose Input Output 165
EPWM11_A	1					O	ePWM-11 Output A
FSIRXC_CLK	13					I	FSIRX-C Input Clock
ESC_RX0_DATA0	14					I	EtherCAT MII Receive-0 Data-0
GPIO166	0, 4, 8, 12	B5				I/O	General-Purpose Input Output 166
EPWM11_B	1					O	ePWM-11 Output B
FSIRXD_D0	13					I	FSIRX-D Primary Data Input
ESC_RX0_DATA1	14					I	EtherCAT MII Receive-0 Data-1
GPIO167	0, 4, 8, 12	E5				I/O	General-Purpose Input Output 167
EPWM12_A	1					O	ePWM-12 Output A
FSIRXD_D1	13					I	FSIRX-D Optional Additional Data Input
ESC_RX0_DATA2	14					I	EtherCAT MII Receive-0 Data-2
GPIO168	0, 4, 8, 12	F5				I/O	General-Purpose Input Output 168
EPWM12_B	1					O	ePWM-12 Output B
FSIRXD_CLK	13					I	FSIRX-D Input Clock
ESC_RX0_DATA3	14					I	EtherCAT MII Receive-0 Data-3

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO198	0, 4, 8, 12	K4	26	G4		I/O	General-Purpose Input Output 198 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP1_A	1					I	eQEP-1 Input A
EPWM9_B	2					O	ePWM-9 Output B
SPIA_PICO	3					I/O	SPI-A Peripheral In, Controller Out (PICO)
ESC_PDI_UC_IRQ	14					O	EtherCAT PDI IRQ Interrupt Line
GPIO199	0, 4, 8, 12	H1	22	F1	9	I/O	General-Purpose Input Output 199 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP1_STROBE	1					I/O	eQEP-1 Strobe
EPWM17_A	2					O	ePWM-17 Output A
SCIB_TX	3					O	SCI-B Transmit Data
EPWM12_A	5					O	ePWM-12 Output A
SPIB_CLK	6					I/O	SPI-B Clock
SD1_D4	7					I	SDFM-1 Channel 4 Data Input
MCANA_TX	9					O	CAN/CAN FD-A Transmit
EMIF1_RAS	10					O	External Memory Interface 1 row address strobe
SPIC_CLK	14					I/O	SPI-C Clock
GPIO200	0, 4, 8, 12	J1	23	G1	10	I/O	General-Purpose Input Output 200 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP1_INDEX	1					I/O	eQEP-1 Index
EPWM17_B	2					O	ePWM-17 Output B
SCIB_RX	3					I	SCI-B Receive Data
EPWM12_B	5					O	ePWM-12 Output B
SPIB_PTE	6					I/O	SPI-B Peripheral Transmit Enable (PTE)
SD1_C4	7					I	SDFM-1 Channel 4 Clock Input
MCANA_RX	9					I	CAN/CAN FD-A Receive
EMIF1_CAS	10					O	External Memory Interface 1 column address strobe
ESC_TX1_DATA1	11					O	EtherCAT MII Transmit-1 Data-1
SPIC_PTE	14					I/O	SPI-C Peripheral Transmit Enable (PTE)
GPIO201	0, 4, 8, 12	J2	24	G2		I/O	General-Purpose Input Output 201 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR1	1					O	Output X-BAR Output 1
EQEP2_A	2					I	eQEP-2 Input A
EPWM18_A	3					O	ePWM-18 Output A
LINB_TX	5					O	LIN-B Transmit
SPIB_PICO	6					I/O	SPI-B Peripheral In, Controller Out (PICO)
SD2_D1	7					I	SDFM-2 Channel 1 Data Input
PMBUSA_SCL	9					I/OD	PMBus-A Open-Drain Bidirectional Clock
EMIF1_DQM0	10					O	External Memory Interface 1 Input/output mask for byte 0
ESC_TX1_DATA2	11					O	EtherCAT MII Transmit-1 Data-2
EPWM13_A	13					O	ePWM-13 Output A

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO202	0, 4, 8, 12	K3	25	G3		I/O	General-Purpose Input Output 202 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR2	1					O	Output X-BAR Output 2
EQEP2_B	2					I	eQEP-2 Input B
EPWM18_B	3					O	ePWM-18 Output B
LINB_RX	5					I	LIN-B Receive
SPIB_POCI	6					I/O	SPI-B Peripheral Out, Controller In (POCI)
SD2_C1	7					I	SDFM-2 Channel 1 Clock Input
PMBUSA_SDA	9					I/OD	PMBus-A Open-Drain Bidirectional Data
EMIF1_DQM1	10					O	External Memory Interface 1 Input/output mask for byte 1
ESC_TX1_DATA3	11					O	EtherCAT MII Transmit-1 Data-3
EPWM13_B	13					O	ePWM-13 Output B
FSITXA_D1	14					O	FSITX-A Optional Additional Data Output
GPIO203	0, 4, 8, 12	K5	27	G5	11	I/O	General-Purpose Input Output 203 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR3	1, 5					O	Output X-BAR Output 3
EQEP2_INDEX	2					I/O	eQEP-2 Index
SPIA_POCI	3					I/O	SPI-A Peripheral Out, Controller In (POCI)
SPIB_CLK	6					I/O	SPI-B Clock
SD3_D1	7					I	SDFM-3 Channel 1 Data Input
PMBUSA_ALERT	9					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
EMIF1_DQM2	10					O	External Memory Interface 1 Input/output mask for byte 2
ESC_MDIO_CLK	11					O	EtherCAT MDIO Clock
EPWM14_A	13					O	ePWM-14 Output A
FSITXA_D0	14					O	FSITX-A Primary Data Output
EPWM8_B	15					O	ePWM-8 Output B
GPIO204	0, 4, 8, 12	L6	28	G6	12	I/O	General-Purpose Input Output 204 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR4	1, 5					O	Output X-BAR Output 4
EQEP2_STROBE	2					I/O	eQEP-2 Strobe
SPIA_CLK	3					I/O	SPI-A Clock
SPIB_PTE	6					I/O	SPI-B Peripheral Transmit Enable (PTE)
SD2_C2	7					I	SDFM-2 Channel 2 Clock Input
PMBUSA_CTL	9					I/O	PMBus-A Control Signal - Target Input/Controller Output
EMIF1_DQM3	10					O	External Memory Interface 1 Input/output mask for byte 3
ESC_MDIO_DATA	11					I/O	EtherCAT MDIO Data
EPWM14_B	13					O	ePWM-14 Output B
FSITXA_CLK	14					O	FSITX-A Output Clock
SD1_D3	15					I	SDFM-1 Channel 3 Data Input
GPIO205	0, 4, 8, 12	M6	29	H6	13	I/O	General-Purpose Input Output 205 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP1_INDEX	1					I/O	eQEP-1 Index
EPWM10_A	2					O	ePWM-10 Output A
SPIA_PTE	3					I/O	SPI-A Peripheral Transmit Enable (PTE)
OUTPUTXBAR1	11					O	Output X-BAR Output 1
SD1_C3	15					I	SDFM-1 Channel 3 Clock Input

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO206	0, 4, 8, 12	L5	30	H5	14	I/O	General-Purpose Input Output 206 This pin also has analog functions which are described in the ANALOG section of this table.
EMIF1_A11	1					O	External Memory Interface 1 address line 11
EPWM10_B	2					O	ePWM-10 Output B
EMIF1_WEn	3					O	External Memory Interface 1 write enable
OUTPUTXBAR2	11					O	Output X-BAR Output 2
ESC_PHY_CLK	14					O	EtherCAT PHY Clock
ESC_LED_STATE_RUN	15					O	EtherCAT LED State Run
GPIO207	0, 4, 8, 12	N5	55	J4	36	I/O	General-Purpose Input Output 207 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP2_A	1					I	eQEP-2 Input A
EPWM11_A	2					O	ePWM-11 Output A
EXTSYNCOUT	3					O	External ePWM Synchronization Pulse
CANA_TX	5					O	CAN-A Transmit
SD4_D1	6					I	SDFM-4 Channel 1 Data Input
SCIA_RX	7					I	SCI-A Receive Data
LINA_RX	9					I	LIN-A Receive
I2CB_SCL	10					I/OD	I2C-B Open-Drain Bidirectional Clock
OUTPUTXBAR3	11					O	Output X-BAR Output 3
ESC_RX1_CLK	14					I	EtherCAT MII Receive-1 Clock
PMBUSA_ALERT	15					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
GPIO208	0, 4, 8, 12	P5	56	K4	37	I/O	General-Purpose Input Output 208 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP2_B	1					I	eQEP-2 Input B
EPWM11_B	2					O	ePWM-11 Output B
EMIF1_D13	3					I/O	External Memory Interface 1 data line 13
SPIB_PICO	5					I/O	SPI-B Peripheral In, Controller Out (PICO)
SD4_C1	6					I	SDFM-4 Channel 1 Clock Input
SCIA_TX	7					O	SCI-A Transmit Data
OUTPUTXBAR4	11					O	Output X-BAR Output 4
ESC_RX1_DV	14					I	EtherCAT MII Receive-1 Data Valid
PMBUSA_CTL	15					I/O	PMBus-A Control Signal - Target Input/Controller Output
GPIO209	0, 4, 8, 12	N6	57	J5	38	I/O	General-Purpose Input Output 209 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP2_STROBE	1					I/O	eQEP-2 Strobe
EPWM12_A	2					O	ePWM-12 Output A
EMIF1_D14	3					I/O	External Memory Interface 1 data line 14
SPIB_POCI	5					I/O	SPI-B Peripheral Out, Controller In (POCI)
SD4_D2	6					I	SDFM-4 Channel 2 Data Input
EPWM12_B	7					O	ePWM-12 Output B
LINB_RX	10					I	LIN-B Receive
OUTPUTXBAR5	11					O	Output X-BAR Output 5
ESC_RX1_ERR	14					I	EtherCAT MII Receive-1 Error
PMBUSA_SDA	15					I/OD	PMBus-A Open-Drain Bidirectional Data

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO210	0, 4, 8, 12	P6	58	K5		I/O	General-Purpose Input Output 210 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP2_INDEX	1					I/O	eQEP-2 Index
EPWM12_B	2					O	ePWM-12 Output B
EMIF1_D15	3					I/O	External Memory Interface 1 data line 15
SD4_C2	6					I	SDFM-4 Channel 2 Clock Input
LINB_TX	10					O	LIN-B Transmit
OUTPUTXBAR6	11					O	Output X-BAR Output 6
ESC_RX0_DATA2	14					I	EtherCAT MII Receive-0 Data-2
PMBUSA_SCL	15					I/OD	PMBus-A Open-Drain Bidirectional Clock
GPIO211	0, 4, 8, 12	R6	59	J6		I/O	General-Purpose Input Output 211 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP6_A	1					I	eQEP-6 Input A
EPWM14_A	2					O	ePWM-14 Output A
SD4_D3	6					I	SDFM-4 Channel 3 Data Input
OUTPUTXBAR7	11					O	Output X-BAR Output 7
ESC_LED_LINK0_ACTIVE	14					O	EtherCAT Link-0 Active
GPIO212	0, 4, 8, 12	T7	60	K6		I/O	General-Purpose Input Output 212 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP6_B	1					I	eQEP-6 Input B
EPWM14_B	2					O	ePWM-14 Output B
SD4_C3	6					I	SDFM-4 Channel 3 Clock Input
ESC_LED_LINK1_ACTIVE	14					O	EtherCAT Link-1 Active
GPIO213	0, 4, 8, 12	T8	62	L5	39	I/O	General-Purpose Input Output 213 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP6_STROBE	1					I/O	eQEP-6 Strobe
EPWM8_A	2					O	ePWM-8 Output A
SD4_D4	6					I	SDFM-4 Channel 4 Data Input
LINB_TX	10					O	LIN-B Transmit
ESC_LED_ERR	14					O	EtherCAT Error LED
GPIO214	0, 4, 8, 12	R8	63	L6	40	I/O	General-Purpose Input Output 214 This pin also has analog functions which are described in the ANALOG section of this table.
CANA_RX	1					I	CAN-A Receive
EMIF1_CLK	2					O	External Memory Interface 1 clock
MCANA_RX	3					I	CAN/CAN FD-A Receive
OUTPUTXBAR7	5					O	Output X-BAR Output 7
EQEP3_STROBE	6					I/O	eQEP-3 Strobe
SD2_D4	7					I	SDFM-2 Channel 4 Data Input
EMIF1_CS4n	9					O	External Memory Interface 1 chip select 4
ESC_LATCH1	10					I	EtherCAT Latch Signal Input 1
ESC_I2C_SCL	11					I/OC	EtherCAT I2C Clock
EPWM16_A	13					O	ePWM-16 Output A
ESC_SYNC1	14					O	EtherCAT SyncSignal Output 1
SPID_PICO	15					I/O	SPI-D Peripheral In, Controller Out (PICO)

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO215	0, 4, 8, 12	P7	64	M6		I/O	General-Purpose Input Output 215 This pin also has analog functions which are described in the ANALOG section of this table.
SCIA_RX	1					I	SCI-A Receive Data
EMIF1_CS4n	2					O	External Memory Interface 1 chip select 4
CANA_RX	3					I	CAN-A Receive
OUTPUTXBAR5	5					O	Output X-BAR Output 5
EQEP3_A	6					I	eQEP-3 Input A
SD2_D3	7					I	SDFM-2 Channel 3 Data Input
EMIF1_CS2n	9					O	External Memory Interface 1 chip select 2
I2CB_SDA	10					I/OD	I2C-B Open-Drain Bidirectional Data
SPIC_POCI	11					I/O	SPI-C Peripheral Out, Controller In (POCI)
EPWM15_A	13					O	ePWM-15 Output A
LINA_TX	14					O	LIN-A Transmit
EMIF1_D12	15					I/O	External Memory Interface 1 data line 12
GPIO216	0, 4, 8, 12	N7	65	N6		I/O	General-Purpose Input Output 216 This pin also has analog functions which are described in the ANALOG section of this table.
SCIA_TX	1					O	SCI-A Transmit Data
EMIF1_SDCKE	2					O	External Memory Interface 1 SDRAM clock enable
SPID_CLK	3					I/O	SPI-D Clock
OUTPUTXBAR6	5					O	Output X-BAR Output 6
EQEP3_B	6					I	eQEP-3 Input B
SD2_C3	7					I	SDFM-2 Channel 3 Clock Input
EMIF1_CS3n	9					O	External Memory Interface 1 chip select 3
ESC_LATCH0	10					I	EtherCAT Latch Signal Input 0
ESC_I2C_SDA	11					I/OC	EtherCAT I2C Data
EPWM15_B	13					O	ePWM-15 Output B
ESC_SYNC0	14					O	EtherCAT SyncSignal Output 0
EMIF1_D13	15					I/O	External Memory Interface 1 data line 13
GPIO217	0, 4, 8, 12	P8	66	M7		I/O	General-Purpose Input Output 217 This pin also has analog functions which are described in the ANALOG section of this table.
CANA_TX	1					O	CAN-A Transmit
EMIF1_WEn	2					O	External Memory Interface 1 write enable
MCANA_TX	3					O	CAN/CAN FD-A Transmit
OUTPUTXBAR8	5					O	Output X-BAR Output 8
EQEP3_INDEX	6					I/O	eQEP-3 Index
SD2_C4	7					I	SDFM-2 Channel 4 Clock Input
EMIF1_RNW	9					O	External Memory Interface 1 read not write
I2CA_SDA	10					I/OD	I2C-A Open-Drain Bidirectional Data
SPID_PTE	11					I/O	SPI-D Peripheral Transmit Enable (PTE)
EPWM16_B	13					O	ePWM-16 Output B
LINB_TX	14					O	LIN-B Transmit
SPID_POCI	15					I/O	SPI-D Peripheral Out, Controller In (POCI)

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO218	0, 4, 8, 12	N8	67	N7		I/O	General-Purpose Input Output 218 This pin also has analog functions which are described in the ANALOG section of this table.
I2CA_SDA	1					I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_CS0n	2					O	External Memory Interface 1 chip select 0
SPIA_PICO	3					I/O	SPI-A Peripheral In, Controller Out (PICO)
EQEP4_A	5					I	eQEP-4 Input A
LINB_TX	6					O	LIN-B Transmit
CLB_OUTPUTXBAR1	7					O	CLB Output X-BAR Output 1
EMIF1_OEn	9					O	External Memory Interface 1 output enable
I2CA_SCL	10					I/OD	I2C-A Open-Drain Bidirectional Clock
SPID_CLK	15					I/O	SPI-D Clock
GPIO219	0, 4, 8, 12	R7	61			I/O	General-Purpose Input Output 219 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP6_INDEX	1					I/O	eQEP-6 Index
EPWM8_B	2					O	ePWM-8 Output B
SD4_C4	6					I	SDFM-4 Channel 4 Clock Input
ESC_LED_RUN	14					O	EtherCAT Run LED
GPIO220	0, 4, 8, 12	F16	123	D13	68	I/O	General-Purpose Input Output 220
EPWM6_A	2					O	ePWM-6 Output A
SPID_POCI	3					I/O	SPI-D Peripheral Out, Controller In (POCI)
OUTPUTXBAR2	5					O	Output X-BAR Output 2
SCIB_TX	6					O	SCI-B Transmit Data
MCANA_TX	7					O	CAN/CAN FD-A Transmit
PMBUSA_ALERT	15					I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
X1	ALT					I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.
GPIO221	0, 4, 8, 12	G16	121	E13	66	I/O	General-Purpose Input Output 221
EPWM6_B	2					O	ePWM-6 Output B
SPID_PTE	3					I/O	SPI-D Peripheral Transmit Enable (PTE)
OUTPUTXBAR3	5					O	Output X-BAR Output 3
SCIB_RX	6					I	SCI-B Receive Data
MCANA_RX	7					I	CAN/CAN FD-A Receive
PMBUSA_CTL	15					I/O	PMBus-A Control Signal - Target Input/Controller Output
X2	ALT					I/O	Crystal oscillator output.
GPIO222	0, 4, 8, 12	T12	77	N9	46	I/O	General-Purpose Input Output 222
TDI	1					I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
EPWM7_A	2					O	ePWM-7 Output A
SPIA_PICO	3					I/O	SPI-A Peripheral In, Controller Out (PICO)
OUTPUTXBAR4	5					O	Output X-BAR Output 4
SCIA_RX	6					I	SCI-A Receive Data
UARTB_TX	7					I/O	UART-B Serial Data Transmit
I2CA_SDA	9					I/OD	I2C-A Open-Drain Bidirectional Data
SPIC_CLK	10					I/O	SPI-C Clock
ESC_PDI_UC_IRQ	14					O	EtherCAT PDI IRQ Interrupt Line
PMBUSA_SDA	15					I/OD	PMBus-A Open-Drain Bidirectional Data

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
GPIO223	0, 4, 8, 12	R12	78	M9	47	I/O	General-Purpose Input Output 223
TDO	1					O	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.
EPWM7_B	2					O	ePWM-7 Output B
EMIF1_A11	3					O	External Memory Interface 1 address line 11
OUTPUTXBAR5	5					O	Output X-BAR Output 5
SCIA_TX	6					O	SCI-A Transmit Data
UARTB_RX	7					I/O	UART-B Serial Data Receive
I2CA_SCL	9					I/OD	I2C-A Open-Drain Bidirectional Clock
SPIC_PTE	10					I/O	SPI-C Peripheral Transmit Enable (PTE)
PMBUSA_SCL	15					I/OD	PMBus-A Open-Drain Bidirectional Clock
GPIO224	0, 4, 8, 12	P16	92	L12		I/O	General-Purpose Input Output 224
ERRORSTS	1					O	Error Status Output. This signal requires an external pulldown.
EMIF1_SDCKE	2					O	External Memory Interface 1 SDRAM clock enable
XCLKOUT	3					O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
OUTPUTXBAR1	5					O	Output X-BAR Output 1
SD2_C1	13					I	SDFM-2 Channel 1 Clock Input
ESC_PDI_UC_IRQ	14					O	EtherCAT PDI IRQ Interrupt Line
TEST, JTAG, AND RESET							
TCK		R13	81	M10	50	I	JTAG test clock with internal pullup.
TMS		T13	80	N10	49	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
VREGENZ		J16	119	E10	64	I	Internal voltage regulator enable with internal pullup. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply.
XRSn		G14	124	D12	69	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.
POWER AND GROUND							
VDD3VFL		R11, T11	72	M8	44		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin. Connect this pin to 3.3-V supply.
VDD		F9, F10, G6, J11, K8, K9	16, 76, 117, 137, 169	F5, F7, G9, J9	8, 45, 63, 78, 95		1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	256 ZEJ	176 PTP	169 NMR	100 PZP	PIN TYPE	DESCRIPTION
VDDA		N1, T6	36, 54	L2, M5	18, 35		3.3-V Analog Power Pins. Place a minimum 2.2-μF decoupling capacitor to VSSA on each pin. Connect this pin to 3.3-V supply.
VDDIO		B1, E15, G7, G8, H5, J5, J10, K7, K10, T15	3, 15, 68, 75, 88, 91, 99, 114, 127, 138, 152, 168	C13, F4, F6, F8, H9, J8	7, 41, 55, 62, 70, 79, 94		3.3-V Digital I/O Power Pins. Place a minimum 0.1-μF decoupling capacitor on each pin. Connect this pin to 3.3-V supply.
VDDOSC		G15	120	E11	65		Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-μF (minimum) decoupling capacitor on each pin. Connect this pin to 3.3-V supply.
VSS		A1, A16, G5, G9, G10, G11, H6, H7, H8, H9, H10, J6, J7, J8, J9, K6, T16	PAD	A1, A13, F9, G7, G8, H7, H8, J7, N13	PAD		Digital Ground
VSSA		M3, N2, T1, T5	34, 52	L1, N1, N5	17, 33		Analog Ground
VSSOSC		F15	122	E12	67		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.

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5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
A0	I	ADC-A Input 0	P1	43	L3	25
A1	I	ADC-A Input 1	P2	42	K3	24
A2	I	ADC-A Input 2	N3	41	J3	23
A3	I	ADC-A Input 3	N4	40	H3	22
A4	I	ADC-A Input 4	M4	39	H2	21
A5	I	ADC-A Input 5	M5	38	H1	20
A6	I	ADC-A Input 6	N6	57	J5	38
A7	I	ADC-A Input 7	P6	58	K5	
A8	I	ADC-A Input 8	R6	59	J6	
A9	I	ADC-A Input 9	T7	60	K6	
A10	I	ADC-A Input 10	T8	62	L5	39
A11	I	ADC-A Input 11	R8	63	L6	40
A14	I	ADC-A Input 14	R1	44	M1	26
A15	I	ADC-A Input 15	R2	45	M2	27
AIO225	I	Analog Pin Used For Digital Input 225	R1	44	M1	26
AIO226	I	Analog Pin Used For Digital Input 226	R2	45	M2	27
AIO227	I	Analog Pin Used For Digital Input 227	P1	43	L3	25
AIO228	I	Analog Pin Used For Digital Input 228	P2	42	K3	24
AIO229	I	Analog Pin Used For Digital Input 229	N3	41	J3	23
AIO230	I	Analog Pin Used For Digital Input 230	N4	40	H3	22
AIO231	I	Analog Pin Used For Digital Input 231	M4	39	H2	21
AIO232	I	Analog Pin Used For Digital Input 232	M5	38	H1	20
AIO233	I	Analog Pin Used For Digital Input 233	T2	46	N2	28
AIO234	I	Analog Pin Used For Digital Input 234	T3	47	N3	29
AIO235	I	Analog Pin Used For Digital Input 235	R3	48	M3	30
AIO236	I	Analog Pin Used For Digital Input 236	P3	49	L4	31
AIO237	I	Analog Pin Used For Digital Input 237	L4	31	H4	15
AIO238	I	Analog Pin Used For Digital Input 238	R5			
AIO239	I	Analog Pin Used For Digital Input 239	K1			
AIO240	I	Analog Pin Used For Digital Input 240	P4	51		
AIO241	I	Analog Pin Used For Digital Input 241	L3			
AIO242	I	Analog Pin Used For Digital Input 242	K2			
B0	I	ADC-B Input 0	T2	46	N2	28
B1	I	ADC-B Input 1	T3	47	N3	29
B2	I	ADC-B Input 2	R3	48	M3	30
B3	I	ADC-B Input 3	P3	49	L4	31
B4	I	ADC-B Input 4	P7	64	M6	
B5	I	ADC-B Input 5	N7	65	N6	
B6	I	ADC-B Input 6	N5	55	J4	36
B7	I	ADC-B Input 7	P5	56	K4	37
B8	I	ADC-B Input 8	P8	66	M7	
B9	I	ADC-B Input 9	N8	67	N7	

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Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
B10	I	ADC-B Input 10	R7	61		
B11	I	ADC-B Input 11	P4	51		
B13	I	ADC-B Input 13	R5			
B14	I	ADC-B Input 14	R1	44	M1	26
B15	I	ADC-B Input 15	R2	45	M2	27
C0	I	ADC-C Input 0	H1	22	F1	9
C1	I	ADC-C Input 1	J1	23	G1	10
C2	I	ADC-C Input 2	L4	31	H4	15
C3	I	ADC-C Input 3	L5	30	H5	14
C4	I	ADC-C Input 4	M6	29	H6	13
C5	I	ADC-C Input 5	L6	28	G6	12
C6	I	ADC-C Input 6	K5	27	G5	11
C7	I	ADC-C Input 7	K4	26	G4	
C8	I	ADC-C Input 8	K3	25	G3	
C9	I	ADC-C Input 9	J2	24	G2	
C10	I	ADC-C Input 10	L3			
C11	I	ADC-C Input 11	K2			
C13	I	ADC-C Input 13	K1			
C14	I	ADC-C Input 14	R1	44	M1	26
C15	I	ADC-C Input 15	R2	45	M2	27
CMP1_HN0	I	CMPSS-1 High Comparator Negative Input 0	N4	40	H3	22
CMP1_HN1	I	CMPSS-1 High Comparator Negative Input 1	P2	42	K3	24
CMP1_HP0	I	CMPSS-1 High Comparator Positive Input 0	N3	41	J3	23
CMP1_HP1	I	CMPSS-1 High Comparator Positive Input 1	P1	43	L3	25
CMP1_HP2	I	CMPSS-1 High Comparator Positive Input 2	P2	42	K3	24
CMP1_HP3	I	CMPSS-1 High Comparator Positive Input 3	N4	40	H3	22
CMP1_LN0	I	CMPSS-1 Low Comparator Negative Input 0	N4	40	H3	22
CMP1_LN1	I	CMPSS-1 Low Comparator Negative Input 1	P2	42	K3	24
CMP1_LP0	I	CMPSS-1 Low Comparator Positive Input 0	N3	41	J3	23
CMP1_LP1	I	CMPSS-1 Low Comparator Positive Input 1	P1	43	L3	25
CMP1_LP2	I	CMPSS-1 Low Comparator Positive Input 2	P2	42	K3	24
CMP1_LP3	I	CMPSS-1 Low Comparator Positive Input 3	P3	49	L4	31
CMP2_HN0	I	CMPSS-2 High Comparator Negative Input 0	M5	38	H1	20
CMP2_HN1	I	CMPSS-2 High Comparator Negative Input 1	N3	41	J3	23

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
CMP2_HP0	I	CMPSS-2 High Comparator Positive Input 0	M4	39	H2	21
CMP2_HP1	I	CMPSS-2 High Comparator Positive Input 1	P8	66	M7	
CMP2_HP2	I	CMPSS-2 High Comparator Positive Input 2	N8	67	N7	
CMP2_HP3	I	CMPSS-2 High Comparator Positive Input 3	M5	38	H1	20
CMP2_LN0	I	CMPSS-2 Low Comparator Negative Input 0	M5	38	H1	20
CMP2_LN1	I	CMPSS-2 Low Comparator Negative Input 1	N3	41	J3	23
CMP2_LP0	I	CMPSS-2 Low Comparator Positive Input 0	M4	39	H2	21
CMP2_LP1	I	CMPSS-2 Low Comparator Positive Input 1	P8	66	M7	
CMP2_LP2	I	CMPSS-2 Low Comparator Positive Input 2	N8	67	N7	
CMP2_LP3	I	CMPSS-2 Low Comparator Positive Input 3	L6	28	G6	12
CMP3_HN0	I	CMPSS-3 High Comparator Negative Input 0	P3	49	L4	31
CMP3_HN1	I	CMPSS-3 High Comparator Negative Input 1	P5	56	K4	37
CMP3_HP0	I	CMPSS-3 High Comparator Positive Input 0	R3	48	M3	30
CMP3_HP1	I	CMPSS-3 High Comparator Positive Input 1	T2	46	N2	28
CMP3_HP2	I	CMPSS-3 High Comparator Positive Input 2	T3	47	N3	29
CMP3_LN0	I	CMPSS-3 Low Comparator Negative Input 0	P3	49	L4	31
CMP3_LN1	I	CMPSS-3 Low Comparator Negative Input 1	P5	56	K4	37
CMP3_LP0	I	CMPSS-3 Low Comparator Positive Input 0	R3	48	M3	30
CMP3_LP1	I	CMPSS-3 Low Comparator Positive Input 1	T2	46	N2	28
CMP3_LP2	I	CMPSS-3 Low Comparator Positive Input 2	T3	47	N3	29
CMP3_LP3	I	CMPSS-3 Low Comparator Positive Input 3	L5	30	H5	14
CMP4_HN0	I	CMPSS-4 High Comparator Negative Input 0	R2	45	M2	27
CMP4_HN1	I	CMPSS-4 High Comparator Negative Input 1	R7	61		
CMP4_HP0	I	CMPSS-4 High Comparator Positive Input 0	R1	44	M1	26
CMP4_HP1	I	CMPSS-4 High Comparator Positive Input 1	R7	61		
CMP4_HP2	I	CMPSS-4 High Comparator Positive Input 2	P4	51		

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Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
CMP4_HP3	I	CMPSS-4 High Comparator Positive Input 3	R2	45	M2	27
CMP4_LN0	I	CMPSS-4 Low Comparator Negative Input 0	R2	45	M2	27
CMP4_LN1	I	CMPSS-4 Low Comparator Negative Input 1	R7	61		
CMP4_LP0	I	CMPSS-4 Low Comparator Positive Input 0	R1	44	M1	26
CMP4_LP1	I	CMPSS-4 Low Comparator Positive Input 1	R7	61		
CMP4_LP2	I	CMPSS-4 Low Comparator Positive Input 2	P4	51		
CMP4_LP3	I	CMPSS-4 Low Comparator Positive Input 3	P6	58	K5	
CMP5_HN0	I	CMPSS-5 High Comparator Negative Input 0	L6	28	G6	12
CMP5_HN1	I	CMPSS-5 High Comparator Negative Input 1	P7	64	M6	
CMP5_HP0	I	CMPSS-5 High Comparator Positive Input 0	M6	29	H6	13
CMP5_HP1	I	CMPSS-5 High Comparator Positive Input 1	P7	64	M6	
CMP5_HP2	I	CMPSS-5 High Comparator Positive Input 2	N7	65	N6	
CMP5_LN0	I	CMPSS-5 Low Comparator Negative Input 0	L6	28	G6	12
CMP5_LN1	I	CMPSS-5 Low Comparator Negative Input 1	P7	64	M6	
CMP5_LP0	I	CMPSS-5 Low Comparator Positive Input 0	M6	29	H6	13
CMP5_LP1	I	CMPSS-5 Low Comparator Positive Input 1	P7	64	M6	
CMP5_LP2	I	CMPSS-5 Low Comparator Positive Input 2	N7	65	N6	
CMP5_LP3	I	CMPSS-5 Low Comparator Positive Input 3	T7	60	K6	
CMP6_HN0	I	CMPSS-6 High Comparator Negative Input 0	L5	30	H5	14
CMP6_HN1	I	CMPSS-6 High Comparator Negative Input 1	H1	22	F1	9
CMP6_HP0	I	CMPSS-6 High Comparator Positive Input 0	L4	31	H4	15
CMP6_HP1	I	CMPSS-6 High Comparator Positive Input 1	H1	22	F1	9
CMP6_HP2	I	CMPSS-6 High Comparator Positive Input 2	J1	23	G1	10
CMP6_LN0	I	CMPSS-6 Low Comparator Negative Input 0	L5	30	H5	14
CMP6_LN1	I	CMPSS-6 Low Comparator Negative Input 1	H1	22	F1	9
CMP6_LP0	I	CMPSS-6 Low Comparator Positive Input 0	L4	31	H4	15

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Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
CMP6_LP1	I	CMPSS-6 Low Comparator Positive Input 1	H1	22	F1	9
CMP6_LP2	I	CMPSS-6 Low Comparator Positive Input 2	J1	23	G1	10
CMP7_HN0	I	CMPSS-7 High Comparator Negative Input 0	P6	58	K5	
CMP7_HN1	I	CMPSS-7 High Comparator Negative Input 1	N5	55	J4	36
CMP7_HP0	I	CMPSS-7 High Comparator Positive Input 0	N6	57	J5	38
CMP7_HP1	I	CMPSS-7 High Comparator Positive Input 1	N5	55	J4	36
CMP7_HP2	I	CMPSS-7 High Comparator Positive Input 2	P5	56	K4	37
CMP7_LN0	I	CMPSS-7 Low Comparator Negative Input 0	P6	58	K5	
CMP7_LN1	I	CMPSS-7 Low Comparator Negative Input 1	N5	55	J4	36
CMP7_LP0	I	CMPSS-7 Low Comparator Positive Input 0	N6	57	J5	38
CMP7_LP1	I	CMPSS-7 Low Comparator Positive Input 1	N5	55	J4	36
CMP7_LP2	I	CMPSS-7 Low Comparator Positive Input 2	P5	56	K4	37
CMP8_HN0	I	CMPSS-8 High Comparator Negative Input 0	T7	60	K6	
CMP8_HN1	I	CMPSS-8 High Comparator Negative Input 1	T8	62	L5	39
CMP8_HP0	I	CMPSS-8 High Comparator Positive Input 0	R6	59	J6	
CMP8_HP1	I	CMPSS-8 High Comparator Positive Input 1	T8	62	L5	39
CMP8_HP2	I	CMPSS-8 High Comparator Positive Input 2	R8	63	L6	40
CMP8_LN0	I	CMPSS-8 Low Comparator Negative Input 0	T7	60	K6	
CMP8_LN1	I	CMPSS-8 Low Comparator Negative Input 1	T8	62	L5	39
CMP8_LP0	I	CMPSS-8 Low Comparator Positive Input 0	R6	59	J6	
CMP8_LP1	I	CMPSS-8 Low Comparator Positive Input 1	T8	62	L5	39
CMP8_LP2	I	CMPSS-8 Low Comparator Positive Input 2	R8	63	L6	40
CMP9_HN0	I	CMPSS-9 High Comparator Negative Input 0	P1	43	L3	25
CMP9_HN1	I	CMPSS-9 High Comparator Negative Input 1	N8	67	N7	
CMP9_HP0	I	CMPSS-9 High Comparator Positive Input 0	R5			
CMP9_HP1	I	CMPSS-9 High Comparator Positive Input 1	K1			

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Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
CMP9_HP2	I	CMPSS-9 High Comparator Positive Input 2	P6	58	K5	
CMP9_LN0	I	CMPSS-9 Low Comparator Negative Input 0	P1	43	L3	25
CMP9_LN1	I	CMPSS-9 Low Comparator Negative Input 1	N8	67	N7	
CMP9_LP0	I	CMPSS-9 Low Comparator Positive Input 0	R5			
CMP9_LP1	I	CMPSS-9 Low Comparator Positive Input 1	K1			
CMP9_LP2	I	CMPSS-9 Low Comparator Positive Input 2	M5	38	H1	20
CMP10_HN0	I	CMPSS-10 High Comparator Negative Input 0	P8	66	M7	
CMP10_HN1	I	CMPSS-10 High Comparator Negative Input 1	M6	29	H6	13
CMP10_HP0	I	CMPSS-10 High Comparator Positive Input 0	L3			
CMP10_HP1	I	CMPSS-10 High Comparator Positive Input 1	K5	27	G5	11
CMP10_HP2	I	CMPSS-10 High Comparator Positive Input 2	K3	25	G3	
CMP10_LN0	I	CMPSS-10 Low Comparator Negative Input 0	P8	66	M7	
CMP10_LN1	I	CMPSS-10 Low Comparator Negative Input 1	M6	29	H6	13
CMP10_LP0	I	CMPSS-10 Low Comparator Positive Input 0	L3			
CMP10_LP1	I	CMPSS-10 Low Comparator Positive Input 1	K5	27	G5	11
CMP10_LP2	I	CMPSS-10 Low Comparator Positive Input 2	K3	25	G3	
CMP11_HN0	I	CMPSS-11 High Comparator Negative Input 0	T2	46	N2	28
CMP11_HN1	I	CMPSS-11 High Comparator Negative Input 1	K1			
CMP11_HP0	I	CMPSS-11 High Comparator Positive Input 0	K2			
CMP11_HP1	I	CMPSS-11 High Comparator Positive Input 1	K4	26	G4	
CMP11_HP2	I	CMPSS-11 High Comparator Positive Input 2	J2	24	G2	
CMP11_LN0	I	CMPSS-11 Low Comparator Negative Input 0	T2	46	N2	28
CMP11_LN1	I	CMPSS-11 Low Comparator Negative Input 1	K1			
CMP11_LP0	I	CMPSS-11 Low Comparator Positive Input 0	K2			
CMP11_LP1	I	CMPSS-11 Low Comparator Positive Input 1	K4	26	G4	
CMP11_LP2	I	CMPSS-11 Low Comparator Positive Input 2	J2	24	G2	
DACA_OUT	O	Buffered DAC-A Output.	P1	43	L3	25

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Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
DACC_OUT	O	Buffered DAC-C Output.	T3	47	N3	29
VDAC	I	Optional external reference voltage for on-chip DACs.	T2	46	N2	28
VREFHIA	I	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. NOTE: Do not load this pin externally	M2	37	K2	19
VREFHIB	I	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. NOTE: Do not load this pin externally	R4	53	M4	34
VREFHIC	I	ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. NOTE: Do not load this pin externally	L2	35	J2	19
VREFLOA	I	ADC-A Low Reference	M1	33	K1	16
VREFLOB	I	ADC-B Low Reference	T4	50	N4	32
VREFLOC	I	ADC-C Low Reference	L1	32	J1	16

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5.3.2 Digital Signals

Table 5-3. Digital Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
ADCSOCAO	O	ADC Start of Conversion A Output for External ADC (from ePWM modules)	8, 12	D1, G4	4, 18	B1, E3	3
ADCSOCBO	O	ADC Start of Conversion B Output for External ADC (from ePWM modules)	10	D4	1	B3	100
CANA_RX	I	CAN-A Receive	5, 18, 30, 36, 58, 61, 62, 70, 214, 215	C15, E7, F3, K15, K16, L10, L13, P7, P12, R8	10, 63, 64, 79, 83, 103, 107, 108, 135, 165	A12, D3, E6, H10, H11, J10, L6, L9, M6, N11	40, 48, 52, 56, 57, 76
CANA_TX	O	CAN-A Transmit	4, 19, 31, 37, 59, 62, 63, 71, 207, 217	B2, B15, D7, D8, K14, K15, L14, N5, N12, P8	12, 55, 66, 84, 104, 108, 109, 136, 158, 164	B11, D1, D6, G13, H10, H13, J4, M7, M11	36, 53, 57, 58, 77, 93
CLB_OUTPUTXBAR1	O	CLB Output X-BAR Output 1	0, 32, 40, 91, 218	E6, F8, J14, N8, P13	67, 87, 116, 160, 173	B4, E7, F12, N7, N12	89, 98
CLB_OUTPUTXBAR2	O	CLB Output X-BAR Output 2	1, 33, 41, 92	A5, A7, R10, R15	69, 89, 161, 174	A4, A6, L7, M12	51, 90, 99
CLB_OUTPUTXBAR3	O	CLB Output X-BAR Output 3	5, 34, 93	C5, E7, P10	70, 165, 175	A3, E6, K7	42
CLB_OUTPUTXBAR4	O	CLB Output X-BAR Output 4	8, 35, 94	D1, D5, N10	18, 71, 176	A2, E3, N8	43
CLB_OUTPUTXBAR5	O	CLB Output X-BAR Output 5	10, 36, 42, 95	A4, D4, E16, P12	1, 83, 130	B3, C12, N11	73, 100
CLB_OUTPUTXBAR6	O	CLB Output X-BAR Output 6	12, 37, 43, 44, 96	B4, D16, G4, J12, N12	4, 84, 113, 131	B1, C11, F10, M11	3, 74
CLB_OUTPUTXBAR7	O	CLB Output X-BAR Output 7	13, 38, 45, 97	A3, C4, J13, M12	5, 85, 115	C1, F11, L11	4
CLB_OUTPUTXBAR8	O	CLB Output X-BAR Output 8	15, 39, 75, 98	B14, C3, E2, L12	7, 86, 142	A10, C3	6
EMIF1_A0	O	External Memory Interface 1 address line 0	35, 38	M12, N10	71, 85	L11, N8	43
EMIF1_A1	O	External Memory Interface 1 address line 1	12, 36, 39	G4, L12, P12	4, 83, 86	B1, N11	3
EMIF1_A2	O	External Memory Interface 1 address line 2	37, 40	N12, P13	84, 87	M11, N12	
EMIF1_A3	O	External Memory Interface 1 address line 3	38, 41	M12, R15	85, 89	L11, M12	51
EMIF1_A4	O	External Memory Interface 1 address line 4	39, 44	J12, L12	86, 113	F10	
EMIF1_A5	O	External Memory Interface 1 address line 5	45, 49, 101	J13, N9, P15	93, 115	F11, L13	
EMIF1_A6	O	External Memory Interface 1 address line 6	46, 50, 102	C13, F14, P14	94, 128	K9	71
EMIF1_A7	O	External Memory Interface 1 address line 7	47, 51	E14, N14	95, 129	K10	72
EMIF1_A8	O	External Memory Interface 1 address line 8	48, 52	N15, R16	90, 96	K11, M13	
EMIF1_A9	O	External Memory Interface 1 address line 9	49, 53	N16, P15	93, 97	K12, L13	
EMIF1_A10	O	External Memory Interface 1 address line 10	50, 54, 106	F1, M13, P14	20, 94, 98	K9, K13	
EMIF1_A11	O	External Memory Interface 1 address line 11	51, 109, 133, 206, 223	G3, J15, L5, N14, R12	30, 78, 95, 118	F13, H5, K10, M9	14, 47
EMIF1_A12	O	External Memory Interface 1 address line 12	52, 108	G2, N15	96	K11	
EMIF1_A13	O	External Memory Interface 1 address line 13	0, 86	B9, F8	156, 160	B7, E7	87, 89
EMIF1_A14	O	External Memory Interface 1 address line 14	1, 87	A7, A9	157, 161	A6, C7	88, 90
EMIF1_A15	O	External Memory Interface 1 address line 15	2, 88	B6, B7	162, 170	B6, C5	91
EMIF1_A16	O	External Memory Interface 1 address line 16	89	C6	171	D5	96
EMIF1_A17	O	External Memory Interface 1 address line 17	90	D6	172	E5	97
EMIF1_A18	O	External Memory Interface 1 address line 18	91	E6	173	B4	98
EMIF1_A19	O	External Memory Interface 1 address line 19	92	A5	174	A4	99
EMIF1_BA0	O	External Memory Interface 1 bank address 0	20, 33, 63, 93, 103	C2, C5, G12, K14, R10	13, 69, 109, 126, 175	A3, D10, E1, G13, L7	58
EMIF1_BA1	O	External Memory Interface 1 bank address 1	21, 34, 64, 92, 94, 100	A5, D2, D5, F4, K13, P10	14, 70, 110, 174, 176	A2, A4, E2, G12, K7	2, 42, 59, 99
EMIF1_CAS	O	External Memory Interface 1 column address strobe	10, 23, 86, 89, 200	B9, C6, D4, G1, J1	1, 21, 23, 156, 171	B3, B7, D5, F2, G1	10, 87, 96, 100
EMIF1_CLK	O	External Memory Interface 1 clock	30, 214	L10, R8	63, 79	L6, L9	40, 48
EMIF1_CS0n	O	External Memory Interface 1 chip select 0	13, 32, 218	A3, J14, N8	5, 67, 116	C1, F12, N7	4
EMIF1_CS2n	O	External Memory Interface 1 chip select 2	18, 28, 34, 38, 215	F3, M12, N11, P7, P10	10, 64, 70, 74, 85	D3, K7, K8, L11, M6	42
EMIF1_CS3n	O	External Memory Interface 1 chip select 3	19, 29, 35, 216	B2, N7, N10, P11	12, 65, 71, 73	D1, L8, N6, N8	43
EMIF1_CS4n	O	External Memory Interface 1 chip select 4	28, 30, 84, 214, 215	D9, L10, N11, P7, R8	63, 64, 74, 79, 154	A8, K8, L6, L9, M6	40, 48, 85
EMIF1_D0	I/O	External Memory Interface 1 data line 0	55, 85	C9, M14	100, 155	A7, J13	86
EMIF1_D1	I/O	External Memory Interface 1 data line 1	56, 83, 84	D9, D12, M15	101, 151, 154	A8, C8, J12	85
EMIF1_D2	I/O	External Memory Interface 1 data line 2	57, 82	E12, M16	102, 150	D8, J11	

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
EMIF1_D3	I/O	External Memory Interface 1 data line 3	58, 81	F12, L13	103, 149	J10	52
EMIF1_D4	I/O	External Memory Interface 1 data line 4	59, 80	A13, L14	104, 148	E8, H13	53, 83
EMIF1_D5	I/O	External Memory Interface 1 data line 5	60, 79	D13, L15	105, 146	B9	54
EMIF1_D6	I/O	External Memory Interface 1 data line 6	61, 78	E13, K16	107, 145	C9, H11	56, 82
EMIF1_D7	I/O	External Memory Interface 1 data line 7	62, 77	F13, K15	108, 144	D9, H10	57
EMIF1_D8	I/O	External Memory Interface 1 data line 8	76	A14	143	E9	
EMIF1_D9	I/O	External Memory Interface 1 data line 9	75	B14	142	A10	
EMIF1_D10	I/O	External Memory Interface 1 data line 10	74	C14	141	B10	
EMIF1_D11	I/O	External Memory Interface 1 data line 11	73	D14	140	C10	81
EMIF1_D12	I/O	External Memory Interface 1 data line 12	72, 215	A15, P7	64, 139	A11, M6	80
EMIF1_D13	I/O	External Memory Interface 1 data line 13	71, 208, 216	B15, N7, P5	56, 65, 136	B11, K4, N6	37, 77
EMIF1_D14	I/O	External Memory Interface 1 data line 14	70, 209	C15, N6	57, 135	A12, J5	38, 76
EMIF1_D15	I/O	External Memory Interface 1 data line 15	69, 210	B16, P6	58, 134	B12, K5	75
EMIF1_D16	I/O	External Memory Interface 1 data line 16	68, 129	C16, L9	133	B13	
EMIF1_D17	I/O	External Memory Interface 1 data line 17	14, 67, 99, 128	B3, C1, D15, M9	6, 17, 132	C2, E4	5
EMIF1_D18	I/O	External Memory Interface 1 data line 18	66, 127	K11, R9	112	G10	61
EMIF1_D19	I/O	External Memory Interface 1 data line 19	65, 126	K12, T9	111	G11	60
EMIF1_D20	I/O	External Memory Interface 1 data line 20	64, 125	K13, M8	110	G12	59
EMIF1_D21	I/O	External Memory Interface 1 data line 21	63, 124	K14, L8	109	G13	58
EMIF1_D22	I/O	External Memory Interface 1 data line 22	62, 123	K15, M7	108	H10	57
EMIF1_D23	I/O	External Memory Interface 1 data line 23	61, 122	K16, L7	107	H11	56
EMIF1_D24	I/O	External Memory Interface 1 data line 24	37, 60, 100, 120	F4, L15, M11, N12	84, 105	M11	2, 54
EMIF1_D25	I/O	External Memory Interface 1 data line 25	59, 119	L14, M10	104	H13	53
EMIF1_D26	I/O	External Memory Interface 1 data line 26	58, 115	L13, P9	103	J10	52
EMIF1_D27	I/O	External Memory Interface 1 data line 27	57, 114	J4, M16	102	J11	
EMIF1_D28	I/O	External Memory Interface 1 data line 28	56, 113	J3, M15	101	J12	
EMIF1_D29	I/O	External Memory Interface 1 data line 29	55, 112	H4, M14	100	J13	
EMIF1_D30	I/O	External Memory Interface 1 data line 30	54, 111	H3, M13	98	K13	
EMIF1_D31	I/O	External Memory Interface 1 data line 31	53, 110	H2, N16	97	K12	
EMIF1_DQM0	O	External Memory Interface 1 Input/output mask for byte 0	6, 24, 88, 92, 201	A5, B6, E8, F7, J2	24, 159, 166, 170, 174	A4, A5, C5, D7, G2	99
EMIF1_DQM1	O	External Memory Interface 1 Input/output mask for byte 1	7, 25, 88, 89, 202	A6, A10, B6, C6, K3	25, 153, 167, 170, 171	B5, B8, C5, D5, G3	84, 96
EMIF1_DQM2	O	External Memory Interface 1 Input/output mask for byte 2	15, 26, 85, 90, 91, 203	C3, C9, D6, E6, K5, L11	7, 27, 82, 155, 172, 173	A7, B4, C3, E5, G5, L10	6, 11, 86, 97, 98
EMIF1_DQM3	O	External Memory Interface 1 Input/output mask for byte 3	27, 87, 91, 99, 204	A9, C1, E6, G13, L6	17, 28, 125, 157, 173	B4, C7, D11, E4, G6	12, 88, 98
EMIF1_OEn	O	External Memory Interface 1 output enable	32, 37, 66, 218	J14, K11, N8, N12	67, 84, 112, 116	F12, G10, M11, N7	61
EMIF1_RAS	O	External Memory Interface 1 row address strobe	8, 22, 87, 90, 199	A2, A9, D1, D6, H1	11, 18, 22, 157, 172	C7, D2, E3, E5, F1	9, 88, 97
EMIF1_RNW	O	External Memory Interface 1 read not write	31, 33, 63, 217	D8, K14, P8, R10	66, 69, 109, 158	G13, L7, M7	58
EMIF1_SDCKE	O	External Memory Interface 1 SDRAM clock enable	29, 216, 224	N7, P11, P16	65, 73, 92	L8, L12, N6	
EMIF1_WAIT	I	External Memory Interface 1 Asynchronous SRAM WAIT	36, 64	K13, P12	83, 110	G12, N11	59
EMIF1_WEn	O	External Memory Interface 1 write enable	31, 36, 65, 206, 217	D8, K12, L5, P8, P12	30, 66, 83, 111, 158	G11, H5, M7, N11	14, 60
EPWM1_A	O	ePWM-1 Output A	0, 145	F8, H15	160	E7	89
EPWM1_B	O	ePWM-1 Output B	1, 146	A7, H16	161	A6	90
EPWM2_A	O	ePWM-2 Output A	2, 147	B7, H12	162	B6	91
EPWM2_B	O	ePWM-2 Output B	3, 148	C7, C12	163	C6	92
EPWM3_A	O	ePWM-3 Output A	4, 149	B12, D7	164	D6	93
EPWM3_B	O	ePWM-3 Output B	5, 60, 150	A12, E7, L15	105, 165	E6	54
EPWM4_A	O	ePWM-4 Output A	6, 46, 151	F7, F11, F14	128, 166	A5	71
EPWM4_B	O	ePWM-4 Output B	7, 47, 152	A6, E11, E14	129, 167	B5	72
EPWM5_A	O	ePWM-5 Output A	8, 59, 153	D1, D11, L14	18, 104	E3, H13	53
EPWM5_B	O	ePWM-5 Output B	9, 73, 154	C11, D14, E1	19, 140	C10, F3	81

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
EPWM6_A	O	ePWM-6 Output A	10, 155, 220	B11, D4, F16	1, 123	B3, D13	68, 100
EPWM6_B	O	ePWM-6 Output B	11, 156, 221	A11, E4, G16	2, 121	B2, E13	1, 66
EPWM7_A	O	ePWM-7 Output A	12, 157, 222	E10, G4, T12	4, 77	B1, N9	3, 46
EPWM7_B	O	ePWM-7 Output B	13, 158, 223	A3, D10, R12	5, 78	C1, M9	4, 47
EPWM8_A	O	ePWM-8 Output A	14, 58, 74, 99, 159, 213	B3, C1, C10, C14, L13, T8	6, 17, 62, 103, 141	B10, C2, E4, J10, L5	5, 39, 52
EPWM8_B	O	ePWM-8 Output B	15, 59, 75, 103, 160, 203, 219	B10, B14, C3, G12, K5, L14, R7	7, 27, 61, 104, 126, 142	A10, C3, D10, G5, H13	6, 11, 53
EPWM9_A	O	ePWM-9 Output A	16, 63, 76, 100, 133, 161	A14, D3, E9, F4, J15, K14	8, 109, 118, 143	C4, E9, F13, G13	2, 58
EPWM9_B	O	ePWM-9 Output B	17, 64, 77, 162, 198	A8, E3, F13, K4, K13	9, 26, 110, 144	D4, D9, G4, G12	59
EPWM10_A	O	ePWM-10 Output A	18, 65, 78, 163, 205	B8, E13, F3, K12, M6	10, 29, 111, 145	C9, D3, G11, H6	13, 60, 82
EPWM10_B	O	ePWM-10 Output B	19, 66, 79, 164, 206	B2, C8, D13, K11, L5	12, 30, 112, 146	B9, D1, G10, H5	14, 61
EPWM11_A	O	ePWM-11 Output A	20, 69, 80, 165, 207	A13, B16, C2, F6, N5	13, 55, 134, 148	B12, E1, E8, J4	36, 75, 83
EPWM11_B	O	ePWM-11 Output B	21, 70, 81, 166, 208	B5, C15, D2, F12, P5	14, 56, 135, 149	A12, E2, K4	37, 76
EPWM12_A	O	ePWM-12 Output A	22, 71, 82, 167, 199, 209	A2, B15, E5, E12, H1, N6	11, 22, 57, 136, 150	B11, D2, D8, F1, J5	9, 38, 77
EPWM12_B	O	ePWM-12 Output B	23, 72, 83, 84, 168, 200, 209, 210	A15, D9, D12, F5, G1, J1, N6, P6	21, 23, 57, 58, 139, 151, 154	A8, A11, C8, F2, G1, J5, K5	10, 38, 80, 85
EPWM13_A	O	ePWM-13 Output A	24, 40, 85, 130, 201	C9, E8, J2, P13, T10	24, 87, 155, 159	A7, D7, G2, N12	86
EPWM13_B	O	ePWM-13 Output B	25, 41, 86, 131, 202	A10, B9, K3, N13, R15	25, 89, 153, 156	B7, B8, G3, M12	51, 84, 87
EPWM14_A	O	ePWM-14 Output A	26, 42, 46, 87, 132, 203, 211	A9, E16, F14, K5, L11, R6, T14	27, 59, 82, 128, 130, 157	C7, C12, G5, J6, L10	11, 71, 73, 88
EPWM14_B	O	ePWM-14 Output B	27, 43, 47, 88, 134, 204, 212	B6, D16, E14, G13, L6, R14, T7	28, 60, 125, 129, 131, 170	C5, C11, D11, G6, K6	12, 72, 74
EPWM15_A	O	ePWM-15 Output A	28, 50, 89, 141, 215	C6, H13, N11, P7, P14	64, 74, 94, 171	D5, K8, K9, M6	96
EPWM15_B	O	ePWM-15 Output B	29, 51, 90, 142, 216	D6, H14, N7, N14, P11	65, 73, 95, 172	E5, K10, L8, N6	97
EPWM16_A	O	ePWM-16 Output A	30, 52, 91, 106, 214	E6, F1, L10, N15, R8	20, 63, 79, 96, 173	B4, K11, L6, L9	40, 48, 98
EPWM16_B	O	ePWM-16 Output B	31, 55, 92, 107, 217	A5, D8, F2, M14, P8	66, 100, 158, 174	A4, J13, M7	99
EPWM17_A	O	ePWM-17 Output A	56, 67, 93, 108, 199	C5, D15, G2, H1, M15	22, 101, 132, 175	A3, F1, J12	9
EPWM17_B	O	ePWM-17 Output B	57, 61, 68, 94, 109, 200	C16, D5, G3, J1, K16, M16	23, 102, 107, 133, 176	A2, B13, G1, H11, J11	10, 56
EPWM18_A	O	ePWM-18 Output A	34, 37, 95, 101, 104, 201	A4, B13, J2, N9, N12, P10	24, 70, 84, 147	A9, G2, K7, M11	42
EPWM18_B	O	ePWM-18 Output B	35, 38, 96, 102, 105, 202	B4, C13, K3, L16, M12, N10	25, 71, 85, 106	G3, H12, L11, N8	43
EQEP1_A	I	eQEP-1 Input A	10, 20, 50, 96, 198	B4, C2, D4, K4, P14	1, 13, 26, 94	B3, E1, G4, K9	100
EQEP1_B	I	eQEP-1 Input B	11, 21, 51, 97	C4, D2, E4, N14	2, 14, 95	B2, E2, K10	1
EQEP1_INDEX	I/O	eQEP-1 Index	13, 23, 53, 99, 200, 205	A3, C1, G1, J1, M6, N16	5, 17, 21, 23, 29, 97	C1, E4, F2, G1, H6, K12	4, 10, 13
EQEP1_STROBE	I/O	eQEP-1 Strobe	12, 22, 52, 98, 199	A2, E2, G4, H1, N15	4, 11, 22, 96	B1, D2, F1, K11	3, 9
EQEP2_A	I	eQEP-2 Input A	24, 54, 78, 100, 201, 207	E8, E13, F4, J2, M13, N5	24, 55, 98, 145, 159	C9, D7, G2, J4, K13	2, 36, 82
EQEP2_B	I	eQEP-2 Input B	25, 55, 79, 101, 202, 208	A10, D13, K3, M14, N9, P5	25, 56, 100, 146, 153	B8, B9, G3, J13, K4	37, 84
EQEP2_INDEX	I/O	eQEP-2 Index	26, 57, 81, 103, 203, 210	F12, G12, K5, L11, M16, P6	27, 58, 82, 102, 126, 149	D10, G5, J11, K5, L10	11
EQEP2_STROBE	I/O	eQEP-2 Strobe	27, 56, 80, 102, 204, 209	A13, C13, G13, L6, M15, N6	28, 57, 101, 125, 148	D11, E8, G6, J5, J12	12, 38, 83
EQEP3_A	I	eQEP-3 Input A	6, 28, 62, 104, 215	B13, F7, K15, N11, P7	64, 74, 108, 147, 166	A5, A9, H10, K8, M6	57

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
EQEP3_B	I	eQEP-3 Input B	7, 29, 63, 105, 216	A6, K14, L16, N7, P11	65, 73, 106, 109, 167	B5, G13, H12, L8, N6	58
EQEP3_INDEX	I/O	eQEP-3 Index	9, 31, 65, 107, 217	D8, E1, F2, K12, P8	19, 66, 111, 158	F3, G11, M7	60
EQEP3_STROBE	I/O	eQEP-3 Strobe	8, 30, 64, 106, 214	D1, F1, K13, L10, R8	18, 20, 63, 79, 110	E3, G12, L6, L9	40, 48, 59
EQEP4_A	I	eQEP-4 Input A	32, 42, 95, 218	A4, E16, J14, N8	67, 116, 130	C12, F12, N7	73
EQEP4_B	I	eQEP-4 Input B	33, 43, 96	B4, D16, R10	69, 131	C11, L7	74
EQEP4_INDEX	I/O	eQEP-4 Index	35, 98	E2, N10	71	N8	43
EQEP4_STROBE	I/O	eQEP-4 Strobe	34, 97	C4, P10	70	K7	42
EQEP5_A	I	eQEP-5 Input A	15, 74, 108, 147	C3, C14, G2, H12	7, 141	B10, C3	6
EQEP5_B	I	eQEP-5 Input B	16, 25, 75, 109, 148	A10, B14, C12, D3, G3	8, 142, 153	A10, B8, C4	84
EQEP5_INDEX	I/O	eQEP-5 Index	14, 18, 77, 111, 150	A12, B3, F3, F13, H3	6, 10, 144	C2, D3, D9	5
EQEP5_STROBE	I/O	eQEP-5 Strobe	13, 17, 76, 110, 149	A3, A14, B12, E3, H2	5, 9, 143	C1, D4, E9	4
EQEP6_A	I	eQEP-6 Input A	84, 211	D9, R6	59, 154	A8, J6	85
EQEP6_B	I	eQEP-6 Input B	66, 85, 212	C9, K11, T7	60, 112, 155	A7, G10, K6	61, 86
EQEP6_INDEX	I/O	eQEP-6 Index	73, 87, 219	A9, D14, R7	61, 140, 157	C7, C10	81, 88
EQEP6_STROBE	I/O	eQEP-6 Strobe	72, 86, 213	A15, B9, T8	62, 139, 156	A11, B7, L5	39, 80, 87
ERRORSTS	O	Error Status Output. This signal requires an external pulldown.	79, 80, 224	A13, D13, P16	92, 146, 148	B9, E8, L12	83
ESC_GPI0	I	EtherCAT General-Purpose Input 0	0, 100	F4, F8	160	E7	2, 89
ESC_GPI1	I	EtherCAT General-Purpose Input 1	1, 101	A7, N9	161	A6	90
ESC_GPI2	I	EtherCAT General-Purpose Input 2	2, 102	B7, C13	162	B6	91
ESC_GPI3	I	EtherCAT General-Purpose Input 3	3, 103	C7, G12	126, 163	C6, D10	92
ESC_GPI4	I	EtherCAT General-Purpose Input 4	4, 104	B13, D7	147, 164	A9, D6	93
ESC_GPI5	I	EtherCAT General-Purpose Input 5	5, 105	E7, L16	106, 165	E6, H12	
ESC_GPI6	I	EtherCAT General-Purpose Input 6	6, 106	F1, F7	20, 166	A5	
ESC_GPI7	I	EtherCAT General-Purpose Input 7	7, 107	A6, F2	167	B5	
ESC_GPI8	I	EtherCAT General-Purpose Input 8	108	G2			
ESC_GPI9	I	EtherCAT General-Purpose Input 9	109	G3			
ESC_GPI10	I	EtherCAT General-Purpose Input 10	110	H2			
ESC_GPI11	I	EtherCAT General-Purpose Input 11	111	H3			
ESC_GPI12	I	EtherCAT General-Purpose Input 12	112	H4			
ESC_GPI13	I	EtherCAT General-Purpose Input 13	113	J3			
ESC_GPI14	I	EtherCAT General-Purpose Input 14	114	J4			
ESC_GPI15	I	EtherCAT General-Purpose Input 15	115	P9			
ESC_GPI16	I	EtherCAT General-Purpose Input 16	116	H11			
ESC_GPI17	I	EtherCAT General-Purpose Input 17	97	C4			
ESC_GPI18	I	EtherCAT General-Purpose Input 18	98	E2			
ESC_GPI19	I	EtherCAT General-Purpose Input 19	119	M10			
ESC_GPI20	I	EtherCAT General-Purpose Input 20	120	M11			
ESC_GPI21	I	EtherCAT General-Purpose Input 21	99	C1	17	E4	
ESC_GPI22	I	EtherCAT General-Purpose Input 22	122	L7			
ESC_GPI23	I	EtherCAT General-Purpose Input 23	123	M7			
ESC_GPI24	I	EtherCAT General-Purpose Input 24	124	L8			
ESC_GPI25	I	EtherCAT General-Purpose Input 25	125	M8			
ESC_GPI26	I	EtherCAT General-Purpose Input 26	126	T9			
ESC_GPI27	I	EtherCAT General-Purpose Input 27	127	R9			
ESC_GPI28	I	EtherCAT General-Purpose Input 28	128	M9			
ESC_GPI29	I	EtherCAT General-Purpose Input 29	129	L9			
ESC_GPI30	I	EtherCAT General-Purpose Input 30	130	T10			
ESC_GPI31	I	EtherCAT General-Purpose Input 31	131	N13			
ESC_GPO0	O	EtherCAT General-Purpose Output 0	8, 132	D1, T14	18	E3	

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
ESC_GPO1	O	EtherCAT General-Purpose Output 1	9, 134	E1, R14	19	F3	
ESC_GPO2	O	EtherCAT General-Purpose Output 2	40	P13	87	N12	
ESC_GPO3	O	EtherCAT General-Purpose Output 3	11	E4	2	B2	1
ESC_GPO4	O	EtherCAT General-Purpose Output 4	12	G4	4	B1	3
ESC_GPO5	O	EtherCAT General-Purpose Output 5	13	A3	5	C1	4
ESC_GPO6	O	EtherCAT General-Purpose Output 6	14	B3	6	C2	5
ESC_GPO7	O	EtherCAT General-Purpose Output 7	15	C3	7	C3	6
ESC_GPO8	O	EtherCAT General-Purpose Output 8	141	H13			
ESC_GPO9	O	EtherCAT General-Purpose Output 9	142	H14			
ESC_GPO10	O	EtherCAT General-Purpose Output 10	95	A4			
ESC_GPO11	O	EtherCAT General-Purpose Output 11	96	B4			
ESC_GPO12	O	EtherCAT General-Purpose Output 12	145	H15			
ESC_GPO13	O	EtherCAT General-Purpose Output 13	146	H16			
ESC_GPO14	O	EtherCAT General-Purpose Output 14	147	H12			
ESC_GPO15	O	EtherCAT General-Purpose Output 15	148	C12			
ESC_GPO16	O	EtherCAT General-Purpose Output 16	149	B12			
ESC_GPO17	O	EtherCAT General-Purpose Output 17	150	A12			
ESC_GPO18	O	EtherCAT General-Purpose Output 18	151	F11			
ESC_GPO19	O	EtherCAT General-Purpose Output 19	152	E11			
ESC_GPO20	O	EtherCAT General-Purpose Output 20	153	D11			
ESC_GPO21	O	EtherCAT General-Purpose Output 21	154	C11			
ESC_GPO22	O	EtherCAT General-Purpose Output 22	155	B11			
ESC_GPO23	O	EtherCAT General-Purpose Output 23	156	A11			
ESC_GPO24	O	EtherCAT General-Purpose Output 24	157	E10			
ESC_GPO25	O	EtherCAT General-Purpose Output 25	158	D10			
ESC_GPO26	O	EtherCAT General-Purpose Output 26	159	C10			
ESC_GPO27	O	EtherCAT General-Purpose Output 27	160	B10			
ESC_GPO28	O	EtherCAT General-Purpose Output 28	161	E9			
ESC_GPO29	O	EtherCAT General-Purpose Output 29	162	A8			
ESC_GPO30	O	EtherCAT General-Purpose Output 30	163	B8			
ESC_GPO31	O	EtherCAT General-Purpose Output 31	164	C8			
ESC_I2C_SCL	I/OC	EtherCAT I2C Clock	30, 41, 68, 151, 214	C16, F11, L10, R8, R15	63, 79, 89, 133	B13, L6, L9, M12	40, 48, 51
ESC_I2C_SDA	I/OC	EtherCAT I2C Data	29, 40, 67, 150, 216	A12, D15, N7, P11, P13	65, 73, 87, 132	L8, N6, N12	
ESC_LATCH0	I	EtherCAT Latch Signal Input 0	29, 34, 50, 60, 125, 216	L15, M8, N7, P10, P11, P14	65, 70, 73, 94, 105	K7, K9, L8, N6	42, 54
ESC_LATCH1	I	EtherCAT Latch Signal Input 1	30, 35, 51, 61, 126, 214	K16, L10, N10, N14, R8, T9	63, 71, 79, 95, 107	H11, K10, L6, L9, N8	40, 43, 48, 56
ESC_LED_ERR	O	EtherCAT Error LED	33, 60, 145, 213	H15, L15, R10, T8	62, 69, 105	L5, L7	39, 54
ESC_LED_LINK0_ACTIVE	O	EtherCAT Link-0 Active	58, 211	L13, R6	59, 103	J6, J10	52
ESC_LED_LINK1_ACTIVE	O	EtherCAT Link-1 Active	59, 212	L14, T7	60, 104	H13, K6	53
ESC_LED_RUN	O	EtherCAT Run LED	39, 61, 146, 219	H16, K16, L12, R7	61, 86, 107	H11	56
ESC_LED_STATE_RUN	O	EtherCAT LED State Run	62, 133, 147, 206	H12, J15, K15, L5	30, 108, 118	F13, H5, H10	14, 57
ESC_MDIO_CLK	O	EtherCAT MDIO Clock	26, 46, 52, 62, 152, 203	E11, F14, K5, K15, L11, N15	27, 82, 96, 108, 128	G5, H10, K11, L10	11, 57, 71
ESC_MDIO_DATA	I/O	EtherCAT MDIO Data	27, 39, 47, 53, 153, 204	D11, E14, G13, L6, L12, N16	28, 86, 97, 125, 129	D11, G6, K12	12, 72
ESC_PDI_UC_IRQ	O	EtherCAT PDI IRQ Interrupt Line	198, 222, 224	K4, P16, T12	26, 77, 92	G4, L12, N9	46
ESC_PHY0_LINKSTATUS	I	EtherCAT PHY-0 Link Status	55, 86, 148	B9, C12, M14	100, 156	B7, J13	87
ESC_PHY1_LINKSTATUS	I	EtherCAT PHY-1 Link Status	14, 68, 149	B3, B12, C16	6, 133	B13, C2	5
ESC_PHY_CLK	O	EtherCAT PHY Clock	48, 54, 154, 206	C11, L5, M13, R16	30, 90, 98	H5, K13, M13	14
ESC_PHY_RESETn	O	EtherCAT PHY Active Low Reset	23, 76, 155	A14, B11, G1	21, 143	E9, F2	
ESC_RX0_CLK	I	EtherCAT MII Receive-0 Clock	24, 77, 163	B8, E8, F13	144, 159	D7, D9	
ESC_RX0_DATA0	I	EtherCAT MII Receive-0 Data-0	27, 80, 165	A13, F6, G13	125, 148	D11, E8	83

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
ESC_RX0_DATA1	I	EtherCAT MII Receive-0 Data-1	24, 28, 81, 166	B5, E8, F12, N11	74, 149, 159	D7, K8	
ESC_RX0_DATA2	I	EtherCAT MII Receive-0 Data-2	29, 82, 167, 210	E5, E12, P6, P11	58, 73, 150	D8, K5, L8	
ESC_RX0_DATA3	I	EtherCAT MII Receive-0 Data-3	83, 84, 168	D9, D12, F5	151, 154	A8, C8	85
ESC_RX0_DV	I	EtherCAT MII Receive-0 Data Valid	25, 78, 162	A8, A10, E13	145, 153	B8, C9	82, 84
ESC_RX0_ERR	I	EtherCAT MII Receive-0 Error	26, 79, 164	C8, D13, L11	82, 146	B9, L10	
ESC_RX1_CLK	I	EtherCAT MII Receive-1 Clock	16, 69, 207	B16, D3, N5	8, 55, 134	B12, C4, J4	36, 75
ESC_RX1_DATA0	I	EtherCAT MII Receive-1 Data-0	63	K14	109	G13	58
ESC_RX1_DATA1	I	EtherCAT MII Receive-1 Data-1	64	K13	110	G12	59
ESC_RX1_DATA2	I	EtherCAT MII Receive-1 Data-2	65, 141	H13, K12	111	G11	60
ESC_RX1_DATA3	I	EtherCAT MII Receive-1 Data-3	66, 142	H14, K11	112	G10	61
ESC_RX1_DV	I	EtherCAT MII Receive-1 Data Valid	17, 70, 208	C15, E3, P5	9, 56, 135	A12, D4, K4	37, 76
ESC_RX1_ERR	I	EtherCAT MII Receive-1 Error	18, 71, 209	B15, F3, N6	10, 57, 136	B11, D3, J5	38, 77
ESC_SYNC0	O	EtherCAT SyncSignal Output 0	29, 34, 104, 127, 216	B13, N7, P10, P11, R9	65, 70, 73, 147	A9, K7, L8, N6	42
ESC_SYNC1	O	EtherCAT SyncSignal Output 1	30, 35, 105, 128, 214	L10, L16, M9, N10, R8	63, 71, 79, 106	H12, L6, L9, N8	40, 43, 48
ESC_TX0_CLK	I	EtherCAT MII Transmit-0 Clock	57, 85, 157	C9, E10, M16	102, 155	A7, J11	86
ESC_TX0_DATA0	O	EtherCAT MII Transmit-0 Data-0	10, 87, 158	A9, D4, D10	1, 157	B3, C7	88, 100
ESC_TX0_DATA1	O	EtherCAT MII Transmit-0 Data-1	11, 88, 159	B6, C10, E4	2, 170	B2, C5	1
ESC_TX0_DATA2	O	EtherCAT MII Transmit-0 Data-2	12, 89, 160	B10, C6, G4	4, 171	B1, D5	3, 96
ESC_TX0_DATA3	O	EtherCAT MII Transmit-0 Data-3	13, 90, 161	A3, D6, E9	5, 172	C1, E5	4, 97
ESC_TX0_ENA	I/O	EtherCAT MII Transmit-0 Enable	56, 84, 156	A11, D9, M15	101, 154	A8, J12	85
ESC_TX1_CLK	I	EtherCAT MII Transmit-1 Clock	44, 93, 130	C5, J12, T10	113, 175	A3, F10	
ESC_TX1_DATA0	O	EtherCAT MII Transmit-1 Data-0	22, 75, 131	A2, B14, N13	11, 142	A10, D2	
ESC_TX1_DATA1	O	EtherCAT MII Transmit-1 Data-1	21, 74, 132, 200	C14, D2, J1, T14	14, 23, 141	B10, E2, G1	10
ESC_TX1_DATA2	O	EtherCAT MII Transmit-1 Data-2	20, 73, 134, 201	C2, D14, J2, R14	13, 24, 140	C10, E1, G2	81
ESC_TX1_DATA3	O	EtherCAT MII Transmit-1 Data-3	19, 72, 202	A15, B2, K3	12, 25, 139	A11, D1, G3	80
ESC_TX1_ENA	I/O	EtherCAT MII Transmit-1 Enable	45, 94, 129	D5, J13, L9	115, 176	A2, F11	
EXTSYNCOUT	O	External ePWM Synchronization Pulse	6, 207	F7, N5	55, 166	A5, J4	36
FSIRXA_CLK	I	FSIRX-A Input Clock	5, 9, 13, 54, 105, 156	A3, A11, E1, E7, L16, M13	5, 19, 98, 106, 165	C1, E6, F3, H12, K13	4
FSIRXA_D0	I	FSIRX-A Primary Data Input	3, 8, 12, 52, 103, 154	C7, C11, D1, G4, G12, N15	4, 18, 96, 126, 163	B1, C6, D10, E3, K11	3, 92
FSIRXA_D1	I	FSIRX-A Optional Additional Data Input	4, 10, 11, 53, 104, 155	B11, B13, D4, D7, E4, N16	1, 2, 97, 147, 164	A9, B2, B3, D6, K12	1, 93, 100
FSIRXB_CLK	I	FSIRX-B Input Clock	11, 60, 112, 162	A8, E4, H4, L15	2, 105	B2	1, 54
FSIRXB_D0	I	FSIRX-B Primary Data Input	9, 58, 70, 110, 160	B10, C15, E1, H2, L13	19, 103, 135	A12, F3, J10	52, 76
FSIRXB_D1	I	FSIRX-B Optional Additional Data Input	10, 59, 111, 161	D4, E9, H3, L14	1, 104	B3, H13	53, 100
FSIRXC_CLK	I	FSIRX-C Input Clock	14, 165	B3, F6	6	C2	5
FSIRXC_D0	I	FSIRX-C Primary Data Input	12, 115, 163	B8, G4, P9	4	B1	3
FSIRXC_D1	I	FSIRX-C Optional Additional Data Input	13, 116, 164	A3, C8, H11	5	C1	4
FSIRXD_CLK	I	FSIRX-D Input Clock	17, 39, 41, 44, 92, 120, 168	A5, E3, F5, J12, L12, M11, R15	9, 86, 89, 113, 174	A4, D4, F10, M12	51, 99
FSIRXD_D0	I	FSIRX-D Primary Data Input	15, 42, 166	B5, C3, E16	7, 130	C3, C12	6, 73
FSIRXD_D1	I	FSIRX-D Optional Additional Data Input	16, 43, 100, 119, 167	D3, D16, E5, F4, M10	8, 131	C4, C11	2, 74
FSITXA_CLK	O	FSITX-A Output Clock	2, 10, 27, 51, 102, 153, 204	B7, C13, D4, D11, G13, L6, N14	1, 28, 95, 125, 162	B3, B6, D11, G6, K10	12, 91, 100
FSITXA_D0	O	FSITX-A Primary Data Output	0, 9, 26, 49, 100, 151, 203	E1, F4, F8, F11, K5, L11, P15	19, 27, 82, 93, 160	E7, F3, G5, L10, L13	2, 11, 89
FSITXA_D1	O	FSITX-A Optional Additional Data Output	1, 8, 25, 50, 101, 152, 202	A7, A10, D1, E11, K3, N9, P14	18, 25, 94, 153, 161	A6, B8, E3, G3, K9	84, 90
FSITXB_CLK	O	FSITX-B Output Clock	8, 56, 65, 108, 159	C10, D1, G2, K12, M15	18, 101, 111	E3, G11, J12	60
FSITXB_D0	O	FSITX-B Primary Data Output	6, 55, 69, 106, 157	B16, E10, F1, F7, M14	20, 100, 134, 166	A5, B12, J13	75
FSITXB_D1	O	FSITX-B Optional Additional Data Output	7, 57, 66, 107, 158	A6, D10, F2, K11, M16	102, 112, 167	B5, G10, J11	61
GPIO0	I/O	General-Purpose Input Output 0	0	F8	160	E7	89

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
GPIO1	I/O	General-Purpose Input Output 1	1	A7	161	A6	90
GPIO2	I/O	General-Purpose Input Output 2	2	B7	162	B6	91
GPIO3	I/O	General-Purpose Input Output 3	3	C7	163	C6	92
GPIO4	I/O	General-Purpose Input Output 4	4	D7	164	D6	93
GPIO5	I/O	General-Purpose Input Output 5	5	E7	165	E6	
GPIO6	I/O	General-Purpose Input Output 6	6	F7	166	A5	
GPIO7	I/O	General-Purpose Input Output 7	7	A6	167	B5	
GPIO8	I/O	General-Purpose Input Output 8	8	D1	18	E3	
GPIO9	I/O	General-Purpose Input Output 9	9	E1	19	F3	
GPIO10	I/O	General-Purpose Input Output 10	10	D4	1	B3	100
GPIO11	I/O	General-Purpose Input Output 11	11	E4	2	B2	1
GPIO12	I/O	General-Purpose Input Output 12	12	G4	4	B1	3
GPIO13	I/O	General-Purpose Input Output 13	13	A3	5	C1	4
GPIO14	I/O	General-Purpose Input Output 14	14	B3	6	C2	5
GPIO15	I/O	General-Purpose Input Output 15	15	C3	7	C3	6
GPIO16	I/O	General-Purpose Input Output 16	16	D3	8	C4	
GPIO17	I/O	General-Purpose Input Output 17	17	E3	9	D4	
GPIO18	I/O	General-Purpose Input Output 18	18	F3	10	D3	
GPIO19	I/O	General-Purpose Input Output 19	19	B2	12	D1	
GPIO20	I/O	General-Purpose Input Output 20	20	C2	13	E1	
GPIO21	I/O	General-Purpose Input Output 21	21	D2	14	E2	
GPIO22	I/O	General-Purpose Input Output 22	22	A2	11	D2	
GPIO23	I/O	General-Purpose Input Output 23	23	G1	21	F2	
GPIO24	I/O	General-Purpose Input Output 24	24	E8	159	D7	
GPIO25	I/O	General-Purpose Input Output 25	25	A10	153	B8	84
GPIO26	I/O	General-Purpose Input Output 26	26	L11	82	L10	
GPIO27	I/O	General-Purpose Input Output 27	27	G13	125	D11	
GPIO28	I/O	General-Purpose Input Output 28	28	N11	74	K8	
GPIO29	I/O	General-Purpose Input Output 29	29	P11	73	L8	
GPIO30	I/O	General-Purpose Input Output 30	30	L10	79	L9	48
GPIO31	I/O	General-Purpose Input Output 31	31	D8	158		
GPIO32	I/O	General-Purpose Input Output 32	32	J14	116	F12	
GPIO33	I/O	General-Purpose Input Output 33	33	R10	69	L7	
GPIO34	I/O	General-Purpose Input Output 34	34	P10	70	K7	42
GPIO35	I/O	General-Purpose Input Output 35	35	N10	71	N8	43
GPIO36	I/O	General-Purpose Input Output 36	36	P12	83	N11	
GPIO37	I/O	General-Purpose Input Output 37	37	N12	84	M11	
GPIO38	I/O	General-Purpose Input Output 38	38	M12	85	L11	
GPIO39	I/O	General-Purpose Input Output 39	39	L12	86		
GPIO40	I/O	General-Purpose Input Output 40	40	P13	87	N12	
GPIO41	I/O	General-Purpose Input Output 41	41	R15	89	M12	51
GPIO42	I/O	General-Purpose Input Output 42	42	E16	130	C12	73
GPIO43	I/O	General-Purpose Input Output 43	43	D16	131	C11	74
GPIO44	I/O	General-Purpose Input Output 44	44	J12	113	F10	
GPIO45	I/O	General-Purpose Input Output 45	45	J13	115	F11	
GPIO46	I/O	General-Purpose Input Output 46	46	F14	128		71
GPIO47	I/O	General-Purpose Input Output 47	47	E14	129		72
GPIO48	I/O	General-Purpose Input Output 48	48	R16	90	M13	
GPIO49	I/O	General-Purpose Input Output 49	49	P15	93	L13	
GPIO50	I/O	General-Purpose Input Output 50	50	P14	94	K9	
GPIO51	I/O	General-Purpose Input Output 51	51	N14	95	K10	
GPIO52	I/O	General-Purpose Input Output 52	52	N15	96	K11	
GPIO53	I/O	General-Purpose Input Output 53	53	N16	97	K12	
GPIO54	I/O	General-Purpose Input Output 54	54	M13	98	K13	

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
GPIO55	I/O	General-Purpose Input Output 55	55	M14	100	J13	
GPIO56	I/O	General-Purpose Input Output 56	56	M15	101	J12	
GPIO57	I/O	General-Purpose Input Output 57	57	M16	102	J11	
GPIO58	I/O	General-Purpose Input Output 58	58	L13	103	J10	52
GPIO59	I/O	General-Purpose Input Output 59	59	L14	104	H13	53
GPIO60	I/O	General-Purpose Input Output 60	60	L15	105		54
GPIO61	I/O	General-Purpose Input Output 61	61	K16	107	H11	56
GPIO62	I/O	General-Purpose Input Output 62	62	K15	108	H10	57
GPIO63	I/O	General-Purpose Input Output 63	63	K14	109	G13	58
GPIO64	I/O	General-Purpose Input Output 64	64	K13	110	G12	59
GPIO65	I/O	General-Purpose Input Output 65	65	K12	111	G11	60
GPIO66	I/O	General-Purpose Input Output 66	66	K11	112	G10	61
GPIO67	I/O	General-Purpose Input Output 67	67	D15	132		
GPIO68	I/O	General-Purpose Input Output 68	68	C16	133	B13	
GPIO69	I/O	General-Purpose Input Output 69	69	B16	134	B12	75
GPIO70	I/O	General-Purpose Input Output 70	70	C15	135	A12	76
GPIO71	I/O	General-Purpose Input Output 71	71	B15	136	B11	77
GPIO72	I/O	General-Purpose Input Output 72	72	A15	139	A11	80
GPIO73	I/O	General-Purpose Input Output 73	73	D14	140	C10	81
GPIO74	I/O	General-Purpose Input Output 74	74	C14	141	B10	
GPIO75	I/O	General-Purpose Input Output 75	75	B14	142	A10	
GPIO76	I/O	General-Purpose Input Output 76	76	A14	143	E9	
GPIO77	I/O	General-Purpose Input Output 77	77	F13	144	D9	
GPIO78	I/O	General-Purpose Input Output 78	78	E13	145	C9	82
GPIO79	I/O	General-Purpose Input Output 79	79	D13	146	B9	
GPIO80	I/O	General-Purpose Input Output 80	80	A13	148	E8	83
GPIO81	I/O	General-Purpose Input Output 81	81	F12	149		
GPIO82	I/O	General-Purpose Input Output 82	82	E12	150	D8	
GPIO83	I/O	General-Purpose Input Output 83	83	D12	151	C8	
GPIO84	I/O	General-Purpose Input Output 84	84	D9	154	A8	85
GPIO85	I/O	General-Purpose Input Output 85	85	C9	155	A7	86
GPIO86	I/O	General-Purpose Input Output 86	86	B9	156	B7	87
GPIO87	I/O	General-Purpose Input Output 87	87	A9	157	C7	88
GPIO88	I/O	General-Purpose Input Output 88	88	B6	170	C5	
GPIO89	I/O	General-Purpose Input Output 89	89	C6	171	D5	96
GPIO90	I/O	General-Purpose Input Output 90	90	D6	172	E5	97
GPIO91	I/O	General-Purpose Input Output 91	91	E6	173	B4	98
GPIO92	I/O	General-Purpose Input Output 92	92	A5	174	A4	99
GPIO93	I/O	General-Purpose Input Output 93	93	C5	175	A3	
GPIO94	I/O	General-Purpose Input Output 94	94	D5	176	A2	
GPIO95	I/O	General-Purpose Input Output 95	95	A4			
GPIO96	I/O	General-Purpose Input Output 96	96	B4			
GPIO97	I/O	General-Purpose Input Output 97	97	C4			
GPIO98	I/O	General-Purpose Input Output 98	98	E2			
GPIO99	I/O	General-Purpose Input Output 99	99	C1	17	E4	
GPIO100	I/O	General-Purpose Input Output 100	100	F4			2
GPIO101	I/O	General-Purpose Input Output 101	101	N9			
GPIO102	I/O	General-Purpose Input Output 102	102	C13			
GPIO103	I/O	General-Purpose Input Output 103	103	G12	126	D10	
GPIO104	I/O	General-Purpose Input Output 104	104	B13	147	A9	
GPIO105	I/O	General-Purpose Input Output 105	105	L16	106	H12	
GPIO106	I/O	General-Purpose Input Output 106	106	F1	20		
GPIO107	I/O	General-Purpose Input Output 107	107	F2			
GPIO108	I/O	General-Purpose Input Output 108	108	G2			

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
GPIO109	I/O	General-Purpose Input Output 109	109	G3			
GPIO110	I/O	General-Purpose Input Output 110	110	H2			
GPIO111	I/O	General-Purpose Input Output 111	111	H3			
GPIO112	I/O	General-Purpose Input Output 112	112	H4			
GPIO113	I/O	General-Purpose Input Output 113	113	J3			
GPIO114	I/O	General-Purpose Input Output 114	114	J4			
GPIO115	I/O	General-Purpose Input Output 115	115	P9			
GPIO116	I/O	General-Purpose Input Output 116	116	H11			
GPIO119	I/O	General-Purpose Input Output 119	119	M10			
GPIO120	I/O	General-Purpose Input Output 120	120	M11			
GPIO122	I/O	General-Purpose Input Output 122	122	L7			
GPIO123	I/O	General-Purpose Input Output 123	123	M7			
GPIO124	I/O	General-Purpose Input Output 124	124	L8			
GPIO125	I/O	General-Purpose Input Output 125	125	M8			
GPIO126	I/O	General-Purpose Input Output 126	126	T9			
GPIO127	I/O	General-Purpose Input Output 127	127	R9			
GPIO128	I/O	General-Purpose Input Output 128	128	M9			
GPIO129	I/O	General-Purpose Input Output 129	129	L9			
GPIO130	I/O	General-Purpose Input Output 130	130	T10			
GPIO131	I/O	General-Purpose Input Output 131	131	N13			
GPIO132	I/O	General-Purpose Input Output 132	132	T14			
GPIO133	I/O	General-Purpose Input Output 133	133	J15	118	F13	
GPIO134	I/O	General-Purpose Input Output 134	134	R14			
GPIO141	I/O	General-Purpose Input Output 141	141	H13			
GPIO142	I/O	General-Purpose Input Output 142	142	H14			
GPIO145	I/O	General-Purpose Input Output 145	145	H15			
GPIO146	I/O	General-Purpose Input Output 146	146	H16			
GPIO147	I/O	General-Purpose Input Output 147	147	H12			
GPIO148	I/O	General-Purpose Input Output 148	148	C12			
GPIO149	I/O	General-Purpose Input Output 149	149	B12			
GPIO150	I/O	General-Purpose Input Output 150	150	A12			
GPIO151	I/O	General-Purpose Input Output 151	151	F11			
GPIO152	I/O	General-Purpose Input Output 152	152	E11			
GPIO153	I/O	General-Purpose Input Output 153	153	D11			
GPIO154	I/O	General-Purpose Input Output 154	154	C11			
GPIO155	I/O	General-Purpose Input Output 155	155	B11			
GPIO156	I/O	General-Purpose Input Output 156	156	A11			
GPIO157	I/O	General-Purpose Input Output 157	157	E10			
GPIO158	I/O	General-Purpose Input Output 158	158	D10			
GPIO159	I/O	General-Purpose Input Output 159	159	C10			
GPIO160	I/O	General-Purpose Input Output 160	160	B10			
GPIO161	I/O	General-Purpose Input Output 161	161	E9			
GPIO162	I/O	General-Purpose Input Output 162	162	A8			
GPIO163	I/O	General-Purpose Input Output 163	163	B8			
GPIO164	I/O	General-Purpose Input Output 164	164	C8			
GPIO165	I/O	General-Purpose Input Output 165	165	F6			
GPIO166	I/O	General-Purpose Input Output 166	166	B5			
GPIO167	I/O	General-Purpose Input Output 167	167	E5			
GPIO168	I/O	General-Purpose Input Output 168	168	F5			
GPIO198	I/O	General-Purpose Input Output 198	198	K4	26	G4	
GPIO199	I/O	General-Purpose Input Output 199	199	H1	22	F1	9
GPIO200	I/O	General-Purpose Input Output 200	200	J1	23	G1	10
GPIO201	I/O	General-Purpose Input Output 201	201	J2	24	G2	
GPIO202	I/O	General-Purpose Input Output 202	202	K3	25	G3	

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
GPIO203	I/O	General-Purpose Input Output 203	203	K5	27	G5	11
GPIO204	I/O	General-Purpose Input Output 204	204	L6	28	G6	12
GPIO205	I/O	General-Purpose Input Output 205	205	M6	29	H6	13
GPIO206	I/O	General-Purpose Input Output 206	206	L5	30	H5	14
GPIO207	I/O	General-Purpose Input Output 207	207	N5	55	J4	36
GPIO208	I/O	General-Purpose Input Output 208	208	P5	56	K4	37
GPIO209	I/O	General-Purpose Input Output 209	209	N6	57	J5	38
GPIO210	I/O	General-Purpose Input Output 210	210	P6	58	K5	
GPIO211	I/O	General-Purpose Input Output 211	211	R6	59	J6	
GPIO212	I/O	General-Purpose Input Output 212	212	T7	60	K6	
GPIO213	I/O	General-Purpose Input Output 213	213	T8	62	L5	39
GPIO214	I/O	General-Purpose Input Output 214	214	R8	63	L6	40
GPIO215	I/O	General-Purpose Input Output 215	215	P7	64	M6	
GPIO216	I/O	General-Purpose Input Output 216	216	N7	65	N6	
GPIO217	I/O	General-Purpose Input Output 217	217	P8	66	M7	
GPIO218	I/O	General-Purpose Input Output 218	218	N8	67	N7	
GPIO219	I/O	General-Purpose Input Output 219	219	R7	61		
GPIO220	I/O	General-Purpose Input Output 220	220	F16	123	D13	68
GPIO221	I/O	General-Purpose Input Output 221	221	G16	121	E13	66
GPIO222	I/O	General-Purpose Input Output 222	222	T12	77	N9	46
GPIO223	I/O	General-Purpose Input Output 223	223	R12	78	M9	47
GPIO224	I/O	General-Purpose Input Output 224	224	P16	92	L12	
I2CA_SCL	I/OD	I2C-A Open-Drain Bidirectional Clock	1, 32, 33, 43, 57, 92, 105, 218, 223	A5, A7, D16, J14, L16, M16, N8, R10, R12	67, 69, 78, 102, 106, 116, 131, 161, 174	A4, A6, C11, F12, H12, J11, L7, M9, N7	47, 74, 90, 99
I2CA_SDA	I/OD	I2C-A Open-Drain Bidirectional Data	0, 31, 32, 42, 56, 91, 104, 217, 218, 222	B13, D8, E6, E16, F8, J14, M15, N8, P8, T12	66, 67, 77, 101, 116, 130, 147, 158, 160, 173	A9, B4, C12, E7, F12, J12, M7, N7, N9	46, 73, 89, 98
I2CB_SCL	I/OD	I2C-B Open-Drain Bidirectional Clock	3, 35, 41, 69, 207	B16, C7, N5, N10, R15	55, 71, 89, 134, 163	B12, C6, J4, M12, N8	36, 43, 51, 75, 92
I2CB_SDA	I/OD	I2C-B Open-Drain Bidirectional Data	2, 34, 40, 66, 215	B7, K11, P7, P10, P13	64, 70, 87, 112, 162	B6, G10, K7, M6, N12	42, 61, 91
LINA_RX	I	LIN-A Receive	7, 15, 207	A6, C3, N5	7, 55, 167	B5, C3, J4	6, 36
LINA_TX	O	LIN-A Transmit	6, 14, 215	B3, F7, P7	6, 64, 166	A5, C2, M6	5
LINB_RX	I	LIN-B Receive	25, 68, 202, 209	A10, C16, K3, N6	25, 57, 133, 153	B8, B13, G3, J5	38, 84
LINB_TX	O	LIN-B Transmit	24, 32, 67, 201, 210, 213, 217, 218	D15, E8, J2, J14, N8, P6, P8, T8	24, 58, 62, 66, 67, 116, 132, 159	D7, F12, G2, K5, L5, M7, N7	39
MCANA_RX	I	CAN/CAN FD-A Receive	5, 10, 18, 23, 30, 36, 70, 75, 200, 214, 221	B14, C15, D4, E7, F3, G1, G16, J1, L10, P12, R8	1, 10, 21, 23, 63, 79, 83, 121, 135, 142, 165	A10, A12, B3, D3, E6, E13, F2, G1, L6, L9, N11	10, 40, 48, 66, 76, 100
MCANA_TX	O	CAN/CAN FD-A Transmit	4, 8, 19, 22, 31, 37, 71, 74, 199, 217, 220	A2, B2, B15, C14, D1, D7, D8, F16, H1, N12, P8	11, 12, 18, 22, 66, 84, 123, 136, 141, 158, 164	B10, B11, D1, D2, D6, D13, E3, F1, M7, M11	9, 68, 77, 93
MCANB_RX	I	CAN/CAN FD-B Receive	7, 21, 40, 44, 72, 120, 146	A6, A15, D2, H16, J12, M11, P13	14, 87, 113, 139, 167	A11, B5, E2, F10, N12	80
MCANB_TX	O	CAN/CAN FD-B Transmit	6, 20, 41, 45, 73, 119, 145	C2, D14, F7, H15, J13, M10, R15	13, 89, 115, 140, 166	A5, C10, E1, F11, M12	51, 81
OUTPUTXBAR1	O	Output X-BAR Output 1	2, 24, 34, 58, 201, 205, 224	B7, E8, J2, L13, M6, P10, P16	24, 29, 70, 92, 103, 159, 162	B6, D7, G2, H6, J10, K7, L12	13, 42, 52, 91
OUTPUTXBAR2	O	Output X-BAR Output 2	3, 25, 37, 59, 202, 206, 220	A10, C7, F16, K3, L5, L14, N12	25, 30, 84, 104, 123, 153, 163	B8, C6, D13, G3, H5, H13, M11	14, 53, 68, 84, 92
OUTPUTXBAR3	O	Output X-BAR Output 3	4, 5, 14, 26, 48, 60, 203, 207, 221	B3, D7, E7, G16, K5, L11, L15, N5, R16	6, 27, 55, 82, 90, 105, 121, 164, 165	C2, D6, E6, E13, G5, J4, L10, M13	5, 11, 36, 54, 66, 93
OUTPUTXBAR4	O	Output X-BAR Output 4	6, 15, 27, 49, 61, 204, 208, 222	C3, F7, G13, K16, L6, P5, P15, T12	7, 28, 56, 77, 93, 107, 125, 166	A5, C3, D11, G6, H11, K4, L13, N9	6, 12, 37, 46, 56
OUTPUTXBAR5	O	Output X-BAR Output 5	7, 28, 115, 209, 215, 223	A6, N6, N11, P7, P9, R12	57, 64, 74, 78, 167	B5, J5, K8, M6, M9	38, 47

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
OUTPUTXBAR6	O	Output X-BAR Output 6	9, 29, 73, 116, 210, 216	D14, E1, H11, N7, P6, P11	19, 58, 65, 73, 140	C10, F3, K5, L8, N6	81
OUTPUTXBAR7	O	Output X-BAR Output 7	11, 16, 30, 211, 214	D3, E4, L10, R6, R8	2, 8, 59, 63, 79	B2, C4, J6, L6, L9	1, 40, 48
OUTPUTXBAR8	O	Output X-BAR Output 8	14, 17, 31, 72, 217	A15, B3, D8, E3, P8	6, 9, 66, 139, 158	A11, C2, D4, M7	5, 80
PMBUSA_ALERT	I/OD	PMBus-A Open-Drain Bidirectional Alert Signal	11, 26, 93, 153, 203, 207, 220	C5, D11, E4, F16, K5, L11, N5	2, 27, 55, 82, 123, 175	A3, B2, D13, G5, J4, L10	1, 11, 36, 68
PMBUSA_CTL	I/O	PMBus-A Control Signal - Target Input/Controller Output	12, 27, 94, 154, 204, 208, 221	C11, D5, G4, G13, G16, L6, P5	4, 28, 56, 121, 125, 176	A2, B1, D11, E13, G6, K4	3, 12, 37, 66
PMBUSA_SCL	I/OD	PMBus-A Open-Drain Bidirectional Clock	14, 24, 91, 151, 201, 210, 223	B3, E6, E8, F11, J2, P6, R12	6, 24, 58, 78, 159, 173	B4, C2, D7, G2, K5, M9	5, 47, 98
PMBUSA_SDA	I/OD	PMBus-A Open-Drain Bidirectional Data	13, 25, 92, 152, 202, 209, 222	A3, A5, A10, E11, K3, N6, T12	5, 25, 57, 77, 153, 174	A4, B8, C1, G3, J5, N9	4, 38, 46, 84, 99
SCIA_RX	I	SCI-A Receive Data	9, 13, 28, 35, 43, 46, 49, 62, 64, 85, 207, 215, 222	A3, C9, D16, E1, F14, K13, K15, N5, N10, N11, P7, P15, T12	5, 19, 55, 64, 71, 74, 77, 93, 108, 110, 128, 131, 155	A7, C1, C11, F3, G12, H10, J4, K8, L13, M6, N8, N9	4, 36, 43, 46, 57, 59, 71, 74, 86
SCIA_TX	O	SCI-A Transmit Data	8, 12, 29, 34, 36, 42, 47, 48, 63, 65, 84, 208, 216, 223	D1, D9, E14, E16, G4, K12, K14, N7, P5, P10, P11, P12, R12, R16	4, 18, 56, 65, 70, 73, 78, 83, 90, 109, 111, 129, 130, 154	A8, B1, C12, E3, G11, G13, K4, K7, L8, M9, M13, N6, N11	3, 37, 42, 47, 58, 60, 72, 73, 85
SCIB_RX	I	SCI-B Receive Data	11, 15, 19, 23, 39, 55, 71, 87, 142, 200, 221	A9, B2, B15, C3, E4, G1, G16, H14, J1, L12, M14	2, 7, 12, 21, 23, 86, 100, 121, 136, 157	B2, B11, C3, C7, D1, E13, F2, G1, J13	1, 6, 10, 66, 77, 88
SCIB_TX	O	SCI-B Transmit Data	9, 10, 14, 18, 22, 38, 54, 70, 86, 141, 199, 220	A2, B3, B9, C15, D4, E1, F3, F16, H1, H13, M12, M13	1, 6, 10, 11, 19, 22, 85, 98, 123, 135, 156	A12, B3, B7, C2, D2, D3, D13, F1, F3, K13, L11	5, 9, 68, 76, 87, 100
SD1_C1	I	SDFM-1 Channel 1 Clock Input	17, 49, 53, 64, 96, 123	B4, E3, K13, M7, N16, P15	9, 93, 97, 110	D4, G12, K12, L13	59
SD1_C2	I	SDFM-1 Channel 2 Clock Input	19, 51, 54, 66, 98, 125	B2, E2, K11, M8, M13, N14	12, 95, 98, 112	D1, G10, K10, K13	61
SD1_C3	I	SDFM-1 Channel 3 Clock Input	21, 53, 55, 68, 90, 113, 127, 205	C16, D2, D6, J3, M6, M14, N16, R9	14, 29, 97, 100, 133, 172	B13, E2, E5, H6, J13, K12	13, 97
SD1_C4	I	SDFM-1 Channel 4 Clock Input	23, 55, 56, 70, 115, 129, 200	C15, G1, J1, L9, M14, M15, P9	21, 23, 100, 101, 135	A12, F2, G1, J12, J13	10, 76
SD1_D1	I	SDFM-1 Channel 1 Data Input	16, 36, 48, 63, 95, 100, 122	A4, D3, F4, K14, L7, P12, R16	8, 83, 90, 109	C4, G13, M13, N11	2, 58
SD1_D2	I	SDFM-1 Channel 2 Data Input	18, 37, 50, 65, 97, 124	C4, F3, K12, L8, N12, P14	10, 84, 94, 111	D3, G11, K9, M11	60
SD1_D3	I	SDFM-1 Channel 3 Data Input	20, 38, 52, 67, 89, 112, 126, 204	C2, C6, D15, H4, L6, M12, N15, T9	13, 28, 85, 96, 132, 171	D5, E1, G6, K11, L11	12, 96
SD1_D4	I	SDFM-1 Channel 4 Data Input	22, 39, 54, 69, 74, 77, 80, 114, 128, 199	A2, A13, B16, C14, F13, H1, J4, L12, M9, M13	11, 22, 86, 98, 134, 141, 144, 148	B10, B12, D2, D9, E8, F1, K13	9, 75, 83
SD2_C1	I	SDFM-2 Channel 1 Clock Input	25, 40, 57, 80, 131, 134, 202, 224	A10, A13, K3, M16, N13, P13, P16, R14	25, 87, 92, 102, 148, 153	B8, E8, G3, J11, L12, N12	83, 84
SD2_C2	I	SDFM-2 Channel 2 Clock Input	27, 48, 58, 59, 74, 133, 204	C14, G13, J15, L6, L13, L14, R16	28, 90, 103, 104, 118, 125, 141	B10, D11, F13, G6, H13, J10, M13	12, 52, 53
SD2_C3	I	SDFM-2 Channel 3 Clock Input	29, 59, 61, 76, 216	A14, K16, L14, N7, P11	65, 73, 104, 107, 143	E9, H11, H13, L8, N6	53, 56
SD2_C4	I	SDFM-2 Channel 4 Clock Input	31, 60, 63, 78, 217	D8, E13, K14, L15, P8	66, 105, 109, 145, 158	C9, G13, M7	54, 58, 82
SD2_D1	I	SDFM-2 Channel 1 Data Input	24, 41, 49, 56, 79, 130, 201	D13, E8, J2, M15, P15, R15, T10	24, 89, 93, 101, 146, 159	B9, D7, G2, J12, L13, M12	51
SD2_D2	I	SDFM-2 Channel 2 Data Input	26, 50, 58, 73, 132	D14, L11, L13, P14, T14	82, 94, 103, 140	C10, J10, K9, L10	52, 81
SD2_D3	I	SDFM-2 Channel 3 Data Input	28, 51, 60, 75, 134, 215	B14, L15, N11, N14, P7, R14	64, 74, 95, 105, 142	A10, K8, K10, M6	54
SD2_D4	I	SDFM-2 Channel 4 Data Input	30, 52, 62, 77, 214	F13, K15, L10, N15, R8	63, 79, 96, 108, 144	D9, H10, K11, L6, L9	40, 48, 57
SD3_C1	I	SDFM-3 Channel 1 Clock Input	72, 76, 105	A14, A15, L16	106, 139, 143	A11, E9, H12	80

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
SD3_C2	I	SDFM-3 Channel 2 Clock Input	78, 82, 84, 107	D9, E12, E13, F2	145, 150, 154	A8, C9, D8	82, 85
SD3_C3	I	SDFM-3 Channel 3 Clock Input	80, 86, 109	A13, B9, G3	148, 156	B7, E8	83, 87
SD3_C4	I	SDFM-3 Channel 4 Clock Input	44, 46, 88, 111	B6, F14, H3, J12	113, 128, 170	C5, F10	71
SD3_D1	I	SDFM-3 Channel 1 Data Input	71, 77, 85, 104, 203	B13, B15, C9, F13, K5	27, 136, 144, 147, 155	A7, A9, B11, D9, G5	11, 77, 86
SD3_D2	I	SDFM-3 Channel 2 Data Input	79, 83, 84, 106	D9, D12, D13, F1	20, 146, 151, 154	A8, B9, C8	85
SD3_D3	I	SDFM-3 Channel 3 Data Input	57, 81, 85, 108	C9, F12, G2, M16	102, 149, 155	A7, J11	86
SD3_D4	I	SDFM-3 Channel 4 Data Input	45, 87, 110	A9, H2, J13	115, 157	C7, F11	88
SD4_C1	I	SDFM-4 Channel 1 Clock Input	10, 90, 208	D4, D6, P5	1, 56, 172	B3, E5, K4	37, 97, 100
SD4_C2	I	SDFM-4 Channel 2 Clock Input	12, 92, 210	A5, G4, P6	4, 58, 174	A4, B1, K5	3, 99
SD4_C3	I	SDFM-4 Channel 3 Clock Input	40, 47, 94, 212	D5, E14, P13, T7	60, 87, 129, 176	A2, K6, N12	72
SD4_C4	I	SDFM-4 Channel 4 Clock Input	42, 100, 103, 219	E16, F4, G12, R7	61, 126, 130	C12, D10	2, 73
SD4_D1	I	SDFM-4 Channel 1 Data Input	11, 89, 207	C6, E4, N5	2, 55, 171	B2, D5, J4	1, 36, 96
SD4_D2	I	SDFM-4 Channel 2 Data Input	13, 91, 209	A3, E6, N6	5, 57, 173	B4, C1, J5	4, 38, 98
SD4_D3	I	SDFM-4 Channel 3 Data Input	41, 93, 211	C5, R6, R15	59, 89, 175	A3, J6, M12	51
SD4_D4	I	SDFM-4 Channel 4 Data Input	43, 73, 76, 78, 99, 213	A14, C1, D14, D16, E13, T8	17, 62, 131, 140, 143, 145	C9, C10, C11, E4, E9, L5	39, 74, 81, 82
SPIA_CLK	I/O	SPI-A Clock	18, 34, 56, 60, 204	F3, L6, L15, M15, P10	10, 28, 70, 101, 105	D3, G6, J12, K7	12, 42, 54
SPIA_PICO	I/O	SPI-A Peripheral In, Controller Out (PICO)	16, 32, 54, 58, 100, 198, 218, 222	D3, F4, J14, K4, L13, M13, N8, T12	8, 26, 67, 77, 98, 103, 116	C4, F12, G4, J10, K13, N7, N9	2, 46, 52
SPIA_POCI	I/O	SPI-A Peripheral Out, Controller In (POCI)	17, 33, 55, 59, 203	E3, K5, L14, M14, R10	9, 27, 69, 100, 104	D4, G5, H13, J13, L7	11, 53
SPIA_PTE	I/O	SPI-A Peripheral Transmit Enable (PTE)	19, 35, 57, 61, 205	B2, K16, M6, M16, N10	12, 29, 71, 102, 107	D1, H6, H11, J11, N8	13, 43, 56
SPIB_CLK	I/O	SPI-B Clock	22, 26, 58, 65, 199, 203	A2, H1, K5, K12, L11, L13	11, 22, 27, 82, 103, 111	D2, F1, G5, G11, J10, L10	9, 11, 52, 60
SPIB_PICO	I/O	SPI-B Peripheral In, Controller Out (PICO)	24, 60, 63, 201, 208	E8, J2, K14, L15, P5	24, 56, 105, 109, 159	D7, G2, G13, K4	37, 54, 58
SPIB_POCI	I/O	SPI-B Peripheral Out, Controller In (POCI)	25, 61, 64, 202, 209	A10, K3, K13, K16, N6	25, 57, 107, 110, 153	B8, G3, G12, H11, J5	38, 56, 59, 84
SPIB_PTE	I/O	SPI-B Peripheral Transmit Enable (PTE)	23, 27, 59, 66, 200, 204	G1, G13, J1, K11, L6, L14	21, 23, 28, 104, 112, 125	D11, F2, G1, G6, G10, H13	10, 12, 53, 61
SPIC_CLK	I/O	SPI-C Clock	22, 52, 71, 102, 124, 199, 222	A2, B15, C13, H1, L8, N15, T12	11, 22, 77, 96, 136	B11, D2, F1, K11, N9	9, 46, 77
SPIC_PICO	I/O	SPI-C Peripheral In, Controller Out (PICO)	20, 50, 69, 100, 122	B16, C2, F4, L7, P14	13, 94, 134	B12, E1, K9	2, 75
SPIC_POCI	I/O	SPI-C Peripheral Out, Controller In (POCI)	21, 51, 70, 101, 123, 215	C15, D2, M7, N9, N14, P7	14, 64, 95, 135	A12, E2, K10, M6	76
SPIC_PTE	I/O	SPI-C Peripheral Transmit Enable (PTE)	23, 53, 72, 103, 125, 200, 223	A15, G1, G12, J1, M8, N16, R12	21, 23, 78, 97, 126, 139	A11, D10, F2, G1, K12, M9	10, 47, 80
SPID_CLK	I/O	SPI-D Clock	32, 75, 90, 93, 128, 216, 218	B14, C5, D6, J14, M9, N7, N8	65, 67, 116, 142, 172, 175	A3, A10, E5, F12, N6, N7	97
SPID_PICO	I/O	SPI-D Peripheral In, Controller Out (PICO)	30, 91, 126, 214	E6, L10, R8, T9	63, 79, 173	B4, L6, L9	40, 48, 98
SPID_POCI	I/O	SPI-D Peripheral Out, Controller In (POCI)	31, 44, 92, 127, 217, 220	A5, D8, F16, J12, P8, R9	66, 113, 123, 158, 174	A4, D13, F10, M7	68, 99
SPID_PTE	I/O	SPI-D Peripheral Transmit Enable (PTE)	33, 45, 89, 94, 129, 217, 221	C6, D5, G16, J13, L9, P8, R10	66, 69, 115, 121, 171, 176	A2, D5, E13, F11, L7, M7	66, 96
TDI	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.	222	T12	77	N9	46
TDO	O	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.	223	R12	78	M9	47
UARTA_RX	I/O	UART-A Serial Data Receive	3, 28, 39, 43, 73, 85	C7, C9, D14, D16, L12, N11	74, 86, 131, 140, 155, 163	A7, C6, C10, C11, K8	74, 81, 86, 92
UARTA_TX	I/O	UART-A Serial Data Transmit	2, 29, 38, 42, 72, 84	A15, B7, D9, E16, M12, P11	73, 85, 130, 139, 154, 162	A8, A11, B6, C12, L8, L11	73, 80, 85, 91
UARTB_RX	I/O	UART-B Serial Data Receive	45, 71, 223	B15, J13, R12	78, 115, 136	B11, F11, M9	47, 77
UARTB_TX	I/O	UART-B Serial Data Transmit	44, 70, 222	C15, J12, T12	77, 113, 135	A12, F10, N9	46, 76

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Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	256 ZEJ	176 PTP	169 NMR	100 PZP
USB0DM	O	USB-0 PHY differential data	42	E16	130	C12	73
USB0DP	O	USB-0 PHY differential data	43	D16	131	C11	74
X1	I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.	220	F16	123	D13	68
X2	I/O	Crystal oscillator output.	221	G16	121	E13	66
XCLKOUT	O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.	73, 224	D14, P16	92, 140	C10, L12	81

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5.3.3 Power and Ground

Table 5-4. Power and Ground

SIGNAL NAME	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
VDD	1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.	F9, F10, G6, J11, K8, K9	16, 76, 117, 137, 169	F5, F7, G9, J9	8, 45, 63, 78, 95
VDD3VFL	3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin. Connect this pin to 3.3-V supply.	R11, T11	72	M8	44
VDDA	3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin. Connect this pin to 3.3-V supply.	N1, T6	36, 54	L2, M5	18, 35
VDDIO	3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin. Connect this pin to 3.3-V supply.	B1, E15, G7, G8, H5, J5, J10, K7, K10, T15	3, 15, 68, 75, 88, 91, 99, 114, 127, 138, 152, 168	C13, F4, F6, F8, H9, J8	7, 41, 55, 62, 70, 79, 94
VDDOSC	Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-µF (minimum) decoupling capacitor on each pin. Connect this pin to 3.3-V supply.	G15	120	E11	65
VSS	Digital Ground	A1, A16, G5, G9, G10, G11, H6, H7, H8, H9, H10, J6, J7, J8, J9, K6, T16	PAD	A1, A13, F9, G7, G8, H7, H8, J7, N13	PAD
VSSA	Analog Ground	M3, N2, T1, T5	34, 52	L1, N1, N5	17, 33
VSSOSC	Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.	F15	122	E12	67

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5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

SIGNAL NAME	PIN TYPE	DESCRIPTION	256 ZEJ	176 PTP	169 NMR	100 PZP
TCK	I	JTAG test clock with internal pullup.	R13	81	M10	50
TMS	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.	T13	80	N10	49
VREGENZ	I	Internal voltage regulator enable with internal pullup. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply.	J16	119	E10	64
XRSn	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.	G14	124	D12	69

5.4 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 5-6 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 5-6 with pullups and pulldowns are always on and cannot be disabled.

Table 5-6. Pins With Internal Pullup and Pulldown

PIN	RESET (XRSn = 0)	DEVICE BOOT	APPLICATION
GPIOx	Pullup disabled	Pullup disabled(1)	Application defined
GPIO222/TDI	Pullup disabled		Application defined
GPIO223/TDO	Pullup disabled		Application defined
TCK	Pullup active		
TMS	Pullup active		
XRSn	Pullup active		
Other pins (including AIOs)	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.5 Pin Multiplexing

Section 5.5.1 lists the GPIO muxed pins.

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5.5.1 GPIO Muxed Pins

Table 5-7. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A			CLB_OUTPUTXBAR1	I2CA_SDA		EMIF1_A13	ESC_GPI0		FSITXA_D0			
GPIO1	EPWM1_B			CLB_OUTPUTXBAR2	I2CA_SCL		EMIF1_A14	ESC_GPI1		FSITXA_D1			
GPIO2	EPWM2_A			OUTPUTXBAR1	I2CB_SDA	UARTA_TX	EMIF1_A15	ESC_GPI2		FSITXA_CLK			
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	I2CB_SCL	UARTA_RX		ESC_GPI3		FSIRXA_D0			
GPIO4	EPWM3_A			OUTPUTXBAR3	CANA_TX		MCANA_TX	ESC_GPI4		FSIRXA_D1			
GPIO5	EPWM3_B		OUTPUTXBAR3	CLB_OUTPUTXBAR3	CANA_RX		MCANA_RX	ESC_GPI5		FSIRXA_CLK			
GPIO6	EPWM4_A	OUTPUTXBAR4	EXTSYNCOUT	EQEP3_A	MCANB_TX	LINA_TX	EMIF1_DQM0	ESC_GPI6		FSITXB_D0			
GPIO7	EPWM4_B		OUTPUTXBAR5	EQEP3_B	MCANB_RX	LINA_RX	EMIF1_DQM1	ESC_GPI7		FSITXB_D1			
GPIO8	EPWM5_A	EMIF1_RAS	ADCSOCAO	EQEP3_STROBE	SCIA_TX	CLB_OUTPUTXBAR4	MCANA_TX	ESC_GPO0		FSITXB_CLK	FSITXA_D1	FSIRXA_D0	
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP3_INDEX	SCIA_RX			ESC_GPO1		FSIRXB_D0	FSITXA_D0	FSIRXA_CLK	
GPIO10	EPWM6_A	EMIF1_CAS	ADCSOCBO	EQEP1_A	SCIB_TX	SD4_C1	MCANA_RX	CLB_OUTPUTXBAR5	ESC_TX0_DATA0	FSIRXB_D1	FSITXA_CLK	FSIRXA_D1	
GPIO11	EPWM6_B	SCIB_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SD4_D1		ESC_GPO3	ESC_TX0_DATA1	FSIRXB_CLK	FSIRXA_D1	PMBUSA_ALERT	
GPIO12	EPWM7_A	CLB_OUTPUTXBAR6	ADCSOCAO	EQEP1_STROBE	SCIA_TX	SD4_C2	EMIF1_A1	ESC_GPO4	ESC_TX0_DATA2	FSIRXC_D0	FSIRXA_D0	PMBUSA_CTL	
GPIO13	EPWM7_B	CLB_OUTPUTXBAR7	EQEP5_STROBE	EQEP1_INDEX	SCIA_RX	SD4_D2	EMIF1_CS0n	ESC_GPO5	ESC_TX0_DATA3	FSIRXC_D1	FSIRXA_CLK	PMBUSA_SDA	
GPIO14	EPWM8_A	SCIB_TX	EQEP5_INDEX	LINA_TX	OUTPUTXBAR3	OUTPUTXBAR8		ESC_GPO6	ESC_PHY1_LINKSTATUS	FSIRXC_CLK	EMIF1_D17	PMBUSA_SCL	
GPIO15	EPWM8_B	SCIB_RX		LINA_RX	OUTPUTXBAR4	CLB_OUTPUTXBAR8		ESC_GPO7	EQEP5_A	FSIRXD_D0		EMIF1_DQM2	
GPIO16	SPIA_PICO		OUTPUTXBAR7	EPWM9_A		SD1_D1			EQEP5_B	FSIRXD_D1		ESC_RX1_CLK	
GPIO17	SPIA_POCI		OUTPUTXBAR8	EPWM9_B		SD1_C1			EQEP5_STROBE	FSIRXD_CLK		ESC_RX1_DV	
GPIO18	SPIA_CLK	SCIB_TX	CANA_RX	EPWM10_A		SD1_D2	MCANA_RX	EMIF1_CS2n	EQEP5_INDEX			ESC_RX1_ERR	
GPIO19	SPIA_PTE	SCIB_RX	CANA_TX	EPWM10_B		SD1_C2	MCANA_TX	EMIF1_CS3n				ESC_TX1_DATA3	
GPIO20	EQEP1_A			EPWM11_A		SD1_D3	MCANB_TX	EMIF1_BA0			SPIC_PICO	ESC_TX1_DATA2	
GPIO21	EQEP1_B			EPWM11_B		SD1_C3	MCANB_RX	EMIF1_BA1			SPIC_POCI	ESC_TX1_DATA1	
GPIO22	EQEP1_STROBE		SCIB_TX	EPWM12_A	SPIB_CLK	SD1_D4	MCANA_TX	EMIF1_RAS			SPIC_CLK	ESC_TX1_DATA0	
GPIO23	EQEP1_INDEX		SCIB_RX	EPWM12_B	SPIB_PTE	SD1_C4	MCANA_RX	EMIF1_CAS			SPIC_PTE	ESC_PHY_RESETn	
GPIO24	OUTPUTXBAR1	EQEP2_A		LINB_TX	SPIB_PICO	SD2_D1	PMBUSA_SCL	EMIF1_DQM0		EPWM13_A	ESC_RX0_DATA1	ESC_RX0_CLK	

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Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO25	OUTPUTXBAR2	EQEP2_B		LINB_RX	SPIB_POCI	SD2_C1	PMBUSA_SDA	EMIF1_DQM1	EQEP5_B	EPWM13_B	FSITXA_D1	ESC_RX0_DV	
GPIO26	OUTPUTXBAR3	EQEP2_INDEX		OUTPUTXBAR3	SPIB_CLK	SD2_D2	PMBUSA_ALERT	EMIF1_DQM2	ESC_MDIO_CLK	EPWM14_A	FSITXA_D0	ESC_RX0_ERR	
GPIO27	OUTPUTXBAR4	EQEP2_STROBE		OUTPUTXBAR4	SPIB_PTE	SD2_C2	PMBUSA_CTL	EMIF1_DQM3	ESC_MDIO_DATA	EPWM14_B	FSITXA_CLK	ESC_RX0_DATA0	
GPIO28	SCIA_RX	EMIF1_CS4n	UARTA_RX	OUTPUTXBAR5	EQEP3_A	SD2_D3	EMIF1_CS2n			EPWM15_A		ESC_RX0_DATA1	
GPIO29	SCIA_TX	EMIF1_SDCKE	UARTA_TX	OUTPUTXBAR6	EQEP3_B	SD2_C3	EMIF1_CS3n	ESC_LATCH0	ESC_I2C_SDA	EPWM15_B	ESC_SYNC0	ESC_RX0_DATA2	
GPIO30	CANA_RX	EMIF1_CLK	MCANA_RX	OUTPUTXBAR7	EQEP3_STROBE	SD2_D4	EMIF1_CS4n	ESC_LATCH1	ESC_I2C_SCL	EPWM16_A	ESC_SYNC1	SPID_PICO	
GPIO31	CANA_TX	EMIF1_WEn	MCANA_TX	OUTPUTXBAR8	EQEP3_INDEX	SD2_C4	EMIF1_RNW	I2CA_SDA		EPWM16_B		SPID_POCI	
GPIO32	I2CA_SDA	EMIF1_CS0n	SPIA_PICO	EQEP4_A	LINB_TX	CLB_OUTPUTXBAR1	EMIF1_OEn	I2CA_SCL				SPID_CLK	
GPIO33	I2CA_SCL	EMIF1_RNW	SPIA_POCI	EQEP4_B		CLB_OUTPUTXBAR2	EMIF1_BA0		ESC_LED_ERR			SPID_PTE	
GPIO34	OUTPUTXBAR1	EMIF1_CS2n	SPIA_CLK	EQEP4_STROBE	I2CB_SDA	CLB_OUTPUTXBAR3	EMIF1_BA1	ESC_LATCH0	EPWM18_A	SCIA_TX	ESC_SYNC0		
GPIO35	SCIA_RX	EMIF1_CS3n	SPIA_PTE	EQEP4_INDEX	I2CB_SCL	CLB_OUTPUTXBAR4	EMIF1_A0	ESC_LATCH1	EPWM18_B	SCIA_RX	ESC_SYNC1		
GPIO36	SCIA_TX	EMIF1_WAIT			CANA_RX	CLB_OUTPUTXBAR5	EMIF1_A1	MCANA_RX		SD1_D1	EMIF1_WEn		
GPIO37	OUTPUTXBAR2	EMIF1_OEn	EPWM18_A		CANA_TX	CLB_OUTPUTXBAR6	EMIF1_A2	MCANA_TX		SD1_D2	EMIF1_D24		
GPIO38		EMIF1_A0	EPWM18_B	UARTA_TX	SCIB_TX	CLB_OUTPUTXBAR7	EMIF1_A3			SD1_D3	EMIF1_CS2n		
GPIO39		EMIF1_A1		UARTA_RX	SCIB_RX	CLB_OUTPUTXBAR8	EMIF1_A4	ESC_MDIO_DATA	ESC_LED_RUN	SD1_D4	FSIRXD_CLK		
GPIO40		EMIF1_A2	EPWM13_A	MCANB_RX	I2CB_SDA	SD4_C3	ESC_GPO2	CLB_OUTPUTXBAR1		SD2_C1	ESC_I2C_SDA		
GPIO41		EMIF1_A3	EPWM13_B	MCANB_TX	I2CB_SCL	SD4_D3		CLB_OUTPUTXBAR2		SD2_D1	ESC_I2C_SCL	FSIRXD_CLK	
GPIO42			EPWM14_A	EQEP4_A	I2CA_SDA	SD4_C4		CLB_OUTPUTXBAR5	UARTA_TX		FSIRXD_D0	SCIA_TX	USB0DM
GPIO43			EPWM14_B	EQEP4_B	I2CA_SCL	SD4_D4		CLB_OUTPUTXBAR6	UARTA_RX		FSIRXD_D1	SCIA_RX	USB0DP
GPIO44	SPID_POCI	EMIF1_A4	MCANB_RX		SD3_C4	UARTB_TX		CLB_OUTPUTXBAR6		FSIRXD_CLK	ESC_TX1_CLK		
GPIO45	SPID_PTE	EMIF1_A5	MCANB_TX		SD3_D4	UARTB_RX		CLB_OUTPUTXBAR7			ESC_TX1_ENA		
GPIO46	EPWM4_A	EMIF1_A6	EPWM14_A		SCIA_RX	SD3_C4					ESC_MDIO_CLK		
GPIO47	EPWM4_B	EMIF1_A7	EPWM14_B		SCIA_TX	SD4_C3					ESC_MDIO_DATA		
GPIO48	OUTPUTXBAR3	EMIF1_A8			SCIA_TX	SD1_D1				SD2_C2	ESC_PHY_CLK		
GPIO49	OUTPUTXBAR4	EMIF1_A9			SCIA_RX	SD1_C1	EMIF1_A5			SD2_D1	FSITXA_D0		
GPIO50	EQEP1_A	EMIF1_A10	EPWM15_A		SPIC_PICO	SD1_D2	EMIF1_A6		ESC_LATCH0	SD2_D2	FSITXA_D1		
GPIO51	EQEP1_B	EMIF1_A11	EPWM15_B		SPIC_POCI	SD1_C2	EMIF1_A7		ESC_LATCH1	SD2_D3	FSITXA_CLK		

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Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO52	EQEP1_STROBE	EMIF1_A12	EPWM16_A		SPIC_CLK	SD1_D3	EMIF1_A8		ESC_MDIO_CLK	SD2_D4	FSIRXA_D0		
GPIO53	EQEP1_INDEX	EMIF1_D31			SPIC_PTE	SD1_C3	EMIF1_A9		ESC_MDIO_DATA	SD1_C1	FSIRXA_D1		
GPIO54	SPIA_PICO	EMIF1_D30		EQEP2_A	SCIB_TX	SD1_D4	EMIF1_A10		ESC_PHY_CLK	SD1_C2	FSIRXA_CLK		
GPIO55	SPIA_POCI	EMIF1_D29	EPWM16_B	EQEP2_B	SCIB_RX	SD1_C4	EMIF1_D0		ESC_PHY0_LINKSTATUS	SD1_C3	FSITXB_D0		
GPIO56	SPIA_CLK	EMIF1_D28	EPWM17_A	EQEP2_STROBE		SD2_D1	EMIF1_D1	I2CA_SDA	ESC_TX0_ENA	SD1_C4	FSITXB_CLK		
GPIO57	SPIA_PTE	EMIF1_D27	EPWM17_B	EQEP2_INDEX		SD2_C1	EMIF1_D2	I2CA_SCL	ESC_TX0_CLK	SD3_D3	FSITXB_D1		
GPIO58	SPIA_PICO	EMIF1_D26	EPWM8_A	OUTPUTXBAR1	SPIB_CLK	SD2_D2	EMIF1_D3	ESC_LED_LINK0_ACTIVE	CANA_RX	SD2_C2	FSIRXB_D0	SPIA_PICO	
GPIO59	EPWM5_A	EMIF1_D25	EPWM8_B	OUTPUTXBAR2	SPIB_PTE	SD2_C2	EMIF1_D4	ESC_LED_LINK1_ACTIVE	CANA_TX	SD2_C3	FSIRXB_D1	SPIA_POCI	
GPIO60	EPWM3_B	EMIF1_D24	ESC_LATCH0	OUTPUTXBAR3	SPIB_PICO	SD2_D3	EMIF1_D5	ESC_LED_ERR		SD2_C4	FSIRXB_CLK	SPIA_CLK	
GPIO61	EPWM17_B	EMIF1_D23	ESC_LATCH1	OUTPUTXBAR4	SPIB_POCI	SD2_C3	EMIF1_D6	ESC_LED_RUN			CANA_RX	SPIA_PTE	
GPIO62	SCIA_RX	EMIF1_D22	ESC_MDIO_CLK	EQEP3_A	CANA_RX	SD2_D4	EMIF1_D7	ESC_LED_STATE_RUN			CANA_TX		
GPIO63	SCIA_TX	EMIF1_D21	EPWM9_A	EQEP3_B	CANA_TX	SD2_C4	EMIF1_RNW	EMIF1_BA0		SD1_D1	ESC_RX1_DATA0	SPIB_PICO	
GPIO64		EMIF1_D20	EPWM9_B	EQEP3_STROBE	SCIA_RX		EMIF1_WAIT	EMIF1_BA1		SD1_C1	ESC_RX1_DATA1	SPIB_POCI	
GPIO65		EMIF1_D19	EPWM10_A	EQEP3_INDEX	SCIA_TX		EMIF1_WEn		FSITXB_CLK	SD1_D2	ESC_RX1_DATA2	SPIB_CLK	
GPIO66	EQEP6_B	EMIF1_D18	EPWM10_B		I2CB_SDA		EMIF1_OEn		FSITXB_D1	SD1_C2	ESC_RX1_DATA3	SPIB_PTE	
GPIO67		EMIF1_D17	EPWM17_A	LINB_TX					ESC_I2C_SDA	SD1_D3			
GPIO68		EMIF1_D16	EPWM17_B	LINB_RX					ESC_I2C_SCL	SD1_C3	ESC_PHY1_LINKSTATUS		
GPIO69		EMIF1_D15	EPWM11_A		I2CB_SCL				FSITXB_D0	SD1_D4	ESC_RX1_CLK	SPIC_PICO	
GPIO70		EMIF1_D14	EPWM11_B	CANA_RX	SCIB_TX	UARTB_TX	MCANA_RX		FSIRXB_D0	SD1_C4	ESC_RX1_DV	SPIC_POCI	
GPIO71		EMIF1_D13	EPWM12_A	CANA_TX	SCIB_RX	UARTB_RX	MCANA_TX			SD3_D1	ESC_RX1_ERR	SPIC_CLK	
GPIO72	EQEP6_STROBE	EMIF1_D12	EPWM12_B	OUTPUTXBAR8	UARTA_TX		MCANB_RX			SD3_C1	ESC_TX1_DATA3	SPIC_PTE	
GPIO73	EQEP6_INDEX	EMIF1_D11	XCLKOUT	OUTPUTXBAR6	UARTA_RX	EPWM5_B	MCANB_TX	SD4_D4		SD2_D2	ESC_TX1_DATA2		
GPIO74	EPWM8_A	EMIF1_D10			EQEP5_A		MCANA_TX	SD1_D4		SD2_C2	ESC_TX1_DATA1		
GPIO75	EPWM8_B	EMIF1_D9			EQEP5_B	SPID_CLK	MCANA_RX	CLB_OUTPUTXBAR8		SD2_D3	ESC_TX1_DATA0		
GPIO76	EPWM9_A	EMIF1_D8			EQEP5_STROBE	SD3_C1		SD4_D4		SD2_C3	ESC_PHY_RESETn		
GPIO77	EPWM9_B	EMIF1_D7			EQEP5_INDEX	SD3_D1		SD1_D4		SD2_D4	ESC_RX0_CLK		
GPIO78	EPWM10_A	EMIF1_D6			EQEP2_A	SD3_C2		SD4_D4		SD2_C4	ESC_RX0_DV		
GPIO79	EPWM10_B	EMIF1_D5		ERRORSTS	EQEP2_B	SD3_D2				SD2_D1	ESC_RX0_ERR		
GPIO80	EPWM11_A	EMIF1_D4		ERRORSTS	EQEP2_STROBE	SD3_C3		SD1_D4		SD2_C1	ESC_RX0_DATA0		

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO81	EPWM11_B	EMIF1_D3			EQEP2_INDEX	SD3_D3					ESC_RX0_DATA1		
GPIO82	EPWM12_A	EMIF1_D2								SD3_C2	ESC_RX0_DATA2		
GPIO83	EPWM12_B	EMIF1_D1								SD3_D2	ESC_RX0_DATA3		
GPIO84	EPWM12_B	EMIF1_D1	EMIF1_CS4n	SCIA_TX	EQEP6_A		SD3_D2		UARTA_TX	SD3_C2	ESC_TX0_ENA	ESC_RX0_DATA3	
GPIO85	EPWM13_A	EMIF1_D0		SCIA_RX	EQEP6_B	SD3_D1			UARTA_RX	SD3_D3	ESC_TX0_CLK	EMIF1_DQM2	
GPIO86	EPWM13_B	EMIF1_A13	EMIF1_CAS	SCIB_TX	EQEP6_STROBE					SD3_C3	ESC_PHY0_LINKSTATUS		
GPIO87	EPWM14_A	EMIF1_A14	EMIF1_RAS	SCIB_RX	EQEP6_INDEX		EMIF1_DQM3			SD3_D4	ESC_TX0_DATA0		
GPIO88	EPWM14_B	EMIF1_A15	EMIF1_DQM0				EMIF1_DQM1			SD3_C4	ESC_TX0_DATA1		
GPIO89	EPWM15_A	EMIF1_A16	EMIF1_DQM1			SD1_D3	EMIF1_CAS			SD4_D1	ESC_TX0_DATA2	SPID_PTE	
GPIO90	EPWM15_B	EMIF1_A17	EMIF1_DQM2			SD1_C3	EMIF1_RAS			SD4_C1	ESC_TX0_DATA3	SPID_CLK	
GPIO91	EPWM16_A	EMIF1_A18	EMIF1_DQM3		I2CA_SDA	SD4_D2	EMIF1_DQM2	PMBUSA_SCL			CLB_OUTPUTXBAR1	SPID_PICO	
GPIO92	EPWM16_B	EMIF1_A19	EMIF1_BA1		I2CA_SCL	SD4_C2	EMIF1_DQM0	PMBUSA_SDA	FSIRXD_CLK		CLB_OUTPUTXBAR2	SPID_POCI	
GPIO93	EPWM17_A		EMIF1_BA0			SD4_D3		PMBUSA_ALERT	ESC_TX1_CLK		CLB_OUTPUTXBAR3	SPID_CLK	
GPIO94	EPWM17_B					SD4_C3	EMIF1_BA1	PMBUSA_CTL	ESC_TX1_ENA		CLB_OUTPUTXBAR4	SPID_PTE	
GPIO95	EPWM18_A	EQEP4_A			SD1_D1			ESC_GPO10			CLB_OUTPUTXBAR5		
GPIO96	EPWM18_B	EQEP4_B		EQEP1_A	SD1_C1			ESC_GPO11			CLB_OUTPUTXBAR6		
GPIO97		EQEP4_STROBE		EQEP1_B	SD1_D2			ESC_GPI17			CLB_OUTPUTXBAR7		
GPIO98		EQEP4_INDEX		EQEP1_STROBE	SD1_C2			ESC_GPI18			CLB_OUTPUTXBAR8		
GPIO99		EMIF1_DQM3	EPWM8_A	EQEP1_INDEX		SD4_D4		ESC_GPI21			EMIF1_D17		
GPIO100	SPIA_PICO	EMIF1_BA1	EPWM9_A	EQEP2_A	SPIC_PICO	SD4_C4	SD1_D1	ESC_GPI0	FSIRXD_D1	FSITXA_D0	EMIF1_D24		
GPIO101	EPWM18_A			EQEP2_B	SPIC_POCI			ESC_GPI1	EMIF1_A5	FSITXA_D1			
GPIO102	EPWM18_B			EQEP2_STROBE	SPIC_CLK			ESC_GPI2	EMIF1_A6	FSITXA_CLK			
GPIO103		EMIF1_BA0	EPWM8_B	EQEP2_INDEX	SPIC_PTE	SD4_C4		ESC_GPI3		FSIRXA_D0			
GPIO104	I2CA_SDA	EPWM18_A		EQEP3_A	SD3_D1			ESC_GPI4		FSIRXA_D1	ESC_SYNC0		
GPIO105	I2CA_SCL	EPWM18_B		EQEP3_B	SD3_C1			ESC_GPI5		FSIRXA_CLK	ESC_SYNC1		
GPIO106	EPWM16_A	EMIF1_A10		EQEP3_STROBE	SD3_D2			ESC_GPI6		FSITXB_D0			
GPIO107	EPWM16_B			EQEP3_INDEX	SD3_C2			ESC_GPI7		FSITXB_D1			
GPIO108	EPWM17_A	EMIF1_A12		EQEP5_A	SD3_D3			ESC_GPI8		FSITXB_CLK			
GPIO109	EPWM17_B	EMIF1_A11		EQEP5_B	SD3_C3			ESC_GPI9					

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Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO110	EMIF1_D31			EQEP5_STROBE	SD3_D4			ESC_GPI10		FSIRXB_D0			
GPIO111	EMIF1_D30			EQEP5_INDEX	SD3_C4			ESC_GPI11		FSIRXB_D1			
GPIO112	EMIF1_D29					SD1_D3		ESC_GPI12		FSIRXB_CLK			
GPIO113	EMIF1_D28					SD1_C3		ESC_GPI13					
GPIO114	EMIF1_D27					SD1_D4		ESC_GPI14					
GPIO115	EMIF1_D26			OUTPUTXBAR5		SD1_C4		ESC_GPI15		FSIRXC_D0			
GPIO116				OUTPUTXBAR6				ESC_GPI16		FSIRXC_D1			
GPIO119	EMIF1_D25			MCANB_TX				ESC_GPI19		FSIRXD_D1			
GPIO120	EMIF1_D24			MCANB_RX				ESC_GPI20		FSIRXD_CLK			
GPIO122	EMIF1_D23				SPIC_PICO	SD1_D1		ESC_GPI22					
GPIO123	EMIF1_D22				SPIC_POCI	SD1_C1		ESC_GPI23					
GPIO124	EMIF1_D21				SPIC_CLK	SD1_D2		ESC_GPI24					
GPIO125	EMIF1_D20				SPIC_PTE	SD1_C2		ESC_GPI25			ESC_LATCH0		
GPIO126	EMIF1_D19				SPID_PICO	SD1_D3		ESC_GPI26			ESC_LATCH1		
GPIO127	EMIF1_D18				SPID_POCI	SD1_C3		ESC_GPI27			ESC_SYNC0		
GPIO128	EMIF1_D17				SPID_CLK	SD1_D4		ESC_GPI28			ESC_SYNC1		
GPIO129	EMIF1_D16				SPID_PTE	SD1_C4		ESC_GPI29			ESC_TX1_ENA		
GPIO130	EPWM13_A					SD2_D1		ESC_GPI30			ESC_TX1_CLK		
GPIO131	EPWM13_B					SD2_C1		ESC_GPI31			ESC_TX1_DATA0		
GPIO132	EPWM14_A					SD2_D2		ESC_GPO0			ESC_TX1_DATA1		
GPIO133	EMIF1_A11	EPWM9_A				SD2_C2			ESC_LED_STATE_RUN				
GPIO134	EPWM14_B					SD2_D3		ESC_GPO1		SD2_C1	ESC_TX1_DATA2		
GPIO141	EPWM15_A				SCIB_TX			ESC_GPO8			ESC_RX1_DATA2		
GPIO142	EPWM15_B				SCIB_RX			ESC_GPO9			ESC_RX1_DATA3		

Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO145	EPWM1_A				MCANB_TX			ESC_GPO12			ESC_LED_ERR		
GPIO146	EPWM1_B				MCANB_RX			ESC_GPO13			ESC_LED_RUN		
GPIO147	EPWM2_A				EQEP5_A			ESC_GPO14			ESC_LED_STATE_RUN		
GPIO148	EPWM2_B				EQEP5_B			ESC_GPO15			ESC_PHY0_LINKSTATUS		
GPIO149	EPWM3_A				EQEP5_STROBE			ESC_GPO16			ESC_PHY1_LINKSTATUS		
GPIO150	EPWM3_B				EQEP5_INDEX			ESC_GPO17			ESC_I2C_SDA		
GPIO151	EPWM4_A				PMBUSA_SCL			ESC_GPO18		FSITXA_D0	ESC_I2C_SCL		
GPIO152	EPWM4_B				PMBUSA_SDA			ESC_GPO19		FSITXA_D1	ESC_MDIO_CLK		
GPIO153	EPWM5_A				PMBUSA_ALERT			ESC_GPO20		FSITXA_CLK	ESC_MDIO_DATA		
GPIO154	EPWM5_B				PMBUSA_CTL			ESC_GPO21		FSIRXA_D0	ESC_PHY_CLK		
GPIO155	EPWM6_A							ESC_GPO22		FSIRXA_D1	ESC_PHY_RESETn		
GPIO156	EPWM6_B							ESC_GPO23		FSIRXA_CLK	ESC_TX0_ENA		
GPIO157	EPWM7_A							ESC_GPO24		FSITXB_D0	ESC_TX0_CLK		
GPIO158	EPWM7_B							ESC_GPO25		FSITXB_D1	ESC_TX0_DATA0		
GPIO159	EPWM8_A							ESC_GPO26		FSITXB_CLK	ESC_TX0_DATA1		
GPIO160	EPWM8_B							ESC_GPO27		FSIRXB_D0	ESC_TX0_DATA2		
GPIO161	EPWM9_A							ESC_GPO28		FSIRXB_D1	ESC_TX0_DATA3		
GPIO162	EPWM9_B							ESC_GPO29		FSIRXB_CLK	ESC_RX0_DV		
GPIO163	EPWM10_A							ESC_GPO30		FSIRXC_D0	ESC_RX0_CLK		
GPIO164	EPWM10_B							ESC_GPO31		FSIRXC_D1	ESC_RX0_ERR		
GPIO165	EPWM11_A									FSIRXC_CLK	ESC_RX0_DATA0		
GPIO166	EPWM11_B									FSIRXD_D0	ESC_RX0_DATA1		
GPIO167	EPWM12_A									FSIRXD_D1	ESC_RX0_DATA2		
GPIO168	EPWM12_B									FSIRXD_CLK	ESC_RX0_DATA3		

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Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO198	EQEP1_A	EPWM9_B	SPIA_PICO								ESC_PDI_UC_IRQ		
GPIO199	EQEP1_STROBE	EPWM17_A	SCIB_TX	EPWM12_A	SPIB_CLK	SD1_D4	MCANA_TX	EMIF1_RAS			SPIC_CLK		
GPIO200	EQEP1_INDEX	EPWM17_B	SCIB_RX	EPWM12_B	SPIB_PTE	SD1_C4	MCANA_RX	EMIF1_CAS	ESC_TX1_DATA1		SPIC_PTE		
GPIO201	OUTPUTXBAR1	EQEP2_A	EPWM18_A	LINB_TX	SPIB_PICO	SD2_D1	PMBUSA_SCL	EMIF1_DQM0	ESC_TX1_DATA2	EPWM13_A			
GPIO202	OUTPUTXBAR2	EQEP2_B	EPWM18_B	LINB_RX	SPIB_POCI	SD2_C1	PMBUSA_SDA	EMIF1_DQM1	ESC_TX1_DATA3	EPWM13_B	FSITXA_D1		
GPIO203	OUTPUTXBAR3	EQEP2_INDEX	SPIA_POCI	OUTPUTXBAR3	SPIB_CLK	SD3_D1	PMBUSA_ALERT	EMIF1_DQM2	ESC_MDIO_CLK	EPWM14_A	FSITXA_D0	EPWM8_B	
GPIO204	OUTPUTXBAR4	EQEP2_STROBE	SPIA_CLK	OUTPUTXBAR4	SPIB_PTE	SD2_C2	PMBUSA_CTL	EMIF1_DQM3	ESC_MDIO_DATA	EPWM14_B	FSITXA_CLK	SD1_D3	
GPIO205	EQEP1_INDEX	EPWM10_A	SPIA_PTE						OUTPUTXBAR1			SD1_C3	
GPIO206	EMIF1_A11	EPWM10_B	EMIF1_WEn						OUTPUTXBAR2		ESC_PHY_CLK	ESC_LED_STATE_RUN	
GPIO207	EQEP2_A	EPWM11_A	EXTSYNCOUT	CANA_TX	SD4_D1	SCIA_RX	LINA_RX	I2CB_SCL	OUTPUTXBAR3		ESC_RX1_CLK	PMBUSA_ALERT	
GPIO208	EQEP2_B	EPWM11_B	EMIF1_D13	SPIB_PICO	SD4_C1	SCIA_TX			OUTPUTXBAR4		ESC_RX1_DV	PMBUSA_CTL	
GPIO209	EQEP2_STROBE	EPWM12_A	EMIF1_D14	SPIB_POCI	SD4_D2	EPWM12_B		LINB_RX	OUTPUTXBAR5		ESC_RX1_ERR	PMBUSA_SDA	
GPIO210	EQEP2_INDEX	EPWM12_B	EMIF1_D15		SD4_C2			LINB_TX	OUTPUTXBAR6		ESC_RX0_DATA2	PMBUSA_SCL	
GPIO211	EQEP6_A	EPWM14_A			SD4_D3				OUTPUTXBAR7		ESC_LED_LINK0_ACTIVE		
GPIO212	EQEP6_B	EPWM14_B			SD4_C3						ESC_LED_LINK1_ACTIVE		
GPIO213	EQEP6_STROBE	EPWM8_A			SD4_D4			LINB_TX			ESC_LED_ERR		
GPIO214	CANA_RX	EMIF1_CLK	MCANA_RX	OUTPUTXBAR7	EQEP3_STROBE	SD2_D4	EMIF1_CS4n	ESC_LATCH1	ESC_I2C_SCL	EPWM16_A	ESC_SYNC1	SPID_PICO	
GPIO215	SCIA_RX	EMIF1_CS4n	CANA_RX	OUTPUTXBAR5	EQEP3_A	SD2_D3	EMIF1_CS2n	I2CB_SDA	SPIC_POCI	EPWM15_A	LINA_TX	EMIF1_D12	
GPIO216	SCIA_TX	EMIF1_SDCKE	SPID_CLK	OUTPUTXBAR6	EQEP3_B	SD2_C3	EMIF1_CS3n	ESC_LATCH0	ESC_I2C_SDA	EPWM15_B	ESC_SYNC0	EMIF1_D13	
GPIO217	CANA_TX	EMIF1_WEn	MCANA_TX	OUTPUTXBAR8	EQEP3_INDEX	SD2_C4	EMIF1_RNW	I2CA_SDA	SPID_PTE	EPWM16_B	LINB_TX	SPID_POCI	
GPIO218	I2CA_SDA	EMIF1_CS0n	SPIA_PICO	EQEP4_A	LINB_TX	CLB_OUTPUTXBAR1	EMIF1_OEn	I2CA_SCL				SPID_CLK	
GPIO219	EQEP6_INDEX	EPWM8_B			SD4_C4						ESC_LED_RUN		
GPIO220		EPWM6_A	SPID_POCI	OUTPUTXBAR2	SCIB_TX	MCANA_TX						PMBUSA_ALERT	X1
GPIO221		EPWM6_B	SPID_PTE	OUTPUTXBAR3	SCIB_RX	MCANA_RX						PMBUSA_CTL	X2

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Table 5-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO222	TDI	EPWM7_A	SPIA_PICO	OUTPUTXBAR4	SCIA_RX	UARTB_TX	I2CA_SDA	SPIC_CLK			ESC_PDI_UC_IRQ	PMBUSA_SDA	
GPIO223	TDO	EPWM7_B	EMIF1_A11	OUTPUTXBAR5	SCIA_TX	UARTB_RX	I2CA_SCL	SPIC_PTE				PMBUSA_SCL	
GPIO224	ERRORSTS	EMIF1_SDCKE	XCLKOUT	OUTPUTXBAR1						SD2_C1	ESC_PDI_UC_IRQ		
AIO225													
AIO226													
AIO227													
AIO228													
AIO229													
AIO230													
AIO231													
AIO232													
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AIO241													
AIO242													

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5.5.2 USB Pin Muxing

Table 5-8 lists assignments of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 5-8. Alternate USB Function

GPIO	GPBAMSEL SETTING	USB FUNCTION
GPIO42	GPBAMSEL[10] = 1b	USB0DM
GPIO43	GPBAMSEL[11] = 1b	USB0DP

5.5.3 High-Speed SPI Pin Muxing

The SPI module on this device has a high-speed mode. To achieve the highest possible speed, a special GPIO configuration is used on a single GPIO mux option for each SPI. These GPIOs may also be used by the SPI when not in high-speed mode (HS_MODE = 0).

To select the mux options that enable the SPI high-speed mode, configure the GPyGMUX and GPyMUX registers as shown in Table 5-9.

Table 5-9. GPIO Configuration for High-Speed SPI

GPIO	SPI SIGNAL	MUX CONFIGURATION	
SPIA			
GPIO58	SPIA_PICO	GPBGMUX2[21:20]=11b	GPBMUX2[21:20]=11b
GPIO59	SPIA_POCI	GPBGMUX2[23:22]=11b	GPBMUX2[23:22]=11b
GPIO60	SPIA_CLK	GPBGMUX2[25:24]=11b	GPBMUX2[25:24]=11b
GPIO61	$\overline{\text{SPIA\_PTE}}$	GPBGMUX2[27:26]=11b	GPBMUX2[27:26]=11b
SPIB			
GPIO63	SPIB_PICO	GPBGMUX2[31:30]=11b	GPBMUX2[31:30]=11b
GPIO64	SPIB_POCI	GPCGMUX1[1:0]=11b	GPCMUX1[1:0]=11b
GPIO65	SPIB_CLK	GPCGMUX1[3:2]=11b	GPCMUX1[3:2]=11b
GPIO66	$\overline{\text{SPIB\_PTE}}$	GPCGMUX1[5:4]=11b	GPCMUX1[5:4]=11b
SPIC			
GPIO69	SPIC_PICO	GPCGMUX1[11:10]=11b	GPCMUX1[11:10]=11b
GPIO70	SPIC_POCI	GPCGMUX1[13:12]=11b	GPCMUX1[13:12]=11b
GPIO71	SPIC_CLK	GPCGMUX1[15:14]=11b	GPCMUX1[15:14]=11b
GPIO72	$\overline{\text{SPIC\_PTE}}$	GPCGMUX1[17:16]=11b	GPCMUX1[17:16]=11b
SPID			
GPIO91	SPID_PICO	GPCGMUX2[23:22]=11b	GPCMUX2[23:22]=11b
GPIO92	SPID_POCI	GPCGMUX2[25:24]=11b	GPCMUX2[25:24]=11b
GPIO93	SPID_CLK	GPCGMUX2[27:26]=11b	GPCMUX2[27:26]=11b
GPIO94	$\overline{\text{SPID\_PTE}}$	GPCGMUX2[29:28]=11b	GPCMUX2[29:28]=11b

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 5-10 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 5-10, any are acceptable. Pins not listed in Table 5-10 must be connected according to the Pin Attributes table.

Table 5-10. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
Analog	
VREFHIx	Tie to VDDA
VREFLOx	Tie to VSSA
ADCINx (except DAC pins)	• No Connect • Tie to VSSA
ADCINx (DAC pins)	• No Connect • Pulldown to VSSA through 5-kΩ resistor
Digital	
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
X1	Tie to VSS
X2	No Connect
TCK	• No Connect • Pullup resistor
TDI	• No Connect • Pullup resistor
TDO	No Connect
TMS	No Connect
ERRORSTS	No Connect
Power and Ground	
VDD	All VDD pins must be connected per the Pin Attributes table.
VDDA	If a dedicated analog supply is not used, tie to VDDIO.
VDDIO	All VDDIO pins must be connected per the Pin Attributes table.
VDD3VFL	Must be tied to VDDIO
VDDOSC	Must be tied to VDDIO
VSS	All VSS pins must be connected to board ground.
VSSA	If a dedicated analog ground is not used, tie to VSS.
VSSOSC	If an external crystal is not used, this pin may be connected to the board ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage	VDDIO with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital/analog input (per pin), I_{IK} (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)[4]	–20	20	mA
	Total for all inputs, $I_{IKTOTAL}$ (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Free-Air temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature[3]	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(4) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.

6.2 ESD Ratings – Commercial

				VALUE	UNIT
F28P650DK, F28P650DH, F28P650SK, F28P650SH in 256-ball ZEJ package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins	±500	
			Corner balls on 256-ball ZEJ: A1, A16, T1, T16	±750	
F28P650DK, F28P650DH, F28P650SK, F28P650SH in 176-pin PTP package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins	±500	
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	±750	
F28P650DK, F28P650DH, F28P650SK, F28P650SH in 169-ball NMR package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins	±500	
			Corner balls on 169-ball NMR: A1, A13, N1, N13	±750	
F28P650DK, F28P650DH, F28P650SK, F28P650SH in 100-pin PZP package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins	±500	
			Corner pins on 100-pin PZP: 1, 25, 26, 50, 51, 75, 76, 100	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Automotive

				VALUE	UNIT
F28P659DK-Q1 in 256-ball ZEJ package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner balls on 256-ball ZEJ: A1, A16, T1, T16	±750	
F28P659DK-Q1, F28P659SH-Q1 in 176-pin PTP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	±750	
F28P659DK-Q1, F28P659DH-Q1, F28P659SH-Q1 in 100-pin PZP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 100-pin PZP: 1, 25, 26, 50, 51, 75, 76, 100	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, VDDIO and VDDA	Internal BOR enabled[(3)]	$V_{BOR-VDDIO}$(MAX) + $V_{BOR-VDDIO-GB}$ [(2)]	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device supply voltage, VDD		1.14	1.2	1.32	V
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply ramp rate[(4)]				
V_{IN}	Digital input voltage	VSS – 0.3		VDDIO + 0.3	V
	Analog input voltage	VSSA – 0.3		VDDA + 0.3	V
Junction temperature, T_J	S version[(1)]	–40		150	°C
Free-Air temperature, T_A	Q version[(1)] (AEC Q100 qualification)	–40		125	°C

(1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.
(2) See the *Power Management Module (PMM)* section.
(3) Internal BOR is enabled by default.
(4) See the *Power Management Module Operating Conditions* table.

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6.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations.

6.5.1 System Current Consumption VREG Enabled

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING MODE						
I_{DDIO}	CPU1 and CPU2 in lockstep active: VDDIO current consumption during operational usage	This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency.	190	280	370	mA
I_{DDIO}	CPU1 and CPU2 non-lockstep active: VDDIO current consumption during operational usage		180	235	315	mA
I_{DDIO}	Single CPU active: VDDIO current consumption during operational usage		160	190	275	mA
I_{DDA}	Any CPU mode: VDDA current consumption during operational usage		0.1	18.6	22	mA
IDLE MODE						
I_{DDIO}	CPU1 and CPU2 in lockstep active: VDDIO current consumption while device is in Idle mode	- CPU is in IDLE mode - Flash is powered down - XCLKOUT is turned off	65	85	170	mA
I_{DDIO}	CPU1 and CPU2 non-lockstep running: VDDIO current consumption while device is in Idle mode		55	80	165	mA
I_{DDIO}	Single CPU active: VDDIO current consumption while device is in Idle mode		45	60	155	mA
I_{DDA}	Any CPU mode: VDDA current consumption while device is in Idle mode		0.001	0.002	0.01	mA
STANDBY MODE						
I_{DDIO}	CPU1 and CPU2 in lockstep active: VDDIO current consumption while device is in Standby mode	- CPU is in STANDBY mode - Flash is powered down - XCLKOUT is turned off	8	25	100	mA
I_{DDIO}	CPU1 and CPU2 non-lockstep active: VDDIO current consumption while device is in Standby mode		8	25	100	mA
I_{DDIO}	Single CPU active: VDDIO current consumption while device is in Standby mode		8	25	100	mA
I_{DDA}	Any CPU mode: VDDA current consumption while device is in Standby mode		0.001	0.002	0.01	mA
HALT MODE						
I_{DDIO}	Any CPU mode: VDDIO current consumption while device is in Halt mode	- CPU is in HALT mode - Flash is powered down - XCLKOUT is turned off	1	8	70	mA
I_{DDA}	Any CPU mode: VDDA current consumption while device is in Halt mode		0.001	0.002	0.01	mA

6.5.1 System Current Consumption VREG Enabled (continued)

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLASH ERASE/PROGRAM						
I_{DDIO}	VDDIO current consumption during Erase/Program cycle(1)	• CPU is running from flash, performing erase and program on the unused sectors. • VREG is enabled. • SYSCLK is running at maximum device speed (PLLENA) • I/Os are inputs with pullups enabled. • Peripheral clocks are turned OFF.	100	190	275	mA
I_{DDA}	VDDA current consumption during Erase/Program cycle		0.001	0.002	0.01	mA
RESET MODE						
I_{DDIO}	VDDIO current consumption while reset is active(2)		1	13	20	mA
I_{DDA}	VDDA current consumption while reset is active(2)		0.001	0.002	0.01	mA

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
(2) This is the current consumption while reset is active, that is XRSn is low.

6.5.2 System Current Consumption VREG Disable - External Supply

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING MODE						
I_{DD}	CPU1 and CPU2 in lockstep mode active: VDD current consumption during operational usage	This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency.	210	330	400	mA
I_{DD}	CPU1 and CPU2 non-lockstep active: VDD current consumption during operational usage		200	270	340	mA
I_{DD}	Single CPU active: VDD current consumption during operational usage		190	230	300	mA
I_{DDIO}	Any CPU mode: VDDIO current consumption during operational usage		0.1	4.2	5	mA
I_{DDA}	Any CPU mode: VDDA current consumption during operational usage		0.1	18.6	22	mA

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6.5.2 System Current Consumption VREG Disable - External Supply (continued)

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDLE MODE						
I_{DD}	CPU1 and CPU2 in lockstep mode active: VDD current consumption while device is in Idle mode	• CPU is in IDLE mode • Flash is powered down • XCLKOUT is turned off	70	90	180	mA
I_{DD}	CPU1 and CPU2 non-lockstep active: VDD current consumption while device is in Idle mode		60	85	170	mA
I_{DD}	Single CPU active: VDD current consumption while device is in Idle mode		50	65	160	mA
I_{DDIO}	Any CPU mode: VDDIO current consumption while device is in Idle mode		0.1	4	5	mA
I_{DDA}	Any CPU mode: VDDA current consumption while device is in Idle mode		0.001	0.002	0.01	mA
STANDBY MODE						
I_{DD}	CPU1 and CPU2 in lockstep mode active: VDD current consumption while device is in Standby mode	• CPU is in STANDBY mode • Flash is powered down • XCLKOUT is turned off	8	25	120	mA
I_{DD}	CPU1 and CPU2 non-lockstep active: VDD current consumption while device is in Standby mode		8	25	120	mA
I_{DD}	Single CPU active: VDD current consumption while device is in Standby mode		8	25	120	mA
I_{DDIO}	Any CPU mode: VDDIO current consumption while device is in Standby mode		0.1	4	5	mA
I_{DDA}	Any CPU mode: VDDA current consumption while device is in Standby mode		0.001	0.002	0.01	mA
HALT MODE						
I_{DD}	Any CPU mode: VDD current consumption while device is in Halt mode	• CPU is in HALT mode • Flash is powered down • XCLKOUT is turned off	1	7	70	mA
I_{DDIO}	Any CPU mode: VDDIO current consumption while device is in Halt mode		0.5	3	4	mA
I_{DDA}	Any CPU mode: VDDA current consumption while device is in Halt mode		0.001	0.002	0.01	mA

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6.5.2 System Current Consumption VREG Disable - External Supply (continued)

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLASH ERASE/PROGRAM						
I_{DD}	VDD Current consumption during Erase/Program cycle(1)	• CPU is running from flash, performing erase and program on the unused sectors. • VREG is disabled. • SYSCLK is running at maximum device speed (PLLENA) • I/Os are inputs with pullups enabled. • Peripheral clocks are turned OFF.	100	195	290	mA
I_{DDIO}	VDDIO Current consumption during Erase/Program cycle(1)		0.1	4.2	5	mA
I_{DDA}	VDDA Current consumption during Erase/Program cycle		0.001	0.002	0.01	mA

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

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6.5.3 Operating Mode Test Description

Section 6.5.1 and Section 6.5.5.1 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- CPU1 and CPU2 are operating at 200 MHz.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.5.4 Current Consumption Graphs

There are different device variants of this device with respect to the number of C28x cores. The three variants are single CPU (CPU1), dual CPU with the second CPU operated in non-lockstep mode (CPU1 + CPU2 non LS), and dual CPU with the second CPU operated in lockstep mode (CPU1 + CPU2 LS). Device can also be operated in VREG disabled or enabled mode. This section provides the typical representation of the relationship between frequency, temperature, VREG mode, and current consumption on the device depending on the operating modes. Actual results will vary based on the system implementation and conditions.

Figure 6-1 and Figure 6-2 show the typical operating mode currents across temperature. Figure 6-3 and Figure 6-4 show the typical standby mode currents across temperature. Figure 6-5 and Figure 6-6 show the typical idle mode currents across temperature. Figure 6-7 and Figure 6-8 show the typical halt mode currents across temperature.

Figure 6-9, Figure 6-10, and Figure 6-11 show a typical representation of the relationship of SYSCLK, temperature, and current consumption on the device at nominal supply condition with VREG disabled.

Figure 6-12, Figure 6-13, and Figure 6-14 show a typical representation of the relationship of SYSCLK, temperature, and current consumption on the device at nominal supply condition with VREG enabled.

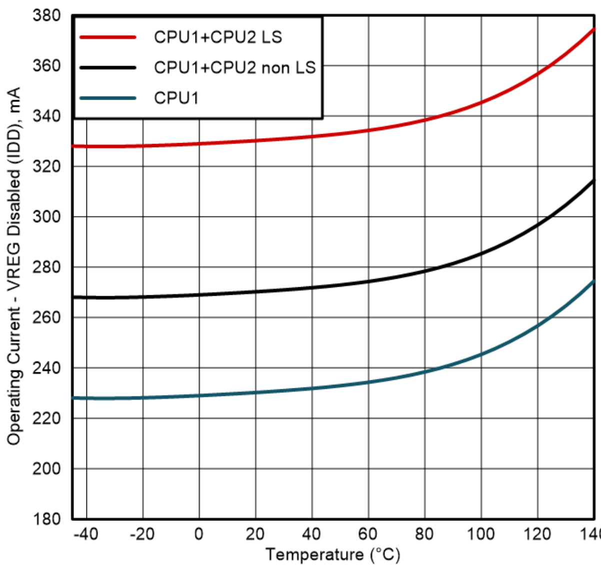

Figure 6-1. Typical Operating Current Versus Temperature - VREG Disabled

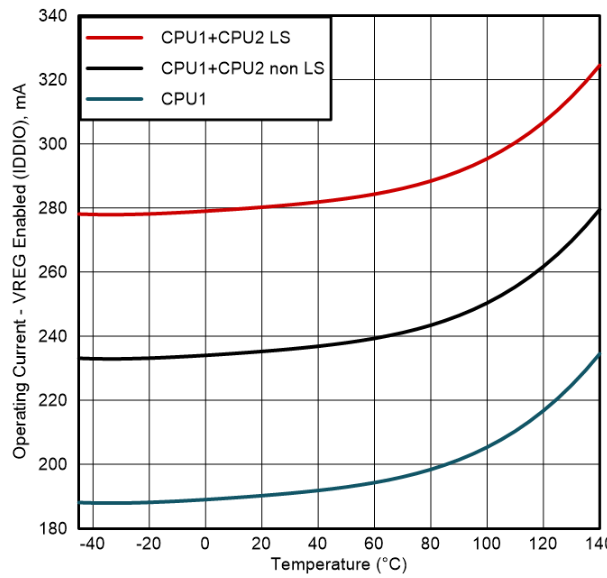

Figure 6-2. Typical Operating Current Versus Temperature - VREG Enabled

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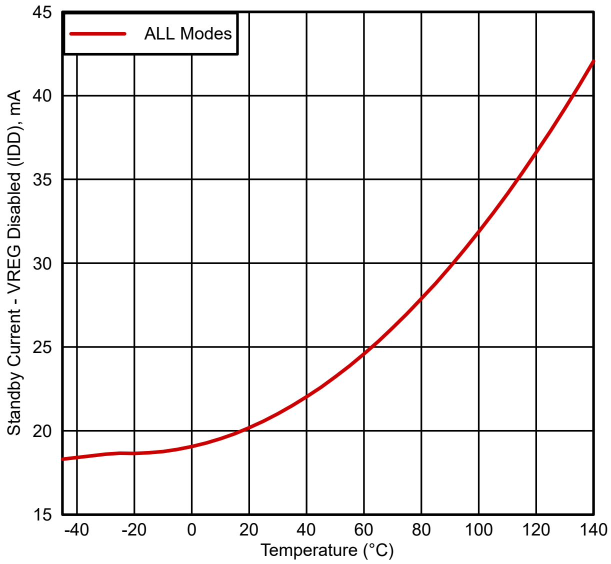

Figure 6-3. Typical Standby Current Versus Temperature - VREG Disabled

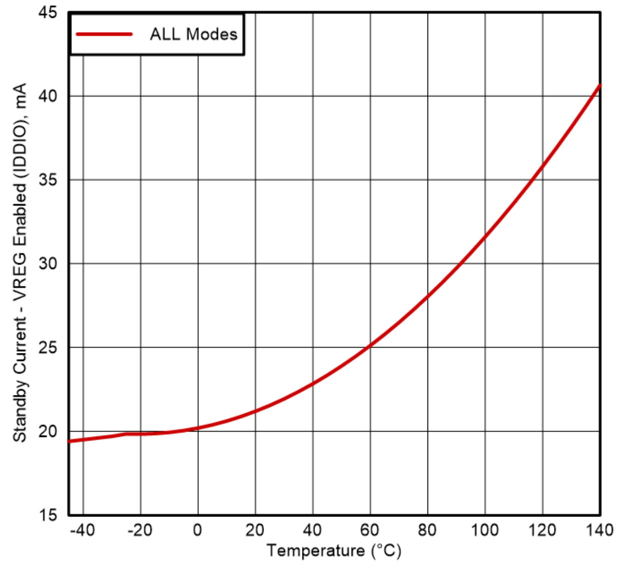

Figure 6-4. Typical Standby Current Versus Temperature - VREG Enabled

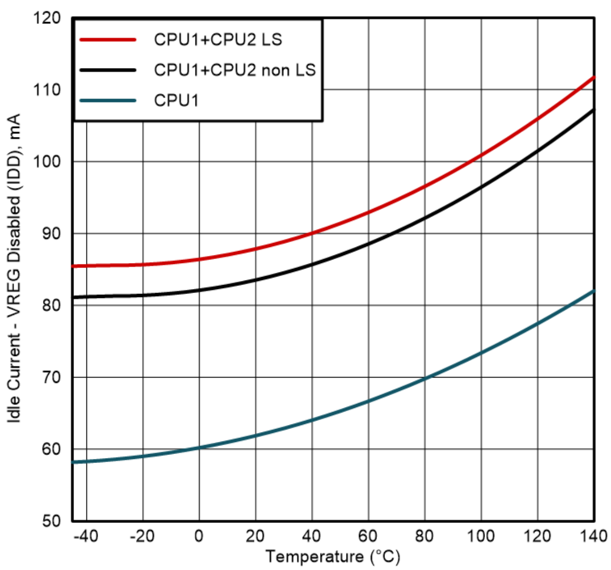

Figure 6-5. Typical Idle Current Versus Temperature - VREG Disabled

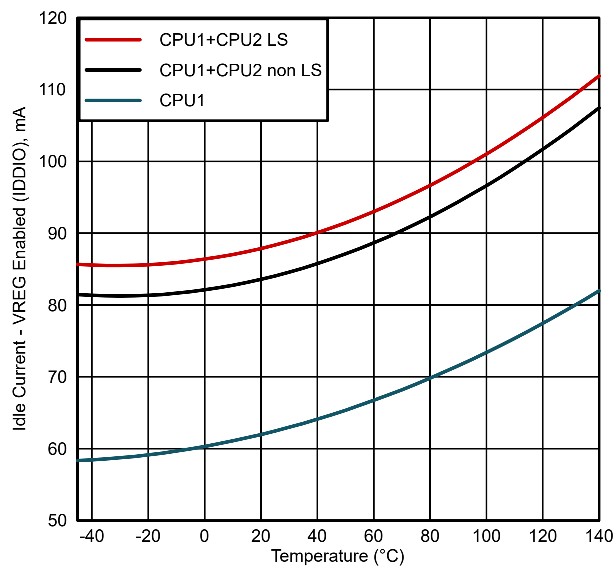

Figure 6-6. Typical Idle Current Versus Temperature - VREG Enabled

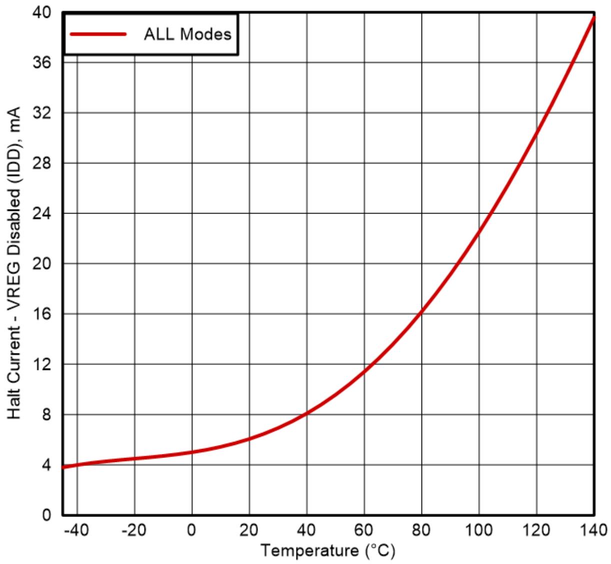

Figure 6-7. Typical Halt Current Versus Temperature - VREG Disabled

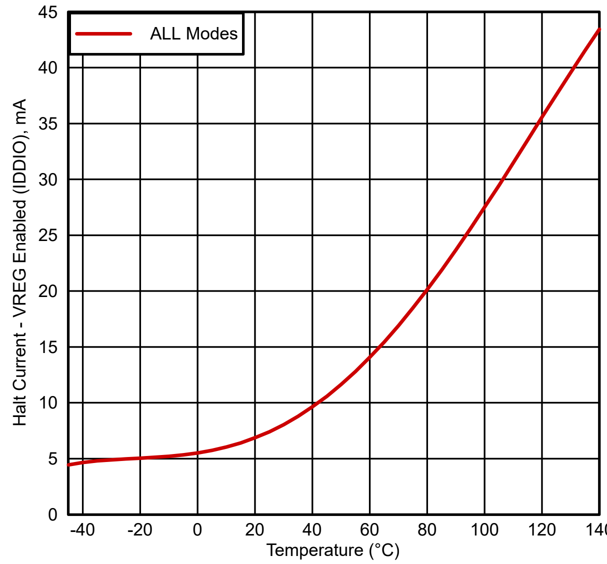

Figure 6-8. Typical Halt Current Versus Temperature - VREG Enabled

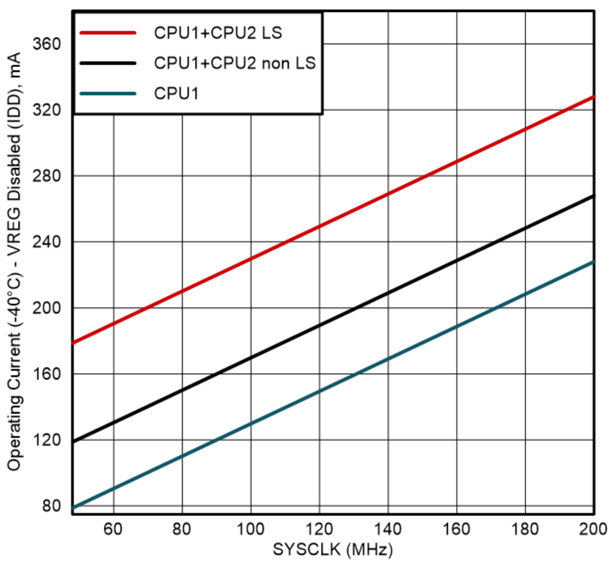

Figure 6-9. Typical Operating Current Versus SYSCLK - VREG Disabled -40°C

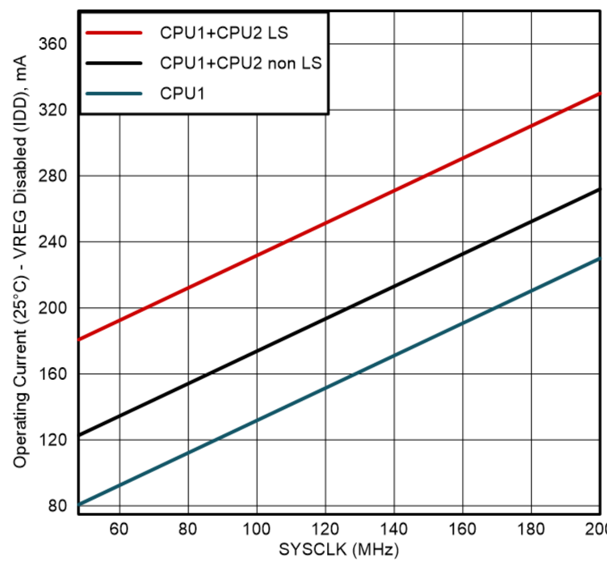

Figure 6-10. Typical Operating Current Versus SYSCLK - VREG Disabled 25°C

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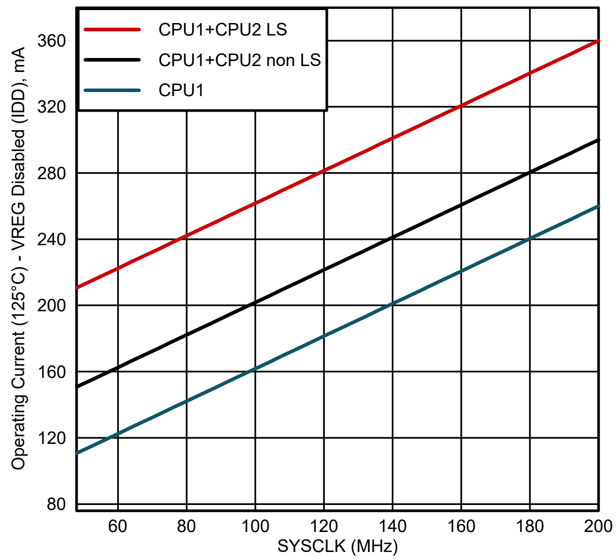

Figure 6-11. Typical Operating Current Versus SYSCLK - VREG Disabled 125°C

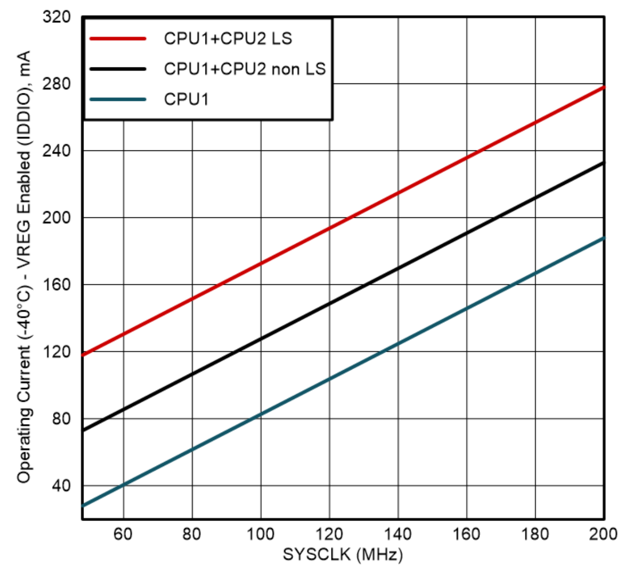

Figure 6-12. Typical Operating Current Versus SYSCLK - VREG Enabled -40°C

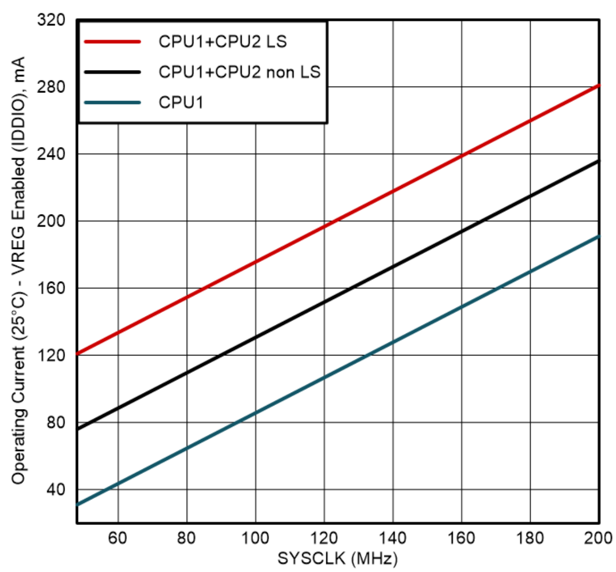

Figure 6-13. Typical Operating Current Versus SYSCLK - VREG Enabled 25°C

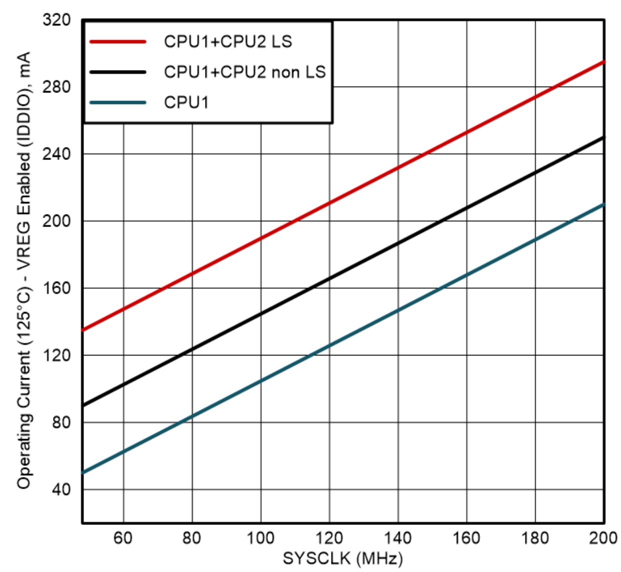

Figure 6-14. Typical Operating Current Versus SYSCLK - VREG Enabled 125°C

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6.5.5 Reducing Current Consumption

The F28P65x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. The Typical Current Reduction per Disabled Peripheral table lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

6.5.5.1 Typical Current Reduction per Disabled Peripheral

PERIPHERAL	I_{DDIO} CURRENT REDUCTION (mA)
ADC(1)	2.90
ADCCHECKER	0.37
AES	0.30
CLA	0.83
CLA BGCRC	0.34
CLB	9.59
CMPSS(1)	8.70
CPU BGCRC	0.52
CPU TIMER	0.17
GPDAC	0.54
DCAN	1.56
DCC	0.38
DMA	1.19
eCAP1 to eCAP5	3.44
eCAP6 and eCAP7(3)	2.38
ePWM1 to ePWM18(4)	25.33
EPG	0.89
ERAD	2.98
eQEP	1.02
ECAT	2.53
FSI RX	2.38
FSI TX	1.31
HRCAL	1.30
I2C	0.89
LIN	1.13
MCAN (CAN-FD)	4.15
MPOST	5.02
PMBUS	0.46
SCI	0.54
SDFM	10.58
SPI	1.47
UART	2.24

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6.5.5.1 Typical Current Reduction per Disabled Peripheral (continued)

PERIPHERAL	I_{DDIO} CURRENT REDUCTION (mA)
USB	3.61

(1) This current represents the current drawn by the digital portion of the each module.
(2) eCAP6 and eCAP7 can also be configured as HRCAP.
(3) ePWM1 to ePWM18 can also be configured as HRPWM.

6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}$ MIN	VDDIO * 0.8			V
			I_{OH} = –100 µA	VDDIO – 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}$ MAX			0.4	V
			I_{OL} = 100 µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	High-level output impedance for all output pins				70		Ω
R_{OL}	Low-level output impedance for all output pins				70		Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis			125			mV
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDDIO = 3.3 V V_{IN} = VDDIO		120		µA
I_{PULLUP}	Input current	Digital inputs with pullup enabled(1)	VDDIO = 3.3 V V_{IN} = 0 V		160		µA
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDDIO			0.1	µA
		Analog pins (except ADCINB3/VDAC)	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	
		ADCINB3/VDAC			2	11	
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins(2)					
VREG, POR and BOR							
VREG, POR, BOR(3)							

(1) See the Pins With Internal Pullup and Pulldown table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in *ADC Input Model* section.
(3) See the *Power Management Module (PMM)* section.

6.7 Thermal Resistance Characteristics for ZEJ Package

		°C/W[(1)]
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	8.2
	Junction-to-case thermal resistance, bottom	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	11.3
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	25.6
Psi_{JT}	Junction-to-package top	0.2
Psi_{JB}	Junction-to-board	11.2

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.8 Thermal Resistance Characteristics for PTP Package

		°C/W[(1)]
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	11.2
	Junction-to-case thermal resistance, bottom	0.5
$R\Theta_{JB}$	Junction-to-board thermal resistance	9.8
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	20.4
Psi_{JT}	Junction-to-package top	0.3
Psi_{JB}	Junction-to-board	9.5

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.9 Thermal Resistance Characteristics for NMR Package

		°C/W[(1)]
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	6.9
	Junction-to-case thermal resistance, bottom	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	11.5
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	29.2
Psi_{JT}	Junction-to-package top	0.2
Psi_{JB}	Junction-to-board	11.4

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

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6.10 Thermal Resistance Characteristics for PZP Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	7.0
	Junction-to-case thermal resistance, bottom	0.5
$R\Theta_{JB}$	Junction-to-board thermal resistance	8.0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	21.1
Psi_{JT}	Junction-to-package top	0.1
Psi_{JB}	Junction-to-board	7.8

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.11 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

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6.12 System

6.12.1 Power Management Module (PMM)

6.12.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.12.1.2 Overview

The block diagram of the PMM is shown in Figure 6-15. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

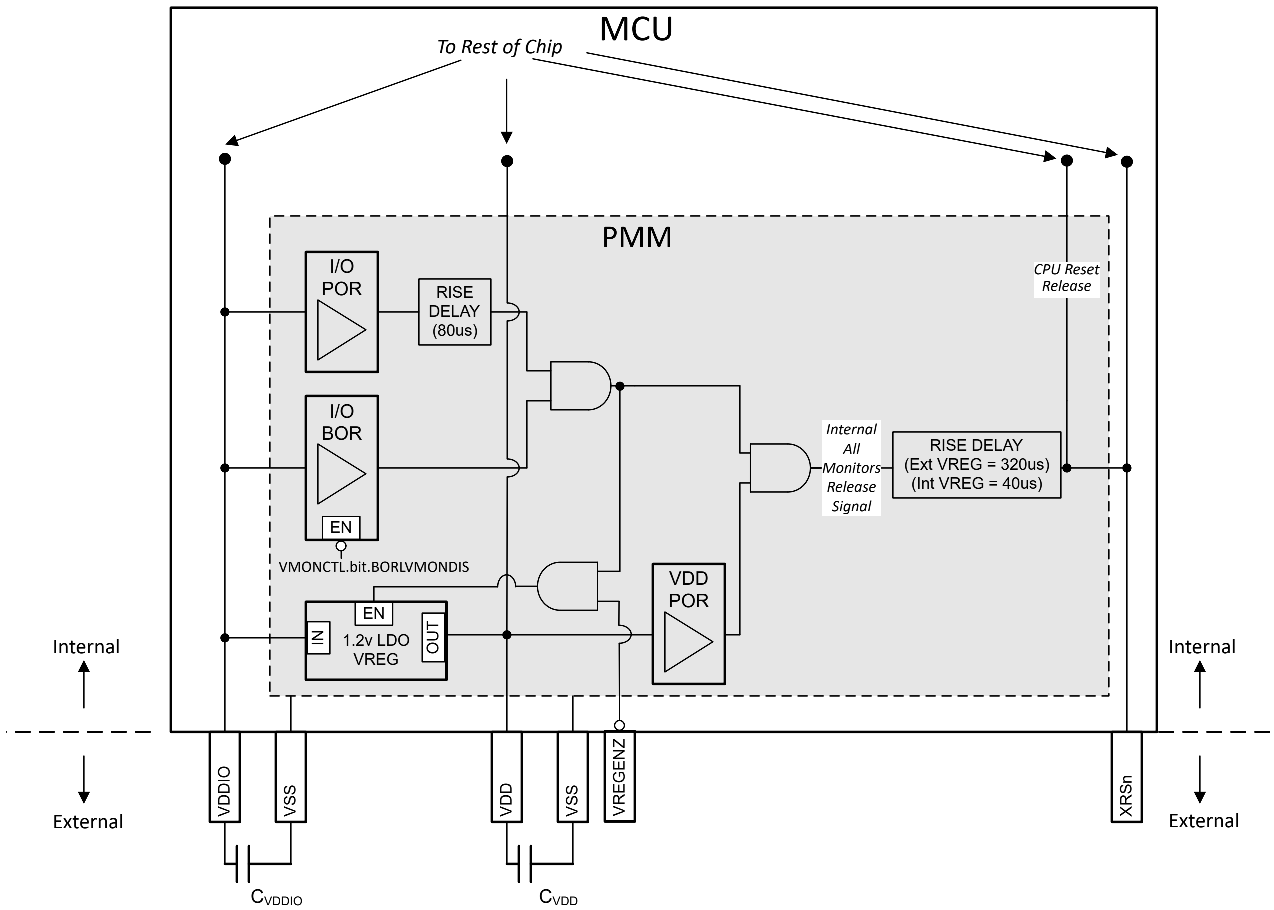

Figure 6-15. PMM Block Diagram

6.12.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

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The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.12.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.12.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-16 shows the operating region of the I/O BOR.

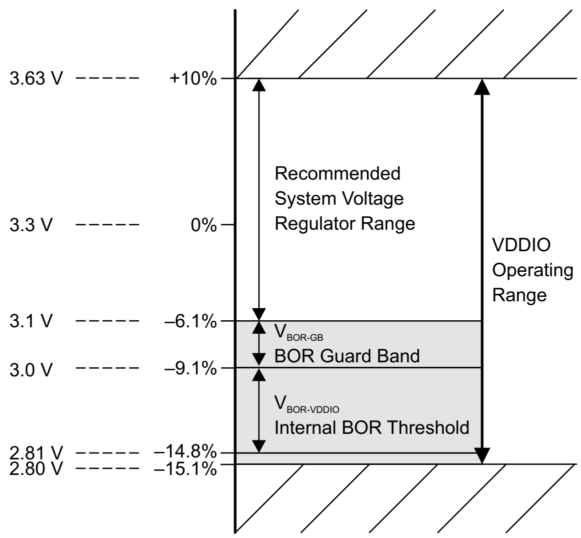

Figure 6-16. I/O BOR Operating Region

6.12.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.12.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.
- VDD supplied from an external supply: The VDD POR is not supported for application use. If VDD monitoring is required by the application, an external supervisor can be used to monitor the VDD rail.

Note

The use of an external supervisor with the internal VREG is not supported.If VDD monitoring is required by the application, a package with a VREGENZ pin must be used to power VDD externally.

6.12.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. These delays are designed to make sure that the voltages are stable when XRSn releases in external VREG mode. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in Power Management Module Electrical Data and Timing for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.12.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. It is enabled by tying the VREGENZ pin low. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.12.1.2.5 VREGENZ

The VREGENZ (VREG disable) pin controls the state of the internal VREG. To enable the internal VREG, connect the VREGENZ pin to a logic low voltage. For applications supplying VDD externally (external VREG), disable the internal VREG by tying the VREGENZ pin high.

6.12.1.3 External Components

6.12.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.12.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in Power Management Module Electrical Data and Timing. The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of C_{VDDIO} * VDDIO pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

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6.12.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in Power Management Module Electrical Data and Timing.

In external VREG mode, the actual amount of decoupling capacitance to use is a requirement of the power supply driving VDD.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL across the VDD pins.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.12.1.4 Power Sequencing

6.12.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In external VREG mode, the VDD pins should be tied together and supplied from a single source.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.12.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI and VDAC). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

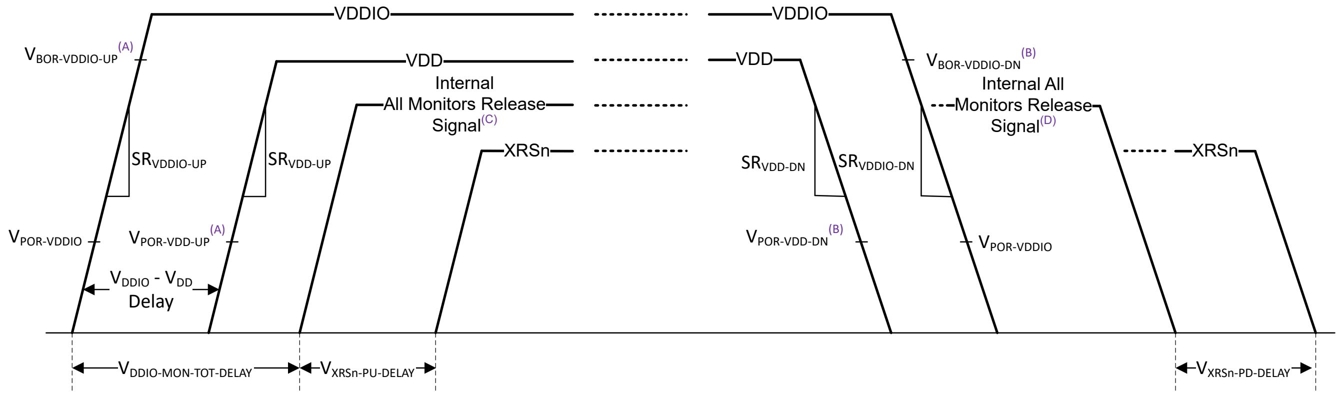
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.12.1.4.3 Supply Pins Power Sequence

6.12.1.4.3.1 External VREG/VDD Mode Sequence

Figure 6-17 depicts the power sequencing requirements for external VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.

B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.

C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.

D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-17. External VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
  2. VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
  3. The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
  4. After the times specified by $V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$ and $V_{XRSN\text{-}PD\text{-}DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  5. The I/O BOR monitor has different release points during power up and power down.
  6. During power up, both VDDIO and VDD rails have to be up before XRSn releases.
- **For Power Down:**
  1. There is no requirement between VDDIO and VDD on which should power down first; however, there is a minimum slew rate specification.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. Any of the POR or BOR monitors that trips during power down will cause XRSn to go low after $V_{XRSN\text{-}PD\text{-}DELAY}$.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

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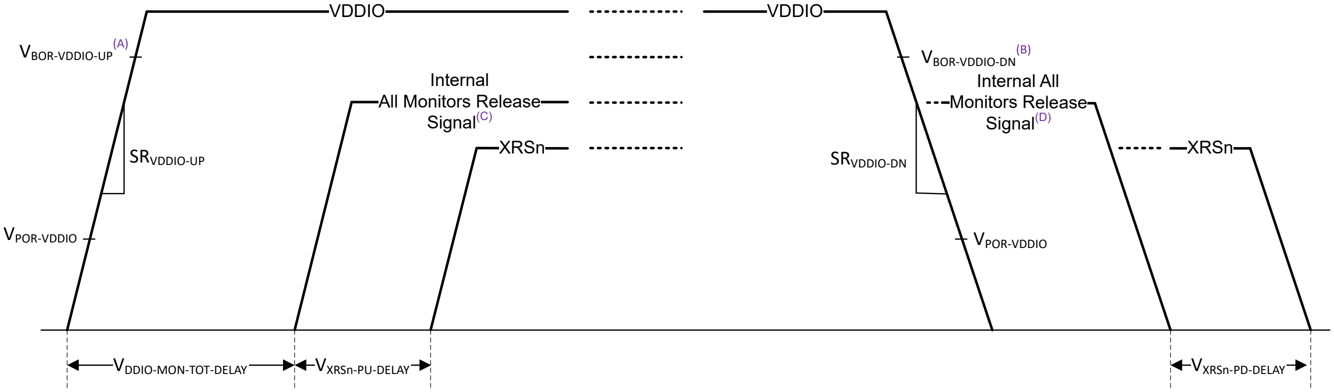
6.12.1.4.3.2 Internal VREG/VDD Mode Sequence

Figure 6-18 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-18. Internal VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
  2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
  3. After the times specified by $V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$ and $V_{XRSN\text{-}PU\text{-}DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  4. The I/O BOR monitor has different release points during power up and power down.
- **For Power Down:**
  1. The only requirement on VDDIO during power down is the slew rate.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSN\text{-}PD\text{-}DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.12.1.4.3.3 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION
Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in Supply Pins Power Sequence is recommended.

Table 6-1. External VREG Sequence Summary

CASE	RAILS POWER-UP ORDER			ACCEPTABLE
	VDDIO	VDDA	VDD	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	-
D	2	3	1	-
E	3	2	1	-
F	3	1	2	-
G	1	1	2	Yes
H	2	2	1	-

Table 6-2. Internal VREG Sequence Summary

CASE	RAILS POWER-UP ORDER		ACCEPTABLE
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	-
C	1	1	Yes

Note
The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.12.1.4.3.4 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note
The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

VDD has a minimum slew rate requirement in external VREG mode. If the minimum slew rate is not met, the VDD POR may release before the VDD operational minimum voltage is met and the device may not start in a properly reset state.

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6.12.1.5 Power Management Module Electrical Data and Timing

6.12.1.5.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
C_{VDDIO} (1) (2)	VDDIO Capacitance Per Pin		0.1			uF
C_{VDDA} (1) (2)	VDDA Capacitance Per Pin		2.2			uF
$V_{BOR\text{-}VDDIO\text{-}GB}$ (5)	VDDIO Brown Out Reset Voltage Guardband			0.1		V
External VREG						
$C_{VDD\ TOTAL}$ (1) (4)	Total VDD Capacitance			10		uF
SR_{VDD33} (3)	Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA)		3		100	mV/us
SR_{VDD12} (3)	Supply Ramp Rate of 1.2V Rail (VDD)		2		100	mV/us
V_{DD33} - V_{DD12} Delay (6)	Ramp Delay Between VDD33 and VDD12		0			us
Internal VREG						
$C_{VDD\ TOTAL}$ (4) (7)	Total VDD Capacitance			10,22		uF
SR_{VDD33} (3)	Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA)		20		100	mV/us
$I_{VREG\text{-}LOAD}$	Voltage Regulator Load Current				500	mA

(1) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
(3) Supply ramp rate faster than the max can trigger the on-chip ESD protection.
(4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
(5) TI recommends $V_{BOR\text{-}VDDIO\text{-}GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR\text{-}VDDIO\text{-}GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(6) Delay between when the 3.3v rail ramps up and when the 1.2v rail ramps up. See the supply sequencing table for the allowable supply ramp sequences.
(7) Typical values can be 10uF or 22uF, with tolerance requirement of +/- 20%

6.12.1.5.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG}	Internal Voltage Regulator Output		1.14	1.2	1.26	V
$V_{VREG\text{-}PU}$	Internal Voltage Regulator Power Up Time				350	us
$V_{VREG\text{-}INRUSH}$ (5)	Internal Voltage Regulator Inrush Current			1150		mA
$V_{POR\text{-}VDDIO}$	VDDIO Power on Reset Voltage	Before and After XRSn Release		2.3		V
$V_{BOR\text{-}VDDIO\text{-}UP}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Up	Before XRSn Release		2.7		V
$V_{BOR\text{-}VDDIO\text{-}DOWN}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Down	After XRSn Release	2.81		3.0	V
$V_{POR\text{-}VDD\text{-}UP}$ (2)	VDD Power on Reset Voltage on Ramp Up	Before XRSn Release		1		V

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6.12.1.5.2 Power Management Module Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{POR\text{-}VDD\text{-}DOWN}$ (2)	VDD Power on Reset Voltage on Ramp Down	After XRSn Release		1		V
$V_{XRSn\text{-}PU\text{-}DELAY}$ (3)	XRSn Release Delay after Supplies are Ramped Up During Power-Up	Internal VREG		40		us
$V_{XRSn\text{-}PU\text{-}DELAY}$ (3)	XRSn Release Delay after Supplies are Ramped Up During Power-Up	External VREG		320		us
$V_{XRSn\text{-}PD\text{-}DELAY}$ (4)	XRSn Trip Delay after Supplies are Ramped Down During Power-Down			2		us
$V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$	Total Delays in Path of VDDIO Monitors (POR, BOR)			80		us
$V_{XRSn\text{-}MON\text{-}RELEASE\text{-}DELAY}$	XRSn Release Delay after a VDDIO POR Event	Internal VREG, Supplies Within Operating Range		40		us
	XRSn Release Delay after a VDDIO BOR			40		us
	XRSn Release Delay after a VDDIO POR Event			120		us
	XRSn Release Delay after a VDDIO POR Event	External VREG, Supplies Within Operating Range		360		us
	XRSn Release Delay after a VDDIO BOR			360		us
	XRSn Release Delay after a VDDIO POR Event			440		us

(1) See the *Supply Voltages* figure.
(2) $V_{POR\text{-}VDD}$ is not supported and it is set to trip at a level below the recommended operating conditions. If monitoring of VDD is needed, an external supervisor is required.
(3) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect.
(4) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply.
(5) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

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6.12.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-19 shows the recommended reset circuit.

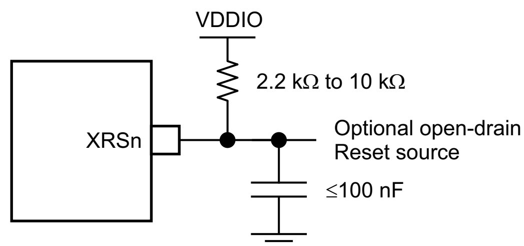

Figure 6-19. Reset Circuit

6.12.2.1 Reset Sources

The Reset Signals table summarizes the various reset signals and their effect on the device.

Table 6-3. Reset Signals

Reset Source	CPU1 Core Reset (C28x, TMU, FPU, VCRC)	CPU1 Peripheral Reset	CPU2 Core Reset (C28x, TMU, FPU, VCRC)	CPU2 and Peripheral Reset	JTAG / Debug Logic Reset	IOs	XRSn Output
POR	Yes	Yes	Yes	Yes	Yes	Hi-Z	Yes
XRSn Pin	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1.SIMRESET.XRSn	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1. $\overline{\text{WDRS}}$	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1. $\overline{\text{NMIWDRS}}$	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1. $\overline{\text{SYSRS}}$ (Debugger Reset)	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1.SIMRESET.CPU1RSn	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1. $\overline{\text{SCCRESET}}$	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1. $\overline{\text{HWBISTRS}}$	Yes	-	-	-	-	-	-
CPU2. $\overline{\text{SYSRS}}$ (Debugger Reset)	-	-	Yes	Yes	-	-	-
CPU2. $\overline{\text{WDRS}}$	-	-	Yes	Yes	-	-	-
CPU2. $\overline{\text{NMIWDRS}}$	-	-	Yes	Yes	-	-	-
CPU2. $\overline{\text{SCCRESET}}$	-	-	Yes	Yes	-	-	-
CPU2. $\overline{\text{HWBISTRS}}$	-	-	Yes	-	-	-	-
ECAT_RESET_OUT	Yes	Yes	Yes	Yes	-	Hi-Z	Yes

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

See the Resets section of the System Control chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

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CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

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6.12.2.2 Reset Electrical Data and Timing

6.12.2.2.1 Reset XRSn Timing Requirements

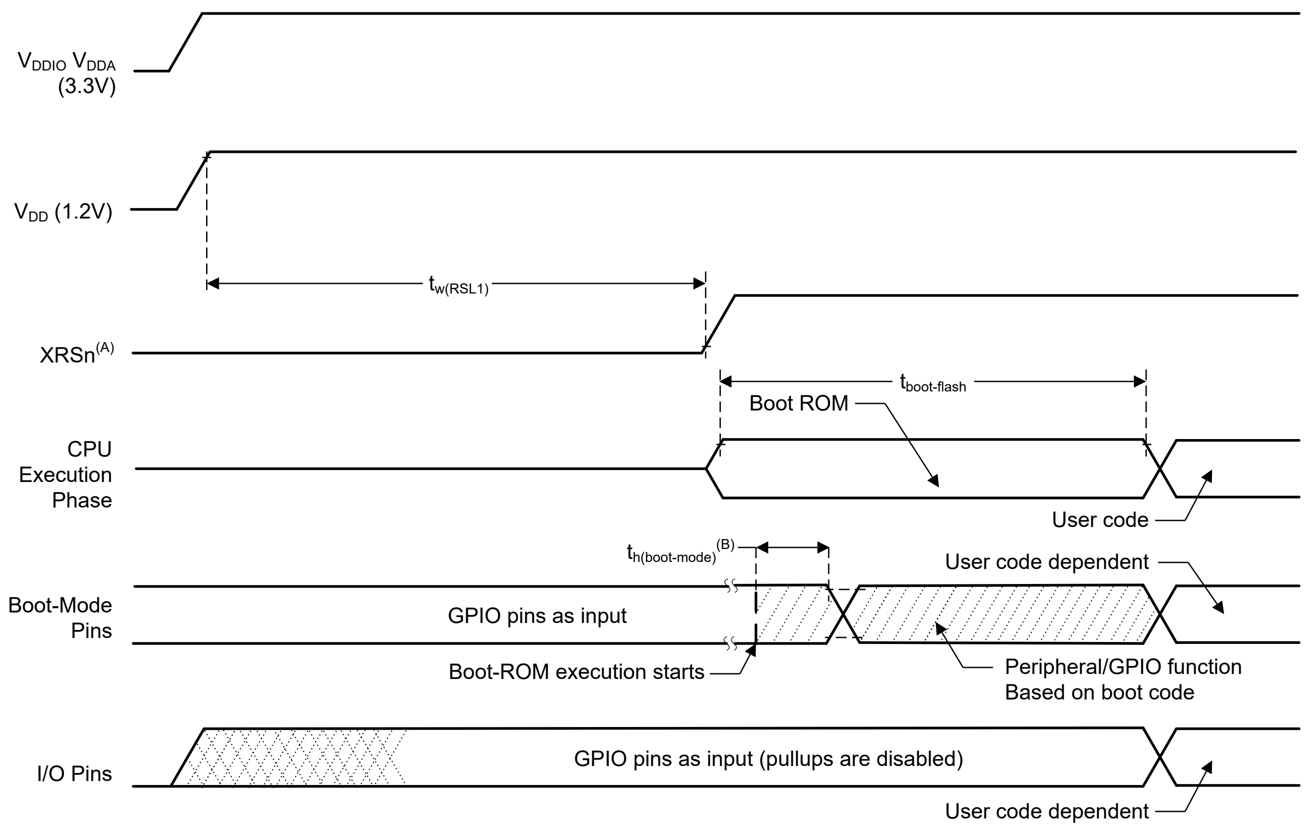
		MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low on warm reset	3.2		µs

6.12.2.2.2 Reset XRSn Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, XRSn driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{boot\text{-}flash}$	Boot-ROM execution time to first instruction fetch in flash			1.2	ms

6.12.2.2.3 Reset Timing Diagrams



A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the Pin Attributes table. On-chip monitors will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see the Reset Sources section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-20. Power-on Reset

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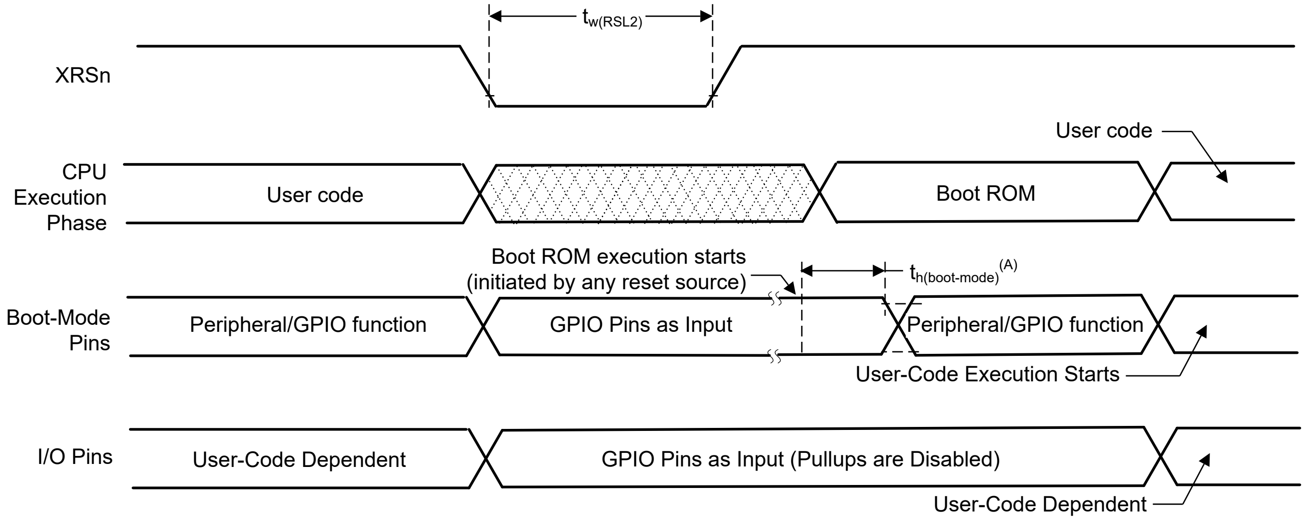

A. After reset from any source (see the Reset Sources section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-21. Warm Reset

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6.12.3 Clock Specifications

6.12.3.1 Clock Sources

Table 6-4. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1	Can be used to provide clock for: • Watchdog block • Main PLL • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.
AUXCLKIN	Can be used to provide clock for: • Auxiliary PLL • CPU-Timer 2	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

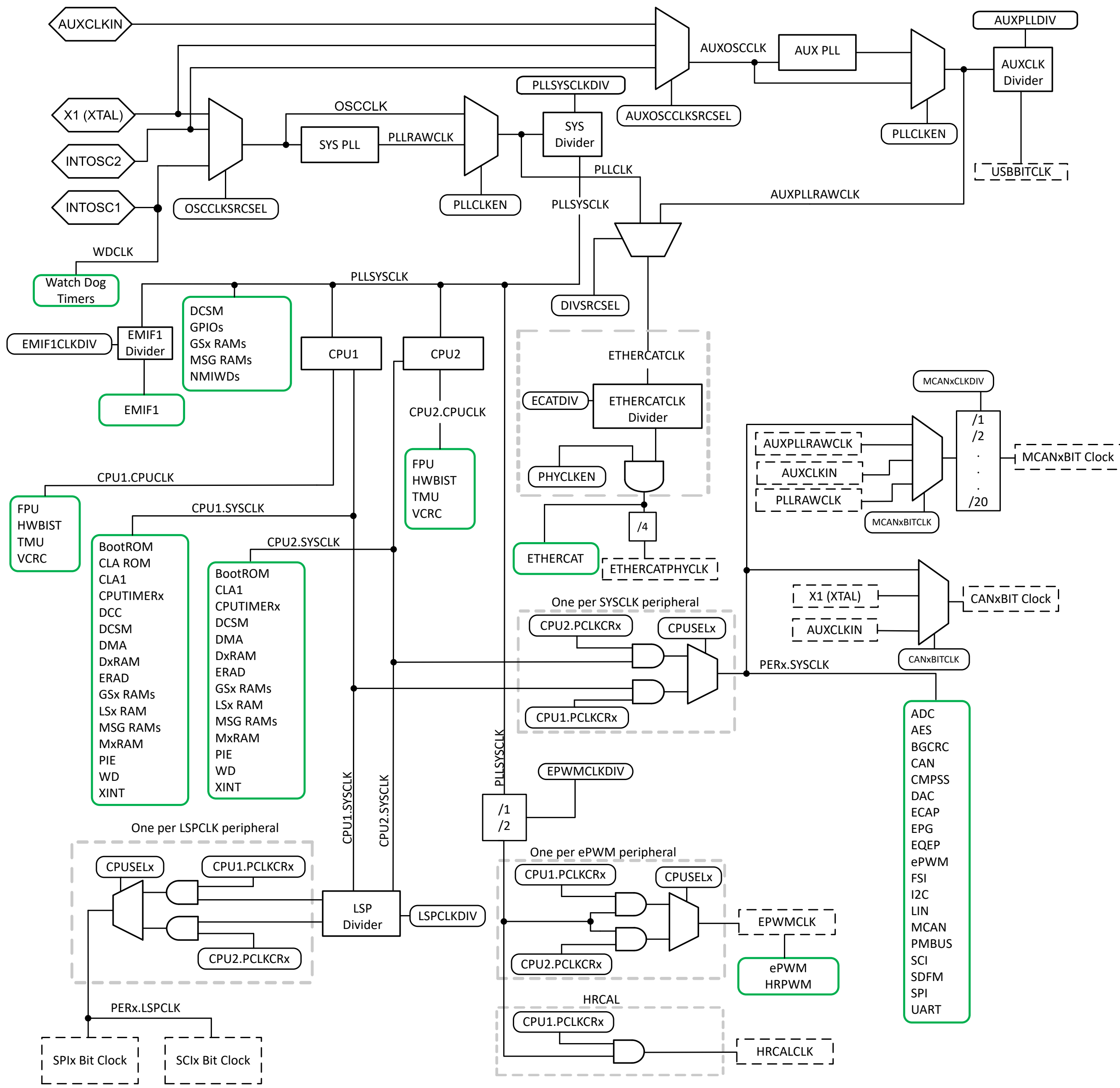

Figure 6-22. Clocking System

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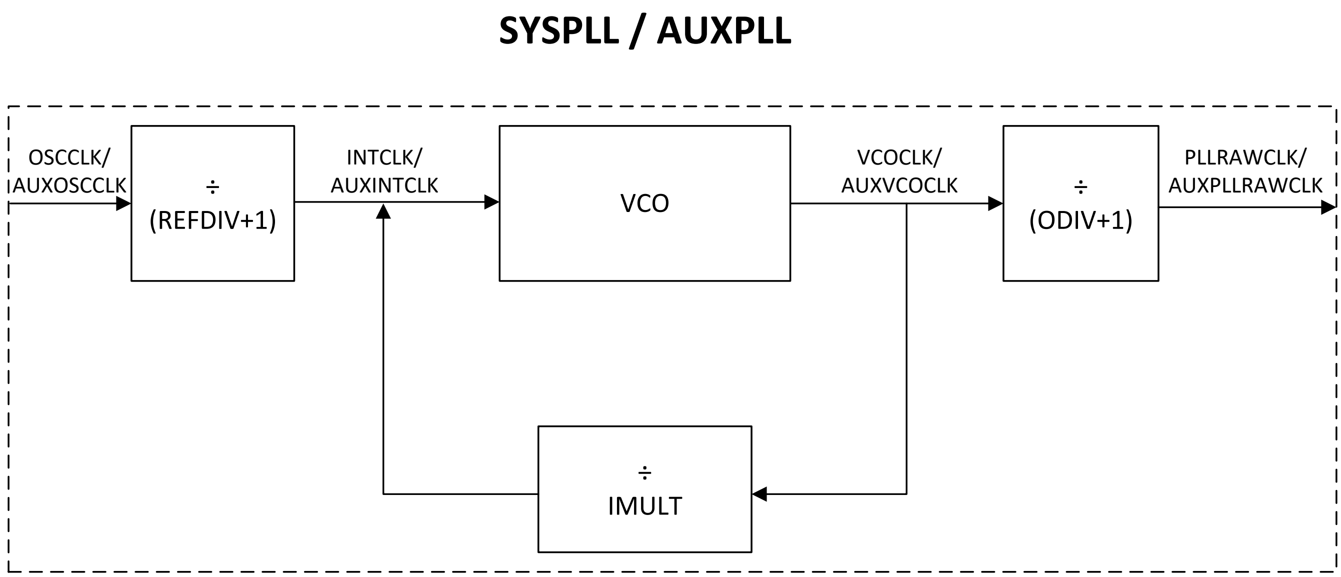

Figure 6-23. SYSPLL/AUXPLL

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REFDIV + 1)} \times \frac{IMULT}{(ODIV + 1)} \quad (1)$$

In the *SYSPLL/AUXPLL* figure,

$$f_{\text{AUXPLLRAWCLK}} = \frac{f_{\text{AUXOSCCLK}}}{(\text{REVDIV} + 1)} \times \frac{\text{IMULT}}{(\text{ODIV} + 1)}$$

6.12.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.12.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.12.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	10	25	MHz

6.12.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

6.12.3.2.1.3 X1 Input Level Characteristics When Using an External Clock Source Not a Crystal

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3	0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO	VDDIO + 0.3	V

6.12.3.2.1.4 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

6.12.3.2.1.5 AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(AUXI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(AUXI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(AUXL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(AUXH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

6.12.3.2.1.6 APLL Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
PLL Lock time				
SYS/AUX PLL Lock Time[3]			5µs + (1024 * (REFDIV + 1) * $t_{c(OSCCLK)}$)	us

(1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

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6.12.3.2.1.7 XCLKOUT Switching Characteristics PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2[2]	H + 2[2]	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2[2]	H + 2[2]	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

(1) A load of 40 pF is assumed for these parameters.
(2) H = $0.5t_{c(XCO)}$

6.12.3.2.1.8 Internal Clock Frequencies

		MIN	TYP	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		200	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	5		500	ns
$f_{(INTCLK)}$	Frequency, system PLL going into VCO (after REFDIV)[1]	10		25	MHz
$f_{(VCOCLK)}$	Frequency, system PLL VCO (before ODIV)	220		600	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	6		400	MHz
$f_{(AUXINTCLK)}$	Frequency, auxiliary PLL going into VCO (after REFDIV)	10		25	MHz
$f_{(AUXVCOCLK)}$	Frequency, auxiliary PLL VCO (before ODIV)	220		600	MHz
$f_{(AUXPLLRAWCLK)}$	Frequency, auxiliary PLL output (before AUXCLK divider)	6		400	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200	MHz
$f_{(PLL\_LIMP)}$	Frequency, PLL Limp Frequency [2]		45/(ODIV+1)		MHz
$f_{(AUXPLL)}$	Frequency, AUXPLLCLK	2		150	MHz
$f_{(AUXPLL\_LIMP)}$	Frequency, AUXPLL Limp Frequency [3]		45/(ODIV+1)		MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		200	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	5		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)		See respective clock		MHz
$f_{(AUXOSCCLK)}$	Frequency, auxiliary OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1 or AUXCLKIN)		See respective clock		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK			200	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		200	MHz

(1) INTOSC1 and INTOSC2 with +/-3% resolution can be used as a Reference Clock to PLL
(2) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp)
(3) PLL output frequency when AUXOSCCLK is dead (Loss of AUXOSCCCLK causes AUXPLL to Limp)

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6.12.3.3 Input Clocks

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 6-24 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 (also referred to as XTAL) and AUXCLKIN.

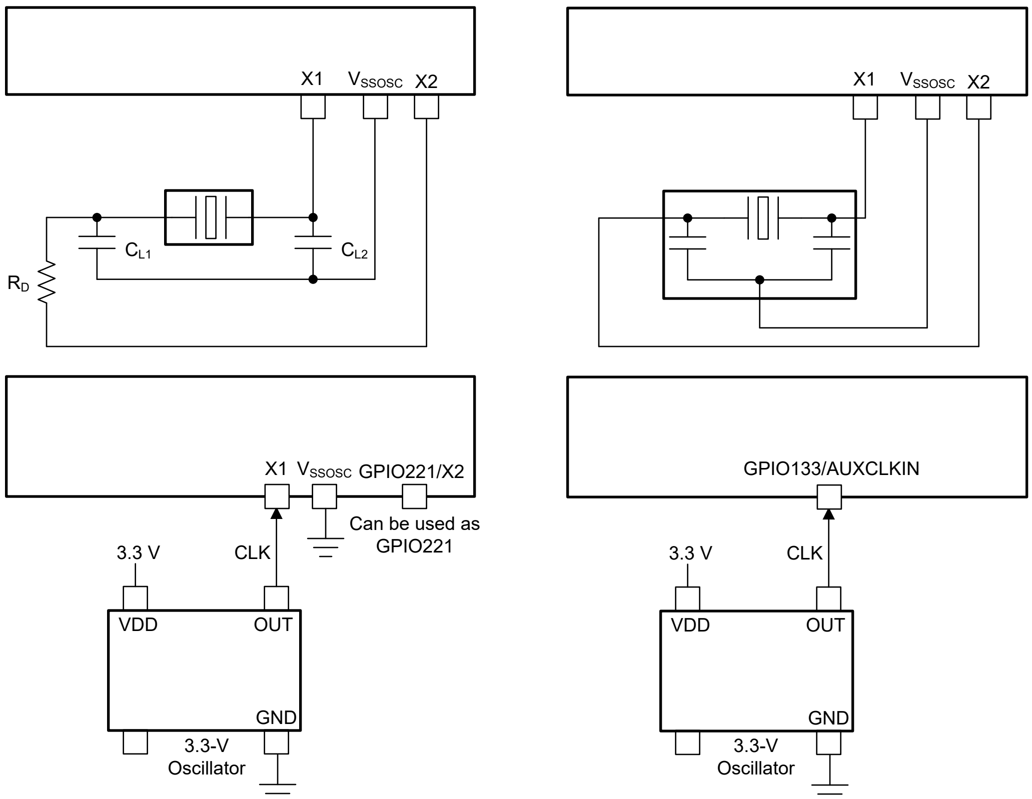

Figure 6-24. Connecting Input Clocks to a F28P65x Device

6.12.3.4 XTAL Oscillator

6.12.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.12.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.12.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 6-25 illustrates the components of the electrical oscillator and the tank circuit.

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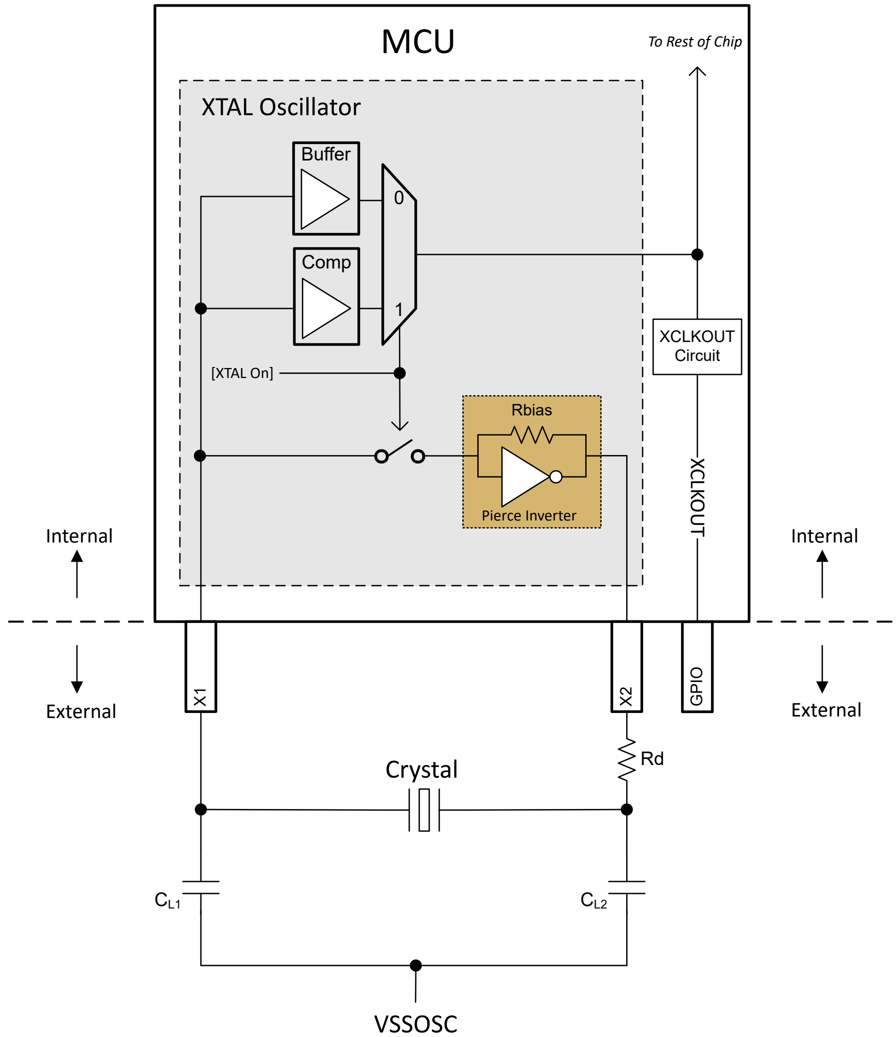

Figure 6-25. Electrical Oscillator Block Diagram

6.12.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.12.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when [XTAL On] = 1, which is achieved by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

6.12.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

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This mode is enabled when [XTAL On] = 0, which can be achieved by setting XTALCR.OSCOFF = 1 and XTALCR.SE = 1.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.12.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the GPIO Muxed Pins table for a list of GPIOs that XCLKOUT comes out on.

6.12.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-26 and explained below.

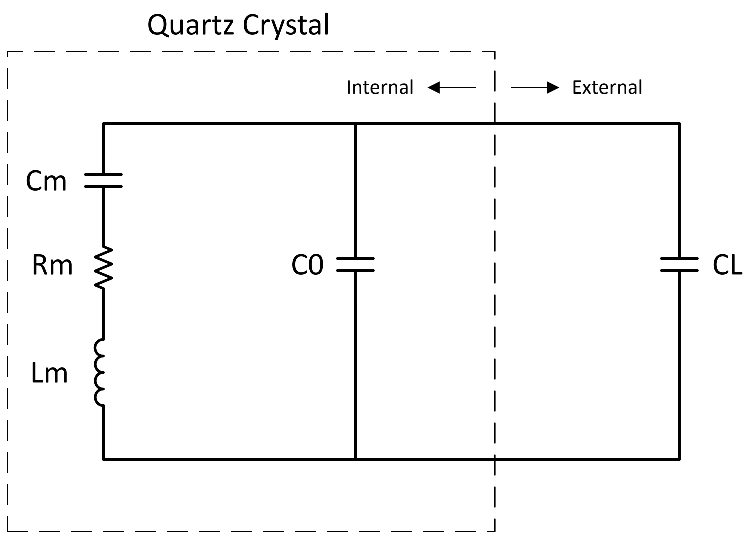

Figure 6-26. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-25, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

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Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.12.3.4.2.3 GPIO Modes of Operation

Refer to the External Oscillator (XTAL) section of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* .

6.12.3.4.3 Functional Operation

6.12.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \qquad (2)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.12.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 6-27 and Figure 6-28 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 6-5 for minimum and maximum values for design considerations.

6.12.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the Rneg – Negative Resistance section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to Crystal Oscillator Specifications for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.12.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified

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by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.12.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
   - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
   - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

6.12.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.12.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the How to Choose a Crystal section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

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6.12.3.4.7 Crystal Oscillator Specifications

6.12.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF			4	ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF			2	ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.12.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 6-5. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

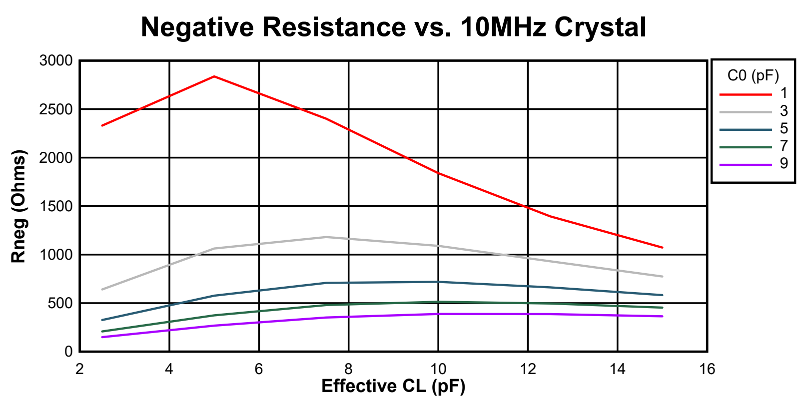

Figure 6-27. Negative Resistance Variation at 10 MHz

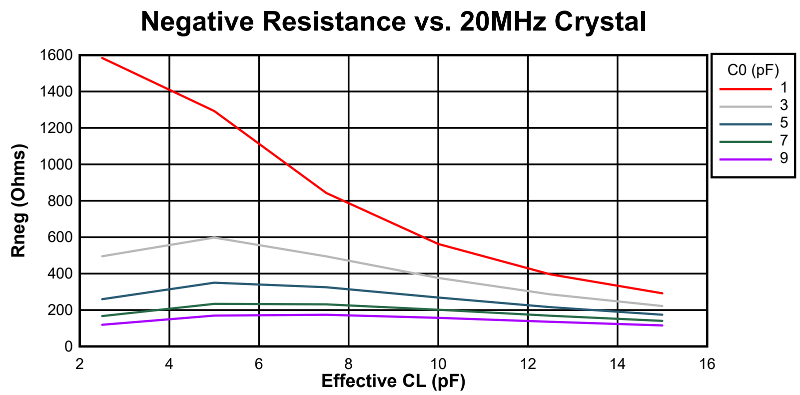

Figure 6-28. Negative Resistance Variation at 20 MHz

6.12.3.4.7.3 Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

6.12.3.4.7.4 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

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6.12.3.5 Internal Oscillators

To reduce production board costs and application development time, all devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

Applications requiring tighter **SCI baud rate matching** can use the SCI baud tuning example (baud_tune_via_uart) available in C2000Ware.

6.12.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		PACKAGE SUFFIX	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{INTOSC}	Frequency, INTOSC1 and INTOSC2(1)	All	-40°C to 125°C	9.7 (–3%)	10	10.3 (3.0%)	MHz
$f_{INTOSC\text{-}STABILITY}$	Frequency stability at room temperature	All	30°C, Nominal VDD		±0.1		%
$t_{INT0SC\text{-}ST}$	Start-up and settling time	All				20	µs

(1) INTOSC frequency may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.

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6.12.4 Flash Parameters

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 128-bit-wide prefetch reads and a pipeline buffer. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM.

This device also has an One-Time-Programmable (OTP) sector used for the dual code security module (DCSM), which cannot be erased after it is programmed.

Table 6-6 lists the minimum required flash wait states at different frequencies. The *Flash Parameters* table lists the flash parameters.

Table 6-6. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

CPUCLK (MHz)	Wait States (FRDCNTL[RWAIT][(1)])
160 < CPUCLK ≤ 200	4
120 < CPUCLK ≤ 160	3
80 < CPUCLK ≤ 120	2
0 < CPUCLK ≤ 80	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

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6.12.4.1 Flash Parameters

PARAMETER		MIN	TYP	MAX	UNIT
Program Time[(1)]	128 data bits + 16 ECC bits		62.5	625	µs
	2KB (Sector)		8	80	ms
Erase Time[(2) (3)] at < 25 cycles	2KB (Sector)		15	55	ms
	64KB		17	61	ms
	128KB		18	66	ms
	256KB		21	78	ms
Erase Time[(2) (3)] at 1000 cycles	2KB (Sector)		25	130	ms
	64KB		28	143	ms
	128KB		30	157	ms
	256KB		35	183	ms
Erase Time[(2) (3)] at 2000 cycles	2KB (Sector)		30	221	ms
	64KB		33	243	ms
	128KB		36	265	ms
	256KB		42	310	ms
Erase Time[(2) (3)] at 20K cycles	2KB (Sector)		120	1003	ms
	64KB		132	1102	ms
	128KB		145	1205	ms
	256KB		169	1410	ms
N_{wec} Write/Erase Cycles per sector				20000	cycles
N_{wec} Write/Erase Cycles for entire Flash (combined all sectors)				100000	cycles
$t_{retention}$ Data retention duration at T_J = 85°C		20			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
• Code that uses flash API to program the flash
• Flash API itself
• Flash data to be programmed
In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.
(2) Erase time includes Erase verify by the CPU.
(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

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6.12.5 RAM Specifications

Table 6-7. CPU1 RAM Parameters

RAM TYPE	SIZE	FETCH TIME(1) (CYCLES)	READ TIME(1) (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH	NUMBER OF BUSES AVAILABLE	NUMBER OF WAIT STATES	BURST ACCESS
GS RAM	80KB	2	2	1	16/32 bits	4	0	No
LS RAM	64KB	2	2	1	16/32 bits	2	0	No
Dx RAM(2)	96KB	2	2	1	16/32 bits	1	0	No
M0	2KB	2	2	1	16/32 bits	2	0	No
M1	2KB	2	2	1	16/32 bits	2	0	No
CLA-to-CPU Message RAM	256B	2	2	1	16/32 bits	2	0	No
CPU-to-CLA Message RAM	256B	2	2	1	16/32 bits	2	0	No
CLA-to-DMA Message RAM	256B	2	2	1	16/32 bits	3	0	No
DMA-to-CLA Message RAM	256B	2	2	1	16/32 bits	3	0	No
CPU1-to-CPU2 Message RAM	2KB	2	2	1	16/32 bits	4	0	No
CPU2-to-CPU1 Message RAM	2KB	2	2	1	16/32 bits	4	0	No

(1) Without arbitration between read/write/fetch. Access completes in 2 cycles; otherwise, arbitration priority (Write/Read/Fetch) is followed.
(2) Dx RAM 64KB can be shared with CPU2. So, CPU1 can be between 32KB to 96KB.

Table 6-8. CPU2 RAM Parameters

RAM TYPE	SIZE	FETCH TIME(1) (CYCLES)	READ TIME(1) (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH (CPU/ DMA)	NUMBER OF BUSES AVAILABLE	NUMBER OF WAIT STATES	BURST ACCESS
GS RAM	80KB	2	2	1	16/32 bits	4	0	No
Dx RAM(2)	64KB	2	2	1	16/32 bits	1	0	No
M0	2KB	2	2	1	16/32 bits	2	0	No
M1	2KB	2	2	1	16/32 bits	2	0	No
CPU1-to-CPU2 Message RAM	2KB	2	2	1	16/32 bits	4	0	No
CPU2-to-CPU1 Message RAM	2KB	2	2	1	16/32 bits	4	0	No

(1) Without arbitration between read/write/fetch. Access completes in 2 cycles; otherwise, arbitration priority (Write/Read/Fetch) is followed.
(2) Dx RAM 64KB can be shared with CPU1. So, CPU2 can be between 0KB to 64KB.

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6.12.6 ROM Specifications

Table 6-9. CPU1 ROM Parameters

ROM TYPE	SIZE	FETCH TIME[(1)] (CYCLES)	READ TIME[(1)] (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH	NUMBER OF BUSES AVAILABLE	NUMBER OF WAIT STATES	BURST ACCESS
Boot ROM	88KB	3	3	1	16/32 bits	1	1	No
Secure ROM	16KB	3	3	1	16/32 bits	1	1	No
CLA Data ROM	8KB	2	2	1	16/32 bits	2	0	No

(1) Worst-case time reported for 200 MHz.

Table 6-10. CPU2 ROM Parameters

ROM TYPE	SIZE	FETCH TIME[(1)] (CYCLES)	READ TIME[(1)] (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH (CPU/ DMA)	NUMBER OF BUSES AVAILABLE	NUMBER OF WAIT STATES	BURST ACCESS
Boot ROM	88KB	3	3	1	16/32 bits	1	1	No
Secure ROM	16KB	3	3	1	16/32 bits	1	1	No

(1) Worst-case time reported for 200 MHz.

6.12.7 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). Figure 6-29 shows how the 14-pin JTAG header connects to the MCU’s JTAG port signals. Figure 6-30 shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints in CCS for C2000 devices.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

Note

JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.

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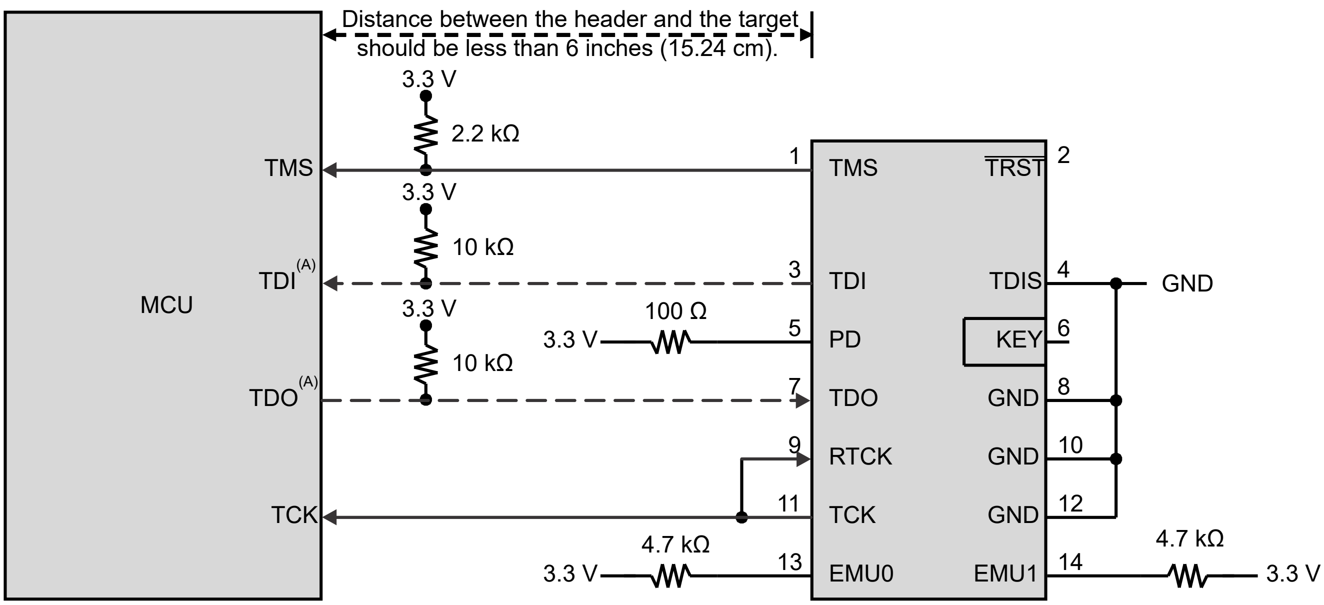
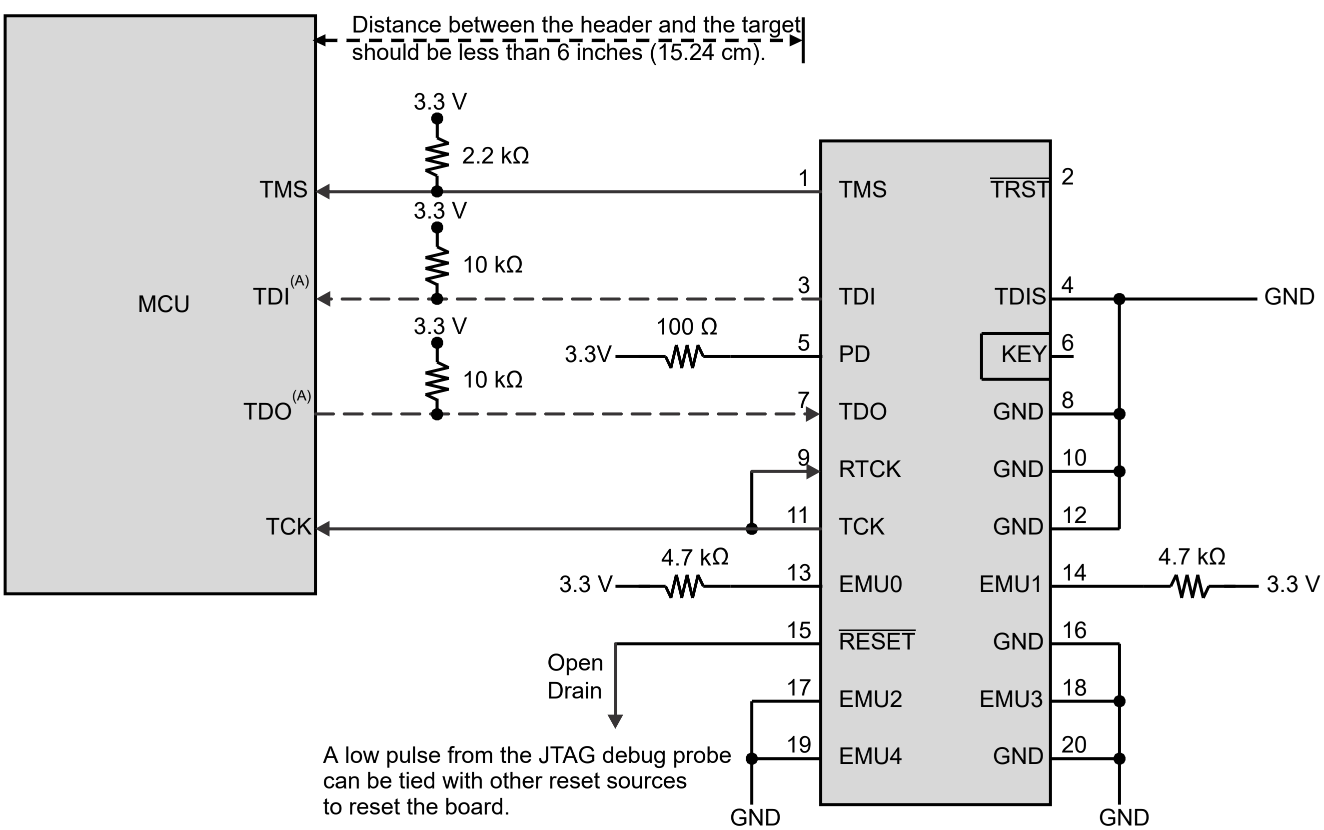


A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-29. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-30. Connecting to the 20-Pin JTAG Header

6.12.7.1 JTAG Electrical Data and Timing

6.12.7.1.1 JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	7		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	7		ns
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		ns

6.12.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	25	ns

6.12.7.1.3 JTAG Timing Diagram

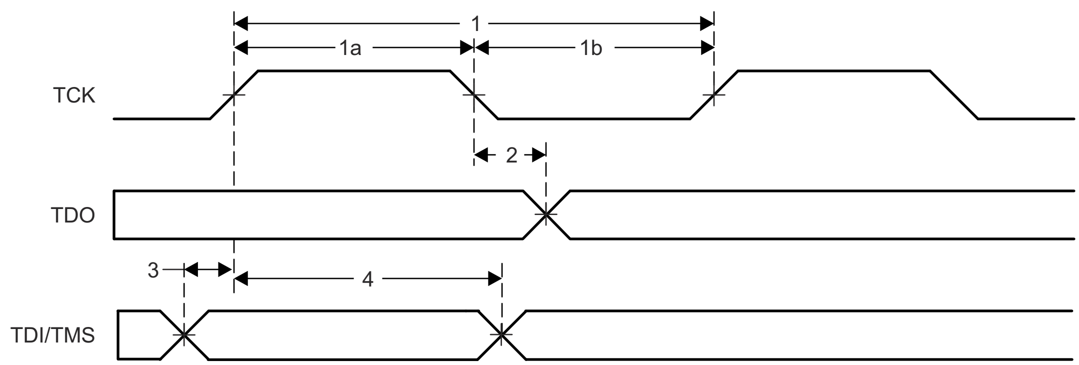


Figure 6-31. JTAG Timing

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6.12.7.2 cJTAG Electrical Data and Timing

6.12.7.2.1 cJTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	100		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	40		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	40		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	7		ns
3	$t_{su(TMS-TCKL)}$	Input setup time, TMS valid to TCK low	7		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	2		ns
4	$t_{h(TCKL-TMS)}$	Input hold time, TMS valid from TCK low	2		ns

6.12.7.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TMS)}$	Delay time, TCK low to TMS valid	6	20	ns
5	$t_{dis(TCKH-TMS)}$	Delay time, TCK high to TMS disable		25	ns

6.12.7.2.3 cJTAG Timing Diagram

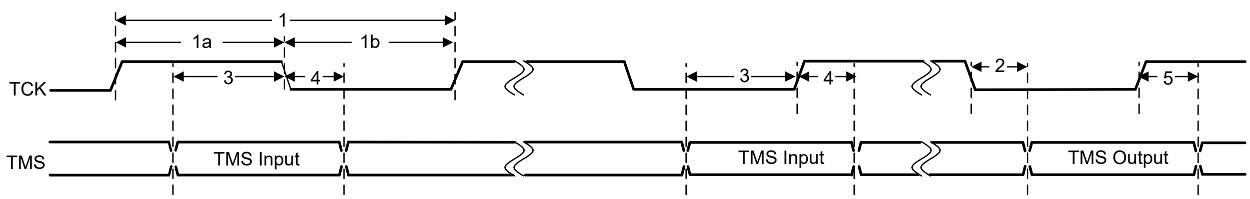

Figure 6-32. cJTAG Timing

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6.12.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

6.12.8.1 GPIO – Output Timing

6.12.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8[(1)]	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8[(1)]	ns
t_{fGPO}	Toggling frequency, GPIO pins			50	MHz

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

6.12.8.1.2 General-Purpose Output Timing Diagram

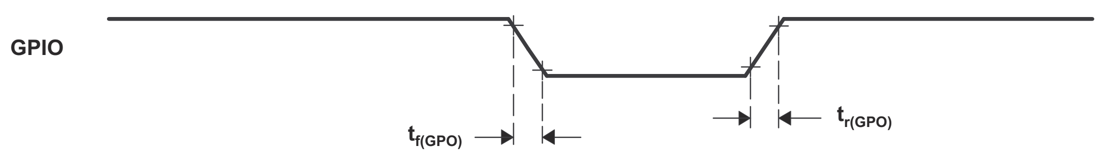

Figure 6-33. General-Purpose Output Timing

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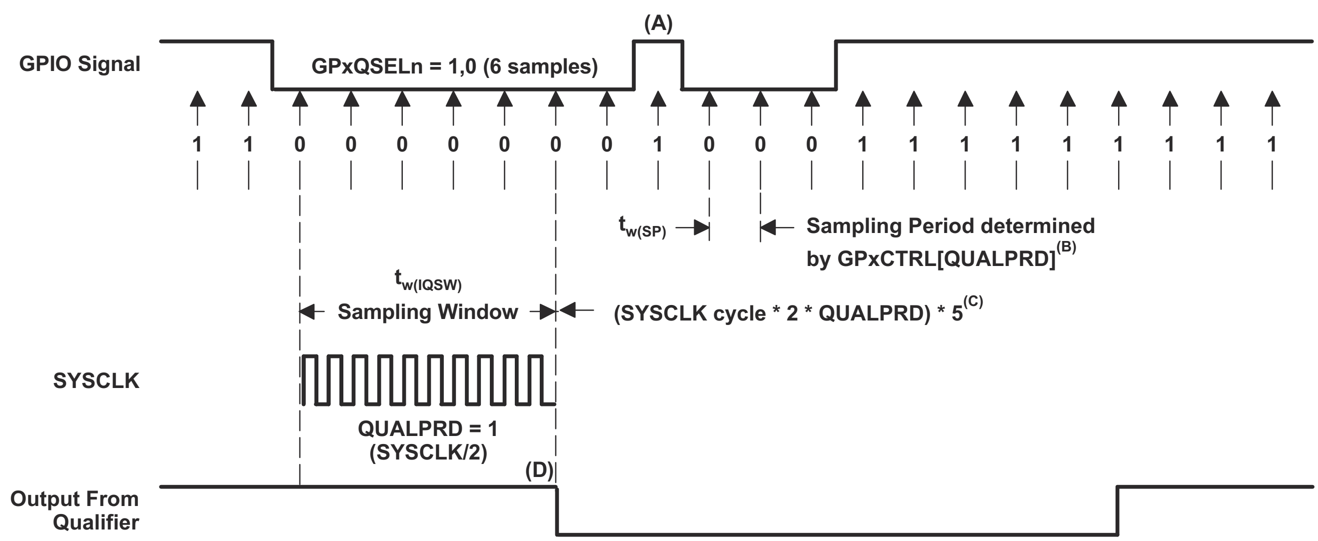
6.12.8.2 GPIO – Input Timing

6.12.8.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n[(1)] – 1)		cycles
$t_{w(GPI)}$ [(2)]	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.12.8.2.2 Sampling Mode



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-34. Sampling Mode

6.12.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

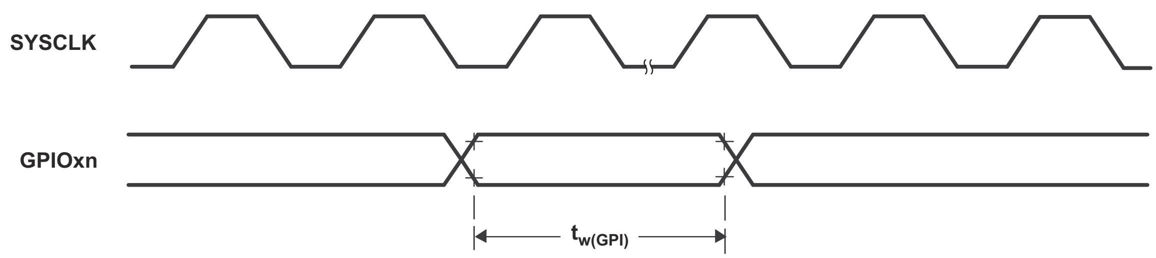


Figure 6-35. General-Purpose Input Timing

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6.12.9 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-36 shows the interrupt architecture for this device.

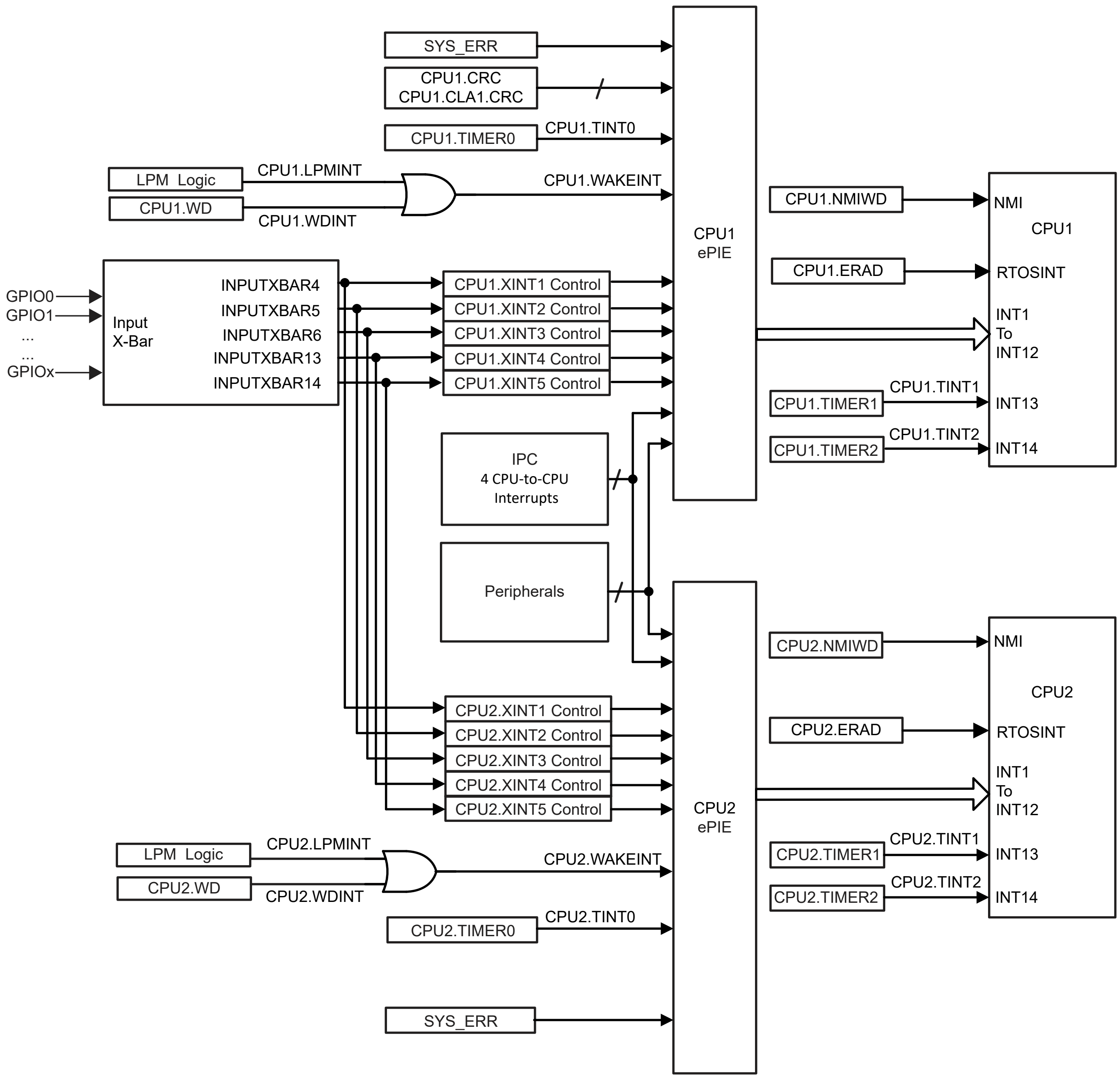

Figure 6-36. Device Interrupt Architecture

6.12.9.1 External Interrupt (XINT) Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.12.9.1.1 External Interrupt Timing Requirements

			MIN MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$	cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$	cycles

6.12.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch(1)	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) This assumes that the ISR is in a single-cycle memory.

6.12.9.1.3 External Interrupt Timing

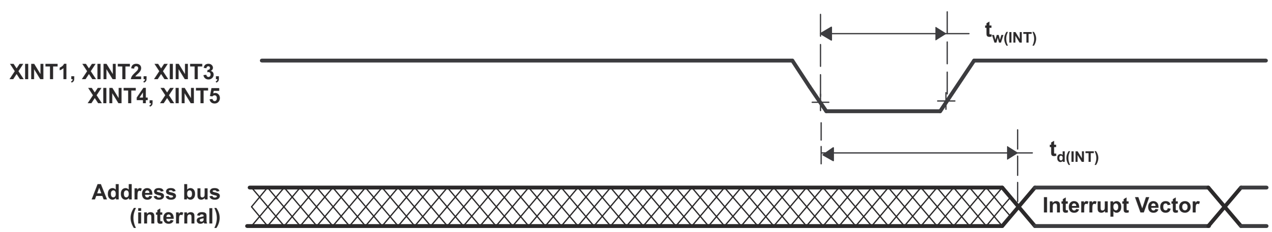

Figure 6-37. External Interrupt Timing

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6.12.10 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low-Power Modes section of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

6.12.10.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. Table 6-11 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-11. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	IDLE	STANDBY	HALT
SYSCLK	Active	Gated	Gated
CPUCLK	Gated	Gated	Gated
Clock to modules connected to PERx.SYSCLK	Active	Gated	Gated
WDCLK	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
PLL	Powered	Powered	Software must power down PLL before entering HALT.
INTOSC1	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash(1)	Powered	Powered	Powered
XTAL(2)	Powered	Powered	Powered

(1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application. For more information, see the Flash and OTP Memory section of the System Control chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.
(2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

6.12.10.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.12.10.2.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

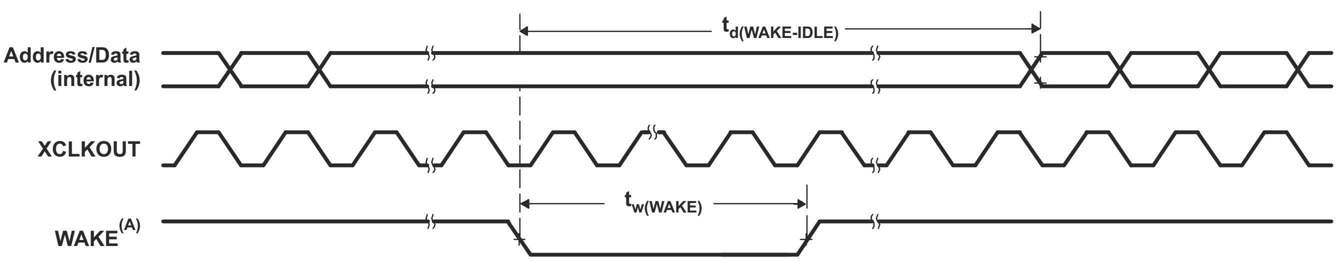
6.12.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume(1)	From Flash (active state)	Without input qualifier		$40t_{c(SYSCLK)}$	cycles
			With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles
		From Flash (sleep state)	Without input qualifier		$6700t_{c(SYSCLK)}$ (2)	cycles
			With input qualifier		$6700t_{c(SYSCLK)}$ (2) + $t_{w(WAKE)}$	cycles
		From RAM	Without input qualifier		$25t_{c(SYSCLK)}$	cycles
			With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.12.10.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-38. IDLE Entry and Exit Timing Diagram

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6.12.10.2.4 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | $(2 + QUALSTDBY)t_{c(OSCCLK)}$ [(1)]	$(2 + QUALSTDBY) * t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

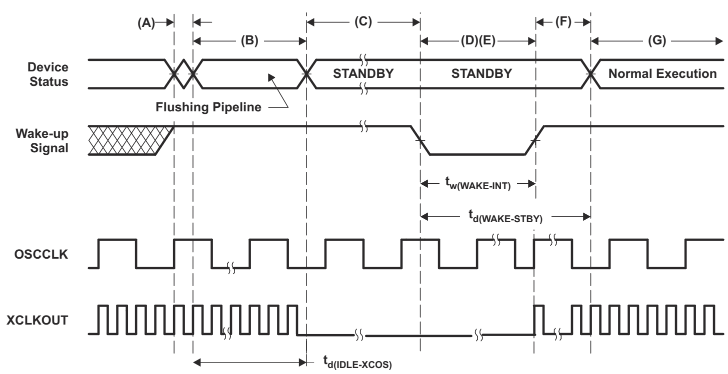
6.12.10.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume[(1)]	Wakeup from flash (Flash module in active state)		$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from flash (Flash module in sleep state)		$6700t_{c(SYSCLK)}$ [(2)] $+ t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from RAM		$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.12.10.2.6 STANDBY Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-39. STANDBY Entry and Exit Timing Diagram

6.12.10.2.7 HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal[(1)]	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal[(1)]	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See *Crystal Oscillator (XTAL)* section for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see the Internal Oscillators section for t_{oscst}. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

6.12.10.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	Wakeup from Flash - Flash module in active state		$75t_{c(OSCCLK)}$	
	Wakeup from Flash - Flash module in sleep state		$17500t_{c(OSCCLK)}$ [(1)]	
	Wakeup from RAM		$75t_{c(OSCCLK)}$	

(1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

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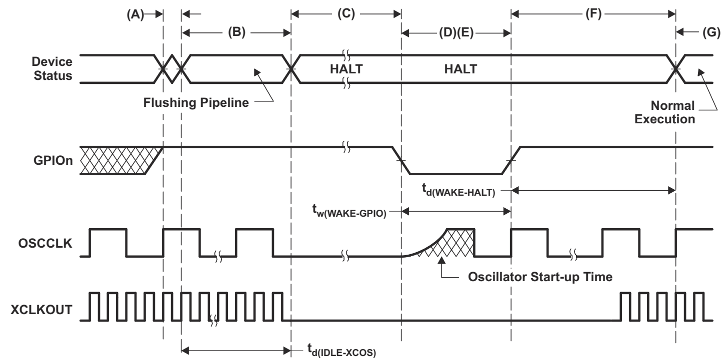
6.12.10.2.9 HALT Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into HALT mode.
B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
G. Normal operation resumes.
H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-40. HALT Entry and Exit Timing Diagram

6.12.11 External Memory Interface (EMIF)

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

6.12.11.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects ($\overline{\text{EMIF\_CS}[4:2]}$). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable time-out
- Select strobe option

6.12.11.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select ($\overline{\text{EMIF\_CS}[0]}$).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in C2000Ware for C2000 MCUs and the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with 8-, 9-, 10-, and 11-column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. The EMIF module does not support mobile SDRAM devices.

On this device, the EMIF does not support burst access for SDRAM configurations. This means every access to an external SDRAM device will have CAS latency.

6.12.11.3 EMIF Electrical Data and Timing

6.12.11.3.1 EMIF Synchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EMIFDV\text{-}EM\_CLKH)}$	Input setup time, read data valid on EMxD[y:0] before EMxCLK rising	2		ns
20	$t_{h(CLKH\text{-}DIV)}$	Input hold time, read data valid on EMxD[y:0] after EMxCLK rising	1.5		ns

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6.12.11.3.2 EMIF Synchronous Memory Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK	10		ns
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK (With 210MHz Timing Closure)	9.52		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMxCLK high or low	3		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ valid		8	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ invalid	1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMxCLK rising to EMxDQM[y:0] valid		8	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMxCLK rising to EMxDQM[y:0] invalid	1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid		8	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid	1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMxCLK rising to EMxD[y:0] valid		8	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMxCLK rising to EMxD[y:0] invalid	1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMxCLK rising to EMxRAS valid		8	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMxCLK rising to EMxRAS invalid	1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMxCLK rising to EMxCAS valid		8	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMxCLK rising to EMxCAS invalid	1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxWE}}$ valid		8	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxWE}}$ invalid	1		ns
17	$t_{d(CLKH-DHZ)}$	Delay time, EMxCLK rising to EMxD[y:0] in tri-state condition		8	ns
18	$t_{oh(CLKH-DLZ)}$	Output hold time, EMxCLK rising to EMxD[y:0] driving	1		ns

6.12.11.3.3 EMIF Synchronous Memory Timing Diagrams

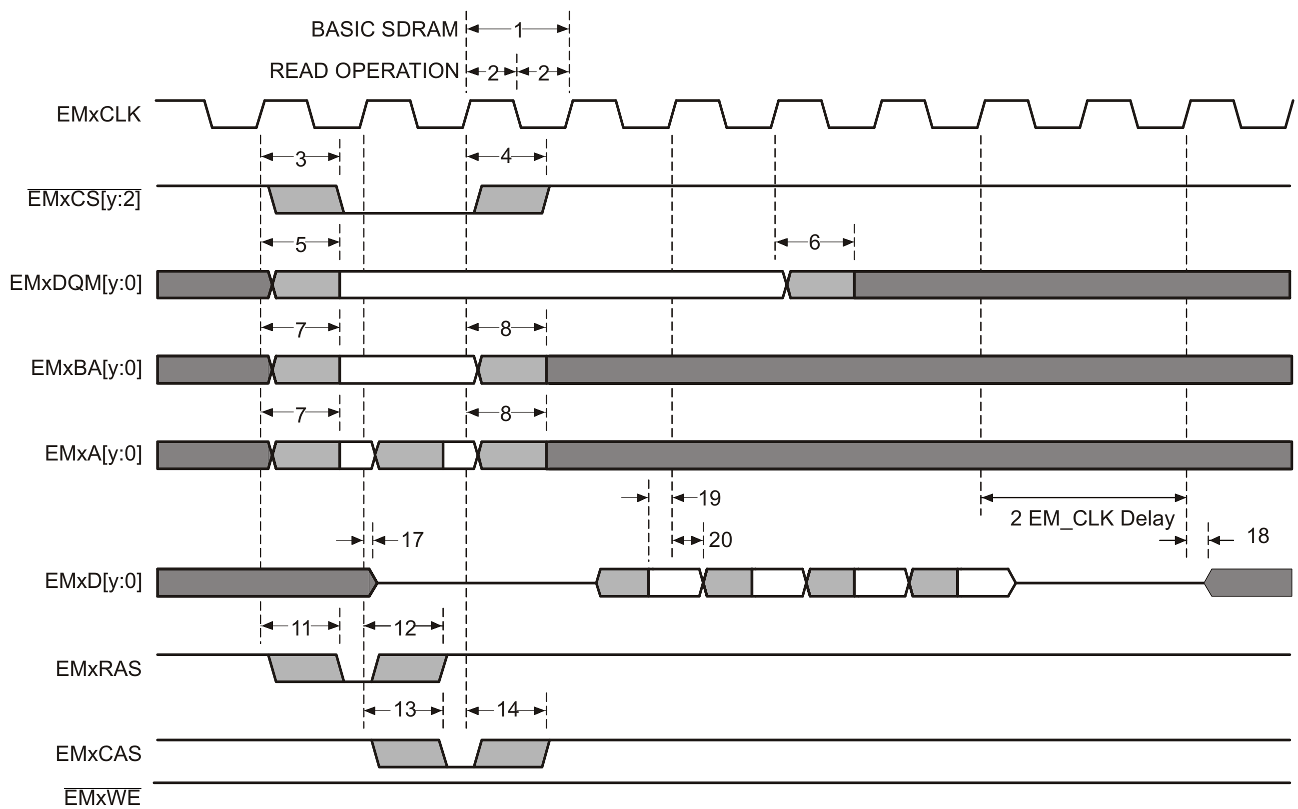

Figure 6-41. Basic SDRAM Read Operation

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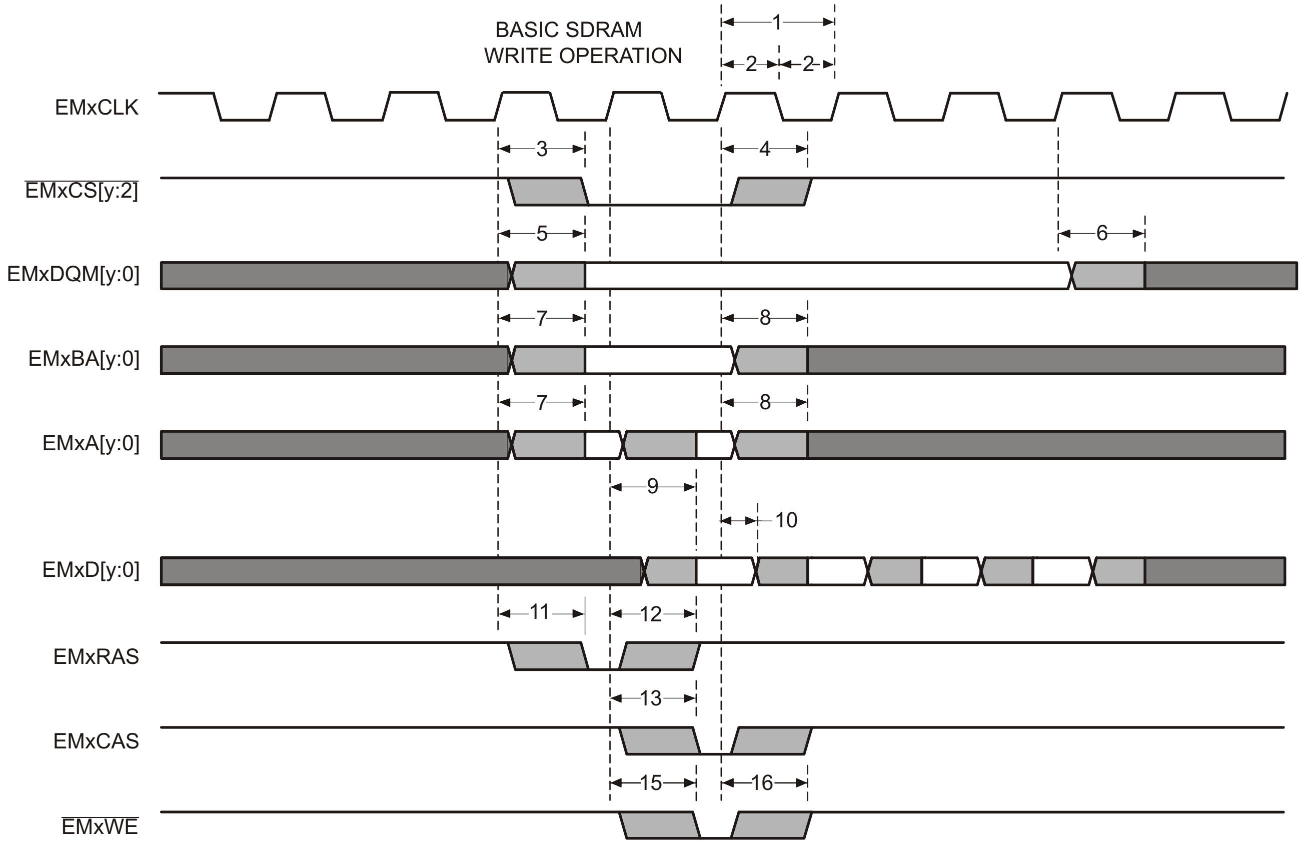

Figure 6-42. Basic SDRAM Write Operation

6.12.11.3.4 EMIF Asynchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
Reads and Writes					
	E	EMIF clock period	$t_{c(SYSCLK)}$		ns
2	$t_{w(EM\_WAIT)}$	Pulse duration, EMxWAIT assertion and deassertion	2E(1)		ns
Reads					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMxD[y:0] valid before EMxOE high	15		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMxD[y:0] valid after EMxOE high	0		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20(1)		ns
Writes					
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20(1)		ns

(1) E = EMxCLK period in ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. The *EMxWAIT Read Timing Requirements* figure and the *EMxWAIT Write Timing Requirements* figure describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

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6.12.11.3.5 EMIF Asynchronous Memory Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[(1) (2) (3)]		MIN	MAX	UNIT
1	$t_{d(TURNAROUND)}$	Turn around time TA=0	(TA)*E–3	(TA)*E+2	ns
Reads					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E–3	(RS+RST+RH)*E+2	ns
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 1)	(RS+RST+RH+ (EWC*16))*E–3	(RS+RST+RH+ (EWC*16))*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{\text{EMxCS[y:2]}}$ low to $\overline{\text{EMxOE}}$ low (SS = 0) RS=0	(RS)*E–3	(RS)*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{\text{EMxCS[y:2]}}$ low to $\overline{\text{EMxOE}}$ low (SS = 1)	–3	2	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{\text{EMxOE}}$ high to $\overline{\text{EMxCS[y:2]}}$ high (SS = 0)	(RH)*E–3	(RH)*E	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{\text{EMxOE}}$ high to $\overline{\text{EMxCS[y:2]}}$ high (SS = 1)	–3	0	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{\text{EMxOE}}$ low	(RS)*E–3	(RS)*E+2	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{\text{EMxOE}}$ high to EMxBA[y:0] invalid	(RH)*E–3	(RH)*E	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EMxA[y:0] valid to $\overline{\text{EMxOE}}$ low	(RS)*E–3	(RS)*E+2	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{\text{EMxOE}}$ high to EMxA[y:0] invalid	(RH)*E–3	(RH)*E	ns
10	$t_{w(EMOEL)}$	$\overline{\text{EMxOE}}$ active low width (EW = 0)	(RST)*E–1	(RST)*E+1	ns
10	$t_{w(EMOEL)}$	$\overline{\text{EMxOE}}$ active low width (EW = 1)	(RST+(EWC*16))*E–1	(RST+(EWC*16))*E+1	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMxWAIT deasserted to $\overline{\text{EMxOE}}$ high	4*E+10	5*E+15	ns
29	$t_{su(EMDQMV-EMOEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{\text{EMxOE}}$ low	(RS)*E–3	(RS)*E+2	ns
30	$t_{h(EMOEH-EMDQMIV)}$	Output hold time, $\overline{\text{EMxOE}}$ high to EMxDQM[y:0] invalid	(RH)*E–3	(RH)*E	ns
Writes					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E–3	(WS+WST+WH)*E+2	ns
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 1)	(WS+WST+WH+ (EWC*16))*E–3	(WS+WST+WH+ (EWC*16))*E+2	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{\text{EMxCS[y:2]}}$ low to $\overline{\text{EMxWE}}$ low (SS = 0)	(WS)*E–3	(WS)*E+2	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{\text{EMxCS[y:2]}}$ low to $\overline{\text{EMxWE}}$ low (SS = 1)	–3	2	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{\text{EMxWE}}$ high to $\overline{\text{EMxCS[y:2]}}$ high (SS = 0)	(WH)*E–3	(WH)*E	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{\text{EMxWE}}$ high to $\overline{\text{EMxCS[y:2]}}$ high (SS = 1)	–3	0	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{\text{EMxWE}}$ high to EMxDQM[y:0] invalid	(WH)*E–3	(WH)*E	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{\text{EMxWE}}$ high to EMxBA[y:0] invalid	(WH)*E–3	(WH)*E	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMxA[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns

6.12.11.3.5 EMIF Asynchronous Memory Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[(1) (2) (3)]		MIN	MAX	UNIT
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxA[y:0] invalid	(WH)*E–3	(WH)*E	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 0)	(WST)*E–1	(WST)*E+1	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 1)	(WST+(EWC*16))*E–1	(WST+(EWC*16))*E+1	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxWE}$ high	4*E+10	5*E+15	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMxD[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+2	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxD[y:0] invalid	(WH)*E–3	(WH)*E	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–4], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* for more information.
(2) E = EMxCLK period in ns.
(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256–1]. The maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* for more information.

6.12.11.3.6 EMIF Asynchronous Memory Timing Diagrams

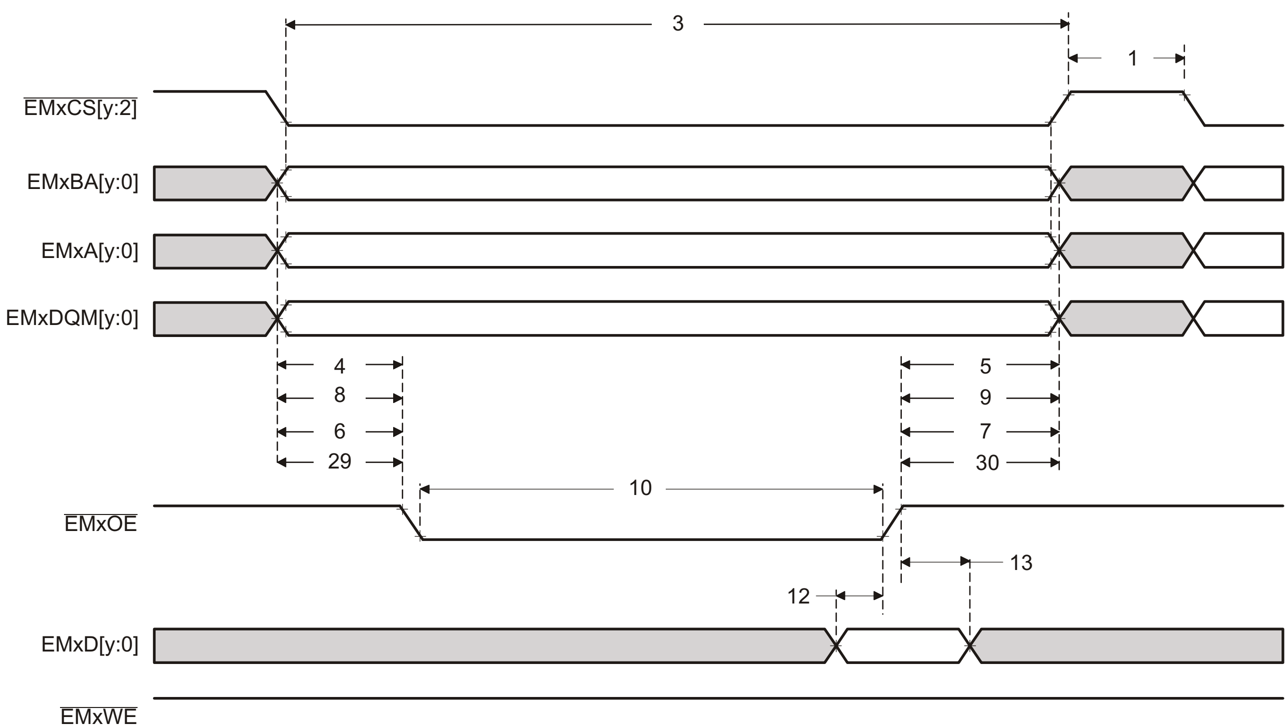

Figure 6-43. Asynchronous Memory Read Timing

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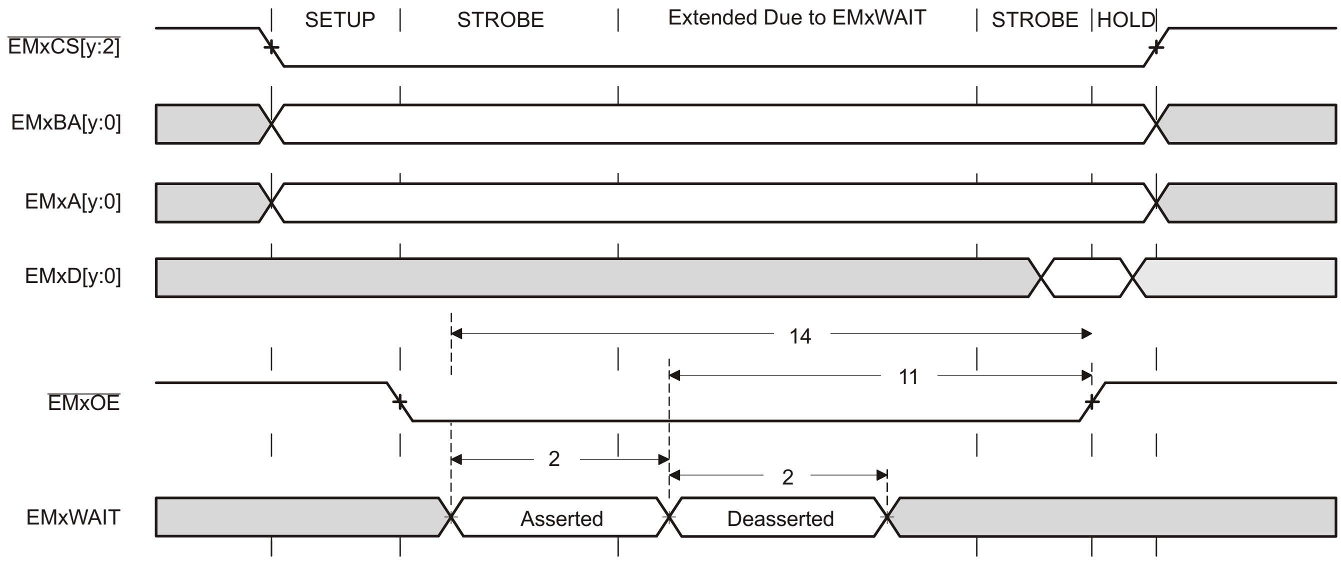

Figure 6-44. EMxWAIT Read Timing Requirements

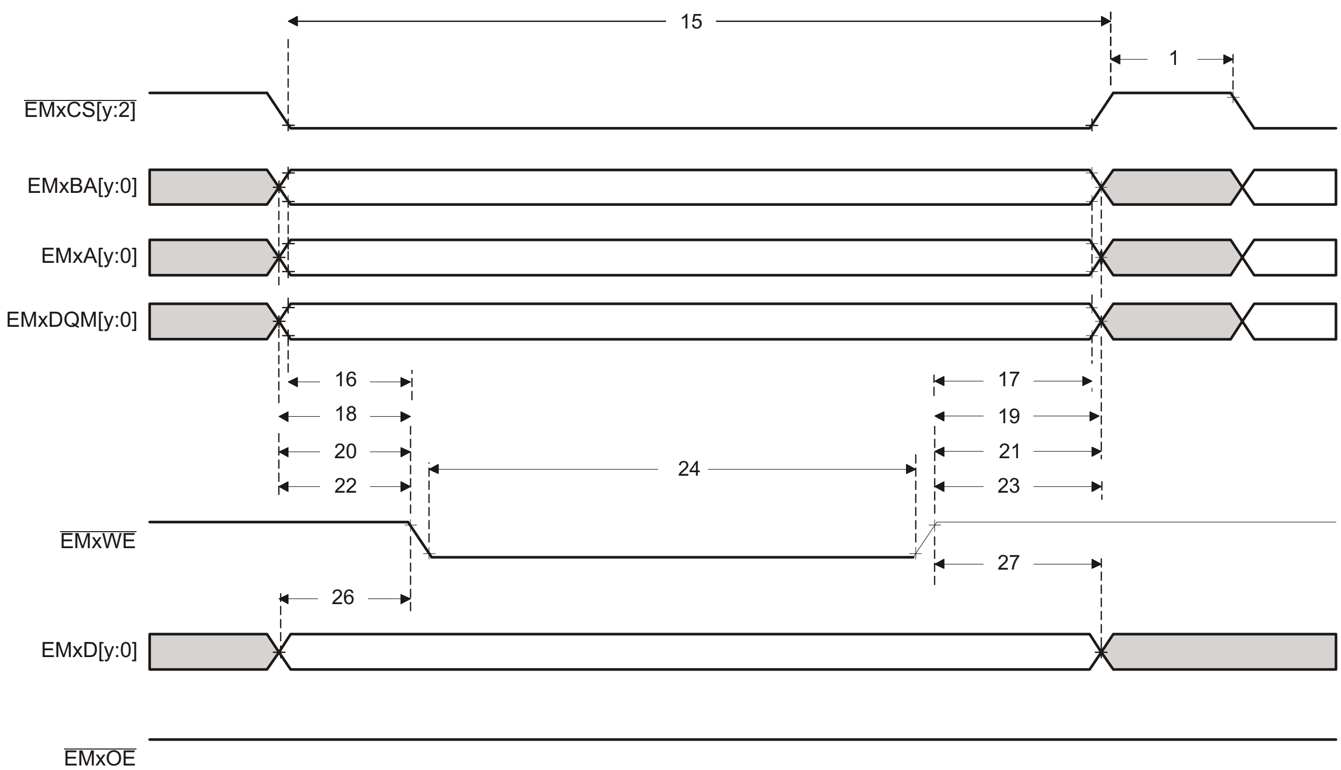

Figure 6-45. Asynchronous Memory Write Timing

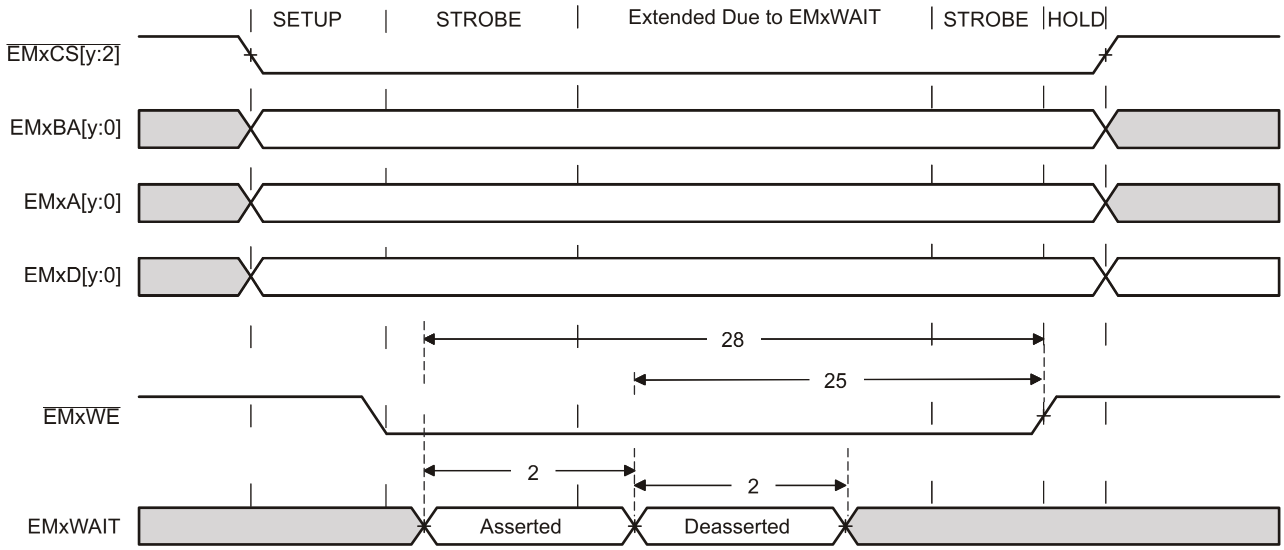

Figure 6-46. EMxWAIT Write Timing Requirements

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6.13 C28x Analog Peripherals

6.13.1 Analog Subsystem

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Buffered Digital-to-Analog Converter (DAC), and Comparator Subsystem (CMPSS).

6.13.1.1 Features

The analog subsystem has the following features:

- Flexible voltage references:
  - The ADCs are referenced to VREFHIx and VREFLOx pins.
    - VREFHIA pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference. VREFHIB and VREFHIC can be connected to the internal reference using an external on-board connection.
    - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V.
  - The buffered DACs are referenced to VREFHIx and VSSA
    - Alternately, these DACs can be referenced to the VDAC pin and VSSA
  - The comparator DACs are referenced to VDDA and VSSA
    - Alternately, these DACs can be referenced to the VDAC pin and VSSA
- Flexible pin usage
  - Buffered DAC outputs, comparator subsystem inputs, and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs

6.13.1.2 Block Diagram

The following analog subsystem block diagrams show the connections between the different integrated analog modules to the device pins. These pins fall into two categories: analog module inputs/outputs and reference pins.

The reference pins, VREFHIA to VREFHIC and VREFLOA to VREFLOC, can be used to supply an external voltage reference to the associated ADCs. VREFHIA can also be used to supply the voltage reference to DAC A, and VREFHIB can be used to supply the voltage reference to DAC C. An internal voltage reference is available and connects to VREFHIA. To use the internal voltage reference on ADC B, ADC C or DAC C, connect VREFHIA to VREFHIB and/or VREFHIC externally.

The VDAC reference pin can be used to set an alternate range for DAC A and DAC C, and for the DACs inside the CMPSS modules (the CMPSS DACs are referenced to VDDA and VSSA by default). Using this pin as a reference prevents the channel from being used as an ADC input (but the ADC can be used to sample the VDAC voltage, if desired). The choice of reference is configurable per module for each CMPSS or buffered DAC; the selection is made using the module's configuration registers.

Some analog pins support digital functionality through muxed AIOs and AGPIOs. AIOs only support digital input functionality, while AGPIOs support full digital input and output functionality.

The following notes apply to all packages:

- Not all analog pins are available on all devices. See Section 5 to determine which pins are available.
- See Section 6.13.2.2 to determine the allowable voltage range for VREFHI and VREFLO.
- An external capacitor is required on the VREFHI pins. See Section 6.13.2.2 for the specific value required.
- For buffered DAC modules, VSSA is the low reference whether VREFHIx or VDAC is selected as the high reference.
- For CMPSS modules, VSSA is the low reference whether VDAC or VDDA is selected as the high reference.

Note

If all ADCs are operating in internal VREF mode, then VREFHIA, VREFHIB, and VREFHIC must be manually connected externally.

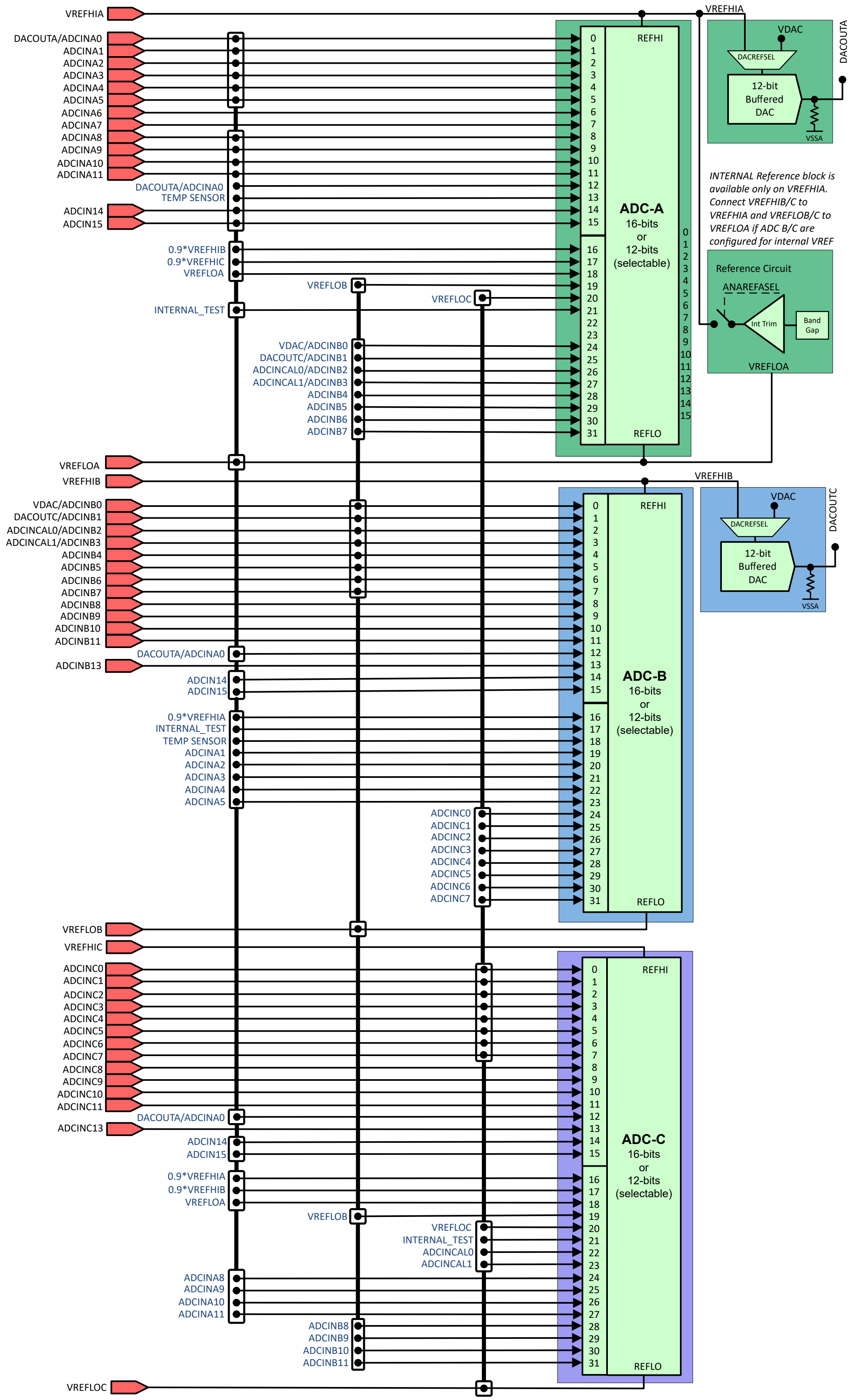

Figure 6-47. Analog System Block Diagram (ADC A, ADC B and ADC C)

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Input connections to the CMPSS modules are selectable through a programmable input mux. Figure 6-48 shows the CMPSS input connections. Table 6-12 shows the mapping of ADC input signals to CMPSS mux inputs.

- To configure the CMPH_POSIN input mux for CMPSSx, write to the CMPxHPMXSEL field in the CMPHPMXSEL or CMPHPMXSEL1 analog subsystem register.
- To configure the CMPH_NEGIN input mux for CMPSSx, write to the CMPxHNMXSEL field in the CMPHNMXSEL analog subsystem register.
- To configure the CMPL_POSIN input mux for CMPSSx, write to the CMPxLPMXSEL field in the CMPLPMXSEL or CMPLPMXSEL1 analog subsystem register.
- To configure the CMPL_NEGIN input mux for CMPSSx, write to the CMPxLNMXSEL field in the CMPLNMXSEL analog subsystem register.

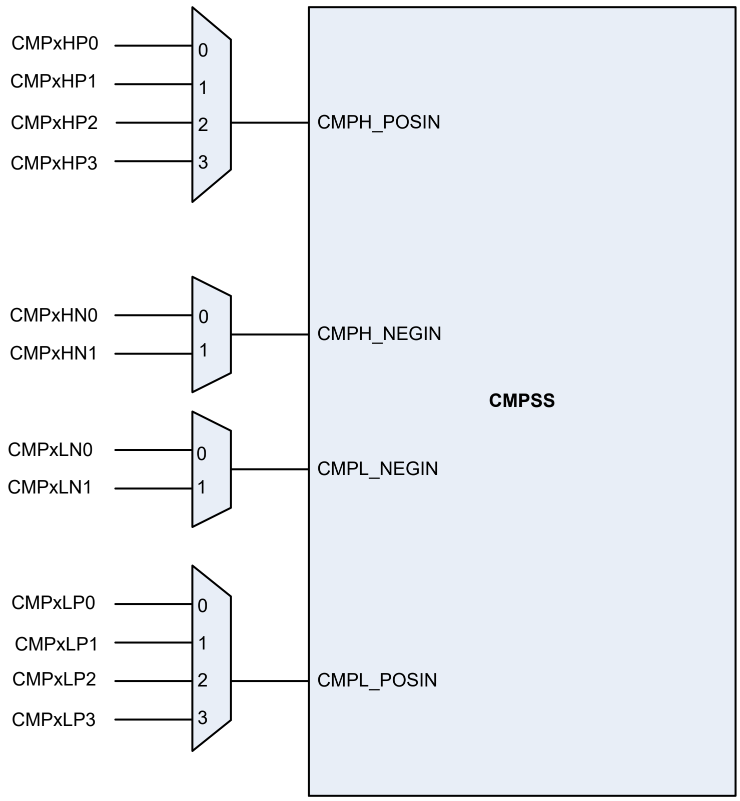

Figure 6-48. CMPSS Input Connections

Table 6-12. CMPSS Input Mux Options

	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7	CMP8	CMP9	CMP10	CMP11
HP0	A2	A4	B2	A14	C4	C2	A6	A8	B13	C10	C11
HP1	A0	B8	B0	B10	B4	C0	B6	A10	C13	C6	C7
HP2	A1	B9	B1	B11	B5	C1	B7	A11	A7	C8	C9
HP3	A3	A5	TS	A15	TS	0.9*VREF HIA	0.9*VREF HIB	0.9*VREF HIC			
HN0	A3	A5	B3	A15	C5	C3	A7	A9	A0	B8	B0
HN1	A1	A2	B7	B10	B4	C0	B6	A10	B9	C4	C13
LP0	A2	A4	B2	A14	C4	C2	A6	A8	B13	C10	C11
LP1	A0	B8	B0	B10	B4	C0	B6	A10	C13	C6	C7
LP2	A1	B9	B1	B11	B5	C1	B7	A11	A5	C8	C9
LP3	B3	C5	C3	A7	A9	0.9*VREF HIA	0.9*VREF HIB	0.9*VREF HIC			

Table 6-12. CMPSS Input Mux Options (continued)

	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7	CMP8	CMP9	CMP10	CMP11
LN0	A3	A5	B3	A15	C5	C3	A7	A9	A0	B8	B0
LN1	A1	A2	B7	B10	B4	C0	B6	A10	B9	C4	C13

Table 6-13. Analog Signal Descriptions

Signal Name	Description
ADCINAx, Ax	ADC A Input
ADCINBx, Bx	ADC B Input
ADCINCx, Cx	ADC C Input
CMPH_POSIN	Comparator subsystem high comparator positive input
CMPH_NEGIN	Comparator subsystem high comparator negative input
CMPL_POSIN	Comparator subsystem low comparator positive input
CMPL_NEGIN	Comparator subsystem low comparator negative input
DACOUTx	Buffered DAC Output
TEMP SENSOR, TS	Internal temperature sensor
VDAC	Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference that cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-μF capacitor on this pin.

Table 6-14. Reference Summary

Module	Reference Option	Configured Where?	Register	Driverlib Function	Notes
ADC	External or Internal	Analog Subsystem	AnalogSubsysRegs.ANAREFCTL.bit.ANAREFxSEL	ASysCtl_setAnalogReferenceInternal, ASysCtl_setAnalogReferenceExternal	Internal reference only connected to ADCA. For ADCB/ADC, VREFHI pins must be externally connected to VREFHIA.
	Internal Reference 2.5V or 3.3V	Analog Subsystem	AnalogSubsysRegs.ANAREFCTL.bit.ANAREFx2P5SEL	ASysCtl_setAnalogReference2P5, ASysCtl_setAnalogReference1P65	
Buffered DAC	VREFHI or VDAC	DAC Module	DacxRegs.DACCTL.bit.DACREFSEL	DAC_setReferenceVoltage	
	External or Internal	Analog Subsystem	AnalogSubsysRegs.ANAREFCTL.bit.ANAREFxSEL	ASysCtl_setAnalogReferenceInternal, ASysCtl_setAnalogReferenceExternal	Internal reference only connected to ADCA. For ADCB/ADC, VREFHI pins must be externally connected to VREFHIA.
CMPSS DACs	VDDA or VDAC	CMPSS Module	CmpssxRegs.COMPDACHCTL.bit.SELREF	CMPSS_COMPDACHCTL_SELREF	

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Table 6-15. Analog Internal Connections

Pin Name	Pins/Package				ADC			DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	256 ZEJ	176 PTP	169 NMR	100 PZP	A	B	C		High Positive	High Negative	Low Positive	Low Negative	
VREFHIA	M2	37	K2	19									
VREFHIB	R4	53	M4	34									
VREFHIC	L2	35	J2	19									
VREFLOA	M1	33	K1	16	A18		C18						
VREFLOB	T4	50	N4	32	A19		C19						
VREFLOC	L1	32	J1	16	A20		C20						
Analog Group 1									CMP1				
A1	P2	42	K3	24	A1	B19			CMP1 (HPMXSEL=2)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=2)	CMP1 (LNMXSEL=1)	AIO228
A3	N4	40	H3	22	A3	B21			CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)		CMP1 (LNMXSEL=0)	AIO230
Analog Group 2									CMP1/CMP2/CMP9				
A2	N3	41	J3	23	A2	B20			CMP1 (HPMXSEL=0)	CMP2 (HNMXSEL=1)	CMP1 (LPMXSEL=0)	CMP2 (LNMXSEL=1)	AIO229
A0	P1	43	L3	25	A0,A12	B12	C12	DACA_OUT	CMP1 (HPMXSEL=1)	CMP9 (HNMXSEL=0)	CMP1 (LPMXSEL=1)	CMP9 (LNMXSEL=0)	AIO227
Analog Group 3									CMP2				
A4	M4	39	H2	21	A4	B22			CMP2 (HPMXSEL=0)		CMP2 (LPMXSEL=0)		AIO231
Analog Group 4									CMP2/CMP9/CMP10				
A5	M5	38	H1	20	A5	B23			CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP9 (LPMXSEL=2)	CMP2 (LNMXSEL=0)	AIO232
B9	N8	67	N7			B9	C29		CMP2 (HPMXSEL=2)	CMP9 (HNMXSEL=1)	CMP2 (LPMXSEL=2)	CMP9 (LNMXSEL=1)	GPIO218
B8	P8	66	M7			B8	C28		CMP2 (HPMXSEL=1)	CMP10 (HNMXSEL=0)	CMP2 (LPMXSEL=1)	CMP10 (LNMXSEL=0)	GPIO217
Analog Group 5									CMP3				
TempSensor					A13	B18			CMP3 (HPMXSEL=3)				
B2	R3	48	M3	30	A26	B2			CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		AIO235
B1	T3	47	N3	29	A25	B1		DACC_OUT	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO234
Analog Group 6									CMP3/CMP1/CMP11				
B3	P3	49	L4	31	A27	B3				CMP3 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP3 (LNMXSEL=0)	AIO236
B0	T2	46	N2	28		B0	A24	VDAC	CMP3 (HPMXSEL=1)	CMP11 (HNMXSEL=0)	CMP3 (LPMXSEL=1)	CMP11 (LNMXSEL=0)	AIO233
Analog Group 7									CMP4				
A14/B14/C14	R1	44	M1	26	A14	B14	C14		CMP4 (HPMXSEL=0)		CMP4 (LPMXSEL=0)		AIO225
A15/B15/C15	R2	45	M2	27	A15	B15	C15		CMP4 (HPMXSEL=3)	CMP4 (HNMXSEL=0)		CMP4 (LNMXSEL=0)	AIO226
B11	P4	51				B11	C31		CMP4 (HPMXSEL=2)		CMP4 (LPMXSEL=2)		AIO240
B10	R7	61				B10	C30		CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	GPIO219
Analog Group 8									CMP5				
TempSensor					A13	B18			CPM5 (HPMXSEL=3)				
B5	N7	65	N6		A29	B5			CMP5 (HPMXSEL=2)		CMP5 (LPMXSEL=2)		GPIO216
B4	P7	64	M6		A28	B4			CMP5 (HPMXSEL=1)	CMP5 (HNMXSEL=1)	CMP5 (LPMXSEL=1)	CMP5 (LNMXSEL=1)	GPIO215
Analog Group 9									CMP5/CMP2/CMP10				
C5	L6	28	G6	12		B29	C5			CMP5 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP5 (LNMXSEL=0)	GPIO204
C4	M6	29	H6	13		B28	C4		CMP5 (HPMXSEL=0)	CMP10 (HNMXSEL=1)	CMP5 (LPMXSEL=0)	CMP10 (LNMXSEL=1)	GPIO205
Analog Group 10									CMP6				
0.9*VREFHIA						B16	C16		CMP6 (HPMXSEL=3)		CMP6 (LPMXSEL=3)		

Table 6-15. Analog Internal Connections (continued)

Pin Name	Pins/Package				ADC			DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	256 ZEJ	176 PTP	169 NMR	100 PZP	A	B	C		High Positive	High Negative	Low Positive	Low Negative	
C0	H1	22	F1	9		B24	C0		CMP6 (HPMXSEL=1)	CMP6 (HNMXSEL=1)	CMP6 (LPMXSEL=1)	CMP6 (LNMXSEL=1)	GPIO199
C1	J1	23	G1	10		B25	C1		CMP6 (HPMXSEL=2)		CMP6 (LPMXSEL=2)		GPIO200
C2	L4	31	H4	15		B26	C2		CMP6 (HPMXSEL=0)		CMP6 (LPMXSEL=0)		AIO237
Analog Group 11									CMP6/CMP3				
C3	L5	30	H5	14		B27	C3			CMP6 (HNMXSEL=0)	CMP3 (LPMXSEL=3)	CMP6 (LNMXSEL=0)	GPIO206
Analog Group 12									CMP7				
0.9*VREFHIB					A16		C17		CMP7 (HPMXSEL=3)		CMP7 (LPMXSEL=3)		
B6	N5	55	J4	36	A30	B6			CMP7 (HPMXSEL=1)	CMP7 (HNMXSEL=1)	CMP7 (LPMXSEL=1)	CMP7 (LNMXSEL=1)	GPIO207
A6	N6	57	J5	38	A6				CMP7 (HPMXSEL=0)		CMP7 (LPMXSEL=0)		GPIO209
Analog Group 13									CMP7/CMP3				
B7	P5	56	K4	37	A31	B7			CMP7 (HPMXSEL=2)	CMP3 (HNMXSEL=1)	CMP7 (LPMXSEL=2)	CMP3 (LNMXSEL=1)	GPIO208
Analog Group 14									CMP8				
0.9*VREFHIC					A17				CMP8 (HPMXSEL=3)		CMP8 (LPMXSEL=3)		
A8	R6	59	J6		A8		C24		CMP8 (HPMXSEL=0)		CMP8 (LPMXSEL=0)		GPIO211
A11	R8	63	L6	40	A11		C27		CMP8 (HPMXSEL=2)		CMP8 (LPMXSEL=2)		GPIO214
A10	T8	62	L5	39	A10		C26		CMP8 (HPMXSEL=1)	CMP8 (HNMXSEL=1)	CMP8 (LPMXSEL=1)	CMP8 (LNMXSEL=1)	GPIO213
Analog Group 15									CMP8/CMP5				
A9	T7	60	K6		A9		C25			CMP8 (HNMXSEL=0)	CMP5 (LPMXSEL=3)	CMP8 (LNMXSEL=0)	GPIO212
Analog Group 16									CMP9				
B13	R5					B13			CMP9 (HPMXSEL=0)		CMP9 (LPMXSEL=0)		AIO238
Analog Group 17									CMP9/CMP4/CMP7/CMP11				
A7	P6	58	K5		A7				CMP9 (HPMXSEL=2)	CMP7 (HNMXSEL=0)	CMP4 (LPMXSEL=3)	CMP7 (LNMXSEL=0)	GPIO210
C13	K1						C13		CMP9 (HPMXSEL=1)	CMP11 (HNMXSEL=1)	CMP9 (LPMXSEL=1)	CMP11 (LNMXSEL=1)	AIO239
Analog Group 18									CMP10				
C8	K3	25	G3				C8		CMP10 (HPMXSEL=2)		CMP10 (LPMXSEL=2)		GPIO202
C6	K5	27	G5	11		B30	C6		CMP10 (HPMXSEL=1)		CMP10 (LPMXSEL=1)		GPIO203
C10	L3						C10		CMP10 (HPMXSEL=0)		CMP10 (LPMXSEL=0)		AIO241
Analog Group 19									CMP11				
C9	J2	24	G2				C9		CMP11 (HPMXSEL=2)		CMP11 (LPMXSEL=2)		GPIO201
C11	K2						C11		CMP11 (HPMXSEL=0)		CMP11 (LPMXSEL=0)		AIO242
C7	K4	26	G4			B31	C7		CMP11 (HPMXSEL=1)		CMP11 (LPMXSEL=1)		GPIO198

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6.13.2 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with selectable resolution of 12 bits or 16 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*).

Each ADC has the following features:

- Selectable resolution of 12 bits or 16 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended or differential signal mode
- Input multiplexer with up to 26 channels (single ended) or 10 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- External analog input mux selection per SOC, up to 4 bits
- Multiple trigger sources
  - Software immediate start
  - All ePWMs: ADCSOC A or B
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
  - ECAP events in capture mode (CEVT1, CEVT2, CEVT3, and CEVT4) and APWM mode (period match, compare match, or both).
  - Global software trigger for multiple ADCs
- Four flexible PIE interrupts
- Burst-mode triggering option
- Hardware oversampling mode up to 128x, with configurable trigger spread delay
- Hardware undersampling mode
- Trigger phase delay function
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture
  - Absolute value calculation
  - 24-bit accumulation register for oversampling, with configurable binary shift
  - Minimum/maximum calculation for outlier rejection

Note

Not every channel can be pinned out from all ADCs. See the Pin Configuration and Functions section to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-49.

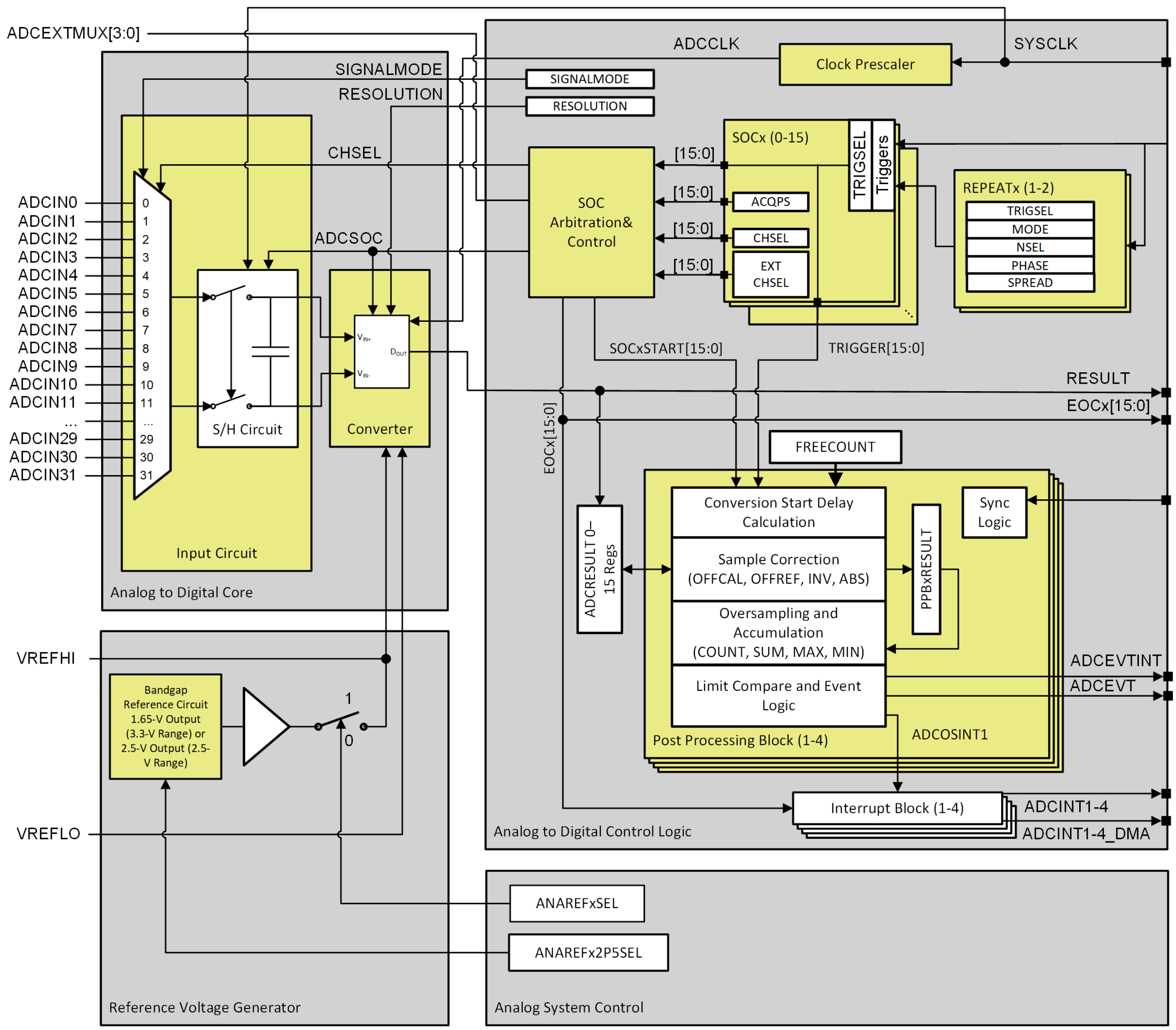

Figure 6-49. ADC Module Block Diagram

6.13.2.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-16 summarizes the basic ADC options and their level of configurability.

Table 6-16. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	Per module(1)
Resolution	Per module(1)
Signal mode	Per module
Reference voltage source	Per module (external or internal)(2)(3)
Trigger source	Per SOC(1)
Converted channel	Per SOC
Acquisition window duration	Per SOC(1)
EOC location	Per module
Burst mode	Per module(1)

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.
(2) Lower pin count packages may share one VREFHI pin among multiple ADCs. In this case, the ADCs that share a reference pin must have their reference modes configured identically.
(3) 3.3 V internal reference mode is not supported when using 16-bit resolution.

6.13.2.1.1 Signal Mode

The ADC supports two signal modes: single-ended and differential. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. In differential signaling mode, the input voltage to the converter is sampled through a pair of input pins, one of which is the positive input (ADCINxP) and the other is the negative input (ADCINxN). The actual input voltage is the difference between the two (ADCINxP − ADCINxN). Figure 6-50 shows the differential signaling mode. Figure 6-51 shows the single-ended signaling mode.

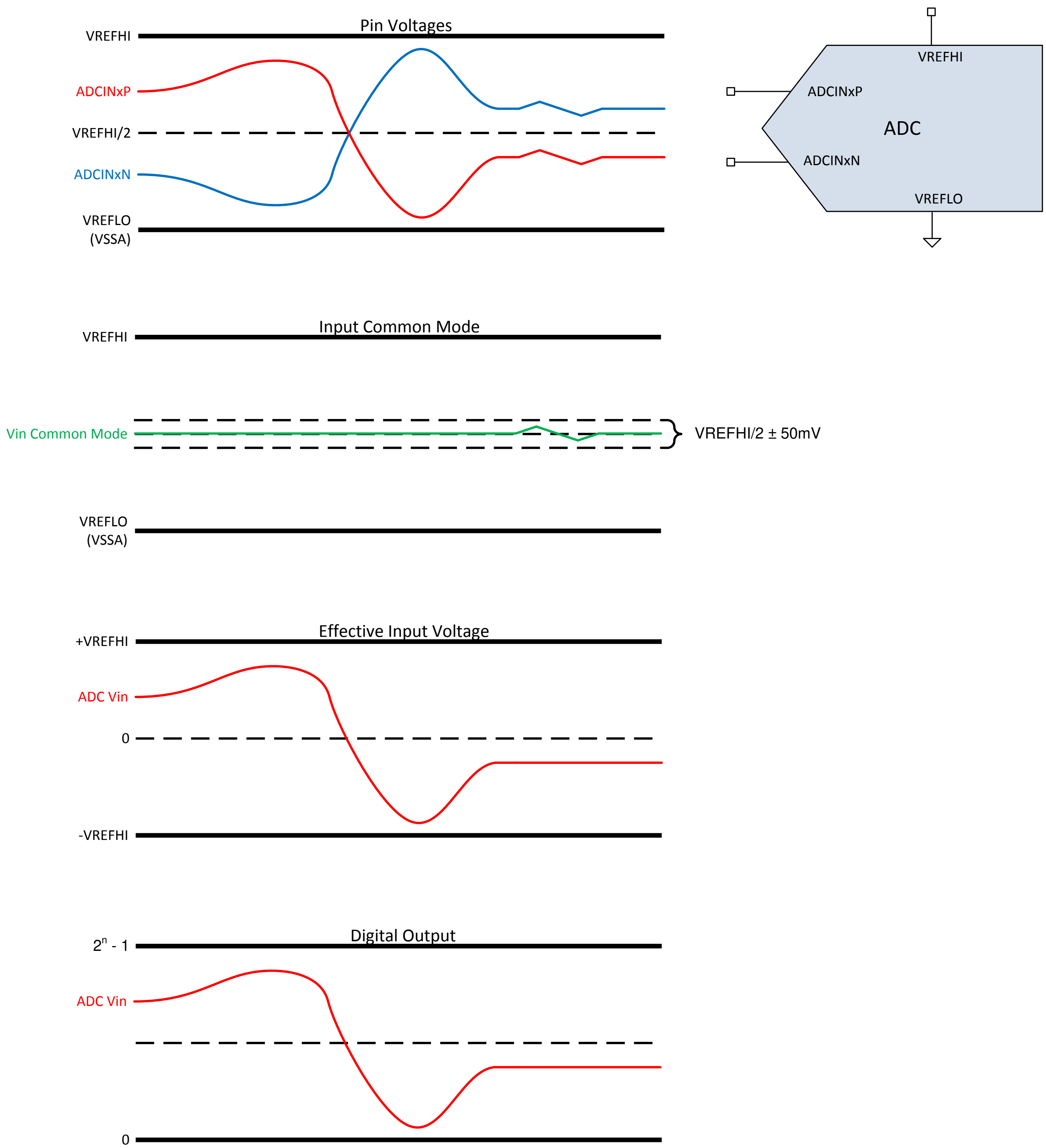

Figure 6-50. Differential Signaling Mode

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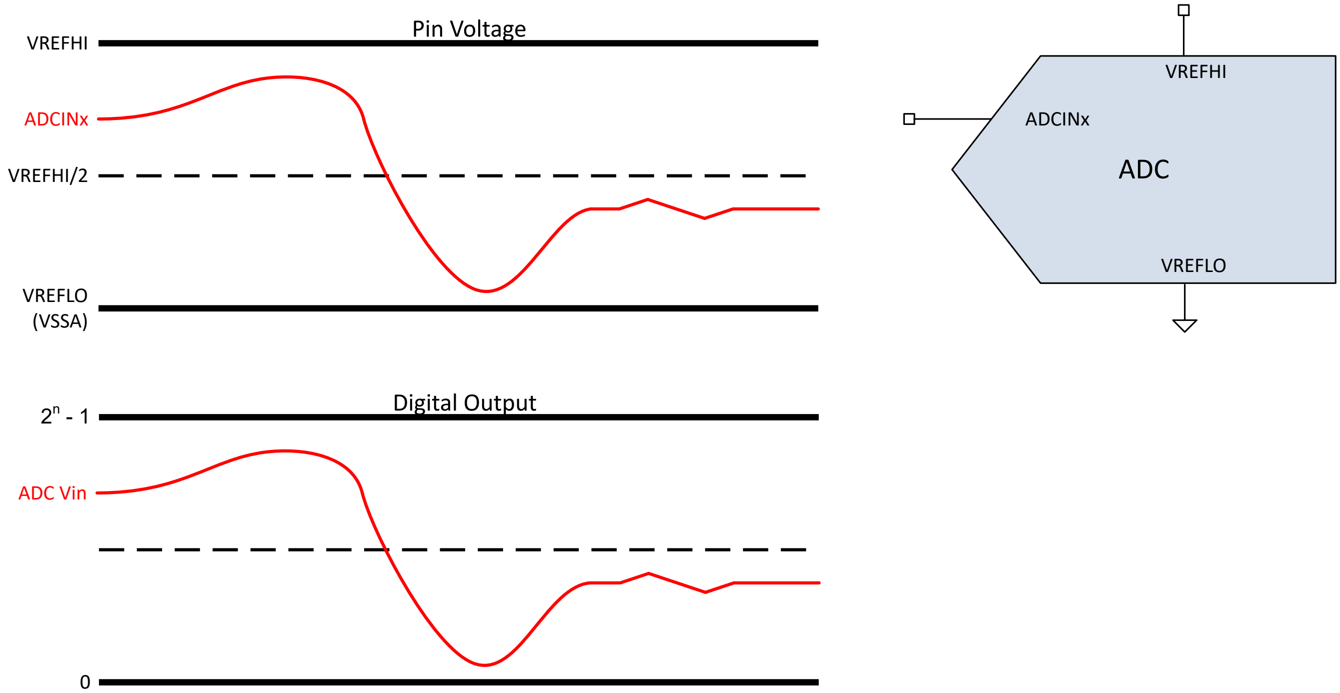

Figure 6-51. Single-ended Signaling Mode

6.13.2.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.13.2.2.1 ADC Operating Conditions 12-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		57	MHz
Sample rate[3]	200-MHz SYSCLK			3.92	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)[1]	With 50 Ω or less R_s Pin with AIO	75			ns
	With 50 Ω or less Rs Pin with AGPIO	90			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI[2]	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.13.2.2.2 ADC Operating Conditions 12-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		57	MHz
Sample rate[3]	200-MHz SYSCLK			3.92	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)[1]	With 50 Ω or less R_s pin with AIO	75			ns
	With 50 Ω or less R_s pin with AGPIO	90			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI[2]	Internal Reference = 3.3V Range		Not supported		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V

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6.13.2.2.2 ADC Operating Conditions 12-bit Differential (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion range	Internal Reference = 3.3 V Range		Not supported		V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.13.2.2.3 ADC Operating Conditions 16-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		57	MHz
Sample rate	200-MHz SYSCLK			1.19	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s Pin with AIO	320			ns
	With 50 Ω or less Rs Pin with AGPIO	405			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		Not supported		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range		Not supported		V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

6.13.2.2.4 ADC Operating Conditions 16-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		57	MHz
Sample rate	200-MHz SYSCLK			1.19	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s Pin with AIO	320			ns
	With 50 Ω or less R_s Pin with AGPIO	320			ns
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		Not supported		V
	Internal Reference = 2.5V Range		2.5		V
VREFLO		VSSA		VSSA	V
Conversion range	Internal Reference = 3.3 V Range		Not supported		V
	Internal Reference = 2.5 V Range	0		2.5	V
	External Reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.

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6.13.2.2.5 ADC Characteristics 12-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	10.1		11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			130		µA
Internal Reference Capacitor Value(2)		2.2			µF
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error(6)	Internal reference	–45		45	LSB
	External reference	–5	±3	5	LSB
Offset Error		–5	±2	5	LSB
Channel-to-Channel Gain Error(4)			±2		LSB
Channel-to-Channel Offset Error(4)			±2		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		±4		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		±2		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±1.0	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs		Not supported		LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		69.2		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		64.1		dB
THD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		–81.5		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		85		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		69.0		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		64.0		dB
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.2		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.2		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not supported		bits

6.13.2.2.5 ADC Characteristics 12-bit Single-Ended (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.
(6) ADC result output can be automatically adjusted for offset error by using the PPB Offset Calibration feature.

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6.13.2.2.6 ADC Characteristics 12-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	10.1		11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current[1]			130		µA
Internal Reference Capacitor Value[2]		2.2			µF
External Reference Capacitor Value[2]		2.2			µF
DC Characteristics					
Gain Error	Internal reference	–45		45	LSB
	External reference	–5	±3	5	LSB
Offset Error[6]		–5	±2	5	LSB
Channel-to-Channel Gain Error[4]			±2		LSB
Channel-to-Channel Offset Error[4]			±2		LSB
ADC-to-ADC Gain Error[5]	Identical VREFHI and VREFLO for all ADCs		±4		LSB
ADC-to-ADC Offset Error[5]	Identical VREFHI and VREFLO for all ADCs		±1		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±0.5	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs		Not supported		LSBs
AC Characteristics					
SNR[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		72.1		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		65.2		dB
THD[3]	VREFHI = 2.5 V, fin = 100 kHz		-86.9		dB
SFDR[3]	VREFHI = 2.5 V, fin = 100 kHz		90		dB
SINAD[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		72		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		65.1		dB
ENOB[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.7		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.7		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		bits

6.13.2.2.6 ADC Characteristics 12-bit Differential (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.
(6) ADC result output can be automatically adjusted for offset error by using the PPB Offset Calibration feature.

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6.13.2.2.7 ADC Characteristics 16-bit Single-Ended

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	29.6		31	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current[1]			190		µA
Internal Reference Capacitor Value[2]		22			µF
External Reference Capacitor Value[2]		22			µF
DC Characteristics					
Gain Error	Internal reference 2.5V	-720		720	LSB
	External reference	–64	±20	64	LSB
Offset Error[6]	Internal reference 2.5V	-16	±6	16	LSB
	External reference	–16	±6	16	LSB
Channel-to-Channel Gain Error[4]			±6		LSB
Channel-to-Channel Offset Error[4]			±6		LSB
ADC-to-ADC Gain Error[5]	Identical VREFHI and VREFLO for all ADCs		±6		LSB
ADC-to-ADC Offset Error[5]	Identical VREFHI and VREFLO for all ADCs		±6		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–6	±1.5	6	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–2		2	LSBs
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs		Not supported		LSBs
AC Characteristics					
SNR[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		83.5		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		78.2		
THD[3]	VREFHI = 2.5 V, fin = 100 kHz		–95		dB
SFDR[3]	VREFHI = 2.5 V, fin = 100 kHz		93		dB
SINAD[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		83.2		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		78.1		
ENOB[3]	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		13.5		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		13.5		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		

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6.13.2.2.7 ADC Characteristics 16-bit Single-Ended (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		77		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 800 kHz		74		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		77		
	VDDA = 3.3-V DC + 200 mV Sine at 800 kHz		74		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.
(6) ADC result output can be automatically adjusted for offset error by using the PPB Offset Calibration feature.

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6.13.2.2.8 ADC Characteristics 16-bit Differential

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	200-MHz SYSCLK	29.6		31	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			190		µA
Internal Reference Capacitor Value(2)		2.2			µF
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error	Internal reference 2.5V	-720		720	LSB
	External reference	–64	±9	64	LSB
Offset Error(6)	Internal reference 2.5V	-6	±4	6	LSB
	External reference	–6	±4	6	LSB
Channel-to-Channel Gain Error(4)			±6		LSB
Channel-to-Channel Offset Error(4)			±3		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		±6		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		±3		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–3.5	±1.0	3.5	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–2		2	LSBs
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs		Not supported		LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		89.8		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		66.3		dB
THD(3)	VREFHI = 2.5 V, fin = 100 kHz		–98		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz		99		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		89.2		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		66.1		dB
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		14.52		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		14.52		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		bits

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6.13.2.2.8 ADC Characteristics 16-bit Differential (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		77		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		74		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		77		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		74		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.
(6) ADC result output can be automatically adjusted for offset error by using the PPB Offset Calibration feature.

6.13.2.2.9 ADC Performance Per Pin

ADC performance of each pin is affected by adjacent pins. The following plots provide details on how these pins differ in performance.

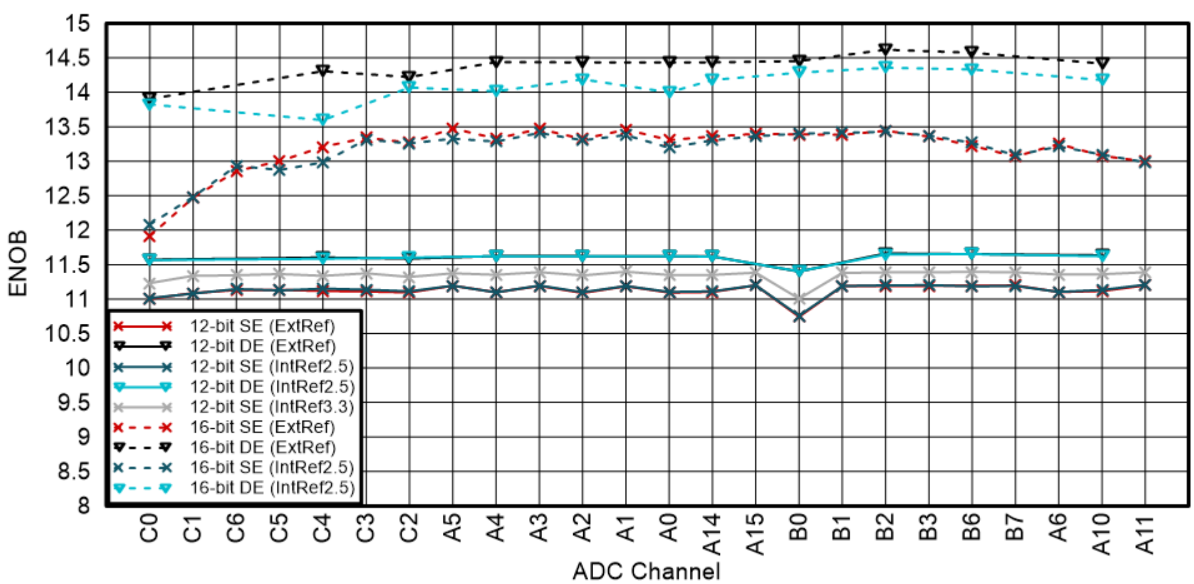

Figure 6-52. Per-Channel ENOB for 100-Pin PZP

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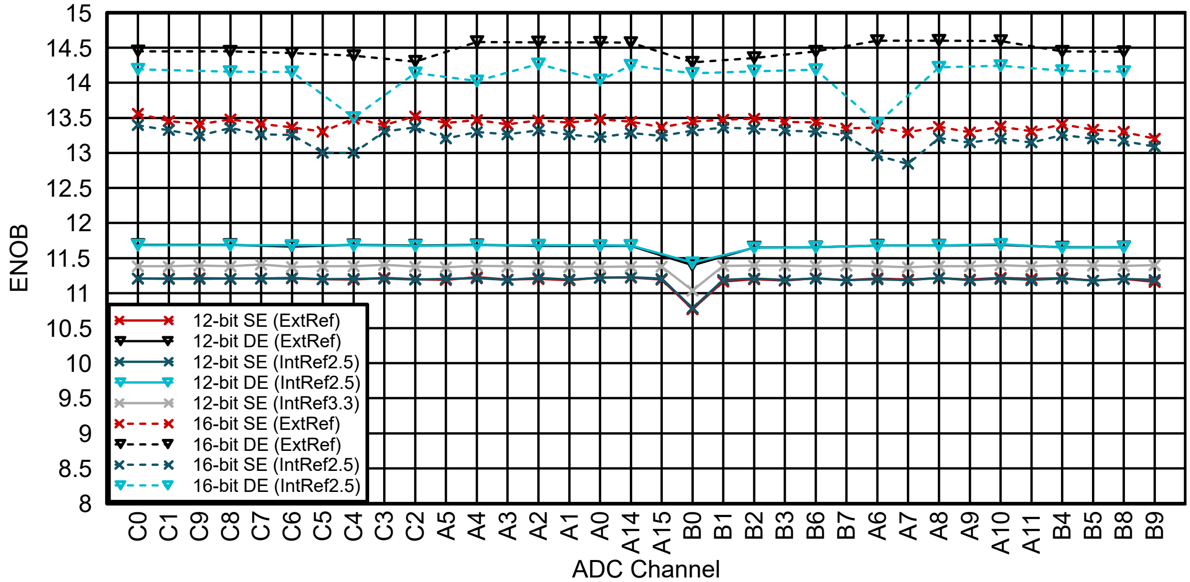

Figure 6-53. Per-Channel ENOB for 169-Ball NMR

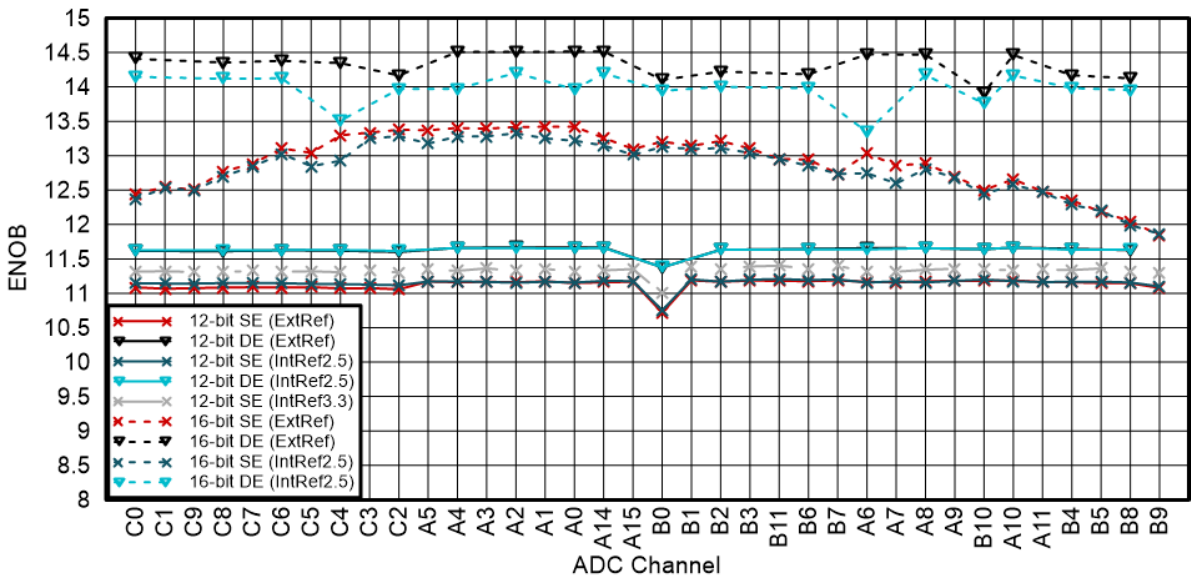

Figure 6-54. Per-Channel ENOB for 176-Pin PTP

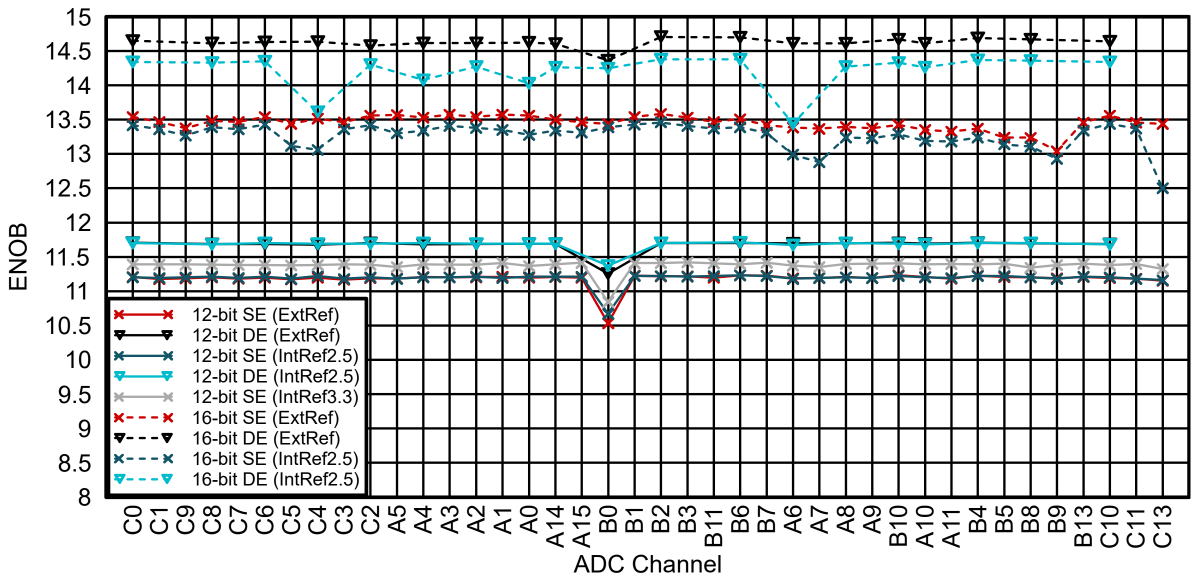

Figure 6-55. Per-Channel ENOB for 256-Ball ZEJ

6.13.2.2.10 ADC Input Models

The ADC input characteristics are given by Table 6-17, Table 6-18, Figure 6-56, and Figure 6-57.

Table 6-17. Single-Ended Input Model Parameters (12-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-21 to Table 6-24
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	14.5 pF
R_s	Nominal source impedance	50 Ω

Table 6-18. Single-Ended Input Model Parameters (16-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-21 to Table 6-24
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	32.5 pF
R_s	Nominal source impedance	50 Ω

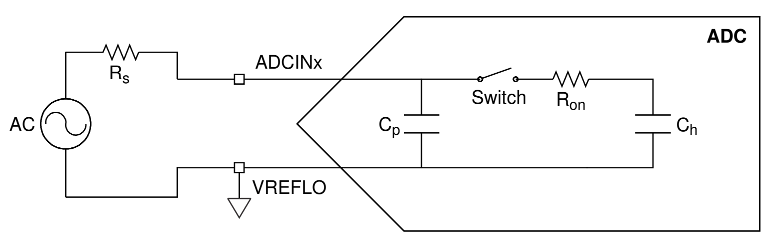

Figure 6-56. Single-Ended Input Model

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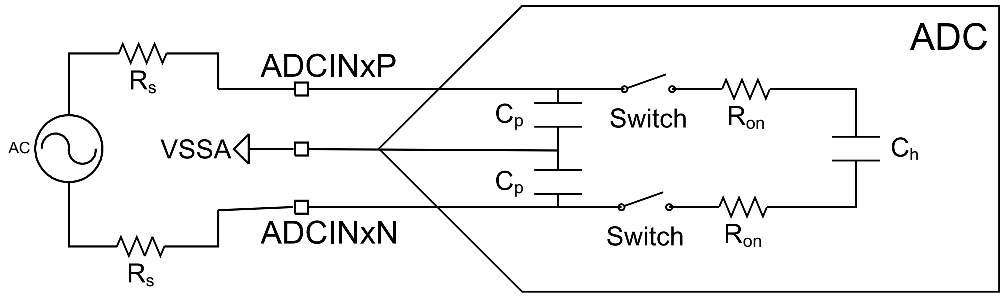

Figure 6-57. Differential Input Model

Table 6-19. Differential Input Model Parameters (12-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-21 to Table 6-24
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	7.5 pF
R_s	Nominal source impedance	50 Ω

Table 6-20. Differential Input Model Parameters (16-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-21 to Table 6-24
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

These input models should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the Choosing an Acquisition Window Duration section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*. For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Report.

Table 6-21. Per-Channel Parasitic Capacitance for 256-Ball ZEJ nFBGA

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0	4.6	7.1
A1	2.7	5.2
A2	2.7	5.2
A3	2.7	5.2
A4	2.1	4.6
A5	2.3	4.8
A6	2	4.5
A7	2.7	5.2
A8	2.6	5.1
A9	2.8	5.3
A10	2.7	5.2
A11	2.6	5.1
A14,B14,C14	3.9	6.4
A15,B15,C15	3.2	5.7
B0	11.5	14
B1	3.1	5.6

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Table 6-21. Per-Channel Parasitic Capacitance for 256-Ball ZEJ nFBGA (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
B2	2.4	4.9
B3	2.7	5.2
B4	2.6	5.1
B5	2.1	4.6
B6	2.4	4.9
B7	2.6	5.1
B8	2.6	5.1
B9	2.5	5
B10	3.6	6.1
B11	2.8	5.3
B13	1.9	4.4
C0	2.7	5.2
C1	2.7	5.2
C2	2.7	5.2
C3	3.1	5.6
C4	2.3	4.8
C5	2.5	5
C6	1.8	4.3
C7	2.3	4.8
C8	1.1	3.6
C9	1.2	3.7
C10	1.1	3.6
C11	1.7	4.2
C13	1.9	4.4

Table 6-22. Per-Channel Parasitic Capacitance for 176-Pin PTP HLQFP

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0	4.6	7.1
A1	2.7	5.2
A2	2.7	5.2
A3	2.7	5.2
A4	2.1	4.6
A5	2.3	4.8
A6	2	4.5
A7	2.7	5.2
A8	2.6	5.1
A9	2.8	5.3
A10	2.7	5.2
A11	2.6	5.1
A14,B14,C14	3.9	6.4
A15,B15,C15	3.2	5.7
B0	11.5	14
B1	3.1	5.6

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Table 6-22. Per-Channel Parasitic Capacitance for 176-Pin PTP HLQFP (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
B2	2.4	4.9
B3	2.7	5.2
B4	2.6	5.1
B5	2.1	4.6
B6	2.4	4.9
B7	2.6	5.1
B8	2.6	5.1
B9	2.5	5
B10	3.6	6.1
B11	2.8	5.3
C0	2.7	5.2
C1	2.7	5.2
C2	2.7	5.2
C3	3.1	5.6
C4	2.3	4.8
C5	2.5	5
C6	1.8	4.3
C7	2.3	4.8
C8	1.1	3.6
C9	1.2	3.7

Table 6-23. Per-Channel Parasitic Capacitance for 169-Ball NMR nFBGA

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0	4.6	7.1
A1	2.7	5.2
A2	2.7	5.2
A3	2.7	5.2
A4	2.1	4.6
A5	2.3	4.8
A6	2	4.5
A7	2.7	5.2
A8	2.6	5.1
A9	2.8	5.3
A10	2.7	5.2
A11	2.6	5.1
A14,B14,C14	3.9	6.4
A15,B15,C15	3.2	5.7
B0	11.5	14
B1	3.1	5.6
B2	2.4	4.9
B3	2.7	5.2
B4	2.6	5.1
B5	2.1	4.6

Table 6-23. Per-Channel Parasitic Capacitance for 169-Ball NMR nFBGA (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
B6	2.4	4.9
B7	2.6	5.1
B8	2.6	5.1
B9	2.5	5
C0	2.7	5.2
C1	2.7	5.2
C2	2.7	5.2
C3	3.1	5.6
C4	2.3	4.8
C5	2.5	5
C6	1.8	4.3
C7	2.3	4.8
C8	1.1	3.6
C9	1.2	3.7

Table 6-24. Per-Channel Parasitic Capacitance for 100-Pin PZP HTQFP

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0	4.6	7.1
A1	2.7	5.2
A2	2.7	5.2
A3	2.7	5.2
A4	2.1	4.6
A5	2.3	4.8
A6	2	4.5
A10	2.7	5.2
A11	2.6	5.1
A14,B14,C14	3.9	6.4
A15,B15,C15	3.2	5.7
B0	11.5	14
B1	3.1	5.6
B2	2.4	4.9
B3	2.7	5.2
B6	2.4	4.9
B7	2.6	5.1
C0	2.7	5.2
C1	2.7	5.2
C2	2.7	5.2
C3	3.1	5.6
C4	2.3	4.8
C5	2.5	5
C6	1.8	4.3

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6.13.2.2.11 ADC Timing Diagrams

The following diagrams show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-25 lists the descriptions of the ADC timing parameters. Table 6-26 and Table 6-27 list the ADC timings.

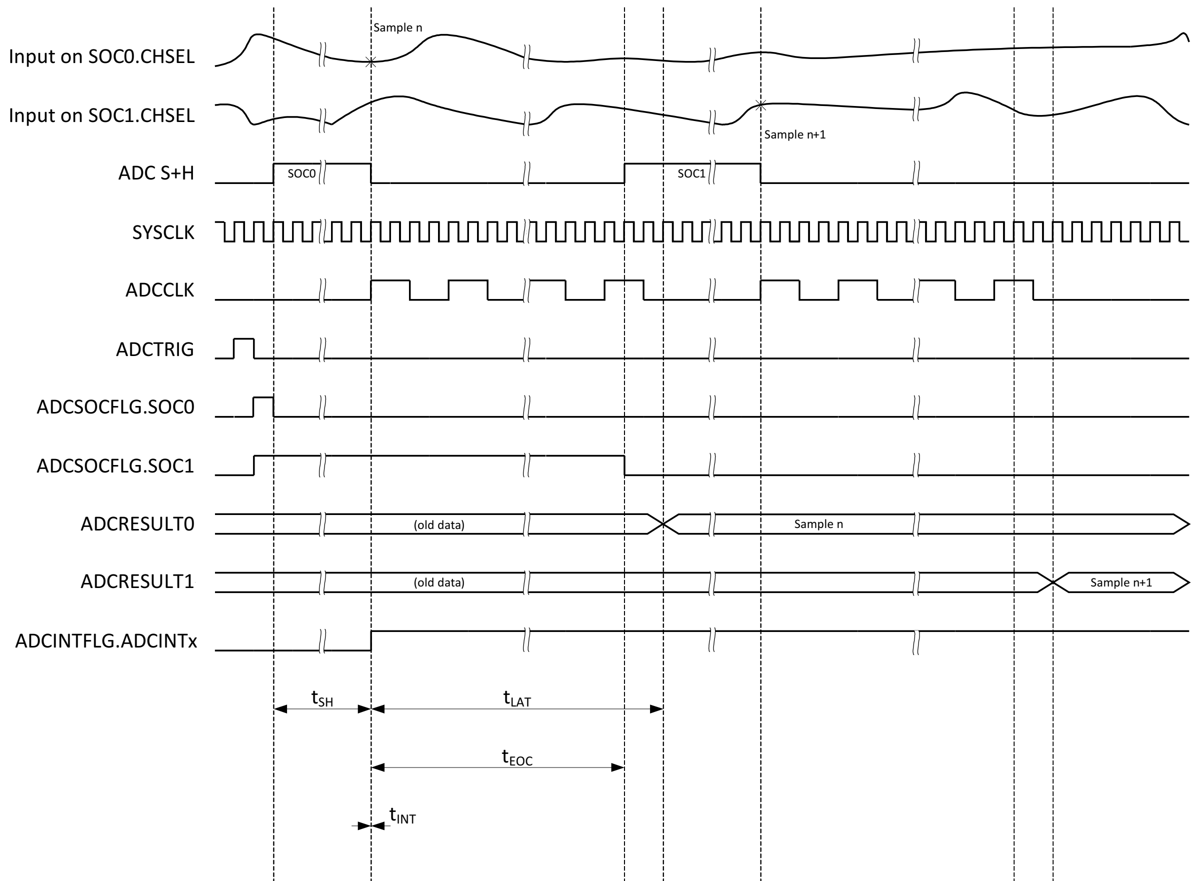

Figure 6-58. ADC Timings for 12-bit Mode in Early Interrupt Mode

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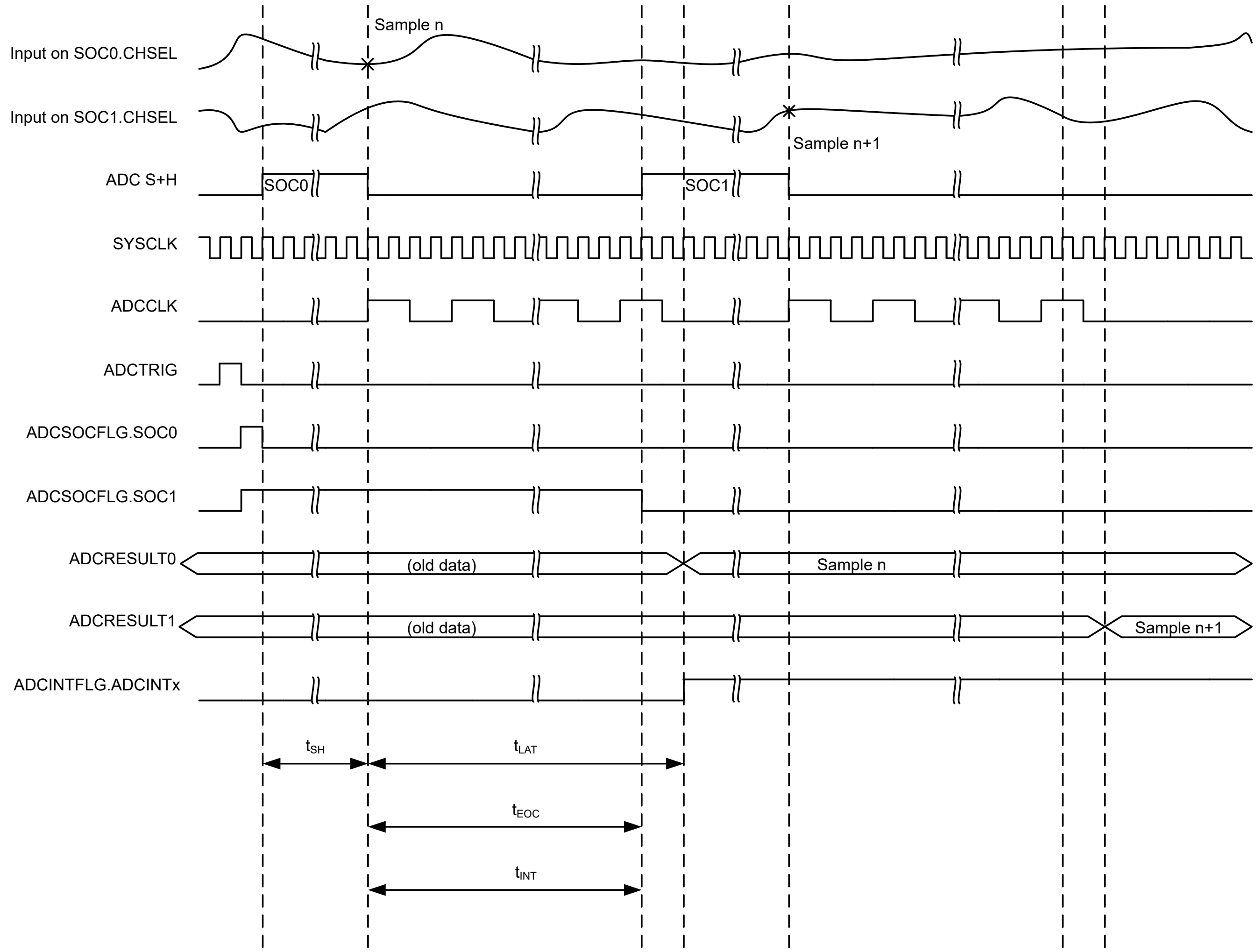

Figure 6-59. ADC Timings for 12-bit Mode in Late Interrupt Mode

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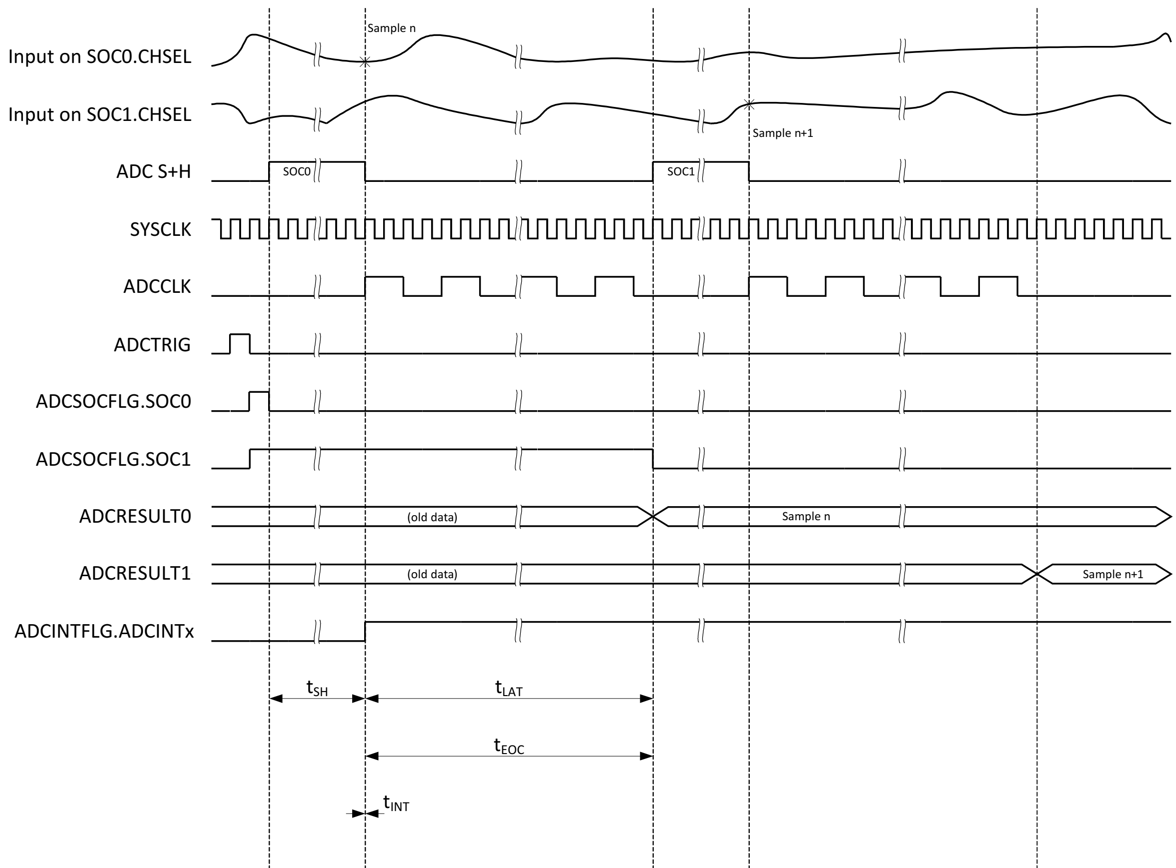

Figure 6-60. ADC Timings for 16-bit Mode in Early Interrupt Mode

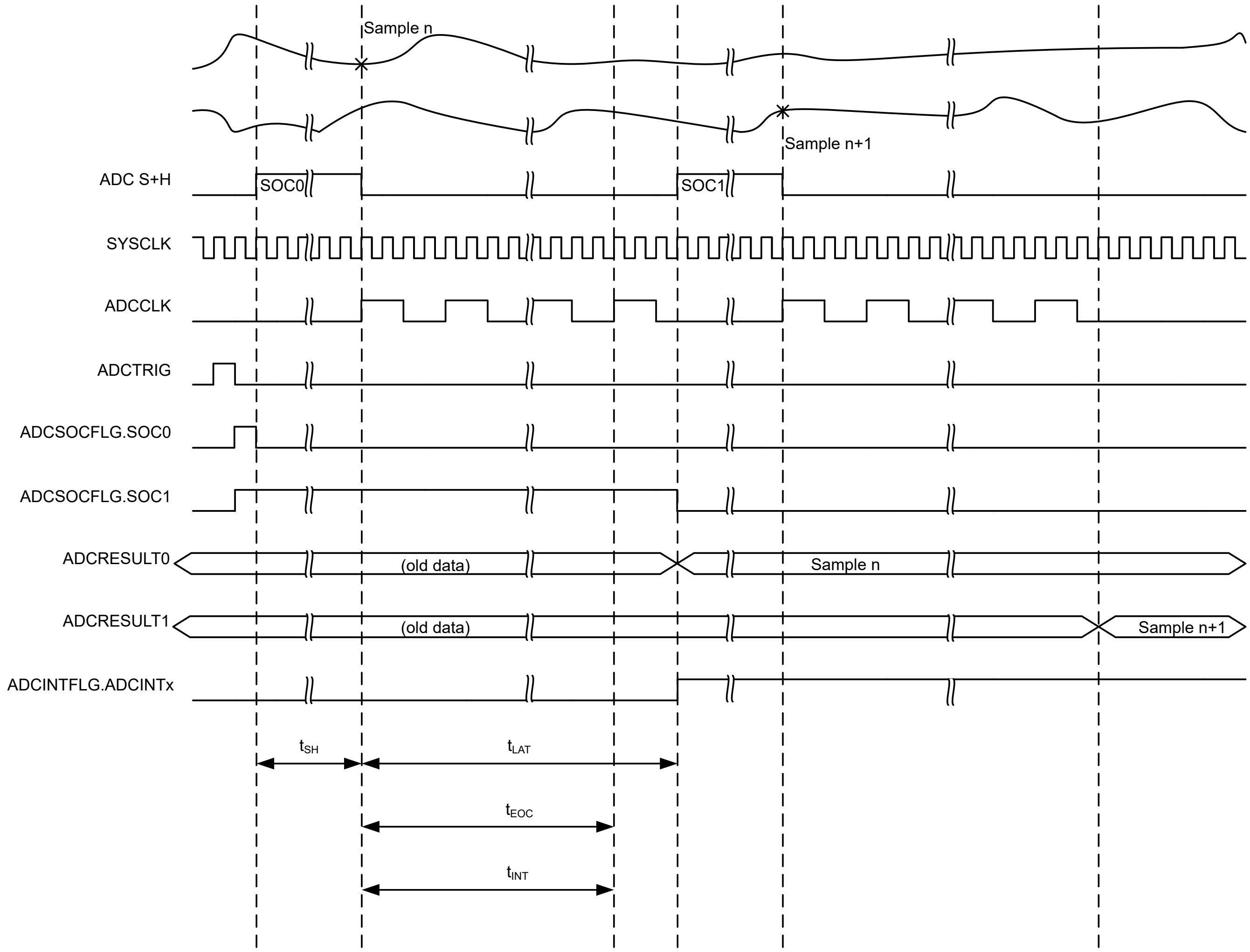

Figure 6-61. ADC Timings for 16-bit Mode in Late Interrupt Mode (SYSCLK Cycles)

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Table 6-25. ADC Timing Parameter Descriptions

PARAMETER	DESCRIPTION
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs. **Note:** The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned.
t_{EOC}	The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. In 16-bit mode, this coincides with the latching of the conversion results, while in 12-bit mode, the subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal. If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read). If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there is a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR or trigger the DMA exactly when the sample is ready.
t_{DMA}	The time from the end of the S+H window until a DMA read of the ADC conversion result is triggered, when ADCCTL1.TDMAEN = 1. If TDMAEN is set to 0, then the DMA trigger occurs at T_{INT}. In certain conditions, the ADCINT flag can be set before the ADCRESULT value is latched. To make sure that the DMA read occurs after the ADCRESULT value has been latched, write 1 to ADCCTL1.TDMAEN to enable DMA timings.

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Table 6-26. ADC Timings in 12-bit Mode

ADCCLK Prescale		SYSCLK Cycles				
ADCCTL2. PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)	t_{DMA}
0	1	11	13	0	11	13
2	2	21	23	0	21	23
3	2.5	26	28	0	26	28
4	3	31	34	0	31	34
5	3.5	36	39	0	36	39
6	4	41	44	0	41	44
7	4.5	46	49	0	46	49
8	5	51	55	0	51	55
9	5.5	56	60	0	56	60
10	6	61	65	0	61	65
11	6.5	66	70	0	66	70
12	7	71	76	0	71	76
13	7.5	76	81	0	76	81
14	8	81	86	0	81	86
15	8.5	86	91	0	86	91

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

Table 6-27. ADC Timings in 16-bit Mode

ADCCLK Prescale		SYSCLK Cycles				
ADCCTL2. PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)	t_{DMA}
0	1	31	32	0	31	32
2	2	60	61	0	60	61
3	2.5	75	75	0	75	75
4	3	90	91	0	90	91
5	3.5	104	106	0	104	106
6	4	119	120	0	119	120
7	4.5	134	134	0	134	134
8	5	149	150	0	149	150
9	5.5	163	165	0	163	165
10	6	178	179	0	178	179
11	6.5	193	193	0	193	193
12	7	208	209	0	208	209
13	7.5	222	224	0	222	224
14	8	237	238	0	237	238
15	8.5	252	252	0	252	252

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

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6.13.3 Temperature Sensor

6.13.3.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the Temperature Sensor Characteristics table.

6.13.3.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	Internal reference (-40°C to 30°C)	-11	±2	11	°C
		Internal reference (30°C to 85°C)	-4	±2	7	°C
		Internal reference (85°C to 125°C)	-3	±2	10	°C
		Internal reference (125°C to 140°C)	-2	±2	12	°C
		External reference (-40°C to 30°C)	-4	±2	7	°C
		External reference (30°C to 140°C)	-3	±2	7	°C
$t_{startup}$	Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)			500		µs
t_{acq}	ADC acquisition time		450			ns

6.13.4 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs, and two digital filters. The subsystem also includes two ramp generators. The ramp generators ramp up and down. Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the *Analog Subsystem* chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. Two ramp generator circuits are optionally available to control the reference 12-bit DAC values for the high and low comparators in the subsystem. The DAC along with a wrapper can be used to generate a ramp which is used for slope compensation in Peak Current Mode Control (PCMC) and other applications. The subsystem also works with the EPWM to support Diode Emulation Mode.

Each CMPSS includes:

- Two analog comparators
- Two independently programmable reference 12-bit DACs
- Dual decrementing/incrementing ramp generators
- Two digital filters with max filter clock prescale of 2^{24}
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- External connection to CMPSS filters
- Diode emulation support
- Supports connection with ePWM for diode emulation
- Ramp generator prescaler
- Wake-up from standby and halt LPM (Low Power Modes) triggered by CMPSS trip outputs

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6.13.4.1 CMPSS Connectivity Diagram

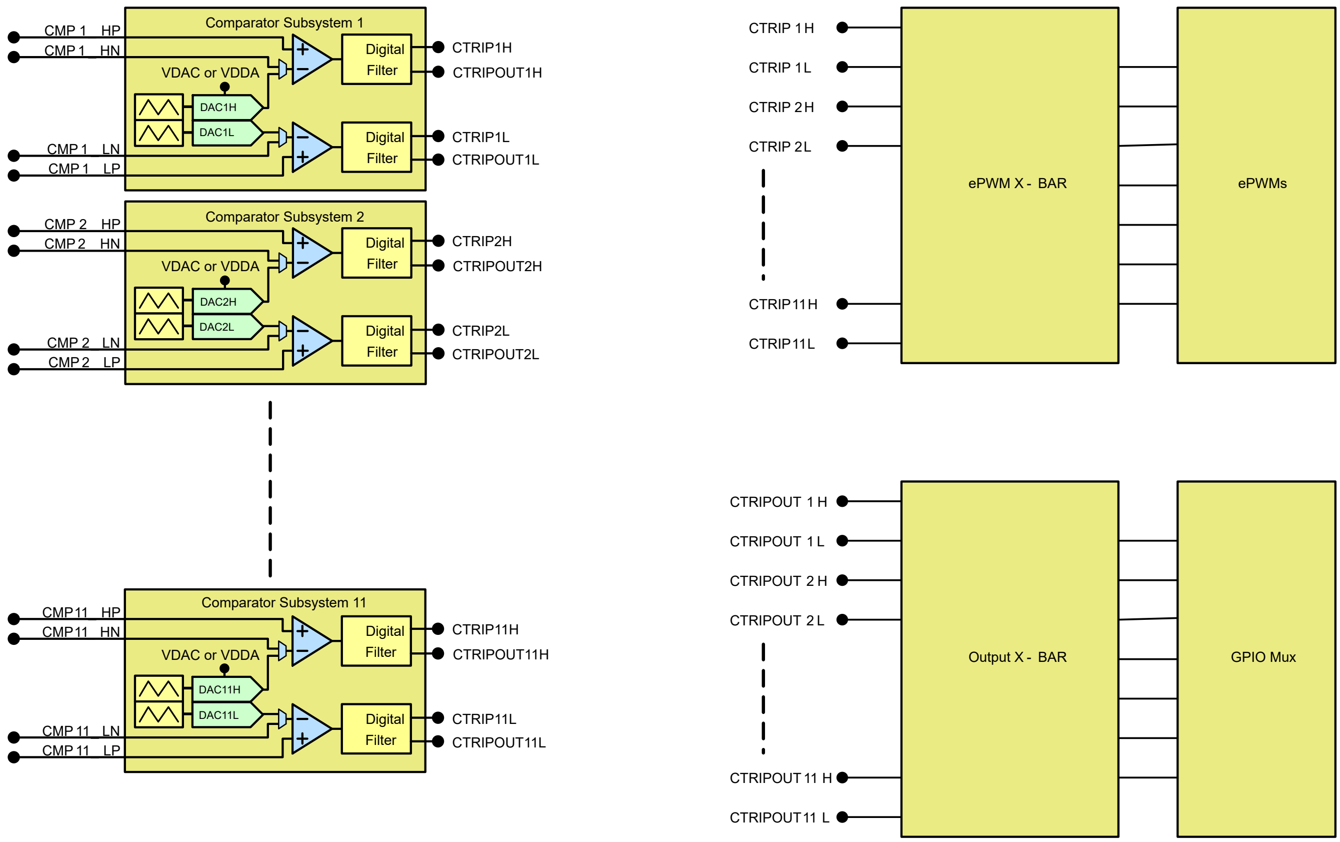

Figure 6-62. CMPSS Connectivity

6.13.4.2 Block Diagram

The block diagram for the CMPSS is shown in Figure 6-63.

- CTRIPx(x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. See the *Enhanced Pulse Width Modulator (ePWM)* chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* for more details on the ePWM X-BAR mux configuration.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the *General-Purpose Input/Output (GPIO)* chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* for more details on the Output X-BAR mux configuration.

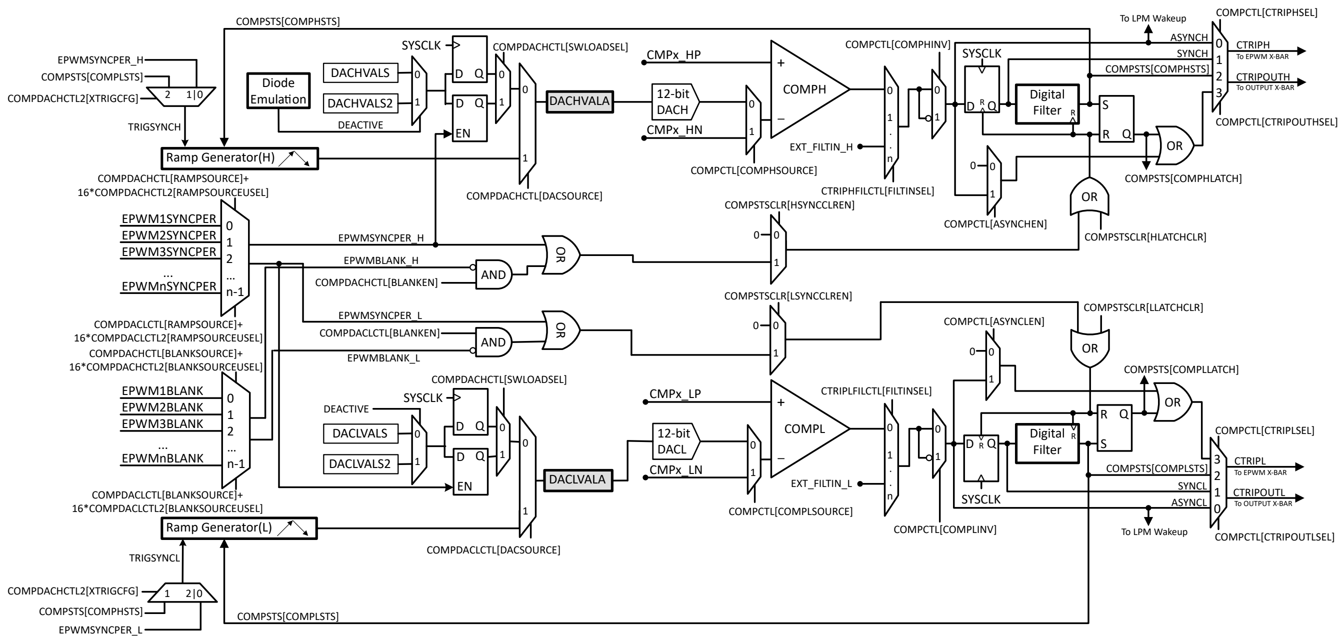

Figure 6-63. CMPSS Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. The reference 12-bit DAC output is internal only and cannot be observed externally. The reference 12-bit DAC is illustrated in Figure 6-64.

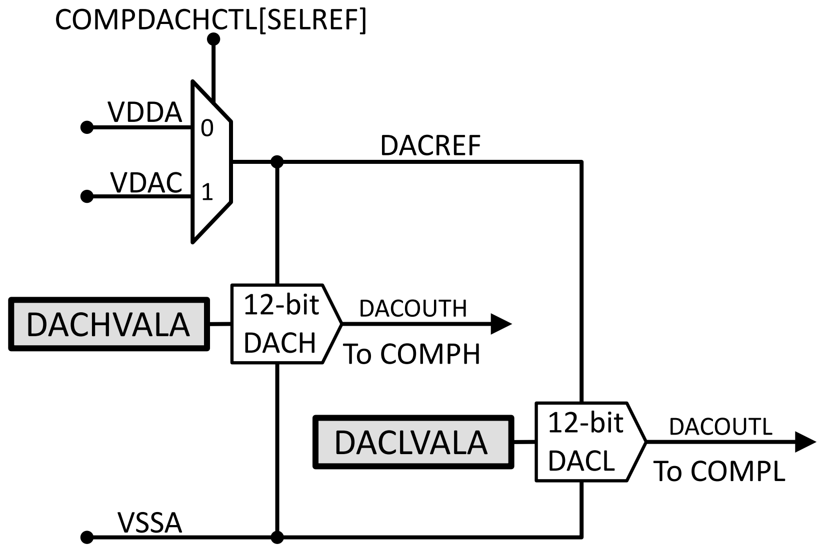

Figure 6-64. Reference DAC Block Diagram

6.13.4.3 CMPSS Electrical Data and Timing

6.13.4.3.1 Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time				500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Low common mode, inverting input set to 50mV	–20		20	mV
Hysteresis[(1)]		1x	4	12	20	LSB
		2x	17	24	33	
		3x	25	36	50	
		4x	30	48	67	
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)		Step response		21	60	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		ns
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

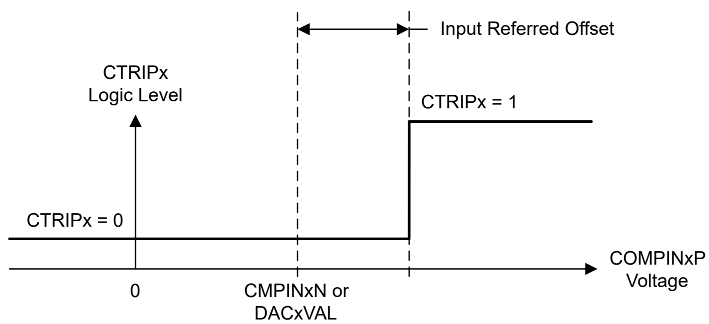

Figure 6-65. CMPSS Comparator Input Referred Offset

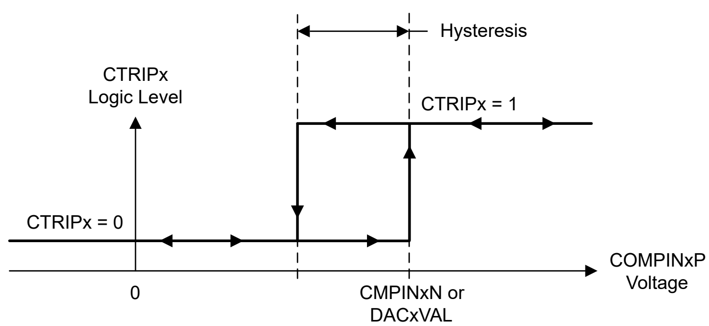

Figure 6-66. CMPSS Comparator Hysteresis

6.13.4.3.2 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		VDDA	V
	External reference	0		VDAC[(4)]	
Static offset error[(1)]		–25		25	mV

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6.13.4.3.2 CMPSS DAC Static Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static gain error[(1)]		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance[(2)]	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time[(2)]				200	ns
VDAC reference voltage	When VDAC is reference	2.4	2.5 or 3.0	VDDA	V
VDAC load[(3)]	When VDAC is reference	6	8	10	kΩ

(1) Includes comparator input referred errors.
(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(3) Per active CMPSS module.
(4) The maximum output voltage is VDDA when VDAC > VDDA.

6.13.4.3.3 CMPSS Illustrative Graphs

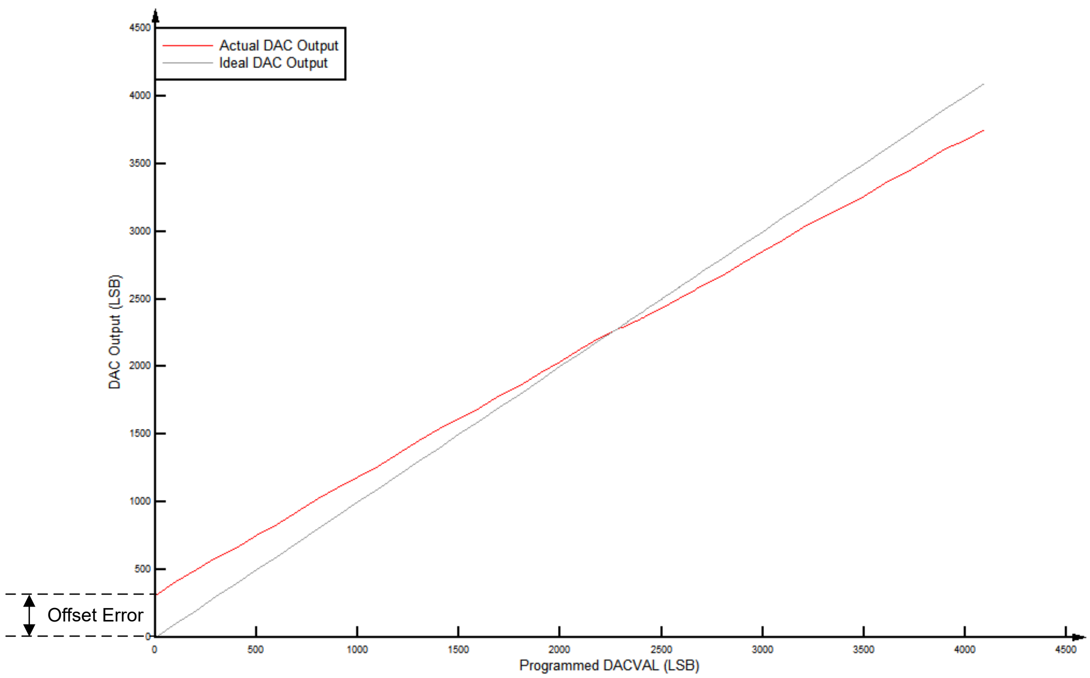

Figure 6-67. CMPSS DAC Static Offset

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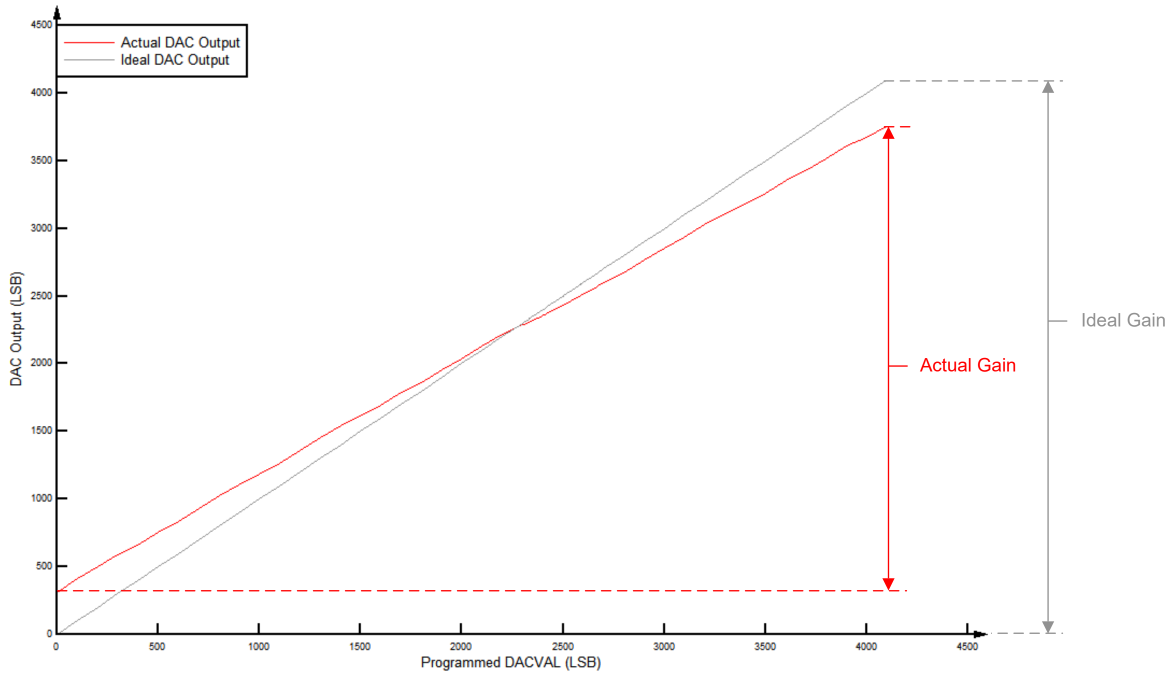

Figure 6-68. CMPSS DAC Static Gain

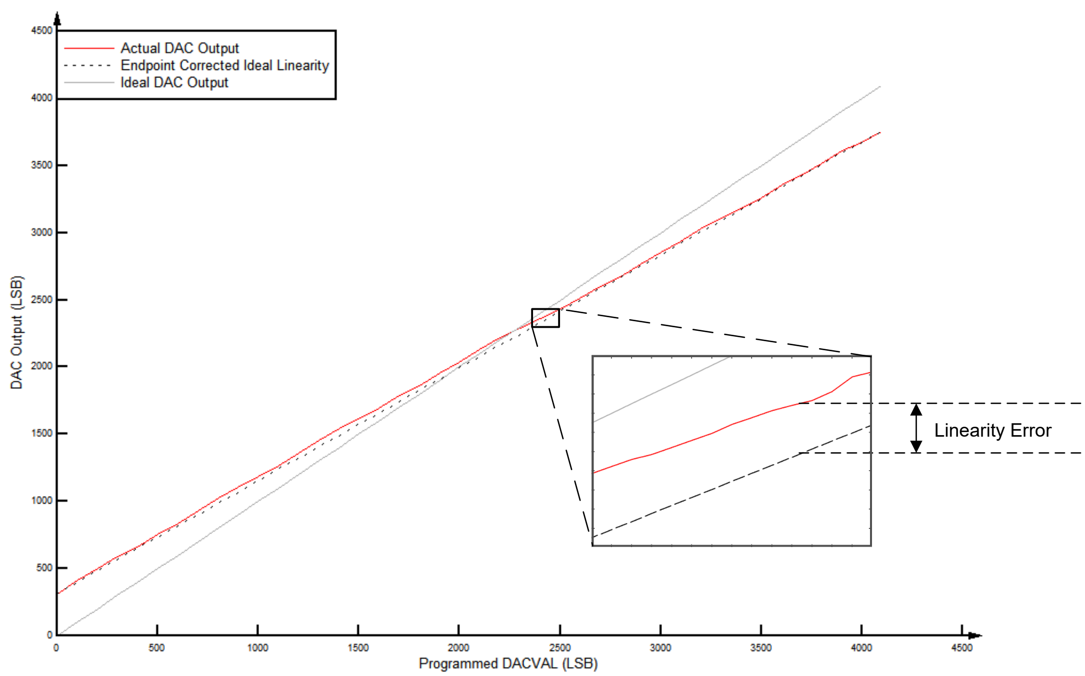

Figure 6-69. CMPSS DAC Static Linearity

6.13.4.3.4 CMPSS DAC Dynamic Error

When using the ramp generator to control the internal DAC, the step size can vary based on the application need. Since the step size of the DAC is less than a full scale transition, the settling time is improved from the electrical specification listed in the *CMPSS DAC Static Electrical Characteristics* table. The equation below and Figure 6-70 can give guidance on the expected voltage error from ideal based on different RAMPxSTEPVALA values.

$$DYNAMICERROR = (m \times RAMPxSTEPVALA) + b \quad (3)$$

Table 6-28. DAC Max Dynamic Error Terms

EQUATION PARAMETER	MIN (LSB)	MAX (LSB)
m	0.167	0.30
b	3.7	5.6

Note

Above error terms are based on the max SYSCLK of the target device. If operating below the max SYSCLK then the "m" error term should be scaled accordingly.

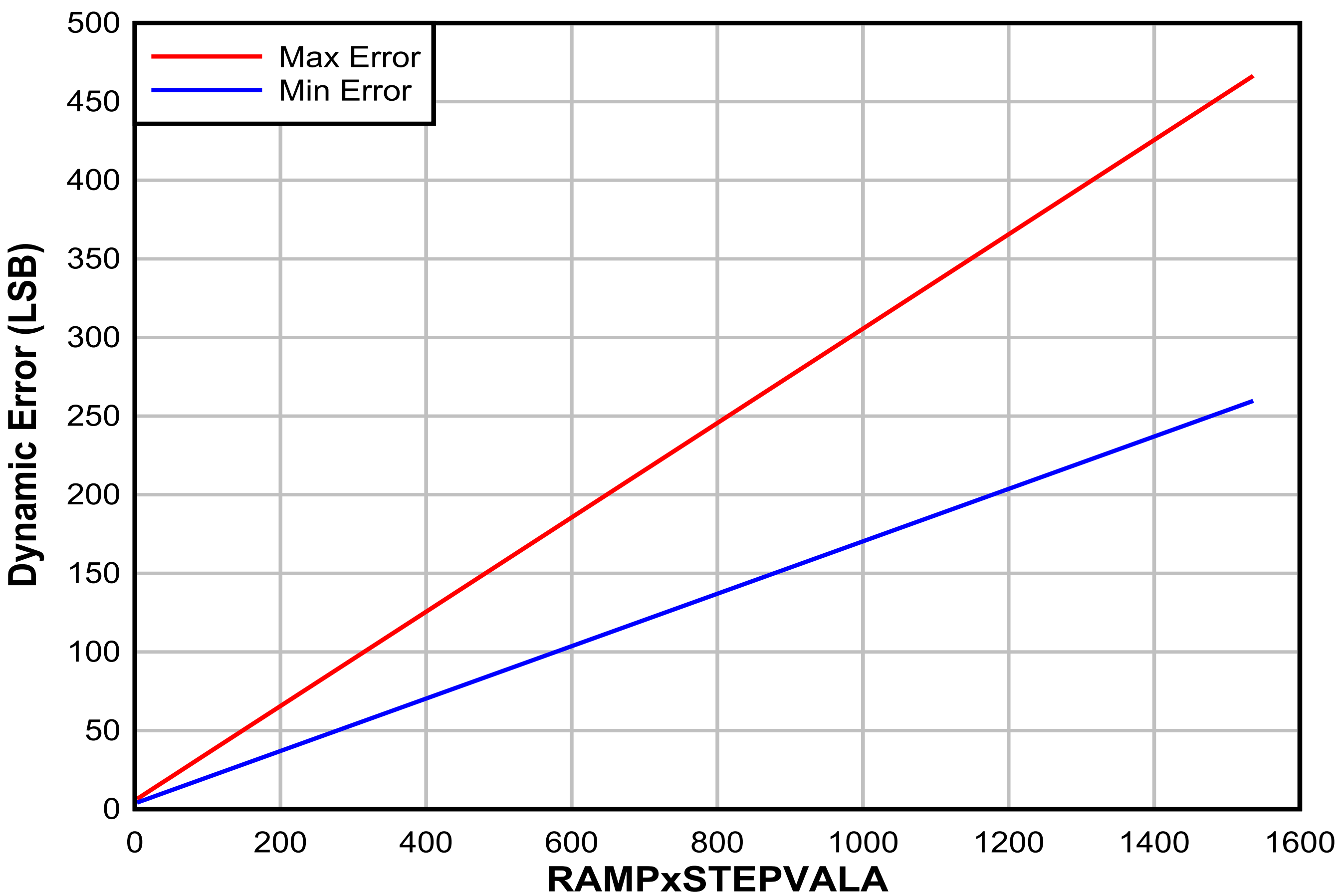

Figure 6-70. CMPSS DAC Dynamic Error

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6.13.5 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that can drive an external load. For driving even higher loads than typical, a trade-off can be made between load size and output voltage swing. For the load conditions of the buffered DAC, see the Buffered DAC Electrical Data and Timing section. The buffered DAC is a general-purpose DAC that can be used to generate a DC voltage or AC waveforms such as sine waves, square waves, triangle waves and so forth. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCO events.

Each buffered DAC has the following features:

- 12-bit resolution
- Selectable reference voltage source
- x1 and x2 gain modes when using internal VREFHI
- Ability to synchronize with EPWMSYNCPER

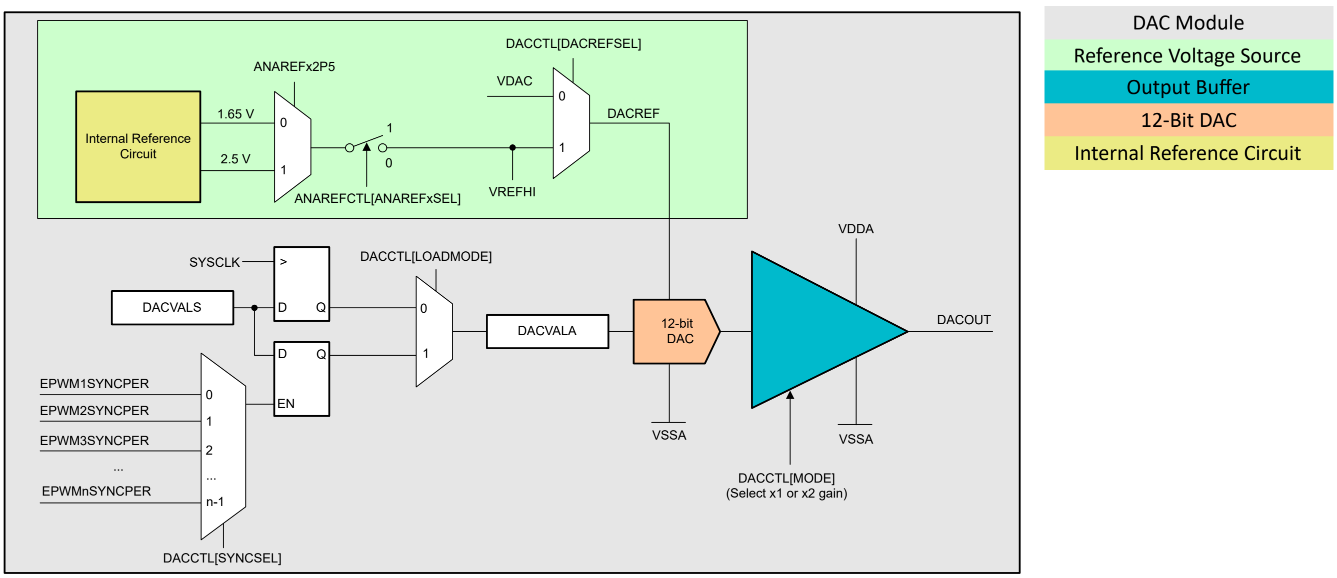

Figure 6-71. DAC Module Block Diagram

6.13.5.1 Buffered DAC Electrical Data and Timing

6.13.5.1.1 Buffered DAC Operating Conditions

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Resistive Load(2)		5			kΩ
C_L	Capacitive Load				100	pF
V_{OUT}	Valid Output Voltage Range(3)	R_L = 5 kΩ	0.3		VDDA – 0.3	V
		R_L = 1 kΩ	0.6		VDDA – 0.6	V
Reference Voltage(4)		VDAC or VREFHI	2.4	2.5 or 3.0	VDDA	V

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
(3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(4) For best PSRR performance, VDAC or VREFHI should be less than VDDA.

6.13.5.1.2 Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Resolution				12		bits
Load Regulation			–1		1	mV/V
Glitch Energy				1.5		V-ns
Voltage Output Settling Time Full-Scale		Settling to 2 LSBs after 0.3V-to-3V transition			2	µs
Voltage Output Settling Time 1/4th Full-Scale		Settling to 2 LSBs after 0.3V-to-0.75V transition			1.6	µs
Voltage Output Slew Rate		Slew rate from 0.3V-to-3V transition	2.8		4.5	V/µs
Load Transient Settling Time		5-kΩ Load			328	ns
		1-kΩ Load			557	ns
Reference Input Resistance(2)		VDAC or VREFHI	160	200	240	kΩ
TPU	Power Up Time	External Reference mode			500	µs
		Internal Reference mode			5000	µs
DC Characteristics						
Offset	Offset Error	Midpoint	–10		10	mV
Gain	Gain Error(3)		–2.5		2.5	% of FSR
DNL	Differential Non Linearity(4)	Endpoint corrected	–1	±0.4	1	LSB
INL	Integral Non Linearity	Endpoint corrected	–5	±2	5	LSB
AC Characteristics						
Output Noise		Integrated noise from 100 Hz to 100 kHz		600		µVrms
		Noise density at 10 kHz		800		nVrms/√Hz
SNR	Signal to Noise Ratio	1 kHz, 200 KSPS		64		dB
THD	Total Harmonic Distortion	1 kHz, 200 KSPS		–64.2		dB
SFDR	Spurious Free Dynamic Range	1 kHz, 200 KSPS		66		dB
SINAD	Signal to Noise and Distortion Ratio	1 kHz, 200 KSPS		61.7		dB

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6.13.5.1.2 Buffered DAC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power Supply Rejection Ratio(5)	DC		70		dB
		100 kHz		30		dB

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) Per active Buffered DAC module.
(3) Gain error is calculated for linear output range.
(4) The DAC output is monotonic.
(5) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.

6.14 C28x Control Peripherals

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

6.14.1 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this chapter include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug. Note that this is not applicable for signal monitoring interrupts, which do not get affected by the event filter reset bit.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCNTRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- DMA trigger source
  - eCAPxDMA was added as a DMA trigger. CEVT[1-4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the eCAP section of the Enhanced Capture (eCAP) chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.
- EALLOW protection
  - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
  - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

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The capture functionality of the Type 3 eCAP is enhanced from the Type 2 eCAP with the following added features:

- Two signal monitoring units to monitor edge, pulse width, and period
  - Signal monitoring can optionally be tightly coupled with ePWM global load strobes and trip events
- Increased the number of multiplexed capture inputs from 128 to 256
- DMA event generation capability in PWM mode of operation
- ADC SOC generation capability, to trigger ADC conversion

6.14.1.1 eCAP Block Diagram

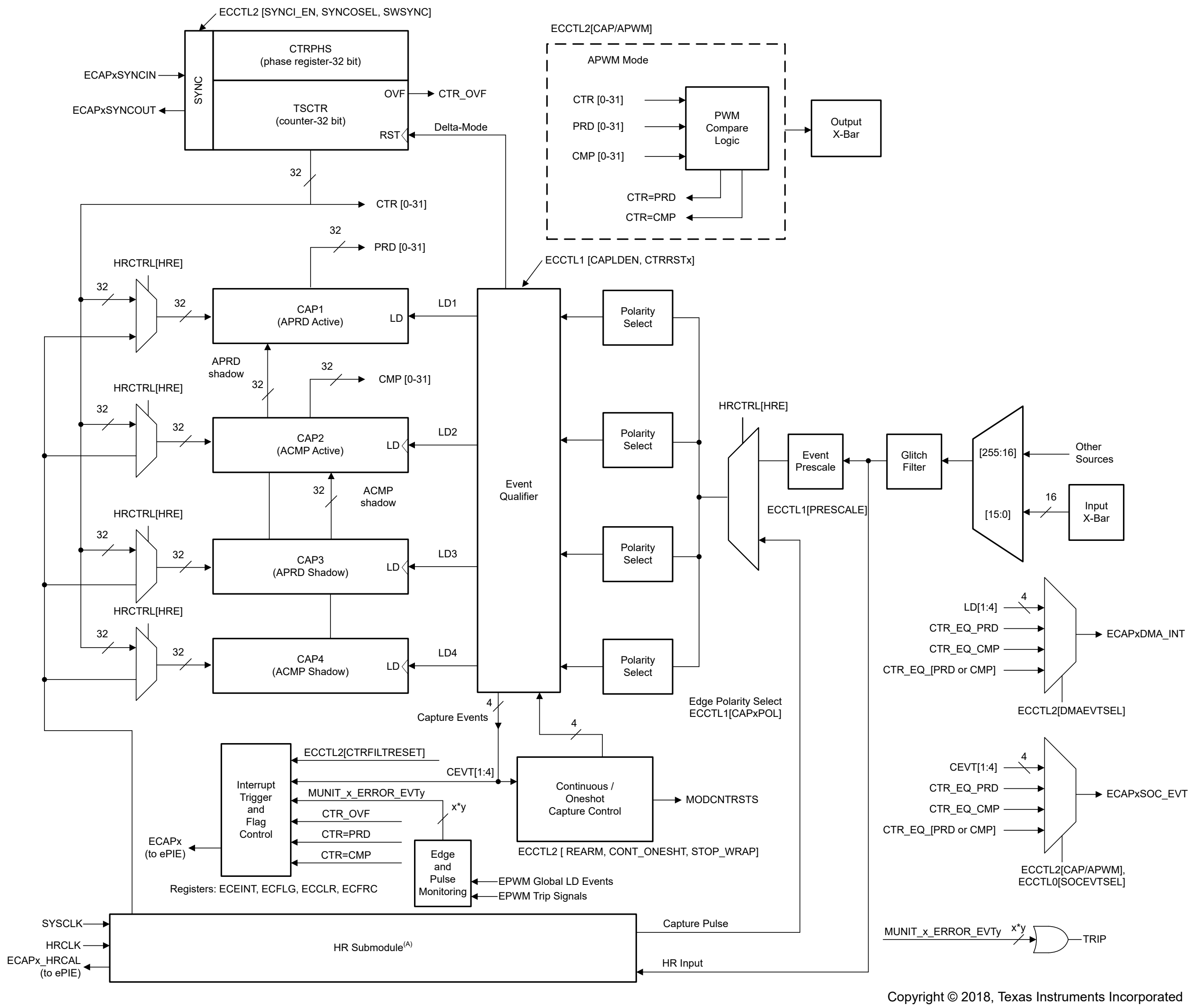

Figure 6-72. eCAP Block Diagram

6.14.1.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-73.

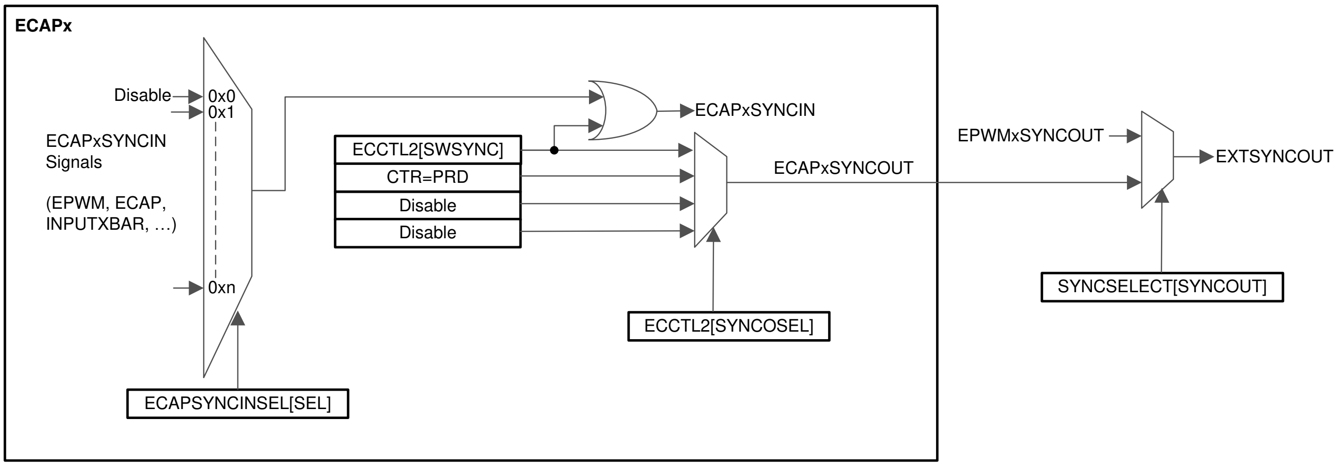

Figure 6-73. eCAP Synchronization Scheme

6.14.1.3 eCAP Electrical Data and Timing

6.14.1.3.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w\_(IQSW)}$			

6.14.1.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

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6.14.2 High-Resolution Capture (HRCAP)

The eCAP3 module can be configured as high-resolution capture (HRCAP) submodules. The HRCAP submodule measures the difference, in time, between pulses asynchronously to the system clock. This submodule is new to the eCAP Type 1 module, and features many enhancements over the Type 0 HRCAP module.

Applications for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty-cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning
- Flow measurements

The HRCAP submodule includes the following features:

- Pulse-width capture in either non-high-resolution or high-resolution modes
- Absolute mode pulse-width capture
- Continuous or "one-shot" capture
- Capture on either falling or rising edge
- Continuous mode capture of pulse widths in 4-deep buffer
- Hardware calibration logic for precision high-resolution capture
- All of the resources in this list are available on any pin using the Input X-BAR.

The HRCAP submodule includes one high-resolution capture channel in addition to a calibration block. The calibration block allows the HRCAP submodule to be continually recalibrated, at a set interval, with no “down time”. Because the HRCAP submodule now uses the same hardware as its respective eCAP, if the HRCAP is used, the corresponding eCAP will be unavailable.

Each high-resolution-capable channel has the following independent key resources.

- All hardware of the respective eCAP
- High-resolution calibration logic
- Dedicated calibration interrupt

6.14.2.1 eCAP and HRCAP Block Diagram

For the HRCAP Block Diagram, see the eCAP and HRCAP Block Diagram in the *Enhanced Capture (eCAP)* section.

6.14.2.2 HRCAP Electrical Data and Timing

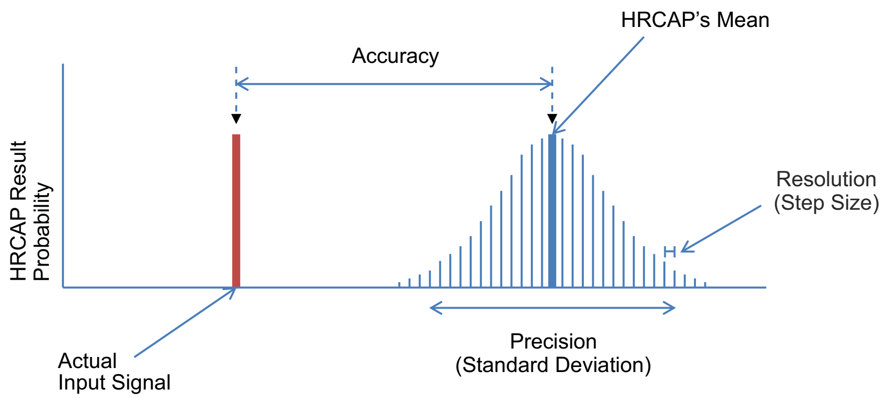
6.14.2.2.1 HRCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input pulse width		110			ns
Accuracy(1) (2) (3) (4)	Measurement length ≤ 5 µs		±390	540	ps
	Measurement length > 5 µs		±450	1450	ps
Standard deviation			See HRCAP Standard Deviation Characteristics figure		
Resolution			300		ps

(1) Value obtained using an oscillator of 100 PPM, oscillator accuracy directly affects the HRCAP accuracy.
(2) Measurement is completed using rising-rising or falling-falling edges
(3) Opposite polarity edges will have an additional inaccuracy due to the difference between V_{IH} and V_{IL}. This effect is dependent on the signal's slew rate.
(4) Accuracy only applies to time-converted measurements.

6.14.2.2.2 HRCAP Figure and Graph



A. The HRCAP has some variation in performance, this results in a probability distribution which is described using the following terms:
- Accuracy: The time difference between the input signal and the mean of the HRCAP's distribution.
- Precision: The width of the HRCAP's distribution, this is given as a standard deviation.
- Resolution: The minimum measurable increment.

Figure 6-74. HRCAP Accuracy Precision and Resolution

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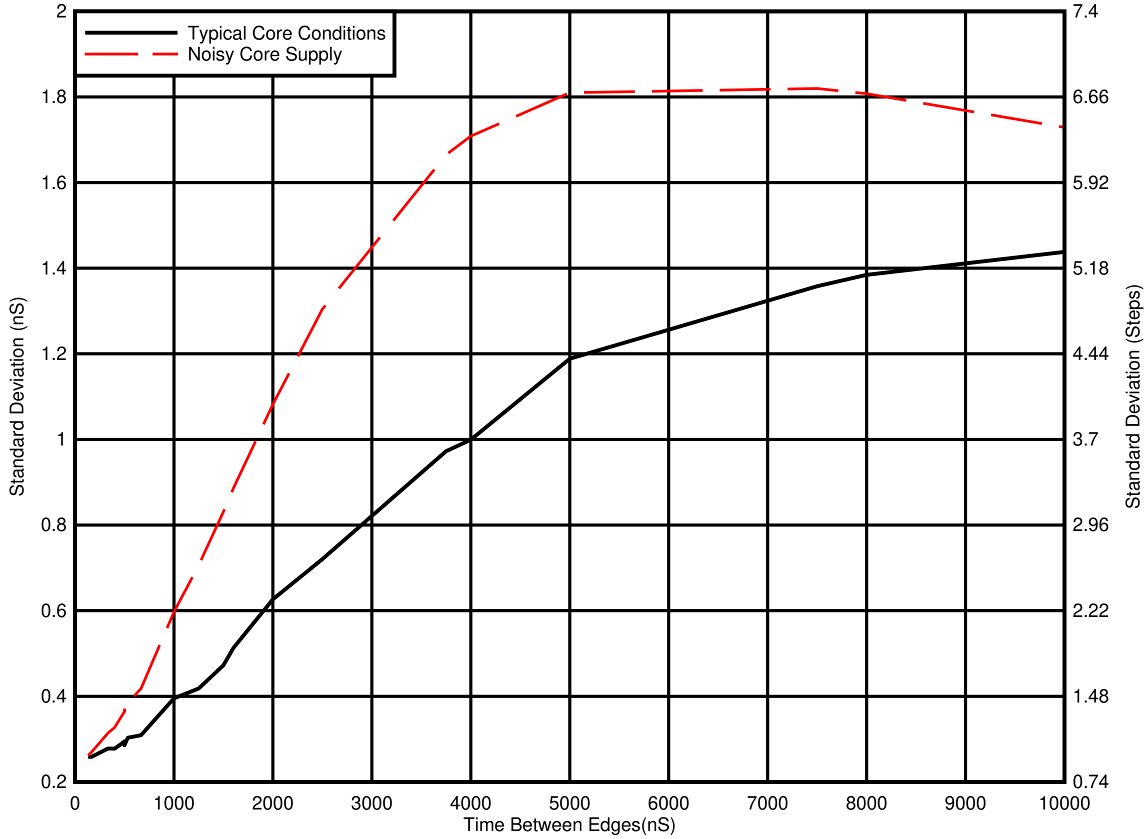

A. Typical core conditions: All peripheral clocks are enabled.
B. Noisy core supply: All core clocks are enabled and disabled with a regular period during the measurement.
C. Fluctuations in current and voltage on the 1.2-V rail cause the standard deviation of the HRCAP to rise. Care should be taken to ensure that the 1.2-V supply is clean, and that noisy internal events, such as enabling and disabling clock trees, have been minimized while using the HRCAP.

Figure 6-75. HRCAP Standard Deviation Characteristics

6.14.3 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities. ePWM type-5 enhancements include expansion of sync chain options, link and global load pulse selection flexibility, XCMP complex waveform generation, event capture capability, addition of diode emulation submodule and minimum dead-band and illegal combo logic submodule, and event trigger submodule enhancements to allow for unevenly spaced over-sampling of ePWM period.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-76 shows the ePWM module. Figure 6-77 shows the ePWM trip input connectivity.

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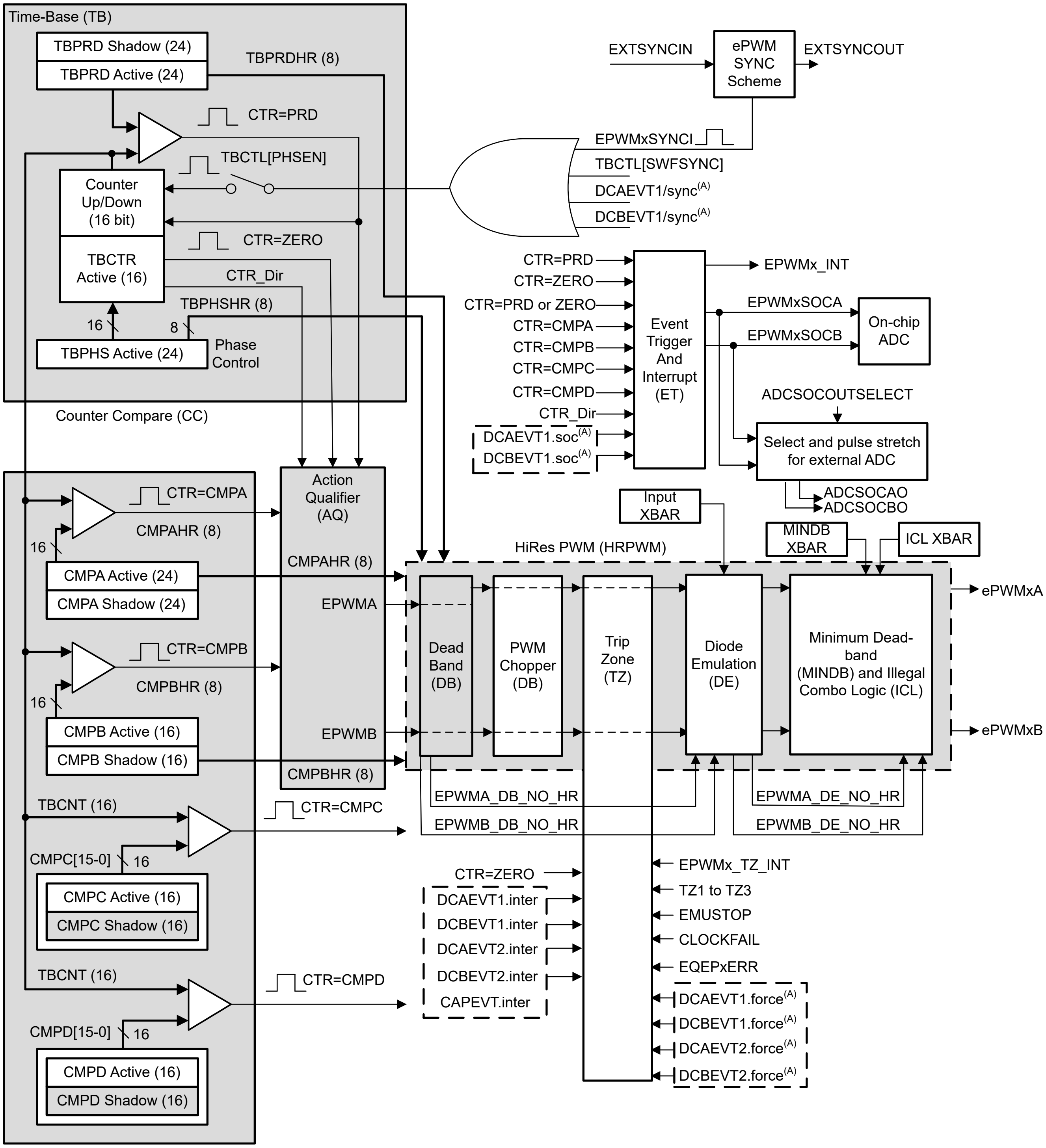

A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-76. ePWM Submodules and Critical Internal Signal Interconnects

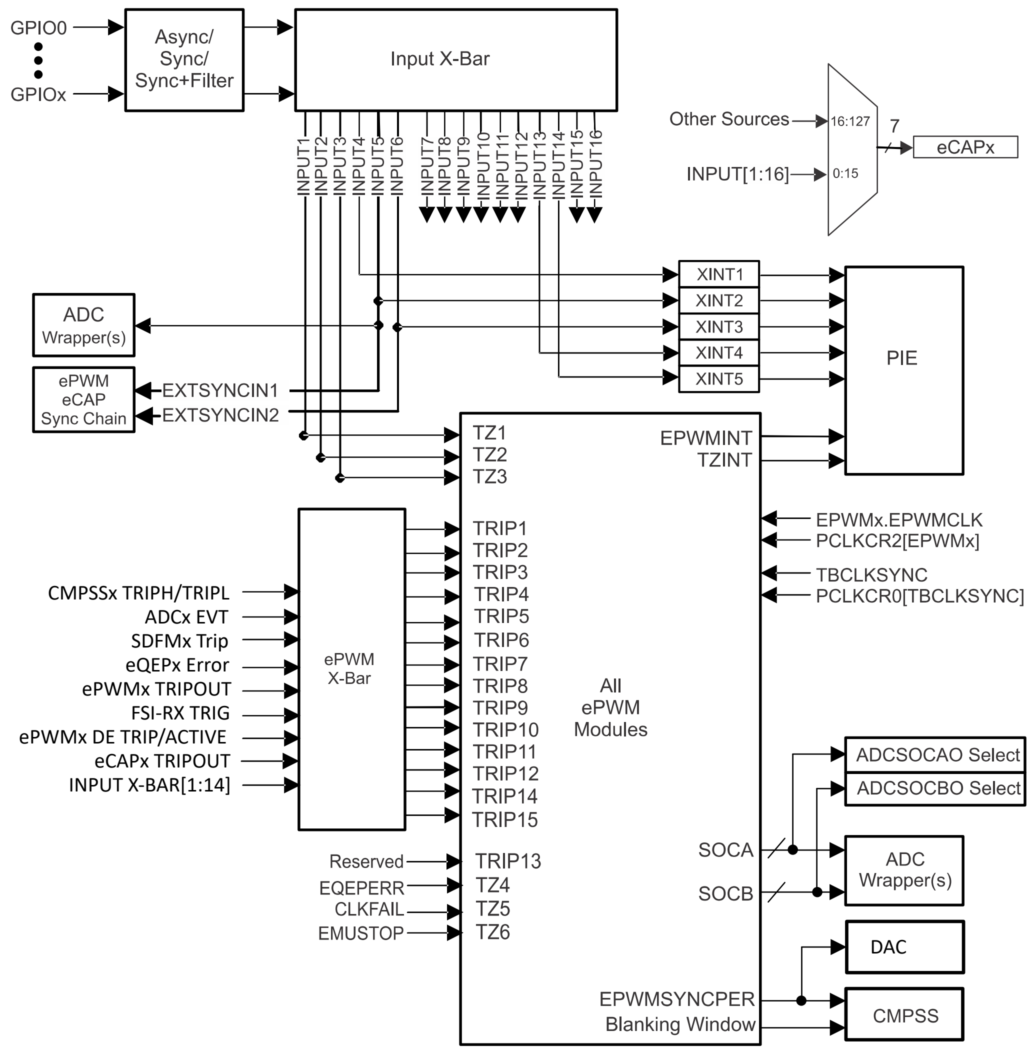

Figure 6-77. ePWM Trip Input Connectivity

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6.14.3.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Figure 6-78 shows the synchronization scheme.

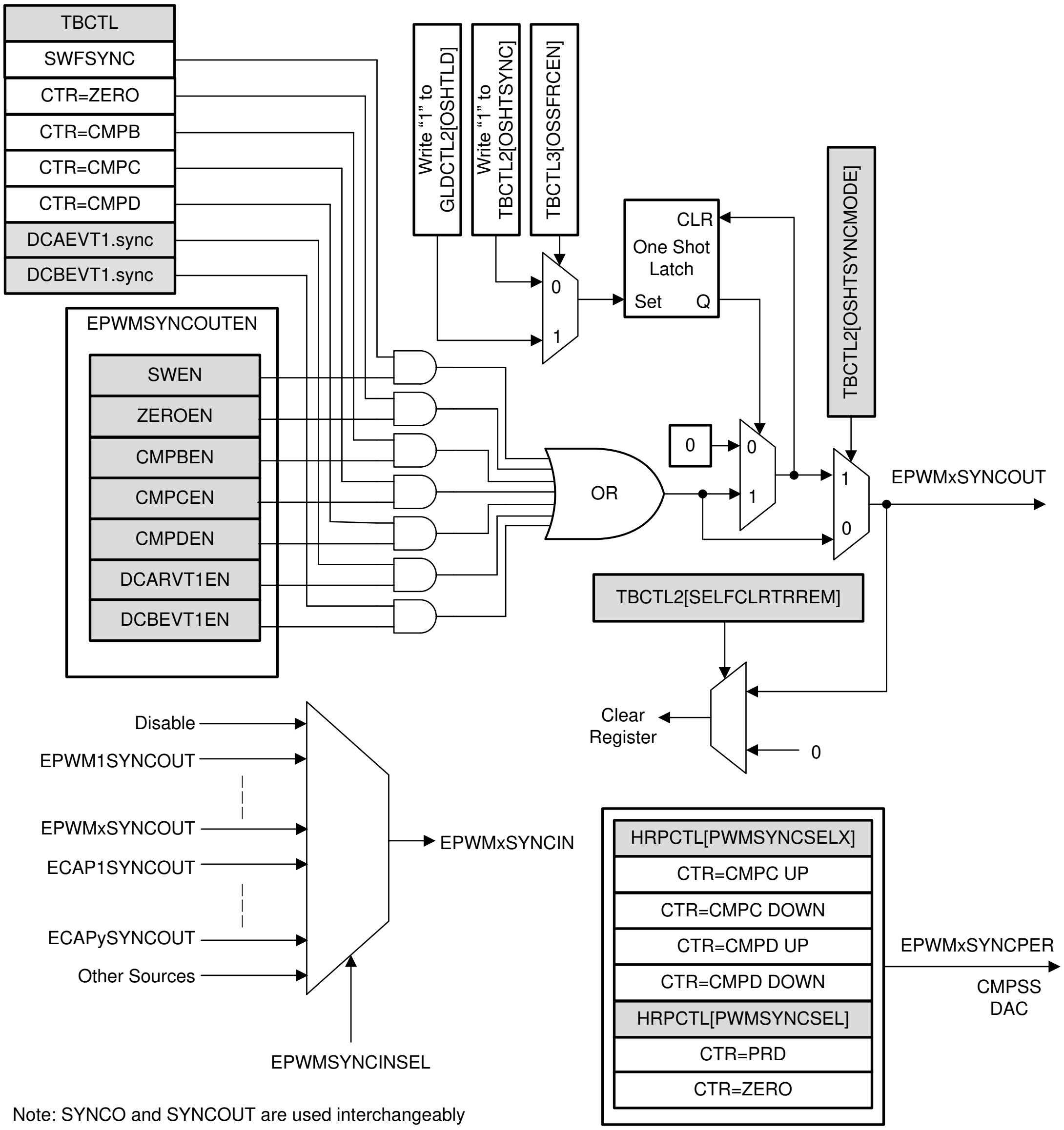


Figure 6-78. Synchronization Chain Architecture

6.14.3.2 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.14.3.2.1 ePWM Timing Requirements

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.14.3.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ\text{-}PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		30	ns
tskew	Skew of all ePWM outputs (Shortest Path)(2)		5.1	ns
tskew	Skew of all ePWM outputs (Longest Path)(2)		5.1	ns
tskew	Skew of all ePWM outputs through HRPWM (Shortest Path)(2)		5.1	ns
tskew	Skew of all ePWM outputs through HRPWM (Longest Path)(2)		5.1	ns

(1) 20-pF load on pin.
(2) The EPWMs have a similar configuration.

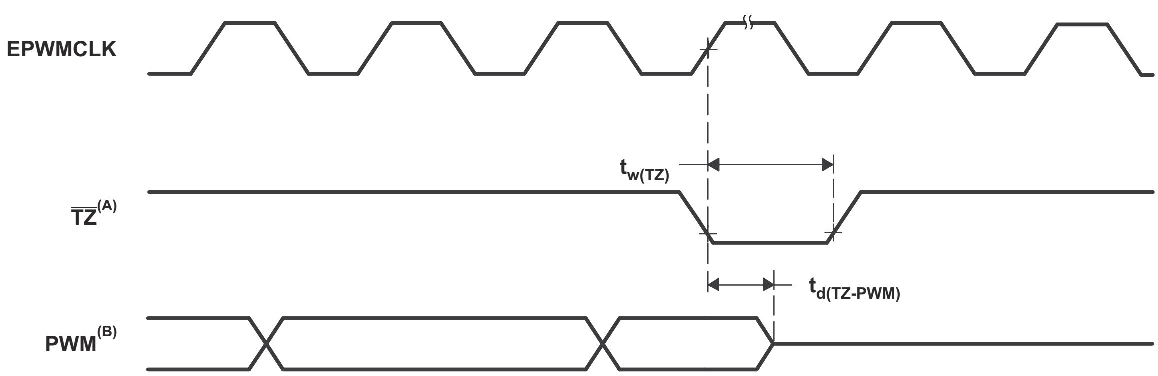
6.14.3.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.14.3.2.3.1 Trip-Zone Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZ}$x input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

6.14.3.2.3.2 PWM Hi-Z Characteristics Timing Diagram



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-79. PWM Hi-Z Characteristics

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6.14.4 External ADC Start-of-Conversion Electrical Data and Timing

6.14.4.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{\text{ADCSOCxO}}$ low	$32t_{c(SYSCLK)}$		cycles

6.14.4.2 $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing Diagram

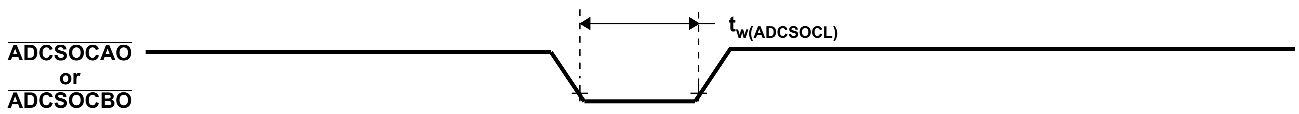

Figure 6-80. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

6.14.5 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.14.5.1 HRPWM Electrical Data and Timing

6.14.5.1.1 High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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6.14.6 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-81):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

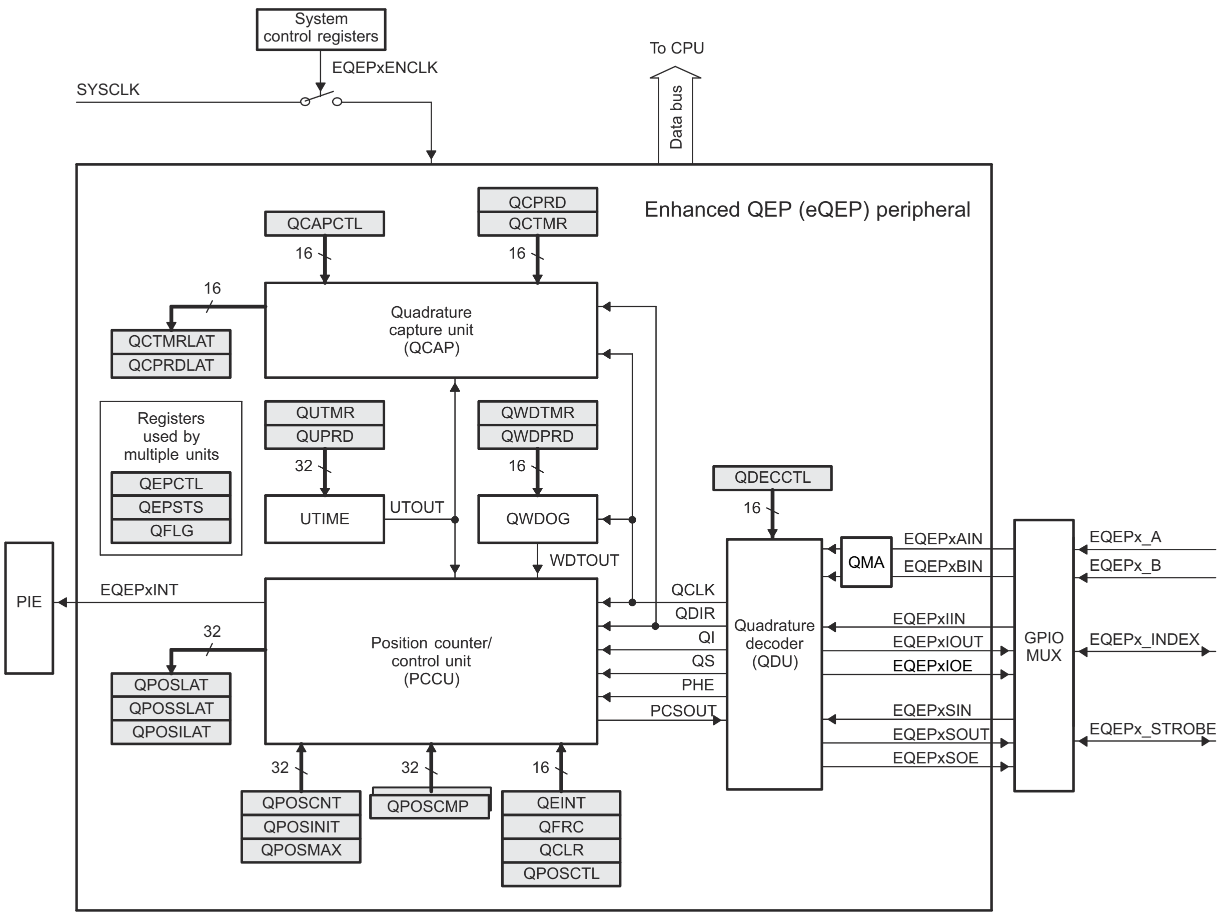

Figure 6-81. eQEP Block Diagram

6.14.6.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.14.6.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous[(1)]	$2t_{c(SYSCLK)}$		cycles
$t_{w(QEPP)}$	QEP input period	Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous[(1)]	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous[(1)]	$2t_{c(SYSCLK)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous[(1)]	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous[(1)]	$2t_{c(SYSCLK)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.14.6.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$7t_{c(SYSCLK)}$	cycles

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6.14.7 Sigma-Delta Filter Module (SDFM)

SDFM features include:

- Eight external pins per SDFM module
  - Four sigma-delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Different configurable modulator clock modes supported:
  - Mode 0: Modulator clock rate equals the modulator data rate.
- Four independent, configurable secondary filter (comparator) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - Ability to detect over-value condition, under-value condition, and Threshold-crossing conditions
    1. Two independent Higher Threshold comparators (used to detect over-value condition)
    2. Two independent Lower Threshold comparators (used to detect under-value condition)
    3. One independent Threshold-Crossing comparator (used to measure duty cycle/frequency with eCAP)
  - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- Four independent configurable primary filter (data filter) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - OSR value for data filter unit (DOSR) programmable from 1 to 256
  - Ability to enable or disable (or both) individual filter module
  - Ability to synchronize all four independent filters of an SDFM module by using the Main Filter Enable (MFE) bit or by using PWM signals
- Data filter output can be represented in either 16 bits or 32 bits.
- Data filter unit has a programmable mode FIFO to reduce interrupt overhead. The FIFO has the following features:
  - The primary filter (data filter) has a 16-deep x 32-bit FIFO.
  - The FIFO can interrupt the CPU after programmable number of data-ready events.
  - FIFO Wait-for-Sync feature: Ability to ignore data-ready events until the PWM synchronization signal (SDSYNC) is received. Once the SDSYNC event is received, the FIFO is populated on every data-ready event.
  - Data filter output can be represented in either 16 bits or 32 bits.
- PWMx.SOCA/SOCB can be configured to serve as SDSYNC source on a per-data-filter-channel basis.
- PWMs can be used to generate a modulator clock for sigma-delta modulators.
- Configurable Input Qualification available for both SD-Cx and SD-Dx
- Ability to use one filter channel clock (SD-C1) to provide clock to other filter clock channels.
- Configurable digital filter available on comparator filter events to blank out comparator events caused by spurious noise

Figure 6-82 shows the SDFM module block diagram.

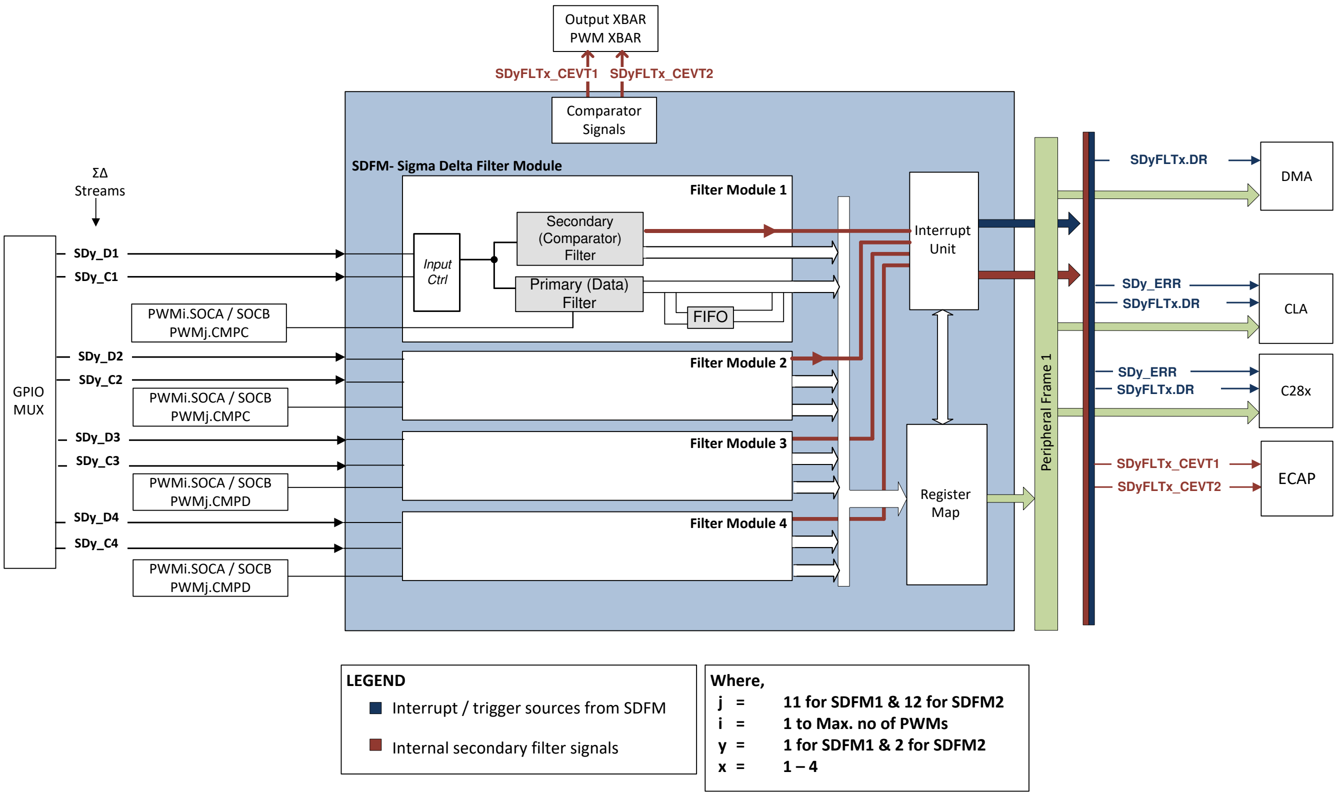

Figure 6-82. Sigma Delta Filter Module (SDFM) Block Diagram

6.14.7.1 SDFM Electrical Data and Timing

WARNING

Special precautions should be taken on both SD-Cx and SD-Dx signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination resistors for ringing noise due to any impedance mismatch of clock driver and spacing of traces from other noisy signals are recommended.

Note

The SDFM SD-Cx and SD-Dx signals, when synchronized to PLLRAWCLK, provide protection against SDFM module corruption due to occasional random noise glitches that may result in a false comparator trip and filter output. However, the signals do not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

6.14.7.1.1 SDFM Timing Requirements When Using Asynchronous GPIO ASYNC Option

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	4 * $t_{c(PLLRAWCLK)}$	256 * SYSCLK period	ns
$t_{w(SDDHL)M0}$	Pulse duration, SDx_Dy (high / Low)	2 * $t_{c(PLLRAWCLK)}$		ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	1 * $t_{c(PLLRAWCLK)}$ + 3		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	1 * $t_{c(PLLRAWCLK)}$ + 3		ns

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6.15 C28x Communications Peripherals

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

6.15.1 Controller Area Network (CAN)

Note

The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard (11-bit) or extended (29-bit) identifier
  - Supports programmable identifier receive mask
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loopback modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after bus-off state by a programmable 32-bit timer
- Two interrupt lines

Note

For a CAN bit clock of 100 MHz, the smallest bit rate possible is 3.90625Kbps.

Note

The accuracy of the on-chip oscillator is in the INTOSC Characteristics table. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 6-83 shows the CAN block diagram.

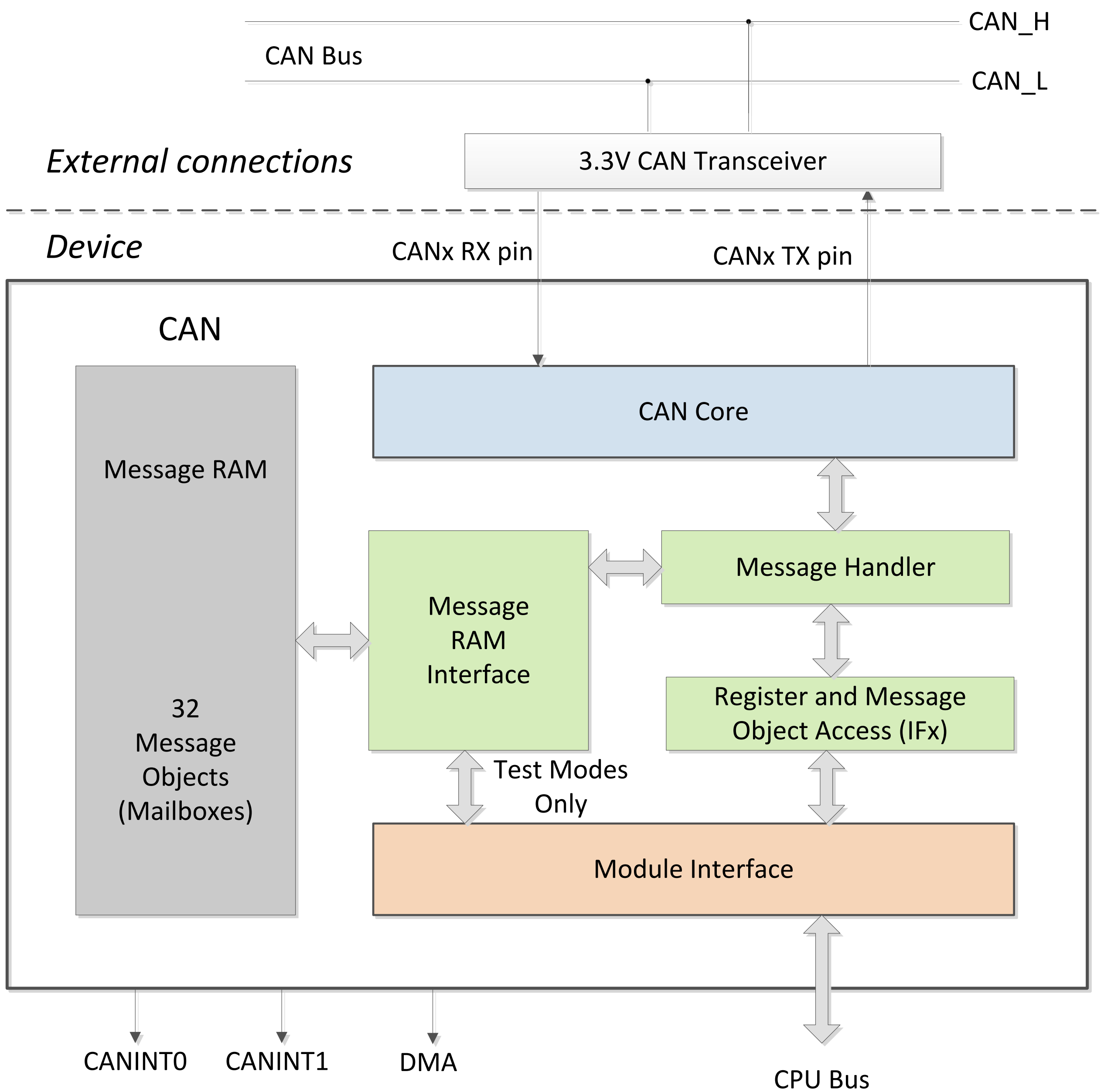

Figure 6-83. CAN Block Diagram

6.15.2 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices may coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

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Note

The availability of the CAN FD feature is dependent on the device's part number. Refer to the device data sheet for more information.

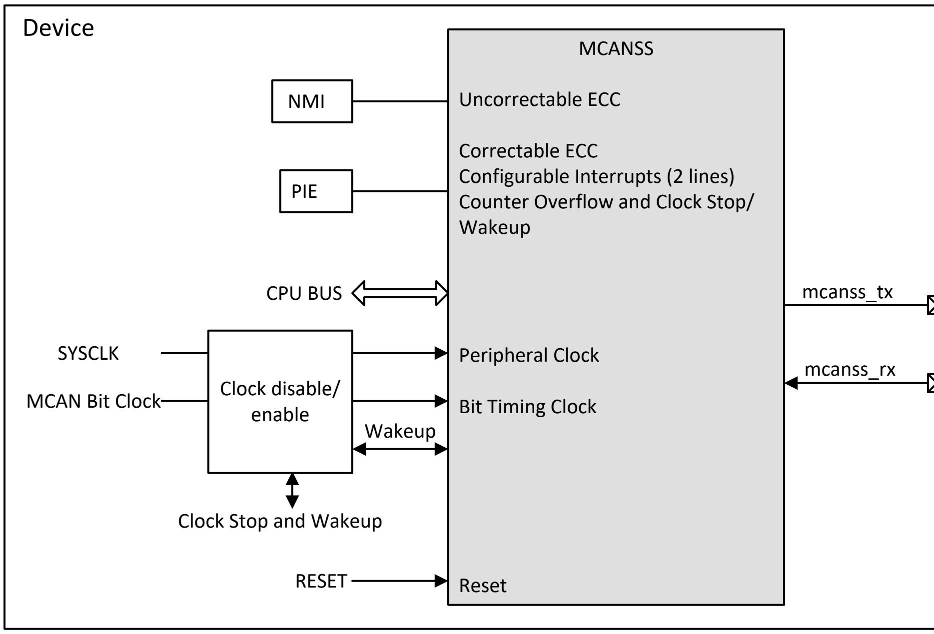

Figure 6-84. MCAN Module Overview

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Flexible Message RAM allocation (maximum configuration below is for a device with 4352 32-bit word message RAM)
  - Up to 32 dedicated transmit buffers
  - Configurable transmit FIFO, up to 32 elements
  - Configurable transmit queue, up to 32 elements
  - Configurable transmit Event FIFO, up to 32 elements
  - Up to 64 dedicated receive buffers
  - Two configurable receive FIFOs, up to 64 elements each
  - Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt (two configurable interrupt lines, correctable ECC, counter overflow and clock stop/ wakeup)
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock/host clock)
- ECC check for Message RAM
- Clock stop and wake-up support
- Timestamp counter

Non-supported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

6.15.3 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- SPI compatibility mode (limited features available)

Operating the FSI at maximum speed (60 MHz) at dual data rate (120Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The *Fast Serial Interface (FSI) Skew Compensation* Application Report provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in the *FSI Transmitter* section and the *FSI Receiver* section of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*, respectively.

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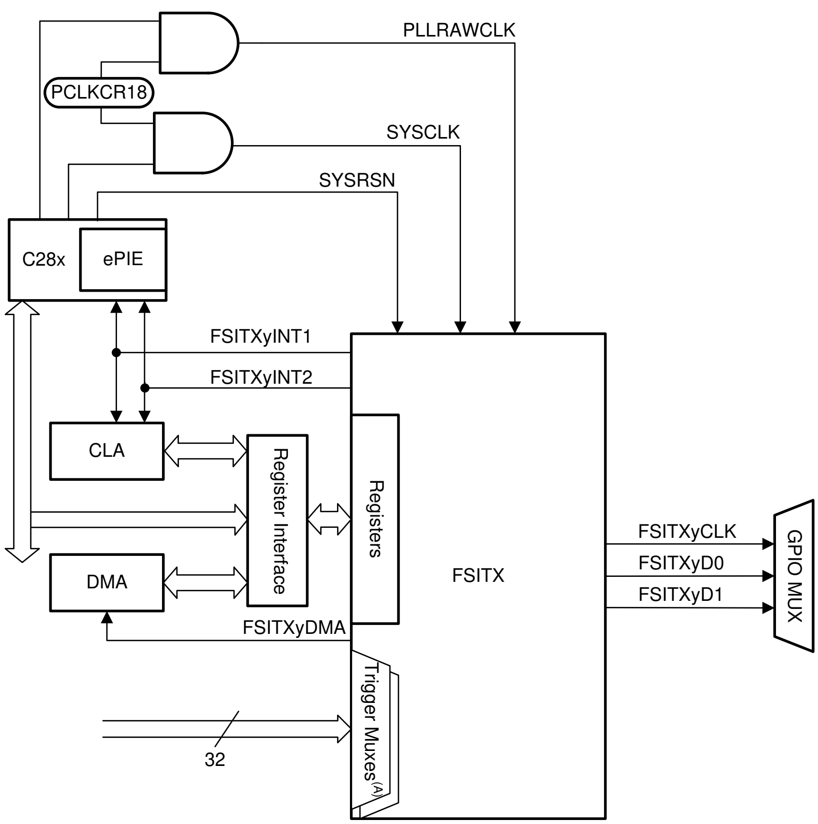
6.15.3.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU (or the CLA) program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU, CLA, and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support
- CLA task triggering

Figure 6-85 shows the FSITX CPU interface. Figure 6-86 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.



A. The signals connected to the trigger muxes are described in the External Frame Trigger Mux section of the Fast Serial Interface (FSI) chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

Figure 6-85. FSITX CPU Interface

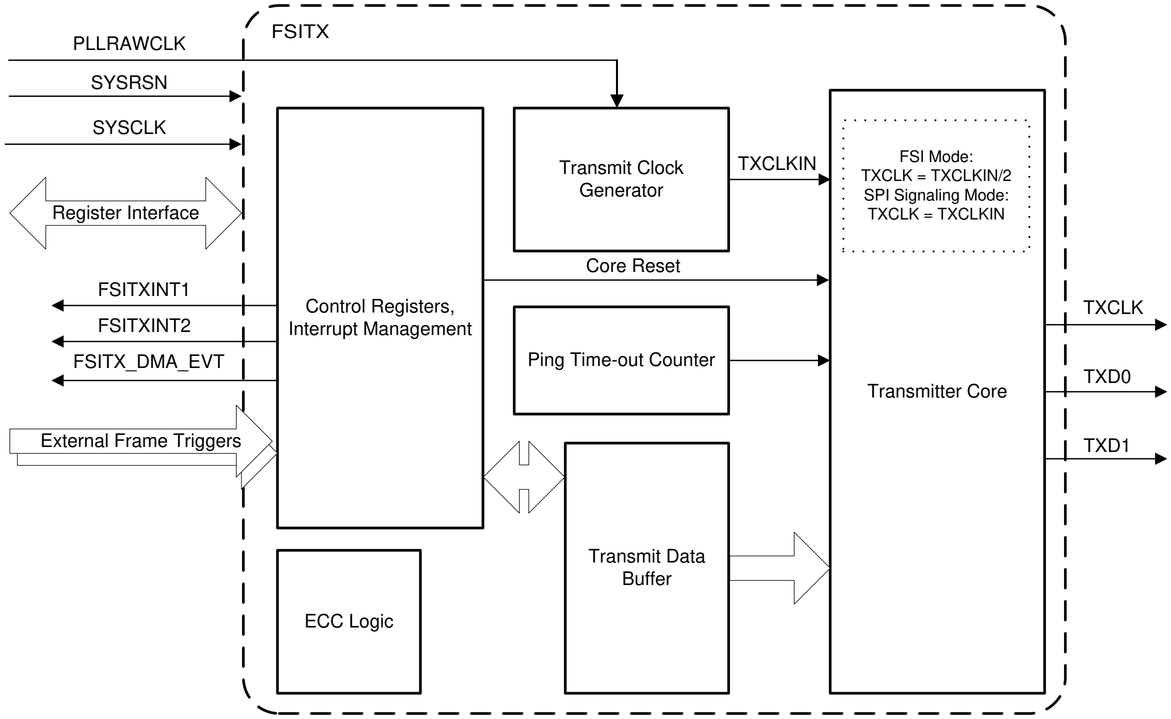


Figure 6-86. FSITX Block Diagram

6.15.3.1.1 FSITX Electrical Data and Timing

6.15.3.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER[(1)]		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	16.67		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) – 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLK–TXD)}$	Delay time, TXCLK rising or falling toTXD valid	$(0.25t_{c(TXCLK)}) – 2$	$(0.25t_{c(TXCLK)}) + 2$	ns
4	$t_{d(TXCLK)}$	TXCLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
5	$t_{d(TXD0)}$	TXD0 delay compensation at TX_DLYLINE_CTRL[TXD0_DLY]=31	9.95	30	ns
6	$t_{d(TXD1)}$	TXD1 delay compensation at TX_DLYLINE_CTRL[TXD1_DLY]=31	9.95	30	ns
7	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for TXCLK, TXD0, and TXD1	0.3	1	ns

(1) 10-pF load on pin.

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6.15.3.1.1.2 FSITX Timings

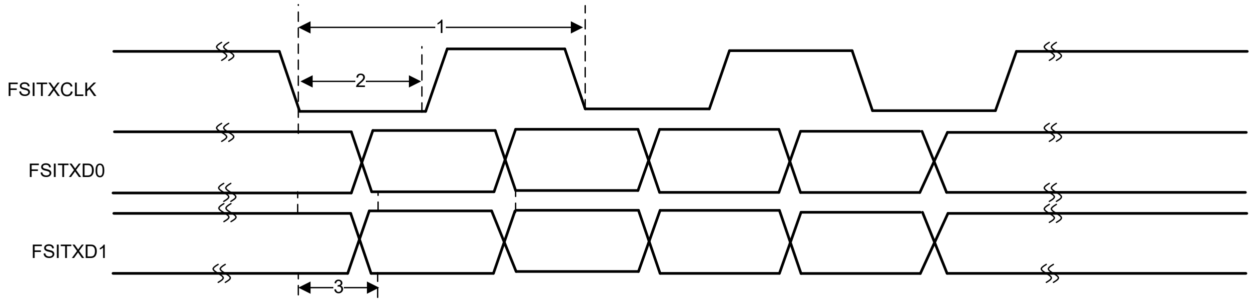

Figure 6-87. FSITX Timings

6.15.3.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU program (or the CLA), control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, CLA, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- SPI compatibility mode
- CLA task triggering

Figure 6-88 shows the FSIRX CPU interface. Figure 6-89 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

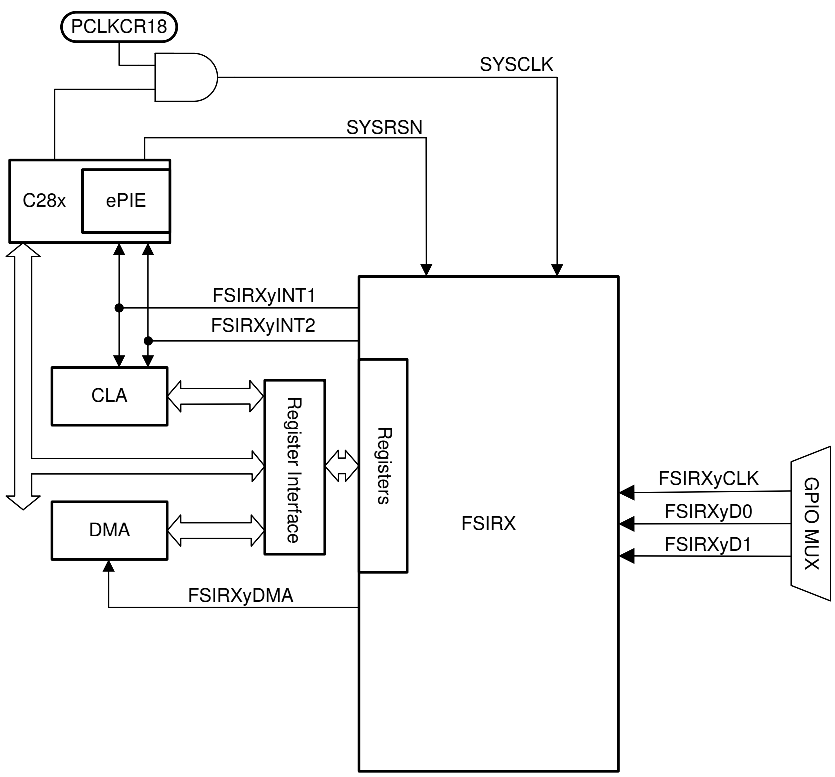

Figure 6-88. FSIRX CPU Interface

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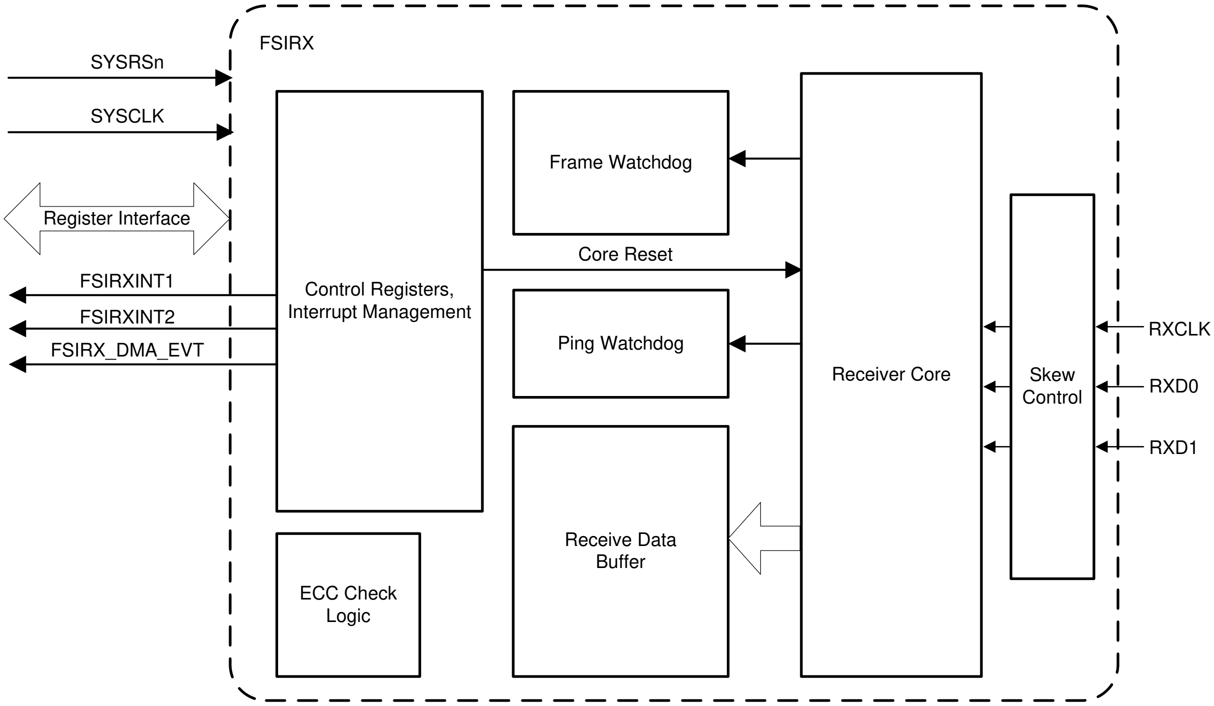

Figure 6-89. FSIRX Block Diagram

6.15.3.2.1 FSIRX Electrical Data and Timing

6.15.3.2.1.1 FSIRX Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(RXCLK)}$	Cycle time, RXCLK	19.417		ns
2	$t_{w(RXCLK)}$	Pulse width, RXCLK low or RXCLK high.	$0.35t_{c(RXCLK)}$	$0.65t_{c(RXCLK)}$	ns
3	$t_{su(RXCLK–RXD)}$	Setup time with respect to RXCLK, applies to both edges of the clock	1.7		ns
4	$t_{h(RXCLK–RXD)}$	Hold time with respect to RXCLK, applies to both edges of the clock	2		ns

6.15.3.2.1.2 FSIRX Switching Characteristics

NO.	PARAMETER(1)		MIN	MAX	UNIT
1	$t_{d(RXCLK)}$	RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	9.7	30	ns
2	$t_{d(RXD0)}$	RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31	9.7	30	ns
3	$t_{d(RXD1)}$	RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31	9.7	30	ns
4	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for RXCLK, RXD0, and RXD1	0.29	1	ns
TDM1	$t_{skew(TDM\_CLK-TDM\_Dx)}$	Delay skew introduced between RXCLK-TDM_CLK delay and RXDx-TDM_Dx delays	-3	3	ns
TDM1	$t_{d(RXCLK-TDM\_CLK)}$	Delay time, RXCLK input to TDM_CLK output	2	14.5	ns
TDM2	$t_{d(RXD0-TXD0)}$	Delay time, RXD0 input to TXD0 output	2	14.5	ns
TDM3	$t_{d(RXD1-TXD1)}$	Delay time, RXD1 input to TXD1 output	2	14.5	ns

(1) 10-pF load on pin.

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6.15.3.2.1.3 FSIRX Timings

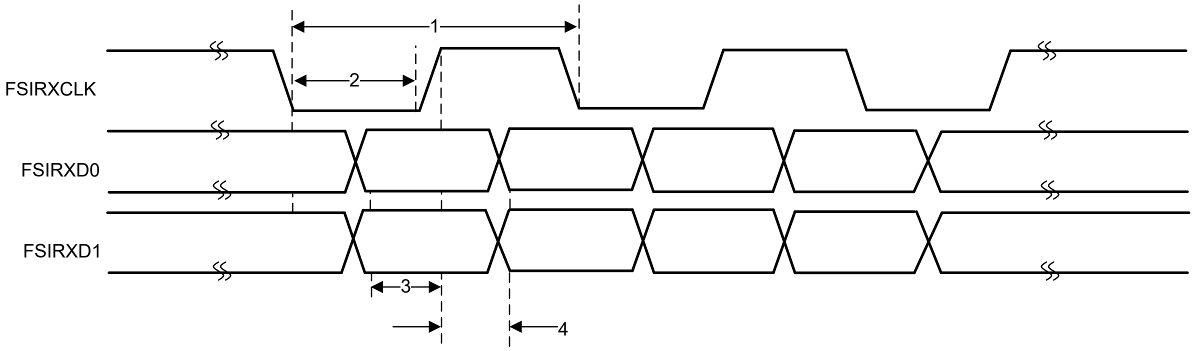

Figure 6-90. FSIRX Timings

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6.15.3.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI peripheral configuration because the FSI TXCLK cannot take an external clock source.

6.15.3.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in the FSIRX Timing Requirements table are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

6.15.3.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER[(1)]		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	19.417		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) – 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLKH–TXD0)}$	Delay time, TXD0 valid after TXCLK high		3	ns
4	$t_{d(TXD1-TXCLK)}$	Delay time, TXCLK high after TXD1 low	$t_{w(TXCLK)} – 3$		ns
5	$t_{d(TXCLK-TXD1)}$	Delay time, TXD1 high after TXCLK low	$t_{w(TXCLK)}$		ns

(1) 10-pF load on pin

6.15.3.3.1.2 FSITX SPI Signaling Mode Timings

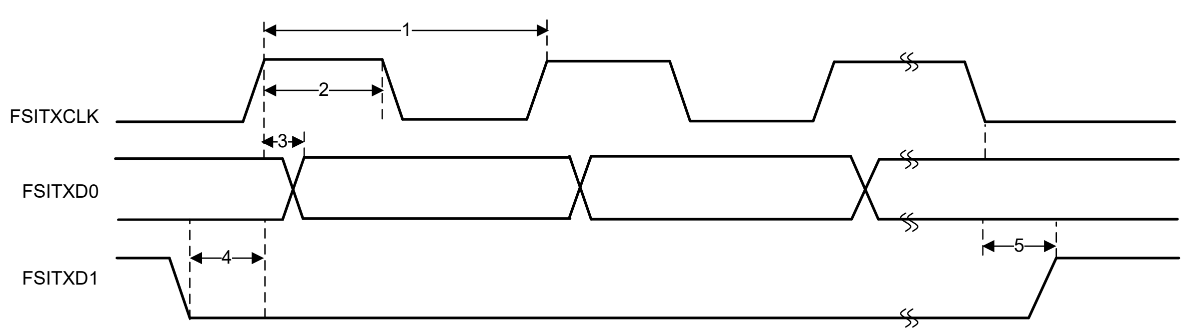

Figure 6-91. FSITX SPI Signaling Mode Timings

6.15.4 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I^2C-bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple controller-transmitters and target-receivers
  - Support for multiple target-transmitters and controller-receivers
  - Combined controller transmit/receive and receive/transmit mode
  - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
  - SMBus 2.0 and below
  - PMBus 1.2 and below
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
  - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
    - Transmit Ready
    - Receive Ready
    - Register-Access Ready
    - No-Acknowledgment
    - Arbitration-Lost
    - Stop Condition Detected
    - Addressed-as-Target
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-92 shows how the I2C peripheral module interfaces within the device.

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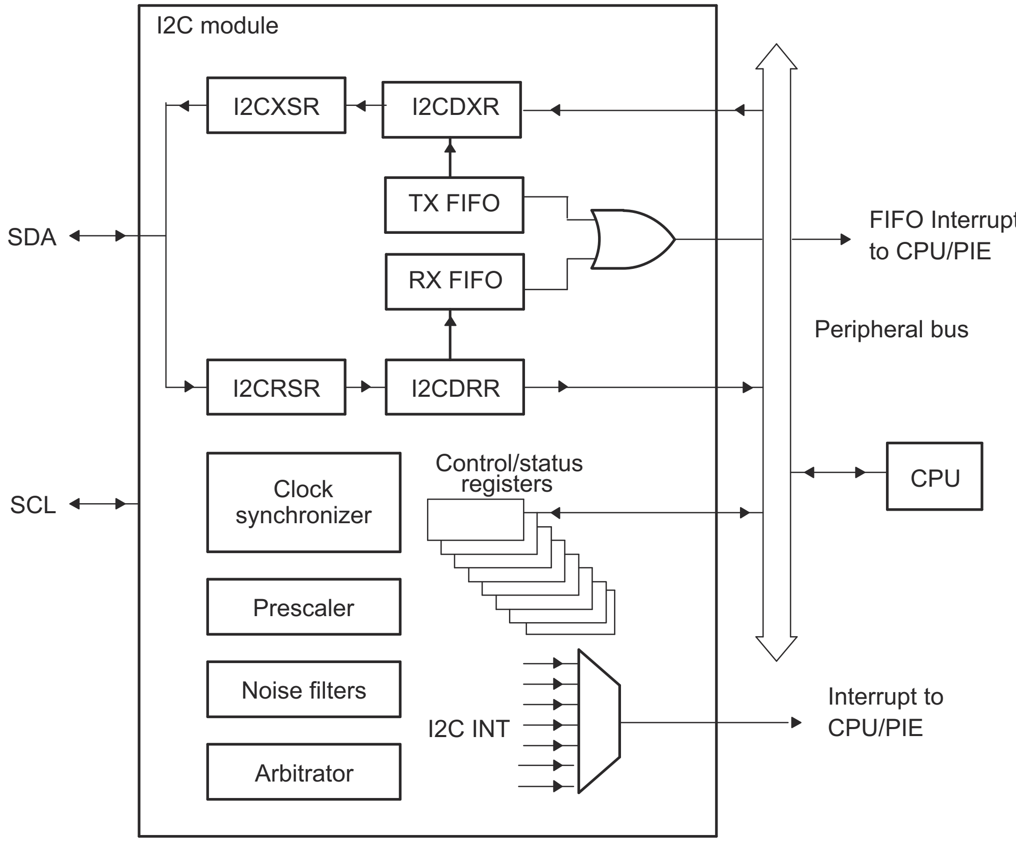

Figure 6-92. I2C Peripheral Module Interfaces

6.15.4.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the *I2C Bus Pullup Resistor Calculation* Application Report.

6.15.4.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.0		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250 (2)		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000 (1)	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000 (1)	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	One I2C module clock	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	One I2C module clock	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

(1) In order to minimize the rise time, TI recommends using a strong pullup on both the SDA and SCL bus lines on the order of 2.2-kΩ net pullup resistance. It is also recommended that the value of the pullup resistance used on both SCL and SDA pins be matched.
(2) The C2000 I2C is a Fast-mode device. There is a limitation when using the I2C as a target transmitter with a standard mode host. For more information, see the *TMS320F28P65x Real-Time MCUs Silicon Errata*.

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6.15.4.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
	V_{IL}	Valid low-level input voltage		–0.3	0.3 * V_{DDIO}	V
	V_{IH}	Valid high-level input voltage		0.7 * V_{DDIO}	V_{DDIO} + 0.3	V
	V_{OL}	Low-level output voltage	Sinking 3 mA	0	0.4	V
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
	V_{IL}	Valid low-level input voltage		–0.3	0.3 * V_{DDIO}	V
	V_{IH}	Valid high-level input voltage		0.7 * V_{DDIO}	V_{DDIO} + 0.3	V
	V_{OL}	Low-level output voltage	Sinking 3 mA	0	0.4	V
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA

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6.15.4.1.3 I2C Timing Diagram

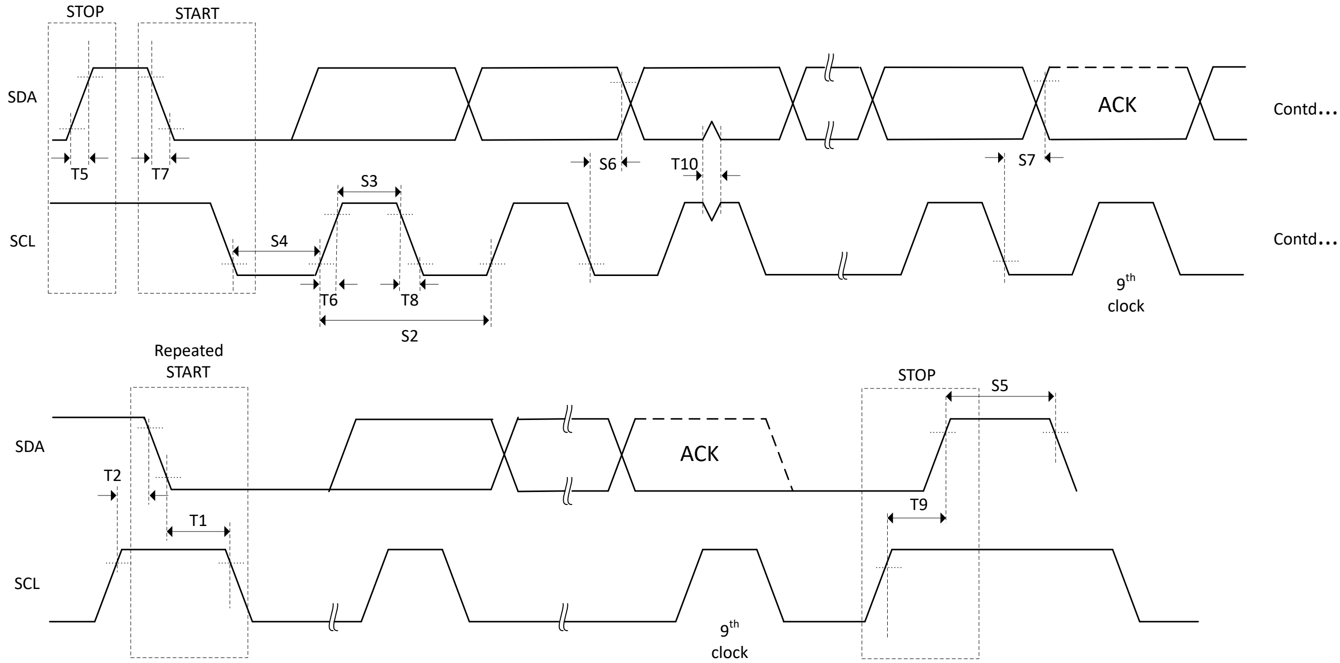

Figure 6-93. I2C Timing Diagram

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6.15.5 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Supports voltage thresholds compatible to:
  - PMBus and below
  - SMBus and below
- Support for controller and target
- Support for I2C mode
- Support for speeds:
  - Standard Mode: Up to 100 kHz
  - Fast Mode: 400 kHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
  - Receive data ready
  - Transmit buffer empty
  - Target address received
  - End of message
  - ALERT input asserted
  - Clock low time-out
  - Clock high time-out
  - Bus free

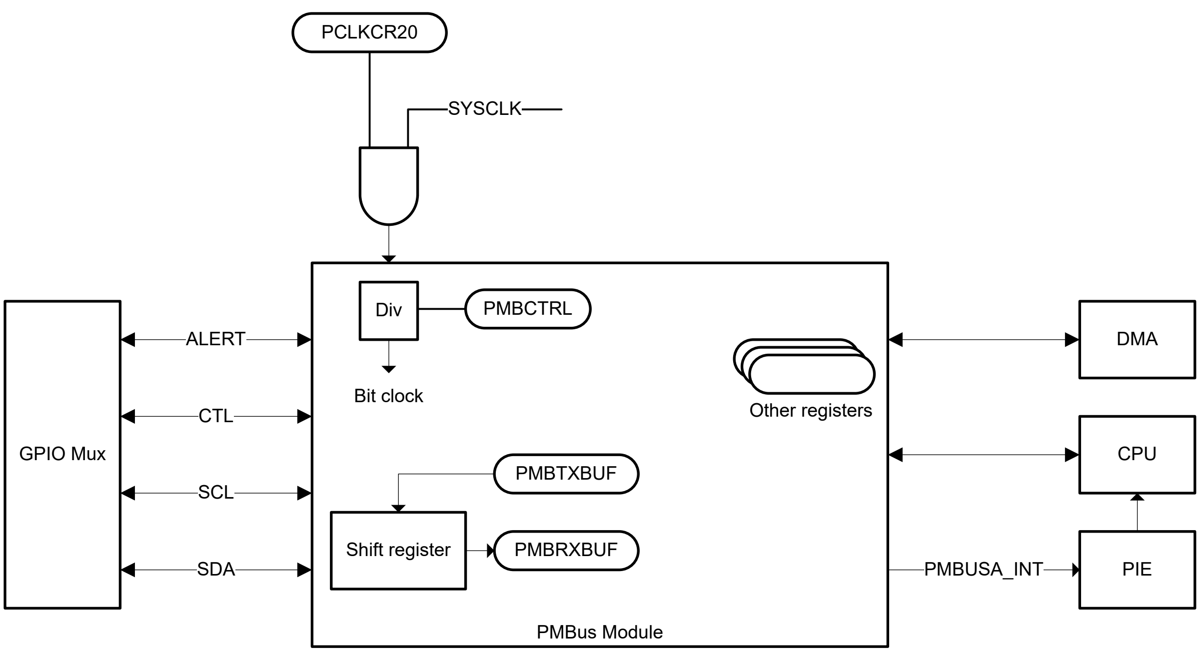

Figure 6-94. PMBus Block Diagram

6.15.5.1 PMBus Electrical Data and Timing

6.15.5.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Valid low-level input voltage				0.8	V
V_{IH}	Valid high-level input voltage		2.1		VDDIO	V
V_{OL}	Low-level output voltage	At I_{pullup} = 4 mA			0.4	V
I_{OL}	Low-level output current	V_{OL} ≤ 0.4 V	4			mA
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0		50	ns
I_i	Input leakage current on each pin	0.1 Vbus < Vi < 0.9 Vbus	–10		10	µA
C_i	Capacitance on each pin				10	pF
V_{noise}	Signal immunity from 10 MHz to 100 MHz		300			mV p-p

6.15.5.1.2 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{MOD}	PMBUS module clock frequency		6.25		10	MHz
f_{SCL}	SCL clock frequency		10		400	kHz
t_{BUF}	Bus free time between STOP and START conditions		1.3			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		0.6			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		0.6			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		0.6			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
$t_{SU;DAT}$	Data setup time before SCL rise		100			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		1.3			µs
t_{HIGH}	High period of the SCL clock		0.6		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (target device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (controller device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL	5% to 95%	20		300	ns
t_f	Fall time of SDA and SCL	95% to 5%	20		300	ns

6.15.5.1.3 PMBus Standard Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{MOD}	PMBUS module clock frequency		6.25		10	MHz
f_{SCL}	SCL clock frequency		10		100	kHz
t_{BUF}	Bus free time between STOP and START conditions		4.7			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		4			µs

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6.15.5.1.3 PMBus Standard Mode Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		4.7			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		4			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
$t_{SU;DAT}$	Data setup time before SCL rise		250			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		4.7			µs
t_{HIGH}	High period of the SCL clock		4		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (target device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (controller device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL				1000	ns
t_f	Fall time of SDA and SCL				300	ns

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6.15.6 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
  - Baud rate programmable to 64K different rates
- Data-word format
  - 1 start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6-95 shows the SCI block diagram.

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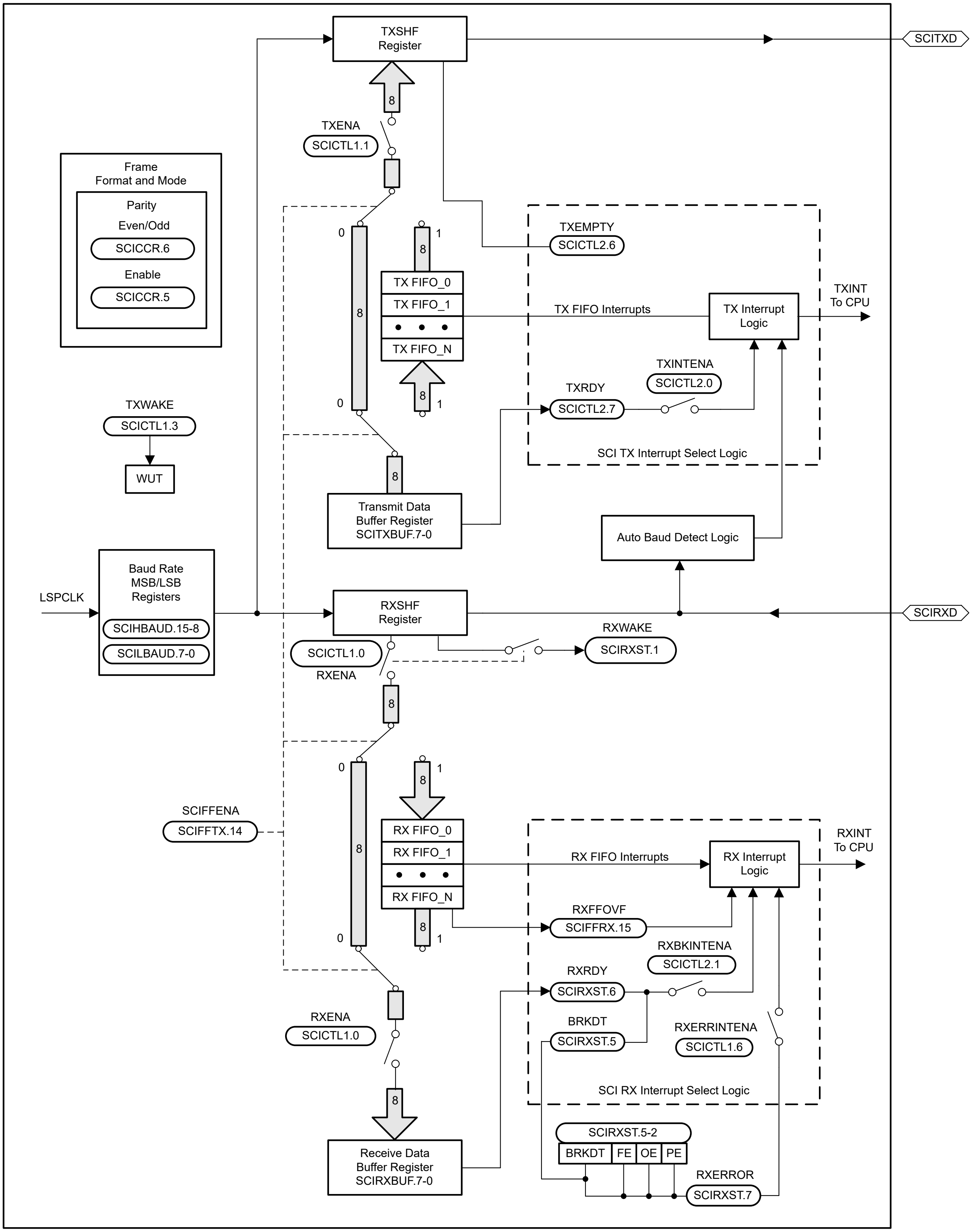

Figure 6-95. SCI Block Diagram

6.15.7 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the controller or peripheral operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPIPOCI: SPI peripheral-output/controller-input pin
- SPIPICO: SPI peripheral-input/controller-output pin
- $\overline{\text{SPIPTE}}$: SPI peripheral transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Controller and Peripheral
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPIPTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-96 shows the SPI CPU interfaces.

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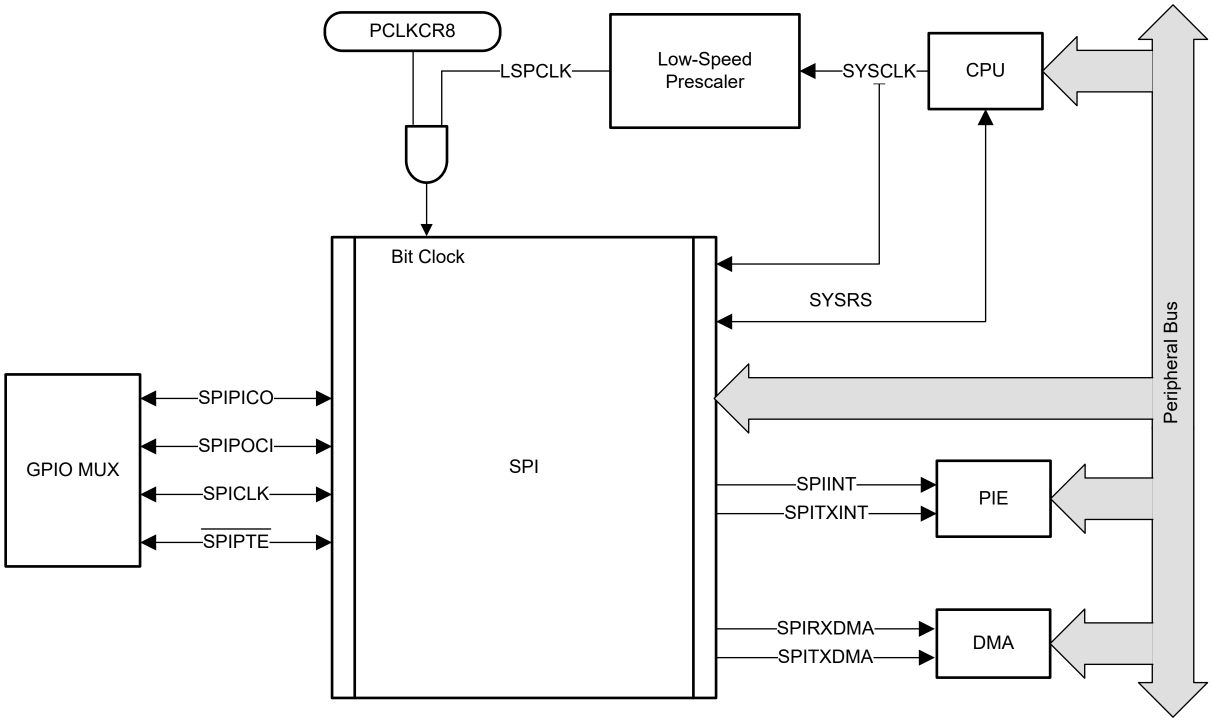

Figure 6-96. SPI CPU Interface

6.15.7.1 SPI Controller Mode Timings

The following section contains the SPI Controller Mode Timings.For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPIPICO, and SPIPOCI.

For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

To use the SPI in High-Speed mode, the application must use the high-speed enabled GPIOs (see the *High-Speed SPI Pin Muxing* section). Table 6-29 lists the SPI clocks for supporting High-Speed Mode.

Table 6-29. SPI Clocks for Supporting High-Speed Mode

SPI CLOCK	GPIO PIN NUMBER
SPICLKA	GPIO60
SPICLKB	GPIO65
SPICLKC	GPIO71
SPICLKD	GPIO93

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6.15.7.1.1 SPI Controller Mode Switching Characteristics Clock Phase 0

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[(1)](2)		(BRR + 1) CONDITION[(3)]	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPIPTE}}$ active to SPICLK	Even	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
			Odd	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$	
24	$t_{v(PTE)M}$	Valid time, SPICLK to $\overline{\text{SPIPTE}}$ inactive	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
High-Speed Mode						
4	$t_{d(PICO)M}$	Delay time, SPICLK to SPIPICO valid	Even, Odd		1	ns
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
Normal Mode						
4	$t_{d(PICO)M}$	Delay time, SPICLK to SPIPICO valid	Even, Odd		5	ns
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

(1) 5-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.15.7.1.2 SPI Controller Mode Switching Characteristics Clock Phase 1

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[(1) (2)]		(BRR + 1) CONDITION[(3)]	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} – 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} – 1$	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} – 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} – 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPIPTE}}$ valid to SPICLK	Even, Odd	$2t_{c(SPC)M} – 3t_{c(SYSCLK)} – 3$	$2t_{c(SPC)M} – 3t_{c(SYSCLK)} + 3$	ns
24	$t_{v(PTE)M}$	Valid time, SPICLK to $\overline{\text{SPIPTE}}$ invalid	Even	– 3	+3	ns
			Odd	– 3	+3	
High-Speed Mode						
4	$t_{d(PICO)M}$	Delay time, SPIPICO valid to SPICLK	Even	$0.5t_{c(SPC)M} – 1$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} – 1$		
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} – 1$		ns
			Odd	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} – 1$		
Normal Mode						
4	$t_{d(PICO)M}$	Delay time, SPIPICO valid to SPICLK	Even	$0.5t_{c(SPC)M} – 5$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} – 5$		
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} – 3$		ns
			Odd	$0.5t_{c(SPC)M} – 0.5t_{c(LSPCLK)} – 3$		

(1) 5-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.15.7.1.3 SPI Controller Mode Timing Requirements

NO.			(BRR + 1) CONDITION[(1)]	MIN	MAX	UNIT
High-Speed Mode						
8	$t_{su(POCI)M}$	Setup time, SPIPOCI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(POCI)M}$	Hold time, SPIPOCI valid after SPICLK	Even, Odd	5		ns
Normal Mode						
8	$t_{su(POCI)M}$	Setup time, SPIPOCI valid before SPICLK	Even, Odd	20		ns
9	$t_{h(POCI)M}$	Hold time, SPIPOCI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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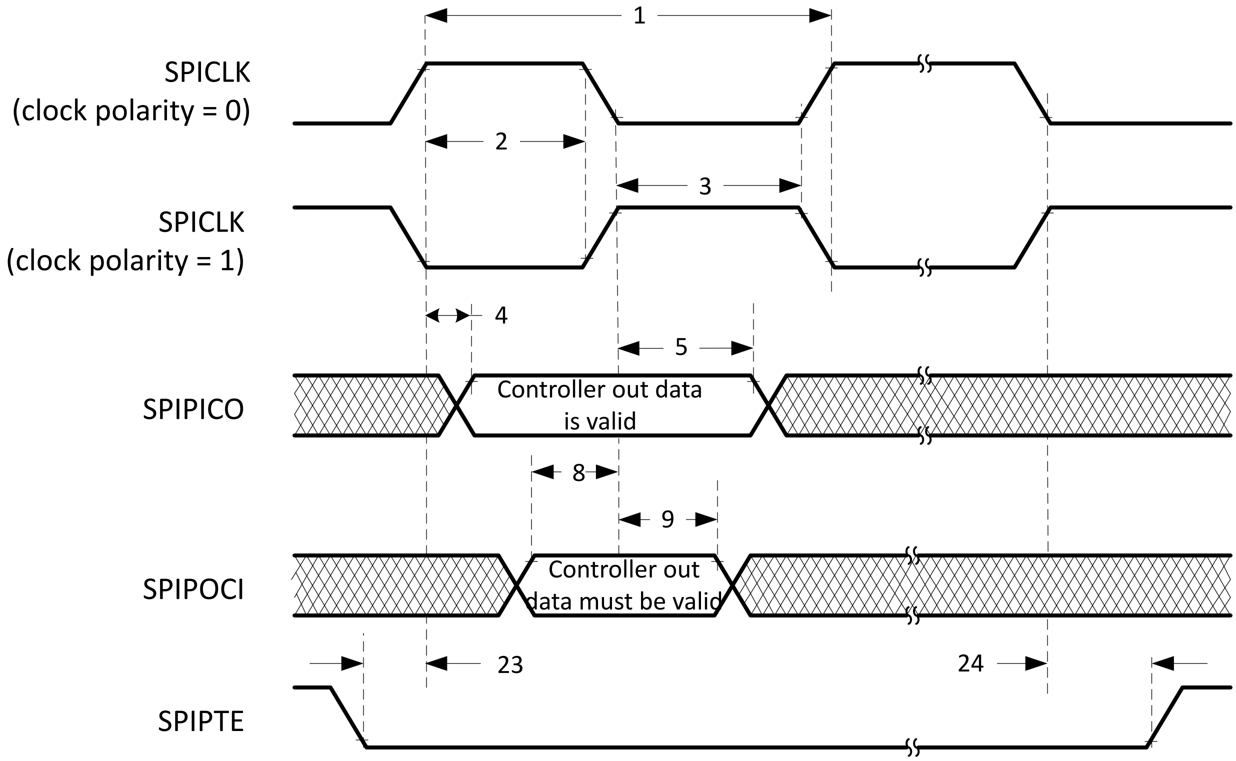
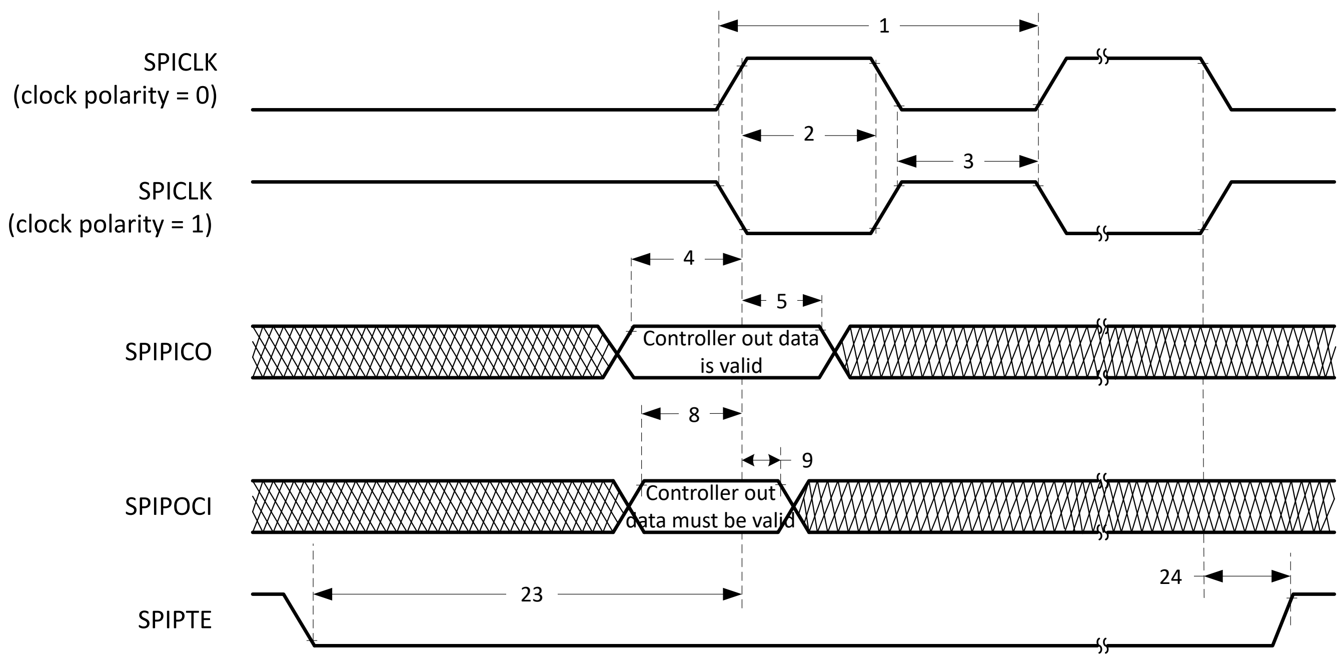
6.15.7.1.4 SPI Controller Mode Timing Diagrams



A. On the trailing end of the word, $\overline{\text{SPIPTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-97. SPI Controller Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPIPTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-98. SPI Controller Mode External Timing (Clock Phase = 1)

6.15.7.2 SPI Peripheral Mode Timings

The following section contains the SPI Peripheral Mode Timings.For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

6.15.7.2.1 SPI Peripheral Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[(1) (2)]		MIN	MAX	UNIT
High-Speed Mode					
15	$t_{d(POCI)S}$	Delay time, SPICLK to SPIPOCI valid		9	ns
16	$t_{v(POCI)S}$	Valid time, SPIPOCI valid after SPICLK	0		ns
Normal Mode					
15	$t_{d(POCI)S}$	Delay time, SPICLK to SPIPOCI valid		20	ns
16	$t_{v(POCI)S}$	Valid time, SPIPOCI valid after SPICLK	0		ns

(1) 5-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.

6.15.7.2.2 SPI Peripheral Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(PICO)S}$	Setup time, SPIPICO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(PICO)S}$	Hold time, SPIPICO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(PTE)S}$	Setup time, $\overline{\text{SPIPTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 11$		ns
		Setup time, $\overline{\text{SPIPTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 20$		ns
26	$t_{h(PTE)S}$	Hold time, $\overline{\text{SPIPTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

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6.15.7.2.3 SPI Peripheral Mode Timing Diagrams

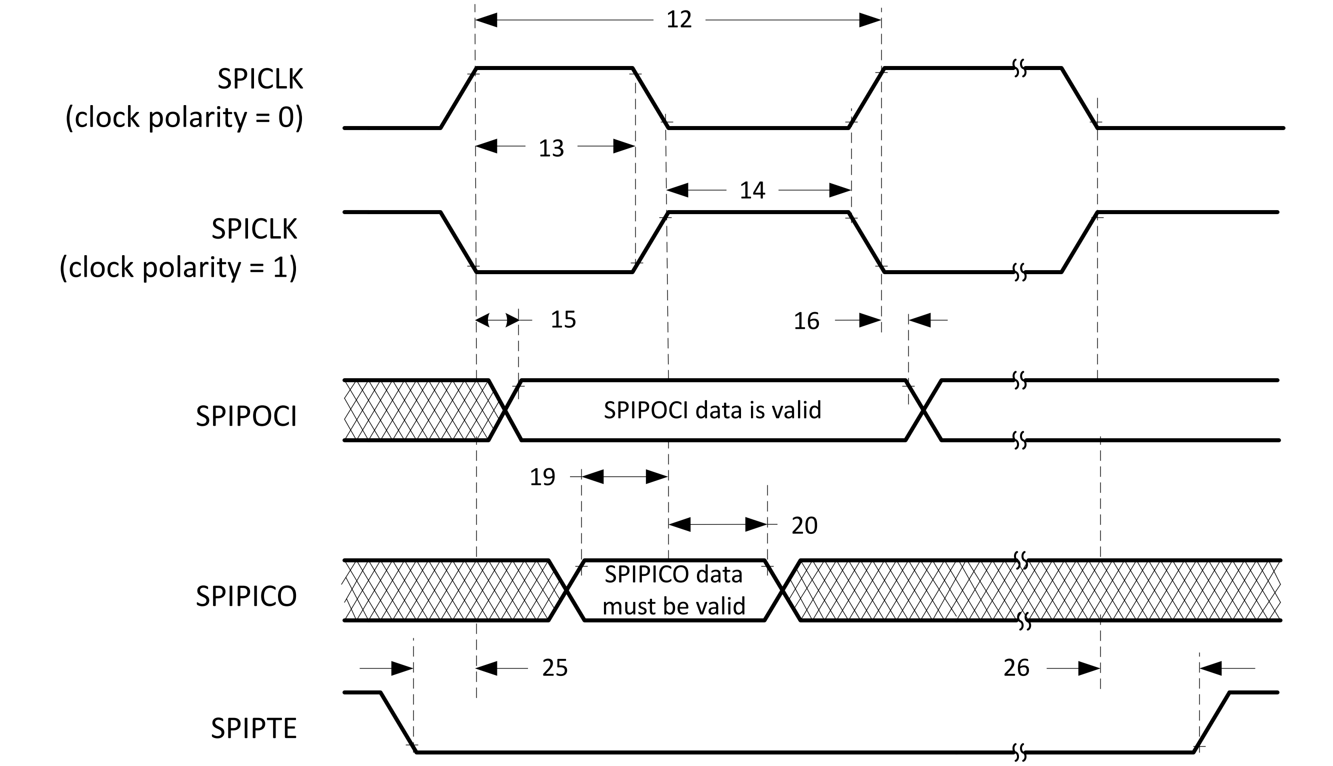

Figure 6-99. SPI Peripheral Mode External Timing (Clock Phase = 0)

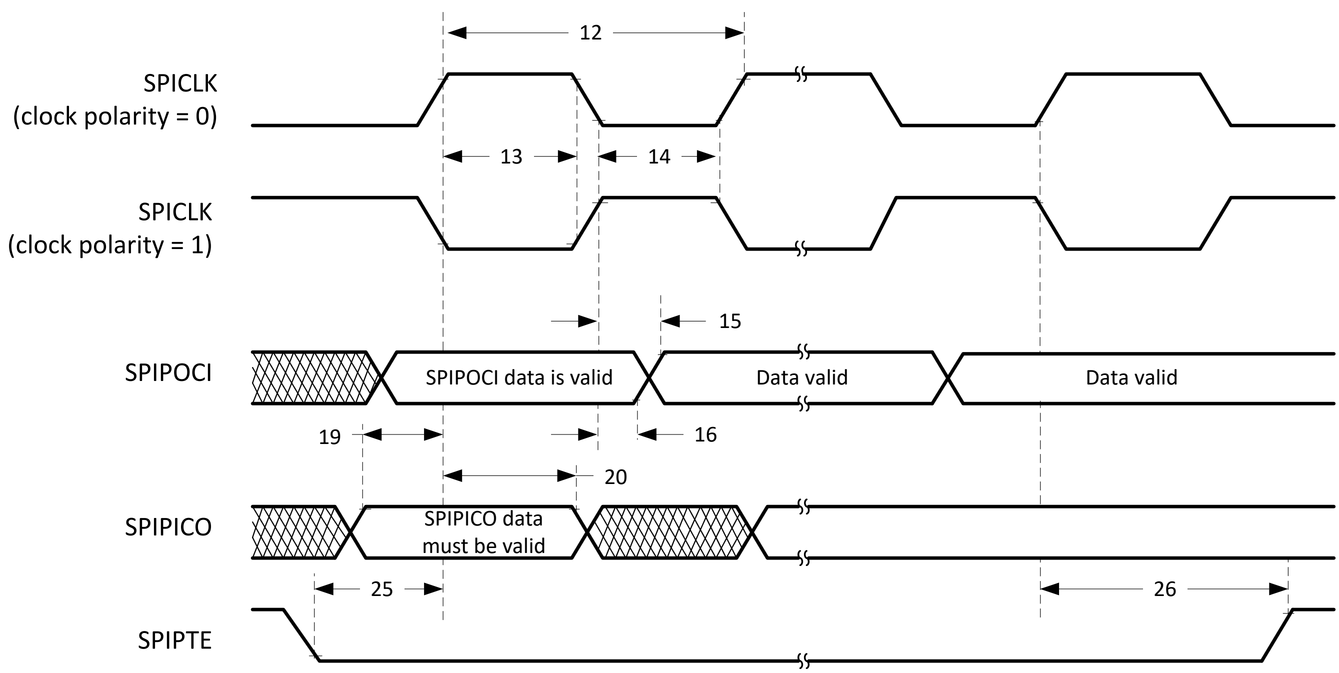

Figure 6-100. SPI Peripheral Mode External Timing (Clock Phase = 1)

6.15.8 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-commander and multiple-responder with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic commander header generation
  - Programmable synchronization break field
  - Synchronization field
  - Identifier field
- Responder automatic synchronization
  - Synchronization break detection
  - Optional baud rate update
  - Synchronization validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wake-up support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error
  - Bus error
  - No-response error
  - Checksum error
  - Synchronization field error
  - Parity error
- Two interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

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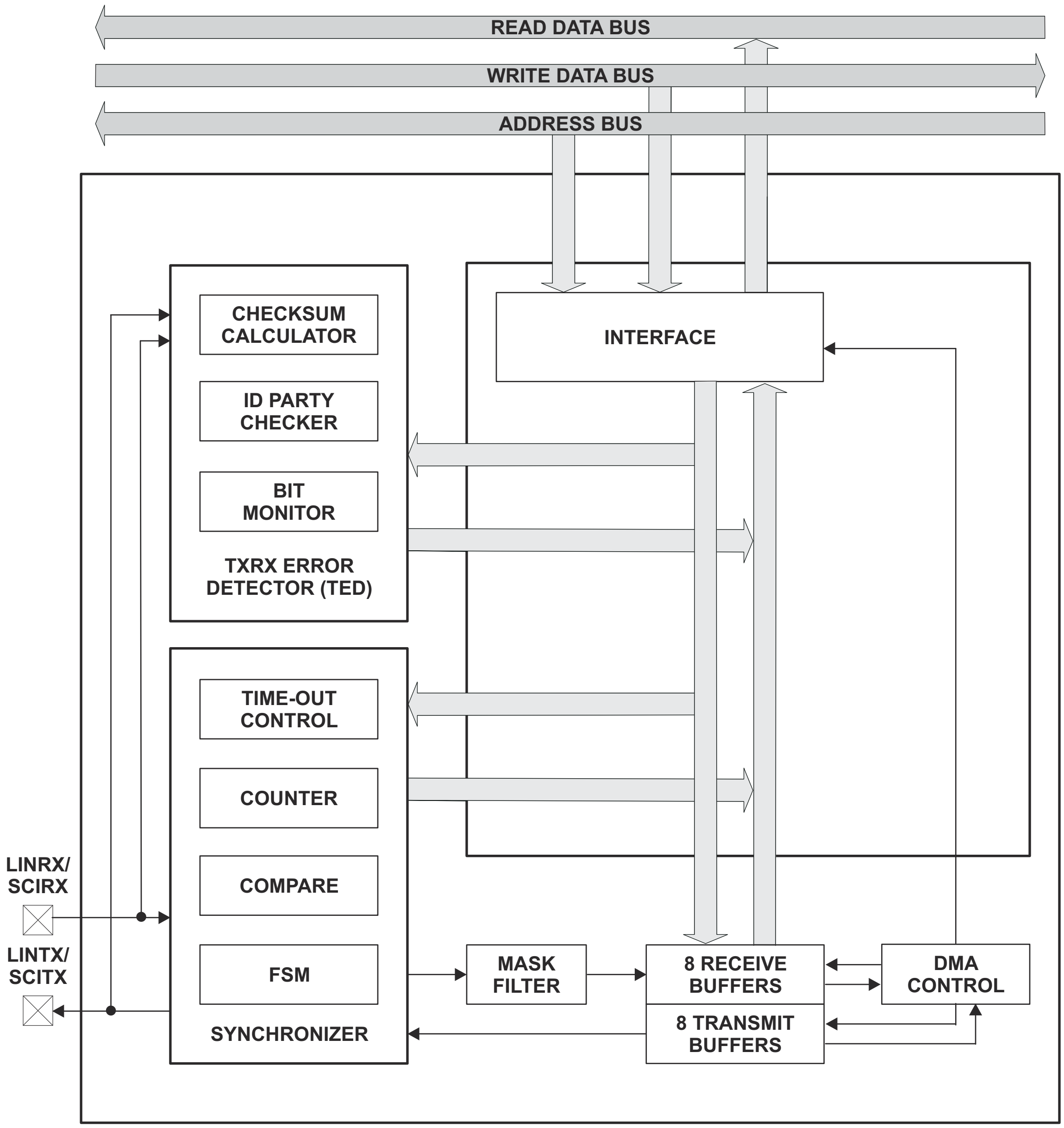

Figure 6-101. LIN Block Diagram

6.15.9 EtherCAT SubordinateDevice Controller (ESC)

Ethernet for Control Automation Technology (EtherCAT®) is an Ethernet-based fieldbus system, invented by Beckhoff Automation and is standardized in IEC 61158. All the SubordinateDevice (or SubDevice) nodes connected to the bus interpret, process, and modify the data addressed to them quickly, without having to buffer the frame inside the node. This real-time behavior, frame processing, and forwarding requirements are implemented by the EtherCAT SubDevice controller (ESC) hardware. EtherCAT does not require software interaction for data transmission inside the SubDevices. EtherCAT only defines the MAC layer while the higher-layer protocols and stack are implemented in software on the microcontrollers connected to the ESC.

The EtherCAT:

- Involves MainDevice (or MDevice) and SubDevices setup where SubDevice nodes are physically connected daisy-chain style but logically operate on a loop
- Specializes in precise, low-jitter synchronization across SubDevice nodes
- Uses IEEE 802.3 Ethernet physical layer and standard Ethernet frames

6.15.9.1 ESC Features

The ESC on this MCU provides the following functionality:

- Up to 2 MII ports to connect to EtherCAT PHYs
- Process data interface through 16-bit asynchronous interface
- 64-bit distributed clocking
  - Sync output signals to synchronize device events and latch input signals supporting time-stamping for events
  - Distributed clock features of SYNC0/1 (o/ps) and LATCH0/1 able to synchronize GPIOs and allow inputs from any GPIOs as well as other muxing options for internal device events
- 8 Field bus Memory Management Units (FMMUs)
  - Support all native types of RD/, WR/, RDWR, and built-in features of bit- and byte-addressing
- 8 Sync Managers
- I2C EEPROM interface
- Up-to 32 general-purpose inputs (GPIs) and 32 general-purpose outputs (GPOs)
- 2 SYNC and 2 LATCH signals connected to GPIO pads
- 16KB RAM with parity

6.15.9.2 ESC Subsystem Integrated Features

In addition to the ESC features, the following are the device-specific features provided by the integration of the ESC and the MCU:

- ESC access allocation to the CPU1 subsystem during initialization
- EtherCAT reset request from MDevice can be routed to NMI or general interrupt controller on MCU
- RAM Parity error routed to NMI on MCU
- DMA access to EtherCAT RAM
- Up to 32 GPIs and up to 32 GPOs feature integrated to 16-bit ASYNC PDI interface
- Interface to CLB
- Distributed clock feature of SYNC0/1 able to synchronize PWMs, generate interrupt/DMA requests, or trigger eCAP capture to allow external component action through GPIO access.
- EtherCAT SYNC0/1 pulse can trigger a CLA task.
- Distributed clock feature of LATCH0/1 allows inputs from any GPIO or PWM crossbar triggers

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6.15.9.3 EtherCAT IP Block Diagram

Figure 6-102 shows the general functionality of EtherCAT IP.

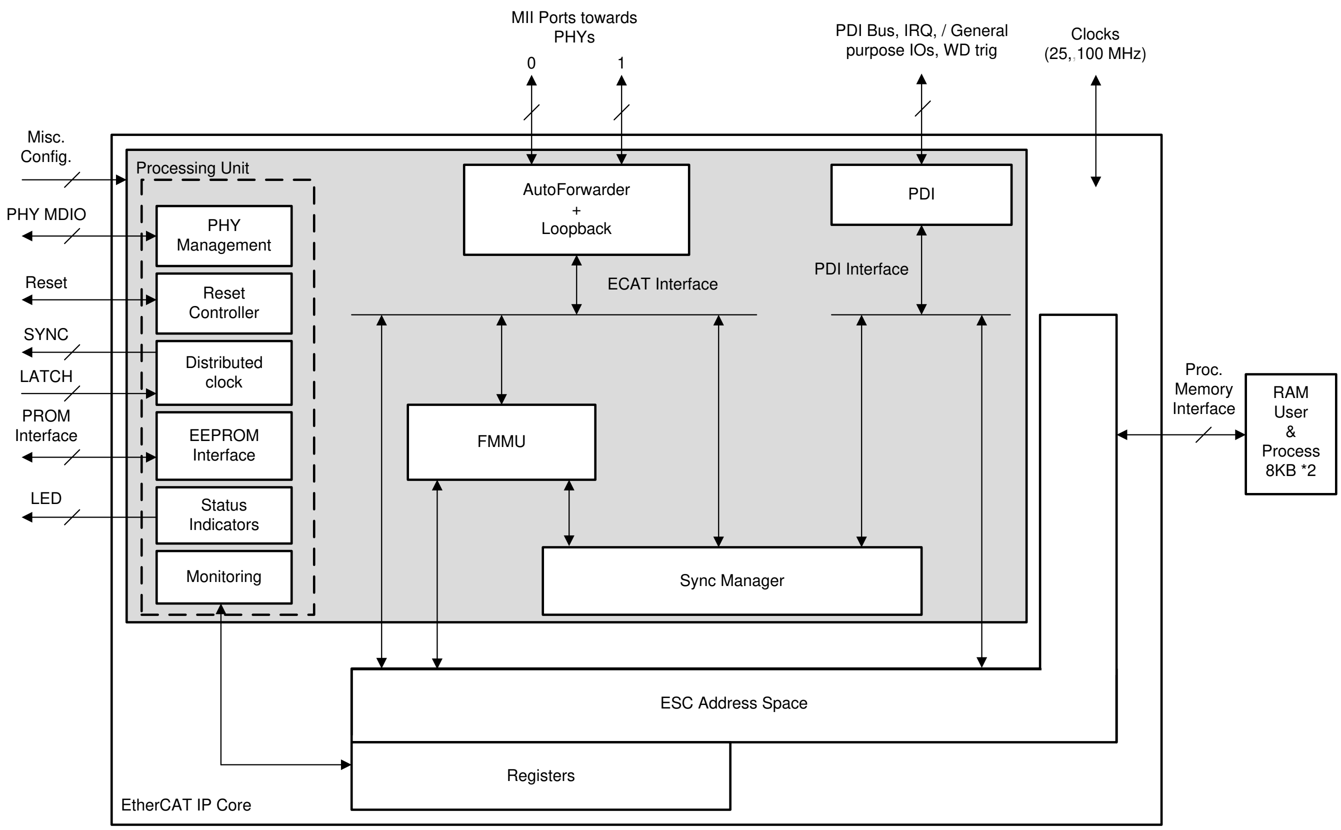

Figure 6-102. EtherCAT IP Block Diagram

6.15.9.4 EtherCAT Electrical Data and Timing

6.15.9.4.1 EtherCAT Timing Requirements

NO.			MIN	NOM	MAX	UNIT
EtherCAT						
	$t_{c(ECATCLK)}$	Cycle time, ECATCLK		10		ns
MII1	$t_{c(TXCLK)}$	Cycle time, ESC_TXy_CLK		40		ns
MII2/MII3	$t_{w(TXCK)}$	Pulse duration, ESC_TXy_CLK high or low	16		24	ns
MII4	$t_{c(RXCK)}$	Cycle time, ESC_RXy_CLK		40		ns
MII5/MII6	$t_{w(RXCK)}$	Pulse duration, ESC_RXy_CLK high or low	16		24	ns
MII8	$t_{su(RXDV-RXCKH)}$	Setup time, receive signals valid before ESC_RXy_CLK high	10			ns
MII9	$t_{h(RXCKH-RXDV)}$	Hold time, receive signals valid after ESC_RXy_CLK high	2			ns
MDIO						
MDIO4	$t_{su(MDV-MCKH)}$	Setup time, ESC_MDIO_DATA valid before ESC_MDIO_CLK high	20			ns
MDIO5	$t_{h(MCKH-MDV)}$	Hold time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	–1			ns

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6.15.9.4.2 EtherCAT Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Auto Shift Compensation						
MII7	$t_{d(TXCLK-TXDV)}$	Delay time, ESC_TXy_CLK to ESC_TXy_DATA[3:0] and ESC_TXy_ENA	20 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK\_100)}$		30 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK\_100)}$	ns
MDIO						
MDIO1	$t_{c(MCK)}$	Cycle time, ESC_MDIO_CLK		400		ns
MDIO2/MDIO3	$t_{w(MCK)}$	Pulse duration, ESC_MDIO_CLK high or low	160		240	ns
MDIO7	$t_{d(MCKH-MDV)}$	Delay time, ESC_MDIO_CLK high to ESC_MDIO_DATA valid			$0.5t_{c(MCK)} + 30$	ns
	$t_{v(MCKH-MDV)}$	Valid time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	$0.5t_{c(MCK)} – 3.0$			ns

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6.15.9.4.3 EtherCAT Timing Diagrams

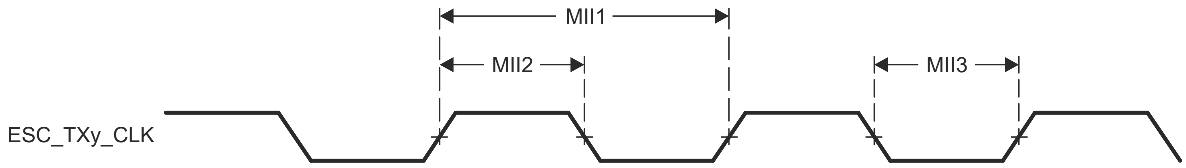

Figure 6-103. EtherCAT Transmit Clock Timing (MII Operation)

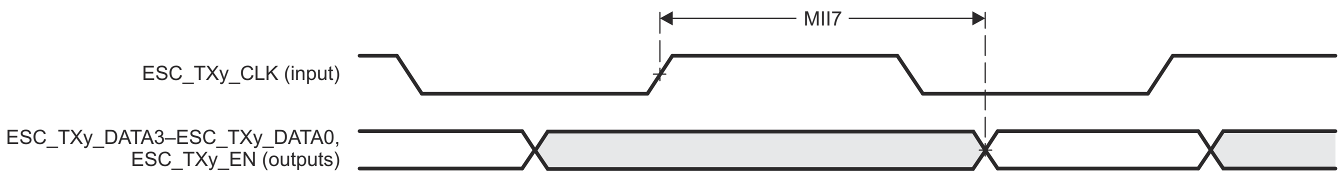

Figure 6-104. EtherCAT Transmit Interface Timing (MII Operation)

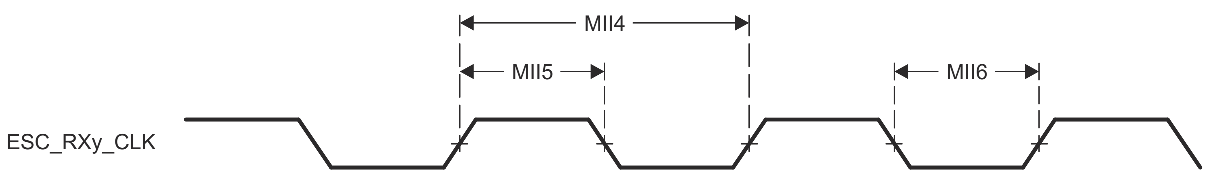

Figure 6-105. EtherCAT Receive Clock Timing (MII Operation)

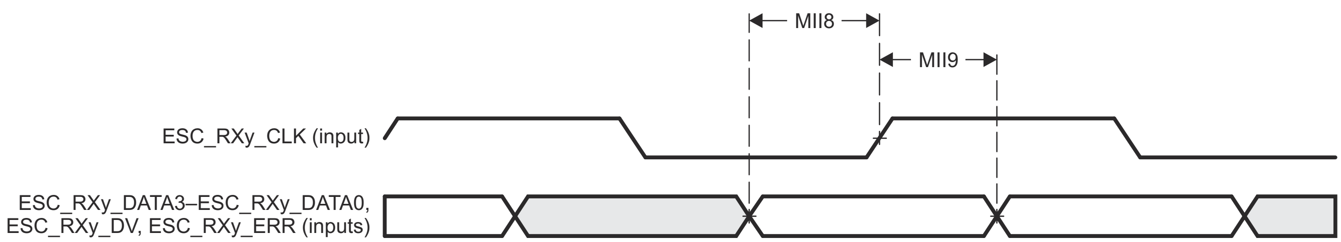

Figure 6-106. EtherCAT Receive Interface Timing (MII Operation)

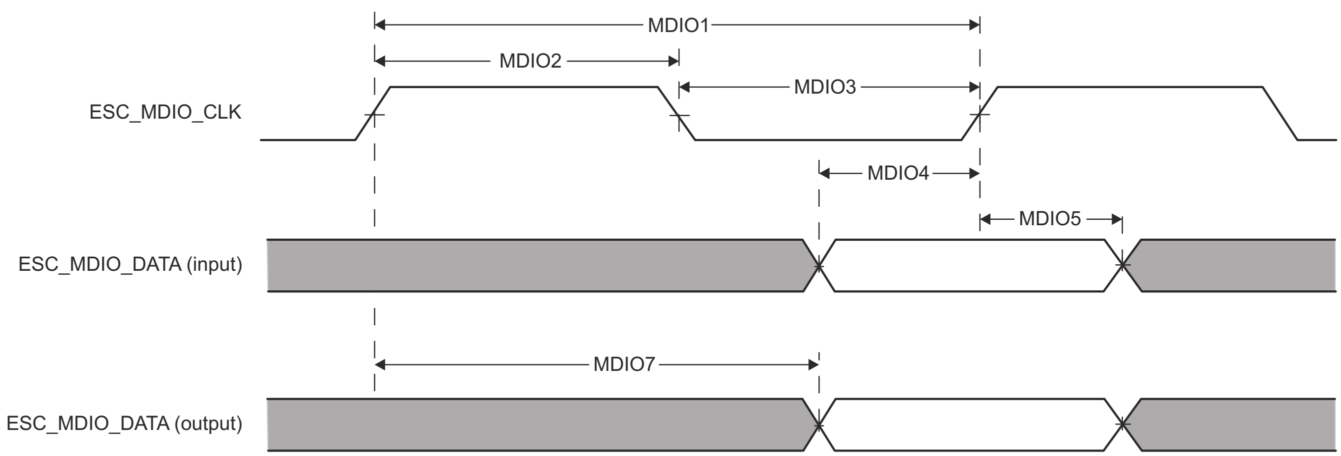

Figure 6-107. EtherCAT MDIO Timing Diagrams

6.15.10 Universal Serial Bus (USB)

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed and low-speed operation
- Integrated PHY
- Three transfer types: control, interrupt, and bulk
- 32 endpoints
  - One dedicated control IN endpoint and one dedicated control OUT endpoint
  - 15 configurable IN endpoints and 15 configurable OUT endpoints
- 4KB of dedicated endpoint memory

Figure 6-108 shows the USB block diagram.

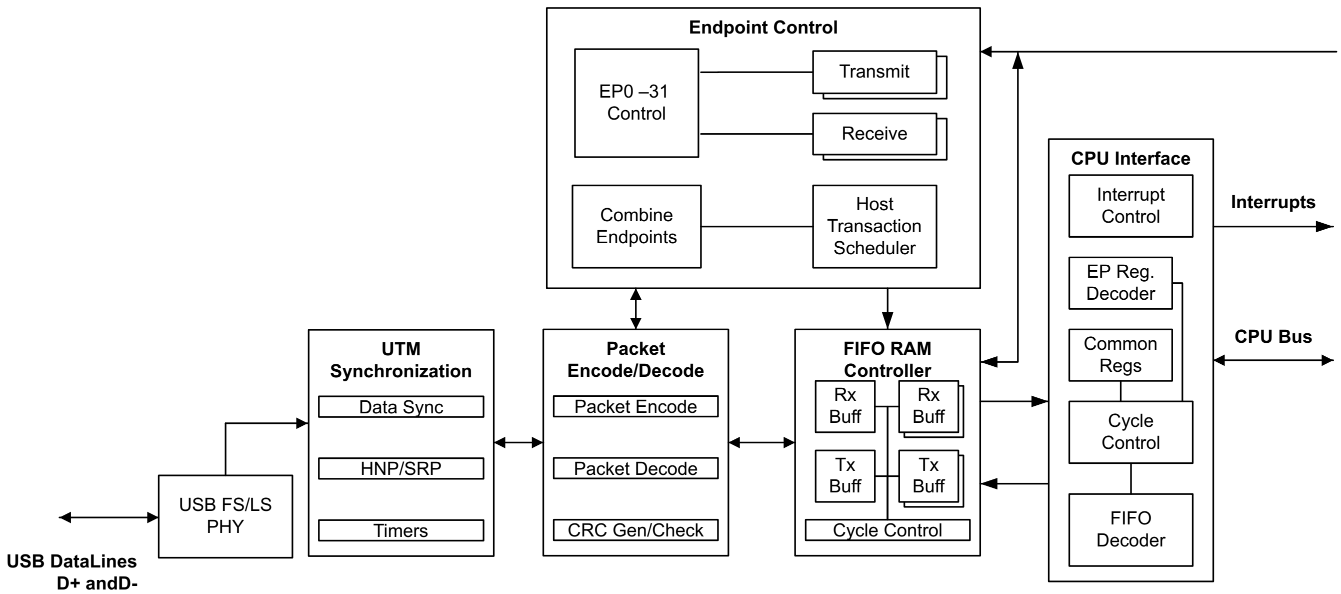

Figure 6-108. USB Block Diagram

Note

The accuracy of the on-chip zero-pin oscillator (see the *INTOSC Characteristics* section) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB. For applications using the USB boot mode, see the *Boot ROM and Peripheral Booting* section for clock frequency requirements.

6.15.10.1 USB Electrical Data and Timing

6.15.10.1.1 USB Input Ports DP and DM Timing Requirements

		MIN	MAX	UNIT
V(CM)	Differential input common mode range	0.8	2.5	V
Z(IN)	Input impedance	300		kΩ
VCRS	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic-low level	0.8		V
V_{IH}	Static SE input logic-high level		2.0	V
VDI	Differential input voltage		0.2	V

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6.15.10.1.2 USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single-ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single-ended	USB 2.0 load conditions	0	0.3	V
Z(DRV)	D+, D– impedance		28	44	Ω
t_r	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_f	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

6.15.11 Universal Asynchronous Receiver-Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) module in this device contains the following features:

- Programmable baud-rate generator allowing speeds of up to 12.5Mbps for regular speed (divide by 16) and 25Mbps for high speed (divide by 8)
- Separate 16-level-deep and 8-bit-wide transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of ⅛, ¼, ½, ¾, and ⅞
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity-bit generation and detection
  - 1 or 2 stop-bit generation
- IrDA serial-IR (SIR) encoder and decoder providing:
  - Programmable use of IrDA SIR or UART input/output
  - Support of IrDA SIR encoder and decoder functions for data rates of up to 115.2Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41 to 2.23 μs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power-mode bit duration
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission (EOT) interrupts
- Efficient transfers using Micro Direct Memory Access (μDMA) Controller
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

Figure 6-109 shows the UART module block diagram.

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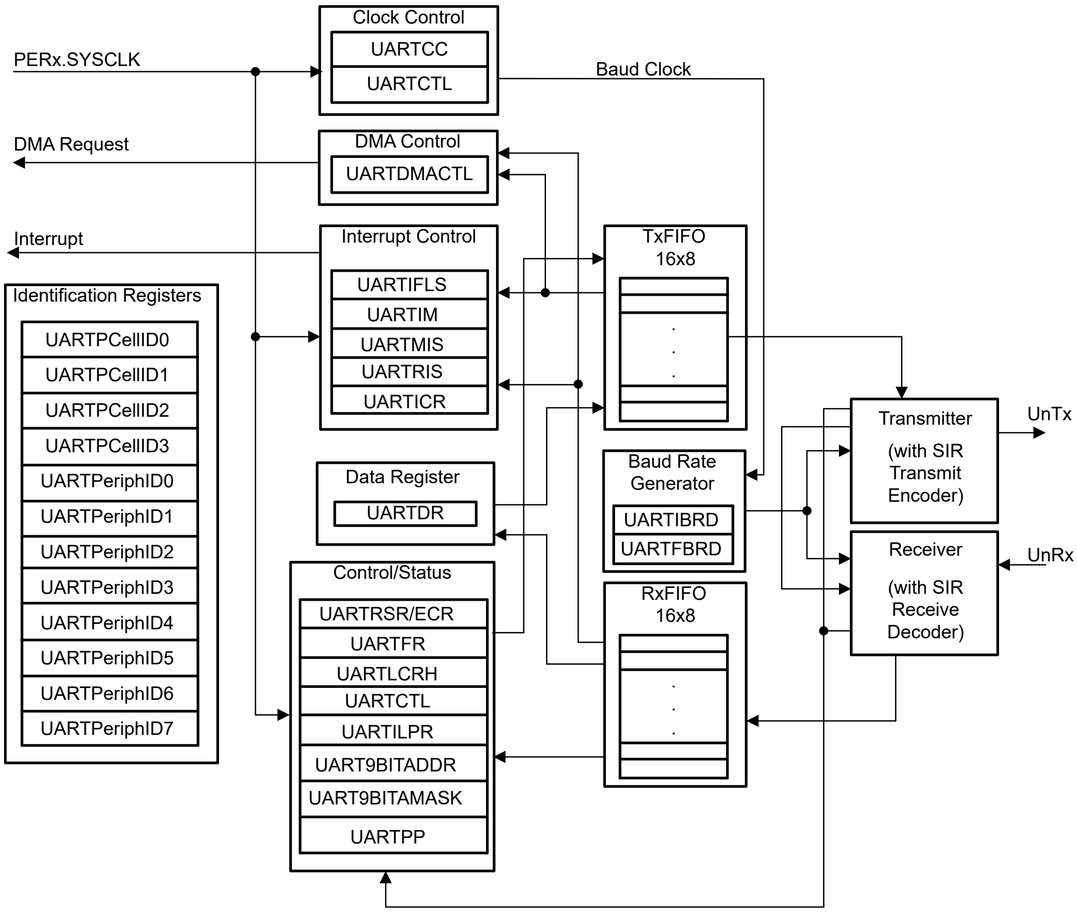

Figure 6-109. UART Module Block Diagram

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7 Detailed Description

7.1 Overview

The TMS320F28P65x (F28P65x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of IGBT, GaN, and SiC technologies.

These include such applications as:

- Industrial motor drives
- Motor control
  - Traction inverter motor control
  - HVAC motor control
  - Mobile robot motor control
- Solar inverters
  - Central inverter
  - Micro inverter
  - String inverter
- Digital power
- Electrical vehicles and transportation
- EV charging infrastructure
- Energy Storage systems
- Industrial & collaborative robot
- Industrial machine & machine tools
- Industrial mobile robot

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 200 MIPS of signal-processing performance in each core for floating- or fixed-point code running from either on-chip flash or SRAM. This is equivalent to the 400-MHz processing power on a Cortex®-M7 based device (C28x DSP core gives two times more performance than the Cortex®-M7 core).The C28x CPU is further boosted by the Trigonometric Math Unit (TMU) and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems. Extended instruction sets enable IEEE double-precision 64-bit floating-point math. Finally, the Control Law Accelerator (CLA) enables an additional 200 MIPS per core of independent processing ability. This is equivalent to the 280-MHz processing power on a Cortex®-M7 based device (CLA CPU gives 40% more performance than the Cortex®-M7 core).

The lockstep dual-CPU comparator option has been added in the secondary C28x CPU along with ePIE and DMA for detection of permanent and transient faults. To allow fast context switching from existing to new firmware, hardware enhancements for Live Firmware Update (LFU) have been added to F28P65x.

High-performance analog blocks are tightly integrated with the processing and control units to provide optimal real-time signal chain performance. The Analog-to-Digital Converter (ADC) has been enhanced with up to 40 analog channels, 22 of which have general-purpose input/output (GPIO) capability. Implementation of oversampling is greatly simplified with hardware improvement. For safety-critical ADC conversions, a hardware redundancy checker has been added that provides the ability to compare ADC conversion results from multiple ADC modules for consistency without additional CPU cycles. Thirty-six frequency-independent PWMs, all with high-resolution capability, enable control of multiple power stages, from 3-phase inverters to advanced multilevel power topologies. The PWMs have been enhanced with Minimum Dead-Band Logic (MINDL) and Illegal Combo Logic (ICL) features.

The inclusion of the Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

An EtherCAT SubDevice Controller and other industry-standard protocols like CAN FD and USB 2.0 are available on this device. The Fast Serial Interface (FSI) enables up to 200 Mbps of robust communications across an isolation boundary.

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As a highly connected device, the F28P65x also offers various security enablers to help designers implement their cyber security strategy and support features like hardware encryption, secure JTAG and secure Boot.

From a safety standpoint, F28P65x supports numerous safety enablers. For more details, see *Industrial Functional Safety for C2000™ Real-Time Microcontrollers* and *Automotive Functional Safety for C2000™ Real-Time Microcontrollers*.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD28P65X evaluation board and download C2000Ware.

7.2 Functional Block Diagram

Figure 7-1 shows the CPU system and associated peripherals.

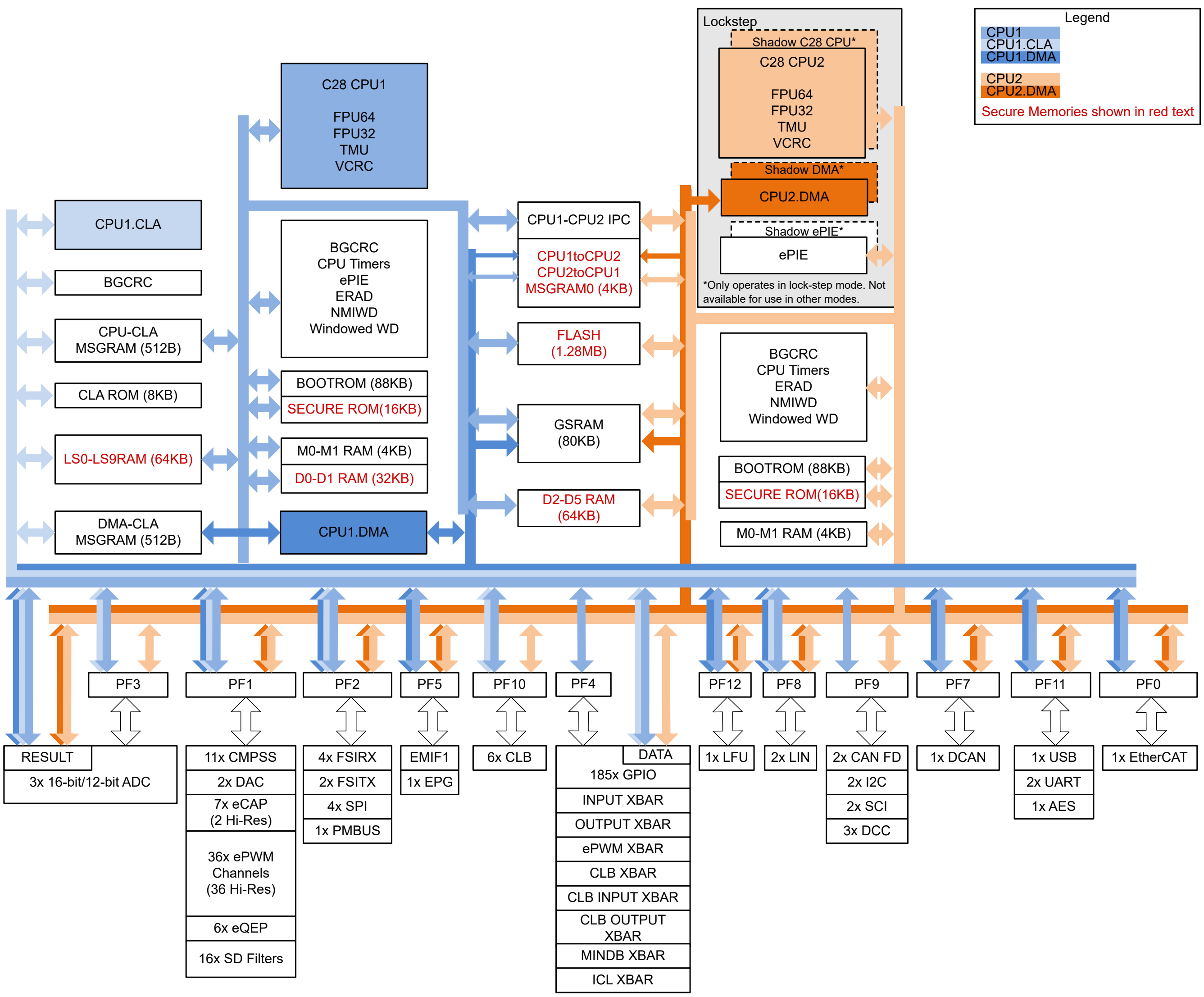

Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 C28x Memory Map

The C28x Memory Map table describes the C28x memory map. See the Memory Controller Module section of the System Control chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-1. C28x Memory Map

START ADDRESS	SIZE	CLA MEMORY	CPU1 MEMORY	CPU2 MEMORY	CLA ACCESS	DMA ACCESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
0x0000 0000	1K x 16	–	M0 RAM	M0 RAM			ECC	Yes	
0x0000 0400	1K x 16	–	M1 RAM	M1 RAM			ECC	Yes	
0x0000 0800	512 x 16	–	Reserved						
0x0000 0A00	768 x 16	–	Peripheral (ADC, Timers)		Yes				
0x0000 0D00	512 x 16	–	PieVectTable	PieVectTable					
0x0000 1480	128 x 16	CPU1.CLA to CPU1 MSGRAM		–	Yes		Parity		
0x0000 1500	128 x 16	CPU1 to CPU1.CLA MSGRAM		–	Yes		Parity		
0x0000 1680	128 x 16	CPU1.CLA to CPU1.DMA MSGRAM		–	Yes	Yes	Parity		
0x0000 1700	128 x 16	CPU1.DMA to CPU1.CLA MSGRAM		–	Yes	Yes	Parity		
0x0000 1800	10K x 16	–	Peripheral (CLB, Control, Analog, Comm, XBAR, GPIO)		Yes				
0x0000 4000	8K x 16	LS8 RAM(CLA1Prog)[3]			Yes		Parity	Yes	Yes
0x0000 6000	8K x 16	LS9 RAM(CLA1Prog)[3]			Yes		Parity	Yes	Yes
0x0000 8000	2K x 16	LS0 RAM (Can be used as CLA program/data or CPU1 local memory)		D2 RAM (CPU2 mapped)[2]	Yes		Parity	Yes	Yes
0x0000 8800	2K x 16	LS1 RAM (Can be used as CLA program/data or CPU1 local memory)			Yes		Parity	Yes	Yes
0x0000 9000	2K x 16	LS2 RAM (Can be used as CLA program/data or CPU1 local memory)			Yes		Parity	Yes	Yes
0x0000 9800	2K x 16	LS3 RAM (Can be used as CLA program/data or CPU1 local memory)			Yes		Parity	Yes	Yes
0x0000 A000	2K x 16	LS4 RAM (Can be used as CLA program/data or CPU1 local memory)		D3 RAM (CPU2 mapped)[2]	Yes		Parity	Yes	Yes
0x0000 A800	2K x 16	LS5 RAM (Can be used as CLA program/data or CPU1 local memory)			Yes		Parity	Yes	Yes
0x0000 B000	2K x 16	LS6 RAM (Can be used as CLA program/data or CPU1 local memory)			Yes		Parity	Yes	Yes
0x0000 B800	2K x 16	LS7 RAM (Can be used as CLA program/data or CPU1 local memory)			Yes		Parity	Yes	Yes
0x0000 C000	8K x 16	–	D0 RAM	D4 RAM (CPU2 mapped)[2]			Parity	Yes	Yes
0x0000 E000	8K x 16	–	D1 RAM	D5 RAM (CPU2 mapped)[2]			Parity	Yes	Yes
0x0000 F000	4K x16	CLA1 Data ROM			Yes		Parity		
0x0001 0000	8K x 16	–	GS0 RAM[1]			Yes	Parity	Yes	
0x0001 2000	8K x 16	–	GS1 RAM[1]			Yes	Parity	Yes	
0x0001 4000	8K x 16	–	GS2 RAM[1]			Yes	Parity	Yes	

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Table 7-1. C28x Memory Map (continued)

START ADDRESS	SIZE	CLA MEMORY	CPU1 MEMORY	CPU2 MEMORY	CLA ACCESS	DMA ACCESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
0x0001 6000	8K x 16	–	GS3 RAM(1)			Yes	Parity	Yes	
0x0001 8000	8K x 16	–	GS4 RAM(1)			Yes	Parity	Yes	
0x0001 A000	8K x 16	–	D2 RAM (CPU1 mapped) (2)	–			Parity	Yes	Yes
0x0001 C000	8K x 16	–	D3 RAM (CPU1 mapped) (2)	–			Parity	Yes	Yes
0x0001 E000	8K x 16	–	D4 RAM (CPU1 mapped) (2)	–			Parity	Yes	Yes
0x0002 0000	8K x 16	–	D5 RAM (CPU1 mapped) (2)	–			Parity	Yes	Yes
0x0002 2000	8K x 16	–	LS8 RAM (CPU1 mapped)	–			Parity	Yes	Yes
0x0002 4000	8K x 16	–	LS9 RAM (CPU1 mapped)	–			Parity	Yes	Yes
0x0003 0800	8K x 16	–	EtherCAT RAM (direct access)			Yes	Parity		
0x0003 A000	1K x 16	–	CPU1 to CPU2 MSGRAM0			Yes	Parity	Yes	Yes
0x0003 B000	1K x 16	–	CPU2 to CPU1 MSGRAM0			Yes	Parity	Yes	Yes
0x0004 1000	2K x 16	–	USB RAM			Yes			
0x0004 9000	2K x 16	–	CAN-A MSGRAM			Yes	Parity		
0x0005 9000	4K x 16	–	MCAN-A MSGRAM			Yes	ECC		
0x0005 B000	4K x 16	–	MCAN-B MSGRAM			Yes	ECC		
0x0007 2000	7.5K x 16	–	TI OTP(4)				ECC		
0x0007 8000	1K x 16	–	User DCSM OTP				ECC		Yes
0x0007 8800	1K x 16	–	User OTP Bank1				ECC		
0x0007 9000	1K x 16	–	User OTP Bank2				ECC		
0x0007 9800	1K x 16	–	User OTP Bank3				ECC		
0x0007 A000	1K x 16	–	User OTP Bank4				ECC		
0x0008 0000	640K x 16	–	Flash				ECC		Yes
0x003F 3000	8K x 16	–	Secure ROM	Secure ROM			Parity		Yes
0x003F 5000	45K x 16	–	Boot ROM	Boot ROM			Parity		
0x003F FFBE	1 x 16	–	Pie Vector Fetch Error (part of Boot ROM)	Pie Vector Fetch Error (part of Boot ROM)			Parity		
0x003F FFC0	64 x 16	–	Default Vectors (part of Boot ROM)	Default Vectors (part of Boot ROM)			Parity		
0x0101 1000	4K x 16	–	CLA Data ROM				Parity		

(1) Shared between CPU subsystems.
(2) Memory can be mapped either to CPU1 or CPU2.
(3) Used as CLA Program Memory only. CLA program fetches from LS8/LS9. CLA data access goes the the peripheral frames on this address range. See LSxMSEL register description for MSEL_LS8 and MSEL_LS9 for mapping details.
(4) TI OTP is for TI internal use only.

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7.3.2 Control Law Accelerator (CLA) Memory Map

Table 7-2 shows the CLA data ROM memory map. For information about the CLA program ROM, see the CLA Program ROM (CLAPROMCRC) chapter in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-2. CLA Data ROM Memory Map

MEMORY	START ADDRESS	END ADDRESS	LENGTH
FFT Tables (Load)	0x0101 1070	0x0101 186F	0x0800
Data (Load)	0x0101 1870	0x0101 1FF9	0x078A
Version (Load)	0x0101 1FFA	0x0101 1FFF	0x0006
FFT Tables (Run)	0x0000 F070	0x0000 F86F	0x0800
Data (Run)	0x0000 F870	0x0000 FFF9	0x078A
Version (Run)	0x0000 FFFA	0x0000 FFFF	0x0006

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7.3.3 Flash Memory Map

On the F28P65x devices, five flash banks (1.3MB [640KW]) are available. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress. The Addresses of Flash Sectors table lists the addresses of flash sectors available for each part number.

7.3.3.1 Addresses of Flash Sectors

Table 7-3. Flash Memory Map

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
ALL	TI OTP Bank 0 (for TI use)	1536 x 16	0x0007 2000	0x0007 25FF	128 x 16	0x0107 0400	0x0107 04BF
	TI OTP Bank 1 (for TI use)	1536 x 16	0x0007 3000	0x0007 35FF	128 x 16	0x0107 0600	0x0107 06BF
	TI OTP Bank 2 (for TI use)	1536 x 16	0x0007 4000	0x0007 45FF	128 x 16	0x0107 0800	0x0107 08BF
	TI OTP Bank 3 (for TI use)	1536 x 16	0x0007 5000	0x0007 55FF	128 x 16	0x0107 0A00	0x0107 0ABF
	TI OTP Bank 4 (for TI use)	1536 x 16	0x0007 6000	0x0007 65FF	128 x 16	0x0107 0C00	0x0107 0CBF
	User Bank 0 (DCSM OTP)	1K x 16	0x0007 8000	0x0007 83FF	128 x 16	0x0107 1000	0x0107 107F
	User OTP Bank 1	1K x 16	0x0007 8800	0x0007 88FF	128 x 16	0x0107 1080	0x0107 10FF
	User OTP Bank 2	1K x 16	0x0007 9000	0x0007 93FF	128 x 16	0x0107 1100	0x0107 117F
	User OTP Bank 3	1K x 16	0x0007 9800	0x0007 98FF	128 x 16	0x0107 1180	0x0107 11FF
	User OTP Bank 4	1K x 16	0x0007 A000	0x0007 A3FF	128 x 16	0x0107 1200	0x0107 127F
ALL	Bank 0[(1)]						
	Sector 0 to 127	128K x 16	0x0008 0000	0x0009 FFFF	16K x 16	0x0108 0000	0x0108 3FFF
	Bank 1[(1)]						
	Sector 0 to 127	128K x 16	0x000A 0000	0x000B FFFF	16K x 16	0x0108 4000	0x0108 7FFF
F28P65xDKx,F28P65xSKx,F28P65xSHx	Bank 2[(1)]						
	Sector 0 to 127	128K x 16	0x000C 0000	0x000D FFFF	16K x 16	0x0108 8000	0x0108 BFFF
F28P65xDKx,F28P65xSKx	Bank 3[(1)]						
	Sector 0 to 127	128K x 16	0x000E 0000	0x000F FFFF	16K x 16	0x0108 C000	0x0108 FFFF
F28P65xDKx,F28P65xSKx,F28P65xDHx	Bank 4[(1)]						
	Sector 0 to 127	128K x 16	0x0010 0000	0x0011 FFFF	16K x 16	0x0109 0000	0x0109 3FFF

(1) Refer to the Flash Sector Offsets table for sector details.

Table 7-4. Flash Sector Offsets

SECTOR	OFFSET FROM FLASH BANK START ADDRESS		OFFSET FROM FLASH BANK ECC START ADDRESS	
	SIZE	OFFSET	SIZE	OFFSET
Sector 0	1K x 16	0x0000 0000	128 x 16	0x0000 0000
Sector 1	1K x 16	0x0000 0400	128 x 16	0x0000 0080
Sector 2	1K x 16	0x0000 0800	128 x 16	0x0000 0100
Sector 3	1K x 16	0x0000 0C00	128 x 16	0x0000 0180
Sector 4	1K x 16	0x0000 1000	128 x 16	0x0000 0200
Sector 5	1K x 16	0x0000 1400	128 x 16	0x0000 0280
Sector 6	1K x 16	0x0000 1800	128 x 16	0x0000 0300
Sector 7	1K x 16	0x0000 1C00	128 x 16	0x0000 0380
Sector 8	1K x 16	0x0000 2000	128 x 16	0x0000 0400
Sector 9	1K x 16	0x0000 2400	128 x 16	0x0000 0480
Sector 10	1K x 16	0x0000 2800	128 x 16	0x0000 0500
Sector 11	1K x 16	0x0000 2C00	128 x 16	0x0000 0580

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Table 7-4. Flash Sector Offsets (continued)

SECTOR	OFFSET FROM FLASH BANK START ADDRESS		OFFSET FROM FLASH BANK ECC START ADDRESS	
	SIZE	OFFSET	SIZE	OFFSET
Sector 12	1K x 16	0x0000 3000	128 x 16	0x0000 0600
Sector 13	1K x 16	0x0000 3400	128 x 16	0x0000 0680
Sector 14	1K x 16	0x0000 3800	128 x 16	0x0000 0700
Sector 15	1K x 16	0x0000 3C00	128 x 16	0x0000 0780
Sector 16	1K x 16	0x0000 4000	128 x 16	0x0000 0800
Sector 17	1K x 16	0x0000 4400	128 x 16	0x0000 0880
Sector 18	1K x 16	0x0000 4800	128 x 16	0x0000 0900
Sector 19	1K x 16	0x0000 4C00	128 x 16	0x0000 0980
Sector 20	1K x 16	0x0000 5000	128 x 16	0x0000 0A00
Sector 21	1K x 16	0x0000 5400	128 x 16	0x0000 0A80
Sector 22	1K x 16	0x0000 5800	128 x 16	0x0000 0B00
Sector 23	1K x 16	0x0000 5C00	128 x 16	0x0000 0B80
Sector 24	1K x 16	0x0000 6000	128 x 16	0x0000 0C00
Sector 25	1K x 16	0x0000 6400	128 x 16	0x0000 0C80
Sector 26	1K x 16	0x0000 6800	128 x 16	0x0000 0D00
Sector 27	1K x 16	0x0000 6C00	128 x 16	0x0000 0D80
Sector 28	1K x 16	0x0000 7000	128 x 16	0x0000 0E00
Sector 29	1K x 16	0x0000 7400	128 x 16	0x0000 0E80
Sector 30	1K x 16	0x0000 7800	128 x 16	0x0000 0F00
Sector 31	1K x 16	0x0000 7C00	128 x 16	0x0000 0F80
Sector 32	1K x 16	0x0000 8000	128 x 16	0x0000 1000
Sector 33	1K x 16	0x0000 8400	128 x 16	0x0000 1080
Sector 34	1K x 16	0x0000 8800	128 x 16	0x0000 1100
Sector 35	1K x 16	0x0000 8C00	128 x 16	0x0000 1180
Sector 36	1K x 16	0x0000 9000	128 x 16	0x0000 1200
Sector 37	1K x 16	0x0000 9400	128 x 16	0x0000 1280
Sector 38	1K x 16	0x0000 9800	128 x 16	0x0000 1300
Sector 39	1K x 16	0x0000 9C00	128 x 16	0x0000 1380
Sector 40	1K x 16	0x0000 A000	128 x 16	0x0000 1400
Sector 41	1K x 16	0x0000 A400	128 x 16	0x0000 1480
Sector 42	1K x 16	0x0000 A800	128 x 16	0x0000 1500
Sector 43	1K x 16	0x0000 AC00	128 x 16	0x0000 1580
Sector 44	1K x 16	0x0000 B000	128 x 16	0x0000 1600
Sector 45	1K x 16	0x0000 B400	128 x 16	0x0000 1680
Sector 46	1K x 16	0x0000 B800	128 x 16	0x0000 1700
Sector 47	1K x 16	0x0000 BC00	128 x 16	0x0000 1780
Sector 48	1K x 16	0x0000 C000	128 x 16	0x0000 1800
Sector 49	1K x 16	0x0000 C400	128 x 16	0x0000 1880
Sector 50	1K x 16	0x0000 C800	128 x 16	0x0000 1900
Sector 51	1K x 16	0x0000 CC00	128 x 16	0x0000 1980
Sector 52	1K x 16	0x0000 D000	128 x 16	0x0000 1A00
Sector 53	1K x 16	0x0000 D400	128 x 16	0x0000 1A80
Sector 54	1K x 16	0x0000 D800	128 x 16	0x0000 1B00
Sector 55	1K x 16	0x0000 DC00	128 x 16	0x0000 1B80
Sector 56	1K x 16	0x0000 E000	128 x 16	0x0000 1C00
Sector 57	1K x 16	0x0000 E400	128 x 16	0x0000 1C80
Sector 58	1K x 16	0x0000 E800	128 x 16	0x0000 1D00
Sector 59	1K x 16	0x0000 EC00	128 x 16	0x0000 1D80
Sector 60	1K x 16	0x0000 F000	128 x 16	0x0000 1E00

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Table 7-4. Flash Sector Offsets (continued)

SECTOR	OFFSET FROM FLASH BANK START ADDRESS		OFFSET FROM FLASH BANK ECC START ADDRESS	
	SIZE	OFFSET	SIZE	OFFSET
Sector 61	1K x 16	0x0000 F400	128 x 16	0x0000 1E80
Sector 62	1K x 16	0x0000 F800	128 x 16	0x0000 1F00
Sector 63	1K x 16	0x0000 FC00	128 x 16	0x0000 1F80
Sector 64	1K x 16	0x0001 0000	128 x 16	0x0000 2000
Sector 65	1K x 16	0x0001 0400	128 x 16	0x0000 2080
Sector 66	1K x 16	0x0001 0800	128 x 16	0x0000 2100
Sector 67	1K x 16	0x0001 0C00	128 x 16	0x0000 2180
Sector 68	1K x 16	0x0001 1000	128 x 16	0x0000 2200
Sector 69	1K x 16	0x0001 1400	128 x 16	0x0000 2280
Sector 70	1K x 16	0x0001 1800	128 x 16	0x0000 2300
Sector 71	1K x 16	0x0001 1C00	128 x 16	0x0000 2380
Sector 72	1K x 16	0x0001 2000	128 x 16	0x0000 2400
Sector 73	1K x 16	0x0001 2400	128 x 16	0x0000 2480
Sector 74	1K x 16	0x0001 2800	128 x 16	0x0000 2500
Sector 75	1K x 16	0x0001 2C00	128 x 16	0x0000 2580
Sector 76	1K x 16	0x0001 3000	128 x 16	0x0000 2600
Sector 77	1K x 16	0x0001 3400	128 x 16	0x0000 2680
Sector 78	1K x 16	0x0001 3800	128 x 16	0x0000 2700
Sector 79	1K x 16	0x0001 3C00	128 x 16	0x0000 2780
Sector 80	1K x 16	0x0001 4000	128 x 16	0x0000 2800
Sector 81	1K x 16	0x0001 4400	128 x 16	0x0000 2880
Sector 82	1K x 16	0x0001 4800	128 x 16	0x0000 2900
Sector 83	1K x 16	0x0001 4C00	128 x 16	0x0000 2980
Sector 84	1K x 16	0x0001 5000	128 x 16	0x0000 2A00
Sector 85	1K x 16	0x0001 5400	128 x 16	0x0000 2A80
Sector 86	1K x 16	0x0001 5800	128 x 16	0x0000 2B00
Sector 87	1K x 16	0x0001 5C00	128 x 16	0x0000 2B80
Sector 88	1K x 16	0x0001 6000	128 x 16	0x0000 2C00
Sector 89	1K x 16	0x0001 6400	128 x 16	0x0000 2C80
Sector 90	1K x 16	0x0001 6800	128 x 16	0x0000 2D00
Sector 91	1K x 16	0x0001 6C00	128 x 16	0x0000 2D80
Sector 92	1K x 16	0x0001 7000	128 x 16	0x0000 2E00
Sector 93	1K x 16	0x0001 7400	128 x 16	0x0000 2E80
Sector 94	1K x 16	0x0001 7800	128 x 16	0x0000 2F00
Sector 95	1K x 16	0x0001 7C00	128 x 16	0x0000 2F80
Sector 96	1K x 16	0x0001 8000	128 x 16	0x0000 3000
Sector 97	1K x 16	0x0001 8400	128 x 16	0x0000 3080
Sector 98	1K x 16	0x0001 8800	128 x 16	0x0000 3100
Sector 99	1K x 16	0x0001 8C00	128 x 16	0x0000 3180
Sector 100	1K x 16	0x0001 9000	128 x 16	0x0000 3200
Sector 101	1K x 16	0x0001 9400	128 x 16	0x0000 3280
Sector 102	1K x 16	0x0001 9800	128 x 16	0x0000 3300
Sector 103	1K x 16	0x0001 9C00	128 x 16	0x0000 3380
Sector 104	1K x 16	0x0001 A000	128 x 16	0x0000 3400
Sector 105	1K x 16	0x0001 A400	128 x 16	0x0000 3480
Sector 106	1K x 16	0x0001 A800	128 x 16	0x0000 3500
Sector 107	1K x 16	0x0001 AC00	128 x 16	0x0000 3580
Sector 108	1K x 16	0x0001 B000	128 x 16	0x0000 3600
Sector 109	1K x 16	0x0001 B400	128 x 16	0x0000 3680

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Table 7-4. Flash Sector Offsets (continued)

SECTOR	OFFSET FROM FLASH BANK START ADDRESS		OFFSET FROM FLASH BANK ECC START ADDRESS	
	SIZE	OFFSET	SIZE	OFFSET
Sector 110	1K x 16	0x0001 B800	128 x 16	0x0000 3700
Sector 111	1K x 16	0x0001 BC00	128 x 16	0x0000 3780
Sector 112	1K x 16	0x0001 C000	128 x 16	0x0000 3800
Sector 113	1K x 16	0x0001 C400	128 x 16	0x0000 3880
Sector 114	1K x 16	0x0001 C800	128 x 16	0x0000 3900
Sector 115	1K x 16	0x0001 CC00	128 x 16	0x0000 3980
Sector 116	1K x 16	0x0001 D000	128 x 16	0x0000 3A00
Sector 117	1K x 16	0x0001 D400	128 x 16	0x0000 3A80
Sector 118	1K x 16	0x0001 D800	128 x 16	0x0000 3B00
Sector 119	1K x 16	0x0001 DC00	128 x 16	0x0000 3B80
Sector 120	1K x 16	0x0001 E000	128 x 16	0x0000 3C00
Sector 121	1K x 16	0x0001 E400	128 x 16	0x0000 3C80
Sector 122	1K x 16	0x0001 E800	128 x 16	0x0000 3D00
Sector 123	1K x 16	0x0001 EC00	128 x 16	0x0000 3D80
Sector 124	1K x 16	0x0001 F000	128 x 16	0x0000 3E00
Sector 125	1K x 16	0x0001 F400	128 x 16	0x0000 3E80
Sector 126	1K x 16	0x0001 F800	128 x 16	0x0000 3F00
Sector 127	1K x 16	0x0001 FC00	128 x 16	0x0000 3F80

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7.3.4 EMIF Chip Select Memory Map

The EMIF1 memory map is the same for both CPU subsystems. The EMIF memory map is shown in the EMIF Chip Select Memory Map table.

Table 7-5. EMIF Chip Select Memory Map

EMIF CS	SIZE(2)	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EMIF1 CS0n - Data(1)	256M x 16	0x8000 0000	0x8FFF FFFF		Yes
EMIF1 CS0n - Program + Data(1)	512K x 16	0x0028 0000	0x002F FFFF		Yes
EMIF1 CS2n - Program + Data	256K x 16	0x0030 0000	0x0033 FFFF		Yes
EMIF1 CS3n - Program + Data	256K x 16	0x0034 0000	0x0037 FFFF		Yes
EMIF1 CS4n - Program + Data	393K x 16	0x0038 0000	0x003D FFFF		Yes

(1) Dual Map - When EMIF1 CS0n is mapped at address 0x2x_xxxx, EMIF1 CS2n is only avaialble from 0x30_0000 to 0x33_FFFF (512K x 16).
(2) Available memory size listed in this table is the maximum possible size assuming 32-bit memory. This may not apply to other memory sizes because of pin mux setting.

7.3.5 Peripheral Registers Memory Map

Table 7-6. Peripheral Registers Memory Map

Structure	DriverLib Name	Base Address	CPU1	CPU1.DMA	CPU1.CLA1	CPU2	CPU2.DMA	Pipeline Protected
Peripheral Frame 0 (PF0)								
ADC_RESULT_REGS	ADCARESULT_BASE	0x0000_0A00	YES	YES	YES	YES	YES	-
ADC_RESULT_REGS	ADCBRESULT_BASE	0x0000_0A80	YES	YES	YES	YES	YES	-
ADC_RESULT_REGS	ADCCRESULT_BASE	0x0000_0B00	YES	YES	YES	YES	YES	-
CPUTIMER_REGS	CPUTIMER0_BASE	0x0000_0C00	YES	-	-	YES	-	-
CLA_ONLY_REGS	CLA1_ONLY_BASE	0x0000_0C00	-	-	YES	-	-	-
CPUTIMER_REGS	CPUTIMER1_BASE	0x0000_0C08	YES	-	-	YES	-	-
CPUTIMER_REGS	CPUTIMER2_BASE	0x0000_0C10	YES	-	-	YES	-	-
PIE_CTRL_REGS	PIECTRL_BASE	0x0000_0CE0	YES	-	-	YES	-	-
CLA_SOFTINT_REGS	CLA1_SOFTINT_BASE	0x0000_0CE0	-	-	YES	-	-	-
PIE_VECT_TABLE	PIEVECTTABLEMAIN_BASE	0x0000_0D00	YES	-	-	YES	-	-
PIE_VECT_TABLE	PIEVECTTABLEEXTENSION_BASE	0x0000_0E00	YES	-	-	YES	-	-
DMA_REGS	DMA_BASE	0x0000_1000	YES	-	-	YES	-	-
DMA_CH_REGS	DMA_CH1_BASE	0x0000_1020	YES	-	-	YES	-	-
DMA_CH_REGS	DMA_CH2_BASE	0x0000_1040	YES	-	-	YES	-	-
DMA_CH_REGS	DMA_CH3_BASE	0x0000_1060	YES	-	-	YES	-	-
DMA_CH_REGS	DMA_CH4_BASE	0x0000_1080	YES	-	-	YES	-	-
DMA_CH_REGS	DMA_CH5_BASE	0x0000_10A0	YES	-	-	YES	-	-
DMA_CH_REGS	DMA_CH6_BASE	0x0000_10C0	YES	-	-	YES	-	-
CLA_REGS	CLA1_BASE	0x0000_1400	YES	-	-	-	-	-
ESCSS_REGS	ESC_SS_BASE	0x0005_7E00	YES	-	-	YES	-	YES
ESCSS_CONFIG_REGS	ESC_SS_CONFIG_BASE	0x0005_7F00	YES	-	-	YES	-	YES
PCTRACE_BUFFER_REGS	ERAD_PCTRACE_BUFFER_BASE	0x0005_FE00	YES	-	-	YES	-	YES
UID_REGS	UID_BASE	0x0007_2172	YES	-	-	-	-	-
DCSM_Z1_OTP	DCSM_Z1OTP_BASE	0x0007_8000	YES	-	-	-	-	-
DCSM_Z2_OTP	DCSM_Z2OTP_BASE	0x0007_8200	YES	-	-	-	-	-
Peripheral Frame 1 (PF1)								
EPWM_REGS	EPWM17_BASE	0x0000_2C00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM17XCMP_BASE	0x0000_2D00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM17DE_BASE	0x0000_2DC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM17MINDBLUT_BASE	0x0000_2DE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM18_BASE	0x0000_2E00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM18XCMP_BASE	0x0000_2F00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM18DE_BASE	0x0000_2FC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM18MINDBLUT_BASE	0x0000_2FE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM1_BASE	0x0000_3000	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM1XCMP_BASE	0x0000_3100	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM1DE_BASE	0x0000_31C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM1MINDBLUT_BASE	0x0000_31E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM2_BASE	0x0000_3200	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM2XCMP_BASE	0x0000_3300	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM2DE_BASE	0x0000_33C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM2MINDBLUT_BASE	0x0000_33E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM3_BASE	0x0000_3400	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM3XCMP_BASE	0x0000_3500	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM3DE_BASE	0x0000_35C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM3MINDBLUT_BASE	0x0000_35E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM4_BASE	0x0000_3600	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM4XCMP_BASE	0x0000_3700	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM4DE_BASE	0x0000_37C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM4MINDBLUT_BASE	0x0000_37E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM5_BASE	0x0000_3800	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM5XCMP_BASE	0x0000_3900	YES	YES	YES	YES	YES	YES

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Table 7-6. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	CPU1	CPU1.DMA	CPU1.CLA1	CPU2	CPU2.DMA	Pipeline Protected
DE_REGS	EPWM5DE_BASE	0x0000_39C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM5MINDBLUT_BASE	0x0000_39E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM6_BASE	0x0000_3A00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM6XCMP_BASE	0x0000_3B00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM6DE_BASE	0x0000_3BC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM6MINDBLUT_BASE	0x0000_3BE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM7_BASE	0x0000_3C00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM7XCMP_BASE	0x0000_3D00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM7DE_BASE	0x0000_3DC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM7MINDBLUT_BASE	0x0000_3DE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM8_BASE	0x0000_3E00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM8XCMP_BASE	0x0000_3F00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM8DE_BASE	0x0000_3FC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM8MINDBLUT_BASE	0x0000_3FE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM9_BASE	0x0000_4000	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM9XCMP_BASE	0x0000_4100	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM9DE_BASE	0x0000_41C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM9MINDBLUT_BASE	0x0000_41E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM10_BASE	0x0000_4200	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM10XCMP_BASE	0x0000_4300	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM10DE_BASE	0x0000_43C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM10MINDBLUT_BASE	0x0000_43E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM11_BASE	0x0000_4400	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM11XCMP_BASE	0x0000_4500	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM11DE_BASE	0x0000_45C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM11MINDBLUT_BASE	0x0000_45E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM12_BASE	0x0000_4600	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM12XCMP_BASE	0x0000_4700	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM12DE_BASE	0x0000_47C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM12MINDBLUT_BASE	0x0000_47E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM13_BASE	0x0000_4800	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM13XCMP_BASE	0x0000_4900	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM13DE_BASE	0x0000_49C0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM13MINDBLUT_BASE	0x0000_49E0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM14_BASE	0x0000_4A00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM14XCMP_BASE	0x0000_4B00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM14DE_BASE	0x0000_4BC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM14MINDBLUT_BASE	0x0000_4BE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM15_BASE	0x0000_4C00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM15XCMP_BASE	0x0000_4D00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM15DE_BASE	0x0000_4DC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM15MINDBLUT_BASE	0x0000_4DE0	YES	YES	YES	YES	YES	YES
EPWM_REGS	EPWM16_BASE	0x0000_4E00	YES	YES	YES	YES	YES	YES
EPWM_XCMP_REGS	EPWM16XCMP_BASE	0x0000_4F00	YES	YES	YES	YES	YES	YES
DE_REGS	EPWM16DE_BASE	0x0000_4FC0	YES	YES	YES	YES	YES	YES
MINDB_LUT_REGS	EPWM16MINDBLUT_BASE	0x0000_4FE0	YES	YES	YES	YES	YES	YES
EQEP_REGS	EQEP1_BASE	0x0000_5080	YES	YES	YES	YES	YES	YES
EQEP_REGS	EQEP2_BASE	0x0000_50C0	YES	YES	YES	YES	YES	YES
EQEP_REGS	EQEP3_BASE	0x0000_5100	YES	YES	YES	YES	YES	YES
EQEP_REGS	EQEP4_BASE	0x0000_5140	YES	YES	YES	YES	YES	YES
EQEP_REGS	EQEP5_BASE	0x0000_5180	YES	YES	YES	YES	YES	YES
EQEP_REGS	EQEP6_BASE	0x0000_51C0	YES	YES	YES	YES	YES	YES
ECAP_REGS	ECAP1_BASE	0x0000_5200	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP1SIGNALMONITORING_BASE	0x0000_5240	YES	YES	YES	YES	YES	YES

Table 7-6. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	CPU1	CPU1.DMA	CPU1.CLA1	CPU2	CPU2.DMA	Pipeline Protected
ECAP_REGS	ECAP2_BASE	0x0000_5300	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP2SIGNALMONITORING_BASE	0x0000_5340	YES	YES	YES	YES	YES	YES
ECAP_REGS	ECAP3_BASE	0x0000_5400	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP3SIGNALMONITORING_BASE	0x0000_5440	YES	YES	YES	YES	YES	YES
ECAP_REGS	ECAP4_BASE	0x0000_5500	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP4SIGNALMONITORING_BASE	0x0000_5540	YES	YES	YES	YES	YES	YES
ECAP_REGS	ECAP5_BASE	0x0000_5600	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP5SIGNALMONITORING_BASE	0x0000_5640	YES	YES	YES	YES	YES	YES
ECAP_REGS	ECAP6_BASE	0x0000_5700	YES	YES	YES	YES	YES	YES
HRCAP_REGS	HRCAP6_BASE	0x0000_5720	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP6SIGNALMONITORING_BASE	0x0000_5740	YES	YES	YES	YES	YES	YES
ECAP_REGS	ECAP7_BASE	0x0000_5800	YES	YES	YES	YES	YES	YES
HRCAP_REGS	HRCAP7_BASE	0x0000_5820	YES	YES	YES	YES	YES	YES
ECAP_SIGNAL_MONITORING	ECAP7SIGNALMONITORING_BASE	0x0000_5840	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS1_BASE	0x0000_5900	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS2_BASE	0x0000_5940	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS3_BASE	0x0000_5980	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS4_BASE	0x0000_59C0	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS5_BASE	0x0000_5A00	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS6_BASE	0x0000_5A40	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS7_BASE	0x0000_5A80	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS8_BASE	0x0000_5AC0	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS9_BASE	0x0000_5B00	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS10_BASE	0x0000_5B40	YES	YES	YES	YES	YES	YES
CMPSS_REGS	CMPSS11_BASE	0x0000_5B80	YES	YES	YES	YES	YES	YES
DAC_REGS	DACA_BASE	0x0000_5C00	YES	YES	YES	YES	YES	YES
DAC_REGS	DACC_BASE	0x0000_5C20	YES	YES	YES	YES	YES	YES
HRPWMCAL_REGS	HRPWMCAL1_BASE	0x0000_5C80	YES	YES	YES	YES	YES	YES
HRPWMCAL_REGS	HRPWMCAL2_BASE	0x0000_5CC0	YES	YES	YES	YES	YES	YES
HRPWMCAL_REGS	HRPWMCAL3_BASE	0x0000_5D00	YES	YES	YES	YES	YES	YES
SDFM_REGS	SDFM1_BASE	0x0000_5E00	YES	YES	YES	YES	YES	YES
SDFM_REGS	SDFM2_BASE	0x0000_5E80	YES	YES	YES	YES	YES	YES
SDFM_REGS	SDFM3_BASE	0x0000_5F00	YES	YES	YES	YES	YES	YES
SDFM_REGS	SDFM4_BASE	0x0000_5F80	YES	YES	YES	YES	YES	YES
Peripheral Frame 2 (PF2)								
SPI_REGS	SPIA_BASE	0x0000_6100	YES	YES	YES	YES	YES	YES
SPI_REGS	SPIB_BASE	0x0000_6110	YES	YES	YES	YES	YES	YES
SPI_REGS	SPIC_BASE	0x0000_6120	YES	YES	YES	YES	YES	YES
SPI_REGS	SPID_BASE	0x0000_6130	YES	YES	YES	YES	YES	YES
BGCRC_REGS	BGCRC_CPU_BASE	0x0000_6340	YES	-	-	YES	-	YES
BGCRC_REGS	BGCRC_CLA_BASE	0x0000_6380	YES	-	YES	-	-	YES
PMBUS_REGS	PMBUSA_BASE	0x0000_6400	YES	YES	YES	YES	YES	YES
FSI_TX_REGS	FSITXA_BASE	0x0000_6600	YES	YES	YES	YES	YES	YES
FSI_RX_REGS	FSIRXA_BASE	0x0000_6680	YES	YES	YES	YES	YES	YES
FSI_TX_REGS	FSITXB_BASE	0x0000_6700	YES	YES	YES	YES	YES	YES
FSI_RX_REGS	FSIRXB_BASE	0x0000_6780	YES	YES	YES	YES	YES	YES
FSI_RX_REGS	FSIRXC_BASE	0x0000_6880	YES	YES	YES	YES	YES	YES
FSI_RX_REGS	FSIRXD_BASE	0x0000_6980	YES	YES	YES	YES	YES	YES
Peripheral Frame 3 (PF3)								
ADC_REGS	ADCA_BASE	0x0000_7400	YES	-	YES	YES	-	YES
ADC_REGS	ADCB_BASE	0x0000_7500	YES	-	YES	YES	-	YES
ADC_REGS	ADCC_BASE	0x0000_7600	YES	-	YES	YES	-	YES
Peripheral Frame 4 (PF4)								
EPWM_XBAR_REGS	EPWMXBARB_BASE	0x0000_7800	YES	-	-	-	-	YES

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Table 7-6. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	CPU1	CPU1.DMA	CPU1.CLA1	CPU2	CPU2.DMA	Pipeline Protected
SYNC_SOC_REGS	SYNCSOC_BASE	0x0000_78F8	YES	-	-	-	-	YES
INPUT_XBAR_REGS	INPUTXBAR_BASE	0x0000_7900	YES	-	-	-	-	YES
XBAR_REGS	XBAR_BASE	0x0000_7920	YES	-	-	-	-	YES
INPUT_XBAR_REGS	CLBINPUTXBAR_BASE	0x0000_7960	YES	-	-	-	-	YES
CPU1_DMA_CLA_SRC_SEL_REGS, CPU2_DMA_CLA_SRC_SEL_REGS	CPU1DMACLASRCSEL_BASE, CPU2DMACLASRCSEL_BASE	0x0000_7980	YES	-	-	YES	-	YES
MINDB_XBAR_REGS	MINDBXBAR_BASE	0x0000_79C0	YES	-	-	-	-	YES
ICL_XBAR_REGS	ICLXBAR_BASE	0x0000_79E0	YES	-	-	-	-	YES
EPWM_XBAR_REGS	EPWMXBARA_BASE	0x0000_7A00	YES	-	-	-	-	YES
CLB_XBAR_REGS	CLBXBAR_BASE	0x0000_7A80	YES	-	-	-	-	YES
OUTPUT_XBAR_EXT64_REGS	OUTPUTXBAR_BASE	0x0000_7B00	YES	-	-	-	-	YES
OUTPUT_XBAR_REGS	CLBOUTPUTXBAR_BASE	0x0000_7B80	YES	-	-	-	-	YES
GPIO_CTRL_REGS	GPIOCTRL_BASE	0x0000_7C00	YES	-	-	-	-	YES
GPIO_DATA_REGS	GPIODATA_BASE	0x0000_7F00	YES	-	YES	YES	-	YES
GPIO_DATA_READ_REGS	GPIODATAREAD_BASE	0x0000_7F80	YES	-	YES	YES	-	YES
Peripheral Frame 5 (PF5)								
EMIF_REGS	EMIF1_BASE	0x0004_7000	YES	-	-	YES	-	YES
CPU1TOCPU2_IPC_REGS_CPU2VIEW	IPC_CPUXTOCPUX_BASE	0x0005_CE00	-	-	-	YES	-	YES
CPU1TOCPU2_IPC_REGS_CPU1VIEW	IPC_CPUXTOCPUX_BASE	0x0005_CE00	YES	-	-	-	-	YES
DEV_CFG_REGS	DEVCFG_BASE	0x0005_D000	YES	-	-	YES	-	YES
CLK_CFG_REGS	CLKCFG_BASE	0x0005_D200	YES	-	-	YES	-	YES
CPU1_SYS_REGS, CPU2_SYS_REGS	CPU1SYS_BASE, CPU2SYS_BASE	0x0005_D300	YES	-	-	YES	-	YES
CPU1_SYS_STATUS_REGS, CPU2_SYS_STATUS_REGS	CPU1SYSSTATUS_BASE, CPU2SYSSTATUS_BASE	0x0005_D400	YES	-	-	YES	-	YES
CPU1_PERIPH_AC_REGS, CPU2_PERIPH_AC_REGS	CPU1PERIPHAC_BASE, CPU2PERIPHAC_BASE	0x0005_D500	YES	-	-	YES	-	YES
ANALOG_SUBSYS_REGS	ANALOGSUBSYS_BASE	0x0005_D700	YES	-	-	-	-	YES
ERAD_GLOBAL_REGS	ERAD_GLOBAL_BASE	0x0005_E800	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP1_BASE	0x0005_E900	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP2_BASE	0x0005_E908	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP3_BASE	0x0005_E910	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP4_BASE	0x0005_E918	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP5_BASE	0x0005_E920	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP6_BASE	0x0005_E928	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP7_BASE	0x0005_E930	YES	-	-	YES	-	YES
ERAD_HWBP_REGS	ERAD_HWBP8_BASE	0x0005_E938	YES	-	-	YES	-	YES
ERAD_COUNTER_REGS	ERAD_COUNTER1_BASE	0x0005_E980	YES	-	-	YES	-	YES
ERAD_COUNTER_REGS	ERAD_COUNTER2_BASE	0x0005_E990	YES	-	-	YES	-	YES
ERAD_COUNTER_REGS	ERAD_COUNTER3_BASE	0x0005_E9A0	YES	-	-	YES	-	YES
ERAD_COUNTER_REGS	ERAD_COUNTER4_BASE	0x0005_E9B0	YES	-	-	YES	-	YES
ERAD_CRC_GLOBAL_REGS	ERAD_CRC_GLOBAL_BASE	0x0005_EA00	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC1_BASE	0x0005_EA10	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC2_BASE	0x0005_EA20	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC3_BASE	0x0005_EA30	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC4_BASE	0x0005_EA40	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC5_BASE	0x0005_EA50	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC6_BASE	0x0005_EA60	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC7_BASE	0x0005_EA70	YES	-	-	YES	-	YES
ERAD_CRC_REGS	ERAD_CRC8_BASE	0x0005_EA80	YES	-	-	YES	-	YES
PCTRACE_REGS	ERAD_PCTRACE_BASE	0x0005_EAD0	YES	-	-	YES	-	YES
EPG_REGS	EPG_BASE	0x0005_EC00	YES	-	-	YES	-	YES
EPG_MUX_REGS	EPGMUX_BASE	0x0005_ECD0	YES	-	-	YES	-	YES

Table 7-6. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	CPU1	CPU1.DMA	CPU1.CLA1	CPU2	CPU2.DMA	Pipeline Protected
ADC_SAFECHECK_INTEVT_REGS	ADCSAFETYINTEVTAGG1_BASE	0x0005_EE00	YES	-	-	-	-	YES
ADC_SAFECHECK_INTEVT_REGS	ADCSAFETYINTEVTAGG2_BASE	0x0005_EE40	-	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK1_BASE	0x0005_EE80	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK2_BASE	0x0005_EE90	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK3_BASE	0x0005_EEA0	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK4_BASE	0x0005_EEB0	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK5_BASE	0x0005_EEC0	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK6_BASE	0x0005_EED0	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK7_BASE	0x0005_EEE0	YES	-	-	YES	-	YES
ADC_SAFECHECK_REGS	ADCSAFETYCHK8_BASE	0x0005_EEF0	YES	-	-	YES	-	YES
DCSM_Z1_REGS	DCSM_Z1_BASE	0x0005_F000	YES	-	-	YES	-	YES
DCSM_Z2_REGS	DCSM_Z2_BASE	0x0005_F080	YES	-	-	YES	-	YES
DCSM_COMMON_REGS	DCSMCOMMON_BASE	0x0005_F0C0	YES	-	-	YES	-	YES
MEM_CFG_REGS	MEMCFG_BASE	0x0005_F400	YES	-	-	YES	-	YES
EMIF1_CONFIG_REGS	EMIF1CONFIG_BASE	0x0005_F4C0	YES	-	-	YES	-	YES
ACCESS_PROTECTION_REGS	ACCESSPROTECTION_BASE	0x0005_F500	YES	-	-	YES	-	YES
MEMORY_ERROR_REGS	MEMORYERROR_BASE	0x0005_F540	YES	-	-	YES	-	YES
ROM_WAIT_STATE_REGS	ROMWAITSTATE_BASE	0x0005_F580	YES	-	-	YES	-	YES
TEST_ERROR_REGS	TESTERROR_BASE	0x0005_F590	YES	-	-	YES	-	YES
FLASH_CTRL_REGS	FLASH0CTRL_BASE	0x0005_F800	YES	-	-	YES	-	YES
FLASH_ECC_REGS	FLASH0ECC_BASE	0x0005_FB00	YES	-	-	YES	-	YES
Peripheral Frame 7 (PF7)								
CAN_REGS	CANA_BASE	0x0004_8000	YES	YES	-	YES	YES	YES
LCM_REGS	LCM_CPU2_BASE	0x0004_C800	-	-	-	YES	-	YES
LCM_REGS	LCM_CPU2.DMA1_BASE	0x0004_E800	-	-	-	YES	-	YES
MCANSS_REGS	MCANASS_BASE	0x0005_A400	YES	-	-	YES	-	YES
MCAN_REGS	MCANA_BASE	0x0005_A600	YES	-	-	YES	-	YES
MCAN_ERROR_REGS	MCANA_ERROR_BASE	0x0005_A800	YES	-	-	YES	-	YES
MCANSS_REGS	MCANBSS_BASE	0x0005_C400	YES	-	-	YES	-	YES
MCAN_REGS	MCANB_BASE	0x0005_C600	YES	-	-	YES	-	YES
MCAN_ERROR_REGS	MCANB_ERROR_BASE	0x0005_C800	YES	-	-	YES	-	YES
DCC_REGS	DCC0_BASE	0x0005_E700	YES	-	-	YES	-	YES
DCC_REGS	DCC1_BASE	0x0005_E740	YES	-	-	YES	-	YES
DCC_REGS	DCC2_BASE	0x0005_E780	YES	-	-	YES	-	YES
Peripheral Frame 8 (PF8)								
LIN_REGS	LINA_BASE	0x0000_6E00	YES	YES	YES	YES	YES	YES
LIN_REGS	LINB_BASE	0x0000_6F00	YES	YES	YES	YES	YES	YES
Peripheral Frame 9 (PF9)								
WD_REGS	WD_BASE	0x0000_7000	YES	-	-	YES	-	YES
NMI_INTRUPT_REGS	NMI_BASE	0x0000_7060	YES	-	-	YES	-	YES
XINT_REGS	XINT_BASE	0x0000_7070	YES	-	-	YES	-	YES
SCI_REGS	SCIA_BASE	0x0000_7200	YES	-	-	YES	-	YES
SCI_REGS	SCIB_BASE	0x0000_7210	YES	-	-	YES	-	YES
I2C_REGS	I2CA_BASE	0x0000_7300	YES	-	-	YES	-	YES
I2C_REGS	I2CB_BASE	0x0000_7340	YES	-	-	YES	-	YES
Peripheral Frame 10 (PF10)								
CLB_LOGIC_CONFIG_REGS	CLB1_LOGICCFG_BASE	0x0000_2000	YES	-	YES	YES	-	YES
CLB_LOGIC_CONTROL_REGS	CLB1_LOGICCTRL_BASE	0x0000_2100	YES	-	YES	YES	-	YES
CLB_DATA_EXCHANGE_REGS	CLB1_DATAEXCH_BASE	0x0000_2180	YES	-	YES	YES	-	YES
CLB_LOGIC_CONFIG_REGS	CLB2_LOGICCFG_BASE	0x0000_2200	YES	-	YES	YES	-	YES
CLB_LOGIC_CONTROL_REGS	CLB2_LOGICCTRL_BASE	0x0000_2300	YES	-	YES	YES	-	YES

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Table 7-6. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	CPU1	CPU1.DMA	CPU1.CLA1	CPU2	CPU2.DMA	Pipeline Protected
CLB_DATA_EXCHANGE_REGS	CLB2_DATAEXCH_BASE	0x0000_2380	YES	-	YES	YES	-	YES
CLB_LOGIC_CONFIG_REGS	CLB3_LOGICCFG_BASE	0x0000_2400	YES	-	YES	YES	-	YES
CLB_LOGIC_CONTROL_REGS	CLB3_LOGICCTRL_BASE	0x0000_2500	YES	-	YES	YES	-	YES
CLB_DATA_EXCHANGE_REGS	CLB3_DATAEXCH_BASE	0x0000_2580	YES	-	YES	YES	-	YES
CLB_LOGIC_CONFIG_REGS	CLB4_LOGICCFG_BASE	0x0000_2600	YES	-	YES	YES	-	YES
CLB_LOGIC_CONTROL_REGS	CLB4_LOGICCTRL_BASE	0x0000_2700	YES	-	YES	YES	-	YES
CLB_DATA_EXCHANGE_REGS	CLB4_DATAEXCH_BASE	0x0000_2780	YES	-	YES	YES	-	YES
CLB_LOGIC_CONFIG_REGS	CLB5_LOGICCFG_BASE	0x0000_2800	YES	-	YES	YES	-	YES
CLB_LOGIC_CONTROL_REGS	CLB5_LOGICCTRL_BASE	0x0000_2900	YES	-	YES	YES	-	YES
CLB_DATA_EXCHANGE_REGS	CLB5_DATAEXCH_BASE	0x0000_2980	YES	-	YES	YES	-	YES
CLB_LOGIC_CONFIG_REGS	CLB6_LOGICCFG_BASE	0x0000_2A00	YES	-	YES	YES	-	YES
CLB_LOGIC_CONTROL_REGS	CLB6_LOGICCTRL_BASE	0x0000_2B00	YES	-	YES	YES	-	YES
CLB_DATA_EXCHANGE_REGS	CLB6_DATAEXCH_BASE	0x0000_2B80	YES	-	YES	YES	-	YES
Peripheral Frame 11 (PF11)								
USB_REGS	USBA_BASE	0x0004_0000	YES	YES	-	YES	YES	YES
AES_REGS	AESA_BASE	0x0004_2000	YES	YES	-	YES	YES	YES
AES_SS_REGS	AESA_SS_BASE	0x0004_2C00	YES	YES	-	YES	YES	YES
UART_REGS, UART_REGS_WRITE	UARTA_BASE, UARTAWRITE_BASE	0x0006_A000	YES	YES	-	YES	YES	YES
UART_REGS, UART_REGS_WRITE	UARTB_BASE, UARTBWRITE_BASE	0x0006_A800	YES	YES	-	YES	YES	YES
Peripheral Frame 12 (PF12)								
CPU1_LFU_REGS, CPU2_LFU_REGS	CPU1LFU_BASE, CPU2LFU_BASE	0x0000_7FE0	YES	-	YES	YES	-	YES

7.3.6 Memory Types

7.3.6.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has dedicated ECC-capable RAM blocks: M0, M1 and Dx. M0/M1 memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). Dx memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection). D2-D5 memory blocks are mappable to either of the CPUs. When mapped to CPU1, D2-D5 memories cannot be accessed by CPU2. Conversely, when D2-D5 memories are mapped to CPU2, CPU1 will not have access to these memory blocks.

7.3.6.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have ECC. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

Table 7-7 lists the initiator access for the LSx RAM.

Table 7-7. Initiator Access for LSx RAM (With Assumption That all Other Access Protections are Disabled)

MSEL_LSx[1]	CLAPGM_LSx	CPU ALLOWED ACCESS	CLA ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

1. MSEL_LS8 and MSEL_LS9 do not have corresponding CLAPGM_LSx bits. If MSEL_LS8 or MSEL_LS9 bits are '1', then these memory blocks are only allocated to CLA program memory

7.3.6.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Each shared RAM block can be owned by either CPU subsystem based on the configuration of respective bits in the GSxMSEL register.

All GSx RAM blocks have parity.

When a GSx RAM block is owned by a CPU subsystem, the CPUx and CPUx.DMA will have full access to that RAM block whereas the other CPUy and CPUy.DMA will only have read access (no fetch/write access).

Table 7-8 lists the initiator access for the GSx RAM.

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Table 7-8. Initiator Access for GSx RAM (With Assumption That all Other Access Protections are Disabled)

GSxMSEL	CPU	INSTRUCTION FETCH	READ	WRITE	CPUx.DMA READ	CPUx.DMA WRITE
0	CPU1	Yes	Yes	Yes	Yes	Yes
	CPU2	–	Yes	–	Yes	–
1	CPU1	–	Yes	–	Yes	–
	CPU2	Yes	Yes	Yes	Yes	Yes

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

7.3.6.4 CPU Message RAM (CPU MSGRAM)

These RAM blocks can be used to share data between CPU1 and CPU2. Since these RAMs are used for interprocessor communication, they are also called IPC RAMs. The CPU MSGRAMs have CPU/DMA read/write access from its own CPU subsystem, and CPU/DMA read only access from the other subsystem.

This RAM has parity.

7.3.6.5 CLA Message RAM (CLA MSGRAM)

These RAM blocks can be used to share data between the CPU and CLA. The CLA has read and write access to the CLA-to-CPU MSGRAM. The CPU has read and write access to the CPU-to-CLA MSGRAM. The CPU and CLA both have read access to both MSGRAMs. This RAM has parity.

7.3.6.6 CLA - DMA Message RAM (CLA-DMA MSGRAM)

These RAM blocks can be used to share data between the DMA and CLA. The CLA has read and write access to the CLA-to-DMA MSGRAM. The DMA has read and write access to the DMA-to-CLA MSGRAM. The DMA and CLA both have read access to both MSGRAMs. This RAM has parity.

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7.4 Identification

Table 7-9 lists the Device Identification Registers. Additional information on these device identification registers can be found in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*. See the register descriptions of PARTIDH and PARTIDL for identification of production status (TMX or TMS) and other device information.

Table 7-9. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDH	0x0005 D00A	2	Device part identification number	
			TMS320F28P650DK9	0x08FF 0800
			TMS320F28P650DK7	0x08FE 0800
			TMS320F28P650DK8	0x08FD 0800
			TMS320F28P659DK8	0x08FD 0800
			TMS320F28P650SK7	0x08FC 0800
			TMS320F28P650DK6	0x08FB 0800
			TMS320F28P650SK6	0x08FA 0800
			TMS320F28P659DH8	0x08F9 0800
			TMS320F28P650SH6	0x08F8 0800
			TMS320F28P659SH6	0x08F8 0800
			TMS320F28P650DH6	0x08F7 0800
			TMS320F28P650SH7	0x08F6 0800
REVID	0x0005 D00C	2	Silicon revision number	
			Revision 0	0x0000 0001
			Revision A	0x0000 0002
UID_UNIQUE	0x0007 2172	4	Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices.	

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7.5 Bus Architecture – Peripheral Connectivity

The C28x Bus Controller Peripheral Access table provides a broad view of the peripheral and configuration register accessibility from each bus controller on the C28x. Peripherals can be individually assigned to the CPU1 or CPU2 subsystem (for example, ePWM can be assigned to CPU1 and eQEP assigned to CPU2).

Table 7-10. C28x Bus Controller Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.DMA
Peripherals that can be assigned to CPU1 or CPU2 and have Secondary Controllers					
Peripheral Frame 1: - ePWM - SDFM - eCAP - eQEP - CMPSS - DAC - HRPWM	Y	Y	Y	Y	Y
Peripheral Frame 2: - SPI - FSI - PMBus	Y	Y	Y	Y	Y
Peripherals that can be assigned to CPU1 or CPU2 subsystems					
SCI			Y	Y	
I2C			Y	Y	
DCAN	Y		Y	Y	Y
CAN-FD			Y	Y	
ADC Configuration		Y	Y	Y	
EMIF1	Y		Y	Y	Y
EPG	Y		Y	Y	Y
USB	Y		Y	Y	Y
UART	Y		Y	Y	Y
EtherCAT	Y		Y	Y	Y
DCC			Y	Y	
Peripherals accessible only on CPU1					
Peripheral Reset, Peripheral CPU Select			Y		
GPIO Pin Mapping and Configuration			Y		
Analog System Control			Y		
Reset Configuration			Y		
Accessible by only one CPU at a time with Semaphore					
Clock and PLL Configuration			Y	Y	
Peripherals and Registers with Unique Copies of Registers for each CPU and CLA					
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y	Y	
Flash Configuration			Y	Y	
CPU Timers			Y	Y	

Table 7-10. C28x Bus Controller Peripheral Access (continued)

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.DMA
DMA and CLA Trigger Source Select			Y	Y	
ERAD			Y	Y	
GPIO Data		Y	Y	Y	
ADC Results	Y	Y	Y	Y	Y

7.6 Boot ROM

On every reset, the device executes a boot sequence in the ROM depending on the reset type and boot configuration. This sequence initializes the device to run the application code. For the CPU, the boot ROM also contains peripheral bootloaders that can be used to load an application into RAM. These bootloaders can be disabled for safety or security purposes.

Table 7-11 shows the boot features that are available for the C28x CPU. Additionally,Table 7-12 shows the sizes of the various ROMs on the device.

Table 7-11. Boot System Overview

BOOT FEATURE	CPU
Initial boot process	Device reset
Boot mode selection	GPIOs
Boot modes supported	Flash boot Secure Flash boot RAM boot FWU boot Wait boot
Peripheral boot loaders supported	Parallel IO SCI/Wait CAN CANFD I2C SPI

Table 7-12. ROM Memory

ROM	CPU SIZE
Secure and Unsecure boot ROM	64KB

7.6.1 Device Boot

This section describes the general boot ROM procedure each time a CPU core is reset. CPU1 always boots first. Once CPU1 boots to the application, then the user's application code in CPU1 can configure the CPU2 and releases CPU2 from reset to boot. Table 7-13 and Table 7-14 list the general boot-up procedures for each core.

During boot, each CPU's boot ROM code updates a boot status location in RAM that details the actions taken during this process. Additionally, CPU2 writes the boot status to the CPU2TOCPU1IPCBOOTSTS register to communicate the status to CPU1.

For more details, see the Boot Status information section of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

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Table 7-13. CPU1 Boot ROM Procedure

STEP	CPU1 ACTION
1	Initialize the device C28x CPU and M0/M1 RAM configuration
2	Initialize the device to use stack addressing mode, initialize DP to lower 64k and clear overflow mode bit
3	Trims are loaded from OTP and device configuration registers are programmed
4	On POR, all CPU RAMs (including GSxRAMs) are initialized. Boot continues once the 2KB RAMs are initialized
5	Non-maskable interrupt (NMI) handling is enabled and DCSM initialization is performed
6	If enabled, the MPOST POR memory test is run. The original clock frequency is NOT restored post MPOST execution
7	Pull-ups are enabled on unbonded IOs
8	Device calibration is performed, setting the analog trims. Then resets are handled and RAM is checked for initialization completion
9	The boot mode GPIO pins are polled to determine the boot mode to run. Boot loader is executed based on boot mode/ configurations. Refer to Boot Flow diagram in the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* for a flow chart of the boot sequences
10	After the application is loaded, the watchdog is enabled before executing application

Table 7-14. CPU2 Boot ROM Procedure

STEP	CPU1 ACTION
1	CPU2 release from reset by CPU1 application
2	Once CPU1TOCPU2IPCFLG0 is set, read the CPU1TOCPU2IPCBOOTMODE register. If it isn't set correctly or has an invalid value, IPC is sent to CPU1 and CPU2 waits forever. The user must reset CPU2 and set valid values
3	The flash is powered up and waits for power up to complete
4	On POR, all CPU2 RAMs (excluding GSxRAMs) are initialized (they are split into two initialization groups)
5	NMI is enabled
6	Initialize the device to configure lock step (not enable). This is to initialize the uninitialized flops in the device
7	Resets are handled
8	Using the value from CPU2 CPU1TOCPU2IPCBOOTMODE register, if "wait for command" mode is specified, a wait loop is entered that waits for CPU1 C28x to update the boot mode and set IPCFLG0. If a boot mode is specified, then boot ROM will enable watchdog and boot to the specified boot mode location
9	When IPCFLG0 is set in "wait for command" mode, watchdog is enabled, and then boot ROM runs the specified boot mode in CPU1TOCPU2IPCBOOTMODE

7.6.2 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-15 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See the *Reset XRSn Switching Characteristics* section and the Power-on Reset figure for $t_{boot\text{-}flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-15. Device Default Boot Modes

BOOT MODE	GPIO72 (Default Boot Mode Select Pin 1)	GPIO84 (Default Boot Mode Select Pin 0)
Parallel IO	0	0
SCI / Wait Boot(1)	0	1
CAN	1	0
Flash / USB(2)	1	1

(1) SCI boot mode is used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.
(2) On an unprogrammed device, selecting flash boot when the default flash entry address is unprogrammed will switch the boot mode from flash boot to USB boot. See Table 7-16 for more details.

Table 7-16. CPU1 Flash-to-USB Boot Decision Table

VALUE AT FLASH ENTRY POINT ADDRESS	REASON FOR VALUE	REALIZED BOOT MODE
0x00000000	Flash is locked/secured	Boot to Flash
0xFFFFFFFF	Flash is not programmed	USB Boot
Any other value	Flash is programmed	Boot to Flash

Note

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, the mode is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boot modes.

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7.6.3 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from 0 boot mode select pins up to 3 boot mode select pins as well as from 1 configured boot mode up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, etc)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot mode options)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to Configuring Boot Mode Pins section of the *TMS320F28P65x Real-Time Microcontroller Technical Reference Manual* for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=CAN Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to Configuring Boot Mode Table Options of the *TMS320F28P65x Real-Time Microcontroller Technical Reference Manual* for all the details on setting up and configuring the custom boot mode table.

Additionally, the Boot Mode Example Use Cases section of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* provides some example use cases on how to configure the BMSPs and custom boot tables.

Note

The CAN boot mode turns on the XTAL. Be sure an XTAL is installed in the application before using CAN boot mode.

7.6.4 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. See the Configuring Boot Mode Table Options section of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual* on how to configure BOOT_DEFx. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Default boot mode GPIO pins:

- Boot mode pin 0 - GPIO84
- Boot mode pin 1 - GPIO72

Guidelines on boot pin selection:

- Avoid pins that have PWM functionality.
- Can not be analog or USB pins.
- Boot mode select pins and default boot peripheral pins can be available on all packages.
- Avoid JTAG emulation pins and crystal pins.
- Boot mode select pins can be inputs.
- Pins can not have PHY bootstrap functionality.

Table 7-17. SCI Boot Options

Option	BOOTDEF Value	SCITXDA GPIO	SCIRXDA GPIO	Package Supported
0 (default)	0x01	GPIO12	GPIO13	All
1	0x21	GPIO84	GPIO85	All
2	0x41	GPIO36	GPIO35	176-QFP, 169-BGA, 256-BGA
3	0x61	GPIO42	GPIO43	All
4	0x81	GPIO65	GPIO64	All
5	0xA1	GPIO29	GPIO28	176-QFP, 169-BGA, 256-BGA
6	0xC1	GPIO8	GPIO9	176-QFP, 169-BGA, 256-BGA

Table 7-18. CAN Boot Options

Option	BOOTDEF Value	CANTXA GPIO	CANRXA GPIO	Package Supported
0 (default)	0x02	GPIO59	GPIO58	All
1	0x22	GPIO4	GPIO5	176-QFP, 169-BGA, 256-BGA
3	0x42	GPIO19	GPIO18	176-QFP, 169-BGA, 256-BGA
4	0x62	GPIO37	GPIO36	176-QFP, 169-BGA, 256-BGA
5	0x82	GPIO63	GPIO62	All

Table 7-19. CAN FD Boot Options

Option	BOOTDEF Value	MCAN TX	MCAN RX	Package Supported
0	0x08	GPIO4	GPIO10	All
1	0x18	GPIO8	GPIO10	176-QFP, 169-BGA, 256-BGA
2	0x28	GPIO19	GPIO18	176-QFP, 169-BGA, 256-BGA
3	0x38	GPIO4	GPIO5	176-QFP, 169-BGA, 256-BGA

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Table 7-19. CAN FD Boot Options (continued)

Option	BOOTDEF Value	MCAN TX	MCAN RX	Package Supported
4	0x48	GPIO74	GPIO75	176-QFP, 169-BGA, 256-BGA

Table 7-20. USB Boot Options

Option	Bootmode Value	USB0 DM	USB0 DP	Package Supported
0 (default)	0x09	GPIO42	GPIO43	All

Table 7-21. I2C Boot Options

Option	BOOTDEF Value	SDAA GPIO	SCLA GPIO	Package Supported
0	0x07	GPIO0	GPIO1	All
1	0x27	GPIO42	GPIO43	All
2	0x47	GPIO91	GPIO92	All
3	0x67	GPIO104	GPIO105	176-QFP, 169-BGA, 256-BGA

Table 7-22. SPI Boot Options

Option	BOOTDEF Value	SPIPICOA	SPIPOCIA	SPICLKA	SPIPTEA	Package Supported
0	0x06	GPIO58	GPIO59	GPIO34	GPIO35	All
1	0x26	GPIO198	GPIO203	GPIO204	GPIO205	176-QFP, 169-BGA, 256-BGA
2	0x46	GPIO16	GPIO17	GPIO18	GPIO19	176-QFP, 169-BGA, 256-BGA
3	0x66	GPIO54	GPIO55	GPIO56	GPIO57	176-QFP, 169-BGA, 256-BGA

Table 7-23. Parallel Boot Options

Option	BOOTDEF Value	D0-D7 GPIO	C28x (DSP) Control GPIO	Host Control GPIO	Package Supported
0 (default)	0x00	D0 - GPIO0 D1 - GPIO1 D2 - GPIO2 D3 - GPIO3 D4 - GPIO4 D5 - GPIO5 D6 - GPIO6 D7 - GPIO7	GPIO10	GPIO11	All
1	0x20	D0 - GPIO89 D1 - GPIO90 D2 - GPIO58 D3 - GPIO59 D4 - GPIO60 D5 - GPIO61 D6 - GPIO62 D7 - GPIO88	GPIO91	GPIO92	176-QFP, 256-BGA

7.7 Security

Security features are enforced by the Dual Code Security Module (DCSM). The primary layer of defense is securing the boundary of the chip, which should always be enabled. Additionally, the Dual Zone Security feature is available to support code partitioning.

7.7.1 Securing the Boundary of the Chip

The following two features, along with authentication in the firmware update code, should be used to help to prevent unauthorized code from running on the device.

7.7.1.1 JTAGLOCK

Enabling the JTAGLOCK feature in the USER OTP disables JTAG access (for example, debug probe) to resources on the device.

7.7.1.2 Zero-pin Boot

Enabling the Zero-pin Boot option along with Flash Boot in the USER OTP blocks all pin-based external bootloader options (for example, SCI, CAN, Parallel).

7.7.2 Dual-Zone Security

The dual-zone security mechanism offers protection for two zones: Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

7.7.3 Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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7.8 Advanced Encryption Standard (AES) Accelerator

The AES module provides hardware-accelerated data encryption and decryption operations based on a binary key. The AES is a symmetric cipher module that supports a 128-, 192-, or 256-bit key in hardware for encryption and decryption. The AES module is based on a symmetric algorithm, which means that the encryption and decryption keys are identical. To encrypt data means to convert it from plain text to an unintelligible form called cipher text. Decrypting cipher text converts previously encrypted data to its original plain text form. The main features of the AES accelerator are discussed below.

Basic AES encrypt and decrypt operations are supported by:

- Galois/Counter mode (GCM), with basic GHASH operation
- Counter mode with CBC-MAC (CCM)
- XTS mode

The following feedback operating modes are available:

- Electronic code book mode (ECB)
- Cipher block chaining mode (CBC)
- Counter mode (CTR)
- Cipher feedback mode (CFB), 128-bit
- F8 mode
- Key sizes: 128, 192, and 256 bits
- Support for CBC_MAC and Fedora 9 (F9) authentication modes
- Basic GHASH operation (when selecting no encryption)
- Key scheduling in hardware
- Support for µDMA transfers
- Fully synchronous design

Figure 7-2 shows the AES block diagram.

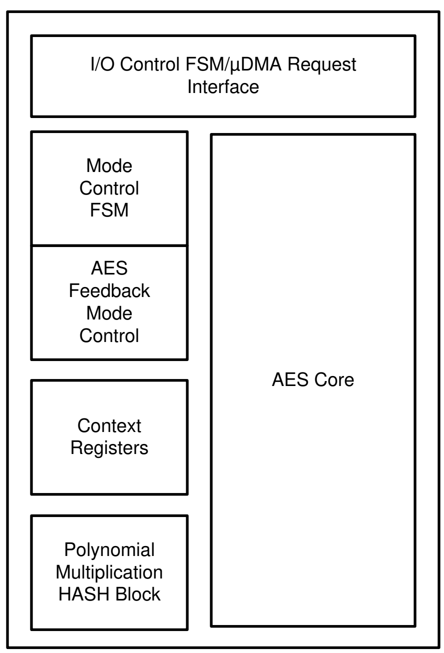

Figure 7-2. AES Block Diagram

For more information about the AES accelerator, see the Advanced Encryption Standard Accelerator (AES) chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

7.9 C28x (CPU1/CPU2) Subsystem

7.9.1 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*.

7.9.1.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information on the C28x Floating Point Unit (FPU), see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.9.1.2 Fast Integer Division Unit

The Fast Integer Division (FINTDIV) unit of the C28x CPU uniquely supports three types of integer division (Truncated, Modulus, Euclidean) of varying data type sizes (16/16, 32/16, 32/32, 64/32, 64/64) in unsigned or signed formats.

- Truncated integer division is naturally supported by C language (/, % operators).
- Modulus and Euclidean divisions are variants that are more efficient for control algorithms and are supported by C intrinsics.

All three types of integer division produce both a quotient and remainder component, are interruptible, and execute in a minimum number of deterministic cycles (10 cycles for a 32/32 division). In addition, the Fast Division capabilities of the C28x CPU uniquely support fast execution of floating-point 32-bit (in 5 cycles) and 64-bit (in 20 cycles) division.

For more information about fast integer division, see the *Fast Integer Division – A Differentiated Offering From C2000™ Product Family Application Report*.

7.9.1.3 Trigonometric Math Unit (TMU)

The trigonometric math unit (TMU) extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 7-24.

Table 7-24. TMU Supported Instructions

Instructions	C Equivalent Operation	Pipeline Cycles
MPY2PIF32 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32 RaH,RbH	a = b / 2pi	2/3
DIVF32 RaH,RbH,RcH	a = b/c	5

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Table 7-24. TMU Supported Instructions (continued)

Instructions	C Equivalent Operation	Pipeline Cycles
SQRTF32 RaH,RbH	a = sqrt(b)	5
SINPUF32 RaH,RbH	a = sin(b*2pi)	4
COSPUF32 RaH,RbH	a = cos(b*2pi)	4
ATANPUF32 RaH,RbH	a = atan(b)/2pi	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

Exponent instruction IEXP2F32 and logarithmic instruction LOG2F32 have been added to support computation of floating-point power function for the nonlinear proportional integral derivative control (NLPID) component of the C2000 Digital Control Library. These two added instructions reduce the power function calculations from a typical of 300 cycles using library emulation to less than 10 cycles.

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

For more information, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.9.1.4 VCRC Unit

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCRC can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCRC can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The following are the CRC polynomials used by the CRC calculation logic of the VCRC:

- CRC8 polynomial = 0x07
- CRC16 polynomial 1 = 0x8005
- CRC16 polynomial 2 = 0x1021
- CRC24 polynomial = 0x5d6dcb
- CRC32 polynomial 1 = 0x04c11db7
- CRC32 polynomial 2 = 0x1edc6f41

This module can calculate CRCs for a byte of data in a single cycle. The CRC calculation for CRC8, CRC16, CRC24, and CRC32 is done byte-wise (instead of computing on a complete 16-bit or 32-bit data read by the C28x core) to match the byte-wise computation requirement mandated by various standards.

The VCRC Unit also allows the user to provide the size (1b-32b) and value of any polynomial to fit custom CRC requirements. The CRC execution time increases to three cycles when using a custom polynomial.

For more information on the Cyclic Redundancy Check (VCRC) instruction sets, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.9.1.5 Lockstep Compare Module (LCM)

Hardware module integrity during run-time is a critical functional safety requirement. Hardware Redundancy implemented by the lockstep CPU architecture (two CPUs executing the same function and the output of the CPUs are continuously compared) is a proven method for achieving high diagnostic coverage for both permanent and transient faults. The Lockstep Comparator Module (LCM) is implemented to compare output from the C28x CPU to detect permanent and transient faults.

The LCM implements the following features:

- Pipelined architecture
- Redundant comparison
- Self-test capability
  - Match and mismatch test
  - Error forcing capability
- Temporal redundancy: The operation of the two modules is skewed by two cycles to address the issue of common cause failures like failure of clock, power, and so on. This makes sure of temporal redundancy.
- Spatial redundancy: Each module is physically separate and their outputs are compared. The physical separation provides spatial redundancy.
- Non-delayed functional output path to provide non-delayed CPU execution for the system (while still having temporal redundancy).
- Register protection of critical memory mapped registers of the module, using a parity scheme.

Figure 7-3 shows the LCM block diagram.

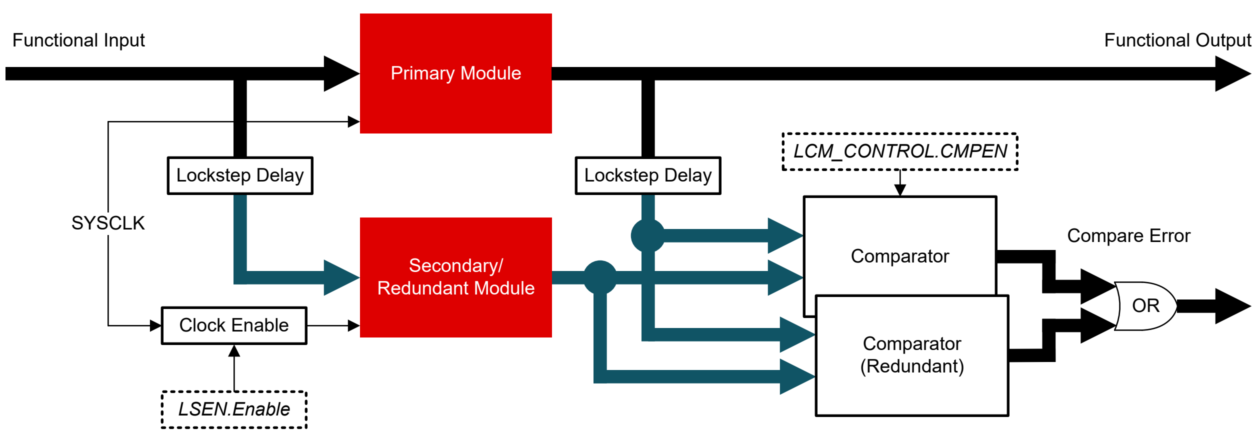

Figure 7-3. LCM Block Diagram

Note

The *Module* described in this block diagram can be either a CPU (for example, CPU1) or a peripheral (for example, DMA) depending on availability for the device.

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7.9.2 Control Law Accelerator (CLA)

The CLA Type-2 is an independent, fully programmable, 32-bit floating-point math processor that brings concurrent control-loop execution to the C28x family. The low interrupt-latency of the CLA allows it to read ADC samples "just-in-time." This significantly reduces the ADC sample to output delay to enable faster system response and higher MHz control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics.

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Using the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently.

The following is a list of major features of the CLA:

- C compilers are available for CLA software development
- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
  - Complete bus architecture:
    - Program Address Bus (PAB) and Program Data Bus (PDB)
    - Data Read Address Bus (DRAB), Data Read Data Bus (DRDB), Data Write Address Bus (DWAB), and Data Write Data Bus (DWDB)
  - Independent 8-stage pipeline.
  - 16-bit program counter (MPC)
  - Four 32-bit result registers (MR0 to MR3)
  - Two 16-bit auxiliary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions
  - Conditional branch and call
  - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines, or seven tasks and a main background task.
  - The start address of each task is specified by the MVECT registers.
  - No limit on task size as long as the tasks fit within the configurable CLA program memory space.
  - One task is serviced at a time until its completion. There is no nesting of tasks.
  - Upon task completion a task-specific interrupt is flagged within the PIE.
  - When a task finishes the next highest-priority pending task is automatically started.
  - The Type-2 CLA can have a main task that runs continuously in the background, while other high-priority events trigger a foreground task.
- Task trigger mechanisms:
  - C28x CPU through the IACK instruction
  - Task1 to Task8: up to 256 possible trigger sources from peripherals connected to the shared bus on which the CLA assumes secondary ownership.
  - Task8 can be set to be the background task, while Tasks 1 to 7 take peripheral triggers.
- Memory and Shared Peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU.
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
  - Two dedicated message RAMs for communication between the CLA and the DMA

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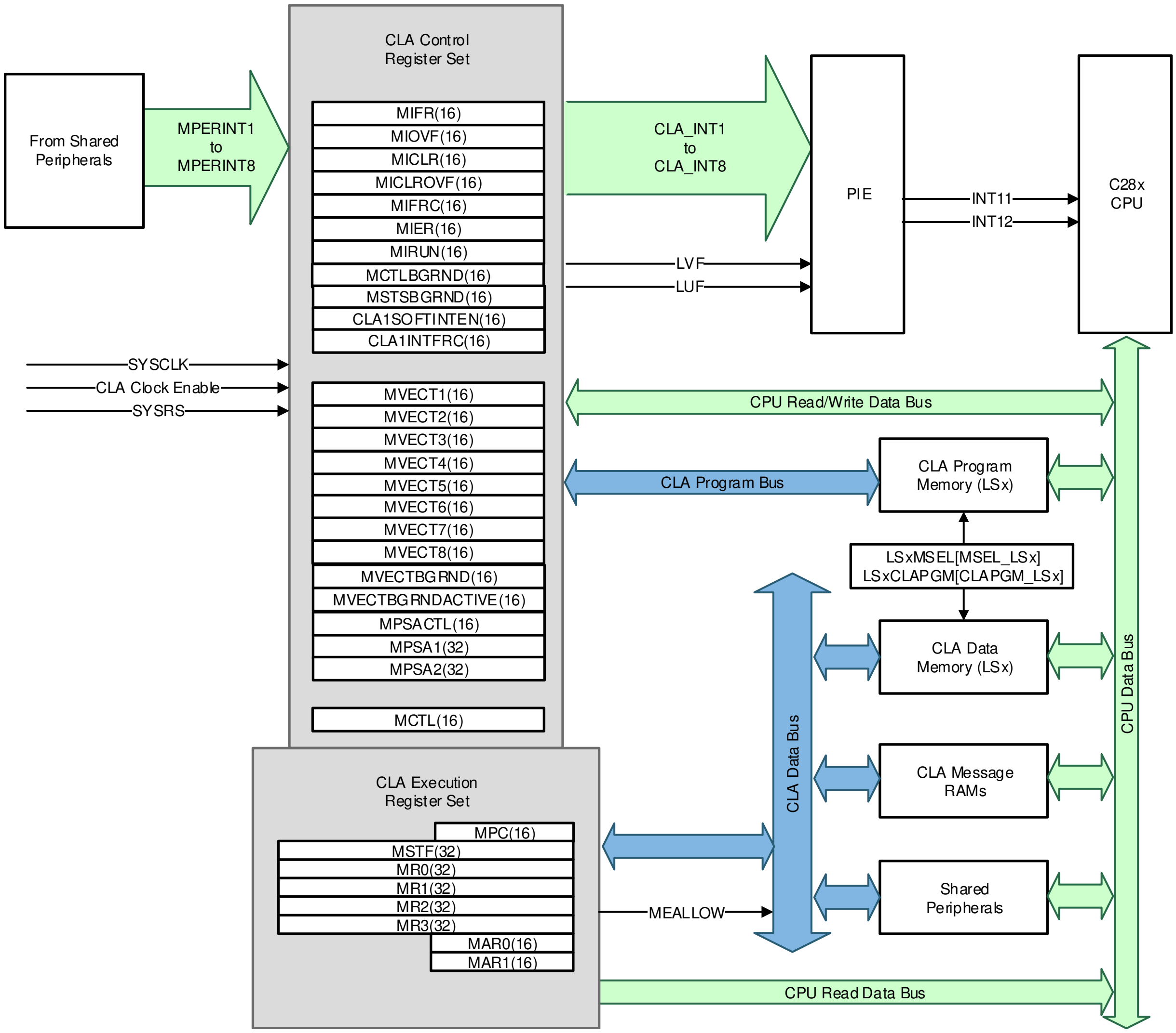

Figure 7-4. CLA Block Diagram

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7.9.3 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the System Event Counter units. The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software, which significantly increases the debug capabilities of many real-time systems, especially in situations where debuggers are not connected. In the TMS320F28P65x devices, the ERAD module contains eight Enhanced Bus Comparator units (which increases the number of Hardware breakpoints from two to ten) and four Benchmark System Event Counter units.

7.9.4 Background CRC-32 (BGCRC)

The Background CRC (BGCRC) module computes a CRC-32 on a configurable block of memory. It accomplishes this by fetching the specified block of memory during idle cycles (when the CPU, CLA or DMA is not accessing the memory block). The calculated CRC-32 value is compared against a golden CRC-32 value to indicate a pass or fail. In essence, the BGCRC helps identify memory faults and corruption.

The BGCRC module has the following features:

- One cycle CRC-32 computation on 32 bits of data
- No CPU bandwidth impact for zero wait state memory
- Minimal CPU bandwidth impact for non-zero wait state memory
- Dual operation modes (CRC-32 mode and scrub mode)
- Watchdog timer to time CRC-32 completion
- Ability to pause and resume CRC-32 computation

7.9.5 Direct Memory Access (DMA)

The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing. Figure 7-5 shows a device-level block diagram of the DMA.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - External Interrupts
  - ePWM SOC signals
  - CPU timers
  - eCAP
  - SPI transmit and receive
  - CAN transmit and receive
  - LIN transmit and receive
- Data sources and destinations:
  - GSx RAM
  - ADC result registers
  - Control peripheral registers (ePWM, eQEP, eCAP)
  - SPI, LIN, CAN, and PMBus registers
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: Four cycles per word without arbitration

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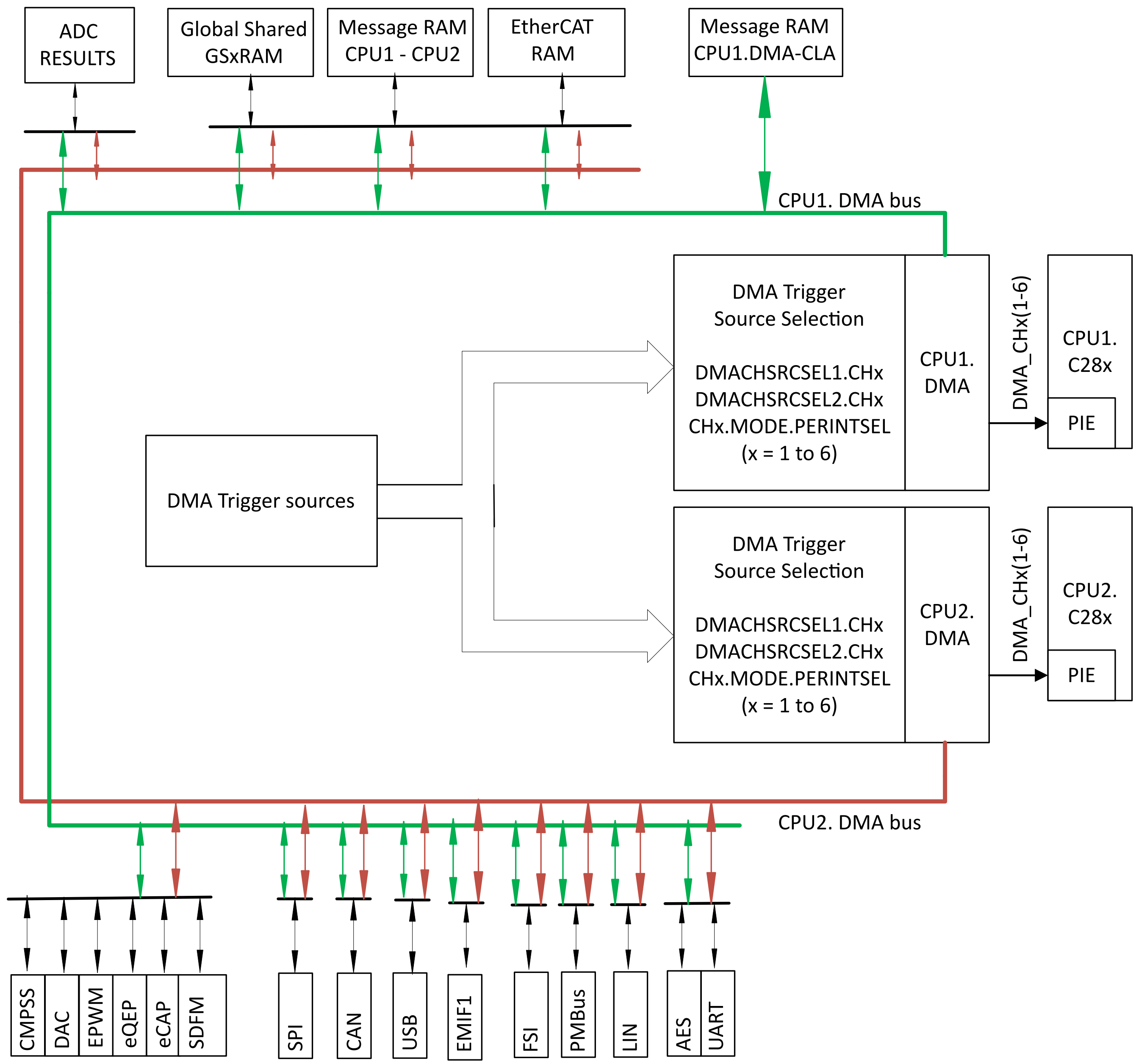

Figure 7-5. DMA Block Diagram

7.9.6 Interprocessor Communication (IPC) Module

The Interprocessor Communication (IPC) module allows communications between the CPU subsystems.

IPC features include:

- Message RAMs
- IPC flags and interrupts
- IPC command registers
- Flash pump semaphore
- Clock configuration semaphore
- Free-running counter

All IPC features are independent of each other, and most do not require any specific data format. There are also two registers for boot mode and status communication. For more information on these registers, see the ROM Code and Peripheral Booting chapter of the *TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual*.

The device has two C28x cores (CPU1, CPU2) and an IPC module:

- CPU1_TO_CPU2 IPC architecture (see Figure 7-6)

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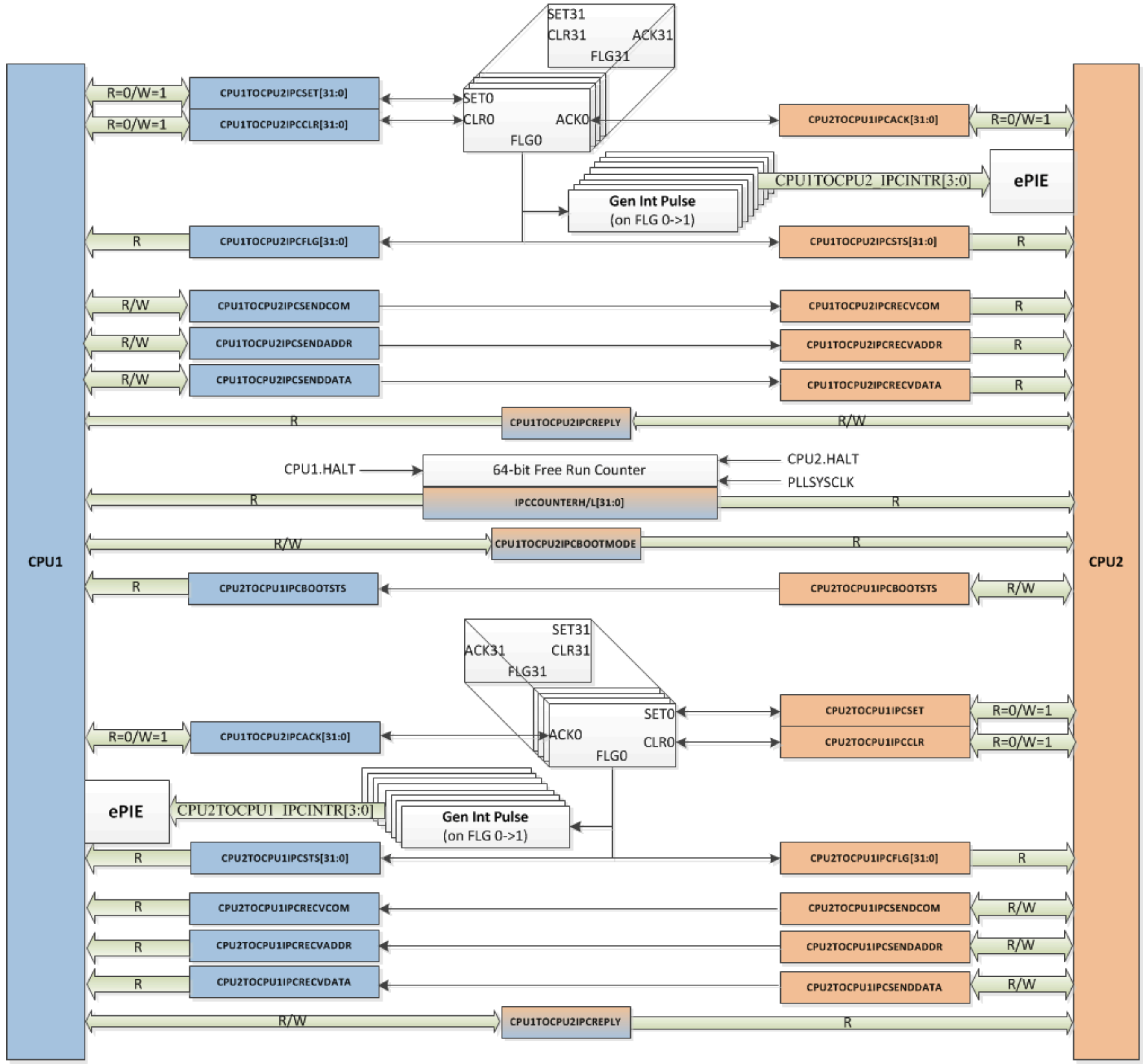

Figure 7-6. CPU1_TO_CPU2 IPC Module

7.9.7 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)

7.9.8 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.9.8.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.9.8.2 Mapping of DCCx Clock Source Inputs

Table 7-25. DCCx Clock Source0 Table

DCCxCLKSRC0[3:0]	CLOCK NAME
0x0	XTAL/X1
0x1	INTOSC1
0x2	INTOSC2
0x4	TCK
0x5	CPU1.SYSCLK
0x8	AUXCLKIN
0xC	INPUT XBAR (Output16 of input-xbar)
others	Reserved

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Table 7-26. DCCx Clock Source1 Table

DCCxCLKSRC1[4:0]	CLOCK NAME
0x0	PLLRAWCLK
0x2	INTOSC1
0x3	INTOSC2
0x6	CPU1.SYSCLK
0x9	Input XBAR (Output15 of the input-xbar)
0xA	AUXCLKIN
0xB	EPWMCLK
0xC	LSPCLK
0xD	ADCCLK
0xE	WDCLK
0xF	CAN0BITCLK
others	Reserved

7.9.9 Nonmaskable Interrupt With Watchdog Timer (NMIWD)

The NMIWD module is used to handle system-level errors. There is an NMIWD module for each CPU. The conditions monitored are:

- Missing system clock due to oscillator failure
- Uncorrectable ECC error on CPU access to flash memory
- Uncorrectable ECC or parity error on CPU, CLA, or DMA access to RAM
- Parity error on CPU access to ROM
- Vector fetch error on the other CPU
- CRC Fail error from BGCRC module
- Reset request from EtherCAT MainDevice or uncorrectable error on access to EtherCAT RAM
- CPU1/CPU2 HWBIST error
- NMI from ERAD module
- CPU1 only: Watchdog or NMI watchdog reset on CPU2

If the CPU does not respond to the latched error condition, then the NMI watchdog will trigger a reset after a programmable time interval. The default time is 65536 SYSCLK cycles.

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7.9.10 Watchdog

The watchdog module is the same as the one on previous TMS320C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-7 shows the various functional blocks within the watchdog module.

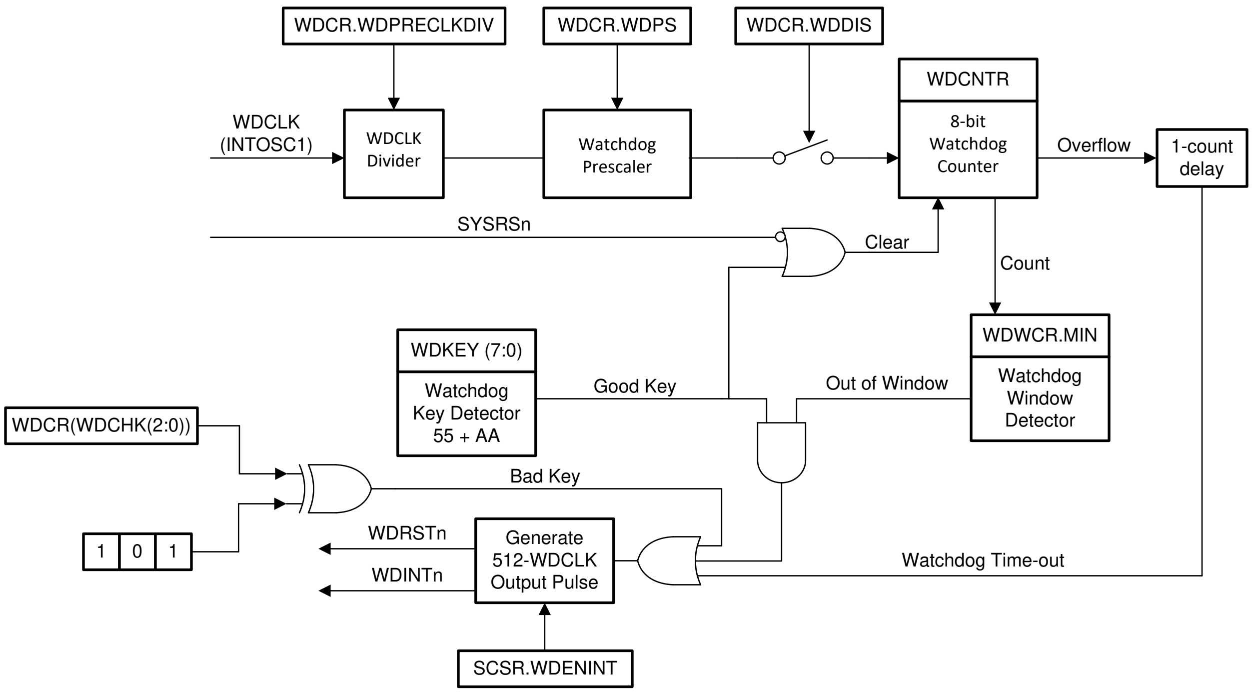

Figure 7-7. Windowed Watchdog

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7.9.11 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports and users guide, please refer to the following location in your C2000Ware for C2000 MCUs package (C2000Ware_2_00_00_03 and higher):

- **C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc**
- *CLB Tool User's Guide*
- *Designing With the C2000™ Configurable Logic Block (CLB) Application Report*
- *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers Application Report*

The CLB module and its interconnections are shown in Figure 7-8.

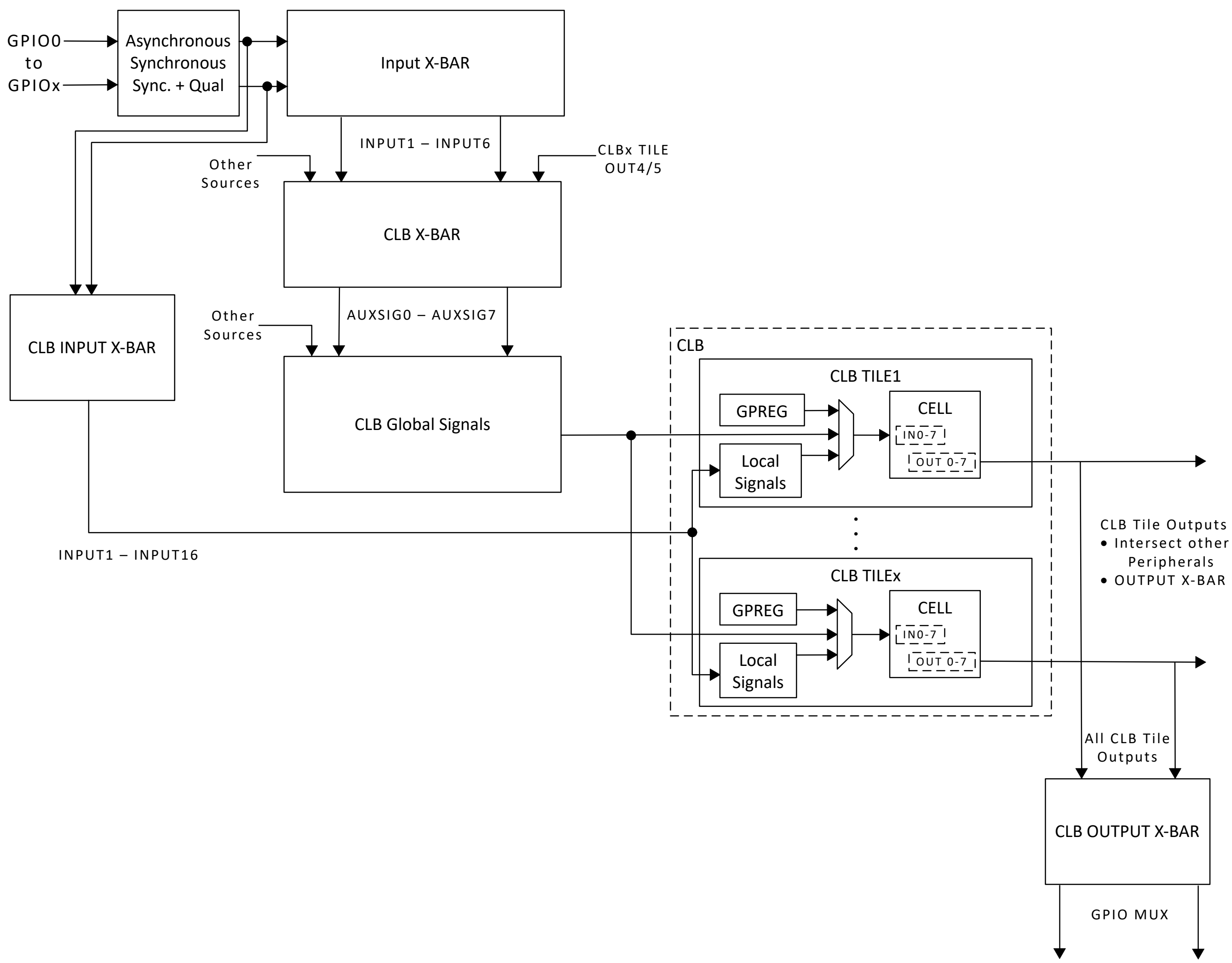

Figure 7-8. GPIO to CLB Tile Connections

Absolute encoder protocol interfaces are now provided as Position Manager solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with C2000Ware MotorControl SDK. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality.

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8 Applications, Implementation, and Layout

8.1 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Key Device Features

Table 8-1. Key Device Features

MODULE	FEATURE	SYSTEM BENEFIT
C28x PROCESSING		
Real-time control CPUs	Up to 600 MIPS Two C28x cores: 400 MIPS (2 x 200 MIPS) One CLA cores: 200 MIPS Flash: Up to 1.28 MB (Shared between C28x CPUs) RAM : Up to 248 KB 64-bit Floating Point Unit (FPU64) Trigonometric Math Unit (TMU) CRC engine and instructions (VCRC) Fast Integer Division (FINTDIV)	TI's two 32-bit C28x DSP cores, provides 400 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM Provides 400 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. **CLA:** Allows user to execute time-critical control loops concurrently with main CPU **FPU64:** Native hardware support for IEEE-754 double-precision floating-point operations **TMU:** Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. Helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms **VCRC:** Provides a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. **FINTDIV:** Supports linear division operations such as Euclidean and Modulus division used in control algorithms See Real-time Benchmarks Showcasing C2000™ControlMCU's Optimized Signal Chain.
SENSING		
Analog-to-Digital Converter (ADC) (configurable 12-bit or 16-bit)	Three ADC modules 16-bit mode: (1.1 MSPS) Single-ended mode: Up to 40 channels Differential mode : Up to 19 channels 12-bit mode: (3.8 MSPS) Single-ended mode: Up to 40 channels Differential mode : Up to 19 channels	ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles. More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance.

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Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Comparator Subsystem (CMPSS)	**CMPSS** 11 windowed comparators with 12-bit Digital to Analog Converters (DAC) Two 12-bit buffered DAC outputs 60-ns detection to trip time DAC ramp generation Low DAC output on external pin Digital filters Slope compensation	**System protection without false alarms:** Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring. PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems. Provides better control accuracy. No need for further CPU configuration to control the PWM with the comparator and 12-bit DAC (CMPSS). Enables protection and control using the same pin.
Sigma Delta Filter Module (SDFM)	Up to 16 independently configurable digital comparator filter channels Up to 16 independently configurable digital data filter channels	Enables galvanic isolation with reinforced delta sigma modulators. SDFMs interface with external delta sigma modulator ADCs, which is ideal for signals that may require isolation. Comparator filter supports overcurrent and undercurrent protection but tripping the PWM without CPU intervention Digital data filter provides higher ENOBs for better control-loop performance
Enhanced Quadrature Encoder Pulse (eQEP)	6 eQEP modules	Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Also can be used in other applications to count input pulses from an external device (such as a sensor).
Enhanced Capture (eCAP)	6 eCAP modules Measures elapsed time between events (up to 4 time-stamped events). Connects to any GPIO through the input X-BAR. When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).	**Applications for eCAP include:** Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors) Elapsed time measurements between position sensor pulses Period and duty-cycle measurements of pulse train signals Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors

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Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
ACTUATION		
Enhanced Pulse Width Modulation (ePWM)/High-Resolution Pulse Width Modulation (HRPWM)	Up to 36 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window	Flexible PWM waveform generation with best power topology coverage. Shadowed Dead band itself and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency.
	HRPWM capability: All 36 channels provide high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, deadband, and phase offsets for 99% greater precision	Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output.
	One-shot and global reload feature	Critical for variable-frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). Enables control of interleaved LLC topologies at high frequencies
	Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) trip event	Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control.
	Load on SYNC (support for shadow-to-active load on a SYNC event)	Enables variable-frequency applications (allows LLC control in power conversion).
	Ability to shut down the PWMs without software intervention (no ISR latency)	Fast protection under fault condition
	Delayed Trip Functionality	Helps implement the deadband with Peak Current Mode Control (PCMC) Phase-Shifted Full Bride (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events).
	Dead band Generator (DB) submodule	Prevents simultaneous ON conditions of High- and Low-side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges.
	Flexible PWM Phase Relationships and Timer Synchronization	Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges perfectly in synchronization with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching.
	Diode Emulation	Diode Emulation logic provides hardware features and the necessary hooks into other IPs to implement robust diode mode sense and control in a noisy environment
CONNECTIVITY		
Serial Peripheral Interface (SPI)	4 high-speed SPI port	Supports 50 MHz
Serial Communication Interface (SCI)	2 SCI (UART) modules	Interfaces with controllers
Controller Area Network (CAN/DCAN)	1 DCAN module	Provides compatibility with classic CAN modules

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Controller Area Network (FD/ MCAN)	2 MCAN modules	MCAN supports both classic CAN and CAN FD protocols
Inter-Integrated Circuit (I2C)	2 I2C modules	Interfaces with external EEPROMs, sensors, or controllers
External Memory Interfaces (EMIFs) with ASRAM and SDRAM support	One EMIF module	Interface with External ASRAM and SDRAM
OTHER SYSTEM FEATURES		
Configurable Logic Block (CLB)	Collection of configurable blocks that can be inter-connected using software to implement custom digital logic functions	User customized PWM protection features, custom logic to off-load complex algorithms/state machines, custom peripherals, and used to implement absolute encoders used in servo drives User also used for protection of multilevel inverter/PFC or multilevel DC-DC Provides the ability to build logic around existing IPs like ETPWM, ECAP, QEP and GPIOs. Enables development of unique IP such as PWM Safety modules, Encoder engines, etc.
Security enhancers	Dual-zone Code Security Module (DCSM) Secure Boot JTAGLOCK BackGround CRC (BGCRC) Generic CRC (GCRC) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity	**DCSM:** Prevents duplication and reverse-engineering of proprietary code **Secure Boot:** Uses AES128 CMAC algorithm to ensure code that runs on the device is authentic **JTAGLOCK:** Ability to block emulation of the device **AES acceleration:** The hardware accelerator vastly improves the cycle time of processing cryptographic messages while freeing up the CPU bandwidth **BGCRC:** Checks memory integrity with no CPU overhead or system performance impact **GCRC:** Designated Connectivity Manager module for computing the CRC value on a configurable block of memory **Watchdog:** Generates reset if CPU gets stuck in endless loops of execution **Write Protection on Registers:** LOCK protection on system configuration registers Protection against spurious CPU writes **MCD:** Automatic clock failure detection **ECC and parity:** Single-bit error correction and double-bit error detection
Crossbars (XBARs)	Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. • Input X-BAR • Output X-BAR • ePWM X-BAR • CLB Input X-BAR • CLB Output X-BAR • CLB X-BAR	**Enhances hardware design versatility:** **Input X-BAR:** Routes signals from any GPIO to multiple IP blocks within the chip **Output XBAR:** Routes internal signals onto designated GPIO pins **ePWM X-BAR:** Routes internal signals from various IP blocks to ePWM **CLB Input X-BAR:** Allows user to route signals directly from any GPIO to Configurable Logic Block (CLB) **CLB Output X-BAR:** Allows user to bring signals from CLB tiles to designated GPIO pins **CLB X-BAR:** Allows user to bring signals from various IP blocks to CLB

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Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Direct Memory Access (DMA) controller	Two 6-channel Direct Memory Access (DMA) controllers	The direct memory access (DMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up CPU bandwidth for other system functions.
USB		Useful for system datalogging and boot to USB for updating on-chip flash

8.3 Application Information

8.3.1 Typical Application

The *Typical Applications* section details *some* applications of this device. For a more extensive list of applications, see the *Applications* section of this data sheet.

8.3.1.1 Servo Drive Control Module

Servo drives require high precision current and voltage sensing for accurate torque control and often supports interfaces for multiple encoder types along with communication interfaces. This C2000 device can be used either as single chip solution for standalone servo drive (shown in Figure 8-1) or can be used in decentralized systems (shown in Figure 8-2). In the later case, the F28P65x C2000 device functions as the controller which samples all the voltage and current inputs and generates the correct PWM signals for inverter. Each C2000 device serves as real-time controller for a target axis, running motor current control loop. Using the Fast Serial Interface (FSI) peripheral, up to 16 axes can be managed with one C2000 device. As an outer loop controller, the C2000 device executes main axis motor control, controls data exchange with all secondary axis over FSI and communicates with a host or PLC through EtherCAT.

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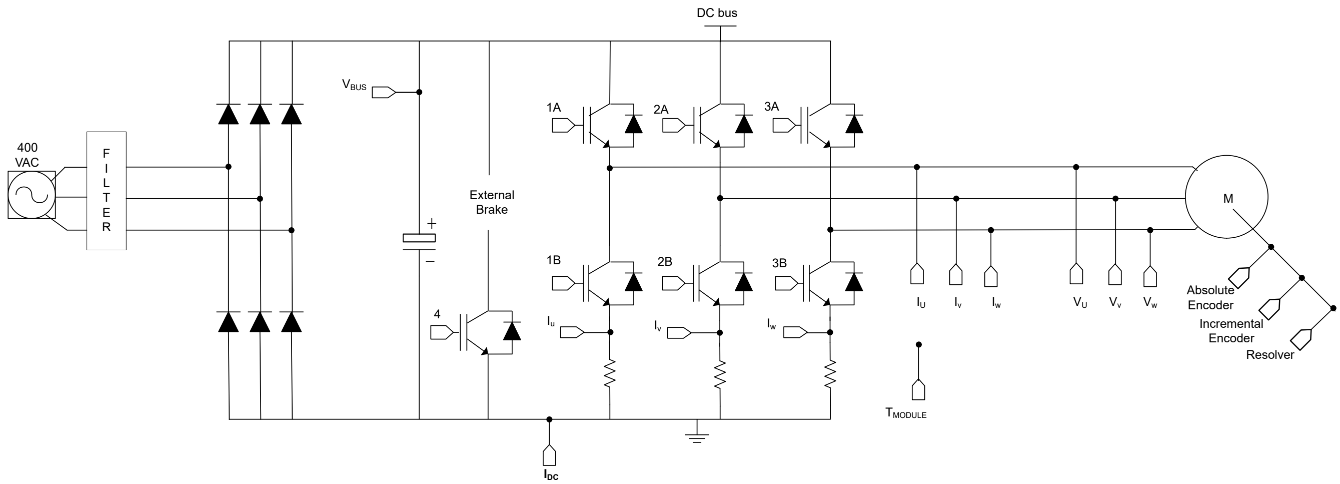
8.3.1.1.1 System Block Diagram



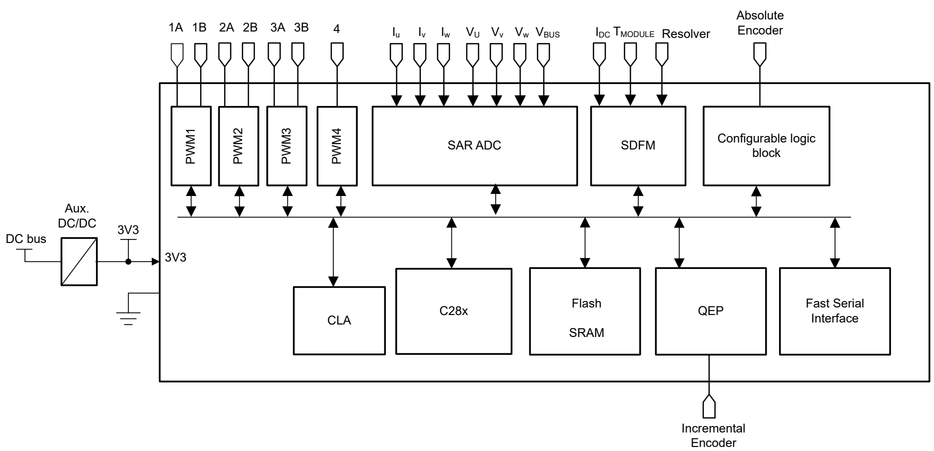


Figure 8-1. Servo Drive Control Module

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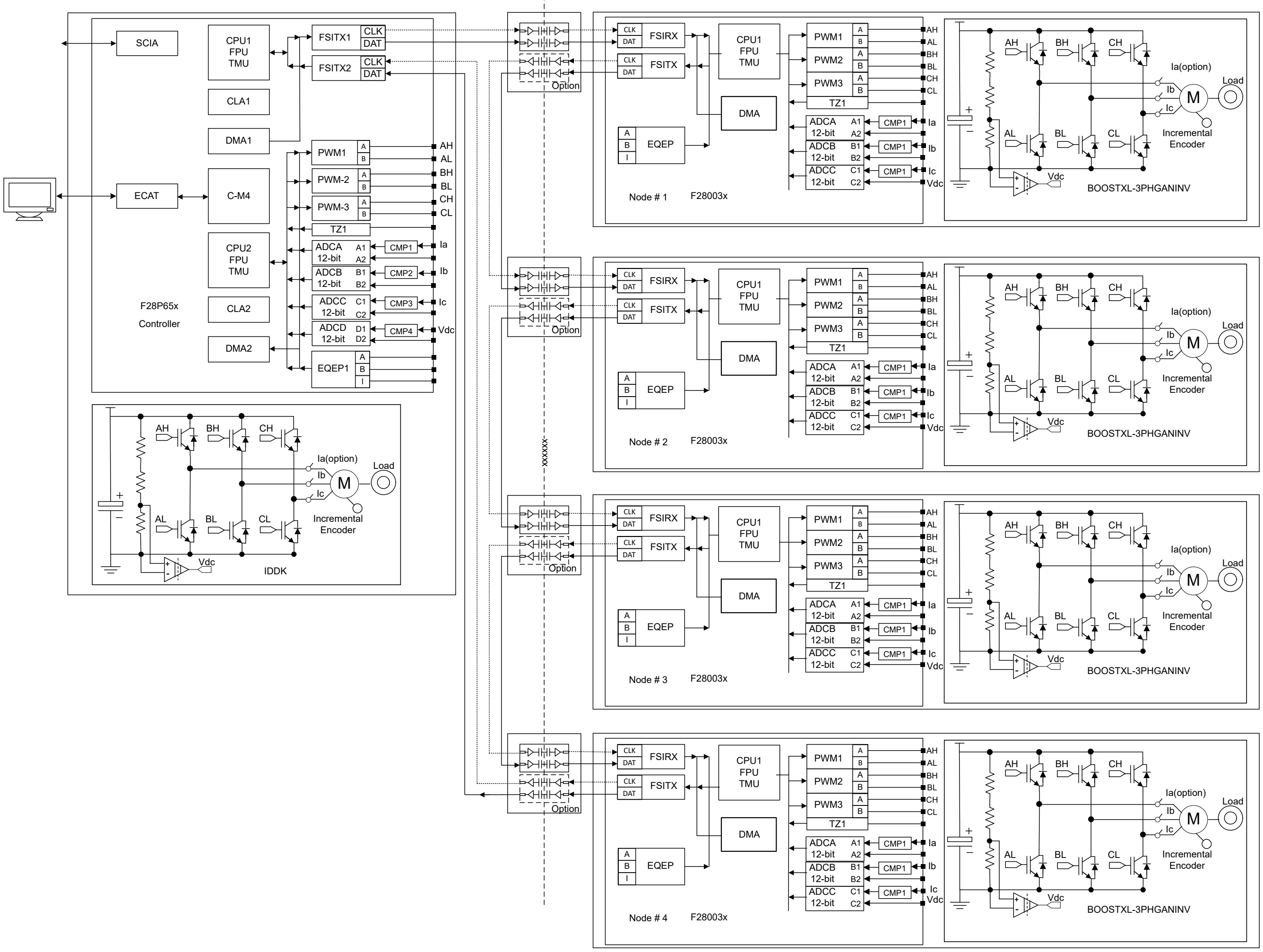

Figure 8-2. Distributed Multi-Axis Servo Drive

8.3.1.1.2 Servo Drive Control Module Resources

Reference Designs and Associated Training Videos

48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Evaluation Module

The BOOSTXL-3PHGANINV evaluation module features a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives.

C2000 DesignDRIVE Development Kit for Industrial Motor Control

The DesignDRIVE Development Kit (IDDK) hardware offers an integrated servo drive design with full power stage to drive a high voltage three-phase motor and eases the evaluation of a range of position feedback, current sensing and control topologies.

C2000 DesignDRIVE position manager BoosterPack™ plug-in module

The PositionManager BoosterPack is a flexible low voltage platform intended for evaluating interfaces to absolute encoders and analog sensors like resolvers and SinCos transducers. When combined with the DesignDRIVE Position Manager software solutions this low-cost evaluation module becomes a powerful tool for interfacing many popular position encoder types such as EnDat, BiSS and T-format with C2000 Real-Time Control devices. C2000 Position Manager technology integrates interfaces to the most popular digital and analog position sensors onto C2000 Real-Time Controller, thus eliminating the need for external FPGAs for these functions.

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C2000Ware MotorControl SDK
MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs) which are targeted for industrial drives, robotics, appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications.

TIDM-02006 Distributed multi-axis servo drive over fast serial interface (FSI) reference design
This reference design presents an example distributed or decentralized multi-axis servo drive over Fast Serial Interface (FSI) using C2000™ real-time controllers. Multi-axis servo drives are used in many applications such as factory automation and robots. The cost per axis, performance and ease of use are always high concerns for such systems. FSI is a cost-optimized and reliable high speed communication interface with low jitter that can daisy-chain multiple C2000 microcontrollers. In this design, each TMS320F280049 or TMS320F280025 real-time controller serves as a real-time controller for a distributed axis, running motor current control loop. A single TMS320F28388D runs position and speed control loops for all axes. The same F2838x also executes a centralized motor control axis plus EtherCAT communication, leveraging its multiple cores. The design uses our existing EVM kits, the software is released within C2000WARE MotorControl SDK.

TIDM-02007 Dual-axis motor drive using fast current loop (FCL) and SFRA on a single MCU reference design
This reference design presents a dual-axis motor drive using fast current loop (FCL) and software frequency response analyzer (SFRA) technologies on a single C2000 controller. The FCL utilizes dual core (CPU, CLA) parallel processing techniques to achieve a substantial improvement in control bandwidth and phase margin, to reduce the latency between feedback sampling and PWM update, to achieve higher control bandwidth and maximum modulation index, to improve DC bus utilization by the drive and to increase speed range of the motor. The integrated SFRA tool enables developers to quickly measure the frequency response of the application to tune speed and current controllers. Given the system-level integration and performance of C2000 series, MCUs have the ability to support dual-axis motor drive requirements simultaneously that delivers very robust position control with higher performance. The software is released within C2000Ware MotorControl SDK.

EtherCAT Protocol: EtherCAT on C2000™ TMS320F2838x Device Family (Video)
This video covers details on the TMS320F2838x device EtherCAT SubordinateDevice (or SubDevice) controller features, details on the TMS320F2838x device EtherCAT SubDevice controller subsystem and device integration, and comparison of TMS320F2838x device EtherCAT IP versus Beckhoff Automation ET1100 EtherCAT ASIC.

EtherCAT-Based Connected Servo Drive Using Fast Current Loop on PMSM Application Report
This application report helps to evaluate EtherCAT® communication and to perform frequency response analysis of fast current loop (FCL) enabled control loops of a connected servo drive using TI's TMS320F28388D real-time controller.

8.3.1.2 Solar Micro Inverter

A Solar Micro Inverter consists of a DC-AC inverter power stage and one or more Maximum Power Point Tracking (MPPT) DC-DC power stages. Typical switching frequency for the inverter (DC-AC) is between 20kHz-50kHz and for DC-DC side can be in the range 100kHz-200kHz. A variety of power stage topologies can be used to achieve this and the diagram only depicts a typical power stage and the control & communication requirements. A C2000 microcontroller has on-chip EPWM, ADC and analog comparator modules to implement complete digital control of such micro inverter system.

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8.3.1.2.1 System Block Diagram

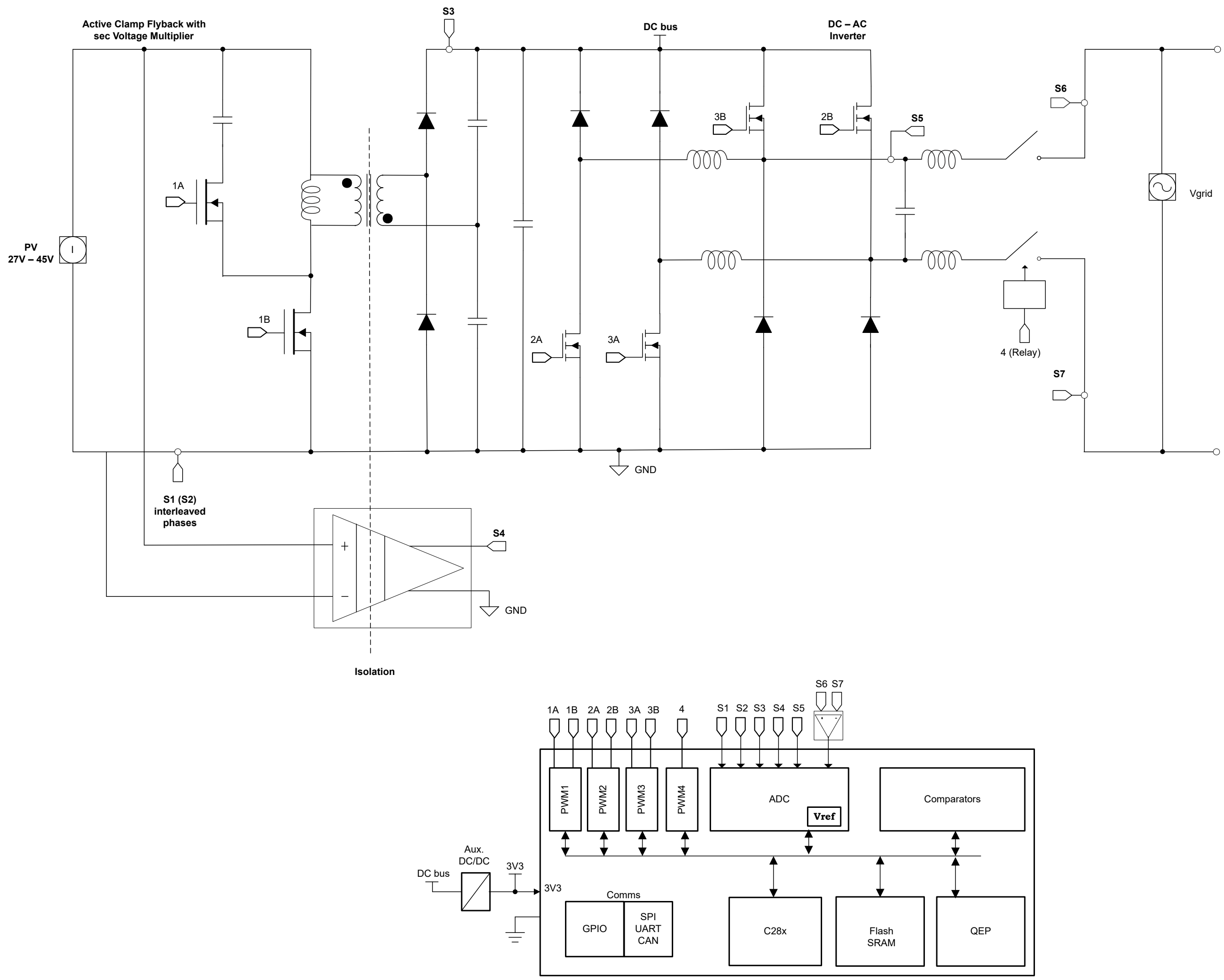

Figure 8-3. Solar Micro Inverter

8.3.1.2.2 Solar Micro Inverter Resources

Reference Designs and Associated Training Videos

C2000™ MCUs - Digital Power (Video)
This training series covers the basics of digital power control and how to implement it on C2000 microcontrollers.

Four Key Design Considerations When Adding Energy Storage to Solar Power Grids
This white paper explores the design considerations in a grid-connected storage-integrated solar installation system

C2000WARE-DIGITALPOWER-SDK
DigitalPower SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs) which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power application

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Digitally Controlled Solar Micro Inverter Design using C2000™ Piccolo Microcontroller
This document presents the implementation details of a digitally-controlled solar micro inverter using the C2000 microcontroller. A 250-W isolated micro inverter design presents all the necessary PV inverter functions using the Piccolo-B (F28035) control card. This document describes the power stages on the micro inverter board, as well as an incremental build level system that builds the software by verifying open loop operation and closed loop operation. This guide describes control structures and algorithms for controlling power flow, maximizing power from the PV panel (MPPT), and locking to the grid using phase locked loop (PLL), along with hardware details of Texas Instruments Solar Micro Inverter Kit (TMDSOLARUINVKIT)

TIDU405B Grid-tied Solar Micro Inverter with MPPT
This C2000 Solar Micro Inverter EVM hardware consists of two stages. These are: (1) an active clamp fly-back DC/DC converter with secondary voltage multiplier and, (2) a DC-AC inverter. A block diagram of this system is shown in Figure 1b. The DC-DC converter draws dc current from the PV panel such that the panel operates at its maximum power transfer point. This requires maintaining the panel output (that is, the DC-DC converter input at a level determined by the MPPT algorithm). The MPPT algorithm determines the panel output current (reference current) for maximum power transfer. Then a current control loop for the fly-back converter ensures that the converter input current tracks the MPPT reference current. The fly-back converter also provides high frequency isolation for the DC-DC stage. The output of the fly-back stage is a high voltage DC bus which drives the DC-AC inverter. The inverter stage maintains the DC bus at a desired set point and injects controlled sine wave current into the grid. The inverter also implements grid synchronization in order to maintain its current waveform locked to phase and frequency of the grid voltage. A C2000 piccolo microcontroller with its on-chip PWM, ADC and analog comparator modules is able to implement complete digital control of such micro inverter system.

Software Phase Locked Loop Design Using C2000™ Microcontrollers for Single Phase Grid Connected Inverter Application Report
Grid connected applications require an accurate estimate of the grid angle to feed power synchronously to the grid. This is achieved using a software phase locked loop (PLL). This application report discusses different challenges in the design of software phase locked loops and presents a methodology to design phase locked loops using C2000 controllers for single phase grid connection applications.

8.3.1.3 EV Charging Station Power Module

The power module in a DC charging station consists of AC/DC power stage and DC/DC power stage. Each converter associated with its power stage comprises of power switches and gate driver, current and voltage sensing, and a real-time micro-controller. On the input side it has three-phase AC mains which are connected to the AC/DC power stage. This block converts the incoming AC voltage into a fixed DC voltage of around 800 V. This voltage serves as input to the DC/DC power stage which processes power and interfaces directly with the battery on the electric vehicle. Each power stage has a separate real-time micro-controller which is responsible for the processing of analog signals and providing fast control action.

The AC/DC stage (also known as the PFC stage) is the first level of power conversion in an EV charging station. It converts the incoming AC power from the grid (380–415 VAC) into a stable DC link voltage of around 800 V. The PFC stage maintains sinusoidal input currents, with typically a THD < 5%, and provides controlled DC output voltage higher than the amplitude of the line-to-line input voltage. The DC/DC stage is the second level of power conversion in an EV charging station. It converts the incoming DC link voltage of 800 V (in case of three-phase systems) to a lower DC voltage to charge the battery of an electric vehicle. The DC/DC converter must be capable of delivering rated power to the battery over a wide range with the capability of charging the battery at constant current or at constant voltage modes, depending on the State Of Charge (SOC) of the battery.

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8.3.1.3.1 System Block Diagram

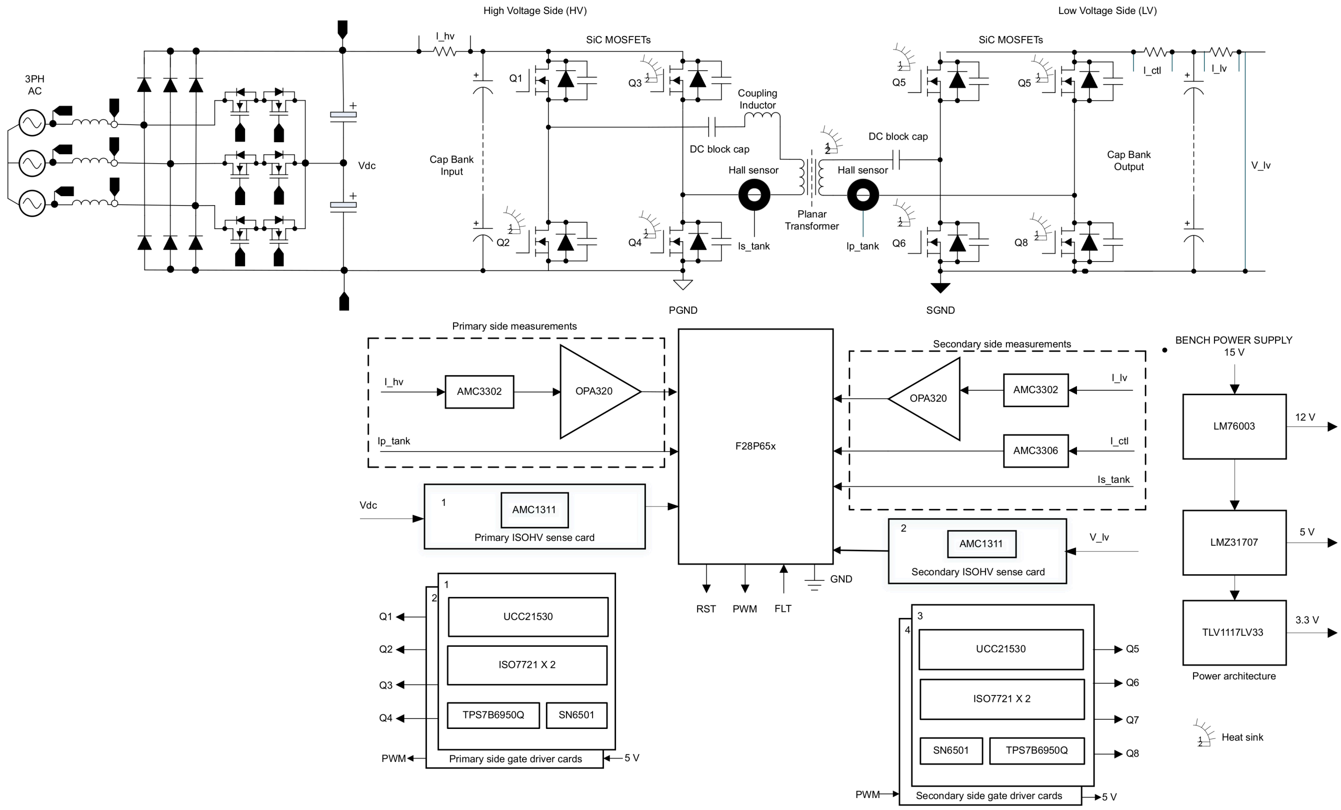

Figure 8-4. Dual-active-bridge DC/DC converter

8.3.1.3.2 EV Charging Station Power Module Resources

Reference Designs and Associated Training Videos

TIDM-02002 CLLLC resonant dual active bridge for HEV/EV onboard charger (Video)
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDA-01606 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC reference design
This reference design provides an overview on how to implement a bidirectional three-level, three-phase, SiC-based active front end (AFE) inverter and PFC stage. The design uses a switching frequency of 50 kHz and a LCL output filter to reduce the size of the magnetics. A peak efficiency of 99% is achieved. The design shows how to implement a complete three phase AFE control in the DQ domain. The control and software is validated on the actual hardware and on hardware in the loop (HIL) setup.

TIDA-010210 11-kW, bidirectional, three-phase ANPC based on GaN reference design
This reference design provides a design template for implementing a three-level, three-phase, gallium nitride (GaN) based ANPC inverter power stage. The use of fast switching power devices makes it possible to switch at a higher frequency of 100 kHz, reducing the size of magnetics for the filter and increasing the power density of the power stage. The multilevel topology allows the use of 600-V rated power devices at higher DC bus voltages of up to 1000 V. The lower switching voltage stress reduces switching losses, resulting in a peak efficiency of 98.5%

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TIDA-010054 Bi-directional, dual active bridge reference design for level 3 electric vehicle charging stations
This reference design provides an overview on the implementation of a single-phase Dual Active Bridge (DAB) DC/DC converter. DAB topology offers advantages like soft-switching commutations, a decreased number of devices and high efficiency. The design is beneficial where power density, cost, weight, galvanic isolation, high-voltage conversion ratio, and reliability are critical factors, making it ideal for EV charging stations and energy storage applications. Modularity and symmetrical structure in the DAB allow for stacking converters to achieve high power throughput and facilitate a bidirectional mode of operation to support battery charging and discharging applications.

C2000™ MCUs - Electric vehicle (EV) training videos (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

Maximizing power for Level 3 EV charging stations
This explains how C2000's rich portfolio provide optimal solutions that help engineers solve design challenges and implement advanced power topologies.

Power Topology Considerations for Electric Vehicle Charging Stations Application Report
This Application Report discusses the topology consideration for designing power modules that acts as a building block for design of these fast DC Charging Station.

TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDM-1000 Vienna Rectifier-Based Three Phase Power Factor Correction Reference Design Using C2000 MCU
The Vienna rectifier power topology is used in high-power, three-phase power factor correction applications such as off-board electric vehicle charging and telecom rectifiers. This design illustrates how to control a Vienna rectifier using a C2000 MCU.

8.3.1.4 On-Board Charger (OBC)

An On-Board Charger (OBC) consists of two power stages: an AC-DC power converter and a subsequent DC-DC power converter stage. The OBC can be implemented by using a single MCU to control both the AC-DC and DC-DC power converters. For example: an 11-kW OBC can be implemented by using three 3.7-kW single-phase OBC modules, as shown in Figure 8-5. This approach allows us to easily support both single-phase 240 AC (North America) and 3-phase AC (rest of the world).

OBC-charging design requirements are as follows:

- High-performance and fast digital control loops enabling highly efficient power conversion and increased power density.
- Enabling precise control and fast shutdown in an overcurrent scenario by high bandwidth and fast response current sensing.
- Safely and efficiently controlling and protecting the power switch [insulated-gate bipolar transistor/silicon carbide (IGBT/SiC)].

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8.3.1.4.1 System Block Diagram

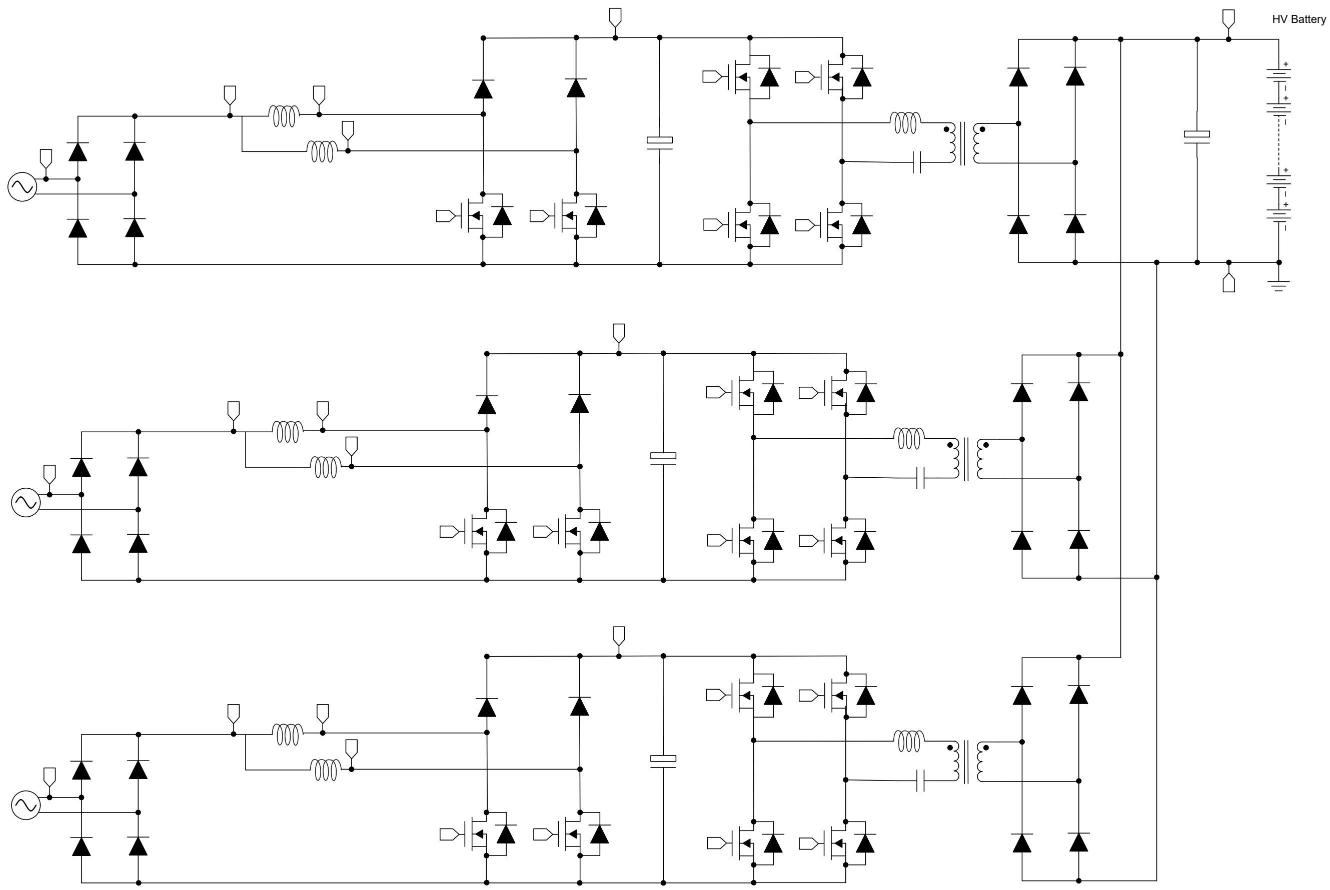

Figure 8-5. 11 kW Modular OBC Power Topology (Unidirectional, bridge PFC)

8.3.1.4.2 OBC Resources

Reference Designs and Associated Training Videos

C2000 Digital Power Training videos
This power topology is capable of bidirectional power flow (PFC and grid-tied inverter) and uses GaN devices, which enables higher efficiency and reduction in size of the power supply. The hardware and software available with this reference design accelerates time to market.

C2000™ MCUs - Electric vehicle (EV) training videos (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

PMP22650 GaN-based, 6.6-kW, bidirectional, onboard charger reference design
The PMP22650 reference design is a 6.6-kW, bidirectional, onboard charger. The design employs a two-phase totem pole PFC and a full-bridge CLLLC converter with synchronous rectification. The CLLLC utilizes both frequency and phase modulation to regulate the output across the required regulation range. The design uses a single processing core inside a TMS320F28388D microcontroller to control both the PFC and CLLLC. Synchronous rectification is implemented via the same microcontroller with Rogowski coil current sensors. High density is achieved through the use of high-speed GaN switches (LMG3522). The PFC is operating at 120 kHz and the CLLLC runs with a variable frequency from 200 kHz to 800 kHz. A peak system efficiency of 96.5% was achieved with an open-frame power density of 3.8 kW/L. While the design calculations were done for a 6.6-kW output power, the design represents a suitable starting point for a 7.x-kW (for example, 7.2-kW to 7.4-kW) rated OBC operating from a 240-V input with a 32-A breaker.

TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDM-02013: 7.4-kW on-board charger reference design with CCM totem pole PFC and CLLLC DC/DC reference design
TIDM-02013 is a bidirectional onboard charger reference design. The design consists of an interleaved continuous conduction mode (CCM) totem-pole (TTPL) bridgeless power-factor correction (PFC) power stage followed by a CLLLC DCDC power stage all controlled using a single C2000™ real-time control microcontroller (MCU), while utilizing a TI gallium nitride (GaN) power module.

TIDUEG3A TIDM-1022 Valley switching boost power factor correction (PFC) reference design
This reference design illustrates a digital control method to significantly improve Boost Power Factor Correction (PFC) converter performance such as the efficiency and Total Harmonic Distortion (THD) under light load condition where efficiency and THD standards are difficult to meet. This is achieved using the integrated digital control feature of the C2000™ microcontroller (MCU). The design supports phase-shedding, valley-switching, valley-skipping, and Zero Voltage Switching (ZVS) for different load and instantaneous input voltage conditions. The software available with this reference design accelerates time to market.

8.3.1.5 High-Voltage Traction Inverter

The traction drive subsystem is designed to drive an AC induction motor or some combination of interior permanent magnet synchronous motor (IPMSM) and synchronous reluctance motor (SynRM). A high-bandwidth, field-oriented control (FOC) scheme with dynamic decoupling is implemented with a C2000 real-time control MCU together with field-weakening and over-modulation techniques to driver motor to industry-leading high speed up to 20,000 RPM, which can enable cost and weight reduction to the traction motor.

A traction drive system normally uses a variable reluctance (VR) resolver, which matches the pole count of the motor, to directly measure the electric angle of the rotor. Resolver-to-digital conversion (RDC) is required to measure position and speed using the resolver signal. RDC is traditionally handled by a separate IC, such as PGA411-Q1. With a C2000 MCU, RDC for a high-speed traction inverter can be integrated into the main control MCU, where the excitation generation can be handled with the DMA without CPU involvement, and feedback is read through the ADC and decoded with the CPU.

A Phase-Shifted Full Bride (PSFB) topology allows the switching devices to switch with zero-voltage switching (ZVS), resulting in lower switching losses and higher efficiency. Peak Current Mode Control (PCMC) is a highly desired control scheme for power converters because of its inherent voltage feed forward, automatic cycle-by-cycle current limiting, flux balancing, and other advantages, which require generating complex PWM drive waveforms along with fast and efficient control loop calculations. This is made possible on C2000 microcontrollers by advanced on-chip control peripherals like PWM modules, analog comparators with DAC and slope compensation hardware, and 12-bit high-speed ADCs coupled with an efficient 32-bit CPU.

Figure 8-6 shows a high-level block diagram of a single C2000™ real-time MCU controlling both an HEV/EV traction inverter and a bidirectional DC-DC converter.

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8.3.1.5.1 System Block Diagram

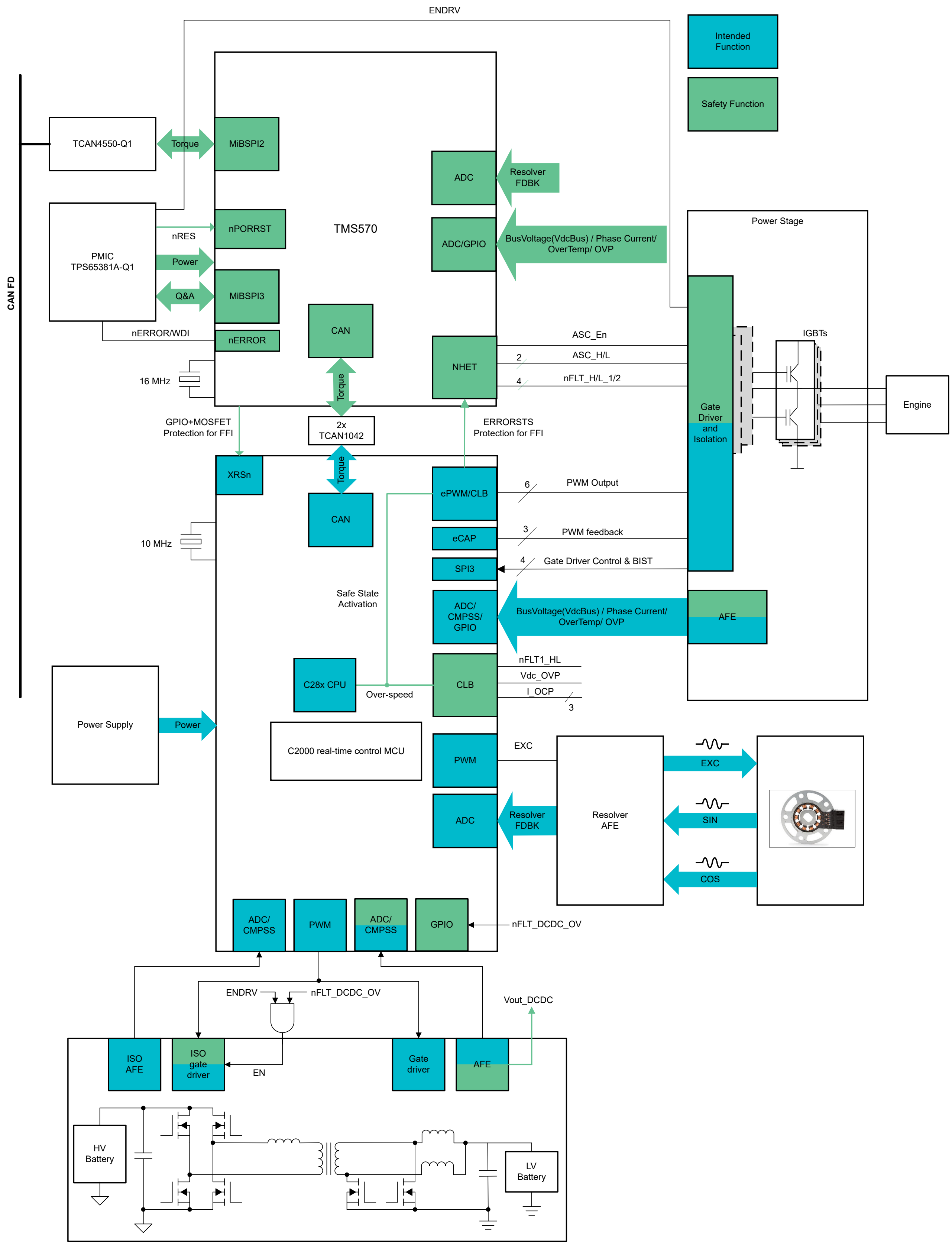

Figure 8-6. Traction Inverter High Voltage

8.3.1.5.2 High-Voltage Traction Inverter Resources

Reference Designs and Associated Training Videos

TIDM-02009 ASIL D Safety Concept-Assessed High-Speed Traction, Bi-directional DC/DC Conversion Reference Design
This reference design demonstrates control of HEV/EV traction inverter and bi-directional DC-DC converter by a single TMS320F28388D real-time C2000™ MCU. The traction control uses a software-based resolver to digital converter (RDC) driving the motor to a high speed up to 20,000 RPM. The DC-DC converter uses peak current mode control (PCMC) technique with phase-shifted full-bridge (PSFB) topology and synchronous rectification (SR) scheme. The traction inverter stage uses silicon carbide (SiC) power stage, driven by UCC5870-Q1 smart gate driver. PCMC waveform is generated using state-of-the-art PWM module and built-in slope compensation in the comparator sub-system (CMPSS). An ASIL decomposition based functional safety concept for the system has been assessed with TÜV SÜD to demonstrate system level safety integrity level up to ISO 26262 ASIL D for representative safety goals.

C2000™ MCUs - Electric vehicle (EV) | TI.com Training Series (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

PSFB Control Using C2000 Microcontrollers Application Report
This application report presents the implementation details of a digitally controlled PSFB system implemented on the high voltage phase shifted full bridge (HVPSFB) kit from Texas Instruments. This kit converts a 400 V DC input to a regulated 12 V DC output and is rated for operations up to 600W. Both peak current mode control (PCMC) and voltage mode control (VMC) implementations are described.

TIDA-BIDIR-400-12 *Bidirectional DC-DC Converter*
This document presents the details of this microcontroller-based implementation of an isolated bidirectional DC-DC converter. A phase-shifted full-bridge (PSFB) with synchronous rectification controls power flow from a 400-V bus or battery to the 12-V battery in step-down mode, while a push-pull stage controls the reverse power flow from the low-voltage battery to the high-voltage bus or battery in boost mode. This design is rated for up to 300 W of output power in either mode.

TIDM-02014 High-power, high-performance automotive SiC traction inverter reference design
TIDM-02014 is a 800-V, 300kW SiC-based traction inverter system reference design developed by Texas Instruments and Wolfspeed provides a foundation for design engineers to create high-performance, high-efficiency traction inverter systems and get to market faster. This solution demonstrates how the traction inverter system technology from TI and Wolfspeed improves system efficiency by reducing the overshoot in available voltages with a high-performance isolated gate driver and real-time variable gate drive strength driving the Wolfspeed SiC power module. TI's high-control performance MCUs featuring tightly-integrated, innovative real-time peripherals enable effective traction motor control even at speeds greater than 20,000 RPM. Fast current loop implementation helps minimize motor torque ripple and provides smooth speed-torque profiles. The mechanical and thermal design of the system is provided by Wolfspeed.

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Getting Started and Next Steps

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28P659DK-Q1). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZEJ).

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

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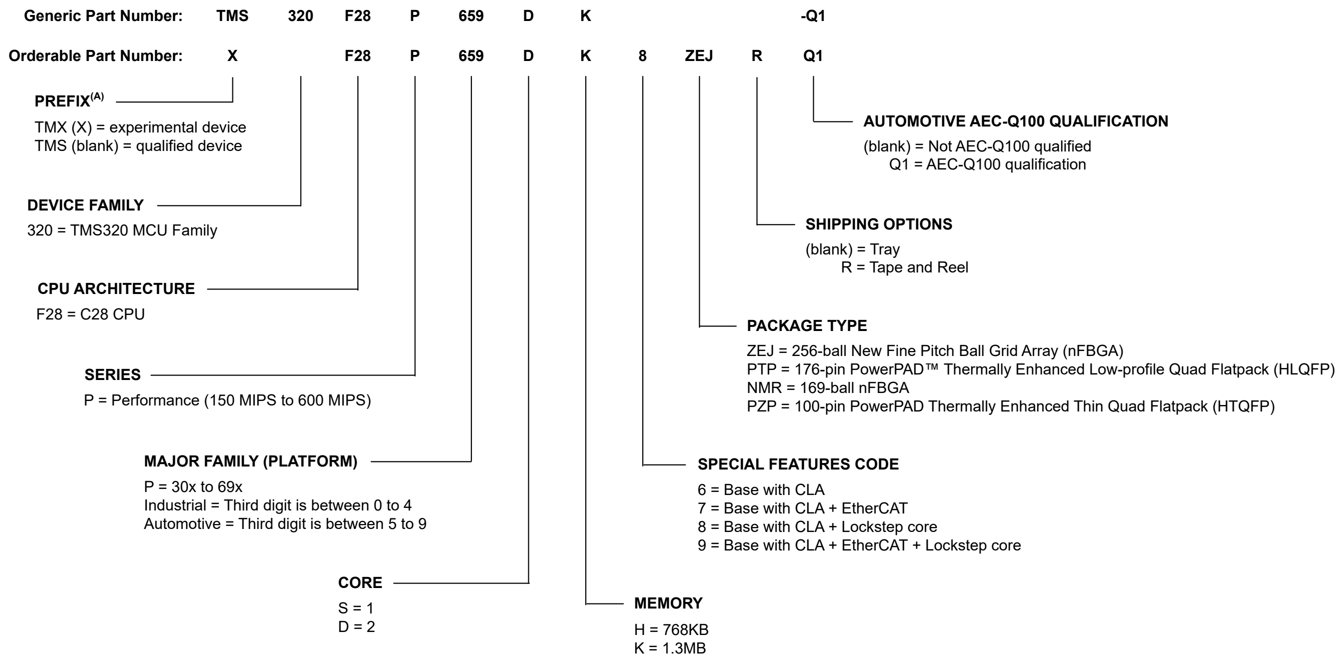

A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.3 Markings

Figure 9-2, Figure 9-3, Figure 9-4, Figure 9-5, Figure 9-6, Figure 9-7, and Figure 9-8 show the package symbolization. Table 9-1 lists the silicon revision codes.

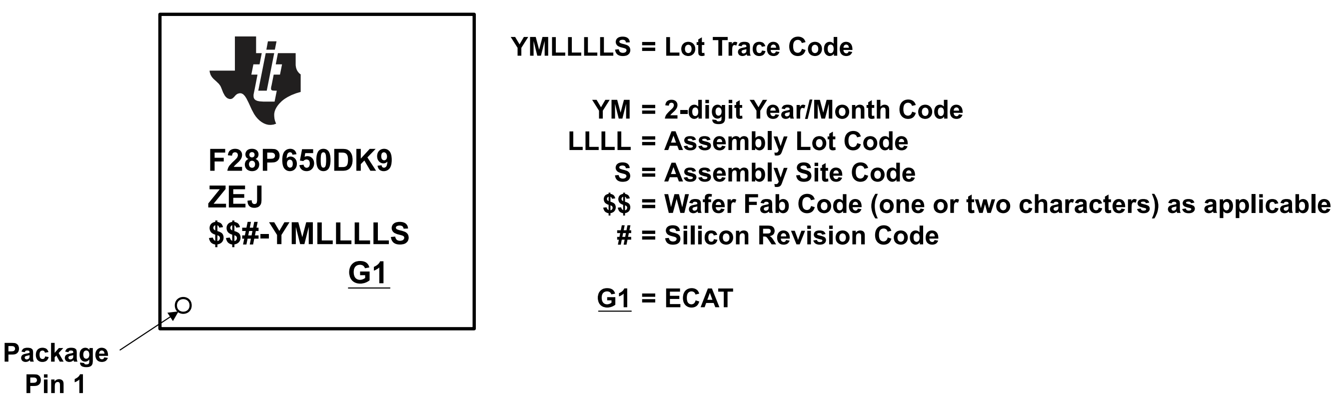

Figure 9-2. Package Symbolization for ZEJ Package – Non-Automotive

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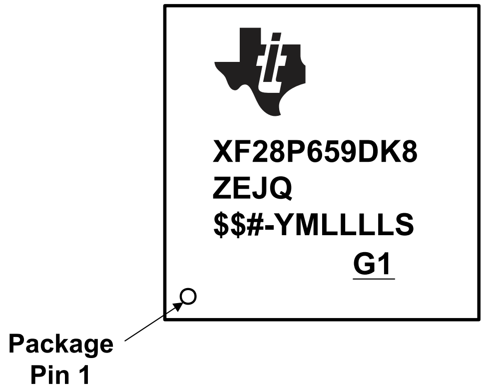
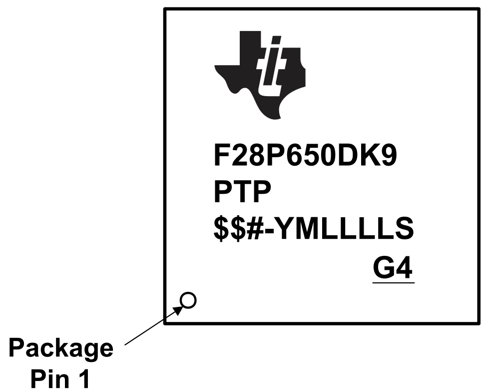


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G1 = ECAT

Figure 9-3. Package Symbolization for ZEJ Package – Automotive

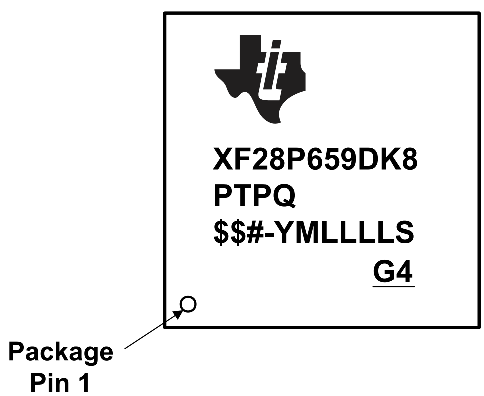


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-4. Package Symbolization for PTP Package – Non-Automotive

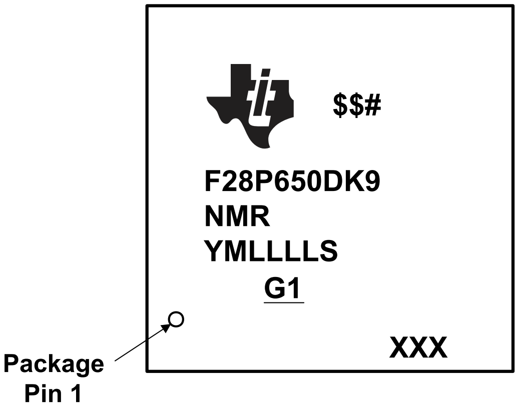


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-5. Package Symbolization for PTP Package – Automotive



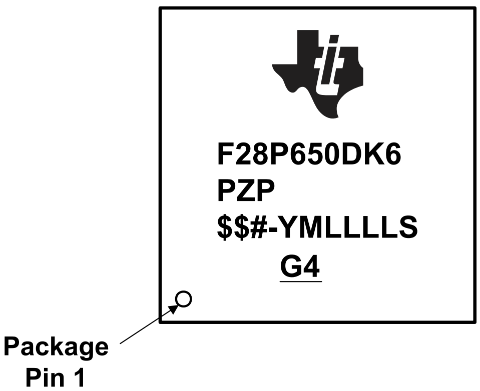
YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G1 = ECAT

XXX = 0–119
Serialized Number to indicate unit location on strip

Figure 9-6. Package Symbolization for NMR Package – Non-Automotive

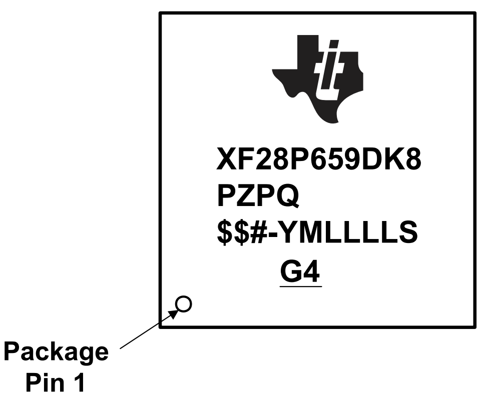


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-7. Package Symbolization for PZP Package – Non-Automotive



YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-8. Package Symbolization for PZP Package – Automotive

Table 9-1. Revision Identification

SILICON REVISION CODE	SILICON REVISION	REVID[(1)] ADDRESS: 0x5D00C	COMMENTS
Blank	0	0x0000 0001	This silicon revision is available as TMX.
A	A	0x0000 0002	This silicon revision is available as TMS.

(1) Silicon Revision ID

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9.4 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

Development Tools

F28P65X controlCARD
TMDSCNCD28P65X is a low-cost evaluation and development board for the TI C2000™ MCU series of F28P65x devices. It comes with a HSEC180 (180-pin high-speed edge connector), and as a controlCARD, is ideal for initial evaluation and prototyping. For evaluation of TMDSCNCD28P65X, a 180-pin docking station TMDSHSECDOCK is required and can be purchased separately or as a bundled kit.

LAUNCHXL-F28P65X
LAUNCHXL-F28P65X is a low-cost development board for the TI C2000™ real-time microcontrollers series of F28P65x devices. Ideal for initial evaluation and prototyping, it provides a standardized and easy-to-use platform to develop your next application. This extended version LaunchPad™ development kit offers extra pins for development and supports the connection of two BoosterPack™ plug-in modules. As part of the vast TI MCU LaunchPad ecosystem, it is also cross-compatible with a broad range of plug-in modules.

TI Resource Explorer
To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

C2000Ware for C2000 MCUs
C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

DigitalPower SDK
DigitalPower SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs), which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

MotorControl SDK
MotorControl SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs), which are targeted for industrial drive and other motor control, MotorControl SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

Code Composer Studio™ integrated development environment (IDE)
Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. Code Composer Studio is available for download across Windows®, Linux® and macOS® desktops. It can also be used in the cloud by visiting https://dev.ti.com. Code Composer Studio includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler and many other features. The intuitive IDE takes you through each step of the application development flow. Familiar tools and interfaces make getting started faster than ever before. The desktop version of Code Composer Studio combines the advantages of the Eclipse software framework with advanced capabilities from TI resulting in a compelling feature-rich environment. The cloud-based Code Composer Studio leverages the Theia application framework enabling development in the cloud without needing to download and install large amounts of software.

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SysConfig System configuration tool
SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the System configuration tool page.

C2000 Third-party search tool
TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

UniFlash Standalone Flash Tool
UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Design tools & simulation section of the Design & development page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site.

9.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Errata

TMS320F28P65x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F28P65x real-time microcontrollers.

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CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x DSPs.

Tools Guides

TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The SMT & packaging application notes website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

The Essential Guide for Developing With C2000™ Real-Time Microcontrollers provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

9.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Windows® is a registered trademark of Microsoft Corporation.
Linux® is a registered trademark of Linus Torvalds.
macOS® is a registered trademark of Apple Inc.
All trademarks are the property of their respective owners.

9.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

Changes from August 8, 2023 to November 14, 2023 **Page**

- **This Revision History lists the changes from SPRSP69A to SPRSP69B.** 1
- **Global:** TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas. For **SPI**, all instances of legacy terminology have been changed to controller and peripheral. All instances of legacy pin names have been changed to: POCI (Peripheral OUT Controller IN); PICO (Peripheral IN Controller OUT); and CS (Chip Select). For the **I2C Bus Interface**, all instances of legacy terminology have been changed to controller and target. For the **CAN and LIN Interface/BUS**, all instances of legacy terminology have been changed to commander and responder. For the **EtherCAT Controller**, all instances of legacy terminology have been changed to MainDevice (or MDevice) and SubordinateDevice (or SubDevice)....1
- **Global:** Changed document status statement from "ADVANCE INFORMATION for preproduction products; subject to change without notice" to "UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA"....1
- **Global:** Information on the TMS320F28P650DK9 and TMS320F28P650DK6 devices is Production Data....1
- **Global:** Information on the TMS320F28P650DK7, TMS320F28P650DK8, TMS320F28P650DH, TMS320F28P650SK, TMS320F28P650SH, TMS320F28P659DK-Q1, TMS320F28P659DH-Q1, and TMS320F28P659SH-Q1 devices is preview information only (not Production Data)....1
- *Features* section: Updated ADC MSPS values for 16-bit mode and 12-bit mode....1
- *Features* section: Updated **Security Peripherals**....1
- *Description* section: Added paragraph about evaluation board and C2000Ware....3
- *Device Information* table: Added "Preview information (not Production Data)" footnote....3
- *Device Comparison* table: Changed "Dual-zone Code Security Module (DCSM) for flash and RAM" to "Security: JTAGLOCK, Zero-pin boot, Dual-zone security"....7
- *Device Comparison* table: Updated MSPS and Conversion Time for ADC 16-bit mode....7
- *Device Comparison* table: Updated MSPS and Conversion Time for ADC 12-bit mode....7
- *Device Comparison* table: Updated device numbers in Package Options row....7
- *Device Comparison* table: Added status footnote for TMS320F28**P650DK** devices. Added "Preview information (not Production Data)" status footnote for all other devices....7
- *Pin Attributes* table: Added "Connect this pin to 3.3-V supply" to Description of VDD3VFL, VDDA, VDDIO, and VDDOSC....10
- *Power and Ground* table: Added "Connect this pin to 3.3-V supply" to Description of VDD3VFL, VDDA, VDDIO, and VDDOSC....64
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- *Analog Internal Connections* table: Updated table....163
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- *ADC Operating Conditions 12-bit Single-Ended* table: Updated table....174
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- *Block Diagram* section: Added "Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator" paragraph. Added "Reference DAC Block Diagram" figure........ 199
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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging information website.

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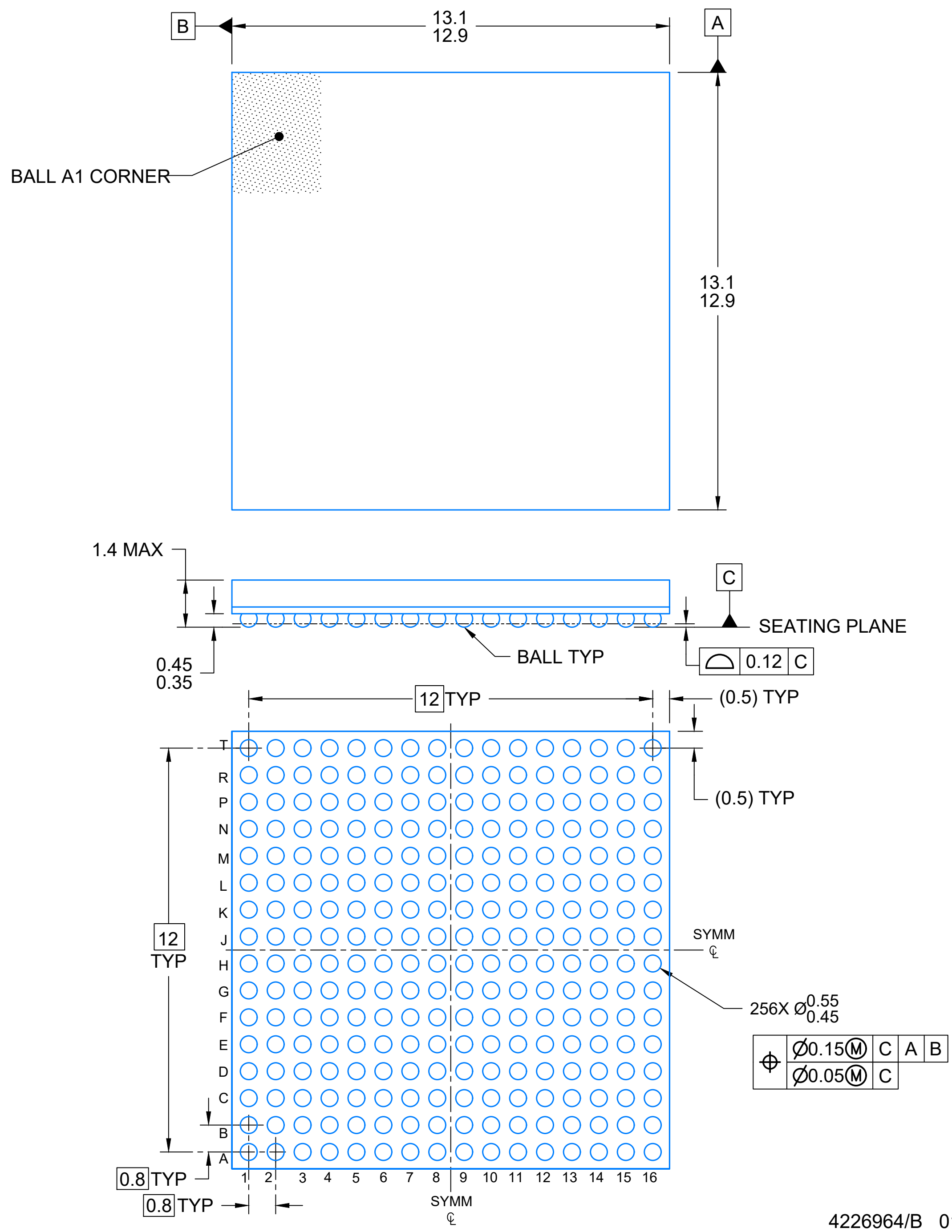
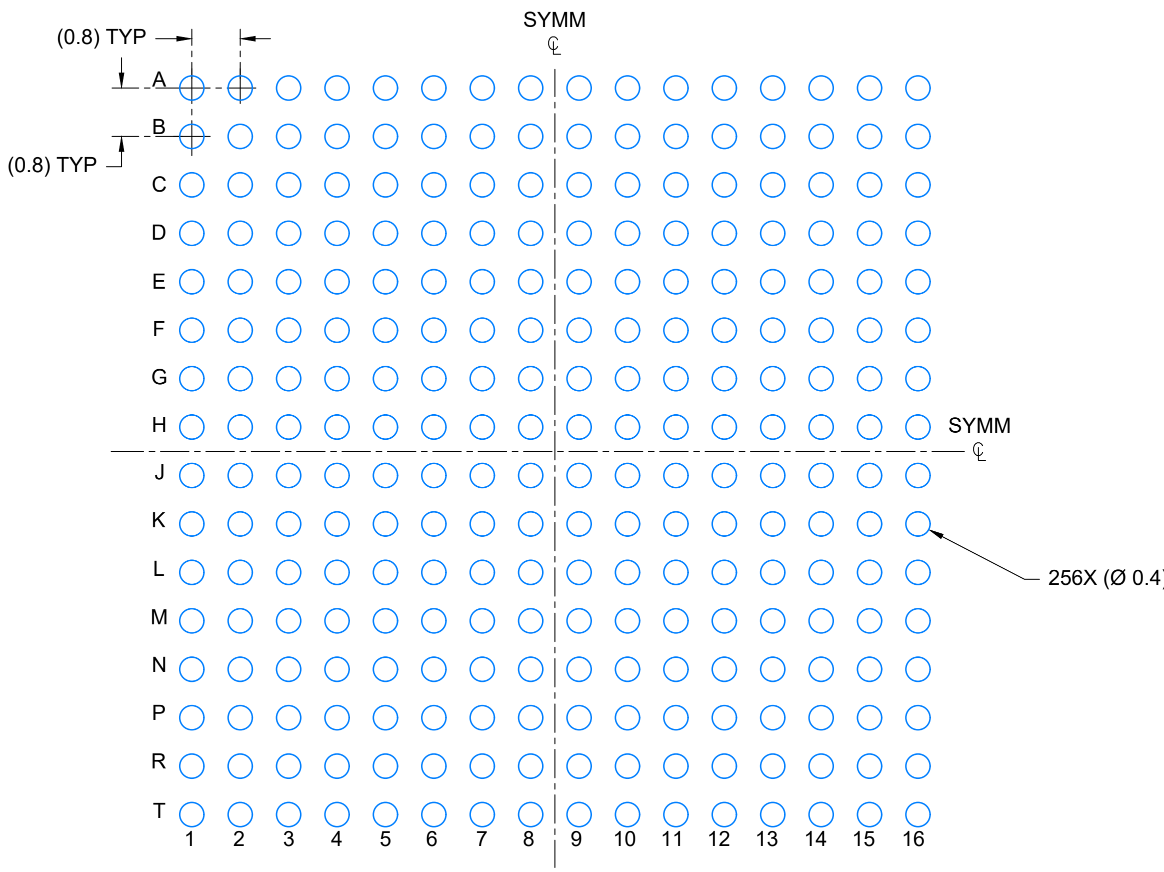


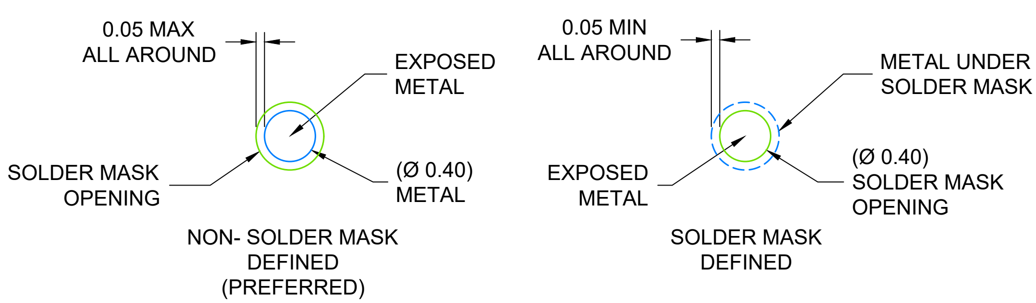
4226964/B 01/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 8X

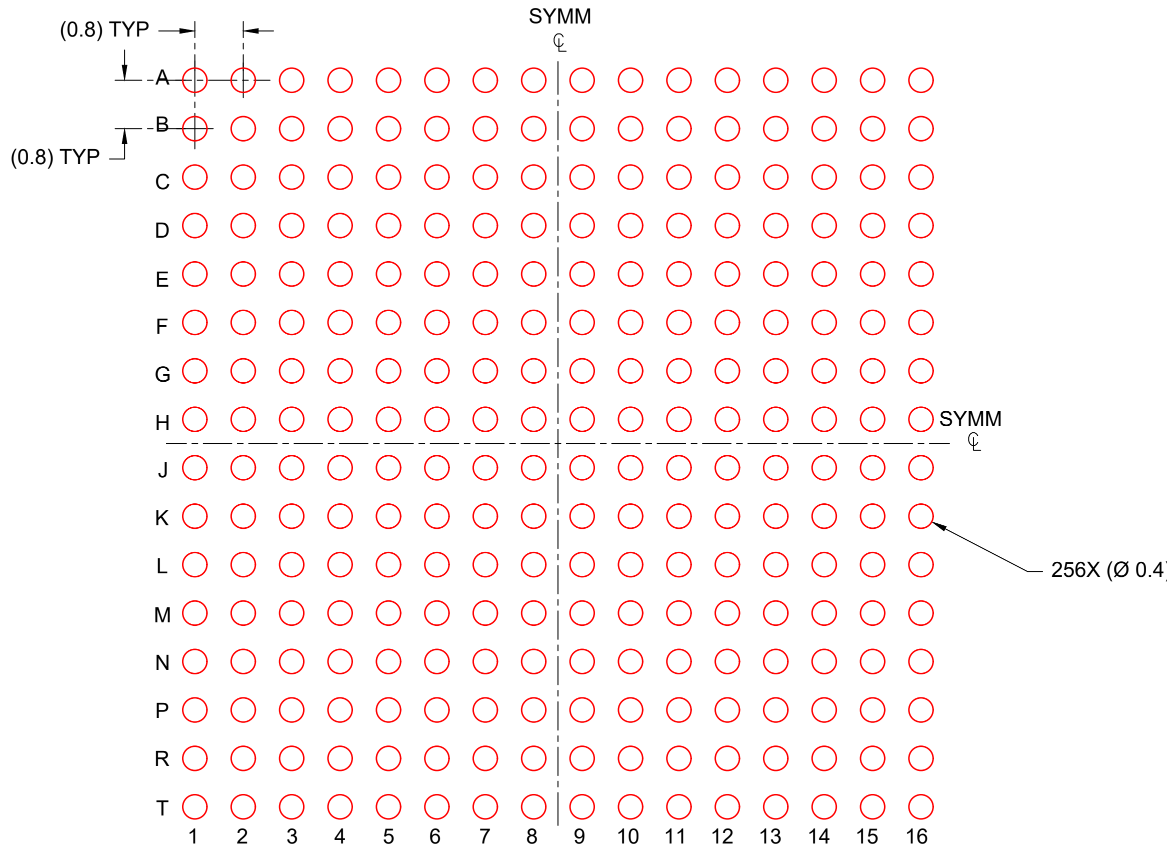


SOLDER MASK DETAILS
NOT TO SCALE

4226964/B 01/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

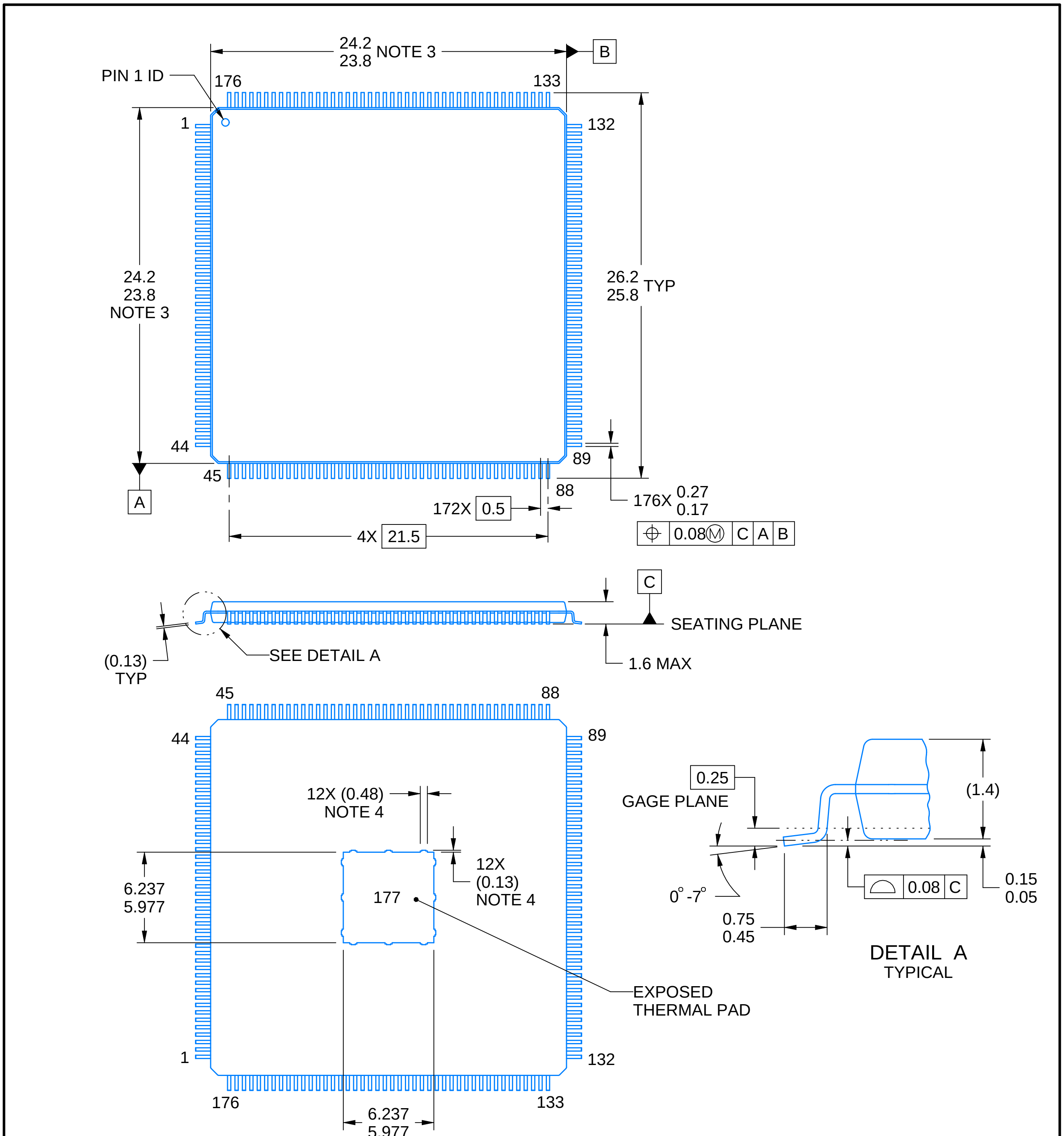


SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4226964/B 01/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

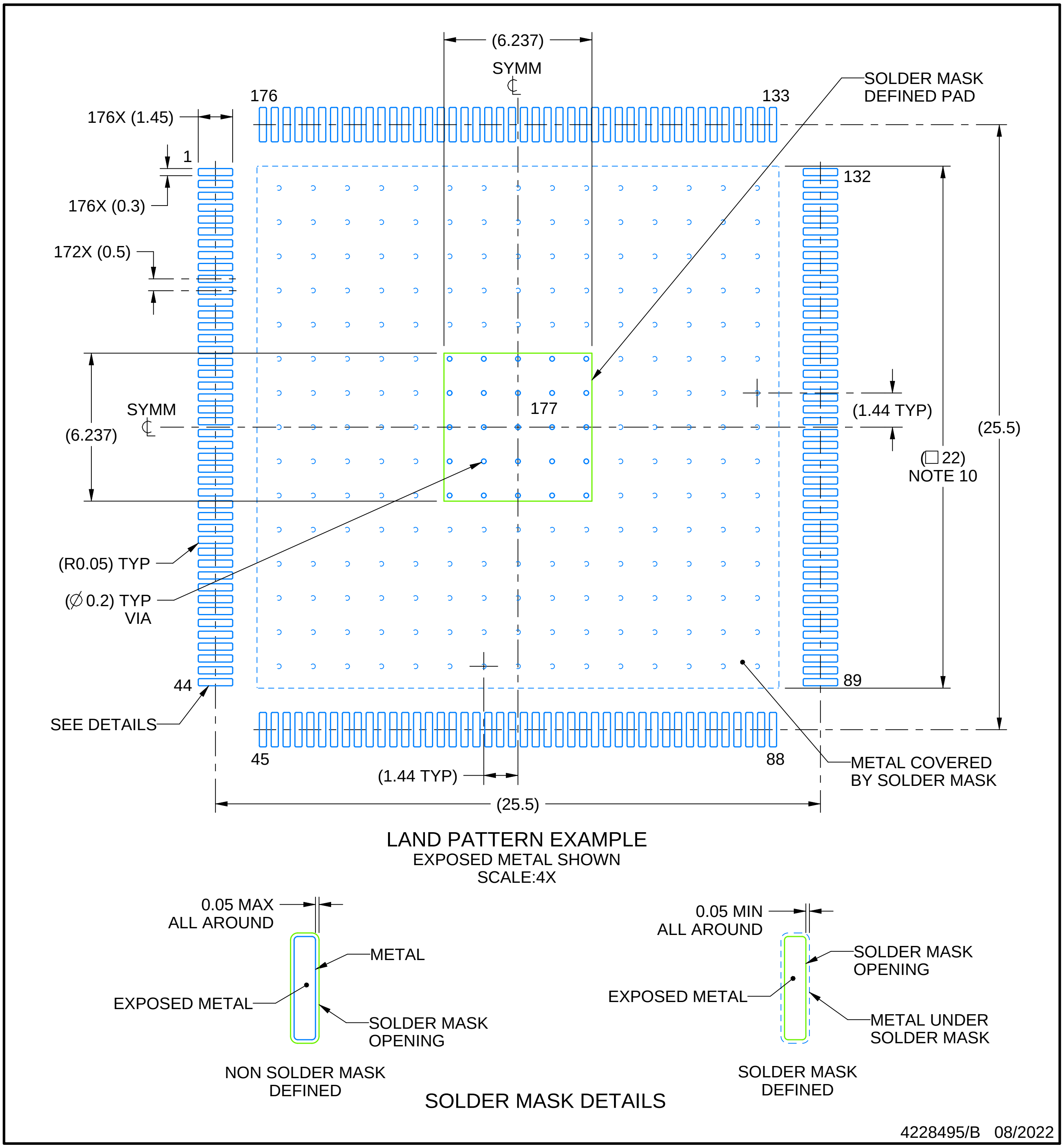


4228495/B 08/2022

PowerPAD is a trademark of Texas Instruments.

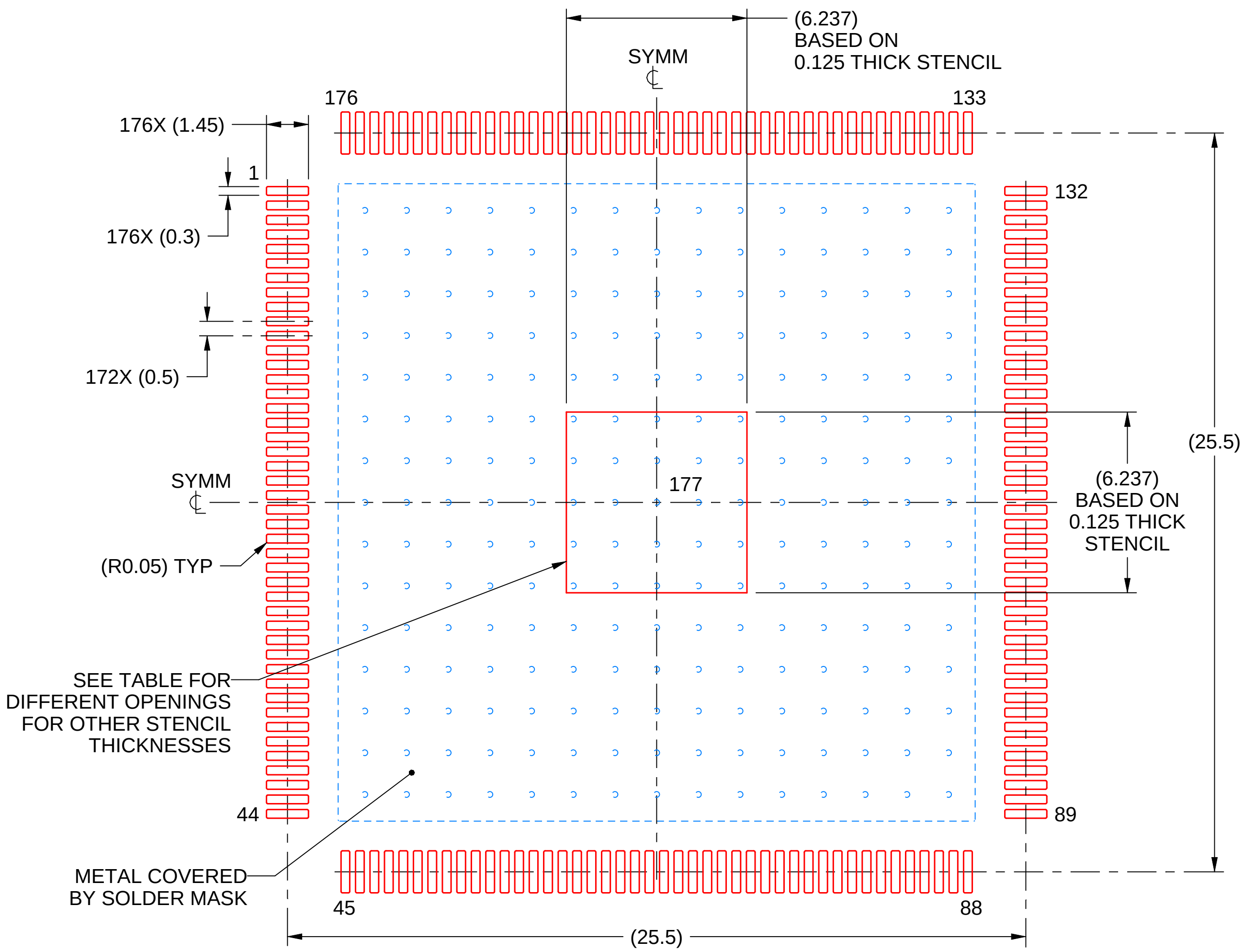
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features my not present.
5. Reference JEDEC registration MS-026.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



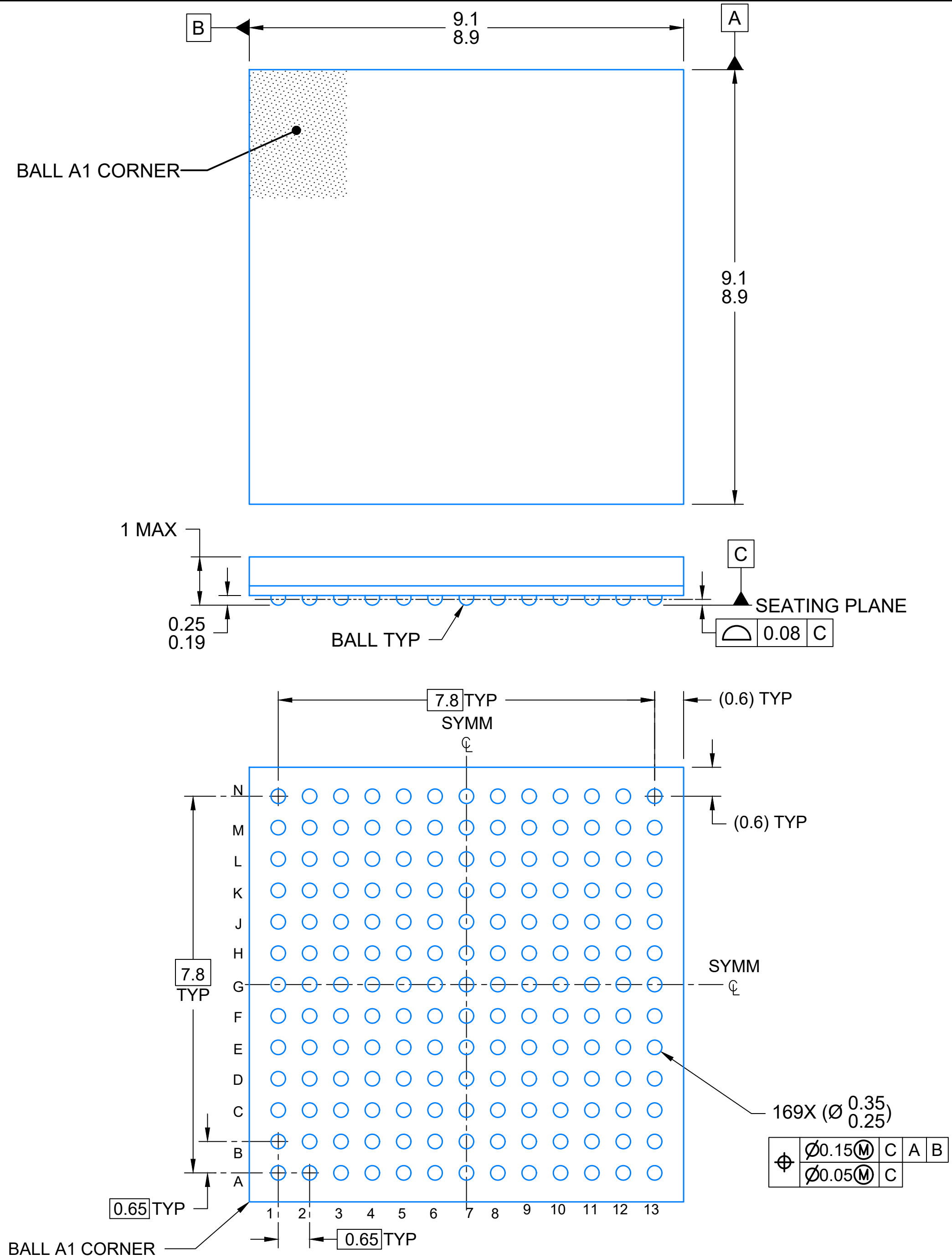
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:4X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.973 X 6.973
0.125	6.237 X 6.237 (SHOWN)
0.150	5.694 X 5.694
0.175	5.271 X 5.271

4228495/B 08/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

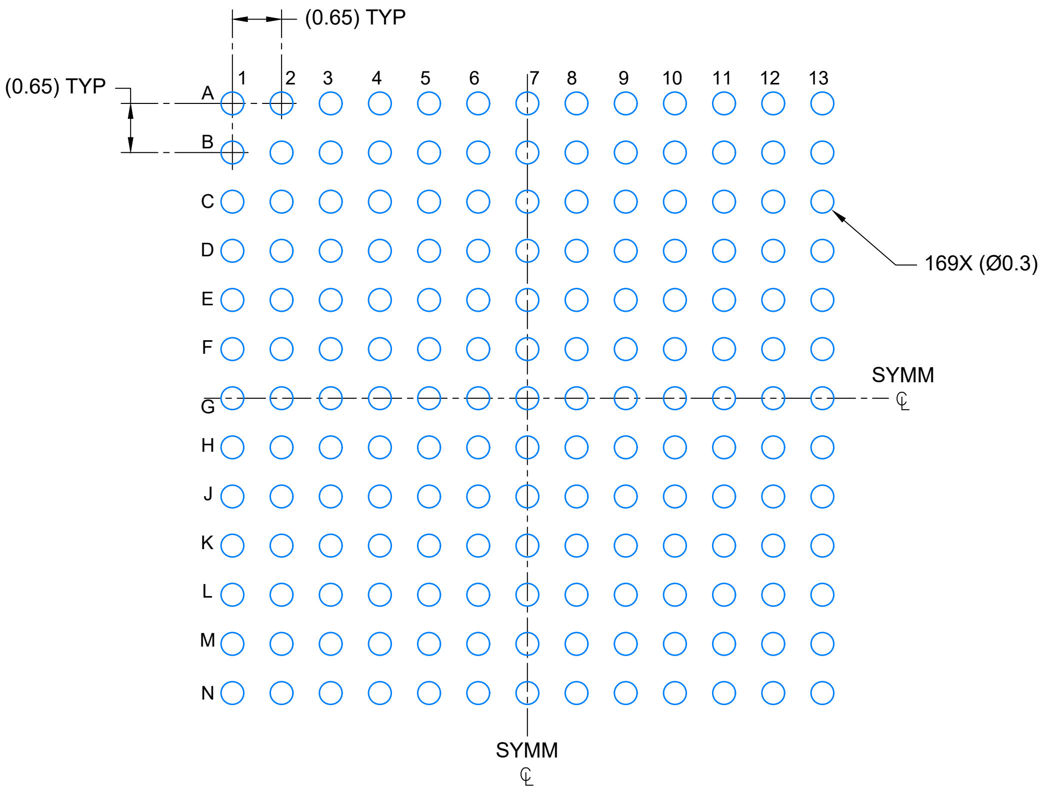


4226721/A 04/2021

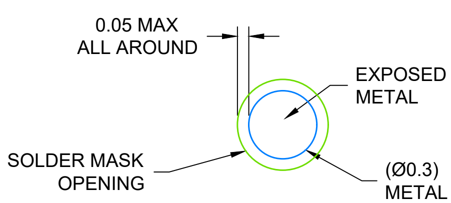
NOTES:

NanoFree is a trademark of Texas Instruments.

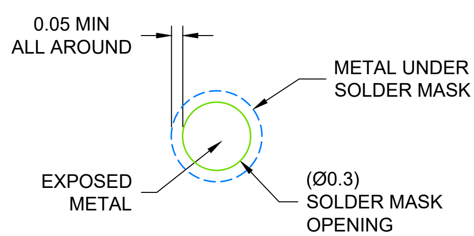
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 10X



NON- SOLDER MASK
DEFINED
(PREFERRED)



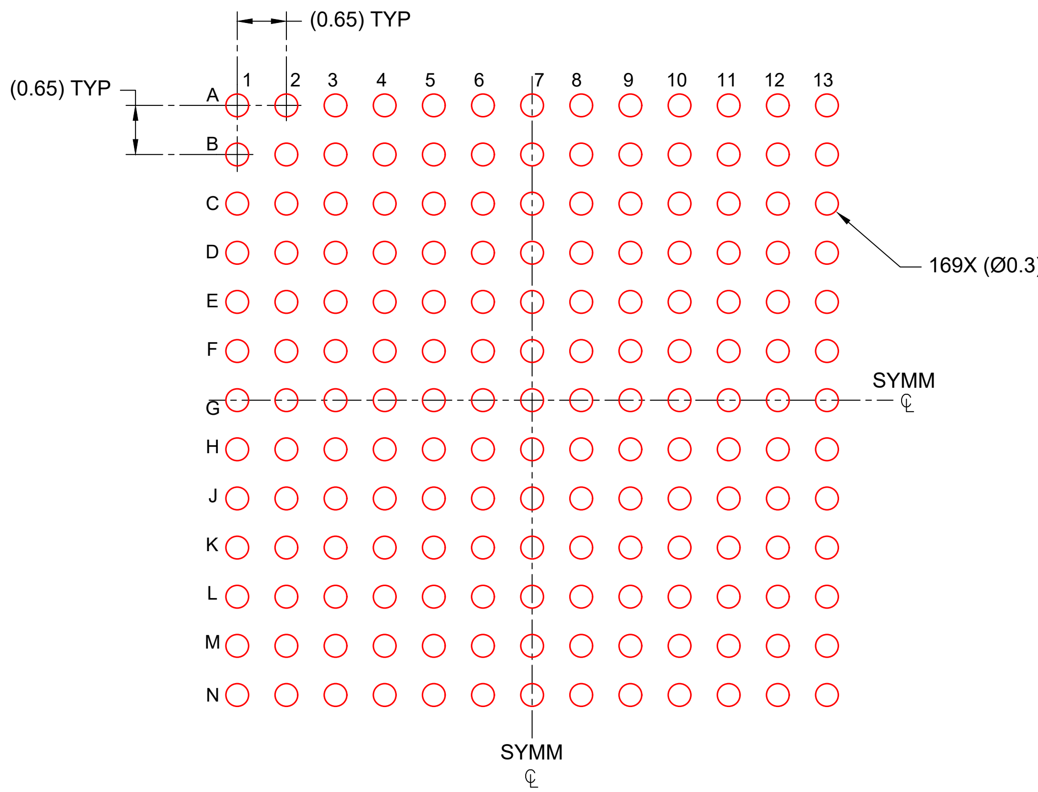
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4226721/A 04/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

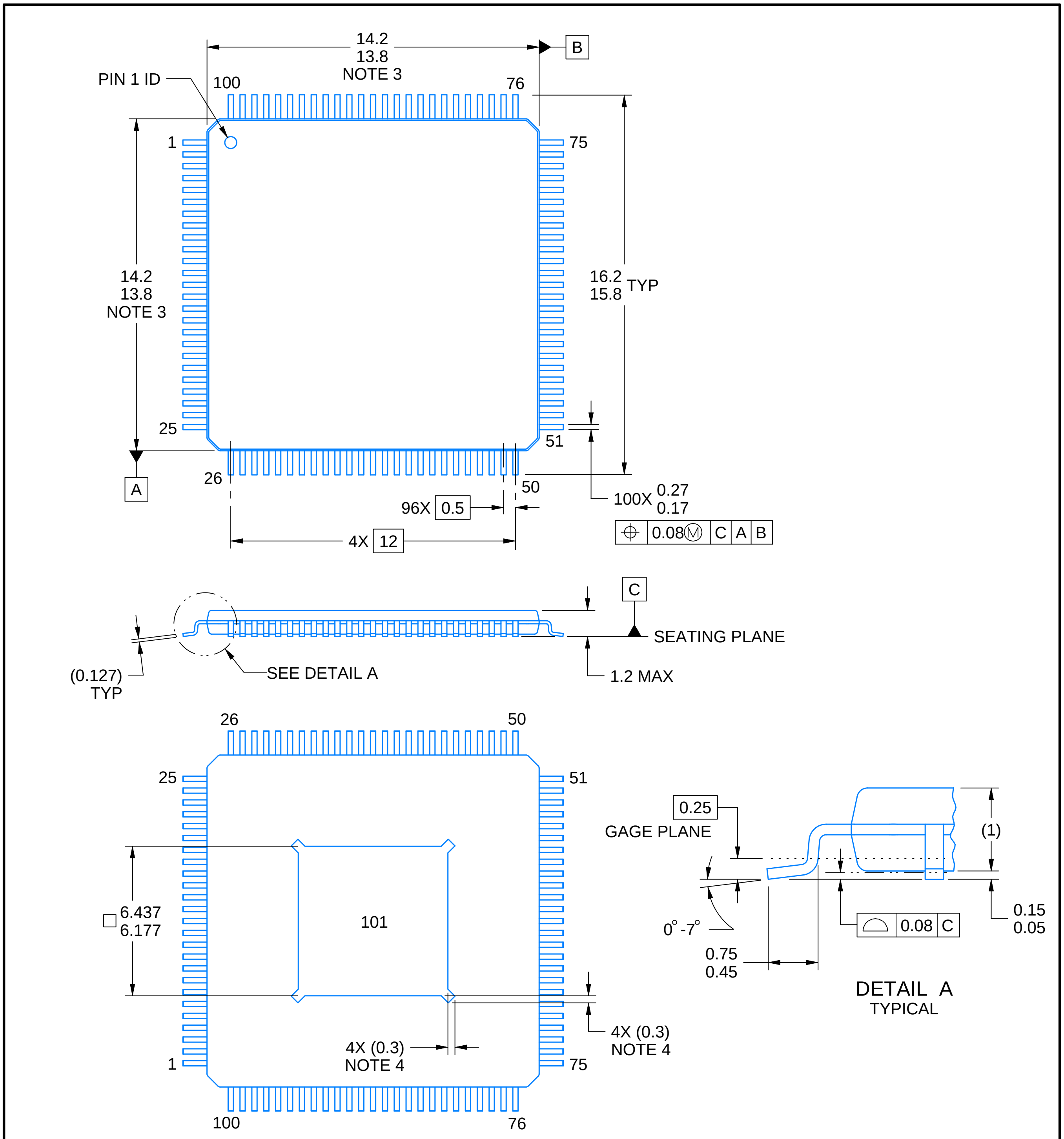


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4226721/A 04/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

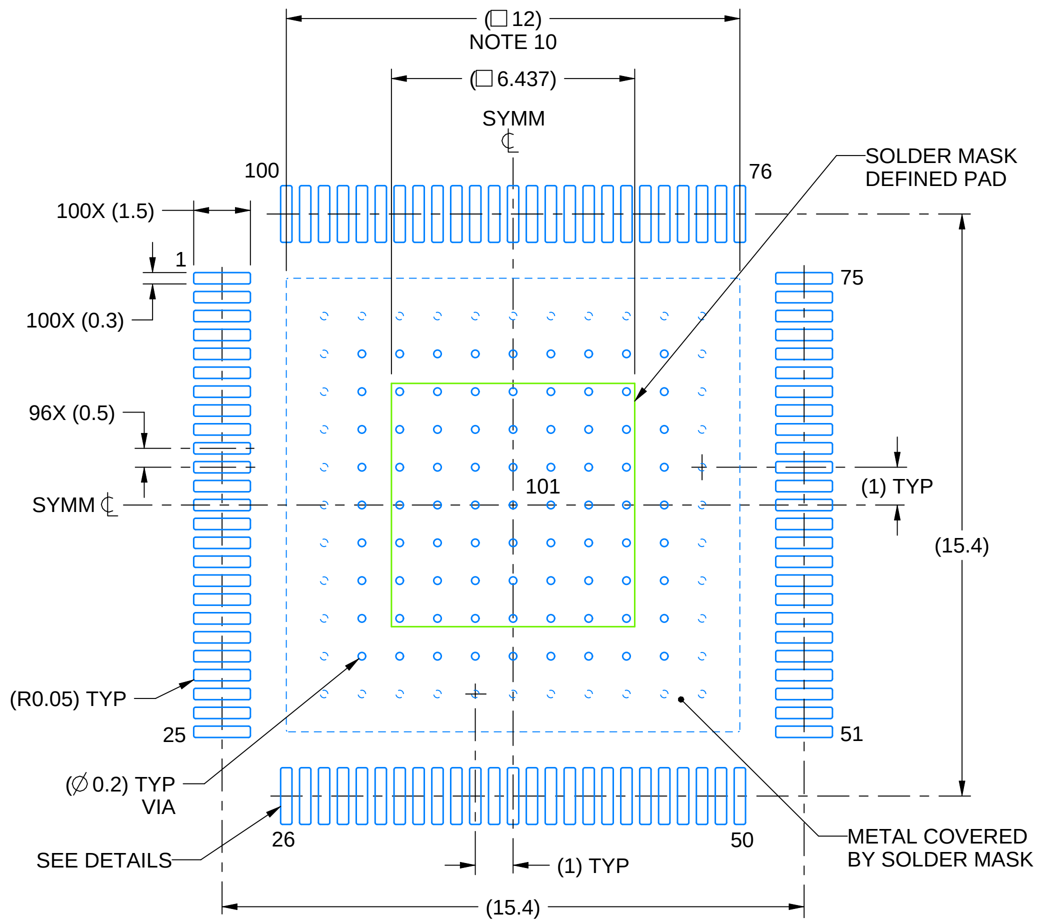


4228494/B 08/2022

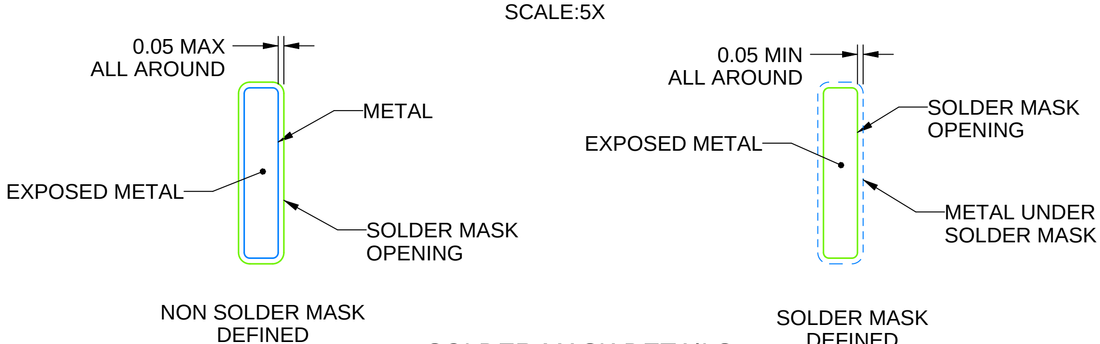
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

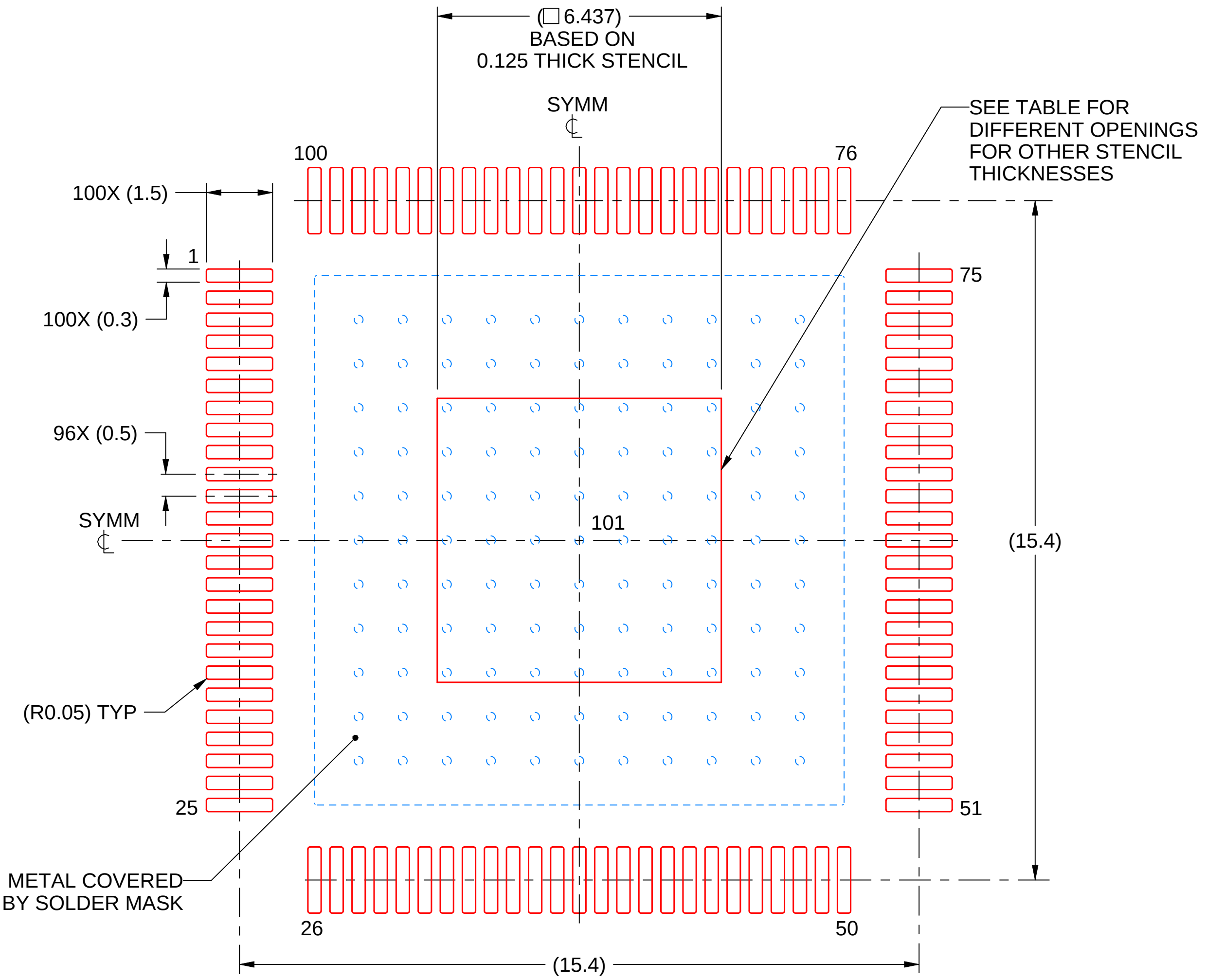


SOLDER MASK DETAILS

4228494/B 08/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.197 X 7.197
0.125	6.437 X 6.437 (SHOWN)
0.150	5.876 X 5.876
0.175	5.440 X 5.440

4228494/B 08/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
F28P650DH6NMRR	ACTIVE	NFBGA	NMR	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650DH6 NMR	Samples
F28P650DH6PTP	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650DH6 PTP	Samples
F28P650DH6PZPR	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650DH6 PZP	Samples
F28P650DH6ZEJR	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650DH6 ZEJ	Samples
F28P650DK6PZPR	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650DK6 PZP	Samples
F28P650DK7ZEJR	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650DK7 ZEJ	Samples
F28P650DK9PTP	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650DK9 PTP	Samples
F28P650SH6NMRR	ACTIVE	NFBGA	NMR	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SH6 NMR	Samples
F28P650SH6PTP	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650SH6 PTP	Samples
F28P650SH6PZPR	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650SH6 PZP	Samples
F28P650SH6ZEJR	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SH6 ZEJ	Samples
F28P650SH7NMRR	ACTIVE	NFBGA	NMR	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SH7 NMR	Samples
F28P650SH7PTP	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650SH7 PTP	Samples
F28P650SH7ZEJR	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SH7 ZEJ	Samples
F28P650SK6NMRR	ACTIVE	NFBGA	NMR	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SK6 NMR	Samples
F28P650SK6PTP	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650SK6 PTP	Samples
F28P650SK6PZPR	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650SK6	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										PZP	
F28P650SK6ZEJR	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SK6 ZEJ	Samples
F28P650SK7NMRR	ACTIVE	NFBGA	NMR	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SK7 NMR	Samples
F28P650SK7PTP	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P650SK7 PTP	Samples
F28P650SK7ZEJR	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P650SK7 ZEJ	Samples
F28P659DH8PZPRQ1	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P659DH8 PZPQ	Samples
F28P659DK8PTPQ1	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P659DK8 PTPQ	Samples
F28P659DK8PZPQ1	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P659DK8 PZPQ	Samples
F28P659DK8PZPRQ1	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P659DK8 PZPQ	Samples
F28P659DK8ZEJQ1	ACTIVE	NFBGA	ZEJ	256	119	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P659DK8 ZEJQ	Samples
F28P659DK8ZEJRQ1	ACTIVE	NFBGA	ZEJ	256	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28P659DK8 ZEJQ	Samples
F28P659SH6PTPQ1	ACTIVE	HLQFP	PTP	176	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P659SH6 PTPQ	Samples
F28P659SH6PZPRQ1	ACTIVE	HTQFP	PZP	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28P659SH6 PZPQ	Samples
XF28P650DK6PZP	ACTIVE	HTQFP	PZP	100	90	TBD	Call TI	Call TI	-40 to 125		Samples
XF28P650DK9PTP	ACTIVE	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		Samples
XF28P650DK9ZEJ	ACTIVE	NFBGA	ZEJ	256	119	TBD	Call TI	Call TI	-40 to 125		Samples
XF28P659DK8PTPQ1	ACTIVE	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		Samples
XF28P659DK8PZPRQ1	ACTIVE	HTQFP	PZP	100	1000	TBD	Call TI	Call TI	-40 to 125		Samples
XF28P659DK8ZEJRQ1	ACTIVE	NFBGA	ZEJ	256	1000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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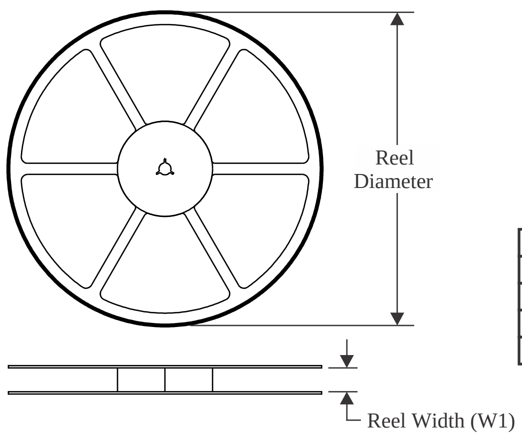
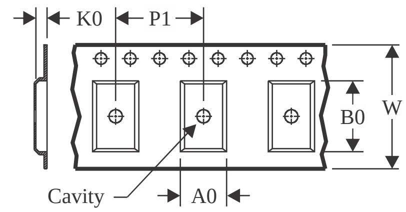
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

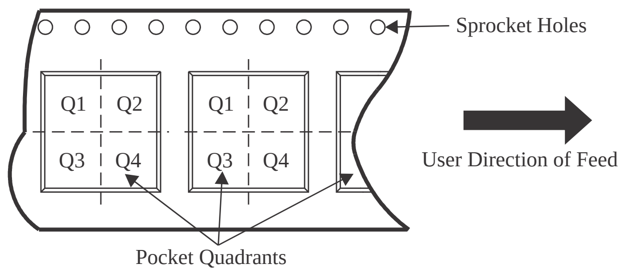


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

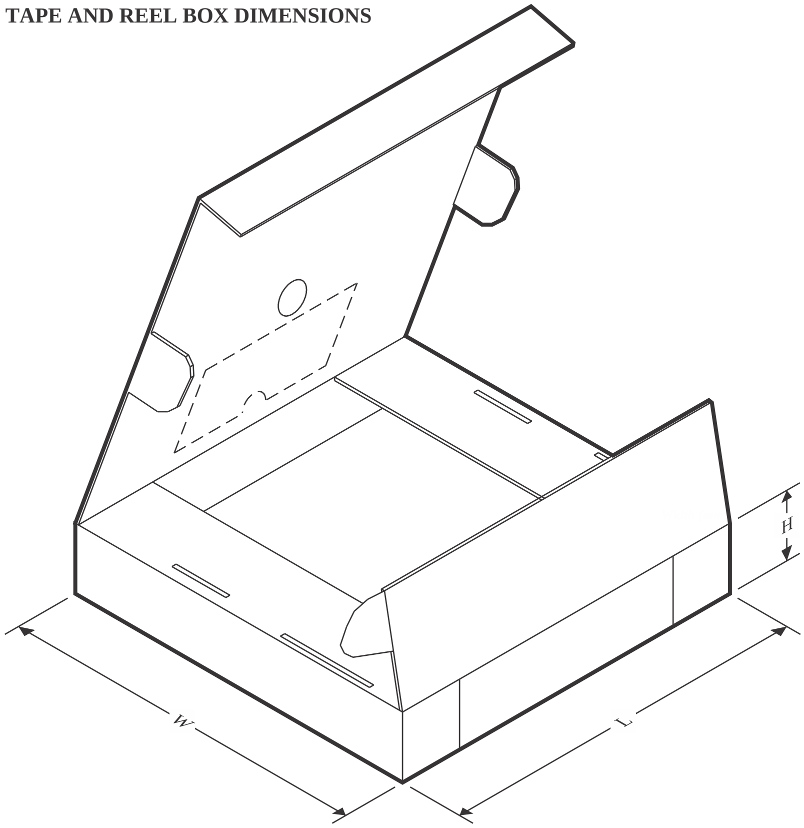


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
F28P650DH6NMRR	NFBGA	NMR	169	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
F28P650DH6PZPR	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
F28P650DH6ZEJR	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P650DK6PZPR	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
F28P650DK7ZEJR	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P650SH6NMRR	NFBGA	NMR	169	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
F28P650SH6PZPR	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
F28P650SH6ZEJR	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P650SH7NMRR	NFBGA	NMR	169	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
F28P650SH7ZEJR	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P650SK6NMRR	NFBGA	NMR	169	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
F28P650SK6PZPR	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
F28P650SK6ZEJR	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P650SK7NMRR	NFBGA	NMR	169	1000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q1
F28P650SK7ZEJR	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P659DH8PZPRQ1	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
F28P659DK8PZPRQ1	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
F28P659DK8ZEJRQ1	NFBGA	ZEJ	256	1000	330.0	24.4	13.35	13.35	2.6	16.0	24.0	Q1
F28P659SH6PZPRQ1	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

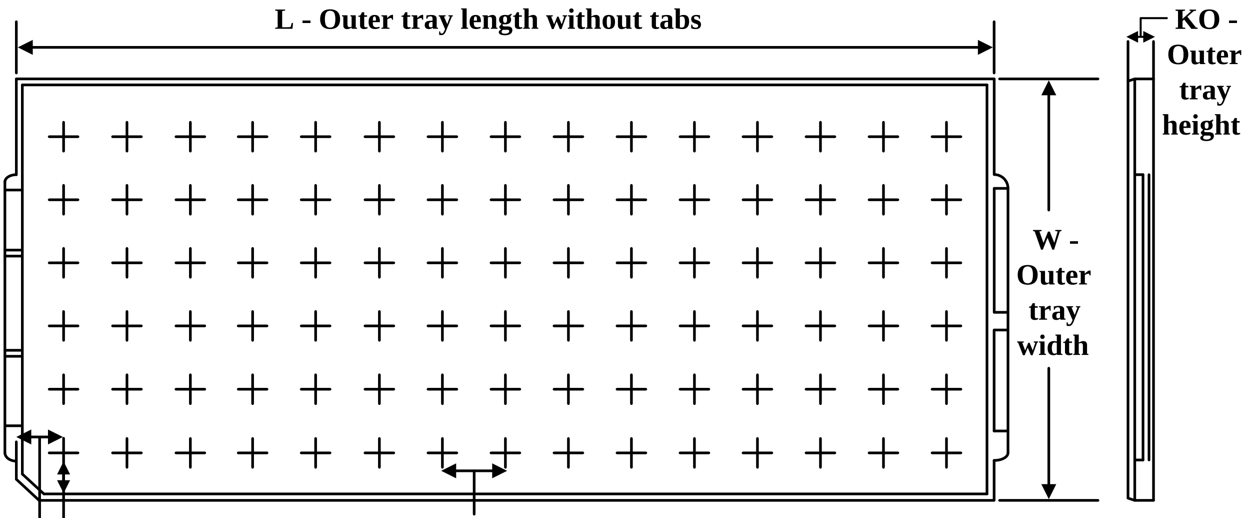


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
F28P650DH6NMRR	NFBGA	NMR	169	1000	336.6	336.6	31.8
F28P650DH6PZPR	HTQFP	PZP	100	1000	367.0	367.0	55.0
F28P650DH6ZEJR	NFBGA	ZEJ	256	1000	336.6	336.6	41.3
F28P650DK6PZPR	HTQFP	PZP	100	1000	367.0	367.0	55.0
F28P650DK7ZEJR	NFBGA	ZEJ	256	1000	336.6	336.6	41.3
F28P650SH6NMRR	NFBGA	NMR	169	1000	336.6	336.6	31.8
F28P650SH6PZPR	HTQFP	PZP	100	1000	367.0	367.0	55.0
F28P650SH6ZEJR	NFBGA	ZEJ	256	1000	336.6	336.6	41.3
F28P650SH7NMRR	NFBGA	NMR	169	1000	336.6	336.6	31.8
F28P650SH7ZEJR	NFBGA	ZEJ	256	1000	336.6	336.6	41.3
F28P650SK6NMRR	NFBGA	NMR	169	1000	336.6	336.6	31.8
F28P650SK6PZPR	HTQFP	PZP	100	1000	367.0	367.0	55.0
F28P650SK6ZEJR	NFBGA	ZEJ	256	1000	336.6	336.6	41.3
F28P650SK7NMRR	NFBGA	NMR	169	1000	336.6	336.6	31.8
F28P650SK7ZEJR	NFBGA	ZEJ	256	1000	336.6	336.6	41.3
F28P659DH8PZPRQ1	HTQFP	PZP	100	1000	367.0	367.0	55.0
F28P659DK8PZPRQ1	HTQFP	PZP	100	1000	367.0	367.0	55.0
F28P659DK8ZEJRQ1	NFBGA	ZEJ	256	1000	336.6	336.6	41.3

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
F28P659SH6PZPRQ1	HTQFP	PZP	100	1000	367.0	367.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
F28P650DH6PTP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P650DK9PTP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P650SH6PTP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P650SH7PTP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P650SK6PTP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P650SK7PTP	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P659DK8PTPQ1	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28P659DK8PZPQ1	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
F28P659DK8ZEJQ1	ZEJ	NFBGA	256	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
F28P659SH6PTPQ1	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7

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