# TPD1E1B04 1-Channel ESD Protection Diode with Low $R_{DYN}$ and Low Clamping Voltage

## 1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±30-kV Contact Discharge
  - ±30-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 6.3 A (8/20 µs)
- IO Capacitance: 1 pF (Typical)
- DC Breakdown Voltage: 6.4 V (Typical)
- Low Leakage Current: 100 nA (Maximum)
- Extremely Low ESD Clamping Voltage
  - 8.5 V at ±16-A TLP
  - $R_{DYN}$: 0.15 Ω
- Industrial Temperature Range: –40°C to +125°C
- Industry Standard 0402 Package

## 2 Applications

- End Equipment
  - Wearables
  - Laptops and Desktops
  - Mobile and Tablets
  - Set-Top Boxes
  - DVR and NVR
  - TV and Monitors
  - EPOS (Electronic Point of Sale)
- Interfaces
  - USB 2.0/1.1
  - GPIO
  - Pushbuttons
  - Audio

## 3 Description

The TPD1E1B04 is a bidirectional TVS ESD protection diode featuring low $R_{DYN}$ and low clamping voltage. The TPD1E1B04 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

The ultra-low dynamic resistance (0.15 Ω) and extremely low clamping voltage (8.5 V at 16-A TLP) ensure system level protection against transient events. This device features a 1-pF IO capacitance making it ideal for protecting interfaces such as USB 2.0.

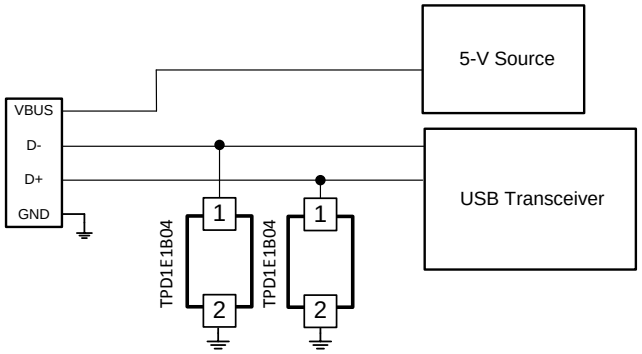
The TPD1E1B04 is offered in the industry standard 0402 (DPY) package.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPD1E1B04 | X1SON (2) | 0.60 mm x 1.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical USB 2.0 Application Schematic**



# Table of Contents



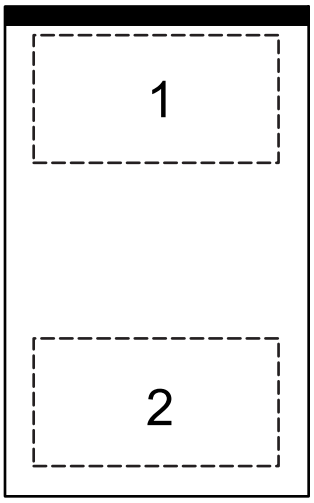
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (May 2016) to Revision A | Page |
|---|---|
| • Changed device status from *Product Preview* to *Production Data* | 1 |

# 5 Pin Configuration and Functions

**DPY Package**
**2-Pin X1SON**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | IO | I/O | ESD Protected Channel. If used as ESD IO, connect pin 2 to ground |
| 2 | IO | I/O | ESD Protected Channel. If used as ESD IO, connect pin 1 to ground |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Electrical fast transient | IEC 61000-4-4 (5/50 ns) | | 80 | A |
| Peak pulse | IEC 61000-4-5 Power ($t_p$ - 8/20 µs) | | 50 | W |
| | IEC 61000-4-5 Current ($t_p$ - 8/20 µs) | | 6.3 | A |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 155 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 ESD Ratings—IEC Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 contact discharge | ±30000 | V |
| | | IEC 61000-4-2 air-gap discharge | ±30000 | |

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IO}$ | Input pin voltage | –3.6 | 3.6 | V |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

## 6.5 Thermal Information

| THERMAL METRIC(1) | | TPD1E1B04 DPY (X1SON) 2 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 420 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 169.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 276.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 122.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 157.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse stand-off voltage | $I_{IO}$ < 100 nA | –3.6 | | 3.6 | V |
| $V_{BRF}$ | Breakdown voltage, any IO pin to GND | Measured as the maximum voltage before device snaps back into $V_{HOLD}$ voltage | | 6.4 | | V |
| $V_{BRR}$ | Breakdown voltage, GND to any IO pin | Measured as the maximum voltage before device snaps back into $V_{HOLD}$ voltage | | –6.4 | | V |
| $V_{HOLD}$ | Holding voltage | $I_{IO}$ = 1 mA, $T_A$ = 25°C | 5 | 6 | 6.6 | V |
| $V_{CLAMP}$ | Clamping voltage | $I_{PP}$ = 1 A, TLP, from IO to GND | | 6.3 | | V |
| | | $I_{PP}$ = 5 A, TLP, from IO to GND | | 6.8 | | |
| | | $I_{PP}$ = 16 A, TLP, from IO to GND | | 8.5 | | |
| | | $I_{PP}$ = 1 A, TLP, from GND to IO | | 6.3 | | |
| | | $I_{PP}$ = 5 A, TLP, from GND to IO | | 6.8 | | |
| | | $I_{PP}$ = 16 A, TLP, from GND to IO | | 8.5 | | |
| $I_{LEAK}$ | Leakage current, IO to GND | $V_{IO}$ = ±2.5 V | | 0.2 | 100 | nA |
| $R_{DYN}$ | Dynamic resistance | IO to GND | | 0.15 | | Ω |
| | | GND to IO | | 0.15 | | |
| $C_L$ | Line capacitance | $V_{IO}$ = 0 V, f = 1 MHz, IO to GND, $T_A$ = 25°C | | 1 | 1.3 | pF |

## 6.7 Typical Characteristics

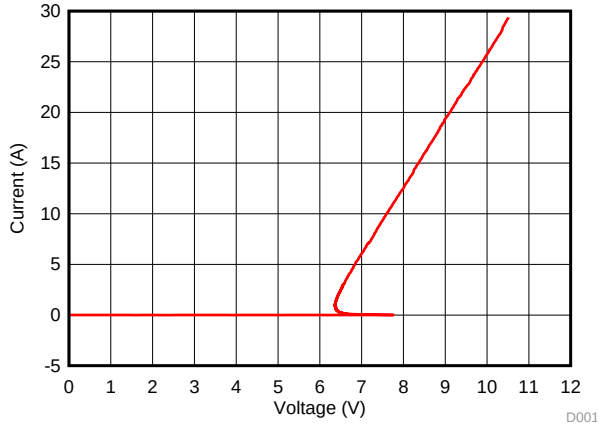



**Figure 1. Positive TLP Curve**

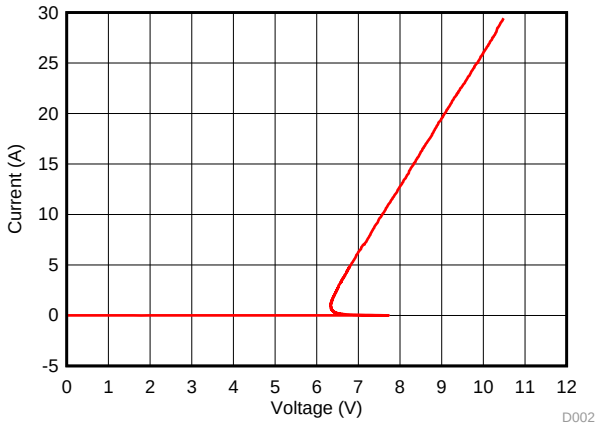



**Figure 2. Negative TLP Curve**

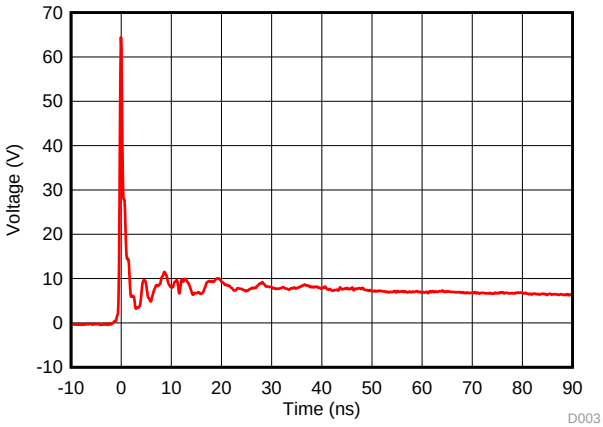



**Figure 3. 8-kV IEC Waveform**

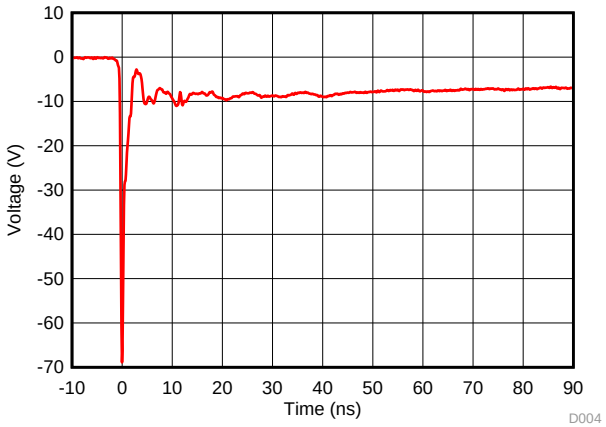



**Figure 4. –8-kV IEC Waveform**

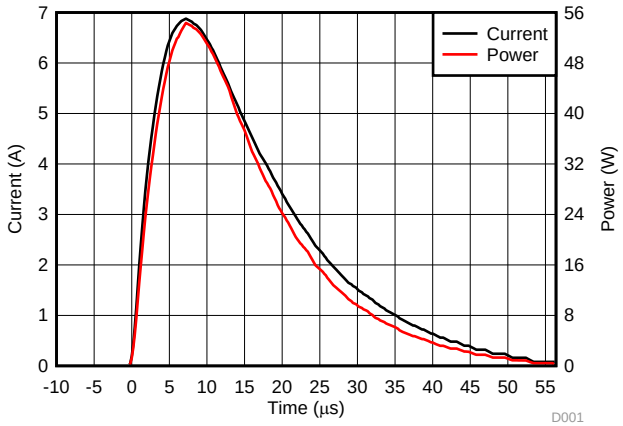



**Figure 5. Surge Curve ($t_p$ = 8/20 µs), Any IO Pin to GND**

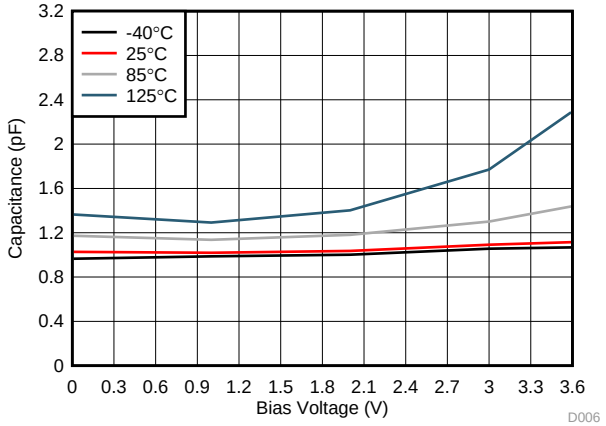



**Figure 6. Capacitance vs. Bias Voltage**

## Typical Characteristics (continued)

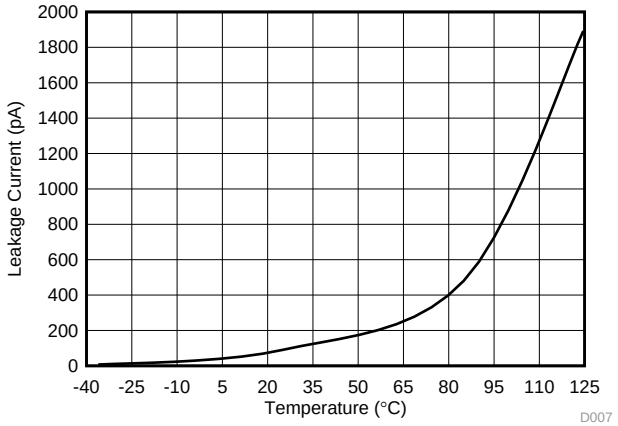



**Figure 7. Leakage Current vs. Temperature**

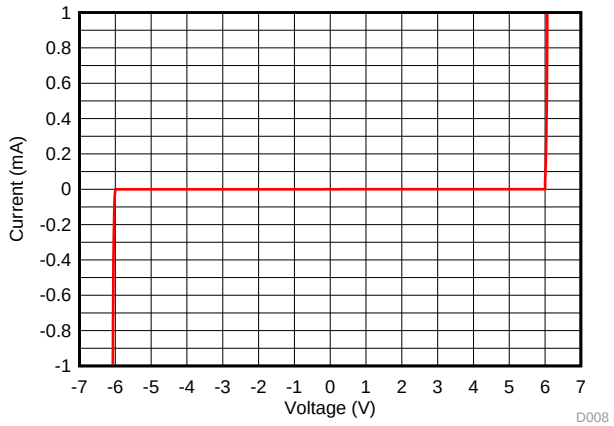



**Figure 8. DC Voltage Sweep I-V Curve**

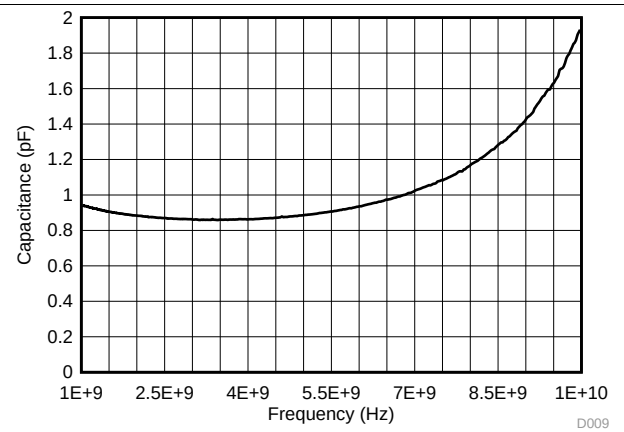



**Figure 9. Capacitance vs. Frequency**

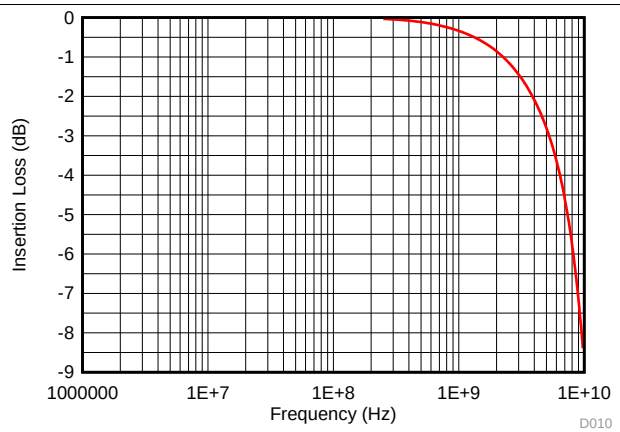


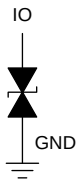

**Figure 10. Insertion Loss**

# 7 Detailed Description

## 7.1 Overview

The TPD1E1B04 is a bidirectional ESD Protection Diode with ultra-low clamping voltage. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low clamping makes this device ideal for protecting any sensitive signal pins.

## 7.2 Functional Block Diagram






## 7.3 Feature Description

### 7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±30-kV contact and ±30-kV air gap. An ESD-surge clamp diverts the current to ground.

### 7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

### 7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 6.3 A and 50 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

### 7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 1 pF (typical) and 1.3 pF (maximum).

### 7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V typical. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

### 7.3.6 Low Leakage Current

The I/O pins feature an low leakage current of 100 nA (maximum) with a bias of ±2.5 V.

### 7.3.7 Extremely Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.5 V ($I_{PP}$ = 16 A).

### 7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

### 7.3.9 Industry Standard Footprint

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

## 7.4 Device Functional Modes

The TPD1E1B04 is a passive integrated circuit that triggers when voltages are above $V_{BRF}$ or below $V_{BRR}$. During ESD events, voltages as high as ±30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E1B04 (usually within 10s of nano-seconds) the device reverts to passive.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPD1E1B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a safe level for the protected IC.

## 8.2 Typical Application

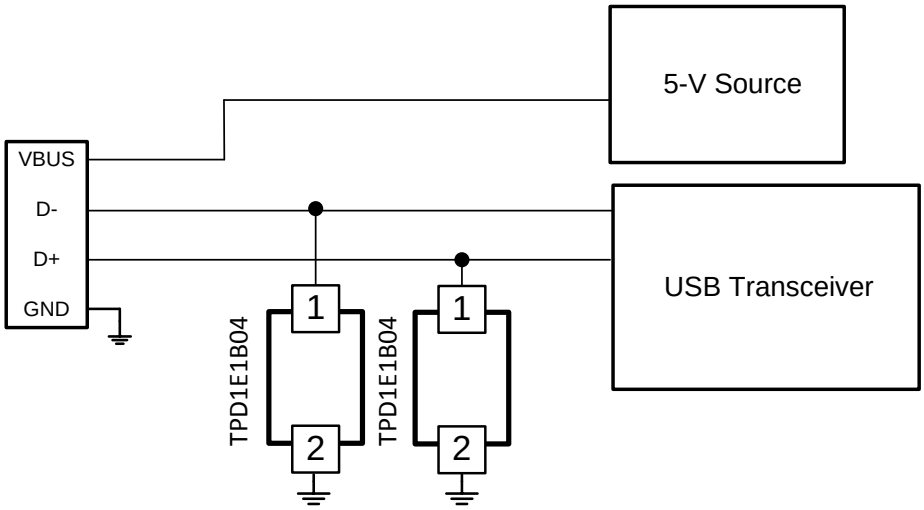





**Figure 11. USB 2.0 ESD Schematic**

### 8.2.1 Design Requirements

For this design example, two TPD1E1B04 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in Table 1 are known.

**Table 1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Signal range on DP-DM lines | 0 V to 3.6 V |
| Operating frequency on DP-DM lines | up to 240 MHz |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Signal Range*

The TPD1E1B04 supports signal ranges between –3.6 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

#### 8.2.2.2 Operating Frequency

The TPD1E1B04 has a 1-pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

### 8.2.3 Application Curve

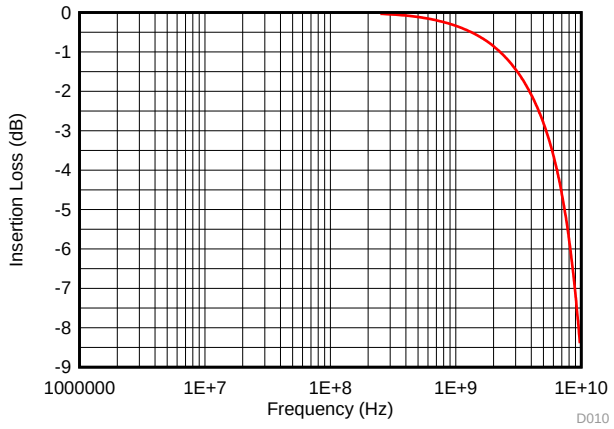



**Figure 12. Insertion Loss**

# 9 Power Supply Recommendations

The TPD1E1B04 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

# 10 Layout

## 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

## 10.2 Layout Example

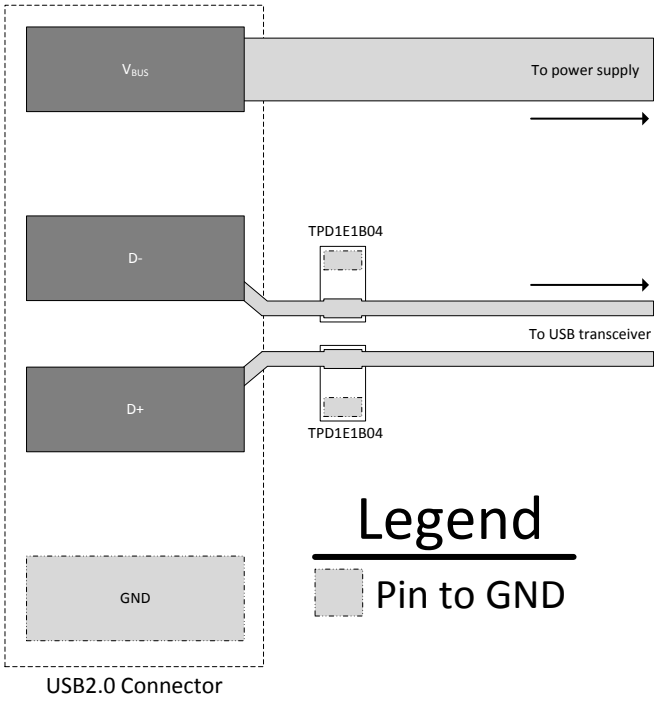



**Figure 13. USB 2.0 ESD Layout**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

*TPD1E1B04 Evaluation Module*, SLVUAN7

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPD1E1B04DPYR | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 4X |
| TPD1E1B04DPYR.B | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4X |
| TPD1E1B04DPYRG4 | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4X |
| TPD1E1B04DPYRG4.B | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4X |
| TPD1E1B04DPYT | Active | Production | X1SON (DPY) \| 2 | 250 \| SMALL T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 4X |
| TPD1E1B04DPYT.B | Active | Production | X1SON (DPY) \| 2 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 4X |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

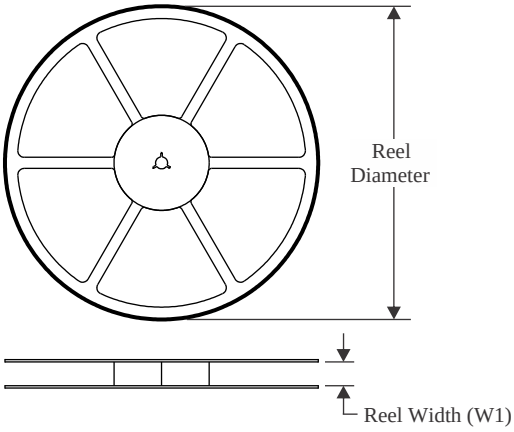
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

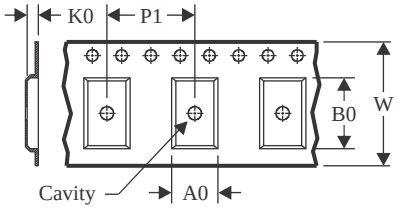
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

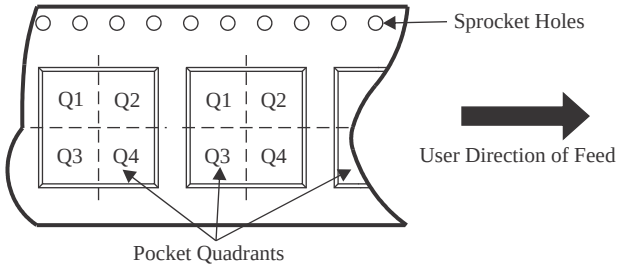



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

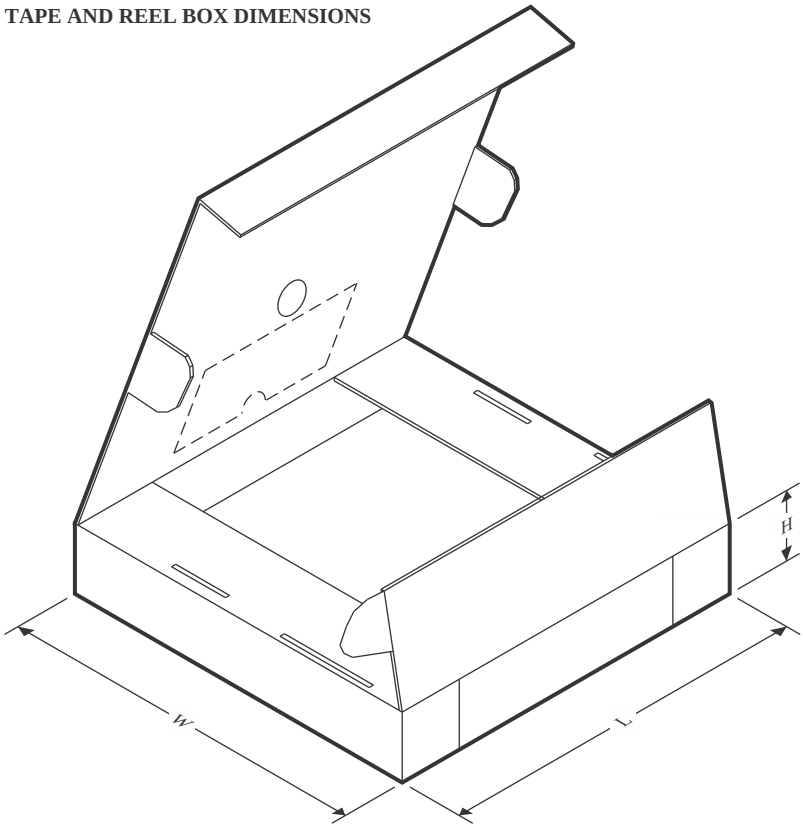
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD1E1B04DPYR | X1SON | DPY | 2 | 10000 | 180.0 | 8.4 | 0.67 | 1.15 | 0.46 | 2.0 | 8.0 | Q2 |
| TPD1E1B04DPYRG4 | X1SON | DPY | 2 | 10000 | 180.0 | 8.4 | 0.67 | 1.15 | 0.46 | 2.0 | 8.0 | Q2 |
| TPD1E1B04DPYT | X1SON | DPY | 2 | 250 | 180.0 | 9.5 | 0.66 | 1.15 | 0.66 | 2.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD1E1B04DPYR | X1SON | DPY | 2 | 10000 | 210.0 | 185.0 | 35.0 |
| TPD1E1B04DPYRG4 | X1SON | DPY | 2 | 10000 | 210.0 | 185.0 | 35.0 |
| TPD1E1B04DPYT | X1SON | DPY | 2 | 250 | 184.0 | 184.0 | 19.0 |

# GENERIC PACKAGE VIEW

## DPY 2

## X1SON - 0.45 mm max height

**1 x 0.6 mm**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

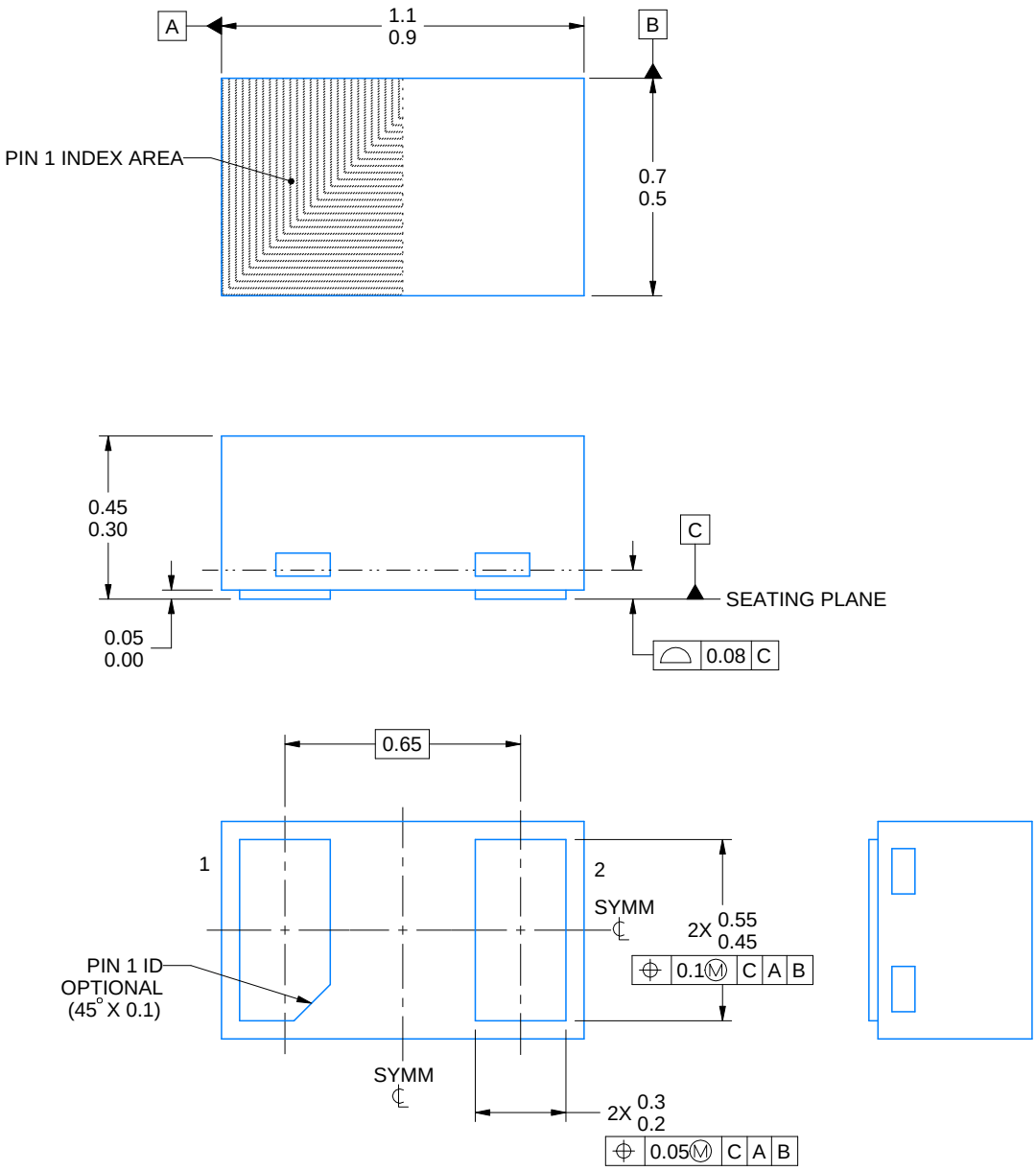

4231484/A

# PACKAGE OUTLINE

## DPY0002A

## X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

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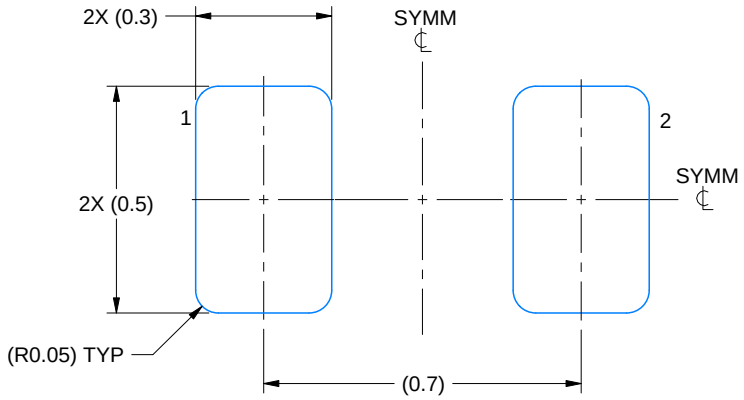
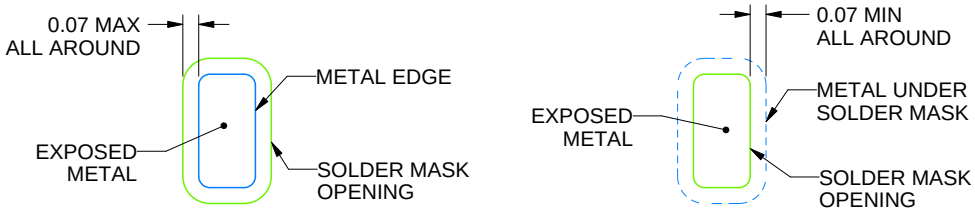
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X




SOLDER MASK DETAILS

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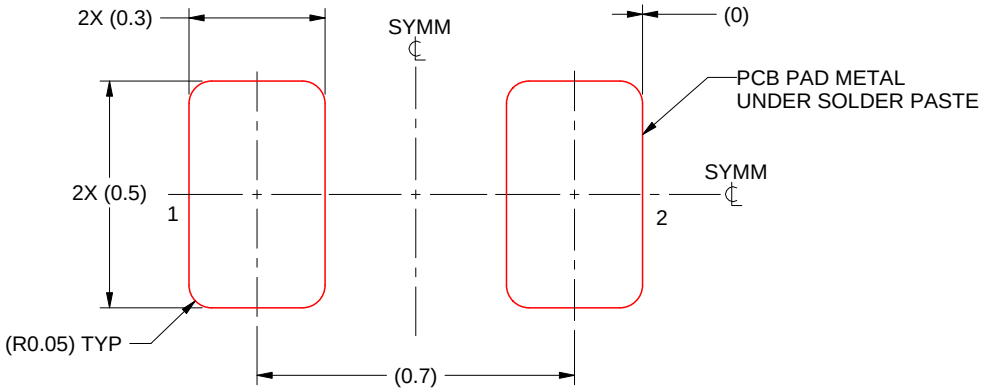
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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