

Phase-Noise and Jitter Performance of CDCLVC1310

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ABSTRACT

Clock jitter is a crucial factor for the overall system performance in today’s high-end systems like data communication, wired and wireless infrastructure and other high-speed applications. While distributing low-jitter clock sources, maintaining the best possible clock jitter over the distribution network to achieve a required system jitter. While distributing low jitter clock sources it is of highest interest to maintain the best clock jitter possible over the distribution network to achieve a required system jitter.

To drive other devices from a clock source with usually restricted driving capability, a buffer on a clock signal path must be added. As system requirements tighten, a question arises: does a simple buffer added on a clock line worsen the clock jitter somehow, and if yes, what kind of values should be considered?

This application report presents and focuses on phase-noise measurements of the CDCLVC1310 as a clock buffer with signal-level translation and as a crystal buffer. In addition, the differences between noise floor, additive jitter and system-level additive jitter are explained.

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1 Introduction

This report presents data demonstrating the ultra low phase noise outputs of the CDCLVC1310. The test results were obtained under nominal conditions: clean power supply, room temperature and no other noise source near the device under test, such as close-by integrated circuits.

The CDCLVC1310 is a highly-versatile, low-jitter, low-power clock fanout buffer distributing one of three inputs to ten low-jitter LVCMOS clock outputs. The primary and secondary inputs on the device feature differential or single-ended signals and a third input adds a crystal input. Such a buffer is intended for use in a variety of wireless and wired infrastructure, data communication, computing, low-power medical imaging and portable test and measurement applications. The input is fail-safe proved and translates any illegal input level into a defined output state. The core can be set to 2.5 V or 3.3 V and the output can be set to 1.5 V, 1.8 V, 2.5 V or 3.3 V. The CDCLVC1310 is configured with pin programming. The overall additive jitter performance is 30 fs_{RMS} (typ).

1.1 Definitions

Noise Floor is defined as the generated phase noise of the buffer if an ideal clock is attached to it. In this application report, the noise floor was calculated from a phase-noise measurement with a very clean signal generator as the input source. The output phase noise was subtracted by the input phase noise to simulate the input with an ideal clock source.

Additive Jitter is defined as the added amount of jitter to the input signal caused by the device itself and can be calculated as $J_{rms,add} = \sqrt{J_{rms,out}^2 - J_{rms,in}^2}$. It assumes that the noise processes are random and the input noise is not correlated to the output noise. Additive jitter must be measured with a clock source where phase noise is below the noise floor of the buffer itself.

System-Level Additive Jitter is defined as the rms phase jitter contribution of the buffer on a system level ($J_{rms,sysLvlAddJit} = J_{rms,out} - J_{rms,in}$). On a system level, the input noise is usually higher than the noise floor of the device so the linear addition method is used to calculate the jitter contribution.

1.2 Guideline: Additive Jitter or System-Level Additive Jitter?

In all implementations of clock distribution trees, the total timing budget is important. For the total timing budget calculation either additive jitter or system-level additive jitter has to be considered.

If the noise floor of a system or a clock tree is already higher than the noise floor of the CDCLVC1310, system-level additive jitter has to be considered. That is the case if the input source noise floor is similar (not less than 3 dB smaller) or higher than the buffer noise floor (-164 dBc/Hz) as in general-purpose clock generators.

In case of a system noise floor which is lower as the noise floor (-164 dBc/Hz) of the CDCLVC1310, additive jitter has to be considered. This is the case if an OCXO is used as input source or if the input noise floor is less than 3 dB smaller than the buffer noise floor.

Other data sheets often report additive jitter measured under the system-level additive jitter condition. This will reflect smaller and misleading additive jitter numbers that cannot be compared with TI's additive jitter numbers.

Table 1. Guideline: Additive Jitter or System-Level Additive Jitter?

Input Noise Floor for CDCLVC1310	Additive Jitter	System-Level Additive Jitter
Less than -164dBc/Hz	X	
Greater than -164dBc/Hz		X

2 Test Setup

The block diagrams of the test setup are shown in [Figure 1](#), [Figure 2](#) and [Figure 3](#). In all three configurations the Agilent E5052 was used as a phase-noise analyzer. All measurements were taken on the CDCLVC1310 EVM with nominal supplies and at room temperature.

The input signal of the system-level additive jitter measurements was generated by the cascade of a signal generator SMA100A and a pulse generator HP8133A. This ensures an input signal with an rms phase noise of roughly 180 fs.

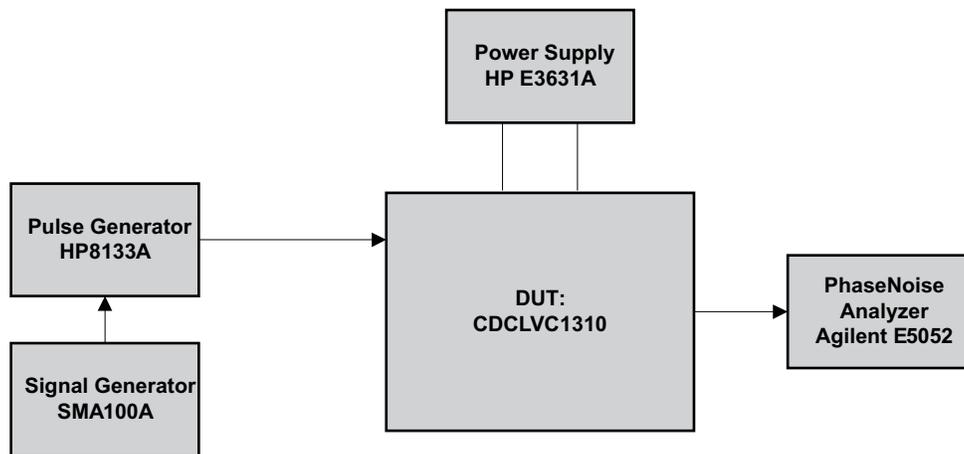


Figure 1. Test Setup for System-Level Additive Jitter Measurements

The additive jitter measurements were done with the Signal Generator SMA100A and with two oven-controlled crystal oscillators (OCXOs) at different frequencies.

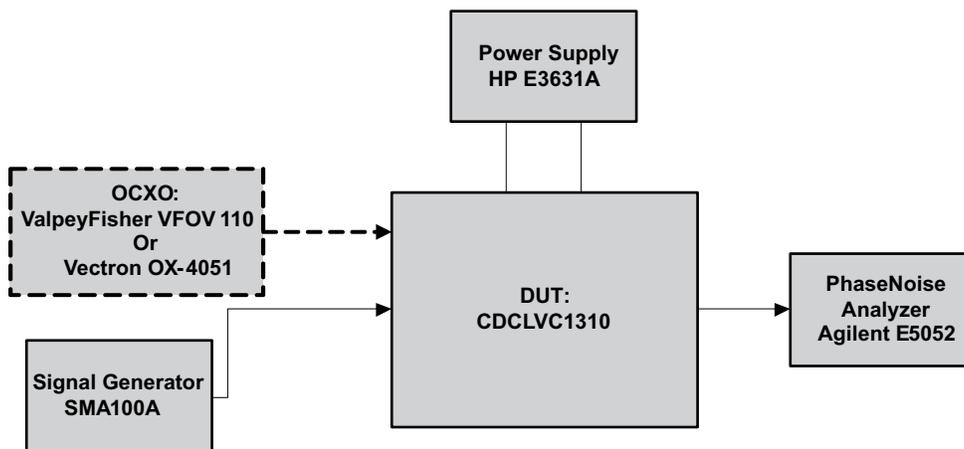


Figure 2. Test Setup for Additive Jitter Measurements

The phase-noise performance of the crystal oscillator was measured with the standard 25-MHz crystal resonator which is mounted on the CDCLVC1310 EVM.

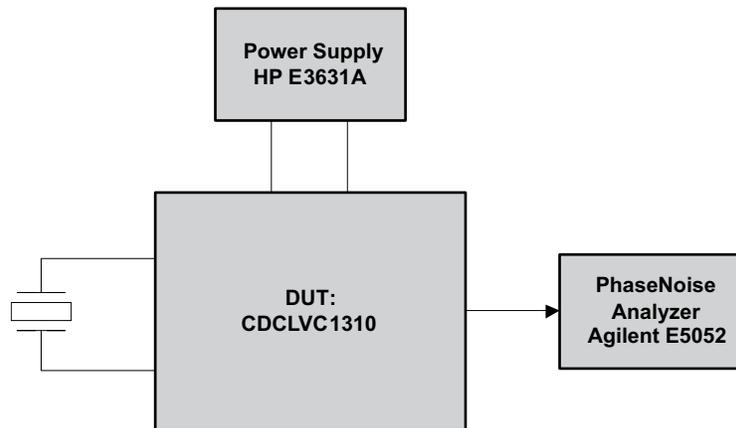


Figure 3. Test Setup for Crystal Oscillator Phase-Noise Measurements

3 Clock Buffer Jitter Measurements

Section 3.1 shows a phase-noise plot and summary of the system-level additive jitter measurements made on the CDCLVC1310 at an input frequency of 125 MHz. Section 3.2 shows the summary of the additive jitter and the noise-floor measurements. Section 3.3 shows the impact of slew rate on additive jitter.

3.1 System-Level Additive Jitter

Table 2 lists the system-level additive jitter values of the CDCLVC1310 with different supply voltages. Figure 4 shows the phase-noise plot of the measurement at a supply voltage of $V_{DD} = V_{DDO} = 3.3$ V.

The system-level additive jitter measurements show there is only a negligible amount of jitter added from the CDCLVC1310 to high phase-noise inputs.

Table 2. System-Level Additive Jitter at 125 MHz

V_{DD}/V_{DDO} Supply Range	Input rms Phase Jitter [fs]	Output rms Phase Jitter [fs]	System-Level Additive Jitter [fs]
3.3 V/3.3 V	182.1	183.8	1.7
3.3 V/2.5 V	182.1	187.1	5.1
3.3 V/1.8 V	182.1	185.5	3.4
3.3 V/1.5 V	182.1	194.4	12.6
2.5 V/2.5 V	183.5	214.5	31.1
2.5 V/1.8 V	183.5	212.9	29.5
2.5 V/1.5 V	183.5	221.0	37.6

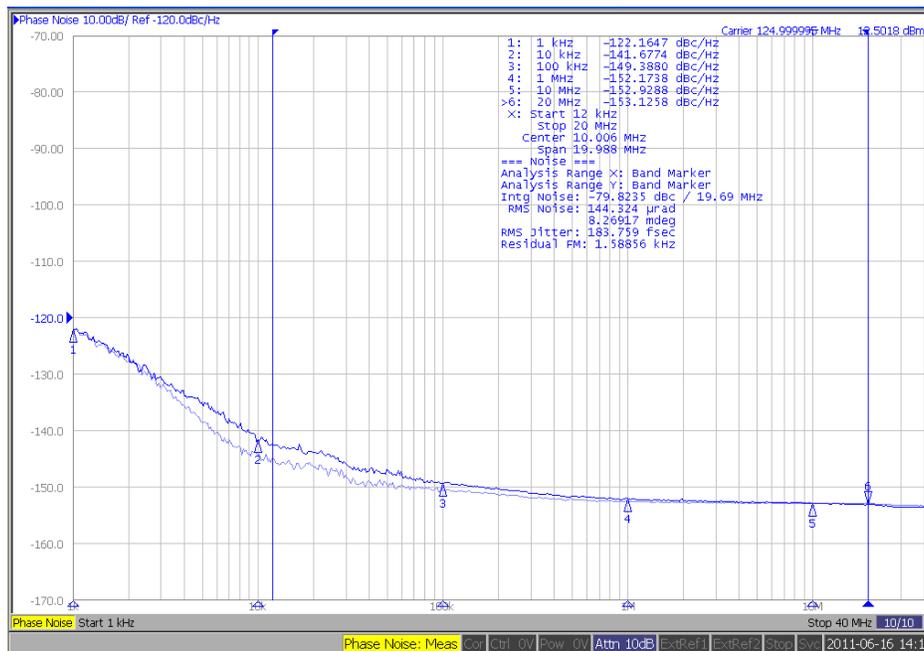


Figure 4. Input Phase Noise (182.1 fs, Light Blue) and Output Phase Noise (183.7 fs, Dark Blue)

3.2 Additive Jitter and Noise Floor

Table 3 lists the additive jitter capability of the CDCLVC1310 in a frequency range of 12 kHz to 20 MHz. Figure 5 shows an example of the measured phase noise profiles. These phase-noise measurements were also used to calculate the noise floor of the CDCLVC1310 (see Table 4).

Table 3. Additive Jitter at 125 MHz Over V_{DD}/V_{DDO} Supply Ranges

V_{DD}/V_{DDO} Supply Range	Input rms Phase Jitter [fs]	Output rms Phase Jitter [fs]	Additive Jitter [fs]
3.3 V/3.3 V	74.4	90.2	51.0
3.3 V/2.5 V	74.4	91.8	53.6
3.3 V/1.8 V	74.4	97.9	63.7
3.3 V/1.5 V	74.4	106.9	76.8
2.5 V/2.5 V	76.5	134.8	111.0
2.5 V/1.8 V	76.5	140.1	117.4
2.5 V/1.5 V	76.5	146.1	124.5

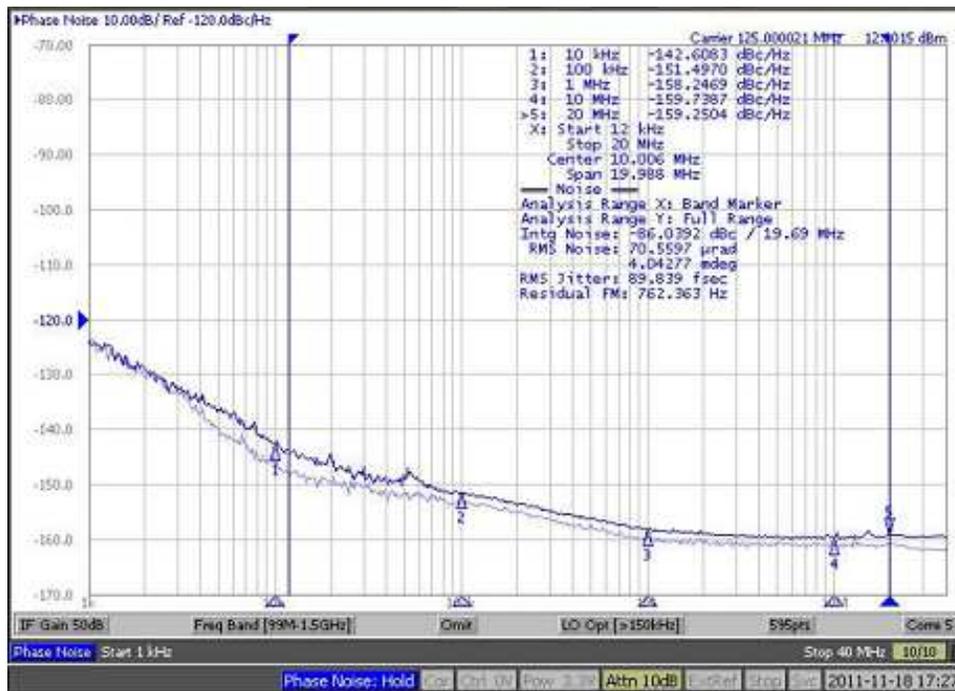


Figure 5. Input Phase Noise (73 fs, Light Blue) and Output Phase Noise (89.8 fs, Dark Blue)

Table 4. Noise Floor at 125 MHz

Phase Noise [dBc/Hz]	f _{offset} [Hz]					
V _{DD} /V _{DDO} Supply Range	10 k	100 k	500 k	1 M	10 M	20 M
3.3 V/3.3 V	-145	-156	-161	-163	-164	-164
2.5 V/2.5 V	-134	-146	-153	-155	-159	-160

The additive jitter measurements were repeated with an 80-MHz and a 100-MHz OCXO. This confirms that the calculated noise floor in Table 4 is correct. Both measurements show a noise floor of -164 dBc/Hz.

The OCXOs are from different vendors:

- 80 MHz: ValpeyFisher VFOV110
- 100 MHz: Vectron OX-4051

Figure 6 and Figure 7 show the input phase noise provided by the two OCXOs and the output phase noise generated by CDCLVC1310.

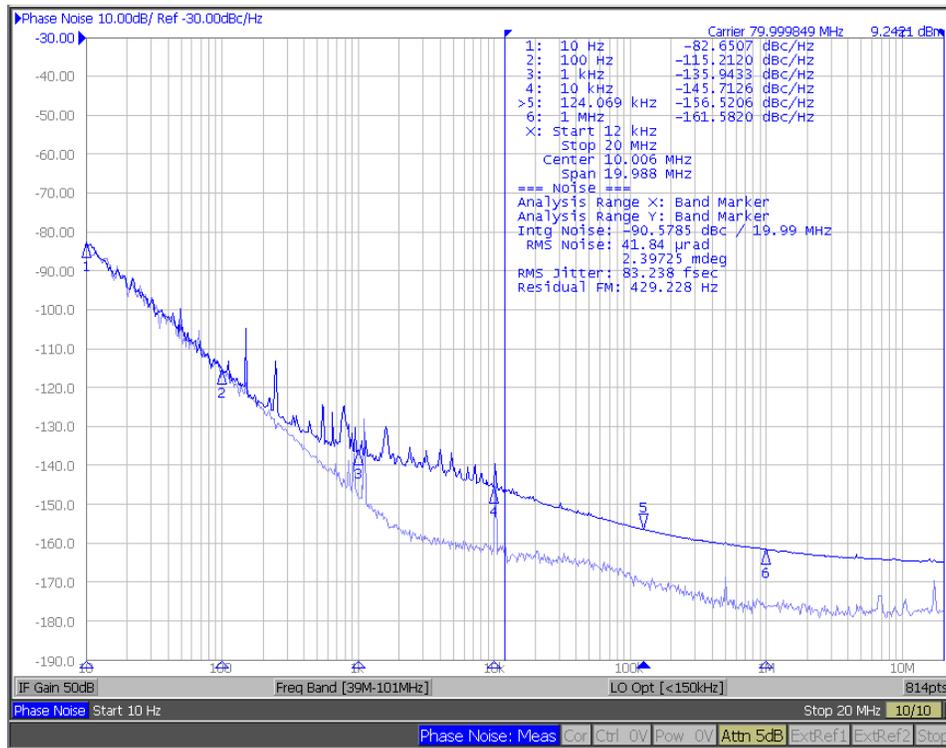


Figure 6. Phase Noise: 80-MHz OCXO (24.9 fs, Light Blue) and Output (83.2 fs, Dark Blue)

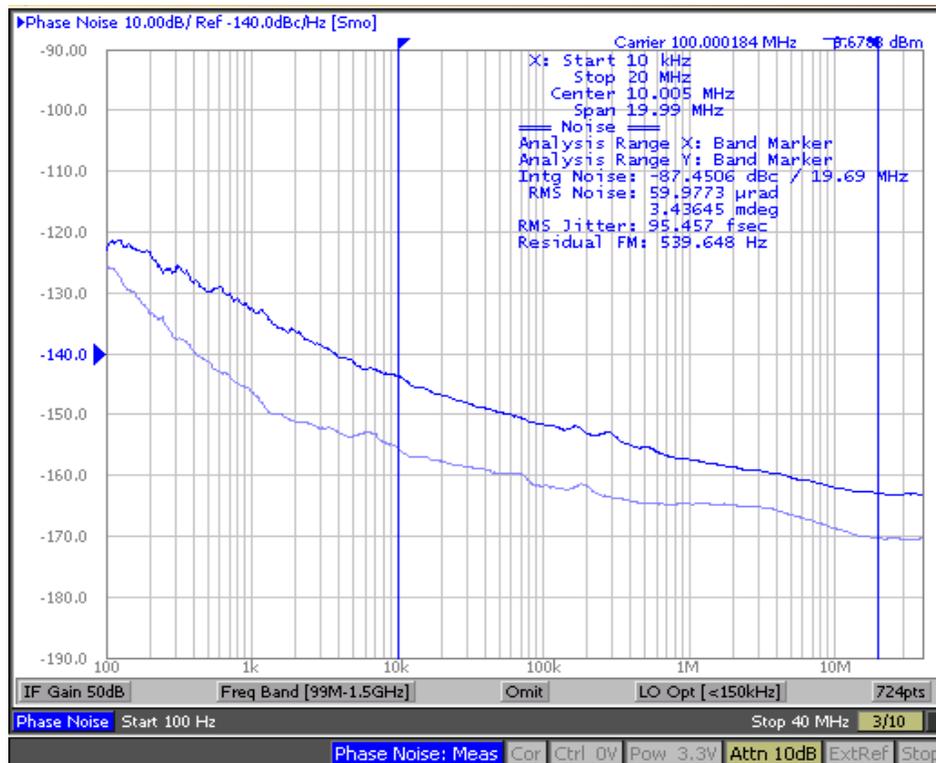


Figure 7. Phase Noise: 100-MHz OCXO (42.66 fs, Light Blue) and Output (95.4 fs, Dark Blue)

3.3 Slew-Rate Impact on Noise Floor

Figure 8 shows the impact of different slew rates on the additive jitter and system-level additive jitter performance.

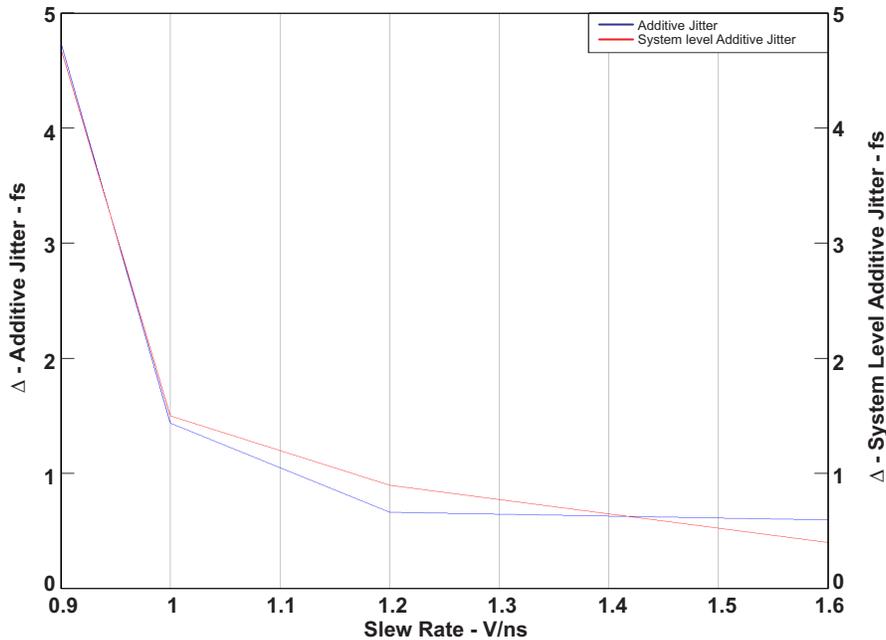


Figure 8. Additive Jitter and System-Level Additive Jitter Impact vs. Slew Rate

4 Crystal Oscillator Phase-Noise Measurements

Section 4.1 shows a summary of the phase-noise measurements of the CDCLVC1310 used as a crystal buffer. Section 4.2 shows the measurement results. The measurements were taken with the standard CDCLVC1310 EVM with a 25-MHz Crystal from ECS Inc. The load capacitance was removed.

The measurement proves that the CDCLVC1310 has an ultralow noise floor of -169 dBc/Hz at 100-kHz offset when used as a crystal buffer.

4.1 Performance Measurement Summary

Table 5 summarizes the phase-noise measurements of the CDCLVC1310 in crystal-buffer mode. It shows the phase noise between a frequency offset of 100-Hz and 5-MHz and the rms phase jitter in a frequency band of 10 kHz to 5 MHz. The measurements were taken with different V_{DD}/V_{DDO} combinations.

Table 5. Crystal Oscillator Phase-Noise Performance with 25-MHz Crystal Resonator

Phase Noise [dBc/Hz]	f_{offset} [Hz]						Rms Phase Jitter [fs] 10 kHz - 5 MHz	
	V_{DD}/V_{DDO} Supply Range	100	1 k	10 k	100 k	1 M		5 M
	3.3 V/3.3 V	-118.2	-138.3	-159.8	-169.2	-170.1	-170.1	64.8
	3.3 V/2.5 V	-118.4	-138.3	-160.3	-168.4	-170.2	-170.1	65.2
	3.3 V/1.8 V	-118.6	-138.3	-159.7	-167.4	-169.1	-169.8	71.4
	3.3 V/1.5 V	-118.3	-137.7	-158.0	-165.8	-168.5	-169.0	79.1
	2.5 V/2.5 V	-113.5	-134.9	-154.9	-165.1	-166.4	-166.6	98.1
	2.5 V/1.8 V	-113.6	-134.9	-155.1	-164.3	-165.9	-166.4	101.9
	2.5 V/1.5 V	-113.2	-134.7	-154.0	-163.2	-165.6	-165.8	109.7

4.2 Measurement Results

Figure 9 through Figure 12 show the measured results for output phase noise with different V_{DD}/V_{DDO} combinations.

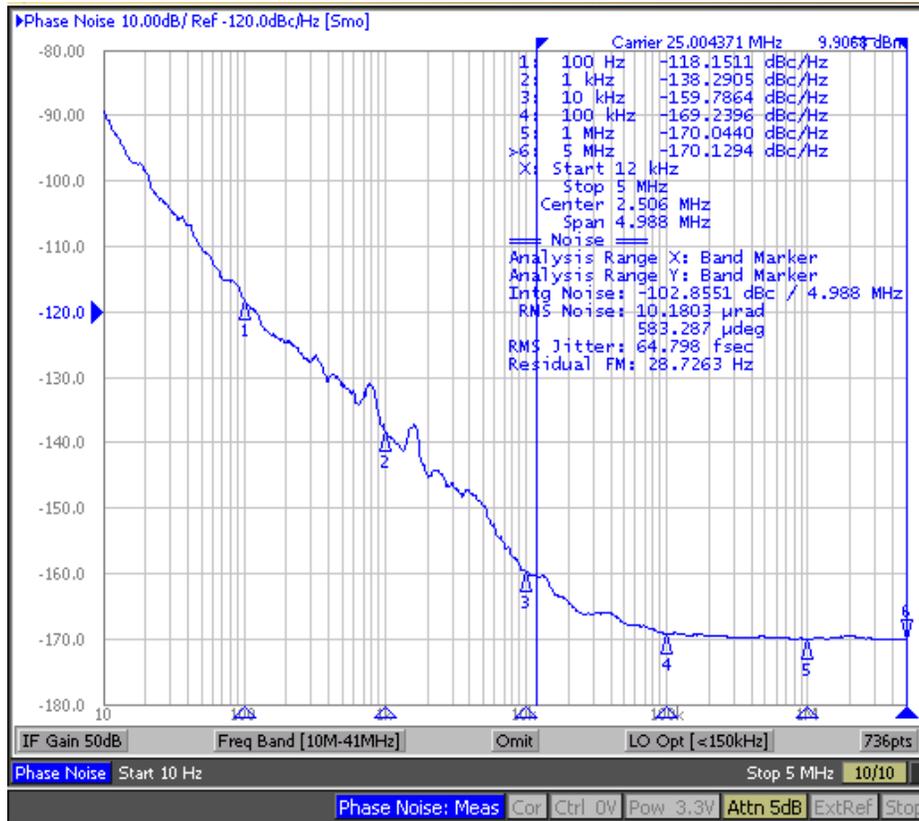


Figure 9. 25-MHz Xtal Output Phase Noise at $V_{DD} = V_{DDO} = 3.3 V$

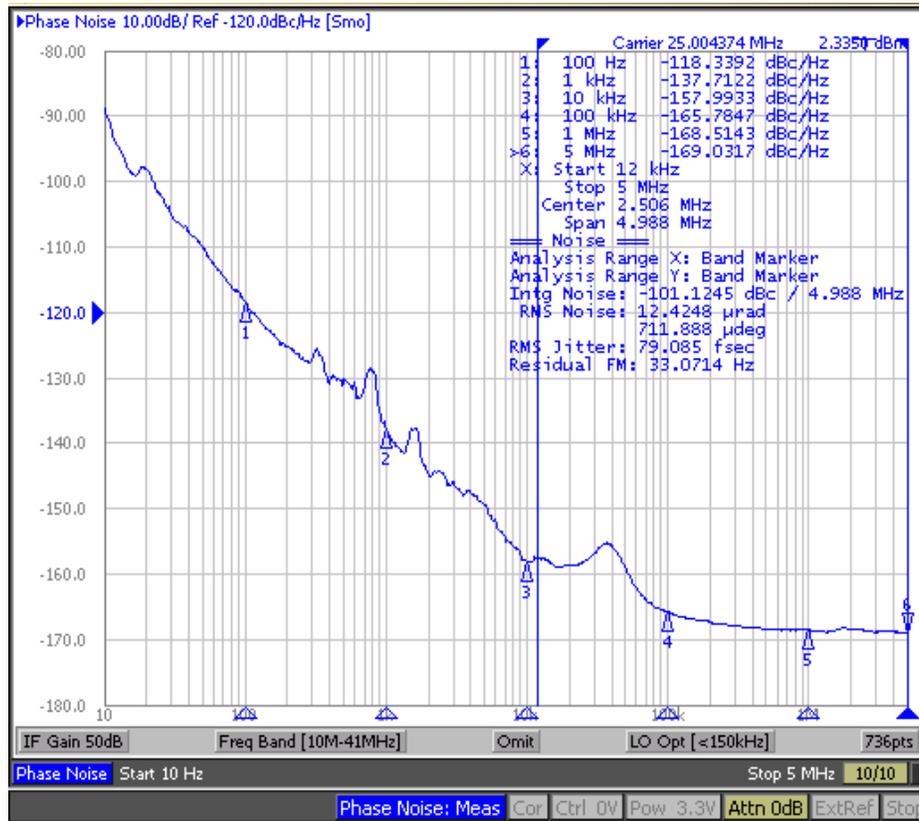


Figure 10. 25-MHz Xtal Output Phase Noise at $V_{DD} = 3.3$ V, $V_{DDO} = 1.5$ V

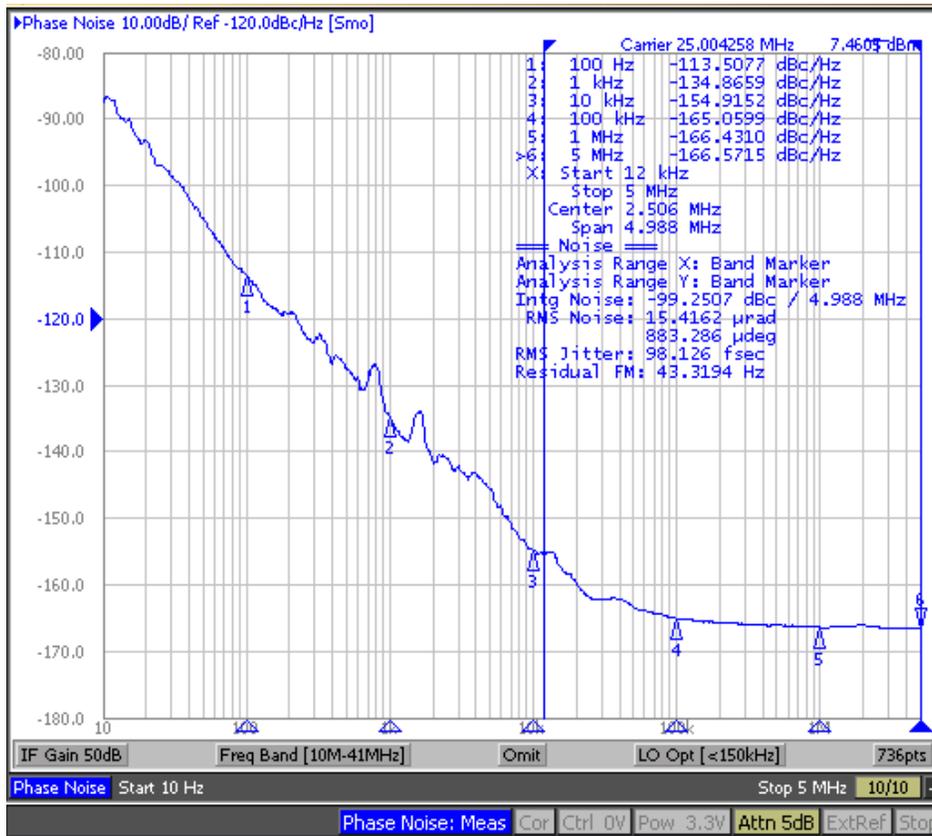


Figure 11. 25-MHz Xtal Output Phase Noise at $V_{DD} = V_{DDO} = 2.5 V$

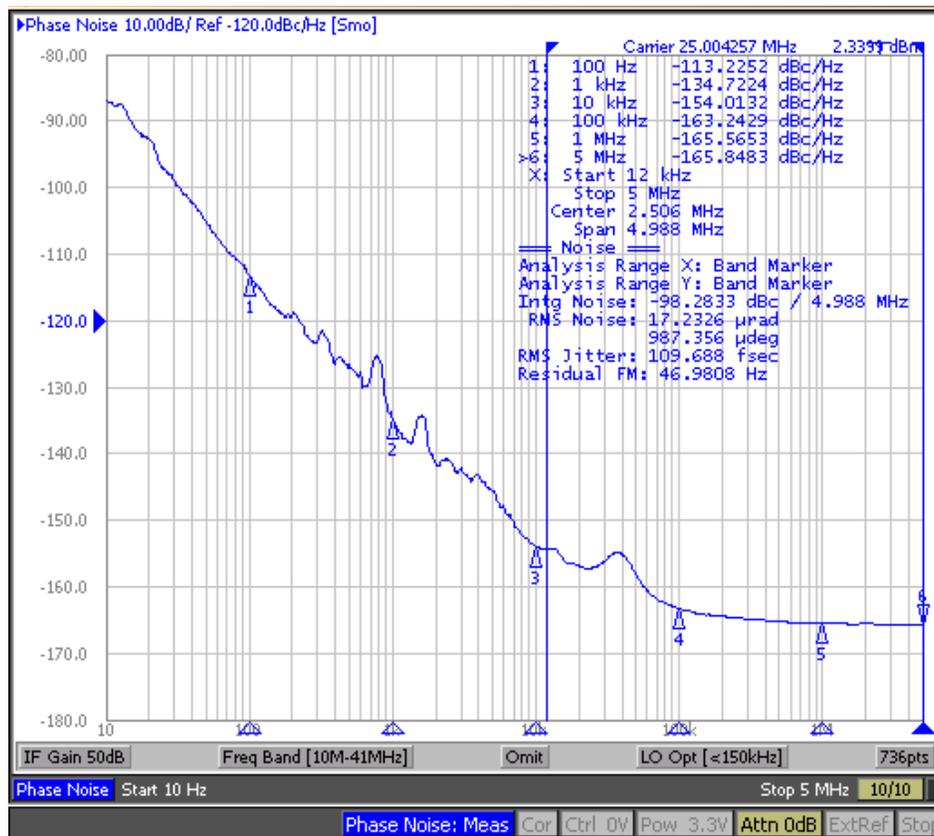


Figure 12. 25-MHz Xtal Output Phase Noise at $V_{DD} = 2.5$ V, $V_{DDO} = 1.5$ V

5 Conclusion

This report demonstrates the ultra low jitter performance of the CDCLVC1310. The device shows a phenomenal phase-noise performance of -170 dBc/Hz in crystal-buffer mode.

5.1 References

1. CDCLVC1310 Evaluation Module ([SCAU046](#))
2. CDCLVC1310 Datasheet ([SCAS917](#))

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