Application Report
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Avoiding ESD and EMI Problems in bq20zxx Battery Pack Electronics

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Battery Management

ABSTRACT

In an increasingly wireless world, electrostatic discharge and electromagnetic interference are both potential issues for portable battery packs. This application report discusses the causes of ESD and EMI issues in battery pack designs and offers solutions for mitigation.

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1 Introduction

Electrostatic discharge (ESD) and electromagnetic interference (EMI) are both potential issues for portable battery packs in an increasingly wireless world. The bq20zxx Impedance Track™ advanced gas gauge family chipsets are based on a low-power microcontroller, which must be protected from severe outside disturbances. For a robust design, careful PCB layout and various mitigation techniques are necessary considerations.

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2 Watery Grave

In the June 23, 2005 edition of EDN magazine, Howard Johnson, Ph.D., wrote an article entitled *Watery Grave*. In the article, he presented the scenario of a person on a lake, in an aluminum canoe, as a terrible thunderstorm was approaching. Given the following three choices, the reader was asked to select the one that would afford the best chance for survival (assuming there would not be a direct hit, which would be fatal in any case).

1. Stay in the canoe
2. Swim to shore
3. Invert the canoe and dive under it for protection (it becomes a Faraday shield)

The correct answer, of course, is to stay in the canoe because the hull of the boat would divert the current around the person. The same strategy could be used to protect integrated circuits inside a battery pack from the miniature lightning of an ESD hit. If the pack could be fitted with a metal case, the solution would be clear. Although the solution with the standard plastic case is not quite so obvious, the method is still the same — the current must be diverted around the unit to be protected.

For an EMI attack, the analogy holds also. RF energy can arrive by either radiation or conduction. Using shielding or bypass techniques, the energy must be diverted around the vulnerable semiconductor structures which can rectify the RF into lower frequency signals able to interfere with system operation.

3 Follow The Electrons

Figure 1 represents the general model for battery pack cells, electronics, and the pack connector. The BMU, or *battery management unit*, is comprised of various integrated circuits and peripheral components in the fuel gauge and safety circuitry design. This model is used to trace the flow of current during an ESD hit and an attack by heavy RF field intensity.

The Li-ion cells, protection FETs, sense resistor, and the pack connector surround the BMU. The single RC filter to the left of the BMU represents one of several connections, which monitor the voltage of each cell. The connections below the BMU represent various connections from the electronics to the common ground point, which is usually located on the PACK— side of the sense resistor. The resistors and zener diode to the right of the BMU represent the typical protection network for one of the communication lines.

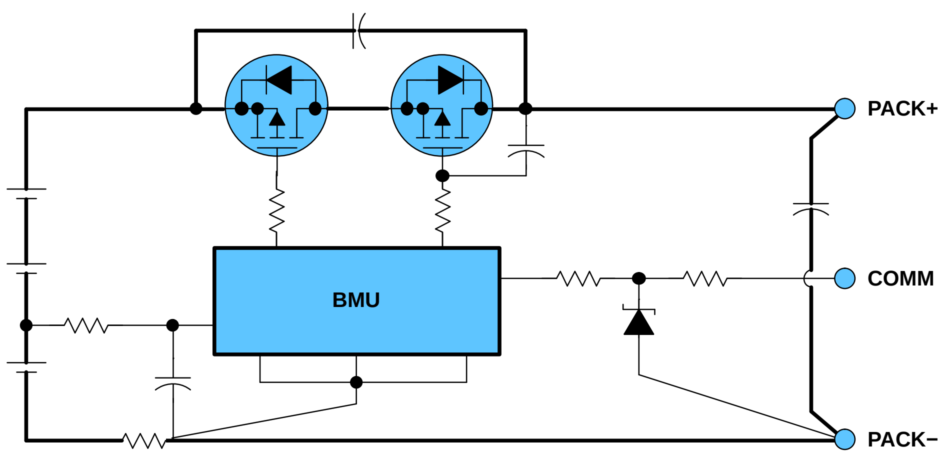

Figure 1. Basic Battery Pack Block Diagram

During an electrostatic discharge from a human body onto the battery pack connector, the current from the charged source tends to flow into the largest available capacitance, which is that of the cells themselves with respect to ground. Naturally, most of the current tends to take the path with the lowest impedance. Wide copper traces, with their low resistance and inductance, become the *diverters*— able to protect the sensitive electronics from grave danger.

In Figure 2 and Figure 3 can be seen the preferred diverting path for a zap to Pack+ and Pack–.

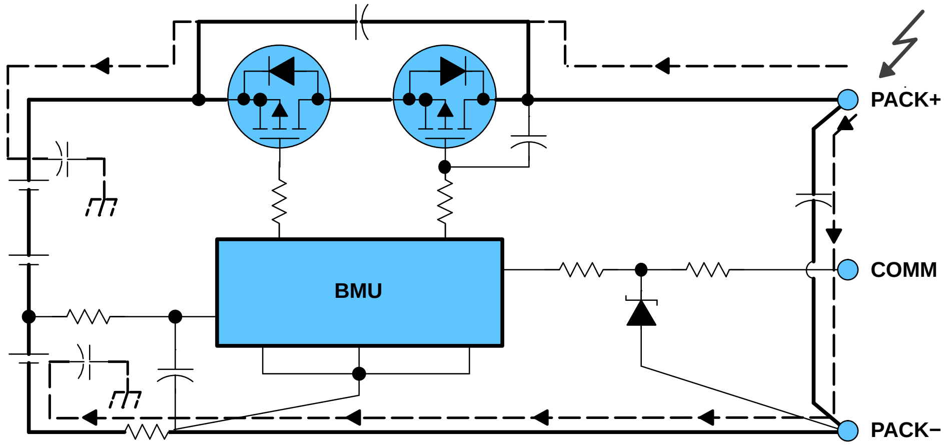

Figure 2. ESD Hit to PACK+ Connector Pin

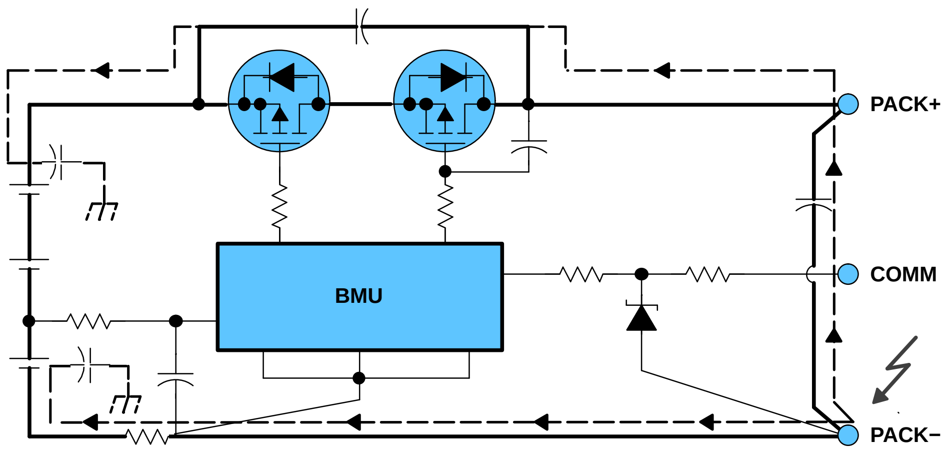

Figure 3. ESD Hit to PACK– Connector Pin

In both cases, the preferred path is similar. The copper to the FETS is wide, but then what? The capacitor (usually two in series in the event that one shorts) across the FETS helps to protect them. But this can only be realized if the copper traces to the capacitor are also wide enough to offer the required low resistance and inductance.

The capacitor (again, usually two in series) between Pack+ and Pack– is equally critical. It is desirable that current from a hit to Pack+ be diverted, as much as possible, away from the FETS and their associated nodes, which lead into the electronics. The copper between the pack connections and the capacitor(s) must be short and thick.

For a zap to a communications pin, again it is desirable to provide a low impedance path to the cell capacitance. In Figure 4, it can be seen that the desired current path is through the first series resistor, through the capacitance of the zener diode, then on to the wide PACK– copper trace. Keeping the zener close to the pack connector and using sufficient copper width ensures that the BMU is protected. In the case of a negative polarity zap, current flows out of the BMU in parallel with current through the zener. The resistor on the BMU side limits the ESD current to a safe level.

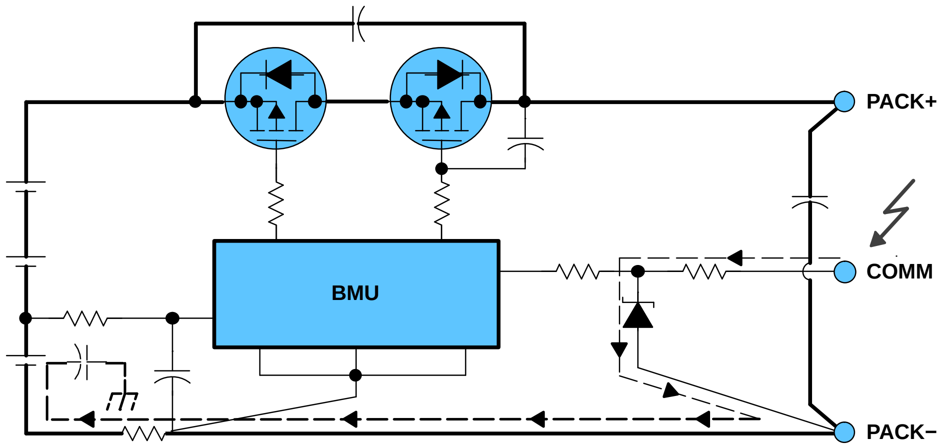

Figure 4. ESD Hit to the CLOCK or DATA Connector Pin

4 Keep ICs Off the Electron Highway

Whereas wide traces help to lower the inductance of copper traces, they still appear quite inductive at ESD pulse frequencies. At high frequencies, the diverting path can act as the primary of a current transformer, injecting unwanted and potentially disruptive currents into adjacent copper loops which feed into sensitive (ultralow power!) electronics.

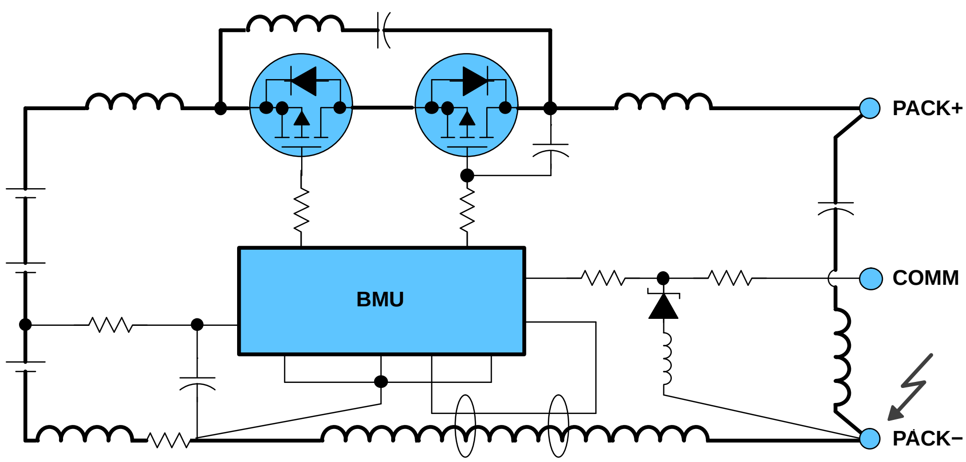

Figure 5. High-Frequency Currents From ESD or Inrush Can Be Inductively Coupled

The best defense against this sort of assault is to physically separate the high-current path from the sensitive electronics. Although this may not be feasible in many battery pack designs, it is an ideal goal for rugged design. High-current inrush pulses and ESD pulses do not mix well with ultralow power electronics. Both inductive and capacitive coupling must be considered in the layout.

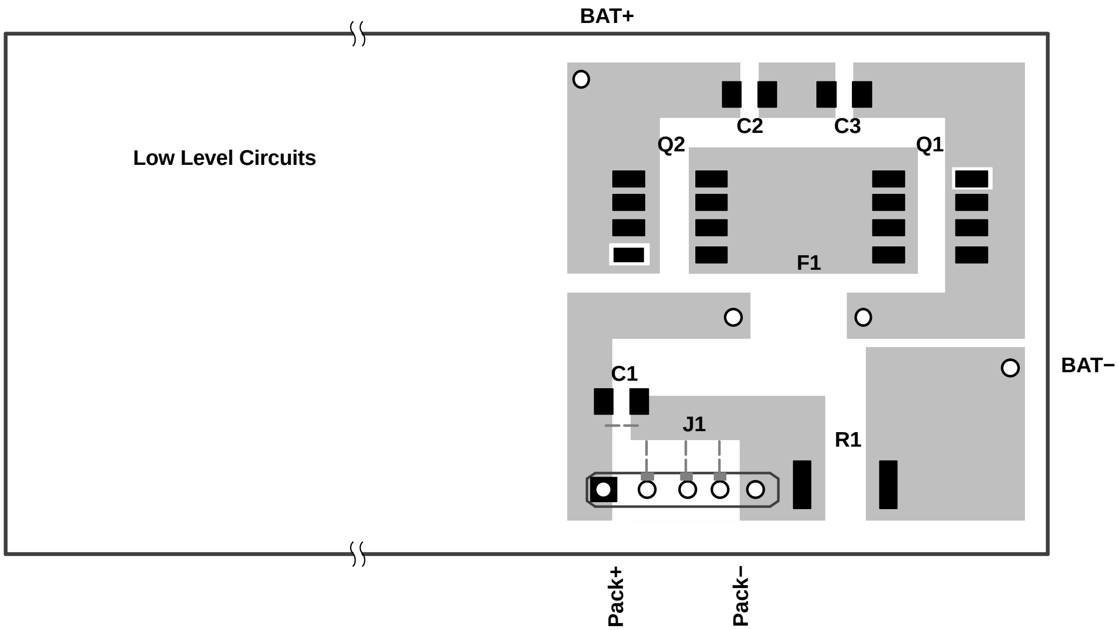

Figure 6. The Ideal Layout Separates the High-Current Path From the Low-Current Electronics

5 Separate Low-Level Ground Systems

Because e = L di/dt, and the derivative of the current is still quite large, significant voltages can be generated along the diverting current path. This is one of the reasons for using a separate low-level ground system with a single-point connection at the sense resistor. This avoids damage to the integrated circuits from circulating currents in the ground system during an ESD event . See Figure 7 and Figure 8.

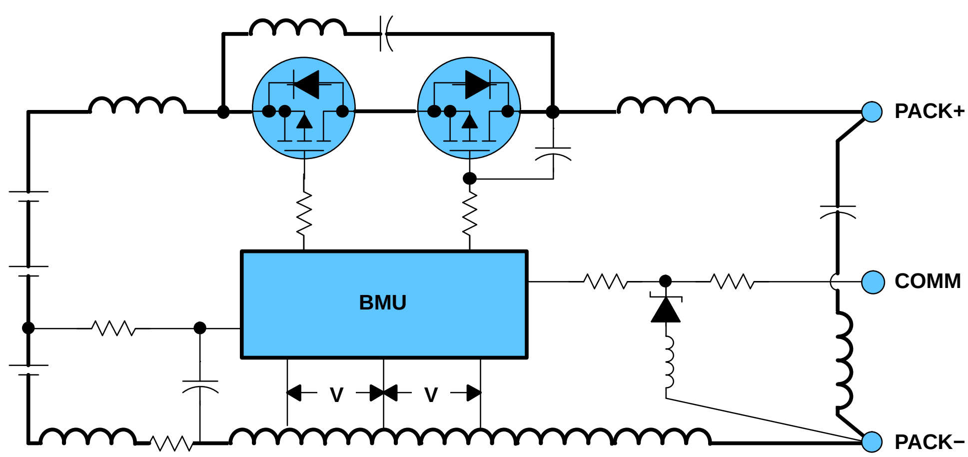

Figure 7. BMU Electronics Can Be Disrupted and Damaged From Circulating Ground Currents

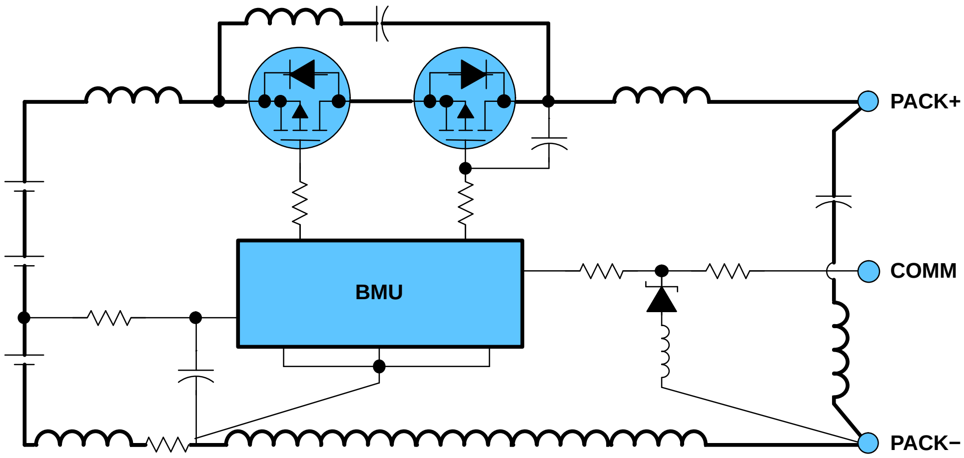

Figure 8. Correct BMU Grounding Is Separated From PACK– Except at the Single Connection at the Sense Resistor

6 Spark Gaps

Spark gaps are quite effective, especially for protecting the communication lines from ESD hits. Use the pattern as shown in the figure below, with a 10-mil (0,2-mm) gap. This provides a voltage breakdown at sea level of about 1500 V. For maximum effectiveness, the spark gaps must be on an outer layer of the PC board and should not be coated with any protective covering.

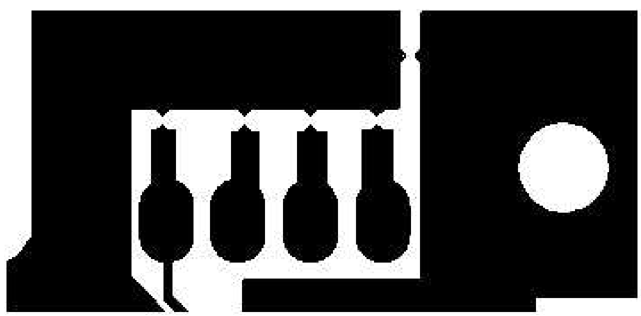

Figure 9. Recommended Spark Gap pattern on Battery Pack Connector

7 RF Bypassing

Perhaps the best way to understand RF interference is with the *crystal set* analogy. All semiconductors behave as diodes and rectify RF signals as with the simple demodulation of AM radio and TV picture transmission. The RF energy can be transported into a battery pack by either radiation or conduction. The cells and their leads can act as an antenna, or copper traces on the PC board itself can be the receiving antenna. Antennas are most effective at multiples of their length. A cell phone operating at 1800 MHz has a fundamental wavelength of 16.7 centimeters. A nice half-wave antenna would be 8.3 cm, while an effective quarter-wave antenna is only 4.2 cm. For this reason, RF testing of a new battery pack design is highly recommended to ensure its dependability in common RF environments, such as cell phones and other two-way radios.

Rectified RF can cause a number of problems including voltage, temperature, and current measurement errors. Also, microcontroller mis-operation and unintended fuse blowing are possible.

If any of these effects are observed during testing, it may be relatively easy to bypass the receiving semiconductor input with one or more small ceramic capacitors. Capacitors in the 68-pF to ~100-pF range have a low shunt impedance at VHF and UHF radio frequencies.

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